CONFIGUM

24950C

Embedded FPGA Module

DTX bus compatible

DATA SHEET

1. Overview

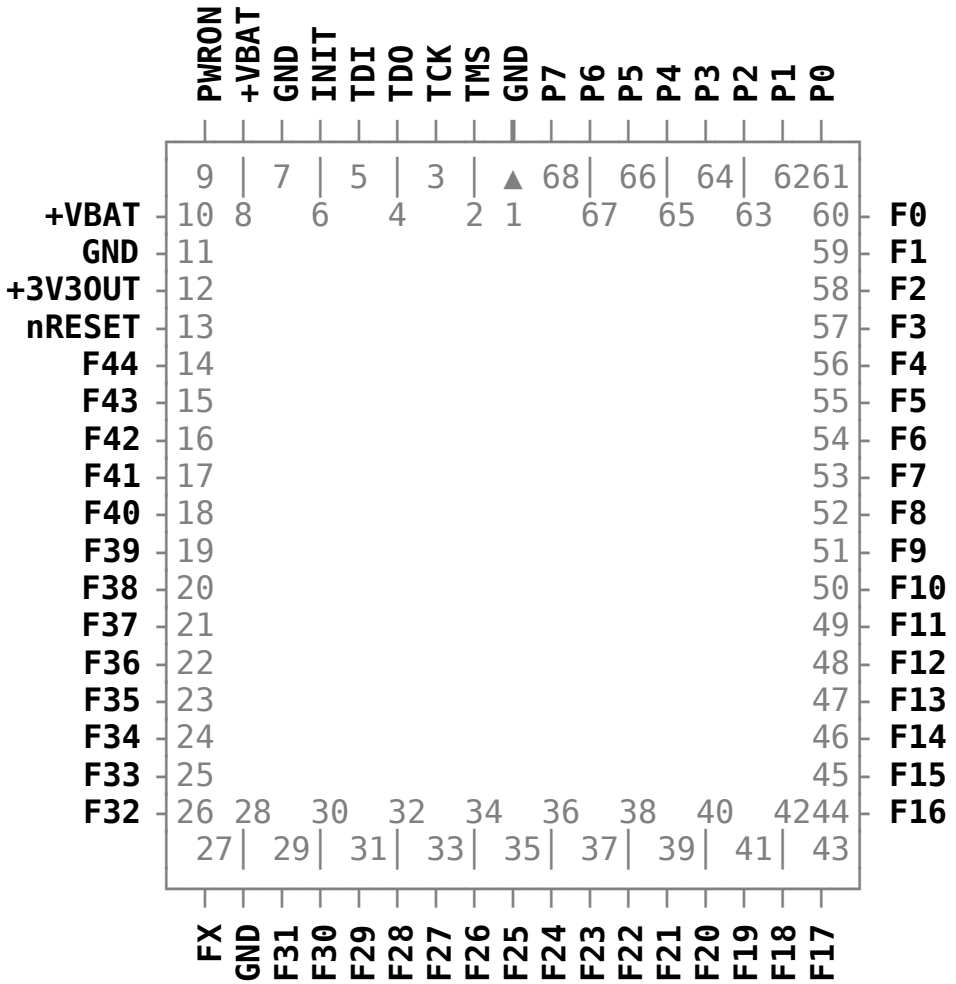
Feature Highlights

68-pin device in standard PLCC68 package; three possible ways of PCB mounting
DTX bus pin-compatible (3.3V logic levels)
Wide range input 5-20V DC power supply with capability of provision to external circuit
Fully self-contained – does not need any external components to run
Xilinx Spartan-6® FPGA with 14579 logic cells (CSG225 package)
Xilinx configuration memory with JTAG support
64 Megabytes DDR memory
micro-SD card connector on board
24MHz crystal oscillator
Four built-in controllable LEDs
Up to 45 FPGA I/O lines plus 8-bit dedicated ADC/DAC/IO front-end
Tag-Connect® pads and reset button
RoHS compliant

Typical Applications

- Soft-core computing
- Robotics
- High-speed data processing
- Hobby and academic projects

2. Pinout



Pinout Summary

Pin	Name	Type	Description
1	GND	P	Ground
2	TMS	I	JTAG TMS line
3	TCK	I	JTAG TCK line
4	TDO	O	JTAG TDO line
5	TDI	I	JTAG TDI line
6	INIT	I	FPGA INIT input; delays initialisation
7	GND	P	Ground
8	+VBAT	P	Positive power lead

9	PWRON	I	Power enabling input (can be connected directly to +VBAT); active high
10	+VBAT	P	Positive power lead
11	GND	P	Ground
12	+3V3OUT	P	+3.3V output from the internal regulator; can be used to supply power to external components and circuits
13	nRESET	I	$\overline{\text{RESET}}$ line; internally biased to +3.3V
14	F44	I,O	FPGA pin B15
15	F43	I,O	FPGA pin H12
16	F42	I,O	FPGA pin F11
17	F41	I,O	FPGA pin G12
18	F40	I,O	FPGA pin F12
19	F39	I,O	FPGA pin G13
20	F38	I,O	FPGA pin F13
21	F37	I,O	FPGA pin H13
22	F36	I,O	FPGA pin G14
23	F35	I,O	FPGA pin E14
24	F34	I,O	FPGA pin B14
25	F33	I,O	FPGA pin C14
26	F32	I,O	FPGA pin H15
27	FX	I,O	FPGA pin J14
28	GND	P	Ground
29	F31	I,O	FPGA pin J13
30	F30	I,O	FPGA pin K13
31	F29	I,O	FPGA pin K12
32	F28	I,O	FPGA pin D15
33	F27	I,O	FPGA pin E15
34	F26	I,O	FPGA pin G15
35	F25	I,O	FPGA pin J15
36	F24	I,O	FPGA pin K15
37	F23	I,O	FPGA pin L14
38	F22	I,O	FPGA pin L15
39	F21	I,O	FPGA pin L12
40	F20	I,O	FPGA pin M15
41	F19	I,O	FPGA pin M13
42	F18	I,O	FPGA pin N15
43	F17	I,O	FPGA pin N14
44	F16	I,O	FPGA pin P15

45	F15	I,O	FPGA pin P14
46	F14	I,O	FPGA pin K11
47	F13	I,O	FPGA pin J11
48	F12	I,O	FPGA pin G11
49	F11	I,O	FPGA pin R11
50	F10	I,O	FPGA pin R10
51	F9	I,O	FPGA pin R9
52	F8	I,O	FPGA pin R8
53	F7	I,O	FPGA pin R6
54	F6	I,O	FPGA pin R5
55	F5	I,O	FPGA pin R4
56	F4	I,O	FPGA pin R13
57	F3	I,O	FPGA pin P13
58	F2	I,O	FPGA pin R7
59	F1	I,O	FPGA pin N11
60	F0	I,O	FPGA pin M11
61	P0	I,O,AI,AO	Universal front-end line 0
62	P1	I,O,AI,AO	Universal front-end line 1
63	P2	I,O,AI,AO	Universal front-end line 2
64	P3	I,O,AI,AO	Universal front-end line 3
65	P4	I,O,AI,AO	Universal front-end line 4
66	P5	I,O,AI,AO	Universal front-end line 5
67	P6	I,O,AI,AO	Universal front-end line 6
68	P7	I,O,AI,AO	Universal front-end line 7

Legend:
I – input with CMOS level
O – digital output
P – power pin
AI – analogue input
AO – analogue output

3. Electrical Parameters

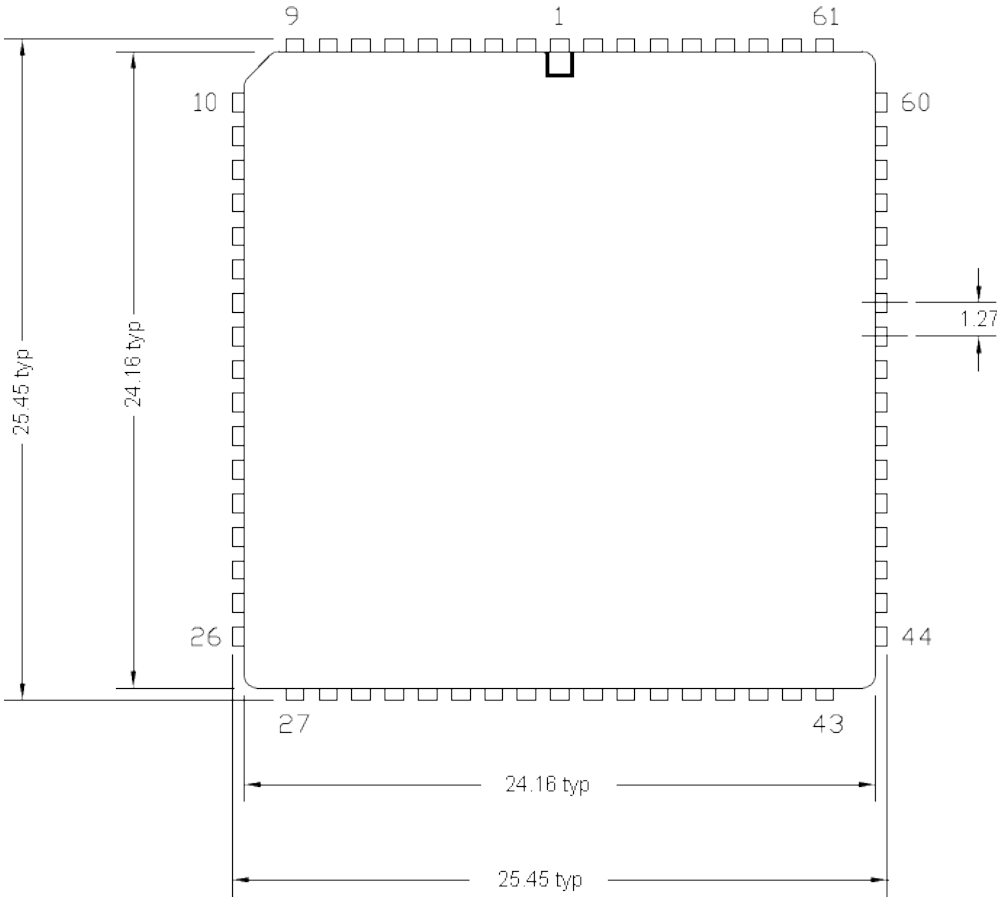
ABSOLUTE MAXIMUM RATINGS:

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

parameter	min	typ	max	units
Power supply voltage range, pin +VBAT with respect to GND	5	9	20	V
Safe load on +3V3OUT pin			250	mA
Parameters of all other functional pins	According to function and IC manufacturer's recommendation			
Operating free-air temperature range	-20		+85	°C
Storage temperature range	-40		+90	°C

4. Mechanical Parameters

Note: *All dimensions are given in millimetres*



5. Internal Schematic