16-BIT CMOS CASCADABLE ALU

IDT7381

FEATURES:

- High-performance 16-bit Arithmetic Logic Unit (ALU)
- 25ns to 55ns clocked ALU operations
- Ideal for radar, sonar or image processing applications
- 74S381 instruction set (8 functions)
- Replaces Gould S614381 or Logic Devices L4C381
- Cascadable with or without carry look-ahead
- Pipeline or flow-through modes
- Internal feedback path for accumulation
- Three-state outputs
- TTL-compatible
- Produced with advanced submicron CMOS technology
- Available in PLCC
- Speeds available: L/25/30/40/55

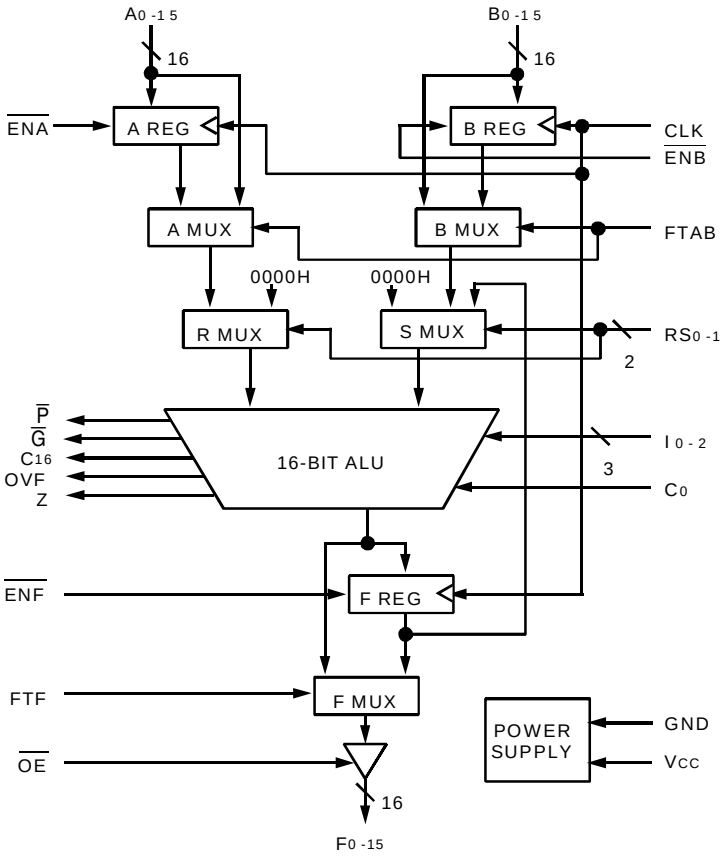
DESCRIPTION:

The IDT7381 is a high-speed cascadable Arithmetic Logic Unit (ALU). These three-bus devices have two input registers, an ultra-fast 16-bit ALU and 16-bit output register. With IDT's high-performance CMOS technology, the IDT7381 can do arithmetic or logic operations in 25ns. The IDT7381 functionally replaces four 54/74S381 four-bit ALUs in a 68-pin package.

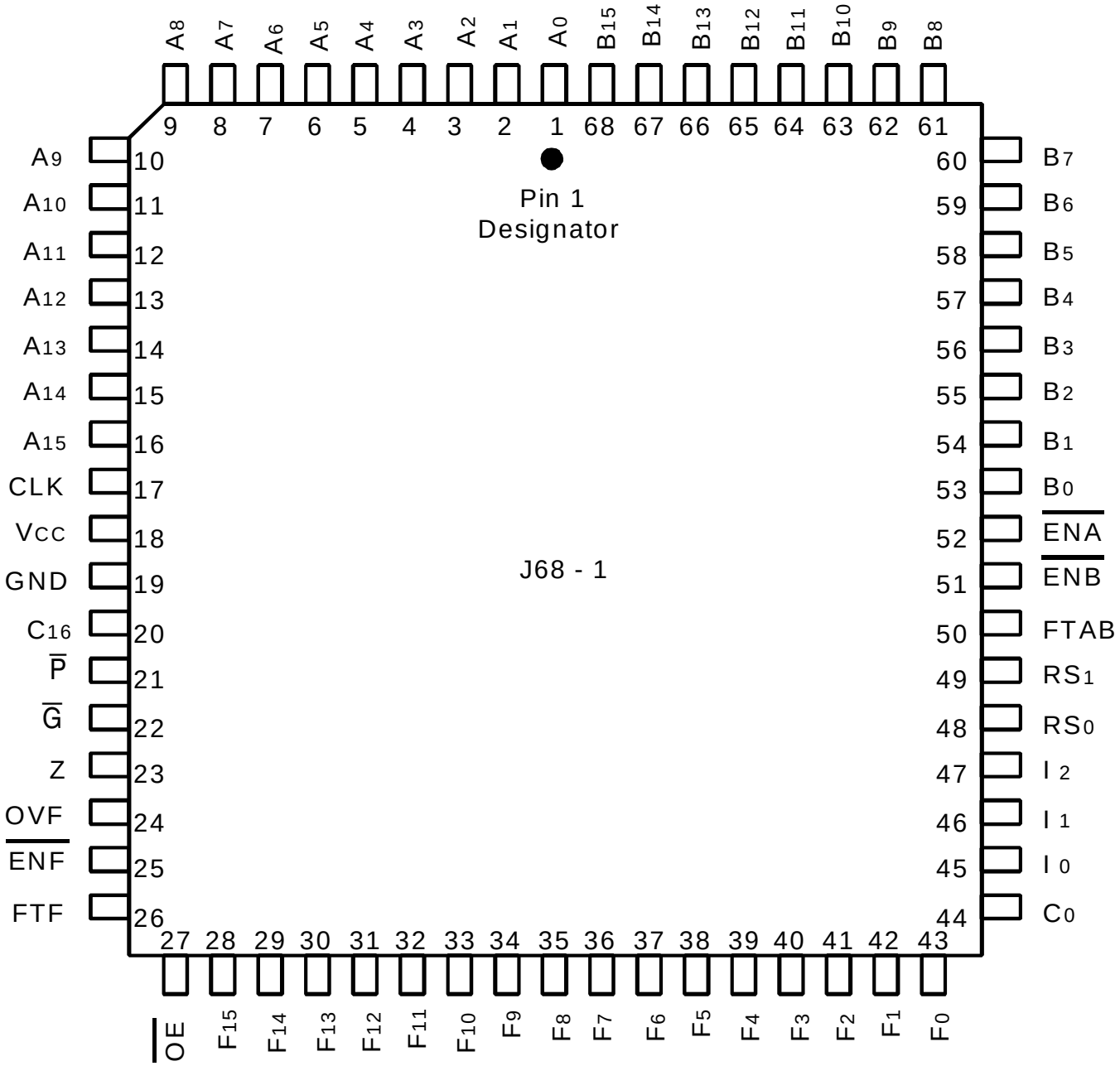
The two input operands, A and B, can be clocked or fed through for flexible pipelining. The F output can also be set into clocked or flow-through mode. An output enable is provided for three-state control of the output port on a bus.

The IDT7381 has three function pins to select 1 of 8 arithmetic or logic operations. The two R and S selection pins determine whether A, B, F or 0 are fed into the ALU. This ALU has carry-out, propagate and generate outputs for cascading using carry look-ahead.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PLCC
TOP VIEW

PIN DESCRIPTION

Pin Name	I/O	Description
A_0 - A_{15}	I	Sixteen–bit data input port.
B_0 - B_{15}	I	Sixteen–bit data input port.
$\overline{ENA}$	I	Register enable for the A input port; active low pin.
$\overline{ENB}$	I	Register enable for the B input port; active low pin.
FTAB	I	Flow–through control pin. When this pin is high, both register A and B are transparent.
F_0 – F_{15}	O	Sixteen–bit data output port.
$\overline{ENF}$	I	Register enable for the F output port; active low pin.
FTF	I	Flow–through control pin. When this pin is high, the F register is transparent.
CLK	I	Clock input.
$\overline{OE}$	I	Output enable control pin. When this pin is high, the output port F is in a high impedance state. When low, the output port F is active.
C_0	I	Carry input. This pin receives arithmetic carries from less significant ALU components in a cascade configuration.
C_{16}	O	Carry output. This pin produces arithmetic carries to more significant ALU components in a cascaded configuration.
OVF	O	This pin indicates a two's complement arithmetic overflow, when high.
Z	O	This pin indicates a zero output result, when high.
RS_0 – RS_1	I	Two control pins used to select input operands for the R and S multiplexers.
I_0 - I_2	I	Three control pins to select the ALU function performed.
P	O	Indicates the carry propagate output state to the ALU.
$\overline{G}$	O	Indicates the carry generate output state to the ALU.
V_{CC}		Power supply pin, 5V.
GND		Ground pin, 0V.

R AND S MUX TABLE

RS_1	RS_0	R Mux	S Mux
0	0	A	F
0	1	A	0
1	0	0	B
1	1	A	B

ALU FUNCTION TABLE

I_2	I_1	I_0	Function
0	0	0	F = 0
0	0	1	F = $\overline{R}$ + S + C_0
0	1	0	F = R + $\overline{S}$ + C_0
0	1	1	F = R + S + C_0
1	0	0	F = R xor S
1	0	1	F = R or S
1	1	0	F = R and S
1	1	1	F = all 1's

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max.	Unit
V_{TERM}	Terminal Voltage with Respect to Ground	–0.5 to V_{CC} + 0.5	V
V_{CC}	Power Supply Voltage	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–55 to +125	° C
I_{OUT}	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Under no circumstances should an input of an I/O Pin be greater than V_{CC} + 0.5V.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Pkg.	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	PGA	10	pF
			PLCC	5	
C_{OUT}	Output Capacitance	V_{OUT} = 0V	PGA	12	pF
			PLCC	7	

NOTE:
1. This parameter is sampled at initial characterization and is not production tested.

DC ELECTRICAL CHARACTERISTICS

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7V		—	—	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.5V		—	—	–10	µA
I_{OS}(3)	Short Circuit Current	V_{CC} = Max., V_{OUT} = GND		–20	—	–100	mA
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.5V	—	–0.1	–20	µA
			V_O = 2.7V	—	–0.1	20	
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –4mA	2.4	—	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8mA	—	—	0.5	V

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} =GND or V_{CC}		—	2	6	mA
ΔI_{CC}[3]	Quiescent Power Supply Current TTL Input HIGH	V_{CC} = Max. V_{IN} = 3.4V		—	0.5	1	mA/ input
I_{CCD}[4]	Dynamic Power Supply Current	V_{CC} = Max. Outputs disabled V_{IN} = GND or V_{CC} Mode: FTAB = FTF = 1		—	15	48	µA/ MHz
I_{CCD1}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Disabled All Data Inputs Disabled f_i = 10MHz, f_{CP} = 10MHz 50% Duty Cycle V_{IL} = GND, V_{IH} = V_{CC} Mode: FTAB = FTF = 1		—	20	33	mA
I_{CCD2}[6]	Dynamic Power Supply Current	V_{CC} = Max. Outputs Enabled. (CL = 50pF) All Data Inputs Sw itching f_i = 10MHz, f_{CP} = 10MHz 50% Duty Cycle V_{IL} = GND, V_{IH} = V_{CC} Mode: FTAB = FTF = 1		—	40	60	mA
I_C[7]	Total Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC} All Data Inputs Switching f_i = 10MHz, f_{CP} = 10MHz 50% Duty Cycle	Outputs Disabled	—	22	39	mA
			Outputs Enabled	—	42	76	mA

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived from I_{CCD1} for use in Total Power Supply calculations.
5. Total power supply current is calculated as follows:
   $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.
6. This parameter is not production tested but is an indicator of the power dissipated with outputs loaded.
7. Values for these conditions are examples of the I_C formula in note 5 above. These are guaranteed but not tested.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 5%, T_A = 0°C to +70°C)

Maximum Combinational Propagation Delays									
	IDT7381L25				IDT7381L30				
From Input	F_{0-15}	$\overline{P}$, $\overline{G}$, N	Z,OVF	C_{16}	F_{0-15}	$\overline{P}$, $\overline{G}$, N	Z,OVF	C_{16}	Unit
FTAB = 0, FTF = 0									
CLK	13	22	26	22	20	28	30	28	ns
C_0	—	—	16	16	—	—	20	20	ns
I_{0-2}, RS_0, RS_1	—	22	22	22	—	28	28	28	ns
FTAB = 0, FTF = 1									
CLK	27	22	26	22	33	28	30	28	ns
C_0	22	—	16	16	28	—	20	20	ns
I_{0-2}, RS_0, RS_1	22	22	22	22	28	28	28	28	ns
FTAB = 1, FTF = 0									
A_0–A_{15}, B_0–B_{15}	—	18	25	22	—	24	30	28	ns
CLK	13	—	—	—	19	—	—	—	ns
C_0	—	—	16	16	—	—	20	20	ns
I_{0-2}, RS_0, RS_1	—	22	22	22	—	28	28	28	ns
FTAB = 1, FTF = 1									
A_0–A_{15}, B_0–B_{15}	26	18	25	22	32	24	30	28	ns
C_0	22	—	16	16	28	—	20	20	ns
I_{0-2}, RS_0, RS_1	22	22	22	22	28	28	28	28	ns

Maximum Combinational Propagation Delays									
	IDT7381L40				IDT7381L55				
From Input	F_{0-15}	$\overline{P}$, $\overline{G}$, N	Z,OVF	C_{16}	F_{0-15}	$\overline{P}$, $\overline{G}$, N	Z,OVF	C_{16}	Unit
FTAB = 0, FTF = 0									
CLK	26	30	44	32	32	38	53	36	ns
C_0	—	—	28	20	—	—	34	22	ns
I_{0-2}, RS_0, RS_1	—	32	34	35	—	42	42	42	ns
FTAB = 0, FTF = 1									
CLK	46	30	44	32	56	38	53	36	ns
C_0	30	—	28	20	37	—	34	22	ns
I_{0-2}, RS_0, RS_1	40	32	34	35	55	42	42	42	ns
FTAB = 1, FTF = 0									
A_0–A_{15}, B_0–B_{15}	—	30	40	32	—	36	46	37	ns
CLK	26	—	—	—	32	—	—	—	ns
C_0	—	—	28	20	—	—	34	22	ns
I_{0-2}, RS_0, RS_1	—	32	34	35	—	42	42	42	ns
FTAB = 1, FTF = 1									
A_0–A_{15}, B_0–B_{15}	40	30	40	32	55	36	46	37	ns
C_0	30	—	28	20	37	—	34	22	ns
I_{0-2}, RS_0, RS_1	40	32	34	35	55	42	42	42	ns

NOTES:
1. Only for FTF = 0.
2. Minimum propagation delays are not production tested but guaranteed to be greater than or equal to 3ns.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 5%, T_A = 0°C to +70°C) - (Cont'd.)

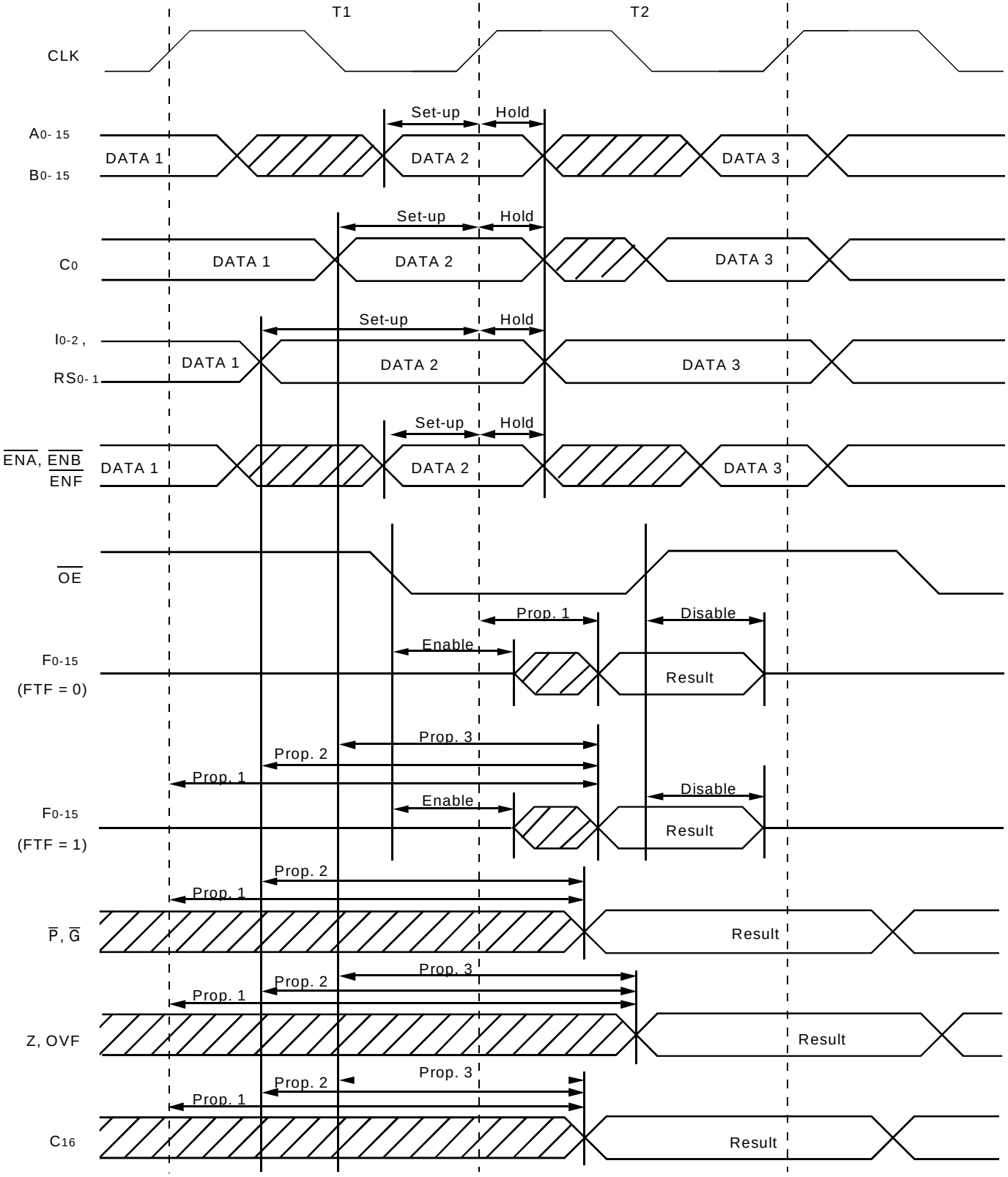
Minimum Set-up and Hold Times Relative to Clock (CLK)									
	IDT7381L25		IDT7381L30		IDT7381L40		IDT7381L55		
Input	Set-up	Hold	Set-up	Hold	Set-up	Hold	Set-up	Hold	Unit
FTAB = 0, FTF = X									
A_0–A_{15}, B_0–B_{15}	6	0	6	0	6	0	8	0	ns
C_0 (1)	16	0	16	0	16	0	21	0	ns
I_{0-2}, RS_0, RS_1 (1)	24	0	29	0	32	0	44	0	ns
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	6	0	6	0	6	0	8	0	ns
FTAB = 1, FTF = 0									
A_0–A_{15}, B_0–B_{15}	16	0	25	0	28	0	35	0	ns
C_0	16	0	16	0	16	0	21	0	ns
I_{0-2}, RS_0, RS_1	24	0	29	0	32	0	44	0	ns
$\overline{ENF}$	6	0	6	0	6	0	8	0	ns

Minimum Clock Cycle Times and Pulse Widths					
Parameter	IDT7381L25	IDT7381L30	IDT7381L40	IDT7381L55	Unit
Clock LOW Time	6	8	10	14	ns
Clock HIGH Time	6	8	10	14	ns
Clock Period	20	25	34	43	ns

Maximum Output Enable/Disable Times					
Parameter	IDT7381L25	IDT7381L30	IDT7381L40	IDT7381L55	Unit
Enable Time	10	15	18	20	ns
Disable Time	10	15	18	20	ns

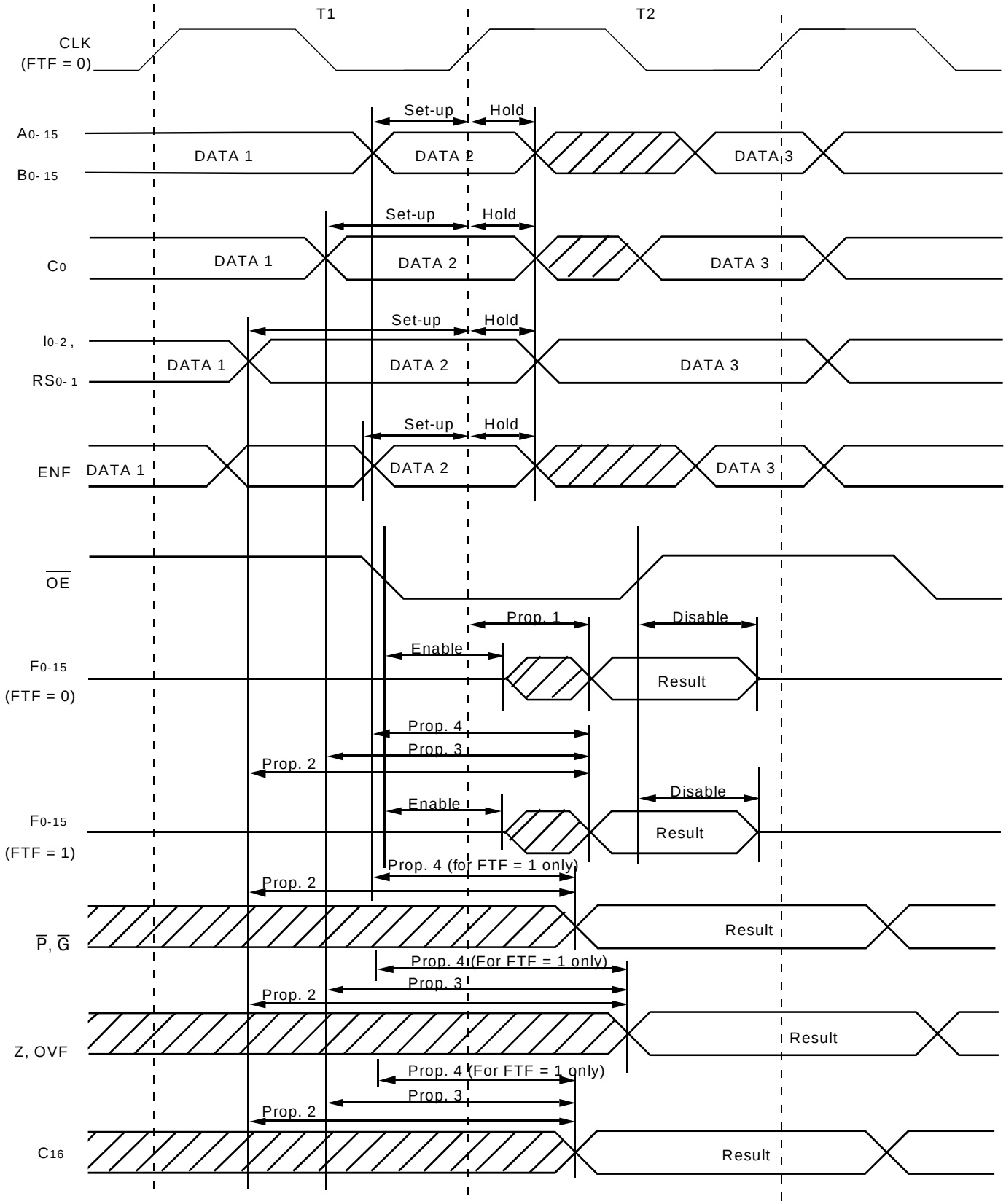
NOTES:
1. Only for FTF = 0.
2. Minimum propagation delays are not production tested but guaranteed to be greater than or equal to 3ns.

WAVEFORMS FOR FTAB = 0, FTF = X



Prop. 1: Propagation delay with respect to the CLK.
Prop. 2: Propagation delay with respect to I_{0-2}, RS_{0-2}.
Prop. 3: Propagation delay with respect to C0.

WAVEFORMS FOR FTAB = 1, FTF = X



Prop. 1: Propagation delay with respect to the CLK.
Prop. 2: Propagation delay with respect to I_{0-2}, RS_{0-2}.
Prop. 3: Propagation delay with respect to C0.
Prop. 4: Propagation delay with respect to A, B.

PROPAGATION DELAY CALCULATIONS FOR TWO IDT7381S

From Input	To Output		To Set PUT Time
	F_{0-15}	Flags [1]	Relative to Clock (CLK)
FTAB = 0, FTF = 0			
CLK	As in 16-bit case	(Clk → C_{16}) + (C_0 → flag)	. . . .
C_0	. . . .	(C_0 → C16) + (C_0 → flag)	(C_0 → C_{16}) + (C_0 set–up time)
I_{0-2}, RS_{0-1}	. . . .	(I_{0-2}, RS_{0-1} → C_{16}) + (C_0 → flag)	(I_{0-2}, RS_{0-1} → C_{16}) + (C_0 set–up time)
A_{0-15}, B_{0-15}	. . . .	. . . .	As in 16-bit case
ENA, ENB,ENF	. . . .	. . . .	As in 16-bit case
FTAB = 0, FTF = 1			
CLK	(Clk → C_{16}) + (C_0 → F_{0-15})	(Clk → C_{16}) + (C_0 → flag)	. . . .
C_0	(C_0 → C_{16}) + (C_0 → F_{0-15})	(C_0 → C_{16}) + (C_0 → flag)	(C_0 → C_{16}) + (C_0 set–up time)
I_{0-2}, RS_{0-1}	(I_{0-2}, RS_{0-1} → C_{16}) + (C_0 → F_{0-15})	(I_{0-2}, RS_{0-1} → C_{16}) + (C_0 → flag)	(I_{0-2}, RS_{0-1} → C_{16}) + (C_0 set–up time)
A_{0-15}, B_{0-15}	. . . .	. . . .	As in 16-bit case
ENA, ENB,ENF	. . . .	. . . .	As in 16-bit case
FTAB = 1, FTF = 0			
CLK	As in 16-bit case	. . . .	. . . .
C_0	. . . .	(C_0 → C_{16}) + (C_0 → flag)	(C_0 → C_{16}) + (C_0 set–up time)
I_{0-2}, RS_{0-1}	. . . .	(I_{0-2}, RS_{0-1} → C_{16}) + (C_0 → flag)	(I_{0-2}, RS_{0-1} → C_{16}) + (C_0 set–up time)
A_{0-15}, B_{0-15}	. . . .	(A_{0-15}, B_{0-15} → C_{16}) + (C_0 → flag)	As in 16-bit case
ENA, ENB,ENF	. . . .	. . . .	As in 16-bit case
FTAB = 0, FTF = 1			
CLK	Don't care condition	Don't care condition	. . . .
C_0	(C_0 → C_{16}) + (C_0 → F_{0-15})	(C_0 → C_{16}) + (C_0 → flag)	. . . .
I_{0-2}, RS_{0-1}	(I_{0-2}, RS_{0-1} → C_{16}) + (C_0 → F_{0-15})	(I_{0-2}, RS_{0-1} → C_{16}) + (C_0 → flag)	. . . .
A_{0-15}, B_{0-15}	(A_{0-15}, B_{0-15} → C_{16}) + (C_0 → F_{0-15})	(A_{0-15}, B_{0-15} → C_{16}) + (C_0 → flag)	. . . .
ENA, ENB,ENF	. . . .	. . . .	. . . .

NOTE:
1. Flags are $\overline{P}$, $\overline{G}$, OVF, Z and C_{16}.

CASCADING THE IDT7381

Some applications require 32-bit or wider input operands. Cascading is the hardware solution. It provides a high speed alternative in handling more than 16-bit wide operands.

1. Cascading the IDT7381

Cascading to 32-bit wide operands takes only two IDT7381s and no external hardware. However, cascading to data widths greater than 32-bit can be done in two ways: without external hardware (slow method) or by using a carry look ahead generator.

a) Cascading the IDT7381 without a carry-look-ahead generator: (Figures 1 and 2)
   1. Connect the C_{16} output of the least significant device into the C_0 input of the next most significant device.
   2. Common lines to all devices are: RS_{0-1}, I_{0-2}, Clk, FTF, FTAB, $\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$.
   3. Take OVF, C_{16}, $\overline{P}$, $\overline{G}$ of the most significant device as valid.
   4. The system's zero flag (Z) is obtained by ANDing all zero flag results.

b) Cascading three or more IDT7381s with carry-look-ahead (CLA) generator: (Figure 3)
   1. Connect the $\overline{P}$ and $\overline{G}$ outputs of each device to the CLA generator's corresponding inputs.
   2. Take the CLA generator outputs into the C_0 inputs of each device (except for the least significant one).
   3. Common lines to all devices are: RS_{0-1}, I_{0-2}, Clk, FTF, FTAB, $\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$.
   4. Take OVF, C_{16}, $\overline{P}$, $\overline{G}$ of the most significant device as valid.
   5. Carry-in to the system should be connected to the C_0 input of the least significant device and also to the CLA generator.

2. Time Delay Considerations

Once cascading has taken place, time delays may become critical in high performance systems. Our main interest here is focused on "propagation delays", i.e. calculating the time required for an input signal to propagate through several cascaded devices up to a specific output in another device within the cascaded system.

Propagation Delay

The propagation delay *for two devices* between the input and output of interest (input to output delay) is done as follows:

1. Calculate delay between the input and C_{16} in the first device.
2. Calculate delay between C_0 and the output in the second device.
3. Add both results.

The following table is an example on how to build a propagation delay table for all inputs in a 32-bit IDT7381 cascaded system.

Propagation delay calculations can be extended to *n–cascaded* devices as the sum of the delays in all devices between the input and output of interest. That is:

$(Input)_1 \rightarrow (C16)_1 = t_1$

...

$(C_0)_i \rightarrow (C_{16})_i = t_i$

$(C_0)_{i+1} \rightarrow (C_{16})_{i+1} = t_{i+1}$

...

$(C_0)_n \rightarrow (Output)_n = t_n$

Where the subscript i denotes the device number and the arrow ($\rightarrow$) represents the delay in between. Notice that i + 1 is the immediate upper device from device i. Adding the delays t_i we get:

Propagation delay = $t_1 + t_2 + ... + t_i + t_{i+1} + ... + t_n$

Total Delay

As seen from Figure 8, the propagation delay is within the IDT7381 devices only. A complete analysis should also include the delay associated with the transmission line Li (which depends on the line length and its impedance). This line delay should then be added to the propagation delay to obtain the total delay for the cascaded system:

Total delay = Propagation delay + Transmission line delay

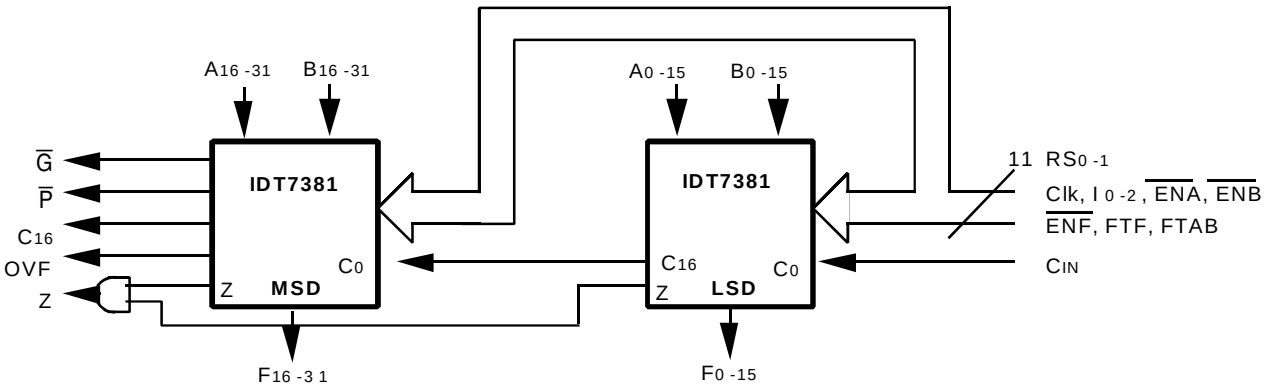


Figure 1. Cascading Two IDT7381s to 32 Bits

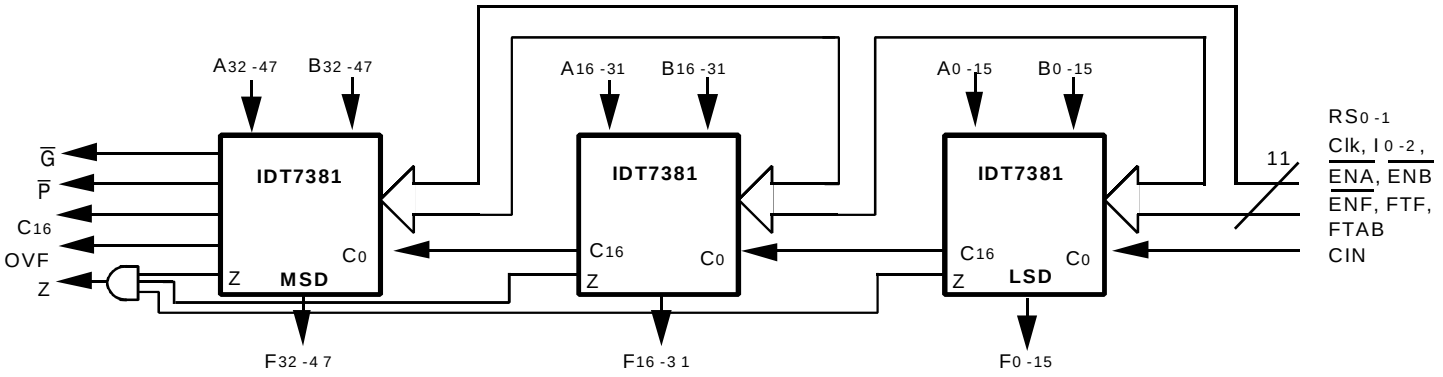


Figure 2. Cascading Three IDT7381s to 48 Bits Wide without a Carry-lookahead Generator

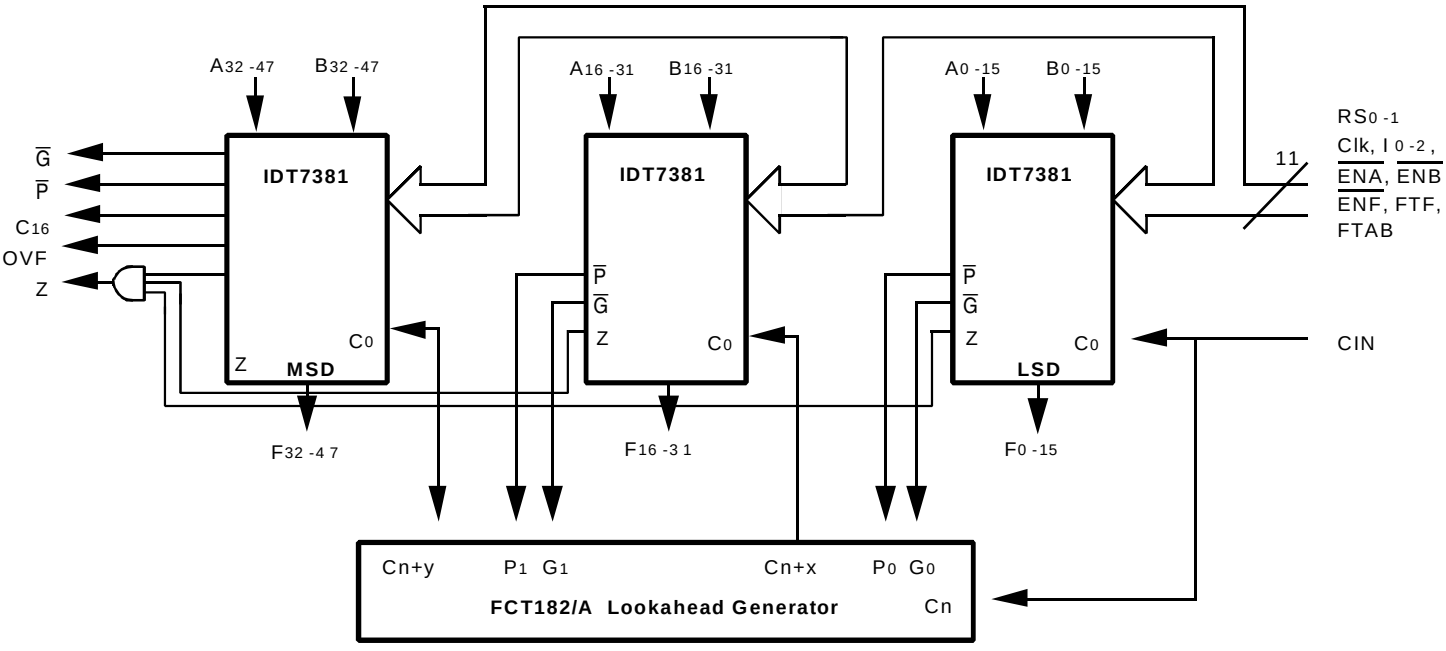


Figure 3. Cascading Three IDT7381s to 48 Bits Wide with a Carry-lookahead Generator

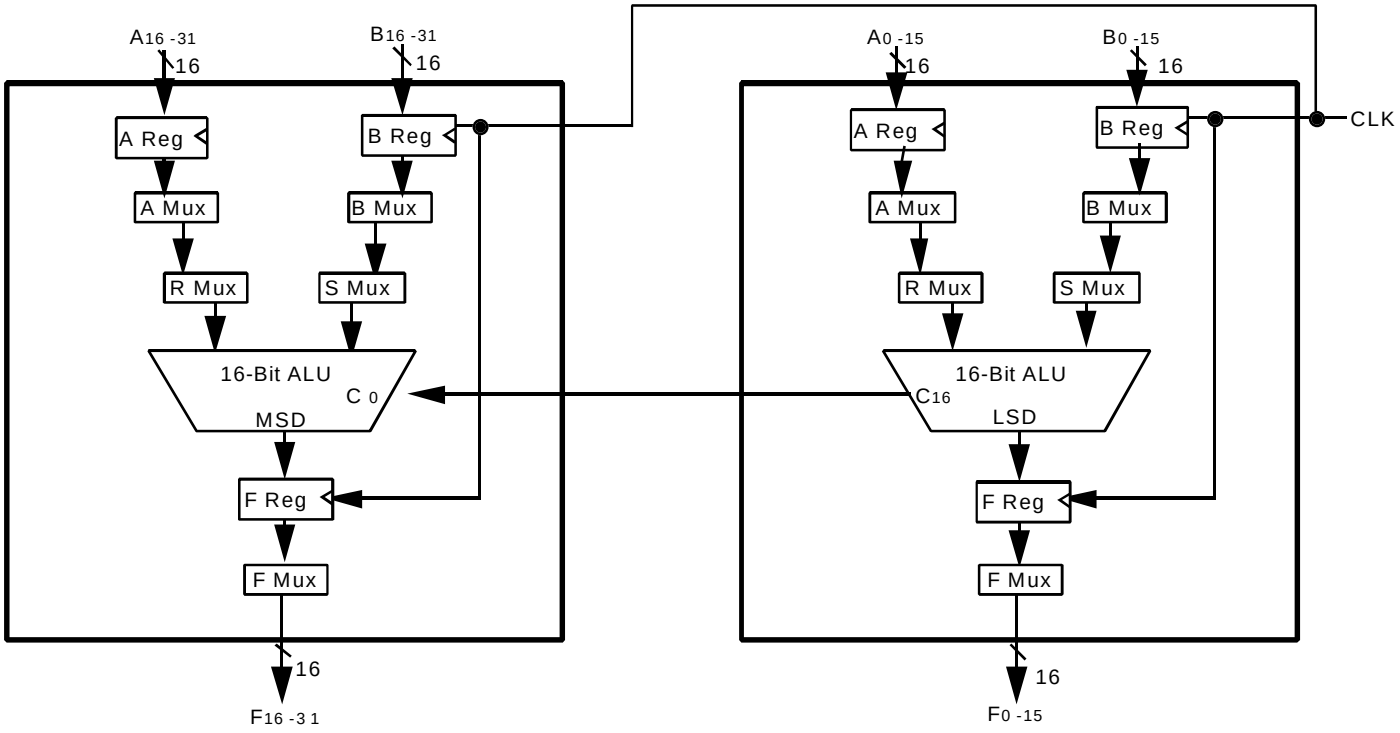


Figure 4. 32-Bit Configuration for FTAB = 0, FTF = 0

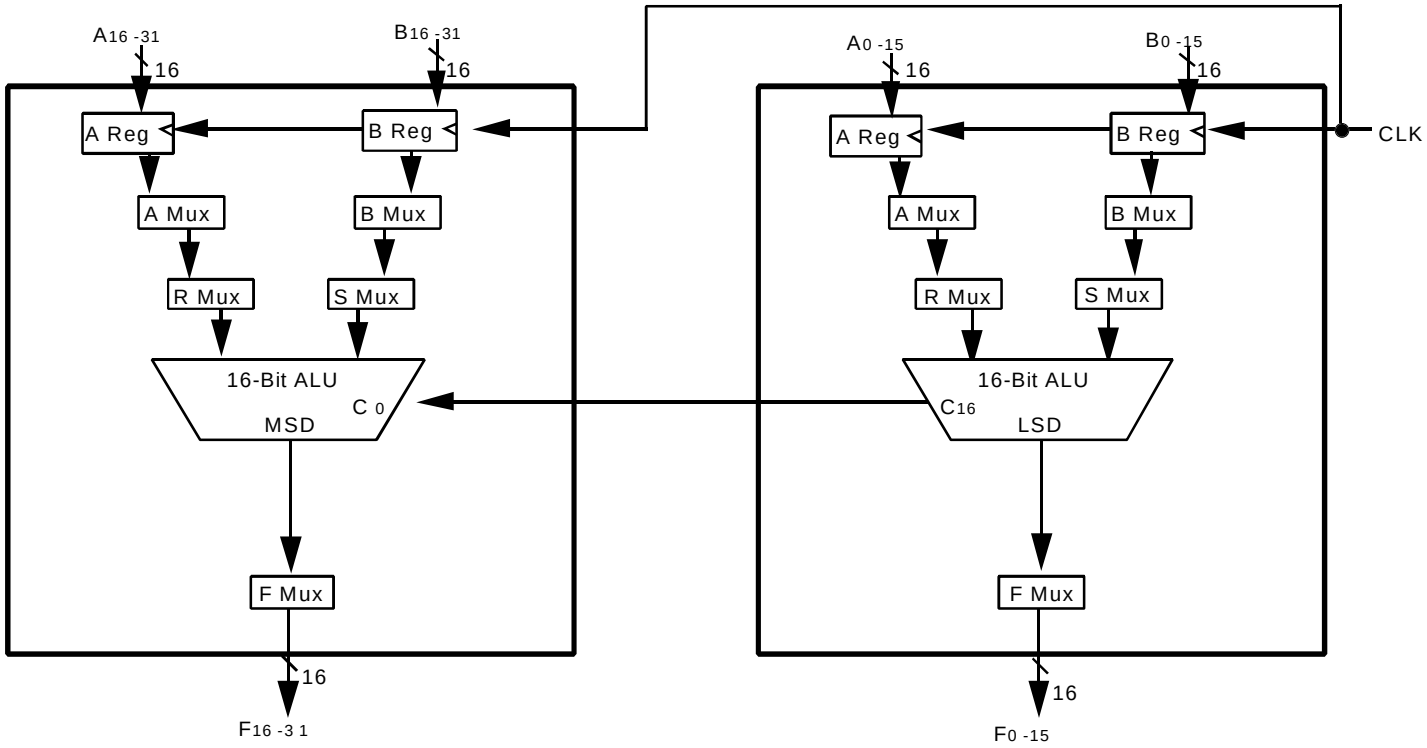


Figure 5. 32-Bit Configuration for FTAB = 0, FTF = 1

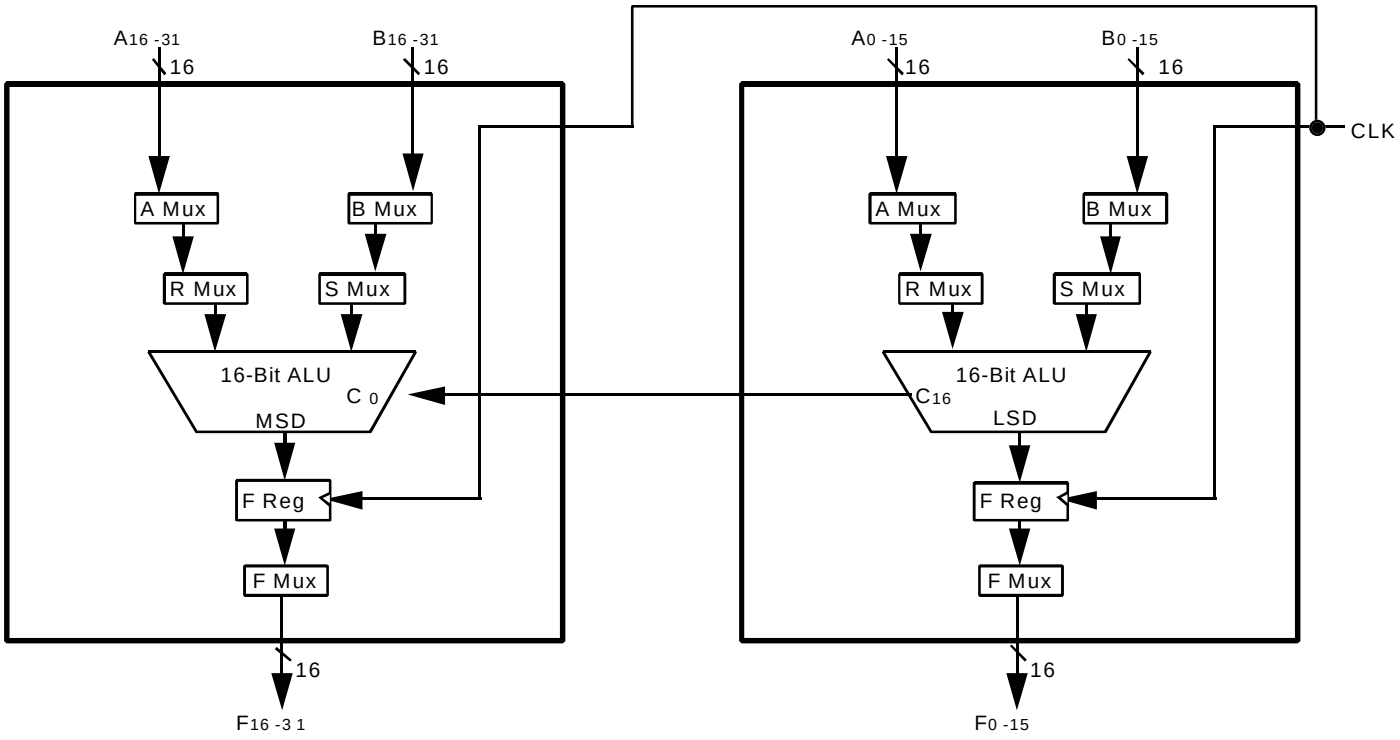


Figure 6. 32-Bit Configuration for FTAB = 1, FTF = 0

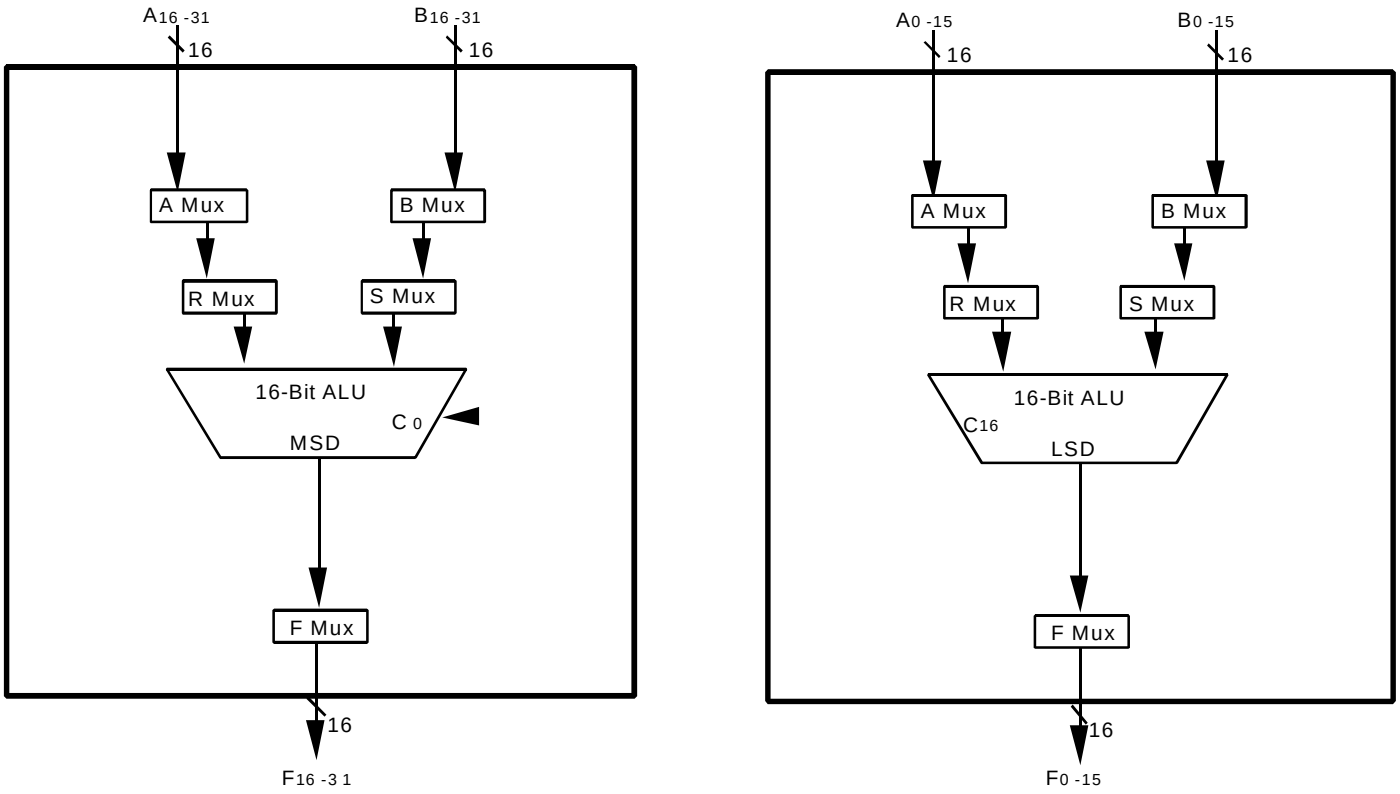


Figure 7. 32-Bit Configuration for FTAB = 1, FTF = 1

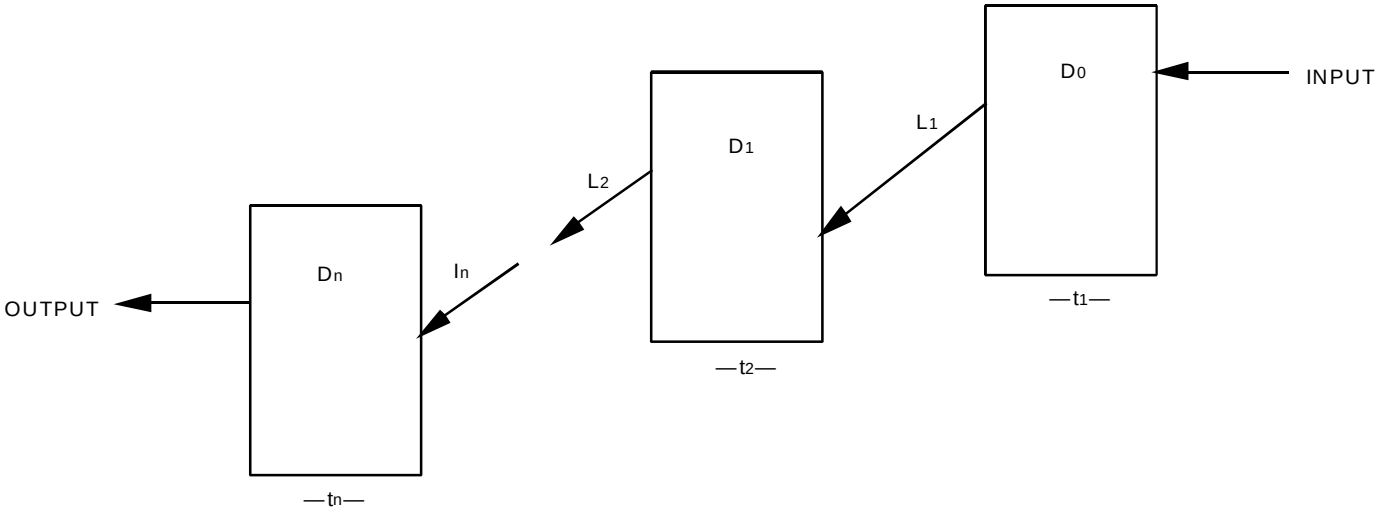


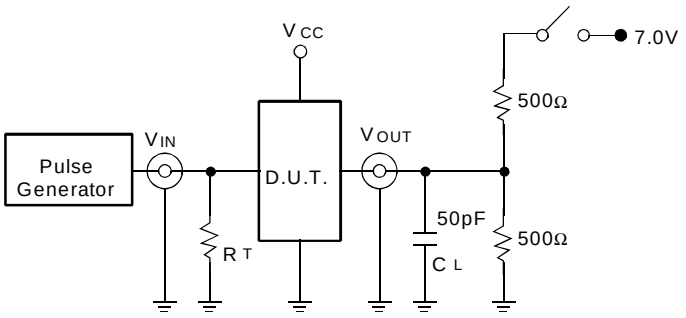
Figure 8. Propagation Delay = t1 + t2 + . . . + tn N-Cascaded Devices

AC TEST CONDITIONS

Input Rise levels	GND to 3V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figure 1

TEST WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

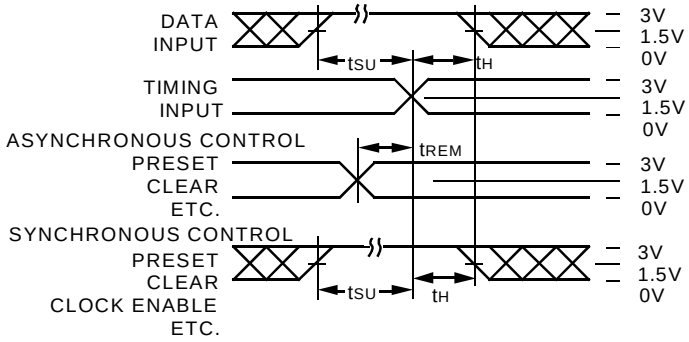
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

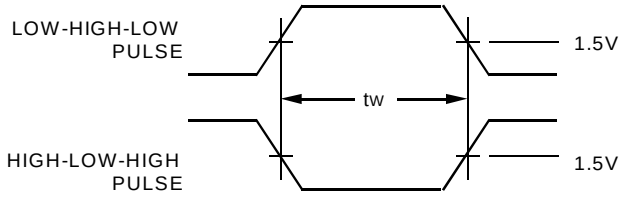
C_L= Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

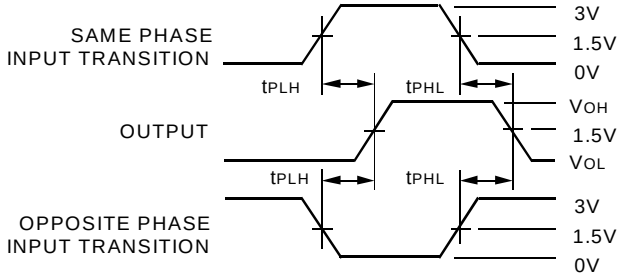
SET-UP, HOLD, AND RELEASE TIMES



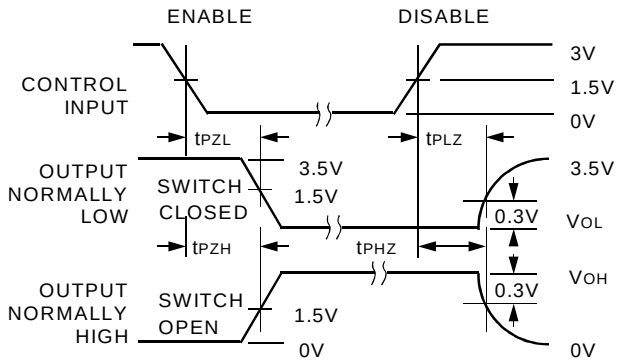
PULSE WIDTH



PROPAGATION DELAY



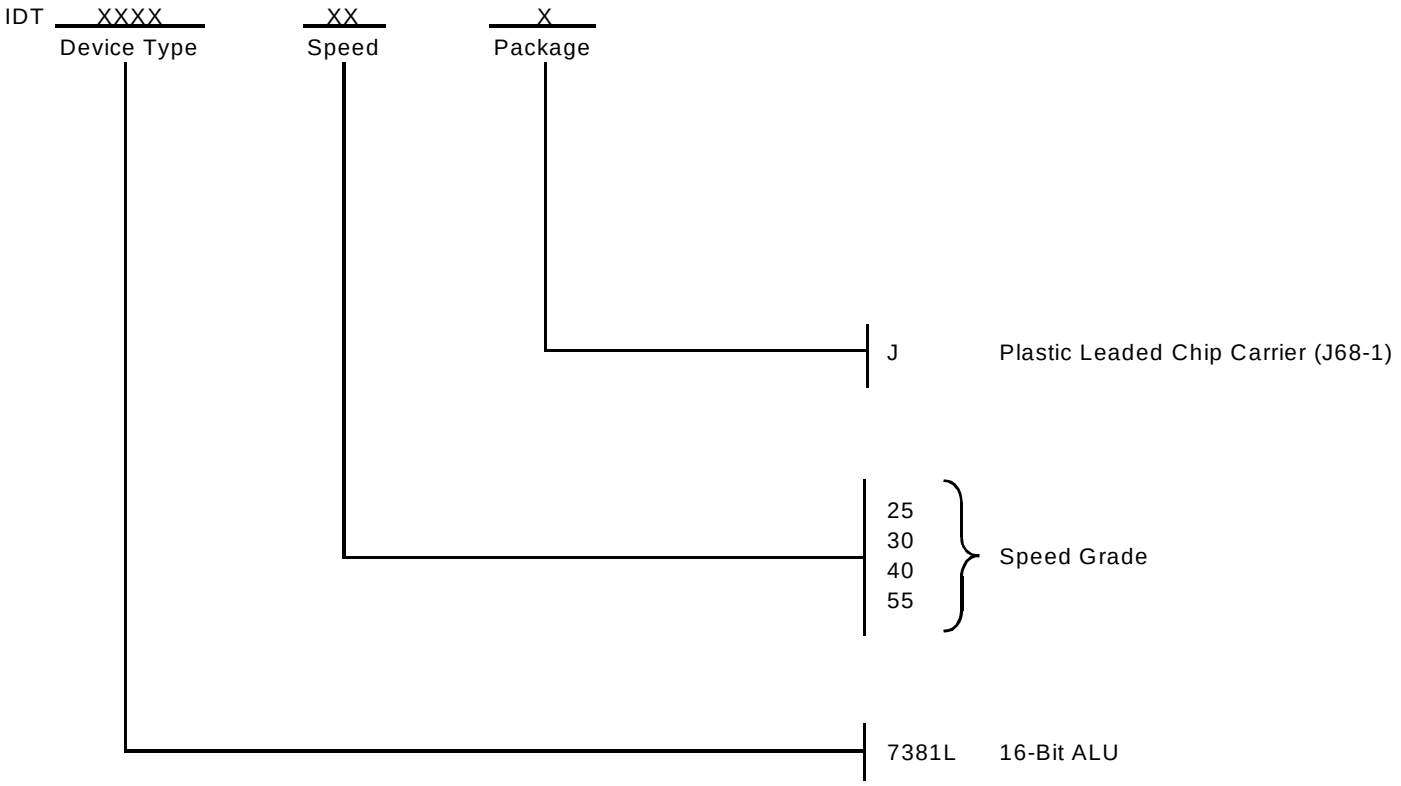
ENABLE AND DISABLE TIMES



NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



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