High Current Solid-State Relays

28 March 2018

Introduction

Solid State Relays (SSR) offer some distinct advantages over their mechanical counterparts: speed, durability, vibration tolerance, clean (chatter free) switching, and combustion protection. But have you priced them – wow! A quick scan on a popular parts site shows unit costs of $40 - $90 for 20A and higher SSRs. On-state resistance and the associated dissipation can also be a problem requiring a larger installed footprint.

Commercial, low power (<10A) SSRs are generally smaller and more cost-effective than discrete solutions. But for higher power, depending on requirements, discrete SSRs can be designed as stand-alone units or integrated as components of larger designs at much lower costs and dissipations. Timing, switching speed, noise & dv/dt immunity, can all be tailored to the application. This paper explores an approach to implementing high current (>10A) MOSFET based SSRs and some approaches to varying cost & performance.

Overview

A MOSFET based SSR uses one or more MOSFETs to perform the switching (relay) action. How many are used depends on the power rating, the number of taps & poles, and if it's intended to be used with AC or DC only. Regardless of the configuration, most require a floating gate drive. Figure 1 depicts the basic design.

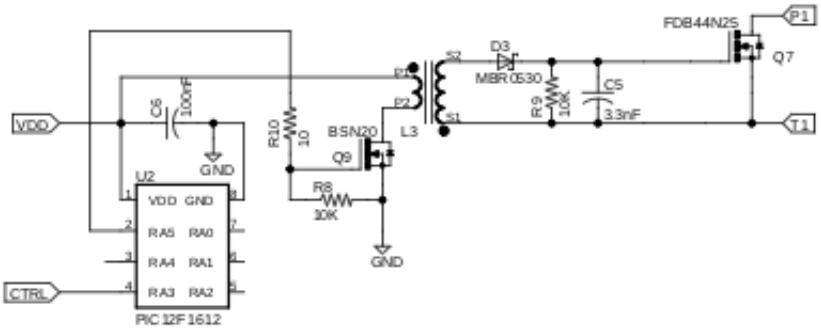

Figure 1

Since an SSR, like a relay, is intended to switch on and remain on for an extended period of time a traditional floating gate drive like a pulse transformer or bootstrap won't work. Many commercial SSRs that employ MOSFETs use a photovoltaic solution to power the floating gate drive. These are efficient but turn-on times are typically slow (several mS).

For my designs I use a flyback inductor. It is fast, efficient, compact, and can run on 3.3 & 5V supplies.

I also prefer MOSFETs over SCR and TRIAC solutions because of their higher dv/dt immunity and lower total dissipation. While a TRIAC will allow you to create an AC relay with that single component (vs. two for MOSFETs), the total dissipation for the MOSFET based design will be lower. This is also true for SCR based solutions which use two in antiparallel configuration (so each handles a half cycle and half the dissipation).

Example: from its data sheet a commercial 5A AC relay capable of switching 120V has a maximum on state voltage drop of 1.5V. At 5A that's 7.5 watts. A MOSFET based design will require two configured back-back (common source) so the body diodes don't conduct when the relay is off. Using the MOSFET's from one of the examples in this paper each has an $R_{DS(ON)}$ of 69mΩ for a total of 138mΩ. At 5A the dissipation is 3.45 watts; less than half its commercial cousin.

Gate Drive

The basic flyback gate drive is depicted below and works as follows.

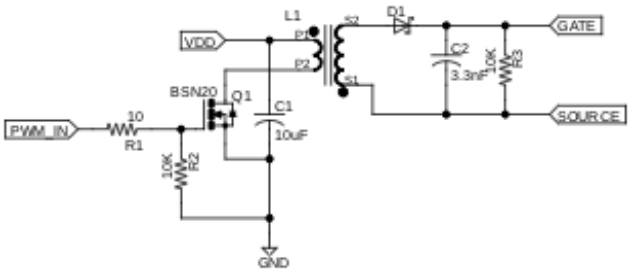

Figure 2

Q1, R1, and R2 form a basic single-ended primary flyback. C1 provides bypass to minimize noise & ripple on Vdd. L1 is a small (6.3mm OD) ferrite toroid with a 6-turn primary and 17-turn secondary. Both are 26AWG magnet wire; smaller gauges can be used but for hand assembly this increases durability for handling. D1 provides rectification, C2 augments the gate capacitance to provide some filtering, and R3 serves both as a burden and pull-down resistor.

The design is driven by a 100kHz PWM with a duty cycle not exceeding ~ 13%. This is important: a ferrite core is used to obtain the required inductance with a small number of turns but it will quickly saturate. This will be examined in the section on switching performance.

The secondary will deliver a constant 10-14V Gate-Source depending on the duty cycle used. If MOSFETs with a large gate capacitance, or several are paralleled, C2 could be eliminated. Likewise, R3 can be adjusted (but not eliminated) to vary the peak voltage and turn-off time.

Many variations of this basic scheme can be employed to improve performance & efficiency.

Controller

The controller is responsible for driving the gate drive circuit. In its most basic form it must be able to deliver a 100kHz, 10-14% DC, logic level signal with reasonable (+/- 5%) precision. It could be a dedicated oscillator but I prefer to use a microcontroller since it allows the integration of other functions (temperature, current, etc. monitoring) and costs about the same as a dedicated chip. And the supporting code is straight-forward.

In some applications it might be possible to omit a dedicated controller and use a spare pin / PWM that is available in a design's main controller.

Baseline Switching Performance

The circuit in figure 3 below was used to examine SSR turn-on / off times and general performance. It's taken from a working design that uses a microcontroller. Note the use of back - back MOSFETs which is required when controlling AC currents.

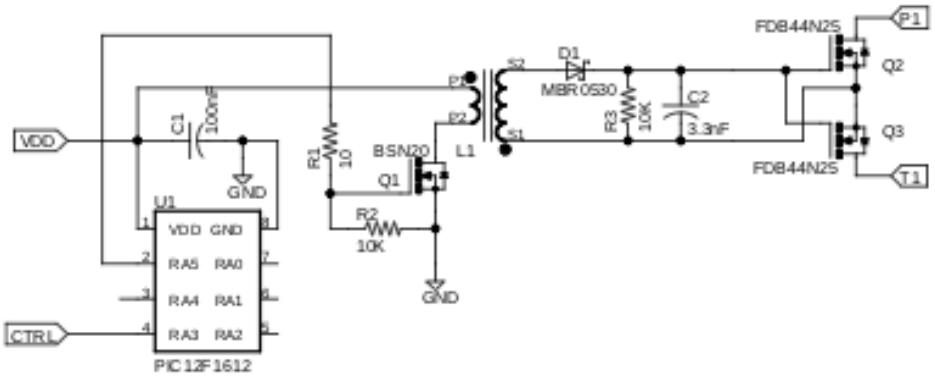

Figure 3

This design depicts an active turn-on and passive turn-off. The turn-off is passive because it relies on R3 to discharge the gate when PWM signal turns off.

This basic circuit will be used throughout the remainder of the article. Vdd=5V, P1 (pole) is connected to a DC bench power supply set to 20V thru a 5Ω power resistor for a 4A load current, and T1 (tap) is grounded.

The simplest method of turning the SSR on & off is switching the PWM signal on & off. When CTRL is TRUE, turn the PWM on at a constant duty cycle. When CTRL is set FALSE stop the PWM. Figure 4 demonstrates this basic turn-on. CH1 is the PWM drive signal from the microcontroller, CH2 measures the flyback switching voltage across Q1's D-S, and CH3 is the voltage across the relay (P1-T1). The PWM is set to a 10% DC (1uS).

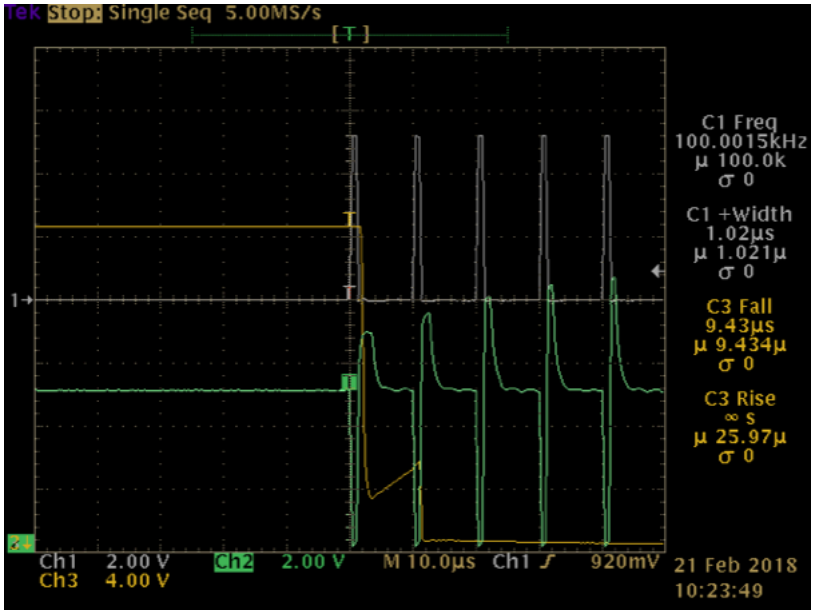

Figure 4

Note the step response of the relay. It takes two cycles to complete the turn-on and another two cycles for the MOSFETs to fully saturate. That's a total turn-on time of 40uS.
Figure 5 depicts the same turn-on but at a shorter time base to show detail in the first cycle. Q1's $R_{DS(ON)}$ is a nominal 2Ω so CH2 can be used to approximate L1's peak current. The cursor measures 312mV which equates to a peak primary current of 156mA. Note the 'knee' at the end of the cycle which indicates the inductor is nearing saturation.

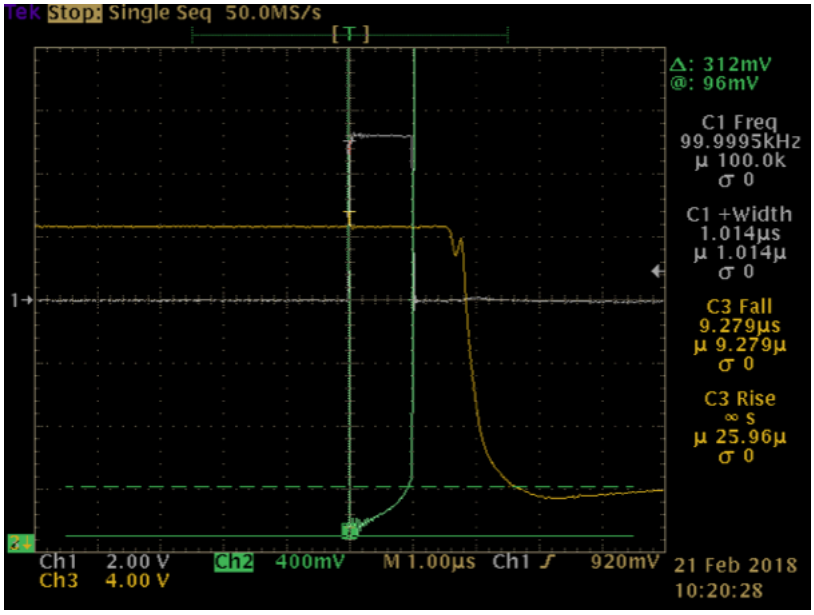

Figure 5

Figure 6 depicts the full turn-off event. The cursor measures the time from PWM termination to the start of relay turn-off.

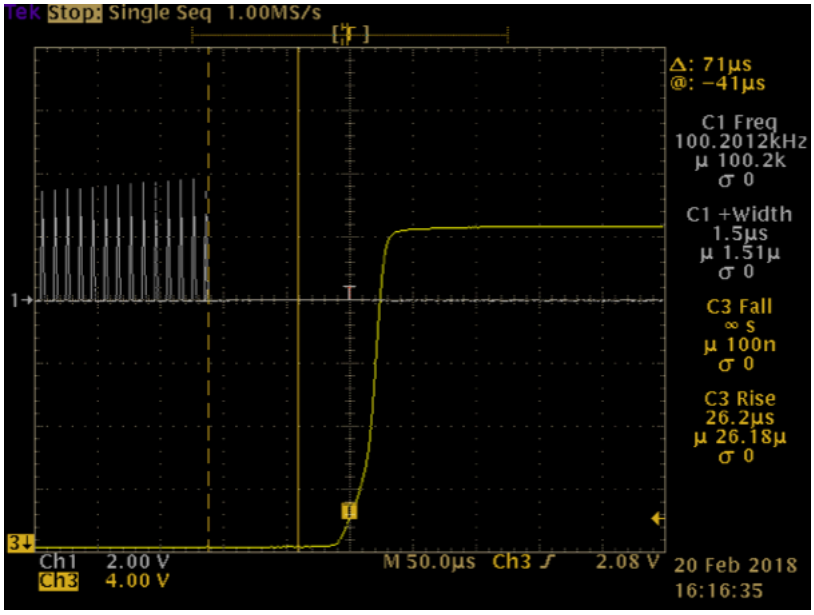

Figure 6

In the basic design the turn-off is entirely passive and relies on R3 to discharge the gate capacitance and C2. Using data sheet values, Q2 & 3 have a combined typical gate charge of 94nC. With V_{GS}=10V, the total capacitance is:

$$\left(\left(\frac{94 \times 10^{-9}}{10}\right) + (3.3 \times 10^{-9})\right) = 12.7nF$$

And a time constant of:

$$12.7 \times 10^{-9} \times 10000 = 127uS$$

With a maximum gate threshold voltage of 5V the time required for a 5V change (with gate starting at 10V) is:

$$127uS \times \ln\frac{1}{1 - \frac{5}{10}} \approx 88uS$$

Which matches nicely with the timing in the trace. However, the majority of the turn-off, and switching losses, occur in the second time constant. The figure below is the same turn-off event depicted with a shorter time base.

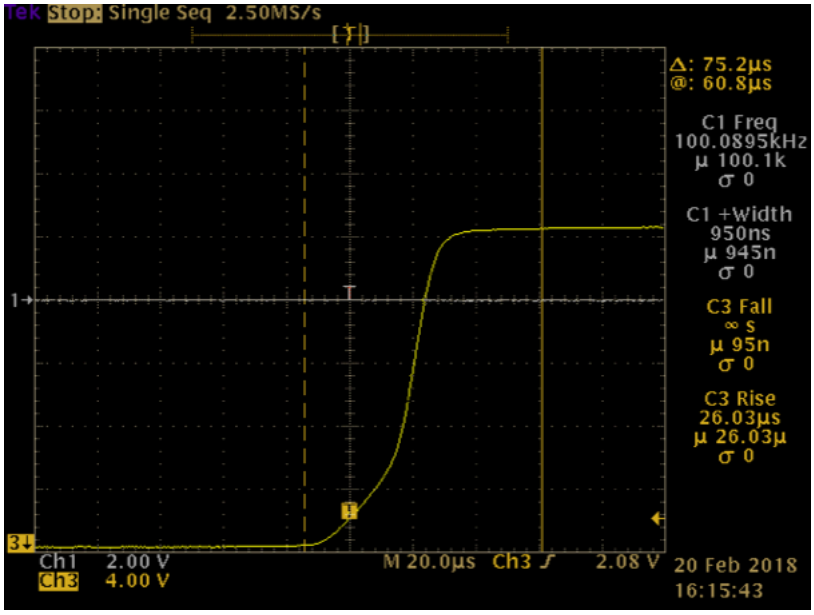

Figure 7

Ripple is relatively low even with the small capacitance compared to a conventional flyback supply. This is due to the high impedance of the gates once charged. Figure 8 below shows the AC component at the gate of the relay transistors in steady state.

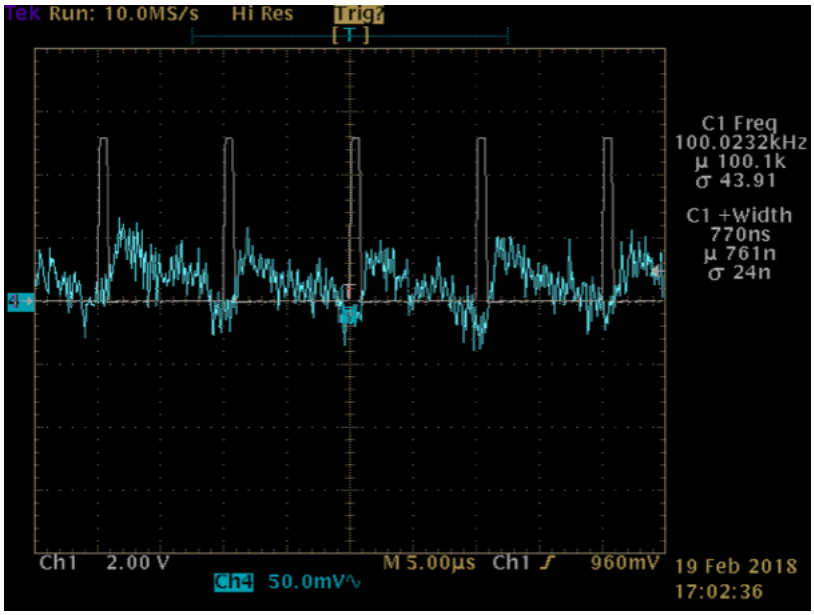

Figure 8

Improving Turn-on

A 40uS turn-on is very good for a relay and could be used to employ zero voltage switching on 60Hz AC circuits. But with a simple software change this can be improved by a factor of 80. This is done by starting the PWM at a higher duty cycle for the first 2~3 cycles and then reducing to a lower value.

This not only achieves a hard turn-on but reduces the steady state operating current of the relay. Figure 9 shows the first cycle at turn-on with a 12% DC. The total fall time is ~ 500nS and the total time to achieve turn-on, including the first PWM period, is 1.5uS.

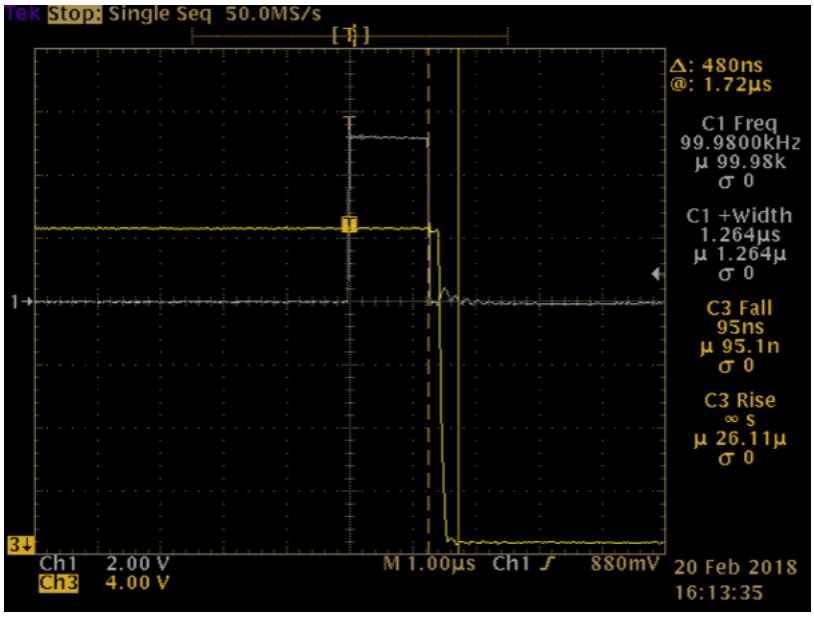

Figure 9

Figure 10 shows the voltage across the flyback primary switch. Unlike the waveform in figure 5 showing the baseline performance, the inductor is saturating. Current is approaching 500mA (the cursor is set to measure what's left of the knee); but since this DC is only maintained for 2~3 periods it isn't a concern.

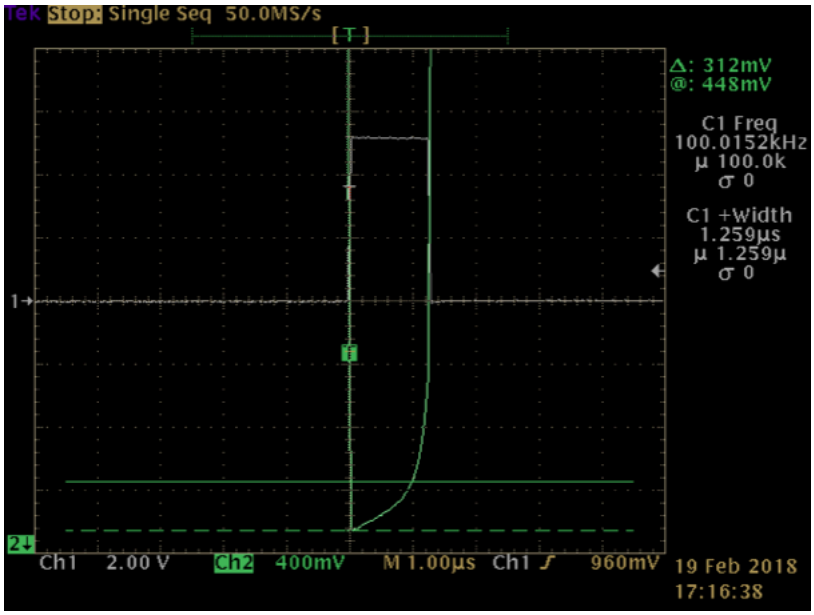

Figure 10

That said, evaluation in the target environment is necessary since environmental factors such as high temperatures could further decrease the ferrite's permeability which could lead to higher currents and destroy the transistor.

With the turn-on complete the DC can be reduced to 7~8% since only the gate leakage and burden resistor currents must be offset. Figure 11 shows the steady state current with an on-time of ~ 750nS. The inductor is not near saturation and the peak current is only 96mA.

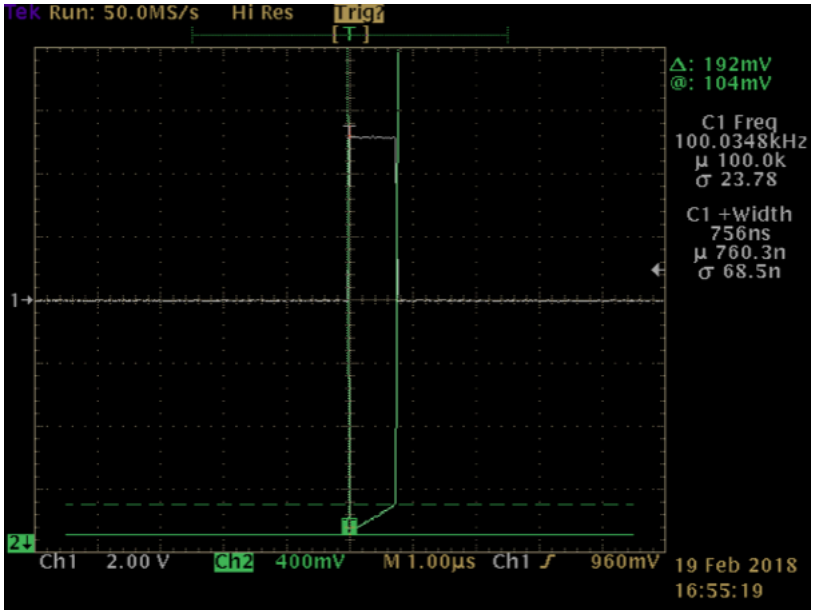

Figure 11

This peak current translates to an average 8mA draw from the power supply to maintain the SSR's on state.

Improving Turn-off

Achieving a crisp turn-off is more difficult and requires additional components. I have found an opto-isolator to be most effective. Figure 13 shows the modified circuit.

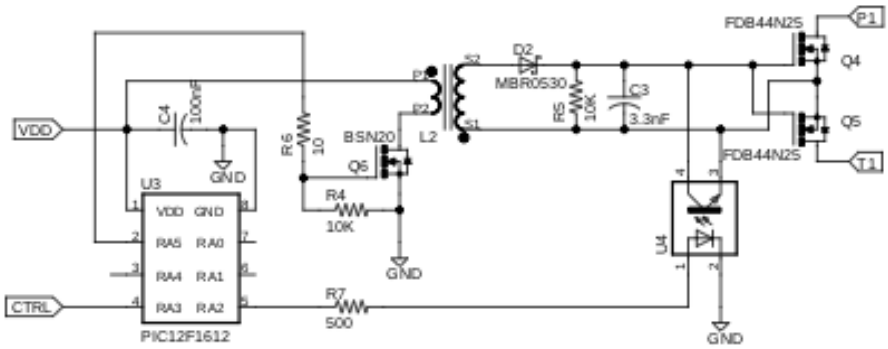

Figure 12

Software modifications are also required to drive the opto-isolator and, there are a few variations on this turn-off scheme depending on the power budget of the target design. First, performance: figure 13 shows the entire turn-off event from the termination of the PWM signal to the relay off.

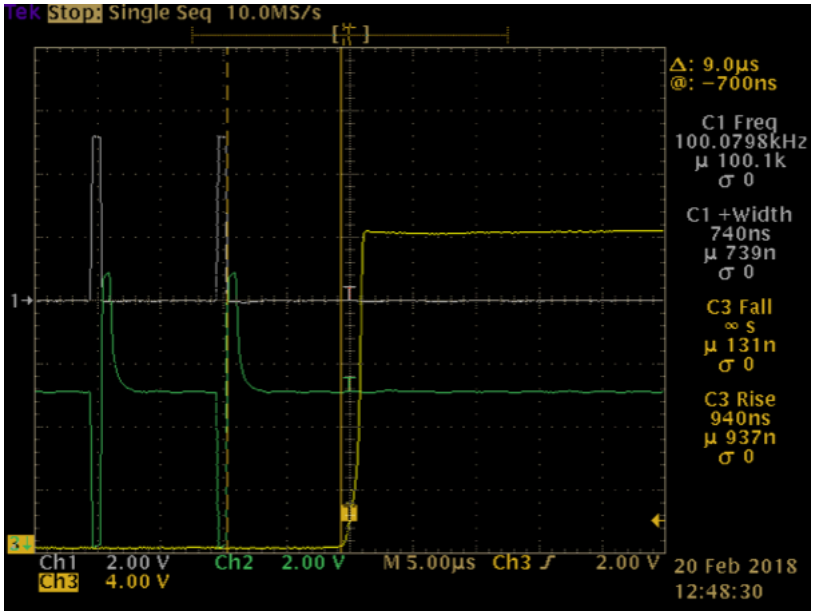

Figure 13

The turn-off is complete in under 10uS, a vast improvement from ~ 150uS. Much of the delay is due to latency in the opto-isolator so it's possible to improve upon this with the right component. Regardless, this performance could be used to implement zero voltage/current switching.

Driving the opto-isolator does require additional current – about 10mA (or less if a slower turn-off can be tolerated). The same approach used to improve turn-on can be employed for turn-off: only drive the opto-isolator for a brief period to discharge the relay's MOSFET gates. This is illustrated in figure 14.

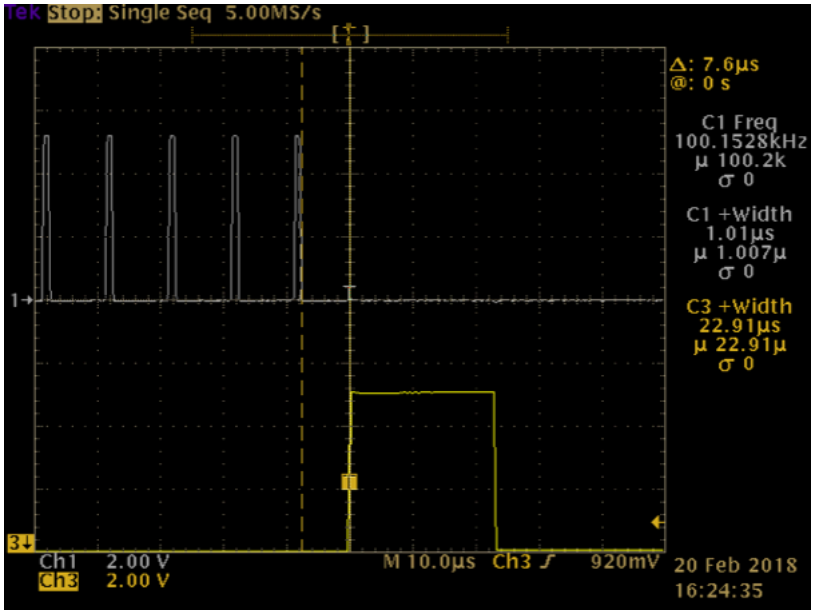

Figure 14 – CH3 shows the opto-isolator turn-off signal

Like the passive arrangement it relies on R5 to maintain the off state. By doing so the relay's power budget remains small: when off the quiescent current of the controller can be less than 500uA depending on the model, clock speed, code efficiency, and what peripherals are active.

In a high noise environment or where transients are a concern, the opto-isolator can be left on to actively hold the G-S potential at 0V. Note that with this feature the turn-on time will increase slightly due to the storage time in the opto-isolator. This could be compensated by adding a software delay between the opto-isolator turn-off and PWM turn-on but either way the total time of the turn-on event increases. See Figure 15 below.

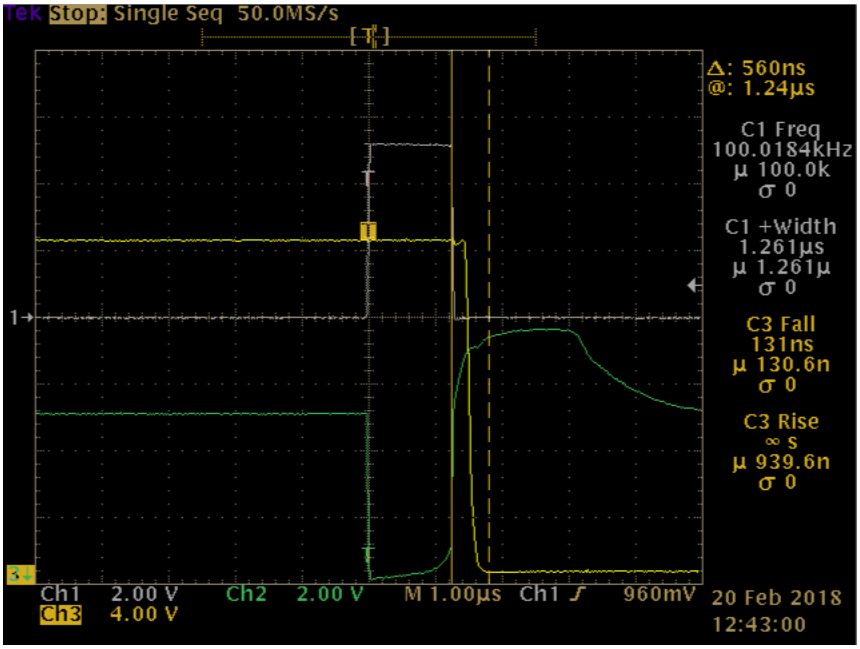

Figure 15 – CH3 shows the opto-isolator turn-off signal

Examples

The form & function of solid state relays is limited only by your imagination and the design's requirements. The can switch AC, as shown in the examples above, or DC, and can have several poles and even taps.

Figure 16 depicts a SPST DC relay reference design capable of handling 60A at 60V DC continuous. Three power MOSFETs with a $R_{DS(ON)}$ of 4.9mΩ each are paralleled. Assuming each transistor shares the load equally the dissipation is 2W/MOSFET for a total of 6W. Not bad.

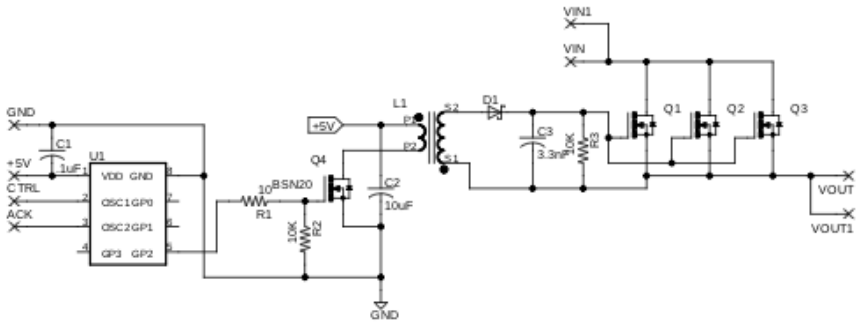

Figure 16

This example highlights an important point: MOSFET selection plays an important role in the design's capabilities, size, and thermal requirements. But unlike packaged commercial devices you have complete control.

A commercial unit meeting this example's specifications would cost $100. The components for the above cost less than $10 in unit quantities and the layout is simple enough to manufacture at home or use a service like OSH Park which would set you back less than $30 for three PCB copies.

Note that the controller incorporates an ACK (Acknowledgement) pin. In it's simplest form it does just that: when the CTRL line is TRUE, the controller starts the PWM and the sets the ACK line TRUE. So all it indicates is that the controller is responsive but there's no validation that the relay is actually on.

With additional hardware this can take on additional meaning: temperature, voltage, and current sensing can be incorporated. The ACK & CTRL lines could be replaced by I^2C or SPI (or whatever your preferred comm bus is).

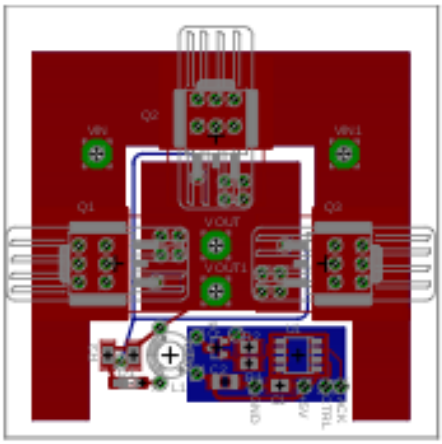

Figure 17

Figure 17, above, is the layout, The board is 6x6cm (2.35”x2.35”). The transistors are arranged for balanced dissipation and incorporate surface mount heat sinks. At typical ambient temps this design could be operated without forced air cooling.

This next example is also a reference design and illustrates a DPST relay that incorporates temperature monitoring using an NTC thermistor. This too is intended for DC currents and could be used for polarity protection on equipment that depends on the user to connect properly to the power source.

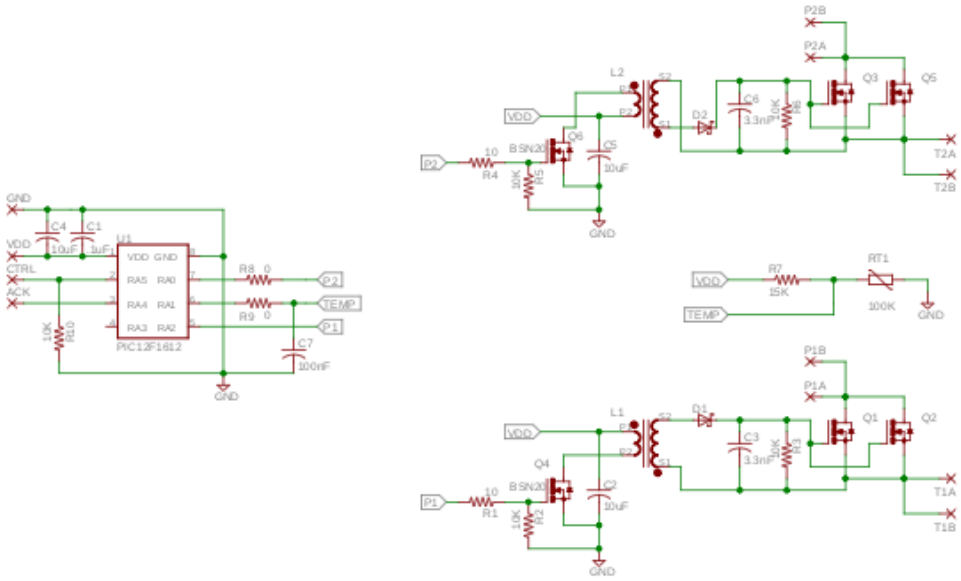

Figure 18

Here the ACK line takes on a bit more meaning. If the high temp threshold is exceeded the relay won’t turn-on and if already on it will set the ACK line FALSE letting the upstream

controller know that something's wrong. Also note the use of two flyback sections which is necessary since each pole can be at different potentials.

And here's the layout – also on a 6x6cm PCB. This design is capable of handling 40A continuous; more with supplemental cooling.

The copper pours are mirrored top & bottom with generous thermal vias which also provide an ample path for the high currents. Two oz copper, minimum, is recommended.

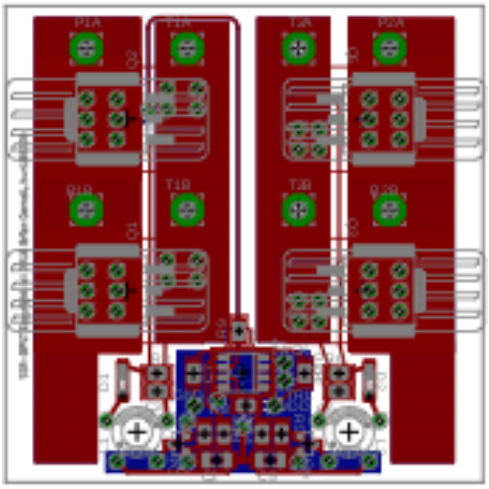

Figure 19

This last example is a derivative of the previous and is taken from a working design. It demonstrates the flexibility you have in working with the base designs to tailor to the application. It too is a DPST but trades the flyback on one of the poles for a simple ground-referenced drive. As hinted in the prior example this relay is incorporated into a design requiring polarity protection.

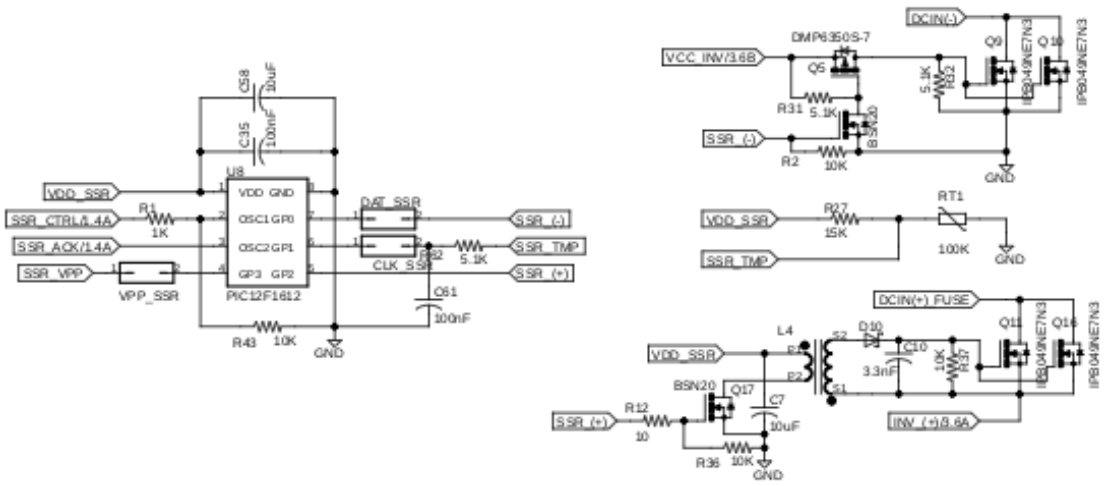

Figure 20

Also note the use of jumpers on the controller. These pins double as the programming pins and, it's wise to include these to allow for in-circuit modifications unless the design has been previously debugged.

Power Consumption

In spite of the relatively high peak currents on the flyback, these designs require little power. Budget for the controller to consume 500uA when idle and 1mA when active. Each flyback drive will draw 10mA max and each opto-isolator 10mA when on.

But be sure to verify in your own design since operating voltage and the specific components used will influence. In all of the examples presented here a 5V supply and Microchip's 12F midrange 8-bit controllers were used.

Last, the flyback circuit should include a small bypass capacitor to minimize noise on the supply line. 10uF is sufficient to keep ripple under 30mV and is implemented in the last example with an MLCC (C7).

Conclusion

This paper has demonstrated a cost-effective approach to implementing custom Solid State Relays that achieve lower cost, dissipation, performance, and flexibility than commercial solutions. Using a simple reference design, derivatives can be easily created for AC & DC environments handling currents in excess of 20A.