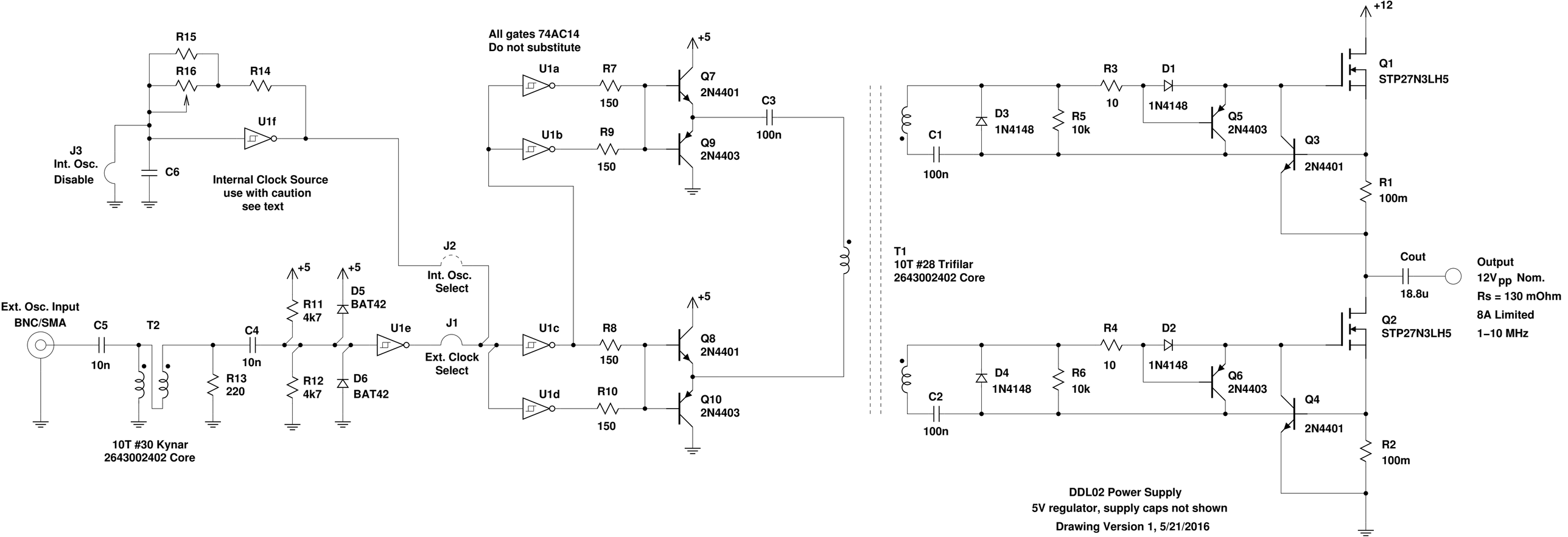
All gates 74AC14
Do not substitute
R15
R16
R14
U1f
J3
Int. Osc.
Disable
C6
Internal Clock Source
use with caution
see text
U1a
R7
150
Q7
2N4401
U1b
R9
150
Q9
2N4403
C3
100n
+5
J2
Int. Osc.
Select
+5
+5
R11
4k7
D5
BAT42
Ext. Osc. Input
BNC/SMA
C5
10n
T2
C4
10n
R13
220
R12
4k7
D6
BAT42
U1e
J1
Ext. Clock
Select
U1c
R8
150
Q8
2N4401
U1d
R10
150
Q10
2N4403
10T #30 Kynar
2643002402 Core
T1
10T #28 Trifilar
2643002402 Core
+12
Q1
STP27N3LH5
R3
10
D1
1N4148
C1
100n
D3
1N4148
R5
10k
Q5
2N4403
Q3
2N4401
R1
100m
Cout
18.8u
Output
12Vpp Nom.
Rs = 130 mOhm
8A Limited
1–10 MHz
Q2
STP27N3LH5
R4
10
D2
1N4148
C2
100n
D4
1N4148
R6
10k
Q6
2N4403
Q4
2N4401
R2
100m
DDL02 Power Supply
5V regulator, supply caps not shown
Drawing Version 1, 5/21/2016