Introduction

This document outlines the theory behind universal diode logic gates.

Diode Types

The key technology in this design is the combined use of *slow* and *fast* diodes, referring to the length of their respective reverse recovery times, usually denoted by t_{rr}. An ideal diode would cease conduction immediately when switched from forward to reverse bias conditions. Actual diodes will continue to conduct in the reverse bias condition for a time equal to t_{rr}. Different types of diodes can exhibit a very wide range of reverse recovery times. "Rectifier" diodes intended for use in rectifying 60Hz AC current (e.g. JEDEC type 1N4007) may have reverse recovery times measured in microseconds, typical PN junction "switching" diodes (e.g. JEDEC type 1N4148) exhibit reverse recovery times of several nanoseconds, while Schottky diodes produced for RF detection (e.g. JEDEC type 1N5711) may show carrier lifetimes in the picosecond region. A special type of device, the PIN (positive-intrinsic-negative) diode, constructed with a layer of intrinsic semiconductor between the p- and n-type semiconductor layers, shows a very long t_{rr}, and is currently in wide use in radio-frequency switches, attenuators, and limiters. In this design, the distinction between *slow* and *fast* diodes is relative to each other and to the power supply frequency: a rectifier diode and a switching diode may be used as a *slow*/*fast* combination with a high-frequency (HF) power supply, while a switching/Schottky diode combination would work as a *slow*/*fast* combination at upper VHF or UHF frequencies. Ideally, a PIN diode / Sckottky diode combination would be used with the highest power supply frequency consistent with the diode parameters, resulting in the fastest logic switching speed.

A key feature of the technology is that *slow* diodes are used to switch RF current based on a lower frequency or DC control signal from previous logic stages, while *fast* diodes are used to rectify the switched RF current into lower frequency or DC control signals for subsequent logic stages. Using PIN diodes to switch RF current based on DC or lower-frequency signals is a widely used technique in RF and microwave transmitter and receiver circuits. Similarly, rectifying, or *detecting* switched or modulated RF current into DC or lower-frequency signals using Schottky diodes is also in wide use, for example in RF power meters or AM radio receiver circuits. Coupling the two uses for the purpose of computing arbitrary digital logic functions is the main innovation in DDL.

Universal Logic Gates

Figure 1 a simple DDL NOR (not-or, or inverted OR) gate. NOR gates, like NAND gates, are known as "universal" logic gates because they can be connected together to compute any arbitrarily complex digital logic function. In contrast, AND and OR gates are not universal; they can only compute a limited subset of all possible digital logic functions. Previous diode logic implementations have been limited to computing AND and OR functions, hence could not be used to build arbitrary logic functions, such as general purpose computing devices. Specifically lacking from previous diode-based logic circuits were an inversion function and positive absolute gain. Without a logical inversion function, previous diode based logic circuits could compute neither NAND nor NOR functions, either of which are necessary in order to compute any arbitrary logic function. Similarly, without positive absolute gain, the output signal from each successive stage of previous diode logic circuits was diminished; this limits the number of stages that can be practically used. In order to compute arbitrarily complex logic functions, logic circuits must exhibit a positive absolute gain, alternatively expressed as the ability to drive two or more subsequent stage inputs without degradation of the output signal below the input signal level. The circuit of Figure 1 exhibits both a logical inversion function (computing a NOR function), and positive absolute gain, allowing more than two subsequent input stages to be driven from a single output, thus allowing an arbitrary logic function to be computed.

Circuit Operation

In Figure 1, input diodes **D1** and **D2** act as a traditional diode OR gate; a HIGH-level voltage signal on *either* of the inputs will cause current to flow through the input diode(s), through resistor **R1**, inductor **L1**, and *slow* diode **D3**. The input diodes, **D1**, **D2**, and any additional input diodes which may be added to increase the gate fan-in may be of either the *slow* or *fast* variety, although typically *fast* diodes will be used. Resistor **R1** serves to limit the current which can flow into the input circuit. Inductor **L1** presents a low impedance path for the DC or lower-frequency logic signals presented to the inputs of the circuit, while presenting a high impedance to the higher power supply frequency. This allows signal-frequency current to flow from the input nodes through to *slow* diode **D3** while

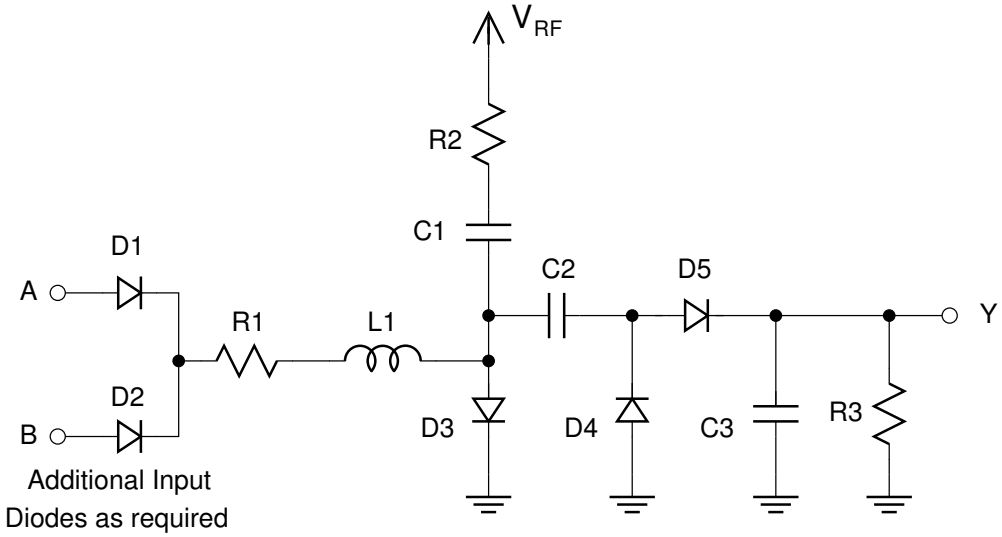

Figure 1: Single stage diode NOR gate

blocking higher frequency power supply current from flowing backwards into previous logic stages.

When *all* input nodes are at LOW signal levels, no significant DC current flows in *slow* diode **D3**. Under these conditions, **D3** presents a high impedance at the power supply frequency. With **D3** presenting a high impedance, power supply current is allowed to flow through **R2** and **C1** to an output voltage doubler circuit comprising **C2**, **C3**, **D4**, and **D5**. A radio-frequency AC power supply, V_{RF}supplies power to the circuit. Resistor **R2** serves to limit the power supply current drawn by the circuit in both the LOW and HIGH output states. Capacitor **C1** blocks the lower-frequency or DC logic signals from flowing into the power supply, while allowing the higher frequency power supply current to flow into either **D3** or **C2**. When power supply current flows through the output voltage doubler, a DC current flows into **C3**, which charges to a HIGH state. Hence, when all inputs to the circuit are in the LOW state, the output of the circuit is in a HIGH state.

When a HIGH state voltage is presented at *either* of the input nodes, DC or low-frequency current flows through the corresponding input diode(s) (**D1**, **D2**, or both), **R1**, **L1**, and *slow* diode **D3**. This causes **D3** to assume a low impedance at the power supply frequency. The low impedance of **D3** shunts power supply current to ground, and away from the output voltage doubler, so no significant current flows through **C2** and the output voltage doubler. No significant DC or low-frequency current flows into **C3**, so the output node remains at a LOW state. Hence, when one or more inputs to the circuit are in the HIGH state, the output of the circuit is in a LOW state.

If the output is in a HIGH state, and one or more inputs is switched from LOW state to HIGH state, DC or low-frequency current will cease flowing from the voltage doubler into **C3**. Any remaining charge on **C3** will then be discharged through the input circuits of any subsequent logic stages and/or resistor **R3**. In the absence of any subsequent logic stages, the HIGH state of **C3** will be discharged solely through **R3**.

Figure 2 shows the logical truth table for the NOR gate of Figure 1. As shown in the table, the gate's output is in the HIGH state if and only if both inputs are in the LOW state. If either input is in the HIGH state, the output is forced into the LOW state. This is the logical NOR function, described by the equation:

$$Y = \overline{A + B}.$$

Here, HIGH and LOW states refer to the voltage level on input or output nodes. In the case of Figure 1, a HIGH state specifically refers to a voltage level on an input node which causes sufficient current to flow through *slow* diode **D3** to shunt RF power supply current away from the output stage, resulting in a LOW output state. Similarly, a LOW state specifically refers to a voltage level on an input node which does not cause significant current flow through **D3**, hence allowing RF power supply current to flow into the output stage.

Single Stage Limitations

Although the single-stage diode NOR gate presented in Figure 1, when constructed with appropriate diode types, and operated with a suitable power supply frequency and amplitude, can provide sufficient gain to be used in practical logic circuits, performance can be significantly improved by adding an additional gain stage. Specifically, the gain of single-stage designs is compromised by the junction capacitance of *slow* diode **D3**. This junction capacitance shunts some fraction of power supply current to ground even with no DC bias flowing through **D3**. The problem presented by junction capacitance in PIN diode RF switches used in RF and microwave transmitter and receiver circuits is well known. A widely used solution to this problem is the application of *reverse bias* on PIN diode switches. Reverse bias reduces the thickness of the *depletion zone* in the diode, hence reducing diode junction capacitance, and increasing impedance at higher frequencies.

One way to improve the performance of the single-stage diode NOR gate of 1 is to introduce a negative bias on diode **D3**. Unfortunately, the magnitude of the allowed negative bias is necessarily limited by the action of the input diodes (**D1** and **D2**) combined with the voltage doubler diodes (**D4** and **D5**) of the previous stage. If a large enough negative bias is applied to the the anode of **D3**, current will flow through **D1** or **D2** and the corresponding **D5** and **D4** of the previous logic stage, limiting the reverse bias on **D3** to the combined forward voltages of **D1** or **D2**, **D5** and **D4**. A better way to improve the performance of the gate is to introduce an additional slow diode stage for the purpose of generating a large negative bias on **D3** in the HIGH output state.

Power Supply

The NOR gate of Figure 1 requires an AC power supply at a frequency such that the period of the power supply waveform is shorter than the reverse recovery time, t_{rr}, of *slow* diode **D3**. For typical Schottky / PIN diode combinations, a power supply frequency in the radio frequency spectrum is required. Specific frequencies required depend on the specifics of the diode devices, and may range from approximately 1 MHz to several GHz, or higher. The power supply waveform may be a sine wave, square wave, or other waveform. Ideally, a *spread spectrum* power supply consisting of a multitude of frequency components spread over a finite region of the radio frequency spectrum may be used to reduce spurious or unintended RF emissions and possible interference with other electronic devices.

NOR Gate Truth Table

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	L
H	L	L
H	H	L

Figure 2: NOR gate truth table