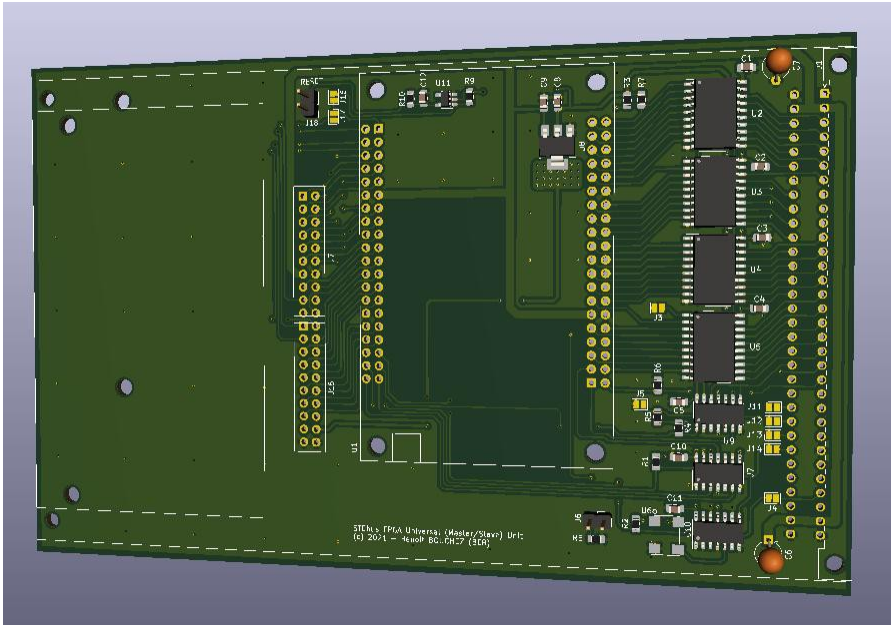
STEBUS UNIVERSAL FPGA MODULE

USER'S MANUAL



Module design by Benoit BOUCHEZ (BEB)

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1 - Introduction

The Universal FPGA Module for STEbus is a IEEE Std1000-1987 compliant microcomputer board.

The module can be used in almost any STEbus system as Default Master or Slave. It does not support Multiple Masters not Arbiter functions.

The Universal FPGA Module supports :

- 20 address lines (full addressing range both for Memory and I/O access)
- two Attention Request lines, to be selected amongst the eight possible ones
- memory and I/O access
- optional host CPU with direct interface to KissBox CPU V4 and Raspberry Pi
- up to 47 freely configurable FPGA I/O lines

The module is based on a DE0 Nano FPGA daughterboard which embeds:

- Cyclone IV EP4CE22F17C6 FPGA (22320 Logic Elements)
- 32MB SDRAM
- 2KB EEPROM
- 8 analog inputs with 12 bits resolution
- Local FPGA configuration device
- Built-in FPGA programmer
- 50 MHz local oscillator
- 3 axis accelerometer

2 - TO READ BEFORE ANYTHING ELSE... SERIOUSLY

As the Universal FPGA Module can be used as a Master or a Slave, the hardware must be configured correctly before anything else, including programming of the FPGA.

VERY IMPORTANT : If configuration is not done properly, contentions may occur between the components, which may damage or even destroy components on the module.

NEVER APPLY POWER SUPPLY TO THE MODULE IF IT IS NOT FULLY CONFIGURED !

3 - Module configuration

The module is configured using solder bridges located on both sides of the printed circuit board (PCB). You must use a soldering iron with a miniature tip to close / open the solder bridges.

When soldering / removing a solder bridge, take care not to overheat the PCB otherwise you may damage it.

3.1 - Master configuration

- J3 = OPEN
- J4 = CLOSE (optional : only if you want the Master to provide SYSCLK signal to STEbus)
- J5 = CLOSE

VERY IMPORTANT : J3 and J5 shall NEVER be closed at the same time. If both Slave and Master configurations are enabled at the same time, this can lead to bus contentions and destructive oscillations

3.2 - Slave configuration

- J3 = CLOSE
- J4 = OPEN
- J5 = OPEN

VERY IMPORTANT : J3 and J5 shall NEVER be closed at the same time. If both Slave and Master configurations are enabled at the same time, this can lead to bus contentions and destructive oscillations

3.3 - Reset source

In most cases, the FPGA must be reset once the configuration file has been loaded (like any other programmable circuit)

The FPGA on the Universal Module can be reset from two different sources :

- local automatic reset at startup with optional external reset control by push-button
- reset controlled by user application hardware (or host CPU)

Note that the two reset sources are exclusive, so you must choose only one !

3.3.1 - FPGA reset signal

Reset signal is transmitted to FPGA daughter board by GPIO_1_IN0 pin (FPGA pin T9) whatever the reset source (host or local generator)

Reset signal is **active low**.

3.3.2 - Automatic reset at startup

- J16 = CLOSE
- J17 = OPEN

An optional pushbutton can be attached to J18 connector. Once external reset pushbutton is released, the reset chip holds FPGA reset signal for 1000ms.

3.3.3 - Reset by user application hardware

- J16 = OPEN
- J17 = CLOSE

When reset is controlled by user application hardware, reset signal duration is fully controlled externally. There is no local pulse duration stretching.

4 - DE0 Nano daughter board installation

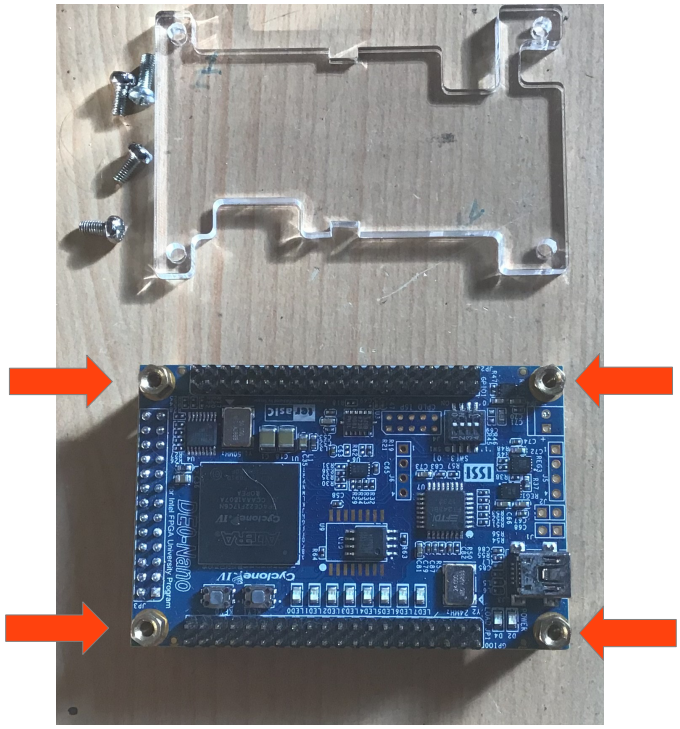
4.1 - Board preparation

Prior to its installation on the main board, the DE0 Nano daughterboard must be prepared so it can be installed on female connectors on main board.

4.1.1 - Plastic cover removal

First remove the transparent plastic cover on DE0 Nano, in order to have better access for the next operation and allow insertion of the daughter board on the main board.

- Remove the four screws holding the transparent plastic cover over the DE0 Nano module
- Remove the plastic cover
- Unscrew the four metallic spacers and remove them from the DE0 Nano board



4.1.2 - Power supply connector removal

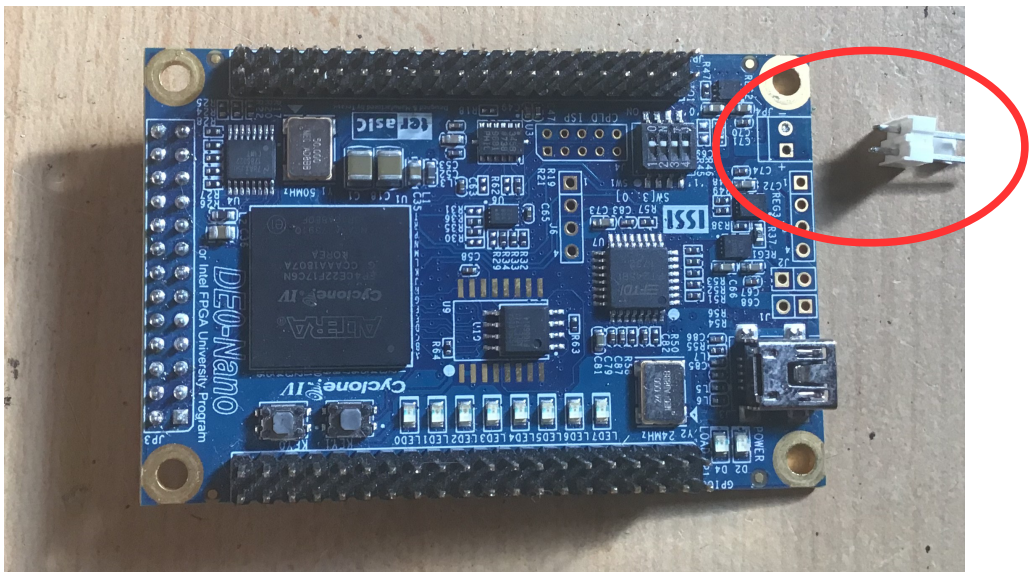
The DE0 Nano includes a power supply connector which prevents the FPGA board to insert fully on the main board, because the pins are too long and touch the PCB.

Two possibilities are offered :

- either cutting the pins with cutting pliers,
- or unsolder and remove the whole connector

Note that the DE0 Nano circuit board is a multi-layer one, so the second solution should be used only if you have adequate tooling and sufficient knowledge about the way to unsolder a through-hole component on a multi-layer PCB.

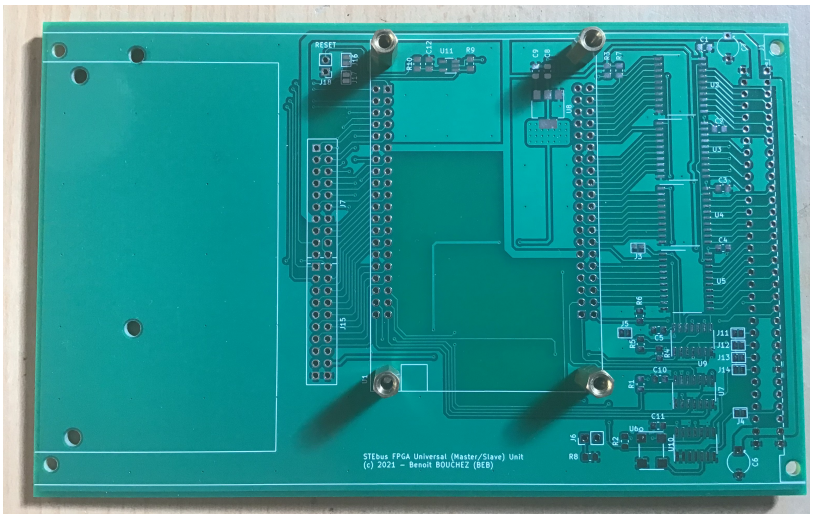
Simply said, if you have any doubt about the way to unsolder the connector : simply cut the pins as near as short as possible.

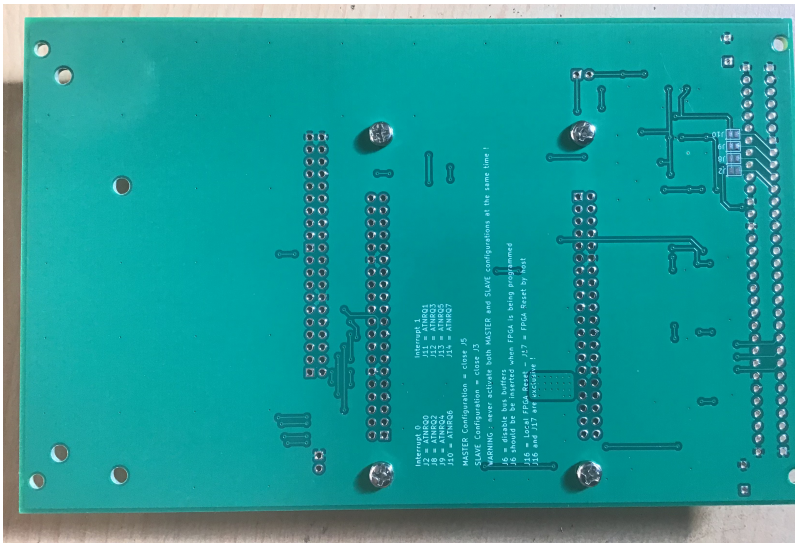


4.1.3 - Installation of spacers on main board

- Take the four **longer** spacers which have been removed from DE0 Nano previously (spacers with female threads on both side) and the four screws used for the transparent cover
- Place the four spacers on the STEbus Universal FPGA Module main board as indicated on the pictures below. Use the screws to attach them on the PCB
- Take care not to damage the copper tracks near the spaces (in case of doubt, place an insulated washer)

NOTE : it is recommended **not** to tighten tightly the screws until the DE0 Nano daughter board is installed

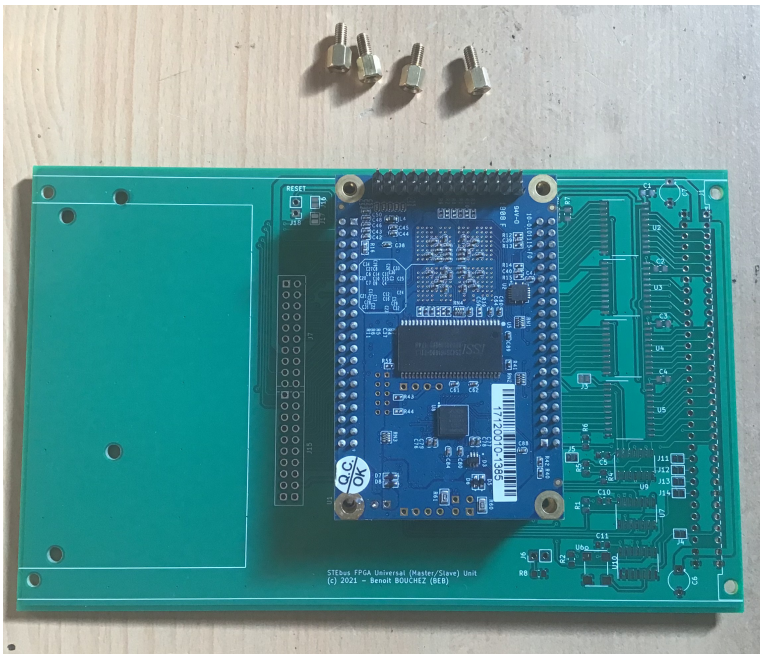


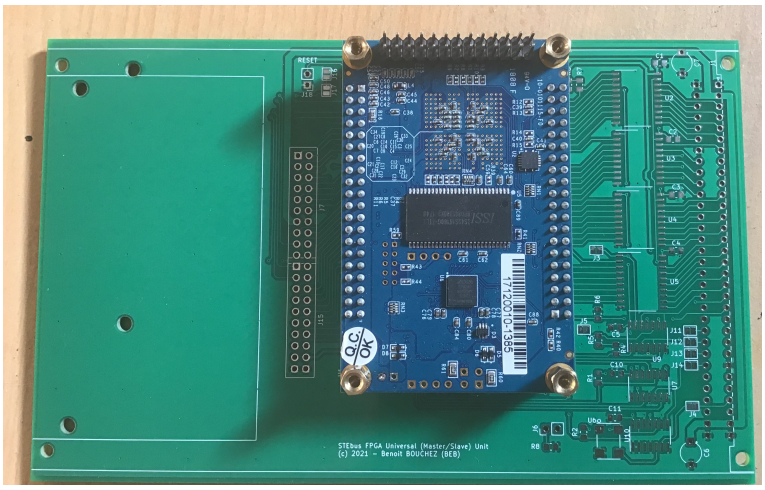


4.1.4 - Installation of DE0 Nano module

- Flip the DE0 Nano to make the Cyclone IV chip facing the Universal Module PCB
- Rotate the DE0 Nano module to have the USB connector on the downside
- Position GPIO0 / GPIO1 headers of DE0 Nano board in front of matching female connectors on the Universal Module. Make sure that all pins are matching between DE0 Nano and Universal FPGA Module
- Press firmly the DE0 Nano daughter board in position so it enters fully in female connectors
- Install the four smaller spaces (male / female spacer) used previously for the plastic cover on four

daughter board corners





Once the four spacers have been reinstalled, the screws can be tightened.

5 - FPGA USER I/O CONNECTOR (J7)

Connector type : male header 2x20 pins 0.1" (2.54 mm) pitch

I/O voltage standard can be modified within Quartus software. It is recommended to use either 3.3V LVCMOS or 3.3V LVTTL for all FPGA I/O on the module.

Connector pin	FPGA pin	Function	Alternate function
1	R13	GPIO14	HOST_D2
2	T12	GPIO15	HOST_D3
3	R12	GPIO16	HOST_D4
4	T11	GPIO17	HOST_D5
5	T14	GPIO12	HOST_D0
6	T13	GPIO13	HOST_D1
7	T10	GPIO18	HOST_D6
8	R11	GPIO19	HOST_D7
9	P11	GPIO110	HOST_A0
10	R10	GPIO111	HOST_A1
11	N12	GPIO112	HOST_A2
12	P9	GPIO113	HOST_A3
13		+5V	
14		0V	
15	N11	GPIO115	nHOST_WR
16	N9	GPIO114	nHOST_OE
17	T9	GPIO1_IN0	nHOST_FPGA_RST
18		Not connected	
19		Not connected	
20	K16	GPIO117	HOST_ATNREQ
21	F13	GPIO10	
22	R9	GPIO1_IN1	
23	T15	GPIO11	
24	L16	GPIO116	
25	L15	GPIO119	
26	R16	GPIO118	
27	P16	GPIO121	
28	P15	GPIO120	
29	N16	GPIO123	
30	R14	GPIO122	
31	P14	GPIO125	
32	N15	GPIO124	

Connector pin	FPGA pin	Function	Alternate function
33	N14	GPIO127	
34	L14	GPIO126	
35	L13	GPIO129	
36		Not connected	
37		Not connected	
38		3.3V (50mA max)	
39		0V	
40		0V	

6 - FPGA DAUGHTER BOARD I/O

The DE0 Nano daughterboard provides 3 more FPGA inputs and 13 more FPGA I/O, available on JP3 connector on the back of the module. JP3 connector also provides 8 analog inputs (ADC128S022 ADC converter located on the DE0 Nano board).

These I/O lines are fully available for user's application.

Connector pin	FPGA pin	Function
1	N/A	3.3V (only use as voltage reference. Do not use as power supply)
2	E15	GPIO2_IN0
3	E16	GPIO2_IN1
4	M16	GPIO2_IN2
5	A14	GPIO20
6	B16	GPIO21
7	C14	GPIO22
8	C16	GPIO23
9	C15	GPIO24
10	D16	GPIO25
11	D15	GPIO26
12	D14	GPIO27
13	F15	GPIO28
14	F16	GPIO29
15	F14	GPIO210
16	G16	GPIO211
17	G15	GPIO212
18	N/A	Analog IN 5
19	N/A	Analog IN 6
20	N/A	Analog IN 7

Connector pin	FPGA pin	Function
21	N/A	Analog IN 3
22	N/A	Analog IN 2
23	N/A	Analog IN 4
24	N/A	Analog IN 0
25	N/A	Analog IN 1
26	N/A	GROUND

Refer to Terasic DE0 User's Manual for details about analog inputs and ADC configuration/control.

7 - FPGA CLOCK

The STEBus Universal FPGA Module uses the DE0 Nano internal clock. This clock is not related by any mean to the STEbus SYSCLK signal.

The DE0 Nano clock is a **50MHz oscillator connected to FPGA pin R8**.

8 - STEbus FPGA I/O

IMPORTANT : all FPGA I/O for the STEbus interface must be configured as 3.3V LVCMOS in Quartus project

Signal	FPGA Pin	Description
nDATACK_IN	A8	Image of STEbus nDATACK line
nDATSTB	D3	Slave : image of STEbus nDATSTB line (input) Master : controls STEbus nDATSTB line (output)
nTFRERR_IN	B8	Image of STEbus nTFRERR line
nADRSTB	C3	Slave : image of STEbus nDATSTB line (input) Master : controls STEbus nDATSTB line (output)
CM2	A2	Slave : image of STEbus CM2 line (input) Master : controls STEbus CM2 line (output)
CM1	A3	Slave : image of STEbus CM1 line (input) Master : controls STEbus CM1 line (output)
CM0	B3	Slave : image of STEbus CM0 line (input) Master : controls STEbus CM0 line (output)
A19	B4	Slave : image of STEbus A19 line (input) Master : controls STEbus A19 line (output)
A18	A4	Slave : image of STEbus A18 line (input) Master : controls STEbus A18 line (output)
A17	B5	Slave : image of STEbus A17 line (input) Master : controls STEbus A17 line (output)
A16	A5	Slave : image of STEbus A16 line (input) Master : controls STEbus A16 line (output)
A15	D5	Slave : image of STEbus A15 line (input) Master : controls STEbus A15 line (output)
A14	B6	Slave : image of STEbus A14 line (input) Master : controls STEbus A14 line (output)
A13	A6	Slave : image of STEbus A13 line (input) Master : controls STEbus A13 line (output)
A12	B7	Slave : image of STEbus A12 line (input) Master : controls STEbus A12 line (output)
A11	D6	Slave : image of STEbus A11 line (input) Master : controls STEbus A11 line (output)
A10	A7	Slave : image of STEbus A10 line (input) Master : controls STEbus A10 line (output)
A9	C6	Slave : image of STEbus A9 line (input) Master : controls STEbus A9 line (output)
A8	C8	Slave : image of STEbus A8 line (input) Master : controls STEbus A8 line (output)
A7	E6	Slave : image of STEbus A7 line (input) Master : controls STEbus A7 line (output)
A6	E7	Slave : image of STEbus A6 line (input) Master : controls STEbus A6 line (output)

Signal	FPGA Pin	Description
A5	D8	Slave : image of STEbus A5 line (input) Master : controls STEbus A5 line (output)
A4	E8	Slave : image of STEbus A4 line (input) Master : controls STEbus A4 line (output)
A3	F8	Slave : image of STEbus A3 line (input) Master : controls STEbus A3 line (output)
A2	F9	Slave : image of STEbus A2 line (input) Master : controls STEbus A2 line (output)
A1	E9	Slave : image of STEbus A1 line (input) Master : controls STEbus A1 line (output)
A0	C9	Slave : image of STEbus A0 line (input) Master : controls STEbus A0 line (output)
D7	D9	STEbus databus bit 7 (bidirectional)
D6	E11	STEbus databus bit 6 (bidirectional)
D5	E10	STEbus databus bit 5 (bidirectional)
D4	C11	STEbus databus bit 4 (bidirectional)
D3	B11	STEbus databus bit 3 (bidirectional)
D2	A12	STEbus databus bit 2 (bidirectional)
D1	D11	STEbus databus bit 1 (bidirectional)
D0	D12	STEbus databus bit 0 (bidirectional)
STE DIR	B12	Controls STEbus databus transceiver direction (output) 0 = databus is read from STEbus 1 = databus is written to STEbus WARNING : this line must always be set in accordance to databus direction in FPGA
nATNREQ_OUT	M10	Normally not used by Master Activates nATNREQx line on STEbus See "STEbus Attention Request lines configuration" chapter for configuration details
nDATACK_OUT	J16	Master : not used. Set as input or set as "1" output Slave : activates nDATACK line on STEbus
nTFRERR_OUT	K15	Master : not used. Set as input or set as "1" output Slave : activates nTFRERR line on STEbus
nATNREQA_IN	J13	**Must be configured as input** Image of nATNREQ0 / nATNREQ2 / nATNREQ4 / nATNREQ6 lines on STEbus See "STEbus Attention Request lines configuration" chapter for configuration details
nATNREQB_IN	J14	**Must be configured as input** Image of nATNREQ1 / nATNREQ3 / nATNREQ5 / nATNREQ7 lines on STEbus See "STEbus Attention Request lines configuration" chapter for configuration details

9 - STEbus Attention Request lines configuration

The STEbus Universal FPGA Board provides support for the eight possible Attention Request lines from STEbus (nATNRQ0 to nATNRQ7). However, in order to save FPGA pins, only two lines can be used by the module at the same time.

The two lines are called "groups" and they are formed of up to four nATNREQx lines.

You can choose which Attention Request line is connected to the group using solder bridges located on the circuit board. In order to use the line within the Universal FPGA Module, you must close one of the bridges.

If a solder bridge is not installed, the corresponding Attention Request line is ignored by the module.

9.1 - Attention Request Group A

Group A is formed of nATNRQ0, nATNRQ2, nATNRQ4, nATNRQ6 lines from STEbus.

J2 = nATNRQ0

J8 = nATNRQ2

J9 = nATNRQ4

J10 = nATNRQ6

9.2 - Attention Request Group B

Group A is formed of nATNRQ1, nATNRQ3, nATNRQ5, nATNRQ7 lines from STEbus.

J11 = nATNRQ1

J12 = nATNRQ3

J13 = nATNRQ5

J14 = nATNRQ7

10 - Buffers disabling

In some special cases, like FPGA debugging, there is a risk of bus contention which may damage electronic components.

The Universal FPGA Module includes a specific option which allows to disable all bus transceivers. When bus transceivers are disabled, they all present a high impedance state to the FPGA, thus eliminating bus contention risks.

To disable bus buffers, install a jumper on J6. This will disable the following signals :

- all address lines (A0 to A19)
- all data lines (D0 to D7)
- CM0, CM1 and CM2 lines
- ADRSTB* line

Note that because of the design of the Universal FPGA Module, the DTASTB* line is not disabled by J6. If you need to disable this line too, the easiest way is to open J3 and J5 (so the module becomes neither Slave, nor Master)

11 - Use with KissBox CPU V4 OEM

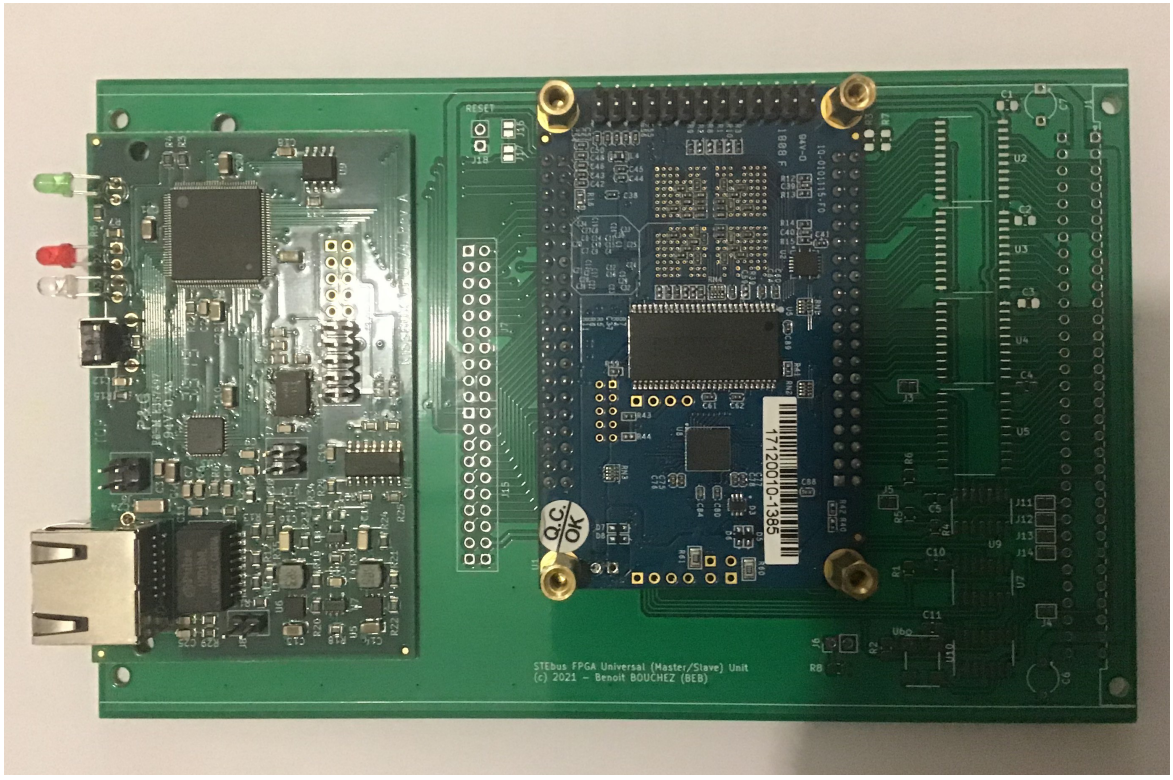
The STEbus Universal FPGA Module is pre-configured to receive a KissBox CPU V4 OEM as an optional host. This host provides extra computing power (KB CPU V4 is based on a dual-core 500MHz 32 bits CPU) and direct Ethernet connectivity.

Note that the KissBox CPU is absolutely not required to use the FPGA module.

Alternate functions described in chapter 5 are the ones of the KissBox CPU V4 parallel bus. Pin assignation can be changed depending on the firmware loaded in the KB CPU V4.

The use of CPU V4 requires a special flat cable between the CPU and the FPGA main board, as the CPU V4 only uses 20 pins. The other pins on J7 are still available for user application. The FPGA I/O pins on DE0 Nano JP3 are also available when a CPU V4 is installed.

The FPGA Module also provides mounting holes matching the CPU V4 ones.



12 - Use with Raspberry Pi

The STEbus Universal FPGA Module can also be interfaced with a Raspberry Pi via its GPIO connector. Alternate signals for J7 are specifically selected to allow the Raspberry to operate in SMI GPIO mode for the fastest possible communication. It is also possible to use SPI communication between the Raspberry and the FPGA.

Note that a special adapter is needed between the Raspberry and the Universal FPGA Module, as the Raspberry GPIO pinout is not directly compatible with J7 alternate functions (without this adapter, a direct connection between the Raspberry and the FPGA board would use the 40 pins, with most of the pins not being reachable by another application)

The Raspberry adapter uses the same pinout as the KB CPU V4, freeing the same FPGA pins.

It is not intended for the Raspberry board to be attached directly on the FPGA module. The Raspberry must be deported from the main board, otherwise access to USB/Ethernet/HDMI connectors becomes almost impossible when the Universal FPGA Module is installed into an Eurorack.

13 - Document revisions

Date	Auteur	Version	Description
05/12/2020	B.Bouchez	1.0	First version

Prepared with OpenOffice Writer software.