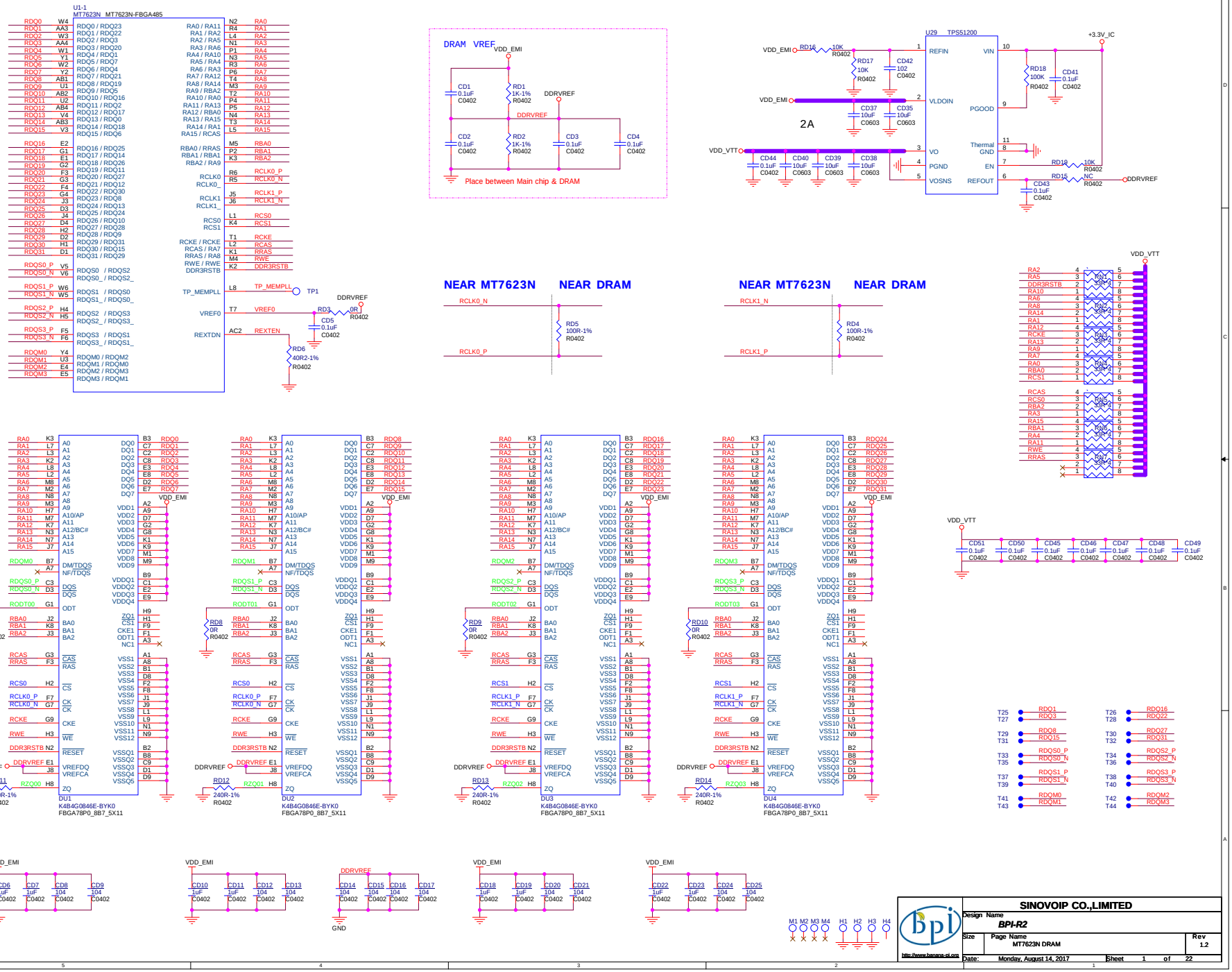
01 MT7623N DRAM



Design Name	BPI-R2
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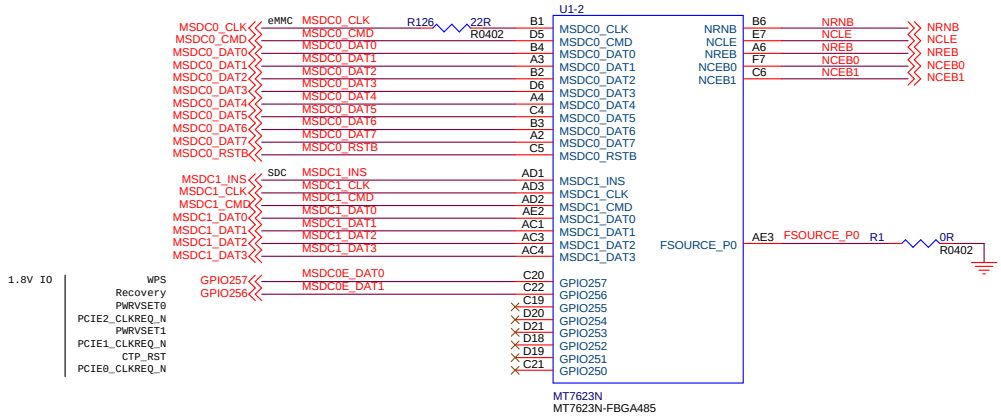
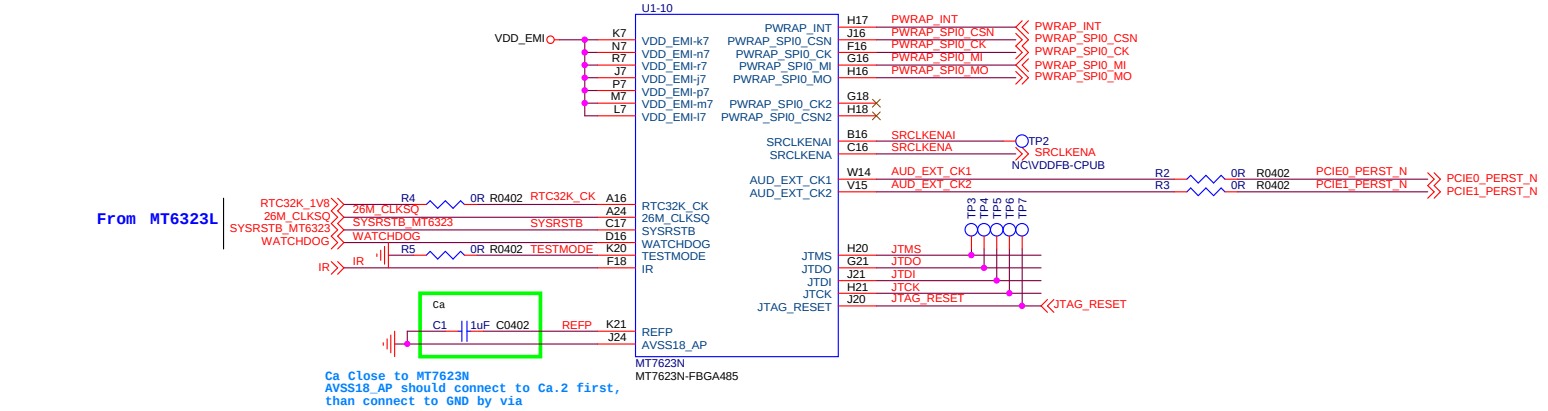
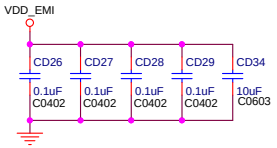
02 MT7623N MSDC /PMIC Interface







SINOVOIP CO.,LIMITED		
Design Name: BPI-R2		
Size	Page Name: MT7623N MSDC /PMIC Interface	Rev 1.2
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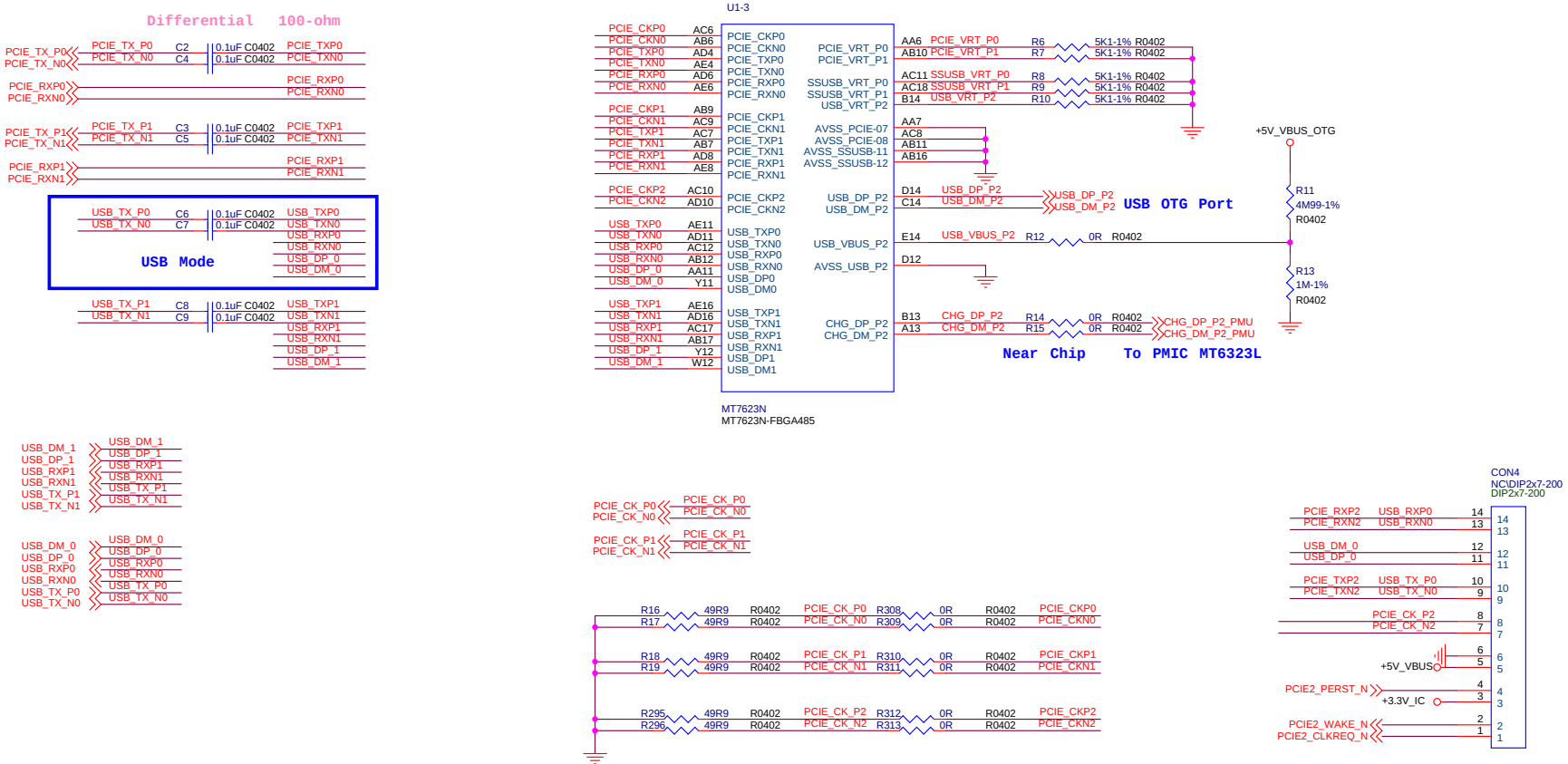
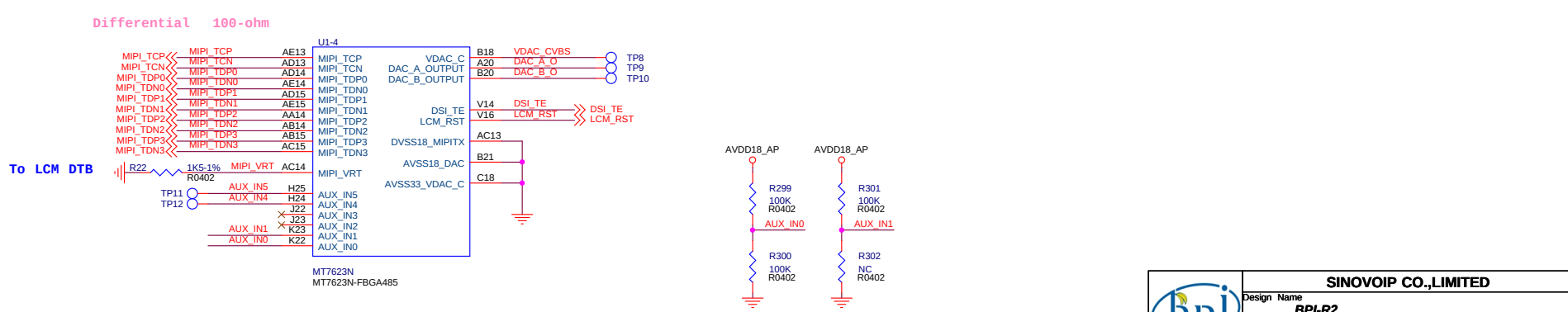
03 MT7623N HIF /PCIe /MIPI /USB





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Design Name: BPI-R2			
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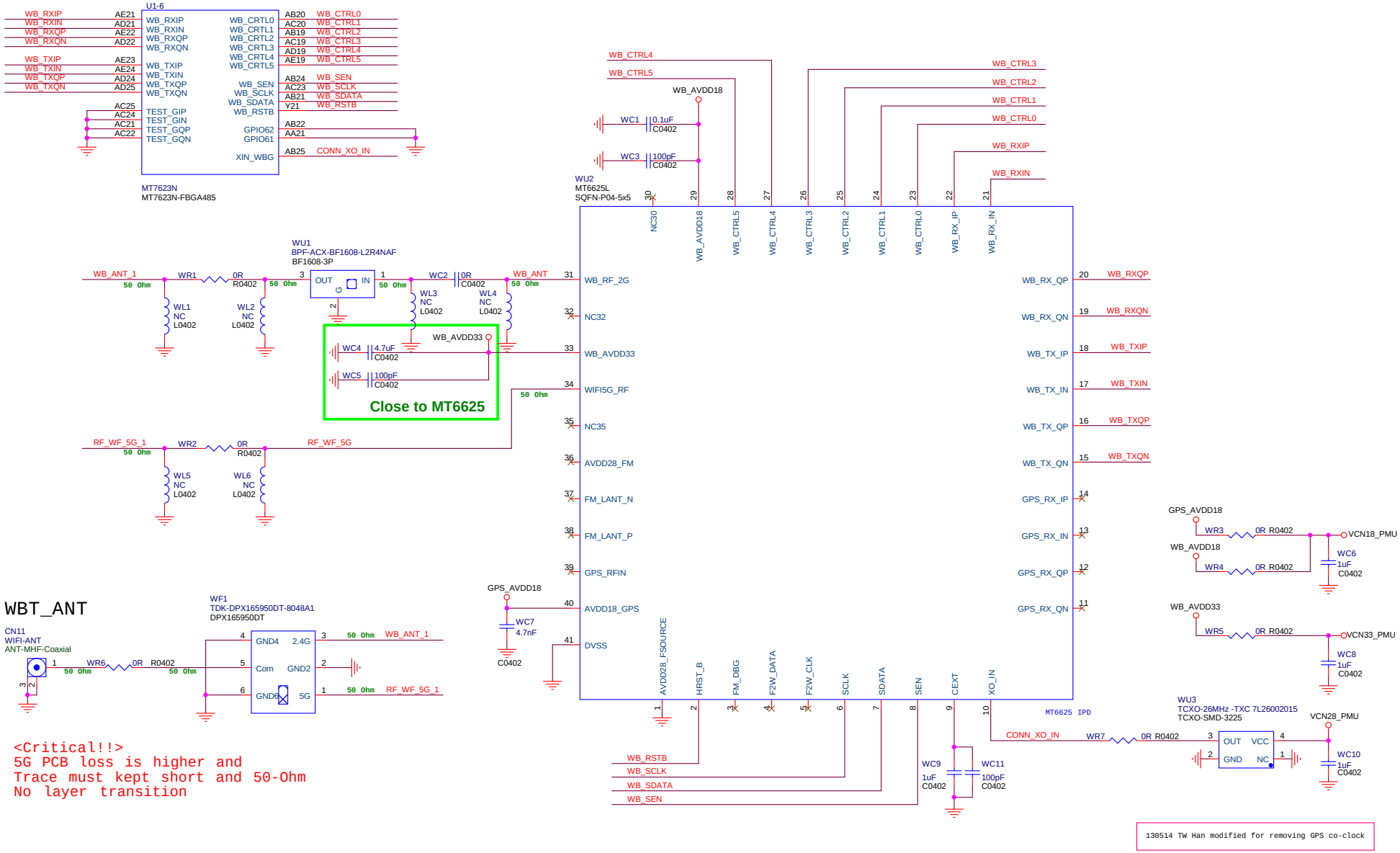
04 MT7623N ConnSYS/ WiFi



<Critical!!>
5G PCB loss is higher and
Trace must kept short and 50-Ohm
No layer transition

130514 TW Han modified for removing GPS co-clock

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	Design Name: BPI-R2	
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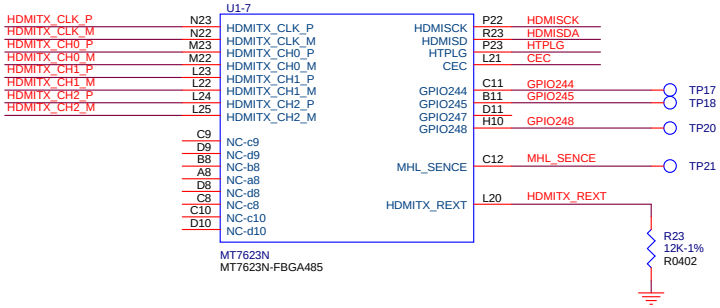
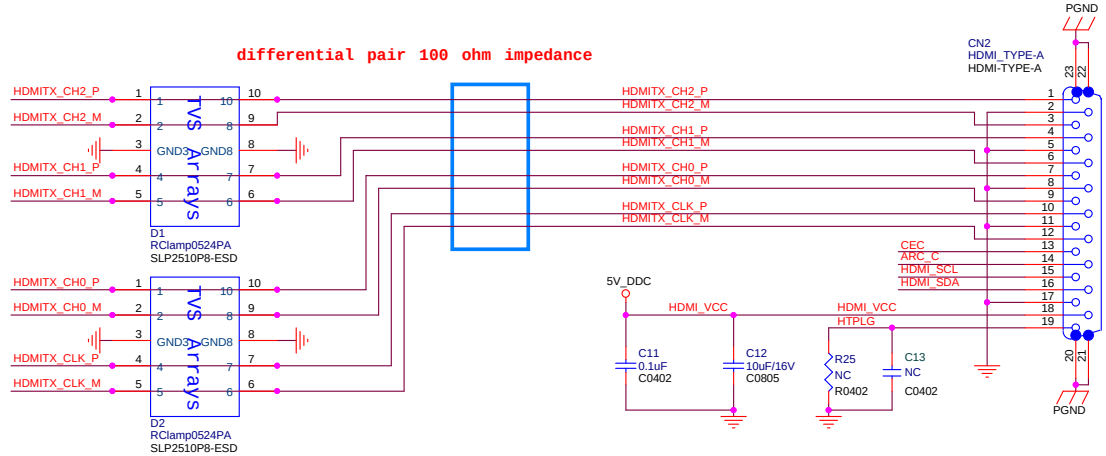
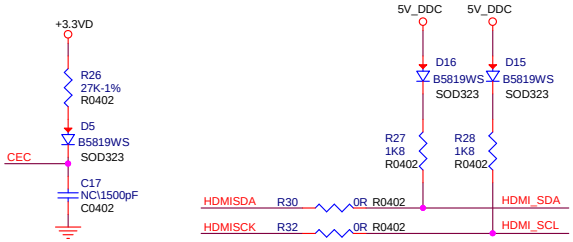
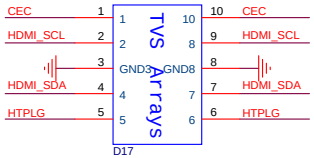
05 MT7623N HDMI

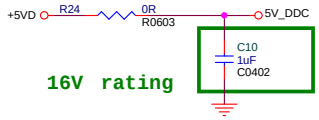


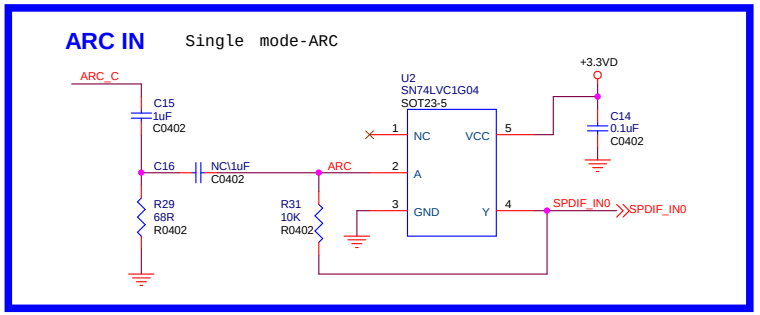
differential pair 100 ohm impedance











	SINOVOIP CO.,LIMITED		
	Design Name: BPI-R2		
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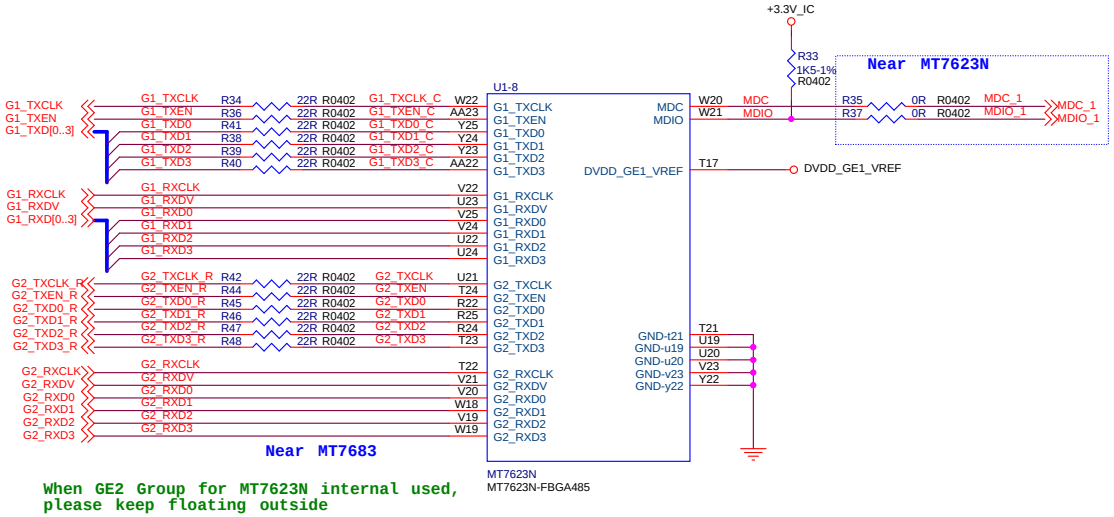
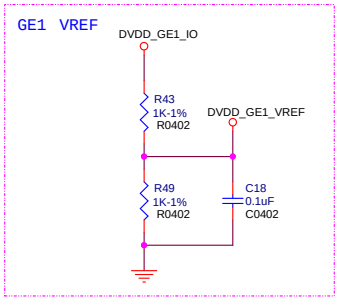
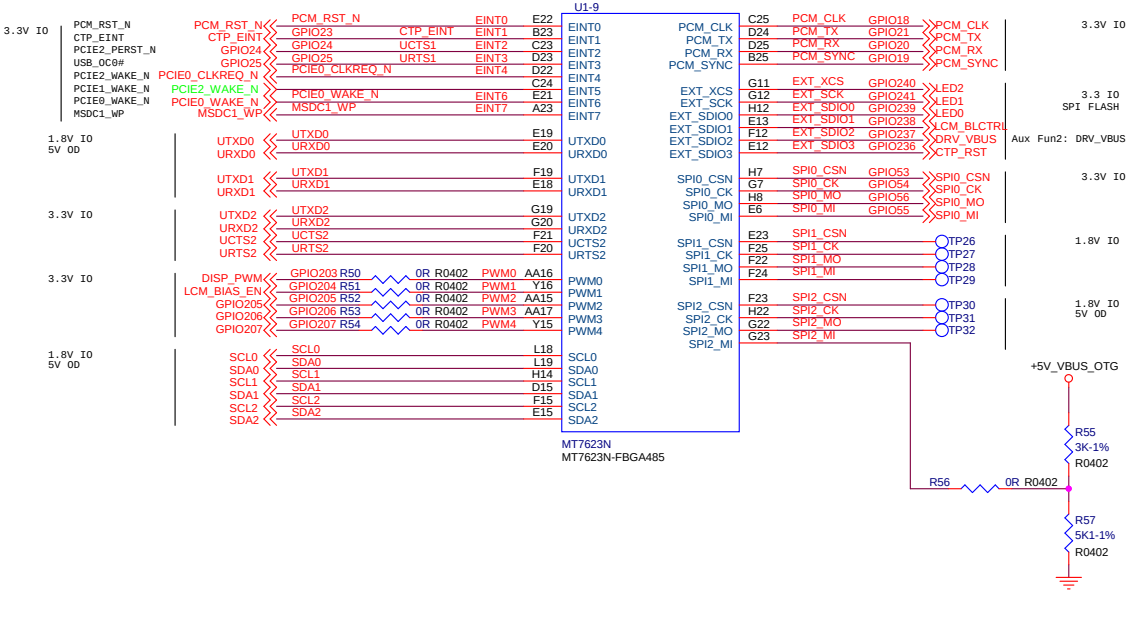
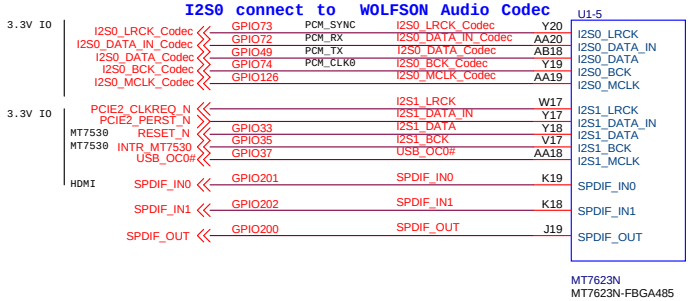
06 MT7623N RGMII /Baseband /I2S









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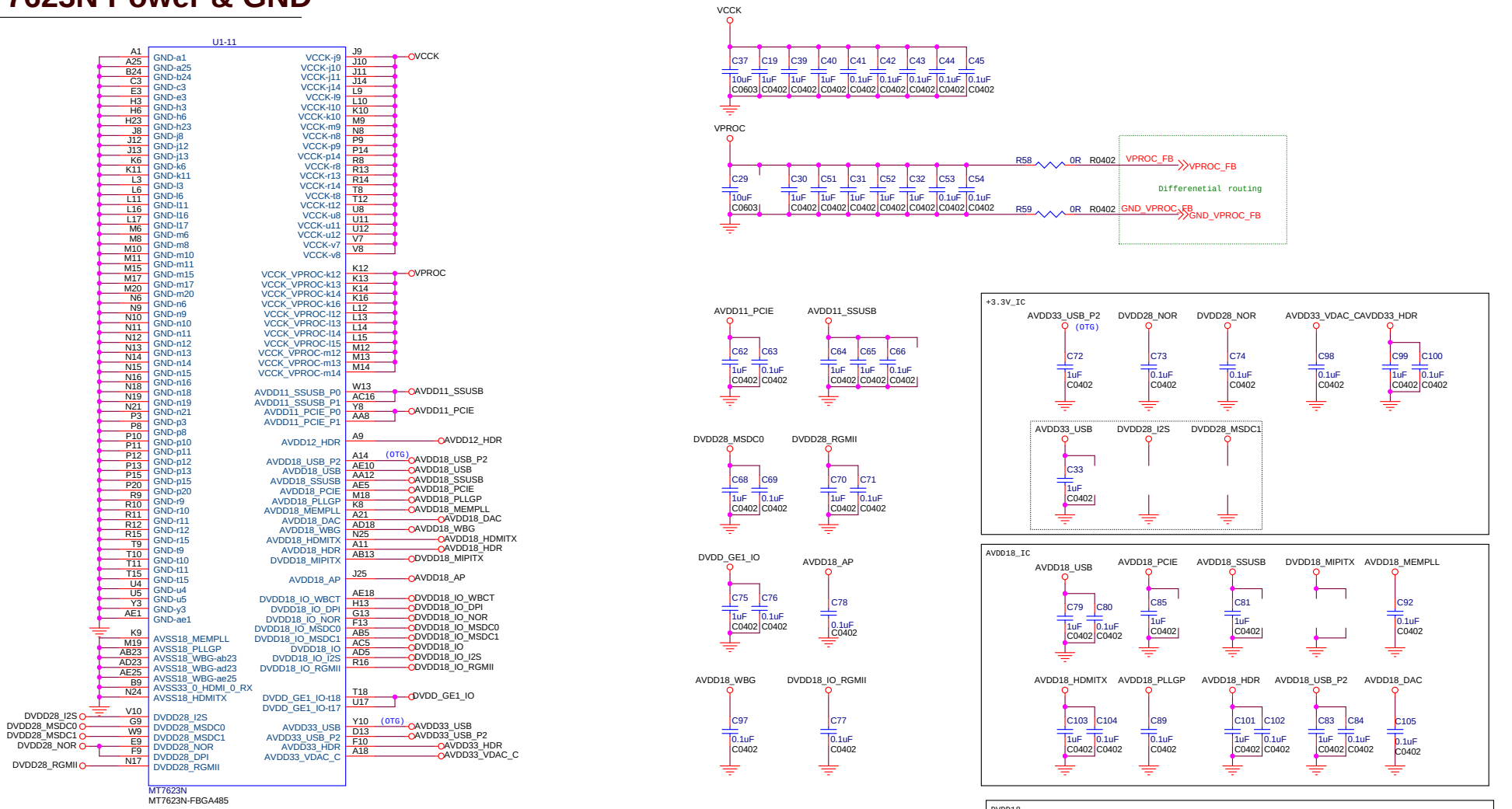
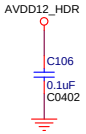
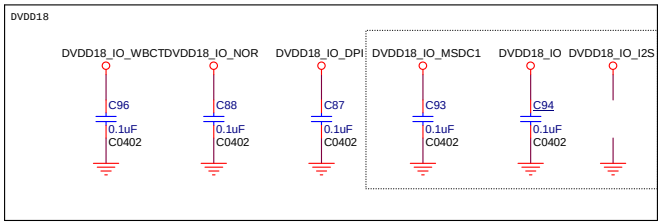
07 MT7623N Power & GND







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08 MT6323L PMIC

Symbol	LPDDR2/1.2V	PCDDR3L/1.35V	PCDDR3/1.5V	LPDDR1/1.8V	Default
SPI_CSN	H	L (20K)	H	L (20K)	PD
AUD_MOSI	L	H (20K)	H (20K)	L	PH

VIO18_PMU — RP2 NC\20K R0402 — PWR_SPI_CSN (Weakly pull high) — RP3 20K R0402

VIO18_PMU — RP4 20K R0402 — AUD_DAT_MOSI

Indicator LED

VBAT

D6 LED-R LED0805 — D7 LED-G LED0805 — D8 LED-B LED0805

Red — ISINK1

Green — ISINK0

Blue — ISINK2

U3 MT6323L MT6323L-TFBGA158

VBAT — RP1 0R R0402 — CP1 4.7uF C0603

SPK_P L1 / SPK_N M1

AU_HSP H4 / AU_HSN H3

AU_HPL J2 / AU_HPR K2

4 mil GND trace with good shielding from baseband (Differential)

1) VPCA7_BB & GND_VPCA7_BB
2) VPCA15_BB & GND_VPCA15_BB
3) DVDD_DVFS & GND_DVDD_DVFS (GND @ bypass-cap)

VBAT_SPK R1 / GND_SPK L2

AU_MICBIAS0 H1 / AU_MICBIAS1 H2

AUDIO: AU_VIN0_P D3 / AU_VIN0_N D4 / AU_VIN1_P G1 / AU_VIN1_N G2 / AU_VIN2_P E2 / AU_VIN2_N E1

DRIVER: ISINK0 C10 ISINK0 / ISINK1 C11 ISINK1 / ISINK2 D11 ISINK2 / ISINK3 B11

VA_PMU — CP2 1uF C0402 — CP3 1uF C0402

AVDD28_ABB J1 / AVDD28_AUXADC D2 / GND_ABB2 F3 / GND_ABB1 K4

ACCDET G3

MT6323_26M_CLK — CLK26M F2

For external PMU use

CHARGER: BATSNS P13 / ISENSE R13 / BATON K3 / VCDT A13 / VDRV P14

CHRLDO R14

Use VBAT PGOOD trigger

PGOOD_R — RP5 NC\1K R0402

CONTROL SIGNAL: PWRKEY P1 / SYSRSTB A1 / RESETB M3 / FSOURCE A10 / INT C7 / EXT_PMIC_EN P12

PWRKEY_R — RP6 1K R0402 — PWRKEY

WATCHDOG — RP7 0R R0402 — PMU_SYSTSTB

SYSRSTB_MT6323 — RP8 0R R0402 — PMU_RESETB

PWRAP_INT — RP9 0R R0402 — PMU_INT

EXT_PWR_EN — RP10 0R R0402 — EXT_PMIC_EN

PMU_TESTMODE N2

AUD_DAT_MOSI — AUD_MOSI B8 / AUD_CLK C8 / AUD_MISO A8

SRCLKENA — RP12 0R R0402 — SRCLKEN_PERI

SRCLKEN A2 / FCHR_ENB N1

TP33

PWRAP_SPI0_CK — RP13 0R R0402 — PWR_SPI_CLK

PWRAP_SPI0_CSN — RP14 0R R0402 — PWR_SPI_CSN

PWRAP_SPI0_MO — RP16 0R R0402 — PWR_SPI_MOSI

PWRAP_SPI0_MI — RP17 0R R0402 — PWR_SPI_MISO

SPI_CLK B10 / SPI_CSN B7 / SPI_MOSI D9 / SPI_MISO B9

VBAT_INPUT: VBAT_VPROC-E14 / VBAT_VPROC-G15 / VBAT_VPROC-F14 / VBAT_VPROC-F15 / VBAT_VPA-A14 / VBAT_VPA-B14 / VBAT_VSYS R7 / VBAT_LDO3-R7 / VBAT_LDO3-P7 / VBAT_LDO2 R5 / VBAT_LDO1 R2

VBAT — 60mil — RP18 0R R0805 60mil — RP20 0R R0402 20mil — RP21 0R R0402 20mil — RP22 0R R0402 20mil — RP23 0R R0402 20mil — RP24 0R R0402 20mil

SOD123 500mW

D9 NC\MMSZ5231BT1G SOD123 VF : 4.85V~5.36V

C107 22uF C0805

Add Zenar Diode Place on the path from VBAT to IC (Battery connector or test point or IO connector)

CP17 4.7uF C0603 / CP18 4.7uF C0603 / CP20 4.7uF C0603 / CP21 4.7uF C0603 / CP22 1uF C0402 / CP23 1uF C0402 / CP24 1uF C0402

VSYS_PMU — RP25 0R R0603 30mil

CP15 10uF C0603 / CP16 10uF C0603

VIO18_PMU — CP19 1uF C0402 20mil — DVDD18_DIG A8 / DVDD18_IO A5

RP26 0R R0402

CP25 1uF C0402

AUXADC_REF — CP31 0.1uF C0402

CP30 0.1uF C0402 — THERM_ADC — AUXADC_VREF18 C2 / AUXADC_AUXIN_GPS B1 / AVSS28_AUXADC B2

CHG_DM_P2_PMU — CHG_DM A11

CHG_DP_P2_PMU — CHG_DP A12

BC 1.1

SIM LVS: SIM1_AP_SCLK C8 / SIM1S1_AP_SIO P11 / SIM1_AP_SRST D8

SIM2_AP_SCLK B6 / SIM2S2_AP_SIO R11 / SIM2_AP_SRST D7

SIM1S1_SCLK N11 / SIM1S1_SIO N12 / SIM1S1_SRST P10

SIM2S2_SCLK M10 / SIM2S2_SIO R10 / SIM2S2_SRST N10

VTCXO_PMU

C108 1uF C0402

X2 TCXO,26MHz,10PPM TCXO-SMD-3225 (VCC, NC, OUT, GND)

26M_CLKSQ — RP27 0R R0402 — 26M_CLKSQ To MT7623

MT6323_26M_CLK — RP28 0R R0402 — To MT6323 PMIC

BUCK OUTPUT

VPROC: VPROC-e15 E15 / VPROC-c15 C15 / VPROC-d15 D15 — LP1 VLS252010ET-R68N IND2520 — VPROC_PMU — CP4 4.7uF C0603

VPROC_FB C13 / GND_VPROC_FB D13

VP: VPA1 A15 / VPA2 B15 — LP2 VLS252010ET-2R2M IND2520 — VGCORE_PMU — CP5 4.7uF C0603

VPA_FB B13

VS: VSYS H15 — VSYS_SW — LP3 VLS252010ET-R68N IND2520 — VSYS_PMU — CP6 4.7uF C0603

ALDO OUTPUT

VA: M4 — VA_PMU — CP13 1uF C0402

VCN28: P2 — VCN28_PMU

VTCXO: N3 — VTCXO_PMU

VCAMA: R3

VCN33: N7 — VCN33_PMU — RP11 0R R0402 — CP7 0.1uF C0402

AVDD33_RTC: C1 — AVDD33_RTC

VRTC

DLDO OUTPUT

VM: J15 — VM_PMU

VRF18: K12 — VRF18_PMU — RP15 0R R0402 — VIO18_PMU — CP8 4.7uF C0603

VIO18: L12

VIO28: P3 — VIO28_PMU — CP9 4.7uF C0603

VCN18: K14 — VCN18_PMU

VCAMD: L15

VCAM_IO: M13

TP34

VEMC_3V3: R6 — VEMC_3V3_PMU — RP19 NC\0R R0402 — DVDD28_RGMII

VMC: M6 — VMC_PMU

VMCH: R4 — VMCH_PMU

VUSB: N6 — VUSB_PMU

VSIM1: R8

VSIM2: P8

VGP1: N8 — VGP1_PMU — VGP1_PMU — CP10 1uF C0402

VIBR: L8

VGP2: M15 — VGP2_PMU — VGP2_PMU — CP11 1uF C0402

VCAM_AF: P6 — VEMC_3V3_PMU — CP12 1uF C0402

VCN33_PMU — CP14 1uF C0402

VMCH_PMU — CP27 1uF C0402

VUSB_PMU — CP28 1uF C0402

VIO28_PMU — CP29 1uF C0402

VREF: P15 — PMU_VREF — CP26 0.1uF C0402 — Must Close to MT6323L — O/P

GND_VREF R15 / GND_LDO31 K7 / GND_LDO30 L6 / GND_LDO29 L9 / GND_LDO28 L11 / GND_LDO27 M12 / GND_LDO26 N13 / GND_LDO25 K10 / GND_LDO24 K11

RTC: RTC_32K1V8 D6 — RTC32K_1V8 — RTC32K_1V8 — TP36

RTC_32K2V8 C5 — RTC32K_2V8

XIN A3 — 32K_XIN

XOUT A4 — 32K_XOUT

X1 32.768KHz, 9pF, 20ppm CRYS-SMD-3215

C109 18pF C0402 / C110 18pF C0402

Close to MT6323L

GND_ISINK E11 / GND_VSYS J12 / GND_VPA G13 / GND_VPROC4 F12 / GND_VPROC3 E11 / GND_VPROC2 G11 / GND_VPROC1 E13 / GND_LDO23 K6 / GND_LDO22 K8 / GND_LDO21 B3 / GND_LDO20 F5 / GND_LDO19 F6 / GND_LDO18 D5 / GND_LDO17 E6 / GND_LDO16 F9 / GND_LDO15 J5 / GND_LDO14 G6

GND_LDO1 J9 / GND_LDO2 J8 / GND_LDO3 J7 / GND_LDO4 H11 / GND_LDO5 H10 / GND_LDO6 E9 / GND_LDO7 J6 / GND_LDO8 H6 / GND_LDO9 H5 / GND_LDO10 G8 / GND_LDO11 G9 / GND_LDO12 G7 — J11

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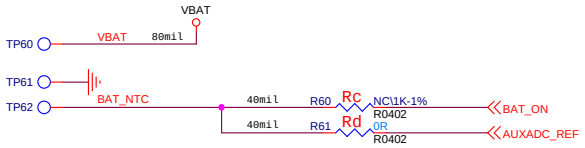
09 MT6323L PMIC VBAT IN

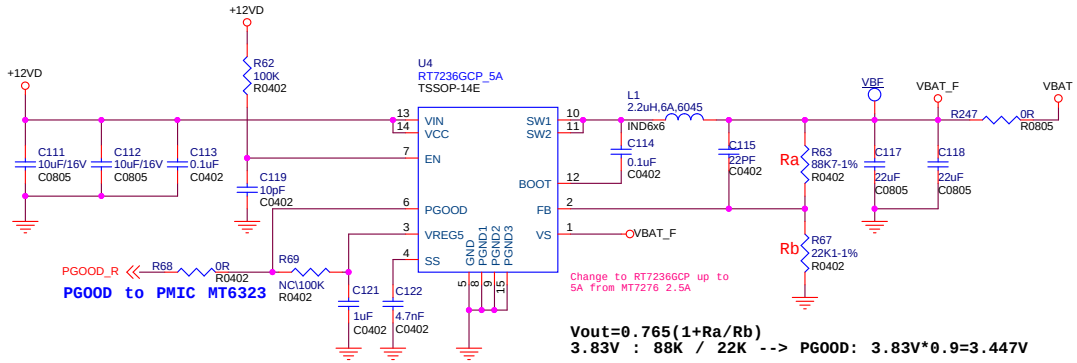


Thermal protection option 1: battery with NTC
(1) if battery NTC is 10kohm; R334=16.9K (+/-1%), R336=27K (+/-1%)
(2) if battery NTC is 47kohm; R334=61.9K (+/-1%), R336=100K (+/-1%)

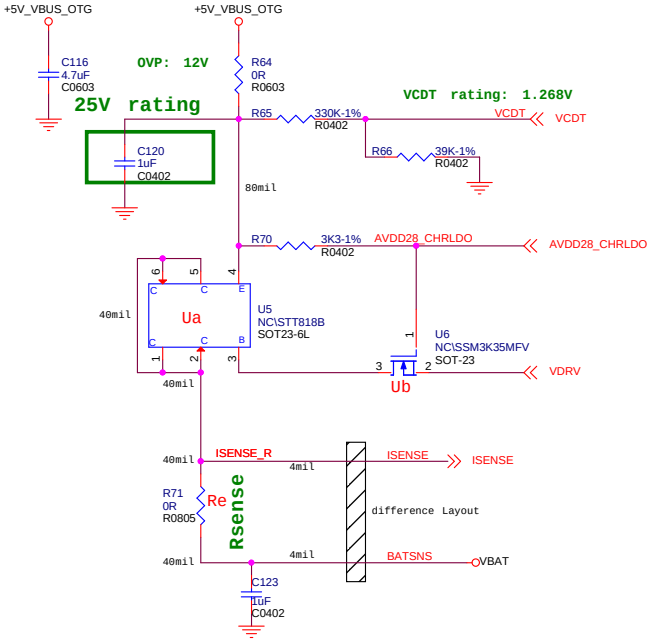
Thermal protection option 2: battery without NTC
(1) Deletc R334, R336
(2) Use R331, NTC301 for thermal protection

緯MT632 3 AUXADC_VREF1 8 PIN ,
and the path need shielding with GND

1. Close to Battery Connector.
(Rsense (R313) <10mm)
2. Main path should be 40mil.
(VBUS -> U301's E, -> U301's C -> R312 -> VBAT)
3. Star connection from R312 to BAT Connector



Vout=0.765(1+Ra/Rb)
3.83V : 88K / 22K --> PGOOD: 3.83V*0.9=3.447V



	Battery mode	Non-Battery mode
Ua	STT818B	NI
Ub	SSM3K35MFV	NI
Re	0.2 ohm/1%	0 ohm
Rc	1K ohm/1%	NI
Rd	16.9K ohn/1%	NI
VR5, VR6	NI/EZJZ0V500AA	NI

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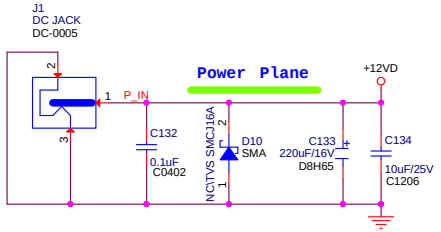
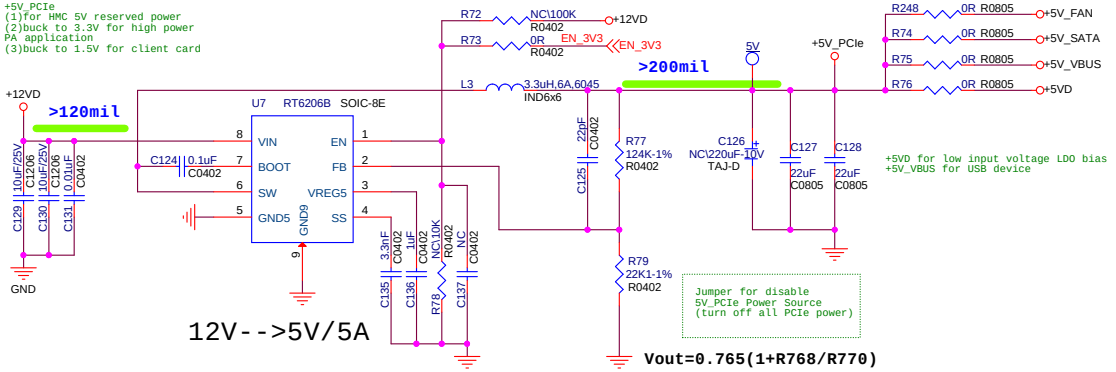
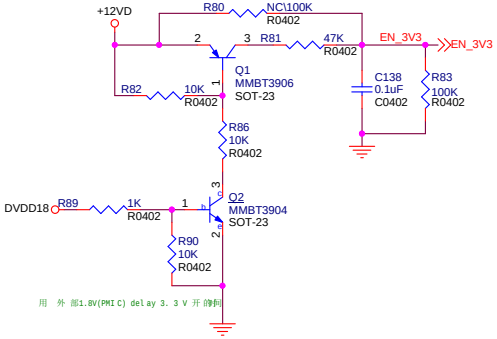
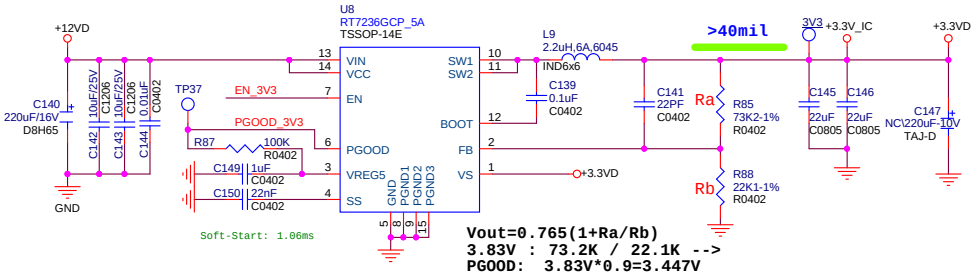
10 PWR +5V/ +3V3/ Vcore

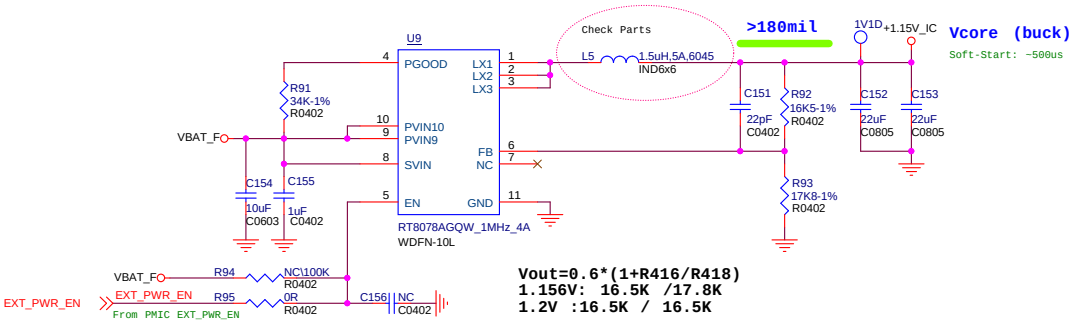




+3.3V_IC:3.3V总 电 流 量测点
To MT7683 / MT7530







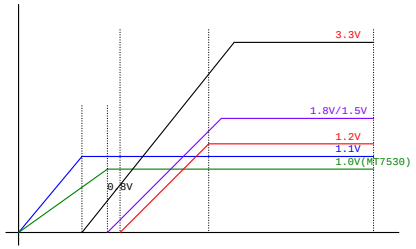


Table 1. Summary of PCI Express Power Supply Requirements

POWER RAIL	×1 CONNECTOR	×4/×8 CONNECTOR	×16 CONNECTOR
12V			
Supply Current	0.5A	2.1A	4.4A (Up to 5.5A)
Capacitive Load	300µF	1000µF	2000µF
3.3V			
Supply Current	3A	3A	3A
Capacitive Load	1000µF	1000µF	1000µF
3.3V$_{AUX}$			
Supply Current	0.375A	0.375A	0.375A
Capacitive Load	150µF	150µF	150µF

Table 2. Summary of PCI Express Mini Card Supply Requirements

POWER RAIL	PRIMARY POWER	AUXILIARY POWER
3.3V		
Peak Supply Current	1A	—
1.5V		
Peak Supply Current	0.5A	—
3.3V$_{AUX}$		
Peak Supply Current	0.33A	0.25A

Note: All values are maximums.

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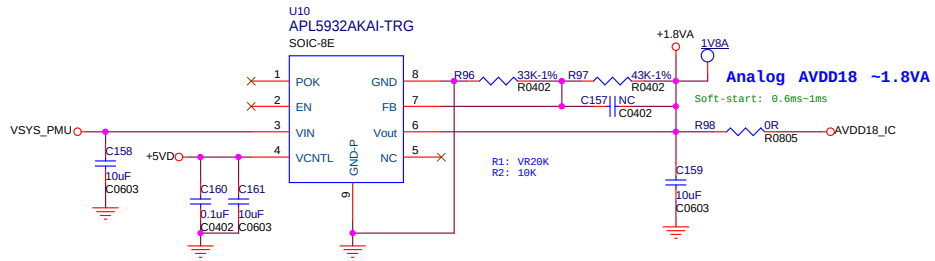
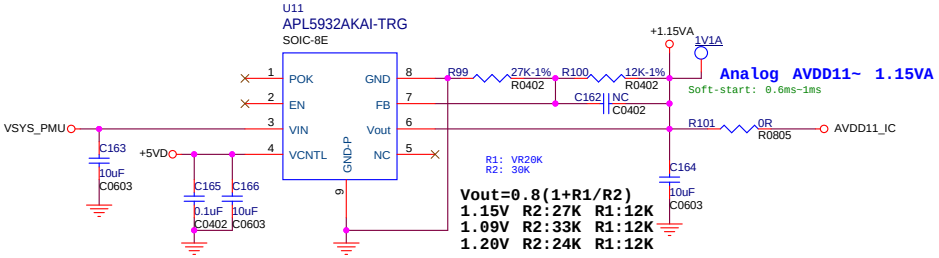
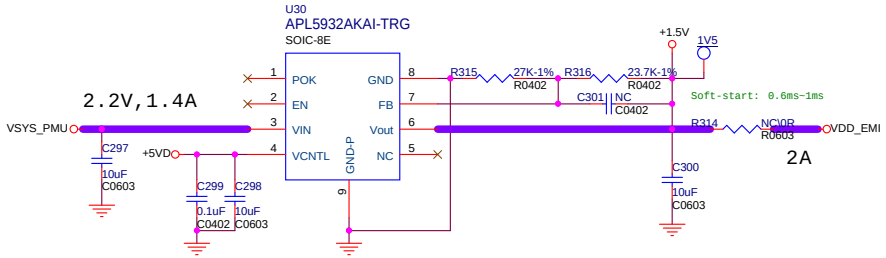
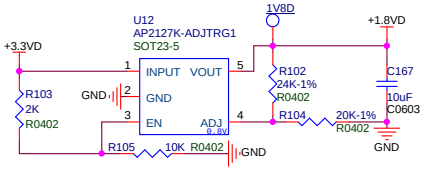
11 PWR External LDO

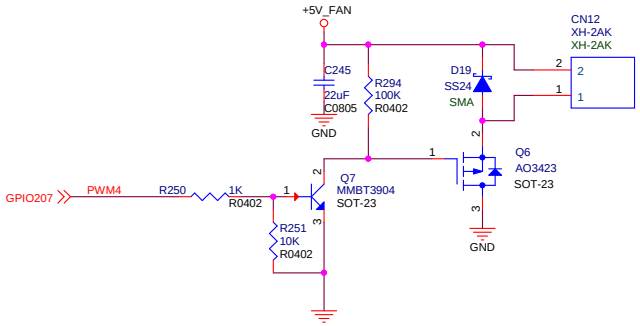






Global Used 1.8V Power





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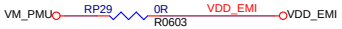
12 Power Connection

1.15V VPROC (CPU) — **Always ON**

BUCK

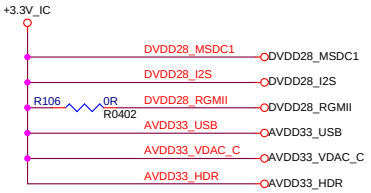
1.35V For DDR3L (DRAM+Controller) — **Always ON**

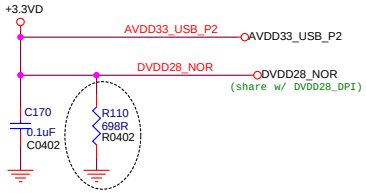
LDO



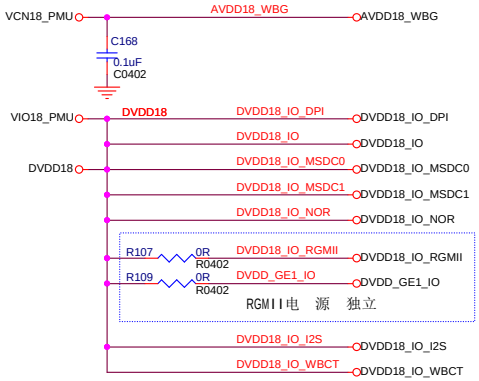
1.0V Giga Core MT7530 — **Always ON**

Always ON



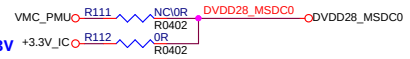


PMIC MT6323L Power Management

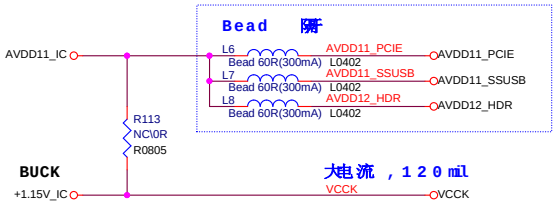


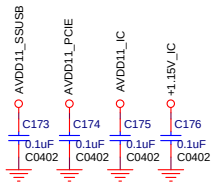
1.8V

Fix 3.3V



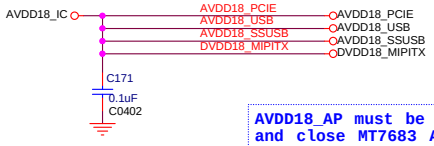
1.15V VCore — **Always ON**



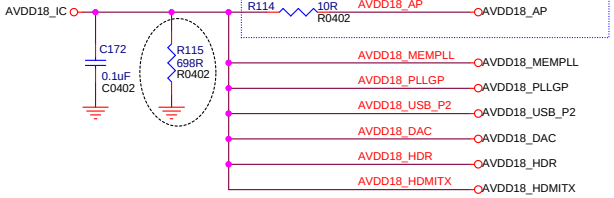


Always ON

AVDD18 Group



AVDD18_AP must be to add 10 ohm and close MT7683 AVDD18_AP pin



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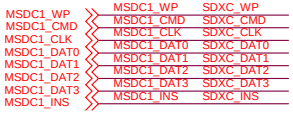
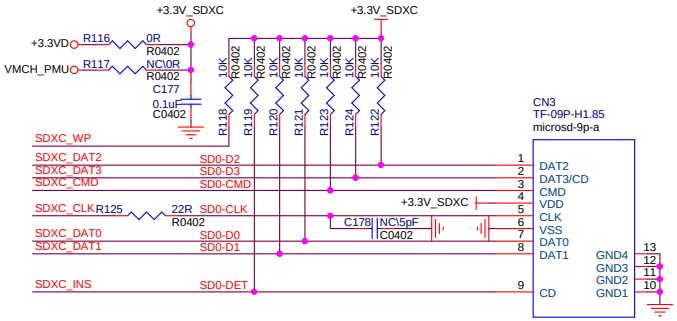
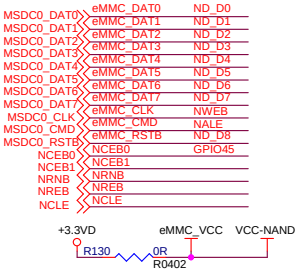
13 MSDC Flash Memory

MSDC1 for SDXC

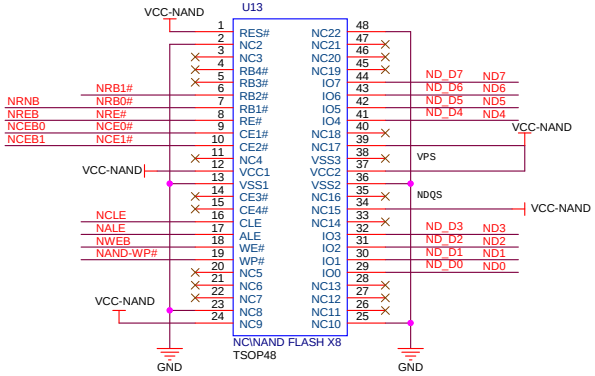


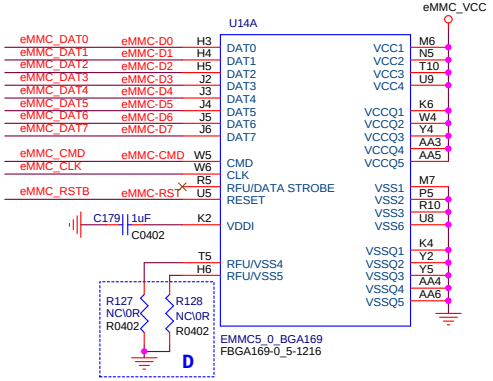


MSDC0 for SLC NAND or eMMC (Default eMMC)

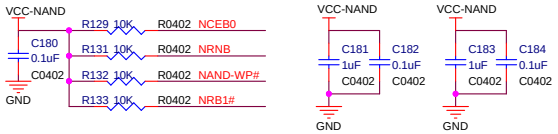


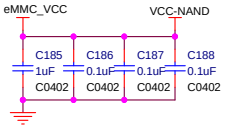
Default Voltage Setting
NAND IO 3.3V
eMMC IO 3.3V
SDXC IO 3.3V

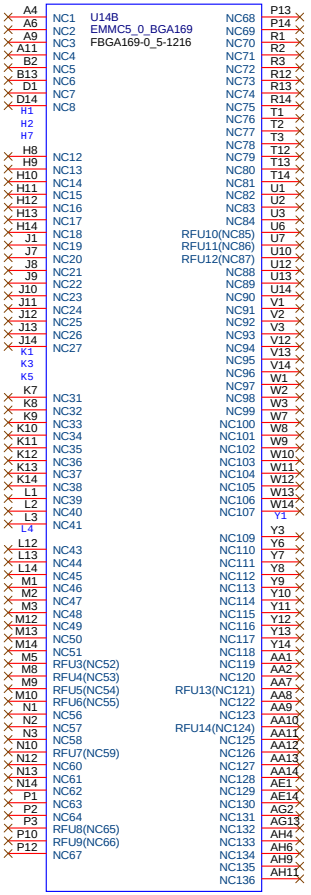




eMMC
VCC: 3.3V
VCCQ: 3.3V



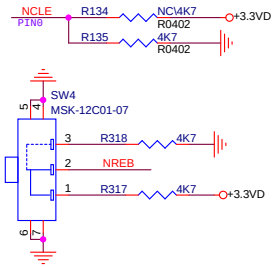


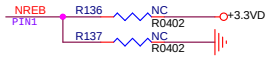


Customized boot order

	0	1	2	3
NREB	L	H	L	H
NCLE	L	L	H	H
1	eMMC	NAND	USB	USB
2	USB	USB	SD	SD
3	SD	SD	eMMC	eMMC
4	NAND	eMMC	NAND	NAND

Default 1 (SD), SW3 switch to 0 (eMMC)





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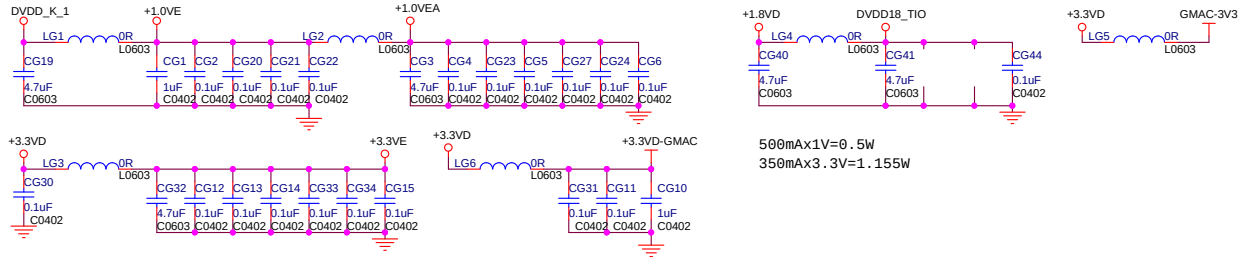
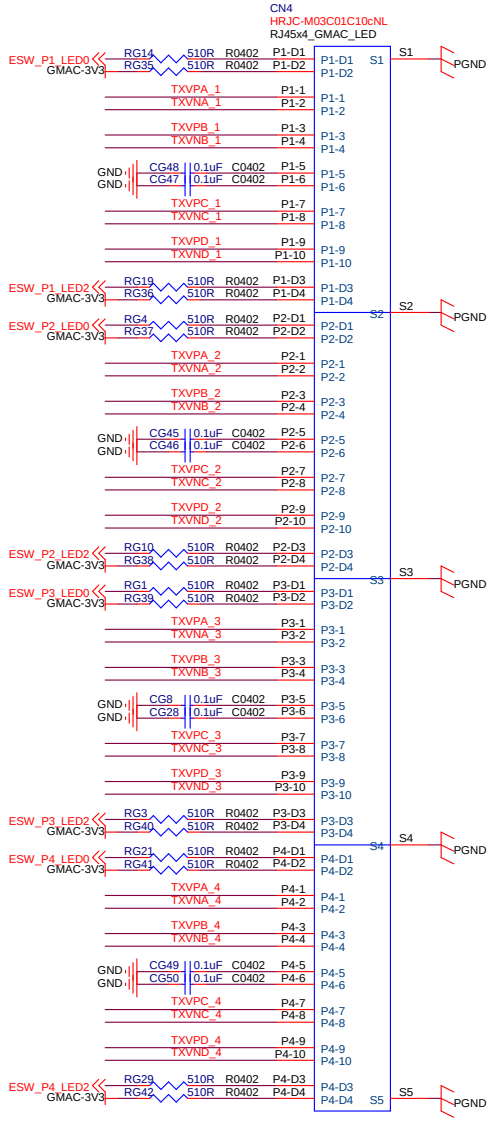
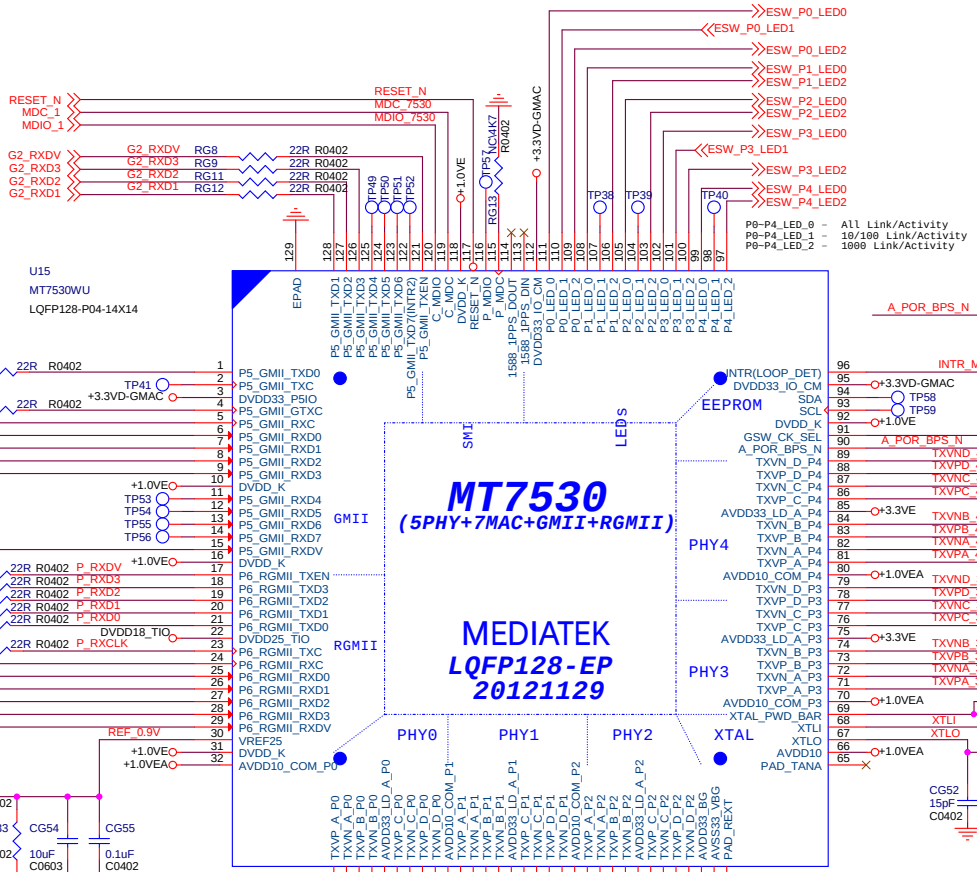
14 MT7530 Giga SW







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	Design Name: BPI-R2		
	Size	Page Name: MT7530 Giga SW	Rev: 1.2
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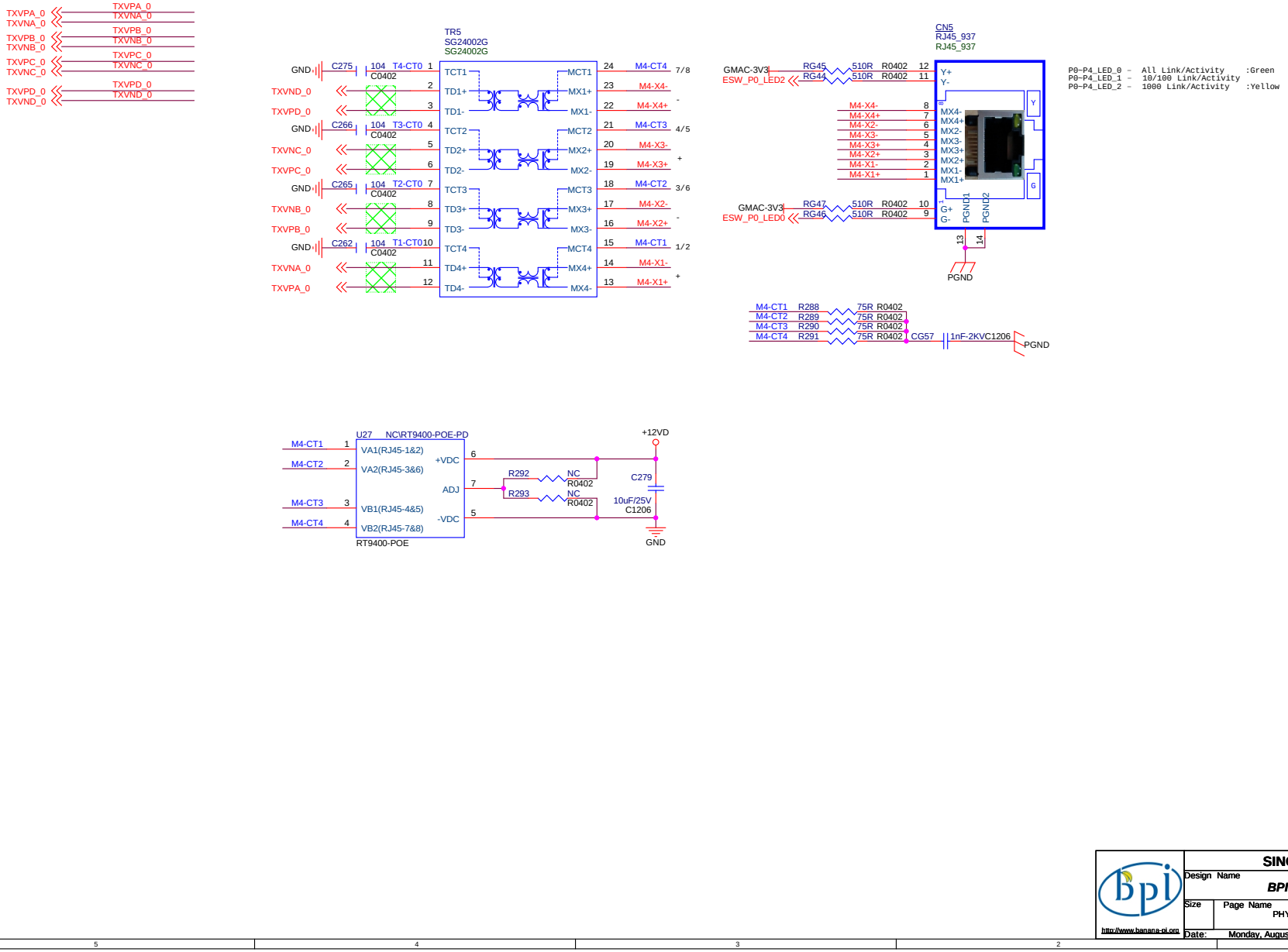
15 PHY0 POE



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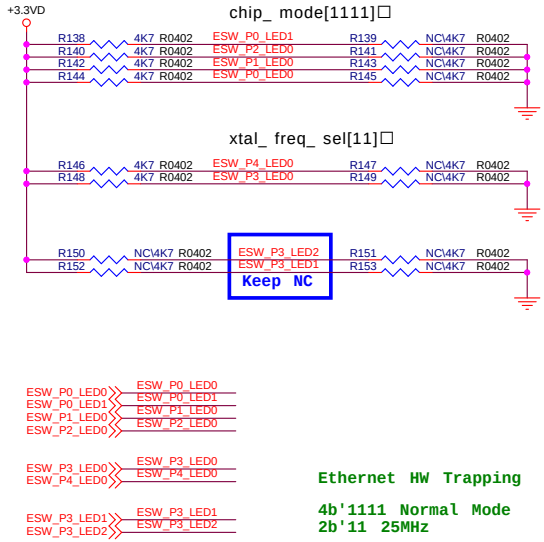
16 Ethernet_Boot Strapping

GigaSwitch Hardware Trap

Pin Name	Trap	Fuction	Description	Default
P0_LED_0	HWTRAP[0]	HT_CHIP_MODE[0]	chip_mode[3:0] 4'b0000: IDDQ mode 4'b0001: IOTEST mode 4'b0010: NANDTREE mode 4'b0011: RING mode (both IO and std-cell) 4'b0100: MBIST 4'b0101: SCAN mode (internal) 4'b0110: SCAN-COMP mode (compression) 4'b0111: SCAN-MBIST-OLT mode 4'b1000: AFE-OLT mode 4'b1001: GPHY ATE mode 4'b1010: GPHY ADUMP mode 4'b1011: GPHY ADUMP probe mode 4'b1100: Reserved 4'b1101: Reserved 4'b1110: bootup probe mode 4'b1111: normal mode	4'b1111
P1_LED_0	HWTRAP[1]	HT_CHIP_MODE[1]		
P2_LED_0	HWTRAP[2]	HT_CHIP_MODE[2]		
P0_LED_1	HWTRAP[3]	HT_CHIP_MODE[3]		
P0_LED_2	HWTRAP[4]	HT_EEPROM_EN	1'b0: disable external EEPROM 1'b1: External EEPROM used	1'b1
P1_LED_1	HWTRAP[5]	HT_C_MDIO_BPS_N	1'b0: Directly access PHY registers via C_MDC/C_MDIO 1'b1: Indirectly access PHY registers	1'b1
P1_LED_2	HWTRAP[6]	HT_P5_INTF_DIS	1'b0: enable 1'b1: disable	1'b1
P2_LED_1	HWTRAP[7]	HT_P5_INTF_MODE	1'b0: GMII/MII 1'b1: RGMII	1'b1
P2_LED_2	HWTRAP[8]	HT_P6_INTF_DIS	1'b0: enable 1'b1: disable	1'b1
P3_LED_0	HWTRAP[9]	HT_XTAL_FSEL[0]	External Crystal Frequency Selection xtal_freq_sel[1:0] 2'b11: 25MHz	2'b11
P4_LED_0	HWTRAP[10]	HT_XTAL_FSEL[1]		
P3_LED_2	HWTRAP[12]	HT_SMI_ADDR[1:0]	chip_smi_addr[4:3] Bits 4 and 3 of the chip SMI address chip_smi_addr[2:0] = 3'b111	2'b11
P3_LED_1	HWTRAP[11]			
P4_LED_1	HWTRAP[13]	HT_P5_INTF_SEL	1'b0: connect to GPHY4 1'b1:connect to GMAC5	1'b1
P4_LED_2	HWTRAP[14]	HT_LOOPDET_DIS	1'b0: loop detection enable 1'b1: loop detection disable	1'b1



Ethernet HW Trapping

4b'1111 Normal Mode
2b'11 25MHz

PU/PD Setting

Pin Name	Fuction	Description	Default
GESW_CK_SEL	Decide gsw_ck frequency	1'b0 : Select 500MHz 1'b1 : Select 200MHz	1'b1
A_POR_BPS_N	Bypass Analog POR Detect	1'b0 : By External Reset Signal Only 1'b1 : By External Reset Signal & Analog logic	1'b1
XTAL_PWDB_N	Crytsal Power Down	1'b0 : SOC Clock 1'b1 : Crytsal Used	1'b1

Hardware Trap for Normal function

Pin Name	Trap	Fuction	Description	Default
P0_LED_2	HWTRAP[2]	EEPROM_EN	1'b0: disable external EEPROM 1'b1: External EEPROM used	1'b1
P1_LED_1	HWTRAP[4]	C_MDIO_BPS_N	1'b0: Directly access PHY registers via C_MDC/C_MDIO 1'b1: Indirectly access PHY registers	1'b1

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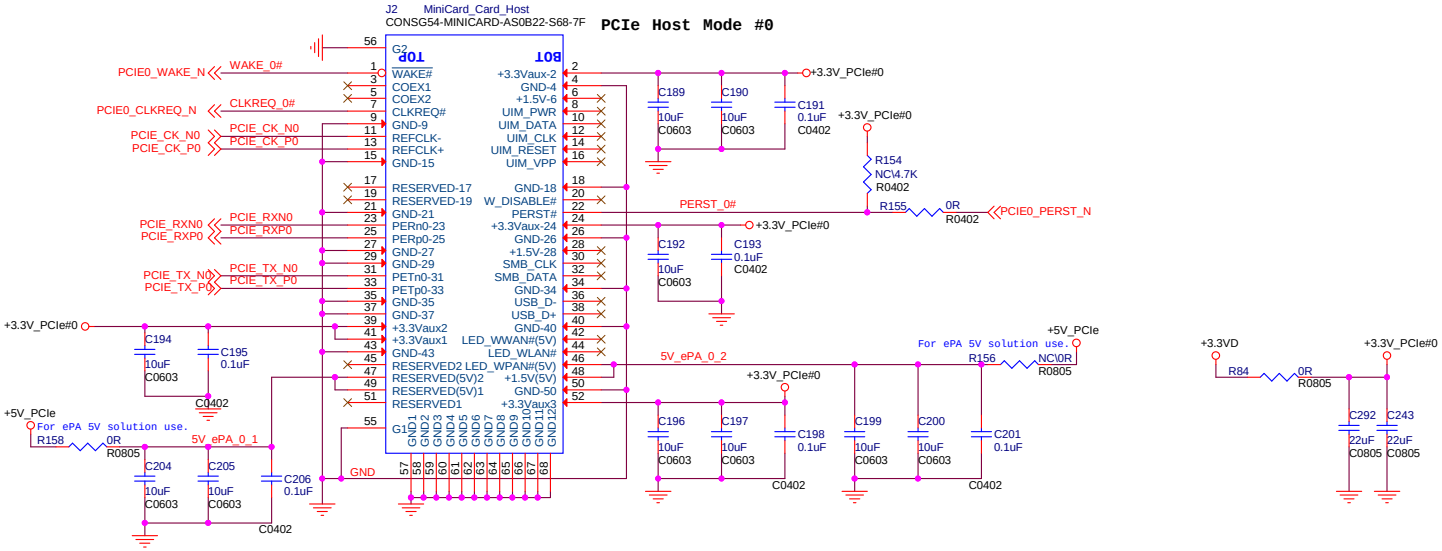
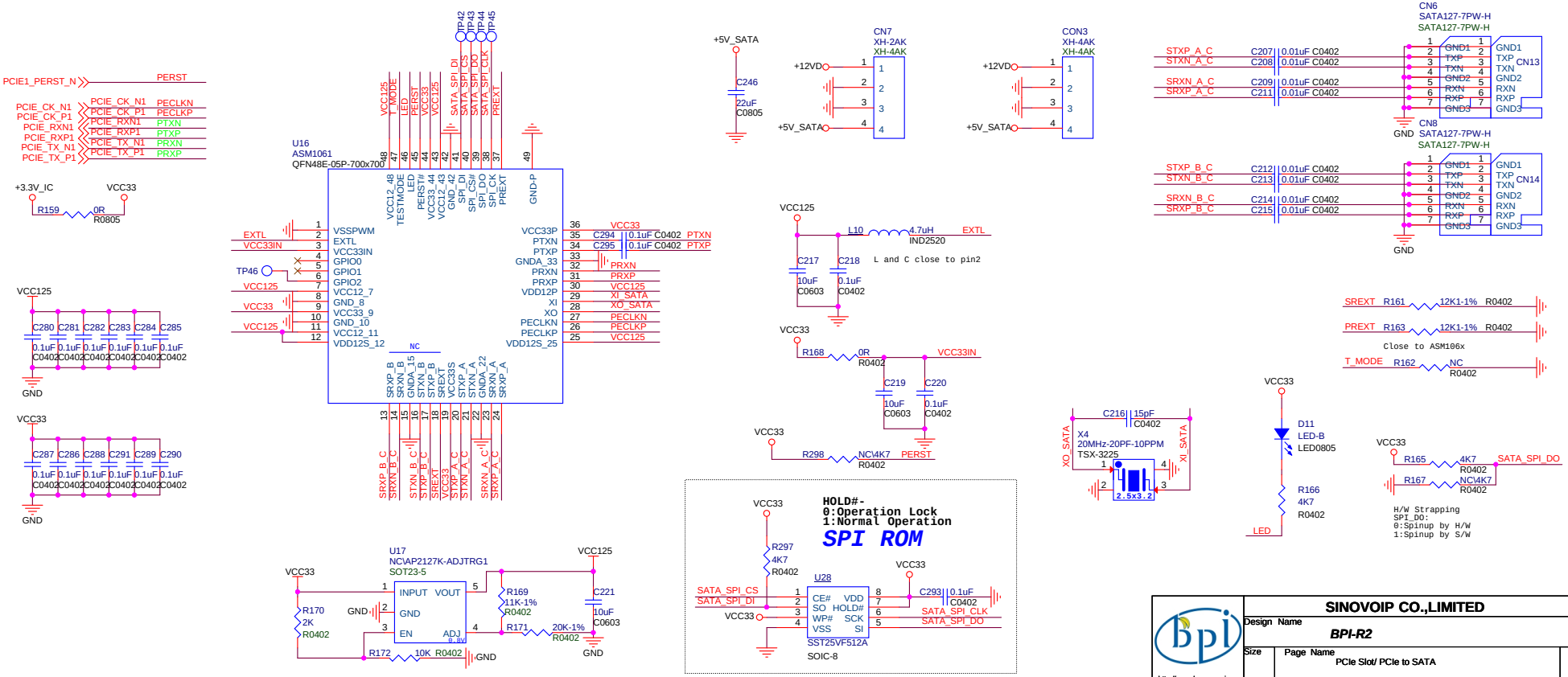
17 PCIe Slot/ PCIe to SATA





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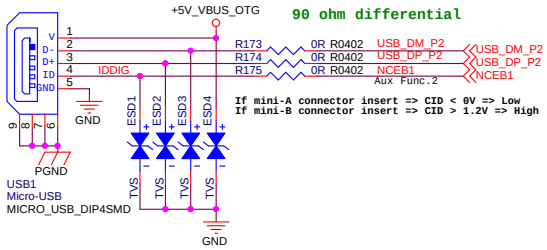
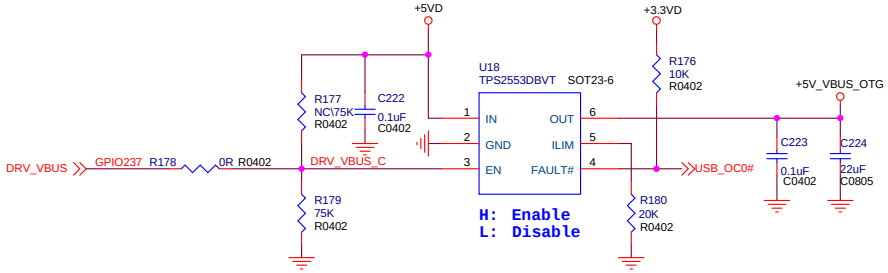
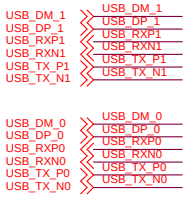
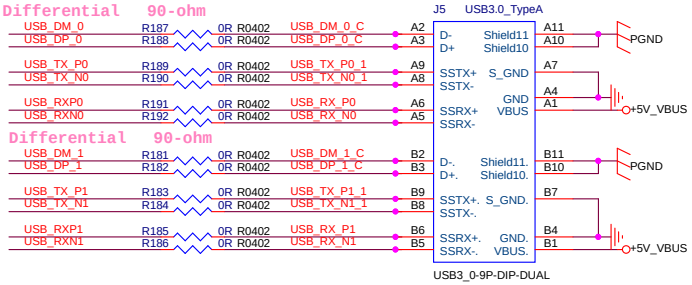
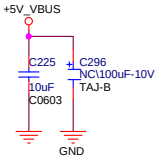
18 USB3.0/ USB OTG

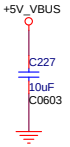












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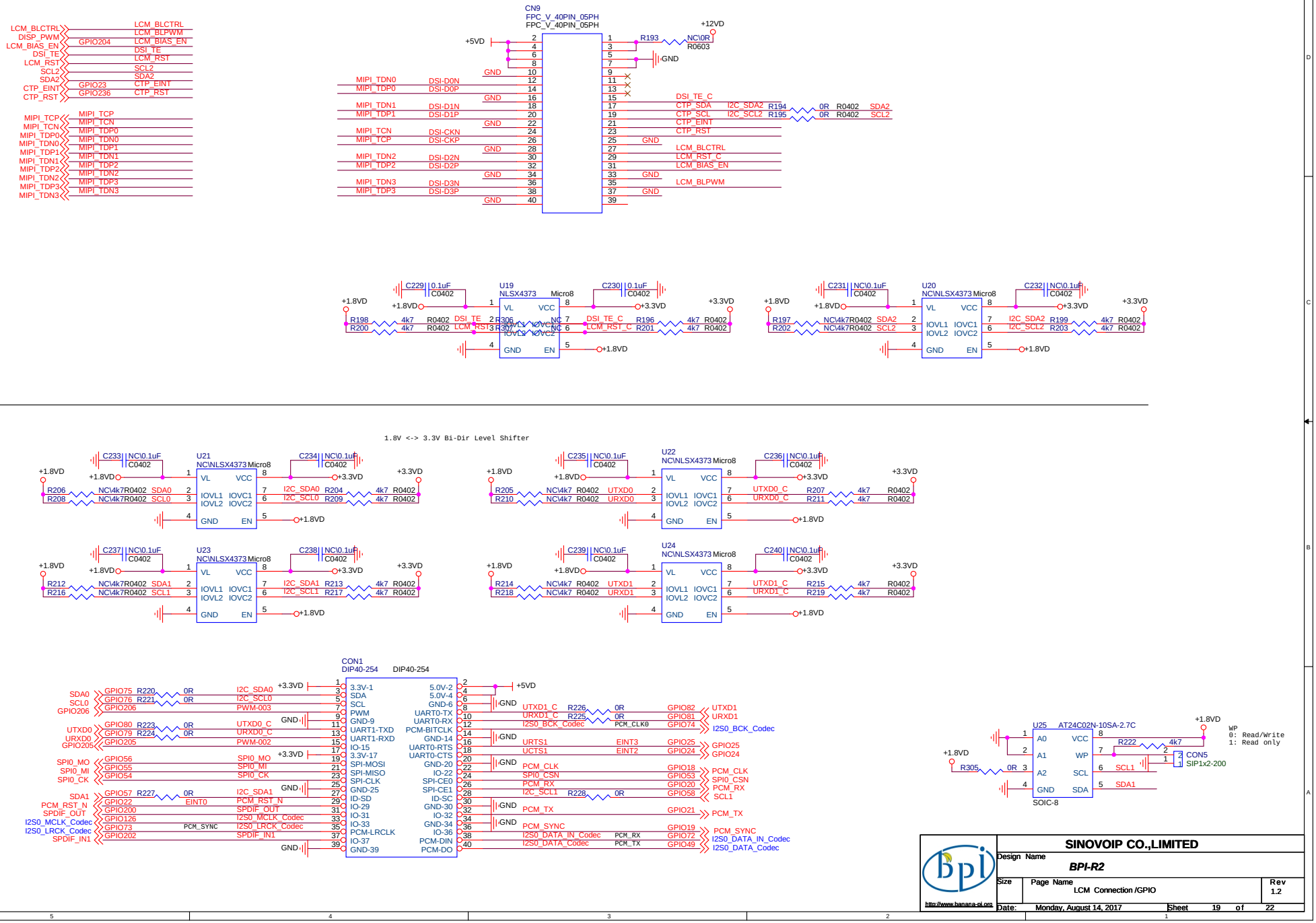
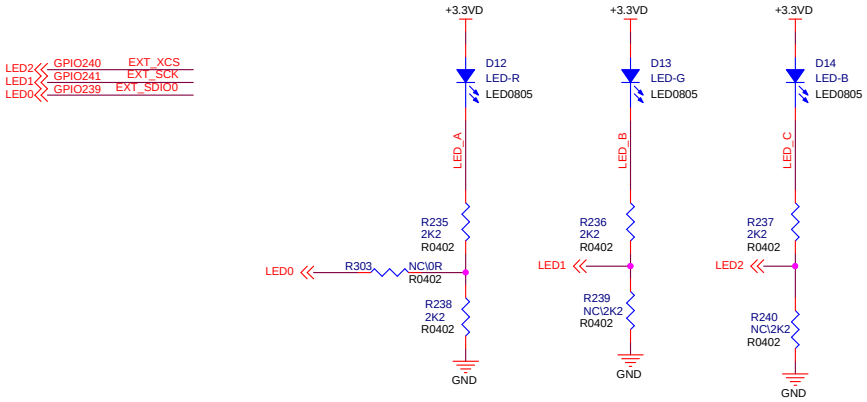
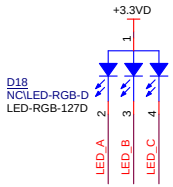
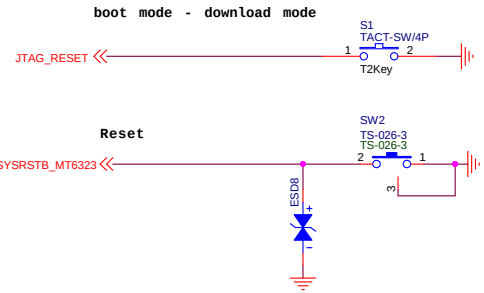
19 LCM Connection/ 40PIN GPIO

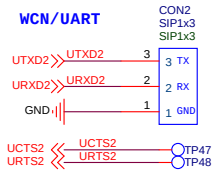


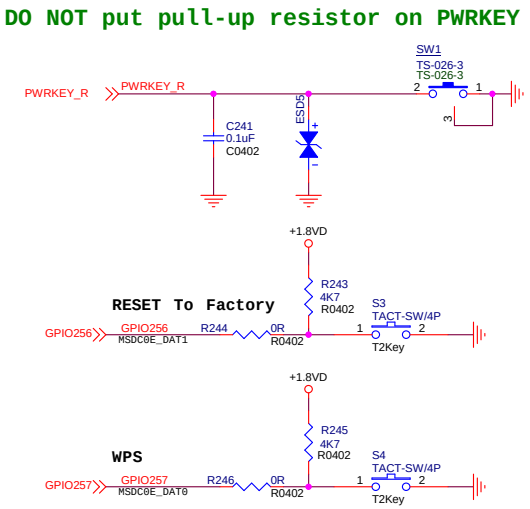
20 LEDs /KEYs /IR

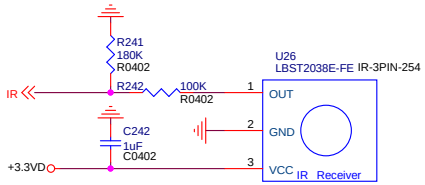












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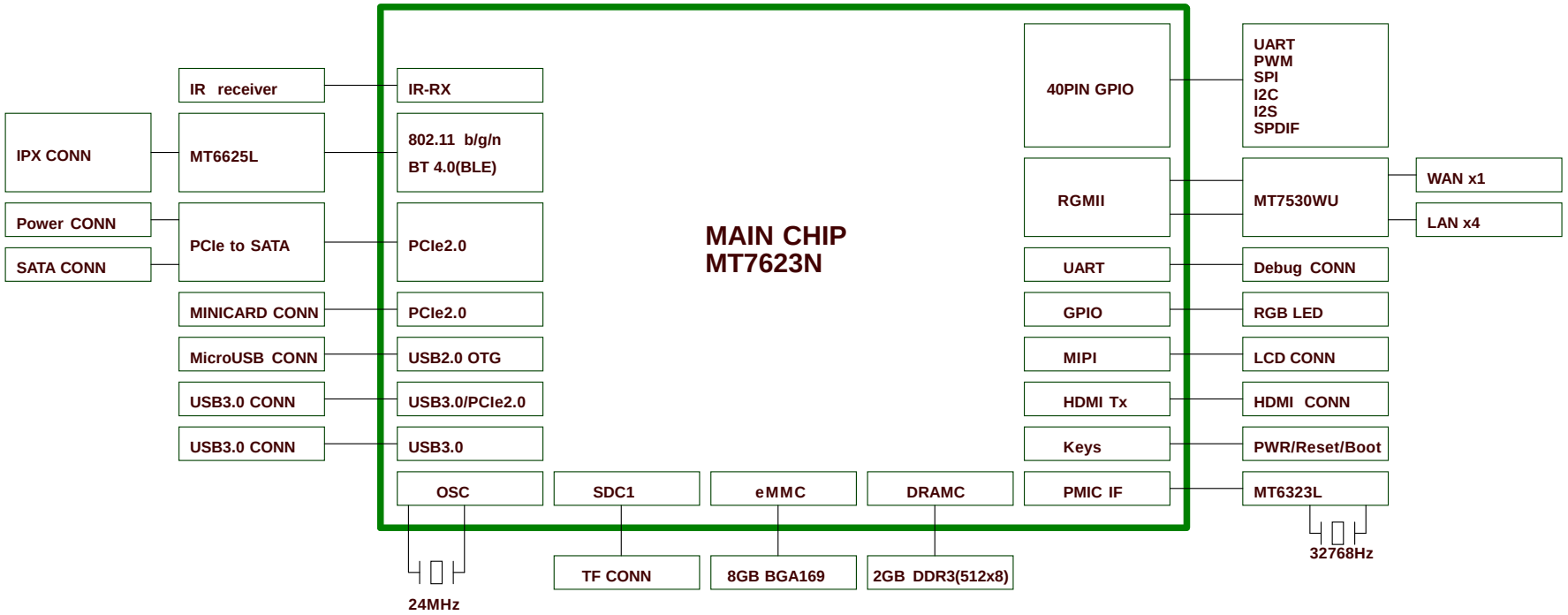

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