

# SIEMENS

## ICs for Consumer Electronics MEGATEXT and MEGATEXT PLUS ICs

SDA 5273 / SDA 5275

SDA 5273-2 / SDA 5275-2

MEGATEXT® and MEGATEXT PLUS ICs SDA 5273 / SDA 5275 SDA 5273-2 / SDA 5275-2 Revision History: 1997-09-01	
Previous Releases: 11.96	
Page	Subjects (changes since last revision)
20	Now also covers SDA 5275-2 and SDA 5273-2 versions; Reset/chip initialization update

## Data Classification

### Maximum Ratings

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

### Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at  $T_A = 25\text{ °C}$  and the given supply voltage.

### Operating Range

In the operating range the functions given in the circuit description are fulfilled.

For detailed technical information about “**Processing Guidelines**” and “**Quality Assurance**” for ICs, see our “**Short Form Catalog**”.

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## MEGATEXT® and MEGATEXT PLUS ICs

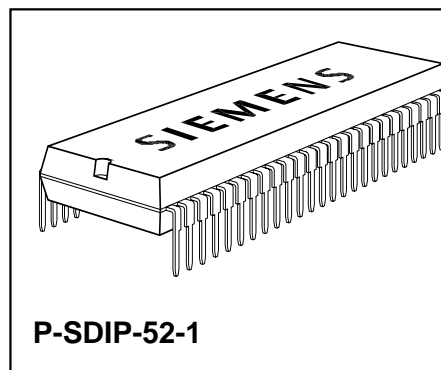
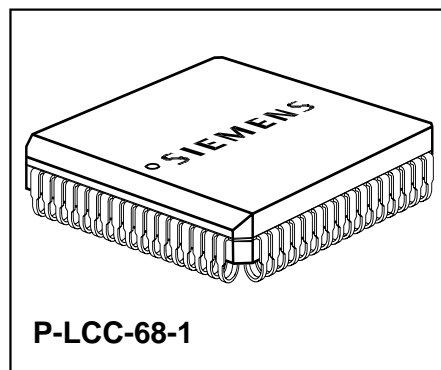
SDA 5273 / 75  
SDA 5273-2 / 75-2

### Preliminary Data

CMOS IC

#### 1 Features

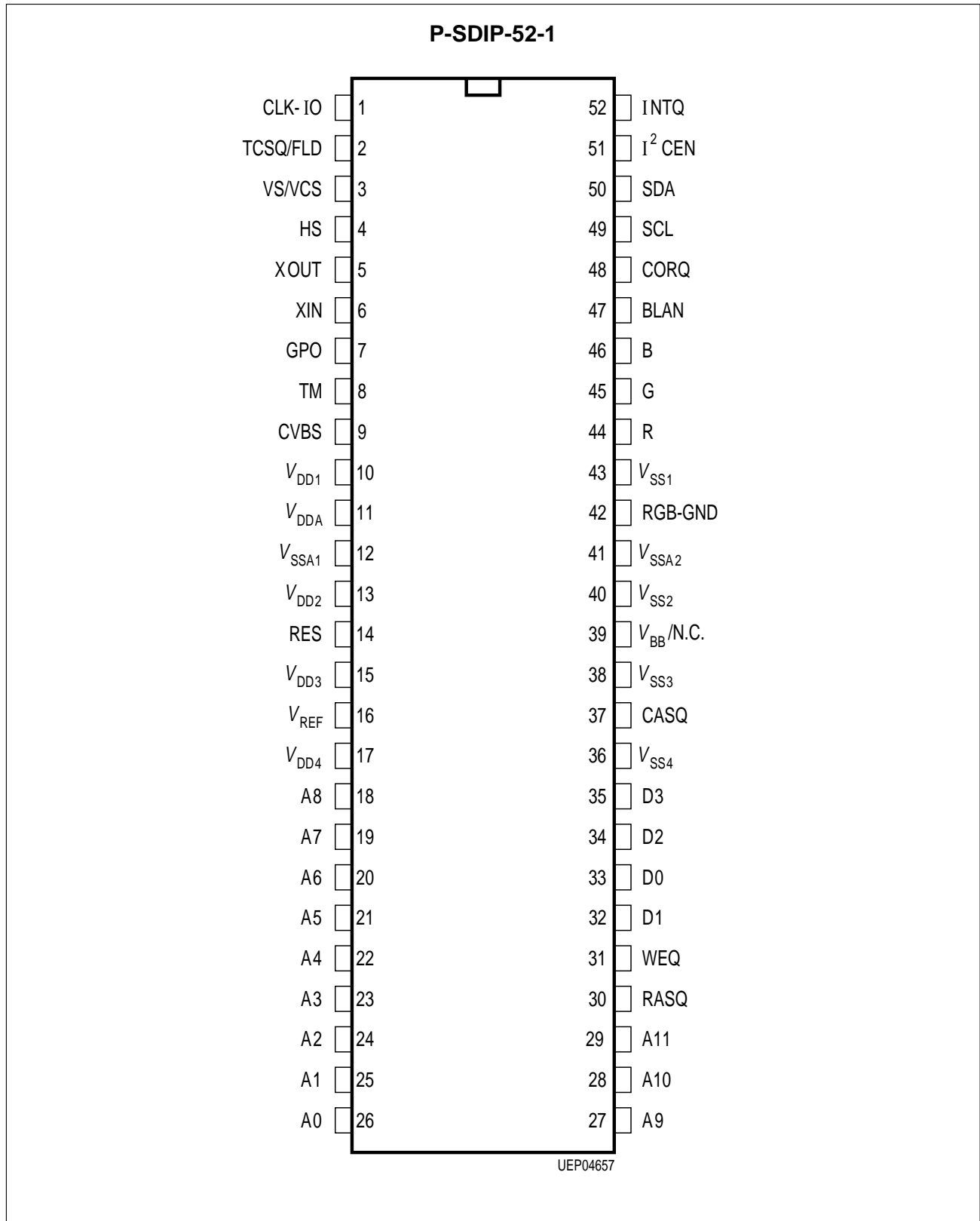
- Single chip teletext IC
- Analog CVBS-input with onchip clamping circuitry
- Slicer
- Supports level 1, 2.5 and 3.5 ETSI teletext standard
- Stores up to 14 teletext pages on chip
- Stores up to 2048 teletext pages with external 16 M memory
- SDA 5275: full level 2.5 processing
  
- Analog RGB-output
- 41 latin script languages
- 12 × 10 character size
- Parallel display attributes
- 64 from 4096 colors selectable
- Enhanced flash modes
- Dynamically redefinable character set (DRCS, PCS)
- Pixel graphics
- Fullscreen display (64 × 32 or 80 × 24 character positions)
- Horizontal and vertical scrolling
- Graphic cursors
- 4:3 and 16:9 display
- Multinorm display (50/60/100/120 Hz)
  
- RISC-processor
- Firmware downloadable
- I<sup>2</sup>C / 3 wire UART-interface (1 Mbit/s)
- Independent clocks for acquisition and display
- Tools for greatly simplified software development
  
- 24-Kbyte on-chip reconfigurable DRAM
- 44160-bit character ROM
- One external crystal for all standards



Type	Ordering Code	Package
SDA 5273 / 75 P	on request	P-LCC-68-1
SDA 5273 / 75 S	on request	P-SDIP-52-1
SDA 5273-2 / 75-2P	on request	P-LCC-68-1
SDA 5273-2 / 75-2S	on request	P-SDIP-52-1
SDA 5273C / 73-2C P	on request	P-LCC-68-1
SDA 5273C / 73-2C S	on request	P-SDIP-52-1

## Pin Configuration

(top view)



## 1.1 Pin Definitions and Functions

Pin No. P-SDIP-52-1	Symbol	Function
1	CLK-IO	System clock input/output
2	TCSQ/FLD	Composite sync output/ field output
3	VS/VCS	Vertical sync input/output
4	HS	Horizontal sync input/output
5	XOUT	20.5-MHz crystal oscillator output
6	XIN	20.5-MHz crystal oscillator input
7	GPO	General purpose output
8	TM	Testpin, leave open or connect to $V_{SS}$
9	CVBS	CVBS-video signal input
10	$V_{DD1}$	+ 5 V digital supply
11	$V_{DDA}$	+ 5 V analog supply
12	$V_{SSA1}$	Analog ground
13	$V_{DD2}$	+ 5 V digital supply
14	RES	Chip reset
15	$V_{DD3}$	+ 5 V digital supply
16	$V_{REF}$	+ 3 V reference voltage input
17	$V_{DD4}$	+ 5 V digital supply
18	A8	External DRAM-address
19	A7	External DRAM-address
20	A6	External DRAM-address
21	A5	External DRAM-address
22	A4	External DRAM-address
23	A3	External DRAM-address
24	A2	External DRAM-address
25	A1	External DRAM-address
26	A0	External DRAM-address
27	A9	External DRAM-address
28	A10	External DRAM-address
29	A11	External DRAM-address
30	RASQ	Row address strobe (DRAM)
31	WEQ	Write enable (DRAM)
32	D1	External DRAM-data

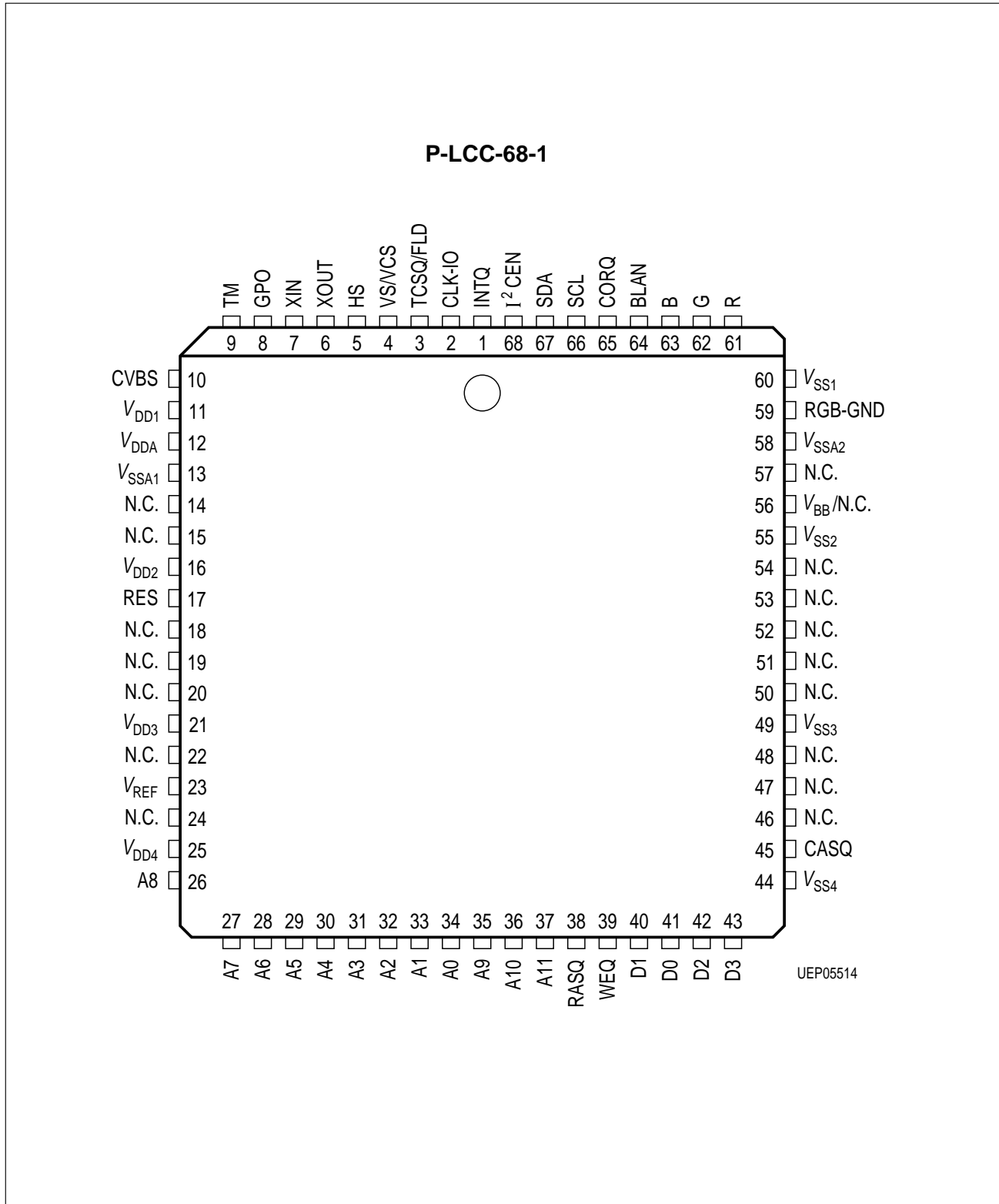
## 1.1 Pin Definitions and Functions (cont'd)

Pin No. P-SDIP-52-1	Symbol	Function
33	D0	External DRAM-data
34	D2	External DRAM-data
35	D3	External DRAM-data
36	$V_{SS4}$	0 V digital supply
37	CASQ	Column address strobe
38	$V_{SS3}$	0 V digital supply
39	$V_{BB}$	Substrate bias voltage N.C. <sup>1)</sup>
40	$V_{SS2}$	0 V digital supply
41	$V_{SSA2}$	Analog ground
42	RGB-GND	RGB-ground
43	$V_{SS1}$	0 V digital supply
44	R	Analog red display output
45	G	Analog green display output
46	B	Analog blue display output
47	BLAN	Blanking signal open drain output
48	CORQ	Contrast reduction open drain output
49	SCL	Bidirectional I <sup>2</sup> C Bus clock port
50	SDA	Bidirectional I <sup>2</sup> C Bus data port
51	I <sup>2</sup> CEN	I <sup>2</sup> C Bus enable
52	INTQ	Interrupt request output to ext. controller

<sup>1)</sup> Depends on version. Please refer to the respective Delta Specification.

## Pin Configuration

(top view)





## 1.2 Pin Definitions and Functions

Pin No. P-LCC-68-1	Symbol	Function
1	INTQ	Interrupt request output to ext. controller
2	CLK-IO	System clock input/output
3	TCSQ/FLD	Composite sync output/ field output
4	VS/VCS	Vertical sync input/output
5	HS	Horizontal sync input/output
6	XOUT	20.5-MHz crystal oscillator output
7	XIN	20.5-MHz crystal oscillator input
8	GPO	General purpose output
9	TM	Testpin, leave open or connect $V_{SS}$
10	CVBS	CVBS-video signal input
11	$V_{DD1}$	+ 5 V digital supply
12	$V_{DDA}$	+ 5 V analog supply
13	$V_{SSA1}$	Analog ground
14	N.C.	Not connected
15	N.C.	Not connected
16	$V_{DD2}$	+ 5 V digital supply
17	RES	Chip reset
18	N.C.	Not connected
19	N.C.	Not connected
20	N.C.	Not connected
21	$V_{DD3}$	+ 5 V digital supply
22	N.C.	Not connected
23	$V_{REF}$	+ 3 V reference voltage input
24	N.C.	Not connected
25	$V_{DD4}$	+ 5 V digital supply
26	A8	External DRAM-address
27	A7	External DRAM-address
28	A6	External DRAM-address
29	A5	External DRAM-address
30	A4	External DRAM-address
31	A3	External DRAM-address
32	A2	External DRAM-address

## 1.2 Pin Definitions and Functions (cont'd)

Pin No. P-LCC-68-1	Symbol	Function
33	A1	External DRAM-address
34	A0	External DRAM-address
35	A9	External DRAM-address
36	A10	External DRAM-address
37	A11	External DRAM-address
38	RASQ	Row address strobe (DRAM)
39	WEQ	Write enable (DRAM)
40	D1	External DRAM-data
41	D0	External DRAM-data
42	D2	External DRAM-data
43	D3	External DRAM-data
44	$V_{SS4}$	0 V digital supply
45	CASQ	Column address strobe
46	N.C.	Not connected
47	N.C.	Not connected
48	N.C.	Not connected
49	$V_{SS3}$	0 V digital supply
50	N.C.	Not connected
51	N.C.	Not connected
52	N.C.	Not connected
53	N.C.	Not connected
54	N.C.	Not connected
55	$V_{SS2}$	0 V digital supply
56	$V_{BB}$	Substrate bias voltage N.C. <sup>1)</sup>
57	N.C.	Not connected
58	$V_{SSA2}$	Analog ground
59	RGB-GND	RGB-ground
60	$V_{SS1}$	0 V digital supply
61	R	Analog red display output
62	G	Analog green display output
63	B	Analog blue display output

<sup>1)</sup> Depends on version. Please refer to the respective Delta Specification.

**1.2 Pin Definitions and Functions (cont'd)**

<b>Pin No.</b> <b>P-LCC-68-1</b>	<b>Symbol</b>	<b>Function</b>
64	BLAN	Blanking signal open drain output
65	CORQ	Contrast reduction open drain output
66	SCL	Bidirectional I <sup>2</sup> C Bus clock port
67	SDA	Bidirectional I <sup>2</sup> C Bus data port
68	I <sup>2</sup> CEN	I <sup>2</sup> C Bus enable

## 2 Electrical Characteristics

### Absolute Maximum Ratings

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply voltage	$V_{DD}$	0		6.0	V	
Ambient temperature	$T_A$	0		70	°C	
Storage temperature	$T_{stg}$	-20		125	°C	
Power consumption	$P_{tot}$			1.8	W	
Electrostatic discharge			2000		V	100 pF, 1 kΩ HBM according to MIL-standard 883 method 3015.7

### Characteristics

$T_A = 0$  to  $70$  °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

### Supply Voltages

	$V_{DDD}$	4.7	5.0	5.3	V	
	$V_{DDA}$	4.7	5.0	5.3	V	$V_{DDD} = V_{DDA}!$

### Supply Currents

	$I_{DDD}$			200	mA	20 pF load per pin
	$I_{DDA}$			60	mA	

### Inputs

Tristate of Outputs: I<sup>2</sup>CEN, HS, VS, GPO, RES, D0-D3

H-input voltage	$V_{IH}$	2.0		$V_{DDD}$	V	
L-input voltage	$V_{IL}$	-1.0		0.8	V	
Input capacitance	$C_I$			7	pF	
Input leakage current	$I_L$			10	μA	$V_{IH} = 5.5$ V
Input current RES	$I_{IH}$			100	μA	$V_{IH} = 5.5$ V

## Characteristics (cont'd)

$T_A = 0$  to  $70$  °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

## Outputs

### TTL-Outputs: A0-A11, D0-D3, RASQ, CASQ, WEQ, HS, VS, GPO, INTQ, TCSQ

H-output voltage	$V_{OH}$	2.4		$V_{DD}$	V	$-I_{OH} = 0.2$ mA
L-output voltage	$V_{OL}$	0		0.4	V	$I_{OL} = 1.6$ mA
Load capacitance	$C_L$			50	pF	
Transition period	$t_r, t_f$			15	ns	

### Open Drain Outputs: BLAN, CORQ

Sink current	$I_{OL}$			5	mA	low level output
L-output voltage	$V_{OL}$			0.4	V	$I_{OL} = 2$ mA
H-output voltage	$V_{OH}$			$V_{DD}$	V	
BLAN = 1: display MEGATEXT RGB-outputs BLAN = 0; display other source CORQ = 1; switch contrast reduction OFF CORQ = 0; switch contrast reduction ON						

### Sourcefollower Output: CVBS at pin TCSQ

DC-offset to CVBS-input			1.2		V	
Gain	$G$		0.9			
Output current	$I_O$	0.9			mA	CVBS = 1 V, TCSQ = 0 V
Output impedance	$R_O$		200		$\Omega$	CVBS = 1 V
Edge response	$t_r$			1	$\mu$ s	10 to 90 %, 1 Vpp, $C_L = 50$ pF

### Sync Timing: HS, VS, TCSQ

#### Sync Output Waveforms

Pulse width HS	$t_{WH}$		2		$\mu$ s	
Pulse width VS	$t_{WH}$		1		line	
VCS-waveform						see diagram 6a, b
TCSQ-waveform						see diagram 6a, b

## Characteristics (cont'd)

$T_A = 0$  to  $70$  °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

### Output Timing: HS, VS, TCSQ

Hold and delay time with respect to 24-MHz system clock output:

Delay time	$t_{OD}$			20	ns	see diagram 2
Hold time	$t_{OH}$	0			ns	see diagram 2

Hold and delay time with respect to 24-MHz external system clock input:

Delay time						not specified
Hold time						not specified

### Input Timing: HS, VS

No synchronous input mode specified!

### Clock Input/Output (see diagram 1)

#### Clock Input

H-input voltage	$V_{IH}$	2.0		$V_{DDD}$	V	
L-input voltage	$V_{IL}$	- 1.0		0.8	V	
Input capacitance	$C_I$			7	pF	
Input leakage current	$I_I$			10	$\mu$ A	$V_{IH} = 5.5$ V
Period	$T_c$	40				24-MHz clock
	$T_c$	35				27-MHz clock
Transition time	$t_{CR}, t_{CL}$			3	ns	
Symmetry ratio	$t_{CH}/t_C$	0.43		0.57		

#### Clock Output

H-output voltage	$V_{OH}$	2.4		$V_{DDD}$	V	$-I_{OH} = 0.2$ mA
L-output voltage	$V_{OL}$	0		0.4	V	$I_{OL} = 1.6$ mA
Load capacitance	$C_L$			50	pF	
Period	$T_c$		41.7		ns	20.5-MHz crystal
Transition time	$t_{CR}, t_{CF}$			5	ns	
Symmetry ratio	$t_{CH}/t_C$	0.3		0.5	ns	

## Characteristics (cont'd)

$T_A = 0$  to  $70$  °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

## RGB-Outputs

						$V_{REF} = 3$ V no resistive load RGB-GND = 0 V
Pin capacitance	$C_P$			7	V	
Output voltage range		0		2.2	V	
RGB-amplitude		1.1	1.25	1.55	V	R83: RGB-GAIN (4:0) = $1F_H$
DC-offset voltage		0.7	0.8	1.0	V	R83: RGB-LEVL (2:0) = 7
Clamp level			0		V	
DAC-resolution			4		bit	
Diff. non-linearity		- 0.5		0.5	LSB	R83: RGB-GAIN (4:0) = $1F_H$ RGB-LEVL (2:0) = 0
Int. non-linearity		- 0.5		0.5	LSB	
Output tracking		- 0.5		0.5	LSB	
Output resistance	$R_O$		270		$\Omega$	
3-dB bandwidth	$\frac{1}{2\pi R_O C_L}$		10		MHz	$C_L = 50$ pF

## Bus Connection: SDA, SCL, I<sup>2</sup>CEN (see diagram 4)

### Inputs: SDA, SCL

H-input voltage	$V_{IH}$	3.0		$V_{DD}$	V	
L-input voltage	$V_{IL}$	- 1.0		1.5	V	
Input capacitance	$C_I$			7	pF	
Input leakage current	$I_L$			10	$\mu$ A	$V_{IH} = 5.5$ V $V_{DD} = 0$ V ... 5.5 V

For modes with external clock MEGATEXT may only be operated in freerun mode as sync master. HS may not be used as an input in these cases.

The RGB-output voltage is proportional to  $V_{REF}$ .

## Characteristics (cont'd)

$T_A = 0$  to  $70$  °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

### Open Drain Outputs: SDA, SCL

L-output voltage	$V_{OL}$	0		0.4	V	$I_{OL} = 3$ mA
Sink current	$I_{OL}$			10	mA	

### I<sup>2</sup>C-Mode Timing

MEGATEXT is an I<sup>2</sup>C-slave transmitter/receiver.  
The Siemens I<sup>2</sup>C Bus specification applies.

SCL-frequency	$f_{SCL}$	0		100	kHz	I <sup>2</sup> CEN = high
Transition time	$t_r, t_f$			2	μs	
Bus capacitance	$C_{BUS}$			400	pF	
Bus free before start	$t_{BUF}$	4.7			μs	
Hold time start	$t_{HSTA}$	4.0			μs	
L-time clock	$t_{LOW}$	4.0			μs	
H-time clock	$t_{HIGH}$	4.0			μs	
Set-up time start	$t_{SUSTA}$	4.0			μs	
Hold time SDA	$t_{HDDAT}$	0			μs	
Set-up time SDA	$t_{SUDAT}$	250			ns	
Set-up time SDA at stop	$t_{SUSTO}$	4.0			μs	
Output fall time	$t_{FO}$			0.2	μs	3 V to 1 V

### M3L-Mode Timing

The MEGATEXT M3L-Bus is specified in accordance with the standard USART-interface of micro controller SDA 30C162.

SCL-frequency	$f_{SCL}$	0		1.0	MHz	20.48-MHz crystal
L-time clock	$t_L$	400			ns	
H-time clock	$t_H$	400			ns	
SCL-load capacitance	$C_{SCL}$			200	pF	
Set-up time SDA-input to SCL-falling edge	$t_{DSL}$	100			ns	
Hold time SDA-input from SCL-falling edge	$t_{DHH}$	400			ns	



## Characteristics (cont'd)

$T_A = 0$  to  $70$  °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

### M3L-Mode Timing (cont'd)

Set-up time SDA to I <sup>2</sup> CEN-rising edge	$t_{IM}$	400			ns	
Set up time I <sup>2</sup> CEN to SDA-falling edge	$t_{IS}$	400			ns	
I <sup>2</sup> CEN-high time	$t_{IH}$	1000			ns	
Delay from SCL-falling edge until SDA-open drain output stage changes impedance	$t_{DO}$	400		600	ns	
L-SDA level output impedance			100		Ω	

The resulting delay of SDA-output data is the sum of the open drain stage plus the time determined by the bus capacitance and the external pullup resistor or the impedance of the internal open drain pulldown transistor respectively.

Wait condition						I <sup>2</sup> CEN = 0
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To force the M3L-master to interrupt the transmission sequence until MEGATEXT is ready for more data, MEGATEXT can force down SCL after the transmission of a complete byte. At that time the bus master has to switch its SCL-output to high impedance and check the state of SCL afterwards. During SCL check I<sup>2</sup>CEN has to be low.

Delay from SCL-rising edge to SCL forced low for WAIT-condition	$t_{DWAIT}$	500		750	ns	
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An internal pullup transistor restores SCL high level at the end of the WAIT-condition.

SCL-pullup time at the end of WAIT	$t_{RWAIT}$	70		100	ns	
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### Reference Voltage: $V_{REF}$

Voltage level	$V_{REF}$	2.8	3.0	3.5	V	
Input leakage current	$I_I$	- 10		10	μA	$V_{REF} = 3$ V

$V_{REF}$  influences the DAC-range, the CVBS-output at pin TCSQ and the CVBS-ADC range.

## Characteristics (cont'd)

$T_A = 0$  to  $70$  °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

### CVBS-Input and ADC ( $V_{REF} = 3$ V)

Input leakage current	$I_I$	- 1.0		1.0	$\mu$ A	CVBS = 2 V
Input capacitance	$C_P$			45	pF	
Ext. coupling capacitance	$C_{CPL}$		100		nF	
Sensitivity of clamp level to current leakage/injection		- 15		15	mV/ $\mu$ A	$I_I = 2$ $\mu$ A $C_{CPL} = 100$ nF
ADC-range		1.7		2.0	V	$V_{REF} = 3$ V
CVBS-sync amplitude		0.1			V	

### Crystal Oscillator: XIN, XOUT

Bias resistance between XIN, XOUT	$R_{Xbias}$	60	120	180	k $\Omega$	
Small signal voltage gain	$G_V$	8	13			100 kHz, 50 mVpp
Feedback capacitance	$C_{FB}$			4.0	pF	
Pin capacitance	$C_P$			7.0	pF	

### Crystal

Nominal frequency	$f_O$		20.48		MHz	
Effect of temperature and accuracy of adjustment	$df/f_O$	- 5 %		+ 5 %		
Temperature range	$T_A$	0		70	°C	
Resonant impedance	$Z_R$			40	$\Omega$	
Equivalent parallel C	$C_L$		15		pF	
Crystal load				0.1	mW	
Ext. capacitors	$C_{1,2}$		15		pF	

The center frequency of the MEGATEXT horizontal PLL is proportional to the crystal frequency. In PAL-mode the centre frequency is 15.625 kHz for the typical crystal frequency of 20.48 MHz. Deviations from the typical crystal frequency will shift the range of the horizontal frequencies where the PLL is able to lock.

## Characteristics (cont'd)

$T_A = 0$  to  $70$  °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

### DRAM-Interface (see diagram 5)

The external DRAM is operated in page mode.

The timing of the DRAM-interface signals are specified below.

Cycle time	$t_{WC}$	420	500	550	ns	
Address hold time from RAS	$t_{RAH}$	25			ns	
Address hold time from CAS	$t_{CAH}$	60			ns	
Address set-up time from RAS	$t_{ASR}$	5			ns	
Address set-up time from CAS	$t_{ASC}$	5			ns	
L-time RAS	$t_{RASP}$	280			ns	
L-time CAS	$t_{CASL}$	70			ns	
H-time RAS	$t_{RP}$	140			ns	
H-time CAS	$t_{CP}$	70			ns	
Refresh period		20			ms	

### Write Cycle

L-time WE	$t_{WEL}$	210			ns	
Data set-up time to CAS	$t_{DS}$	100			ns	
WE set-up time to CAS	$t_{RCS}$	0			ns	
Data hold time from CAS	$t_{DH}$	55			ns	
Data hold time from WE	$t_{OHZ}$			10	ns	

### Read Cycle

H-time WE (output enable)	$t_{OEL}$	210			ns	
Access time from CAS	$t_{CAC}$			60	ns	
Data hold time of DRAM	$t_{OFF}$	40			ns	

## Characteristics (cont'd)

$T_A = 0$  to  $70$  °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

### Reset/Chip Initialization

A power-on reset or a reset pulse at pin RES lead to a hardware reset and a software initialization of registers and internal DRAM. During initialization bus transfers are not allowed.

At / after power-on a reset pulse at pin RES is necessary. RES may return to 0 after the supply voltage reached its lower limit for chip function (4.7 V). This may be achieved by a capacitor  $C$  between RES and  $V_{DD}$  and by a resistor  $R$  between RES and  $V_{SS}$ . The dimensions of  $R$  and  $C$  depend on the worst case rise time of  $V_{DD}$ .

Initialization time after power-on or falling edge of RES	$t_{INIT}$			25	ms	$V_{DD}$ greater 4.7 V
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If the supply voltage drops below  $V_{DD\ min}$ , the IC has to be reset by pin RES.

Pulse width RES		100			ns	
-----------------	--	-----	--	--	----	--

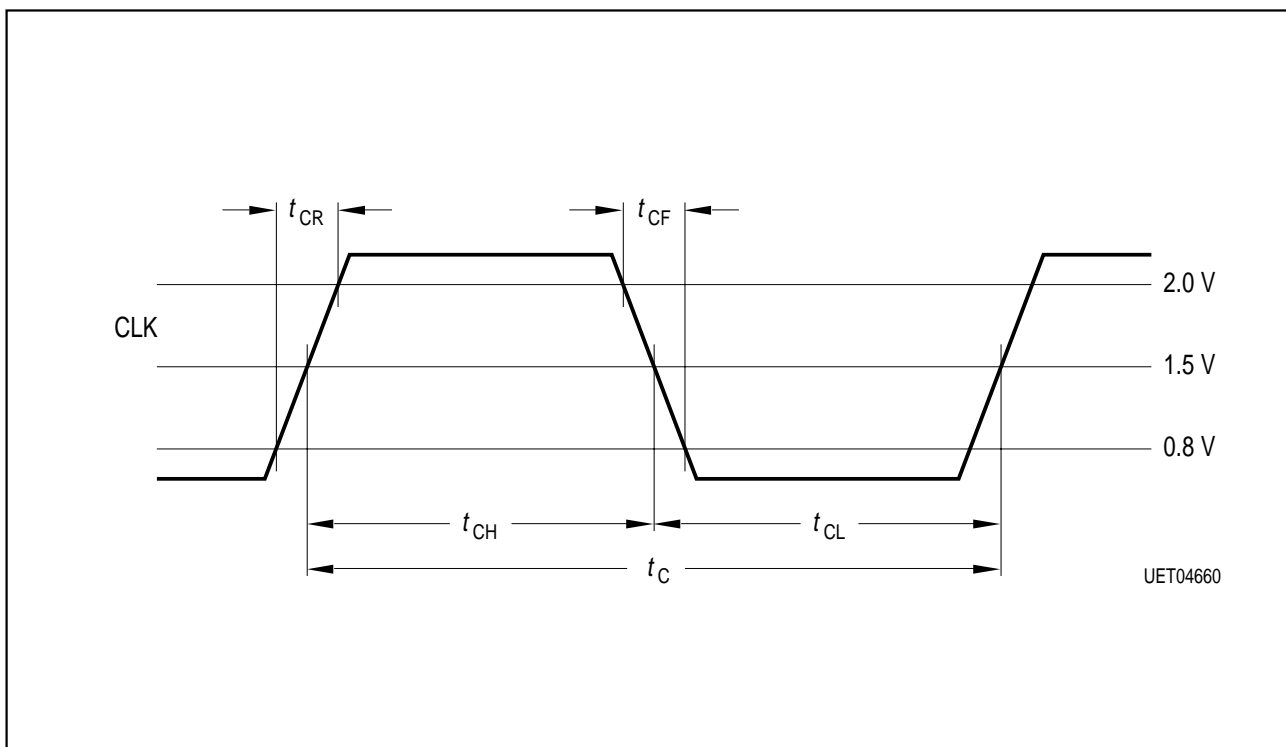
High level at pin RES causes chip reset.

In rare cases, the IC may remain in a permanent reset state after power up, depending on the applicational context. After power up, the software should check proper operation. In case the Megatext does not react properly, power supply should be switched off for at least 3 s. After that, power supply can be switched on again.

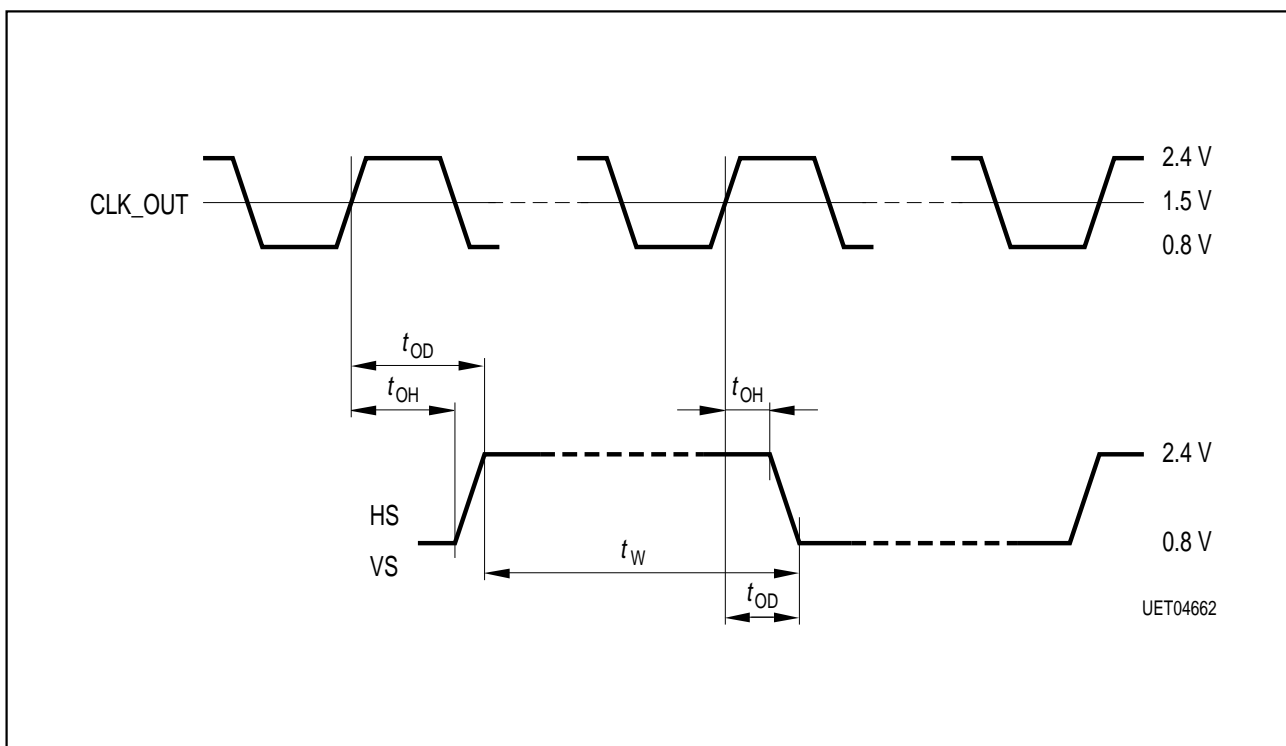
### Other Items

Horizontal frequency pull-in range of CVBS-PLL:		15	15.625	16.2	kHz	PAL 20.48 MHz crystal
		15.2	15.748	16.3	kHz	NTSC 20.48 MHz crystal
Horizontal frequency pull-in range of display-PLL:		15	15.625	16.2	kHz	20.48 MHz crystal

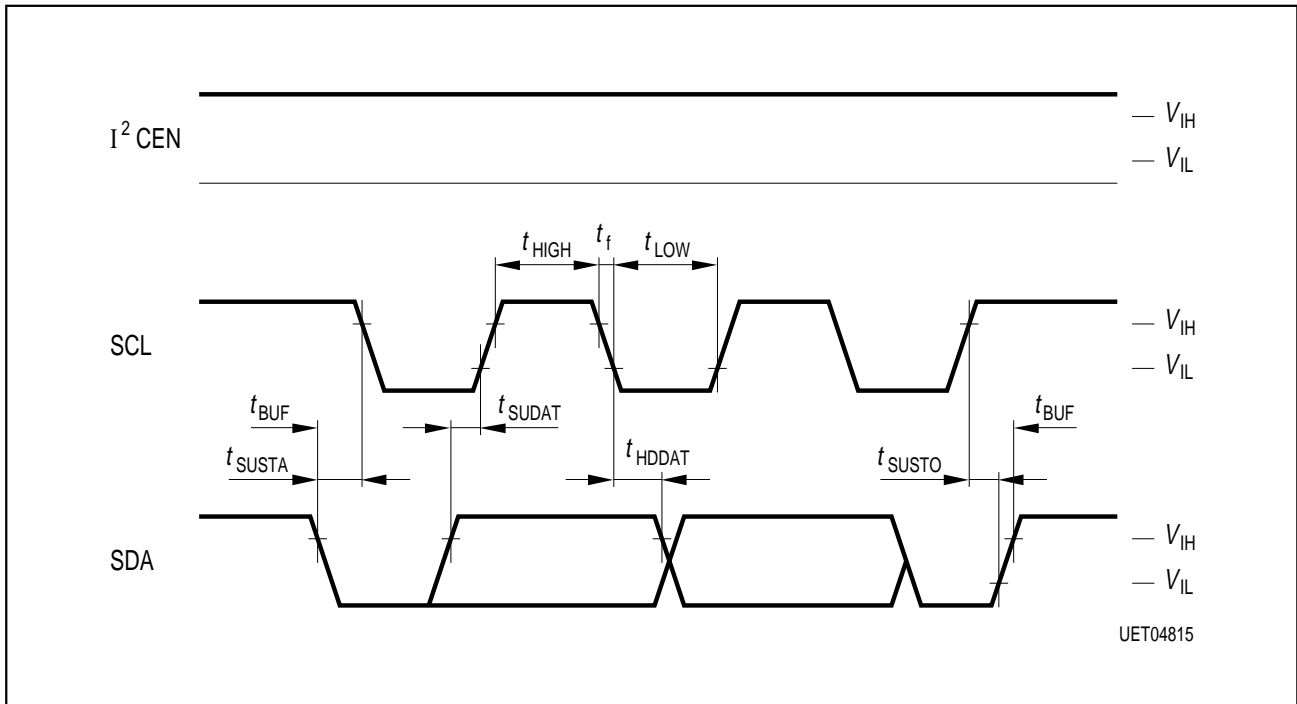
3 Diagrams



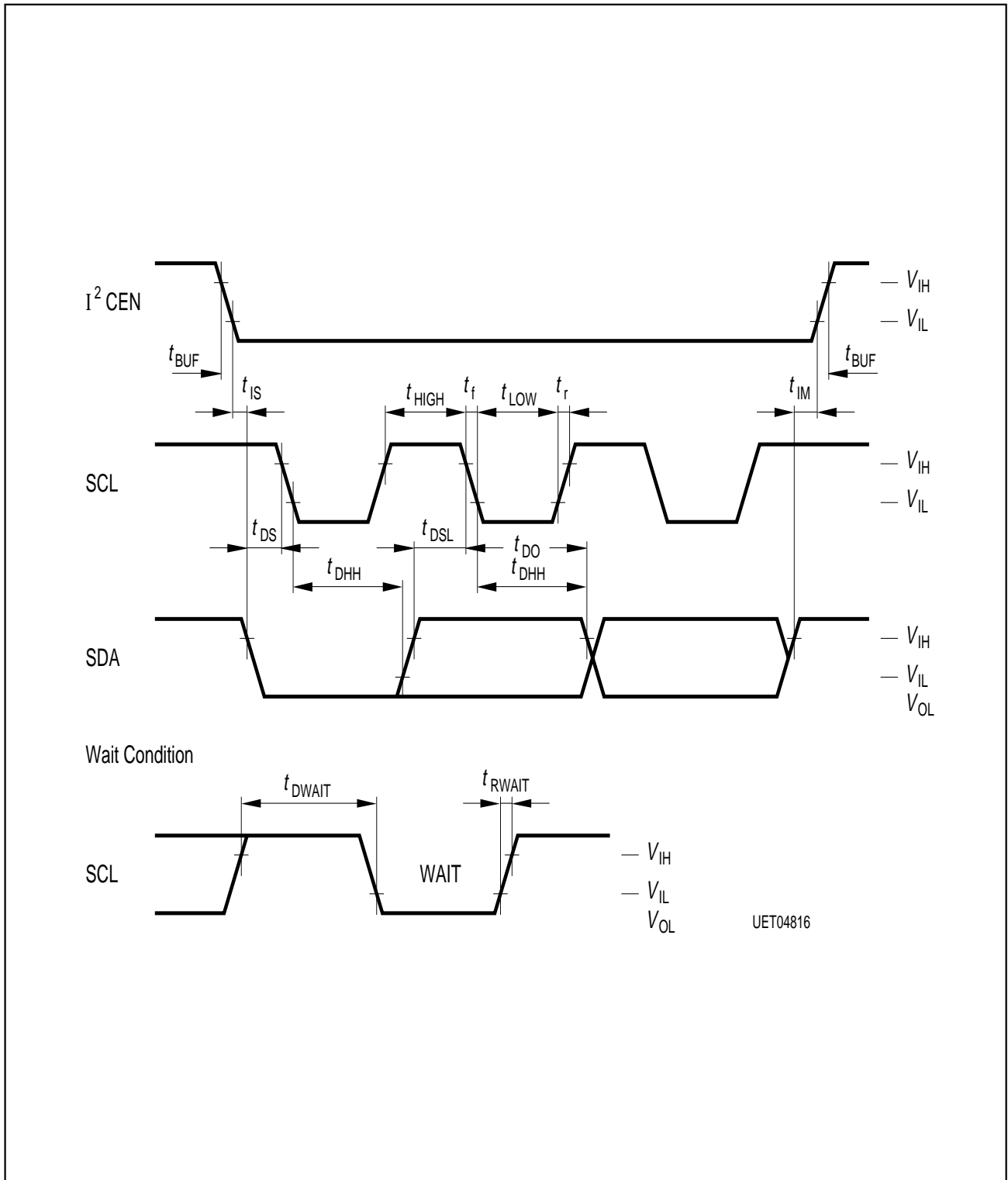
Timing Diagram 1



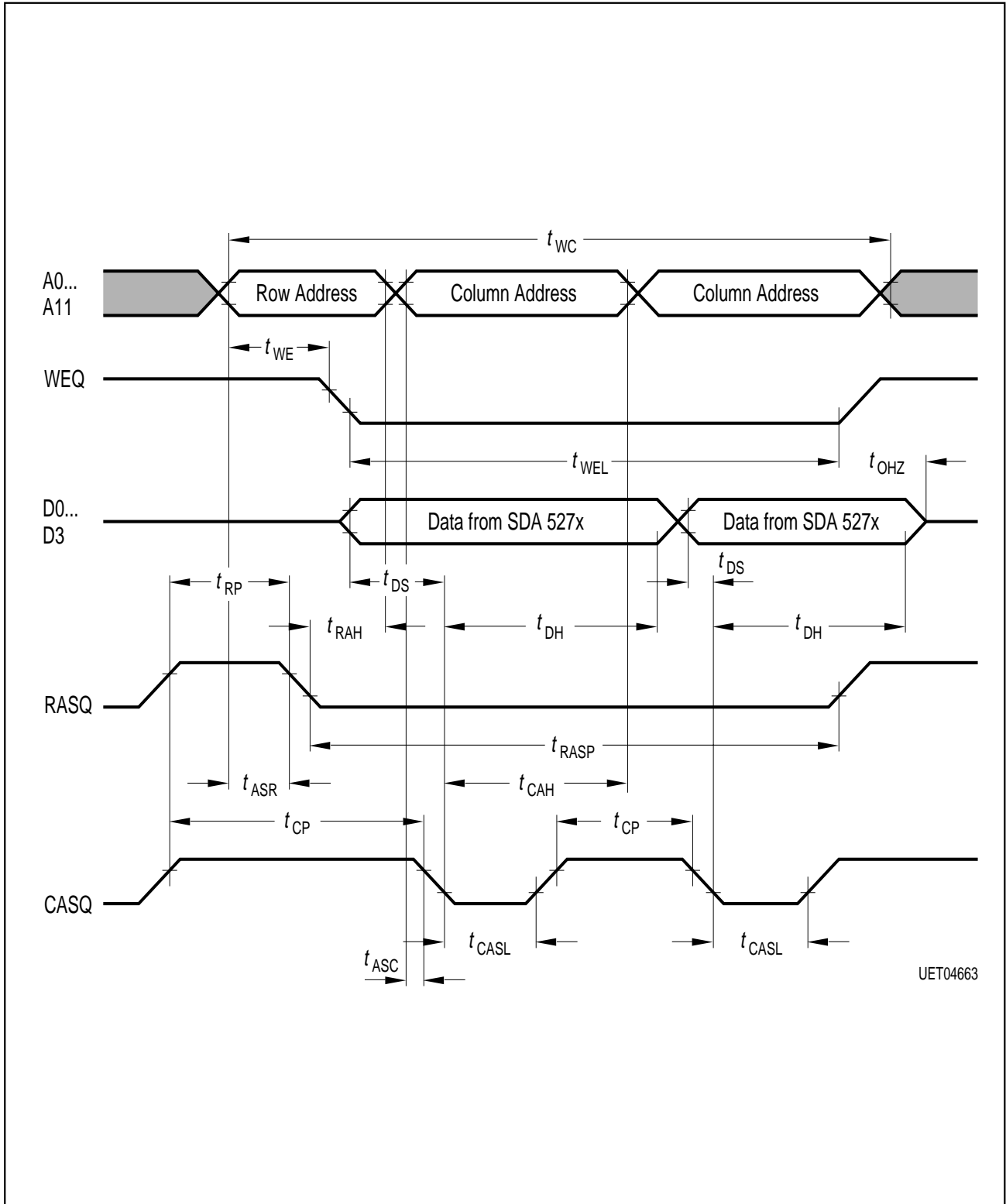
Timing Diagram 2



**Timing Diagram 3a**  
**I<sup>2</sup>C-Bus Mode**

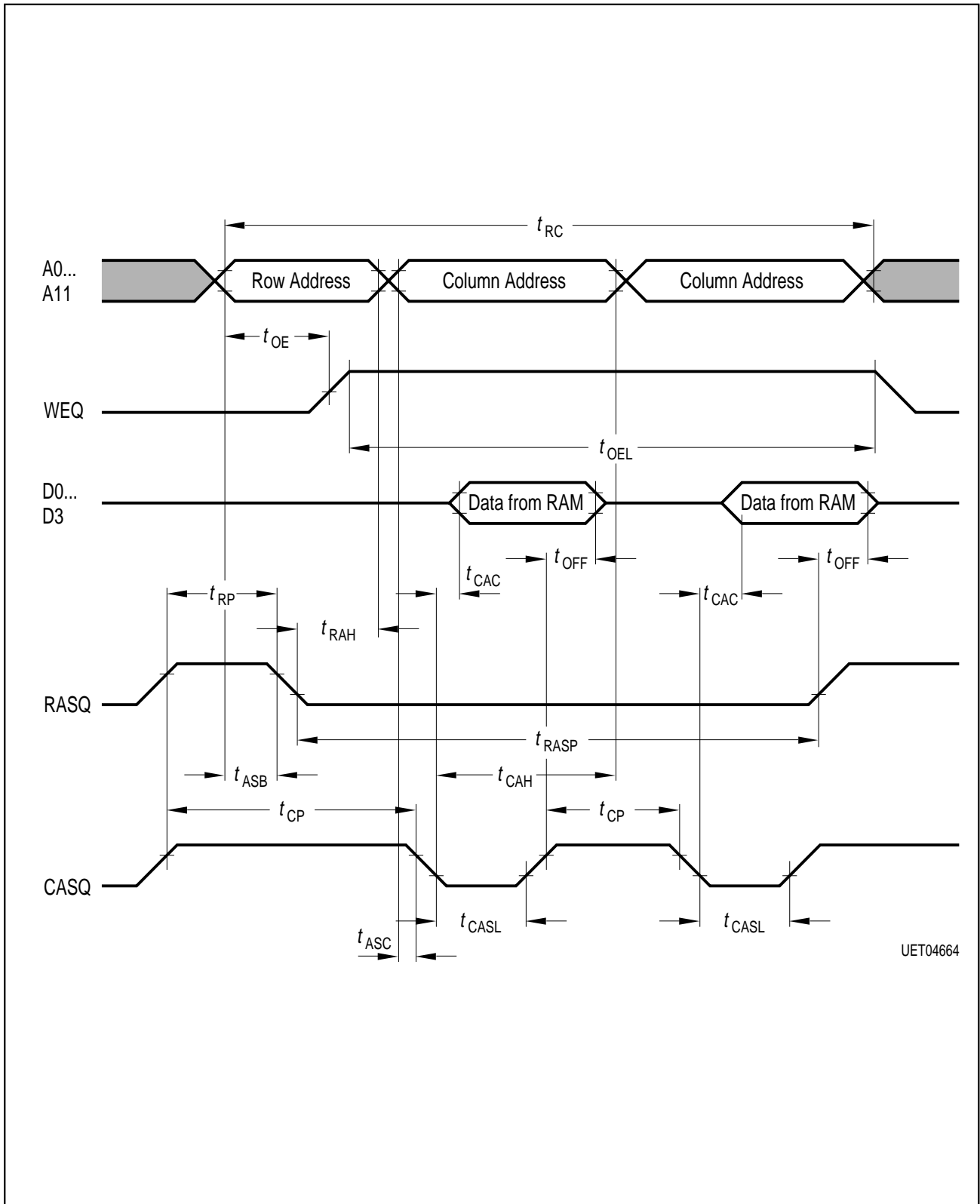


Timing Diagram 3b  
M3L-Bus Mode

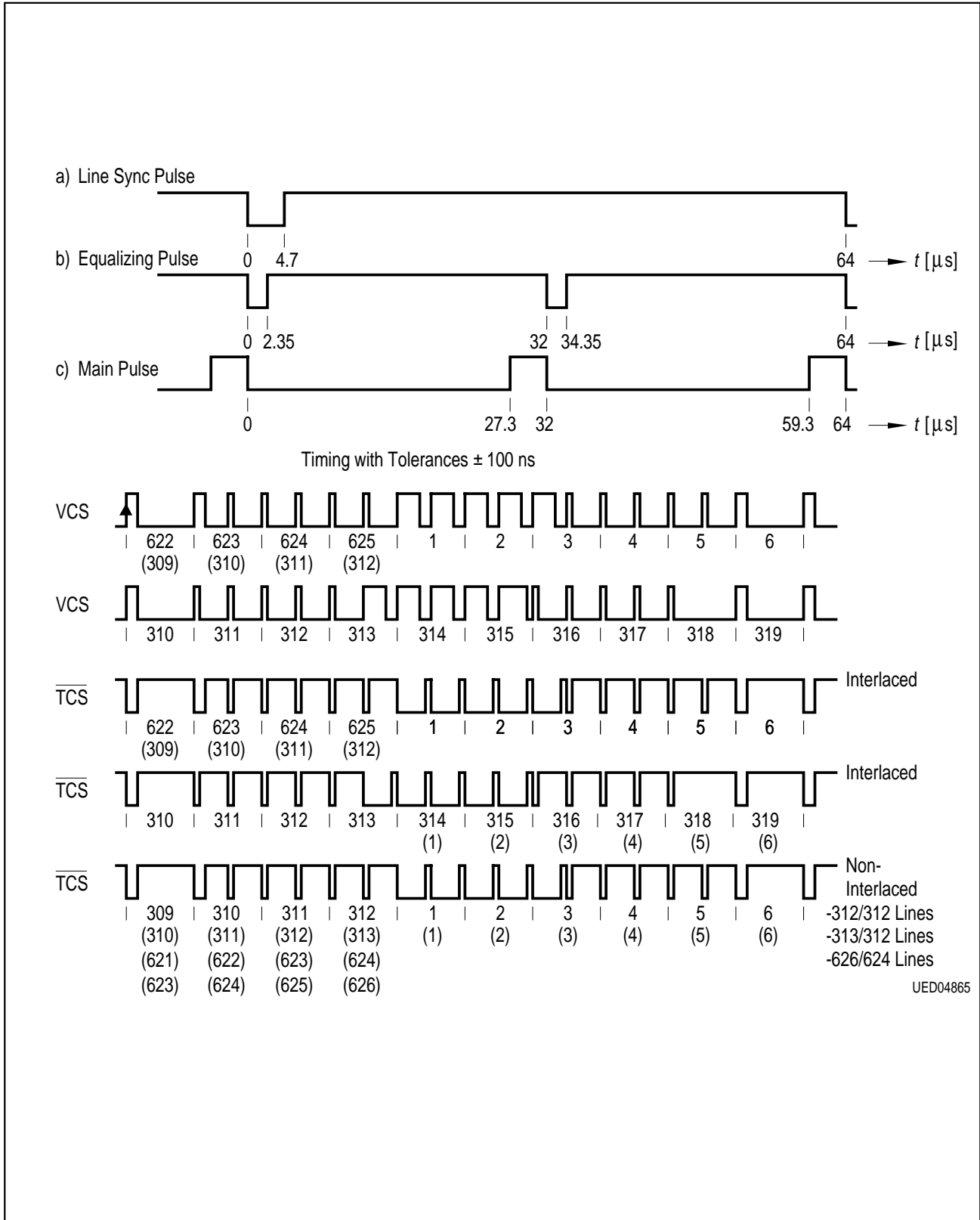


Timing Diagram 4a  
DRAM-Page Mode Write Cycle

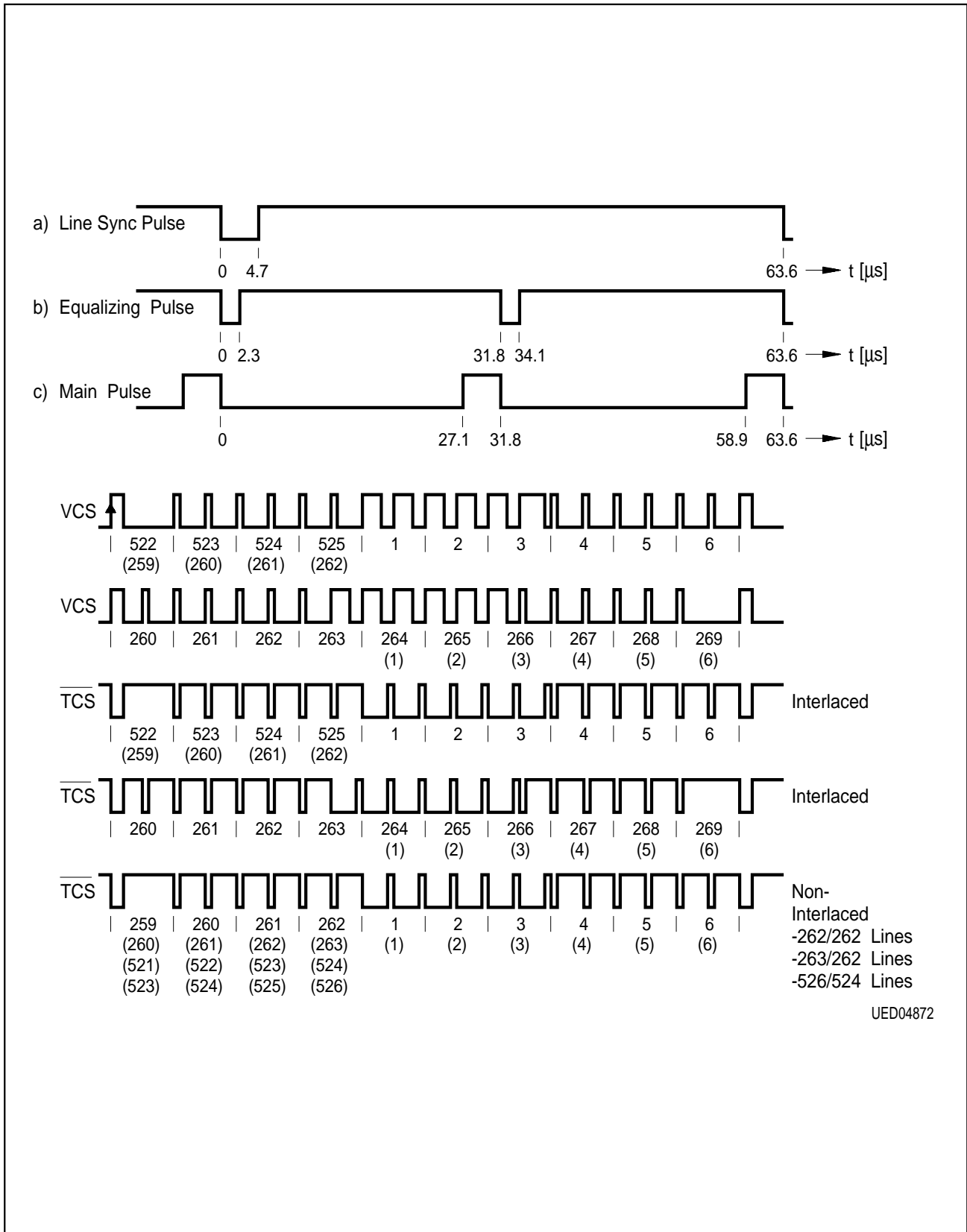




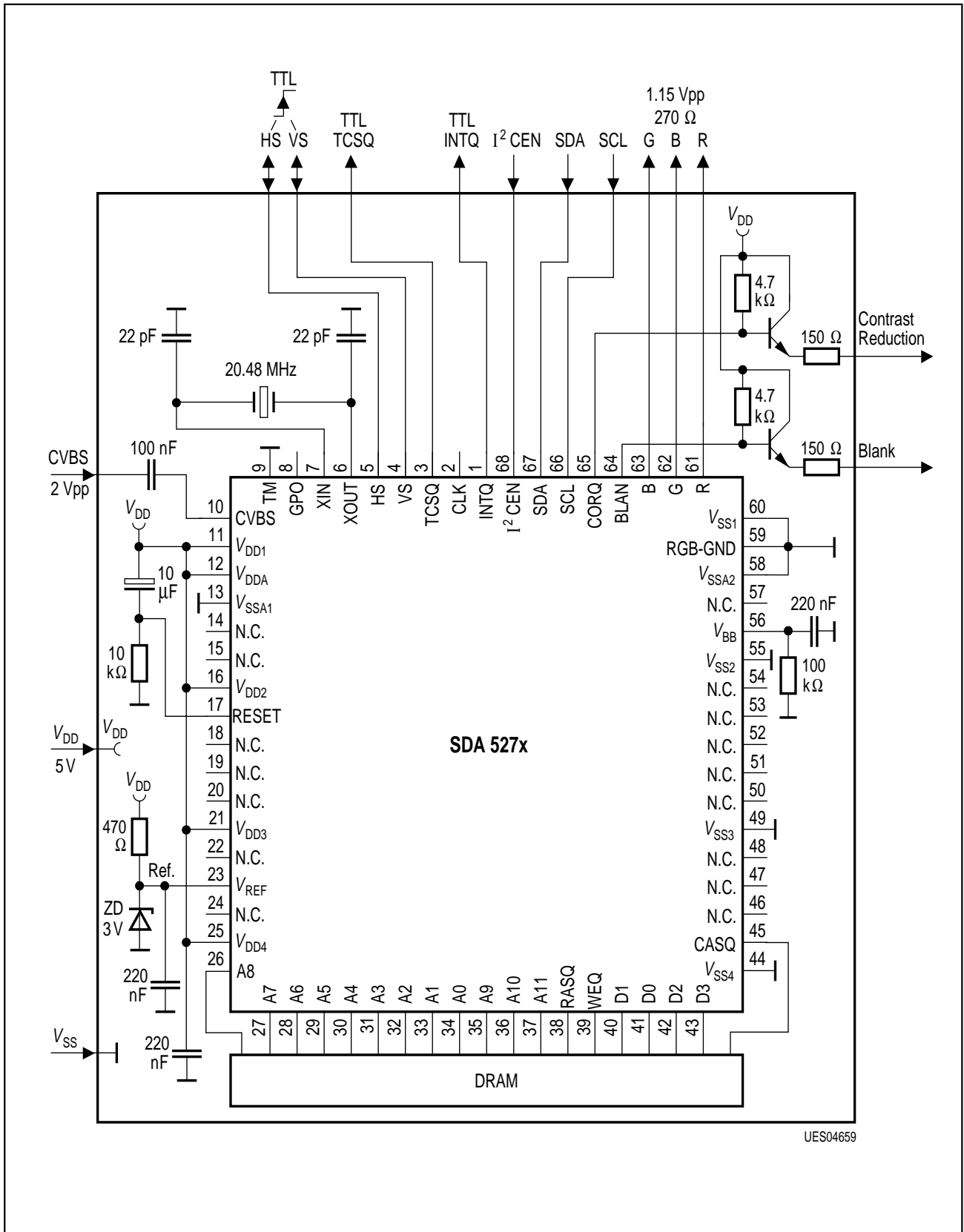
Timing Diagram 4b  
DRAM-Page Mode Read Cycle



Timing Diagram 5a  
VCS and TCS in PAL Freerun Mode



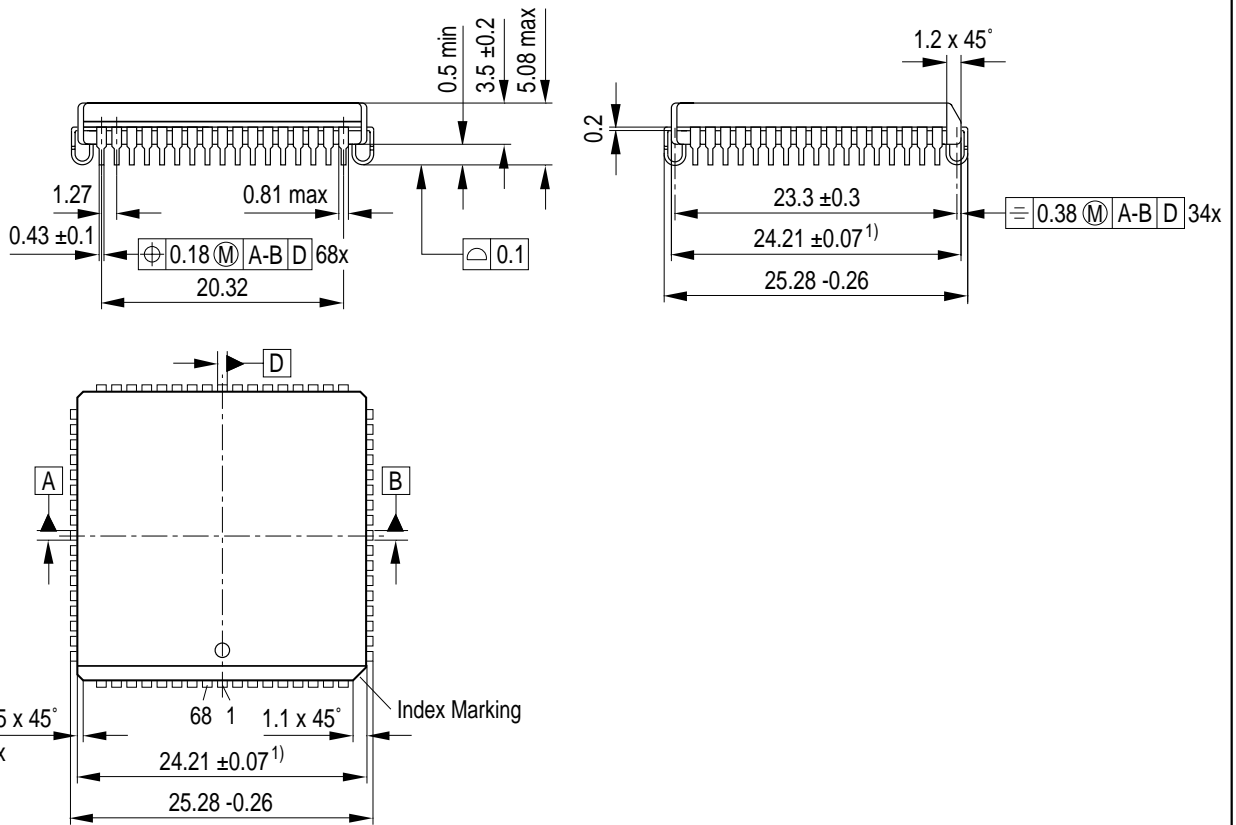
**Timing Diagram 5b**  
**VCS and TCS in NTSC Freerun Mode**



**Application Circuit**

4 Package Outlines

**P-LCC-68-1 (SMD)**  
(Plastic Leaded Chip Carrier)



1) Does not include plastic or metal protrusions of 0.15 max per side

GPL05099

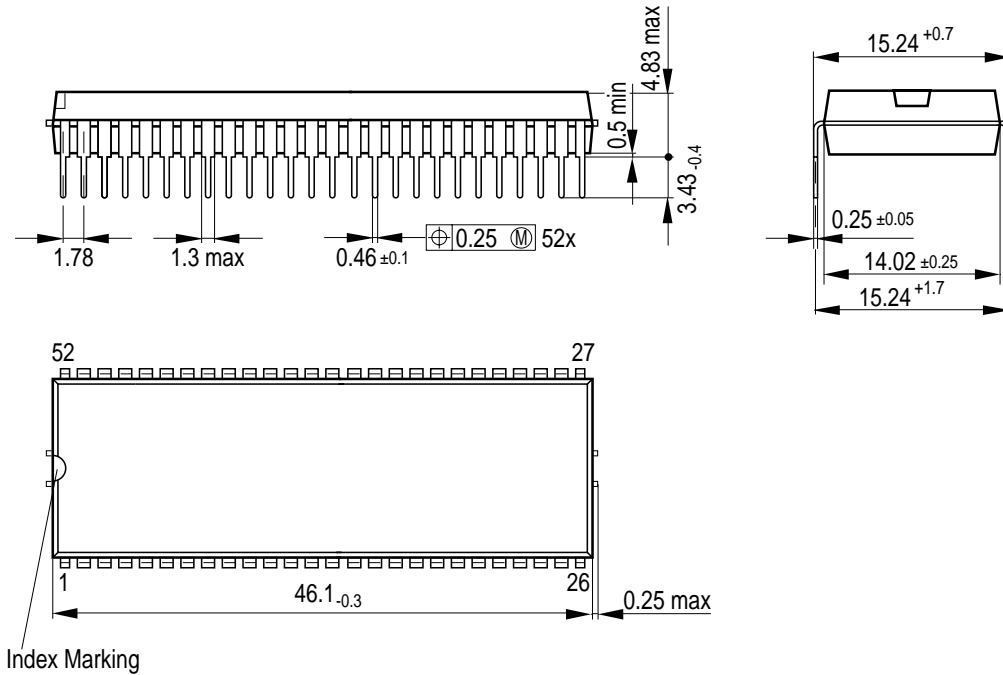
**Sorts of Packing**

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm

**Plastic Package, P-SDIP-52-1**  
 (Plastic Dual In-Line Package)



GPD05262

**Sorts of Packing**

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm