J3
Spikeputor Data Bus Write
IN15 2 1 IN0
IN14 4 3 IN1
IN13 6 5 IN2
IN12 8 7 IN3
IN11 10 9 IN4
IN10 12 11 IN5
IN9 14 13 IN6
IN8 16 15 IN7

J2
Spikeputor Address Bus
O_ADDR15 2 1
O_ADDR14 4 3 O_ADDR1
O_ADDR13 6 5 O_ADDR2
O_ADDR12 8 7 O_ADDR3
O_ADDR11 10 9 O_ADDR4
O_ADDR10 12 11 O_ADDR5
O_ADDR9 14 13 O_ADDR6
O_ADDR8 16 15 O_ADDR7

J4
Spikeputor Data Bus Read
RDATA15 2 1 RDATA0
RDATA14 4 3 RDATA1
RDATA13 6 5 RDATA2
RDATA12 8 7 RDATA3
RDATA11 10 9 RDATA4
RDATA10 12 11 RDATA5
RDATA9 14 13 RDATA6
RDATA8 16 15 RDATA7

Clear command on DEV_RESET or INIT
Latch in command after 8 pulses or after DEV_RESET

U1
74LS595
COPI 14 SER
RSCK 11 SRCLK
INIT 10 SRCLR
CMD_LATCH 12 RCLK
13 OE
VCC 16 +5V
GND 8 GND
QA 15
QB 1
QC 2
QD 3
QE 4 CMD0
QF 5 CMD1
QG 6 CMD2
QH 7 CMD3
QH' 9

CMD_LATCH
TP10

U21A
74LS08
3
1 PULSE8
2 INIT

Latch in address/data on each RSCK rising edge

U4
74LS595
COPI 14 SER
RSCK 11 SRCLK
INIT 10 SRCLR
CS 12 RCLK
BUS_ENABLE 13 OE
VCC 16 +5V
GND 8 GND
QA 15 IN0
QB 1 IN1
QC 2 IN2
QD 3 IN3
QE 4 IN4
QF 5 IN5
QG 6 IN6
QH 7 IN7
QH' 9

U5
74LS595
RSCK 11 SRCLK
INIT 10 SRCLR
CS 12 RCLK
BUS_ENABLE 13 OE
VCC 16 +5V
GND 8 GND
QA 15 IN8
QB 1 IN9
QC 2 IN10
QD 3 IN11
QE 4 IN12
QF 5 IN13
QG 6 IN14
QH 7 IN15
QH' 9

U22
74LS574
ADDR15 2 D0
ADDR14 3 D1
ADDR13 4 D2
ADDR12 5 D3
ADDR11 6 D4
ADDR10 7 D5
ADDR9 8 D6
ADDR8 9 D7
CS 11 Cp
BUS_ENABLE 1 OE
VCC 20 +5V
GND 10 GND
Q0 19 O_ADDR15
Q1 18 O_ADDR14
Q2 17 O_ADDR13
Q3 16 O_ADDR12
Q4 15 O_ADDR11
Q5 14 O_ADDR10
Q6 13 O_ADDR9
Q7 12 O_ADDR8

U23
74LS574
ADDR1 2 D0
ADDR2 3 D1
ADDR3 4 D2
ADDR4 5 D3
ADDR5 6 D4
ADDR6 7 D5
ADDR7 8 D6
GND 9 D7
CS 11 Cp
BUS_ENABLE 1 OE
VCC 20 +5V
GND 10 GND
Q0 19 O_ADDR1
Q1 18 O_ADDR2
Q2 17 O_ADDR3
Q3 16 O_ADDR4
Q4 15 O_ADDR5
Q5 14 O_ADDR6
Q6 13 O_ADDR7
Q7 12

U10
74LS165
GND 10 DS
RDATA0 11 D0
RDATA1 12 D1
RDATA2 13 D2
RDATA3 14 D3
RDATA4 3 D4
RDATA5 4 D5
RDATA6 5 D6
RDATA7 6 D7
INIT 1 PL
TSCK 2 CP
15 CE
VCC 16 +5V
GND 8 GND
Q7 9
Q7 7

U11
74LS165
RDATA8 10 DS
RDATA9 11 D0
RDATA10 12 D1
RDATA11 13 D2
RDATA12 14 D3
RDATA13 3 D4
RDATA14 4 D5
RDATA15 5 D6
6 D7
INIT 1 PL
TSCK 2 CP
15 CE
VCC 16 +5V
GND 8 GND
Q7 9
Q7 7

Latch in status info and data out bus at end of INIT

U2
74LS138
CMD0 1 A0
CMD1 2 A1
CMD2 3 A2
CMD3 6 E3
EXEC 5 E2
INIT 4 E1
VCC 16 +5V
GND 8 GND
O0 15 READ
O1 14 WRITE
O2 13 SETADDR
O3 12 INCADDR
O4 11 RESET
O5 10 IRQ
O6 9 RESTART
O7 7 HALT

J13
Command Outputs
0x80 1
0x90 2
0xA0 3
0xB0 4
0xC0 5
0xD0 6
0xE0 7
0xF0 8

U3
74HCT40103
P0 4
P1 5
GND 6
P2 10
P3 11
P4 12
P5 13
P6 3
P7 9
CS 9
TSCK 1
DEV_RESET 2
VCC 16 +5V
GND 8 GND
TC 14 PULSE8

TP9
PULSE8

TP1
Output Enable
BUS_ENABLE
R8
1k
GND

Set Address Output on rising edge of CS

U6
74LS193
IN1 15 P0
IN2 1 P1
IN3 10 P2
IN4 9 P3
SETADDR 11 Pl
INC 5 CpUp
DEV_RESET 14 CpDw
4 Mr
VCC 16 +5V
GND 8 GND
Q0 3 ADDR1
Q1 2 ADDR2
Q2 6 ADDR3
Q3 7 ADDR4
TcUp 12
TcDw 13

R10
4.7k
+5V

R12
4.7k
+5V

U7
74LS193
IN5 15 P0
IN6 1 P1
IN7 10 P2
IN8 9 P3
SETADDR 11 Pl
DEV_RESET 4 CpUp
5 CpDw
14 Mr
VCC 16 +5V
GND 8 GND
Q0 3 ADDR5
Q1 2 ADDR6
Q2 6 ADDR7
Q3 7 ADDR8
TcUp 12
TcDw 13

R3
4.7k
+5V

U13B
74LS123
6 Cext
7 RCext
GND 9
CS 10
A
B
Clr 12 INIT
Q 5 INIT
Q 11 DEV_RESET
VCC 16 +5V
GND 8 GND

C25
10 nF

TP3
INIT

R1
10k
+5V

Translate command to individual signals on CS negate pulse
Valid command in upper nybble and must have msb HIGH.

Count pulses and create eighth pulse signal

R2
15k
+5V

C24
10 nF

U13A
74LS123
15 RCext
14 Cext
GND 1
CS 2
A
B
Clr 4 EXEC
Q 13 EXEC
Q 3 DEV_RESET
VCC 16 +5V
GND 8 GND

TP2
EXEC

Create 40 µs INIT pulse on CS assert to clear input latches and allow bus to settle.

Create 60 µs EXEC pulse on CS negate to create the command pulses. Longer time required for Spikeputor WE signal.

Set or increment address on execution of READ or WRITE command

U8
74LS193
IN9 15 P0
IN10 1 P1
IN11 10 P2
IN12 9 P3
SETADDR 11 Pl
DEV_RESET 4 CpUp
5 CpDw
14 Mr
VCC 16 +5V
GND 8 GND
Q0 3 ADDR9
Q1 2 ADDR10
Q2 6 ADDR11
Q3 7 ADDR12
TcUp 12
TcDw 13

R9
4.7k
+5V

R11
4.7k
+5V

U9
74LS193
IN13 15 P0
IN14 1 P1
IN15 10 P2
GND 9 P3
SETADDR 11 Pl
DEV_RESET 4 CpUp
5 CpDw
14 Mr
VCC 16 +5V
GND 8 GND
Q0 3 ADDR13
Q1 2 ADDR14
Q2 6 ADDR15
Q3 7
TcUp 12
TcDw 13

D1
IOFLAG
GND
IOFLAG_OUT 2
Q4
2N7000
GND

D2
AUTO_INC
GND
AUTO_INC 2
Q1
2N7000
GND

D3
RESET
GND
RESET_OUT 2
Q2
2N7000
GND

D4
IRQ
GND
IRQ_OUT 2
Q3
2N7000
GND

RN3
470
+5V

U12
74LS165
ADDR1 11 DS
ADDR2 12 D0
CLK_IN 13 D1
ISEL_IN 14 D2
AUTO_INC_SET 3 D3
RESET_OUT 4 D4
IRQ_OUT 5 D5
IOFLAG_OUT 6 D6
D7
INIT 1 PL
TSCK 2 CP
15 CE
VCC 16 +5V
GND 8 GND
Q7 9
Q7 7 CIPO

Send status info and data out on each TSCK rising edge

U17A
74LS74
HALT 2 D
3 Pr
Q 5 HALT_REQ
6 Clr
Q
VCC 14 +5V
GND 7 GND

TP8
HALT_REQ

U17B
74LS74
D 12 ISEL_IN
Pr 13
Q 9
Clr 10
Q 8 IOFLAG_OUT
VCC 14 +5V
GND 7 GND

R5
4.7k
+5V

U21B
74LS08
RESTART 5
DEV_RESET 4
6

1. Set or clear HALT_REQ on HALT or RESTART command.
2. Wait for rising edge of Spikeputor ISEL to assert Spikeputor IOFLAG signal. Negate immediately.

J1
Spikeputor Control Signals
GND 2 1 O_IOFLAG
GND 4 3 O_WE
GND 6 5 I_CLK
GND 8 7 GND
GND 10 9 O_IRQ
GND 12 11 O_RESET
GND 14 13 I_ISEL
GND 16 15 GND

U14
74LS541
IOFLAG_OUT 2 A0
IRQ_OUT 3 A1
RESET_OUT 4 A2
I_CLK 5 A3
I_ISEL 6 A4
I_COPI 7 A5
RES 8 A6
I_SCK 9 A7
1 G1
19 G2
VCC 20 +5V
GND 10 GND
Y0 18 O_IOFLAG
Y1 17 O_IRQ
Y2 16 O_RESET
Y3 15 CLK_IN
Y4 14 ISEL_IN
Y5 13 COPI
Y6 12 DEV_RESET
Y7 11 SCK

U19C
74LS04
5
6 DEV_RESET

TP4
DEV_RESET

U18B
74LS00
READ 4
WRITE 5
6

U18C
74LS00
INCADDR 9
10
AUTO_INC 3
8
AUTO_INC_SET
2
74LS00
U18A

U18D
74LS00
12
13 AUTO_INC
11
TP11
TP7
INC

U21C
74LS08
10 SETADDR
8
9 DEV_RESET

R4
10k
+5V

U24
MC34064P
2 IN
RESET 1
GND 3 GND
RES
C27
1 uF

Jumper pins 1 and 2 for SPI Mode 0
SCK 1
TSCK 2
SCK 3
J8
TSCK Phase Select

Jumper pins 2 and 3 for SPI Mode 0
SCK 1
RSCK 2
SCK 3
J9
RSCK Phase Select

U19A
74LS04
INV1_in 1
2 INV1_out

U19B
74LS04
INV2_in 3
4 INV2_out

U19D
74LS04
INV3_in 9
8 INV3_out

U21D
74LS08
NAND_in1 13
NAND_in2 12
11 NAND_out

Create a 1.7 ms device reset pulse on power-up

1. Set or clear AUTO_INC on INCADDR or SETADDR command.
2. Assert INC signal on AUTO_INC and READ or WRITE command.

GND 16
GND 14
GND 12
GND 10
GND 8
GND 6
GND 4
GND 2
15 O_CIPO
13 I_CS0
11
9
7
5 GND
3 I_SCK
1 I_COPI
SPI Connector
J5

RN1
4.7k

U20
74LS240
WRITE 2 I0a
SCK 4 I1a
CS 6 I2a
11 I3a
13 I0b
15 I1b
17 I2b
I3b
GND 1 OEa
CS 19 OEb
VCC 20 +5V
GND 10 GND
O0a 18 O_WE
O1a 16 SCK
O2a 14 CS
O3a 12 CS
O0b 9
O1b 7
O2b 5
O3b 3 O_CIPO

TP5
IRQ_SET
IRQ
R6
4.7k
U15A
74LS74
D
Pr
Q 5 IRQ_SET
Clr
Q
GND
U15B
74LS74
D 12 ISEL_IN
Pr 11
Q 9 IRQ_OUT
Clr 10
Q 8 IRQ_OUT
DEV_RESET
U19F
74LS04
IRQ_OUT 13
12

1. Assert IRQ_SET on IRQ command pulse.
2. Wait for rising edge of Spikeputor ISEL to assert Spikeputor IRQ signal.
3. Negate IRQ_SET flag.
4. Wait for rising edge of Spikeputor ISEL to negate Spikeputor IRQ signal.

TP6
RES_SET
RESET
R7
4.7k
U16A
74LS74
D
Pr
Q 5 RES_SET
Clr
Q
GND
U16B
74LS74
D 12 CLK_IN
Pr 11
Q 9 RESET_OUT
Clr 10
Q 8 RESET_OUT
DEV_RESET
U19E
74LS04
RESET_OUT 11
10

1. Assert RES_SET on RESET command pulse.
2. Wait for rising edge of Spikeputor CLK to assert Spikeputor RESET signal.
3. Negate RES_SET flag.
4. Wait for rising edge of Spikeputor CLK to negate Spikeputor RESET signal.

J10
Spare Connector
+5V
GND

RN2
4.7k
INV1_in 5
INV2_in 4
INV3_in 3
NAND_in1 2
NAND_in2 1
+5V
Logic Gate Inputs
J11

J12
Logic Gate Outputs
4 INV3_out
3 INV2_out
2 INV1_out
1 NAND_out

J6
1
2
GND

PWR_FLAG
POWER
J7
PWR_FLAG
+5V
GND
C26
220 uF
C28
220 uF
C29
220 uF

U13C
74LS123
U15C
74LS74
U16C
74LS74
U17C
74LS74
U18E
74LS00
U19G
74LS04
U21E
74LS08
GND
VCC
+5V

C1 100 nF
C2 100 nF
C3 100 nF
C4 100 nF
C5 100 nF
C6 100 nF
C7 100 nF
C8 100 nF
C9 100 nF
C10 100 nF
C11 100 nF
C12 100 nF
C13 100 nF
C14 100 nF
C15 100 nF
C16 100 nF
C17 100 nF
C18 100 nF
C19 100 nF
C20 100 nF
C21 100 nF
C22 100 nF
C23 100 nF
C30 100 nF

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