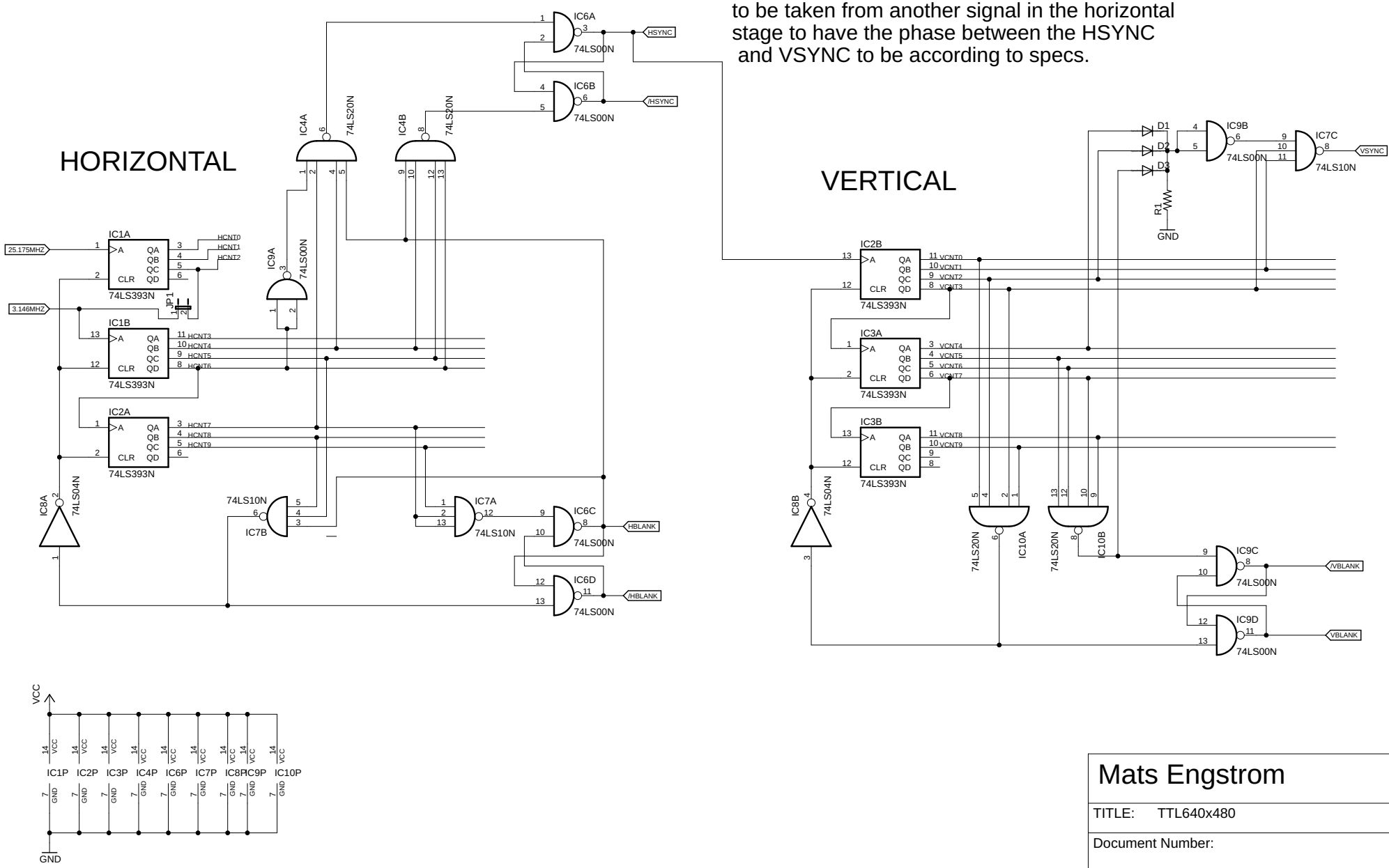
Please note:
The clock for the vertical counter might have to be taken from another signal in the horizontal stage to have the phase between the HSYNC and VSYNC to be according to specs.



Mats Engstrom	
TITLE: TTL640x480	
Document Number:	REV:
Date: 1/13/19 1:46 PM	Sheet: 1/1