SCT3258

Datasheet

Version: 2.0

Date: 2018/02/21

Change History

Version	Date	Change Descriptions
1.0	201308/05	Initial version
1.1	2013/10/23	Add DMR T2 support
1.2	2013/11/25	Update description for PLL
1.3	2013/12/16	Remove Pin HSTS
1.4	1/14/2014	Update the HPI Timing
1.5	10/27/2014	Add support for AMBE+2 Add support for TDMA direct mode，and input clock requirement for TDMA direct mode Add support the non-standard 55 Hz CTCSS tail tone Update naming conventions
1.6	01/09/2015	Add vocoder support information
1.7	02/06/2015	Update PIN definition
1.8	05/09/2016	Update vocoder definition for V and U
1.9	05/27/2016	Add support to SCT3258R model
2.0	02/22/2018	Added footnotes for supply options, contact details for CML Microcircuits Ltd.

Contents:

1 Overview

SCT3258 is a low power high performance base band processor supporting DPMR and DMR protocol. With an external codec (audio band ADC and DAC), it completes the entire physical layer and data link layer, and most of the call control layer processing of DPMR and DMR protocol. In DPMR mode, SCT3258 complies with ETSI TS 102 490 and ETSI TS 102 658. In DMR mode, it complies with ETSI TS 102 361. Figure 1-1 shows SCT3258 used in a DPMR or DMR system with conventional RF circuits. Figure 1-2 shows SCT3258 used with SCT3700. SCT3258 is designed for easy migration from analog radios. The system designer can start with a typical analog radio, replacing the analog base band processor with SCT3258 together with an external codec, to obtain the simplest form of a DPMR or DMR radio. To achieve the full potential of DPMR or DMR, application level software programming is required on the host processor.
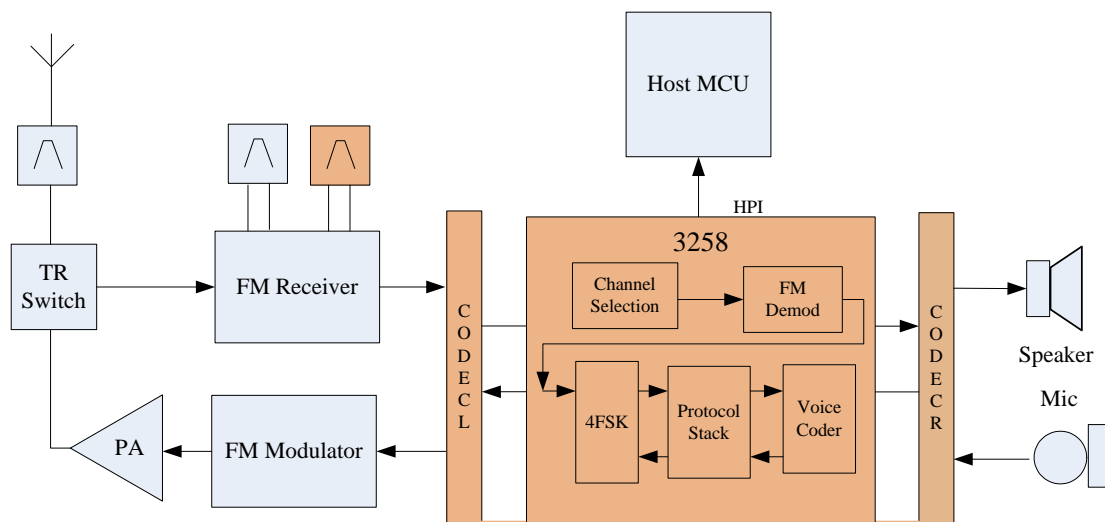
Figure 1-1 DPMR / DMR System Diagram with Conventional RF
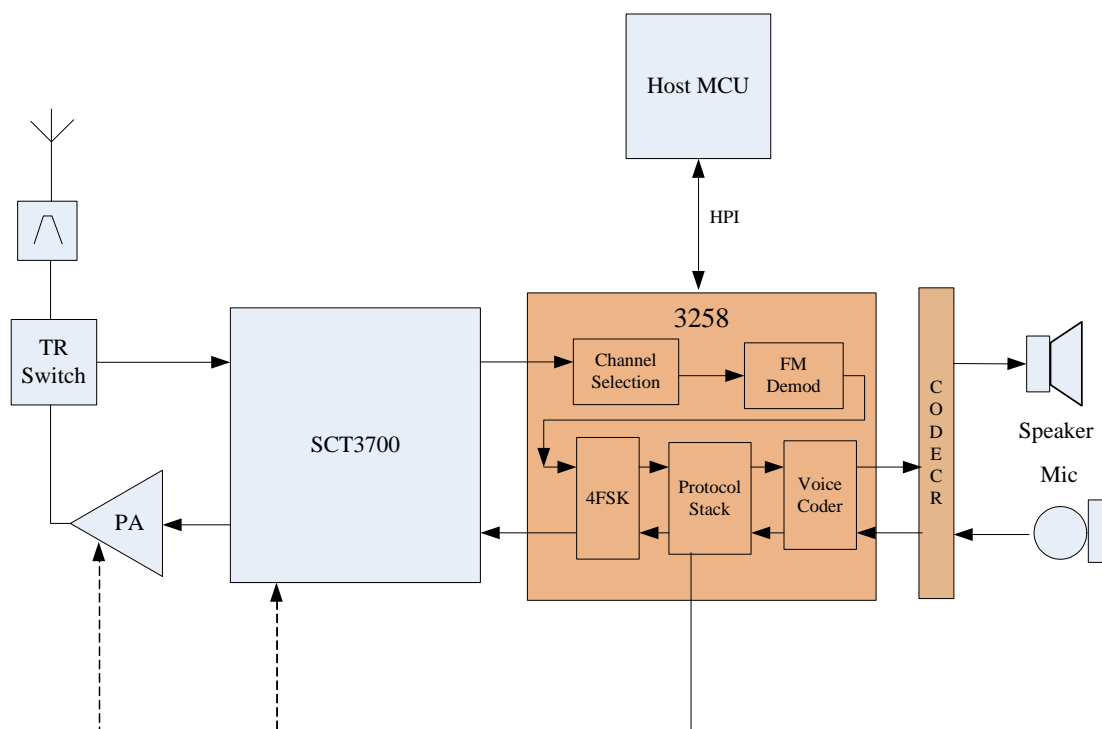
Figure 1-2 DPMR / DMR System Diagram with SCT3700

SCT3258 contains two high-speed serial ports, a single 8-bit processor interface (HPI), and a 4-pin programmable I/O port. The two serial ports are used for connection with external codec and external vocoder.

SCT3258 communicates with host processor with 8 bit HPI port (Intel Mode or Motorola Mode).

The firmware of SCT3258 is stored on chip. At the start of the system, the host processor downloads a small boot loader to SCT3258 to get SCT3258 started. SCT3258 then loads the entire firmware and starts execution.

SCT3258 core logic operates at 1.2 V, and the I/O operates at 2.5-3.3V.

SCT3258 is packaged in QFN64.

2 Features

DPMR

- Support DPMR Tier 1 (ETSI TS 102 490)
- Support DPMR Tier 2 (ETSI TS 102 658) Mode 1 and Mode 2
- Air interface physical layer (layer 1)
- Air interface data link layer (layer 2)
- Air interface call control layer (layer 3)
- Full Annex A support, with BCD addressing and automatic call match

DMR

- Support DMR Tier1 and Tier 2 (ETSI TS 102 361)
- Air interface physical layer (layer 1)
- Air interface data link layer (layer 2)
- Air interface call control layer (layer 3)
- Annex C (TS 102 361-2 Annex C) support, with BCD addressing and automatic call match
- Transmit in slotted or continuous mode
- Receive in slotted or continuous mode
- Support TDMA direct mode

4 FSK Modem

- 4800 bps data rate for DPMR and 9600 bps for DMR
- Automatic frame sync detection
- Programmable modulation index
- Support two point modulation, and I/Q modulation
- BER Test Mode complied with ITU O.153

Vocoder[1]

- Build-in AMBE + 2 vocoder from DVSI (no security key)
- Build-in AMBE + 2C vocoder from DVSI (no security key)
- Build-in ASELP 1.6 and 1.7 vocoder from Tsinghua University (requires 2mm x 1mm security key)
- Build-in ST24 and F100 vocoder
- Support other types of low bit rate vocoder with 3600 bps

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[1] Internal AMBE+2 is the default vocoder supported for DPMR/DMR operation, refer to CML sales representatives for the availability of other vocoder options.

- Support 1031 Hz Tone and Silence Test Mode
- Automatic vocoder switching at the receiver in DPMR mode

Analog Mode Support

- Support voice channel filters (LPF/HPF/Limiter), as well as pre-emphasis and de-emphasis filters.
- Support CTCSS/DCS generation and detection
- Support arbitrary CTCSS/DCS code, and blind detection
- Support the non-standard 55 Hz CTCSS tail tone
- Support compander
- Automatic analog/digital mode detection (analog/DPMR or analog/DMR) in receiver mode

Premium Features[2]

- Voice Recording and Playing back for local and remote
- 16 bit voice encryption

I/O

- Two high-speed TDM serial ports
- 8-bit HPI
- 4-pin PIO port

PLL

- On chip PLL circuit which provide system clock of up to 110.592MHz.

Technology

- QFN64 package
- Low power process, 38 mW in DPMR mode and 64 mW in DMR mode

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[2] Refer to CML sales representatives for the availability of premium feature options.

3 Hardware Architecture

As shown in the diagram below, SCT3258 hardware architecture consists 4FSK modem, DSP core, on-chip instruction and data memory, Boot RAM, two high-speed serial ports (configured as I2S and McBSP port), the host processor interface (HPI), direct memory access (DMA) controller, PIOs, and a phase-locked loop (PLL).

The voice coder/decoder and DPMR / DMR protocol stack are implemented internally in SCT3258.

I2S is used for connection to an external codec, e.g. TLV320AIC3204 from TI or WM8758B from Wolfson. The HPI is used for connection to an external MCU for control. The SCT3258 has on chip flash to stores its firmware. At the start of the system, the host processor downloads a small boot loader to SCT3258 to get it started. SCT3258 then loads the entire firmware and starts execution.

SCT3258 also have an option to connect to an external vocoder (e.g. AMBE 3000) through serial port 0.
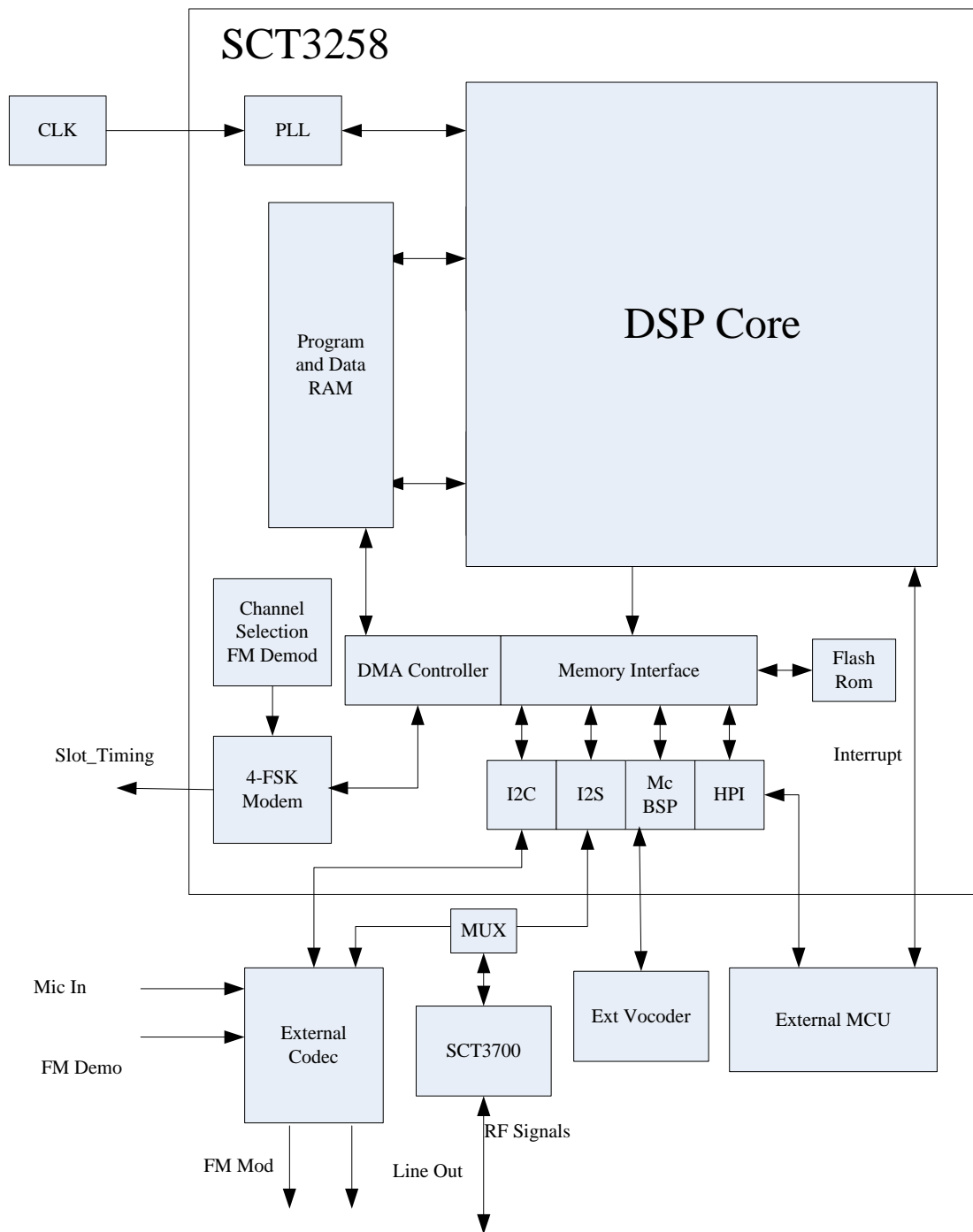
Figure 3-1   SCT3258 Architecture

4 Pin Configurations

SCT3258 is packaged in QFN64 package. The PINOUT of SCT3258 is described in Table 4-1.

PIN No.	PIN Name	I/O	Function
1	VDDIO33	P	I/O Device power
2	S1DO	O	Serial Port 1 Data Output
3	S1XFS	I/O	Serial Port 1 Transmit Frame Sync
4	S1CLK	I/O	Serial Port 1 Transmit or Receive Clock
5	S1RFS	I	Serial Port 1 Receive Frame Sync
6	S1DI	I	Serial Port 1 Data Input
7	VDD2	P	Core Power (1.2V)
8	VDDIO33	P	I/O Device power
9	S0DO	O	Serial Port 0 Data Output, connect to Pin19 FLASH_SI
10	S0XFS	I/O	Serial Port 0 Transmit Frame Sync, tie together with Pin13 S0RFS
11	S0XCLK	I/O	Serial Port 0 Transmit Clock
12	S0RCLK	I	Serial Port 0 Receive Clock
13	S0RFS	I	Serial Port 0 Receive Frame Sync, tie together with Pin10 S0XFS
14	S0DI	I	Serial Port 0 Data Input, connect to Pin42 FLASH_SO
15	PIO3/RF_TIMING	I/O	GPIO 3, RF_TIMING for DMR
16	PIO2	I/O	GPIO 2, connect to Pin40 /FLASH_CS, if SCT3258 is used with SCT3700, please refer to Figure 4-1 schematic
17	PIO1	I/O	GPIO 1
18	PIO0	I/O	GPIO0
19	FLASH_SI	I	SI for flash(refer to Pin9)
20	VDD2	P	Core Power (1.2V)
21	FLASH_SCK	I	SCK for flash
22	VDDIO33	P	I/O Device power
23	VDD2	P	Core Power (1.2V)
24	NC	-	No Connection
25	NC	-	No Connection
26	VDDIO33	P	I/O Device power
27	VDDIO33	P	I/O Device power
28	VDDIO33	P	I/O Device power
29	VDD2	P	Core Power (1.2V)
30	VDDIO33	P	I/O Device power
31	VDDIO33	P	I/O Device power
32	VDD2	P	Core Power (1.2V)

33	VDD2	P	Core Power (1.2V)
34	NC	-	No Connection
35	NC	-	No Connection
36	NC	-	No Connection
37	VDDIO33	P	I/O Device power
38	VDD2	P	Core Power (1.2V)
39	VDDIO33	P	I/O Device power
40	/FLASH_CS	I	/CS for flash(refer to Pin16)
41	VDD2	P	Core Power (1.2V)
42	FLASH_SO	O	SO for flash(refer to Pin14)
43	VDDIO33	P	I/O Device power
44	CLKOUT	O	Clock Out (Reflects the Processor Clock)
45	PLLBYPASS	I	PLL Bypass
46	CLKIN	I	Master Clock Input
47	PLLVDD	P	PLL Power (1.2V). We recommends the use of a ferrite bead to isolate VDD2 from PLLVDD
48	PLLSEL2	I	PLL Multiplier Select
49	VDD2	P	Core Power (1.2V)
50	HPIDATA7	I/O	HPI Data Bus
51	HPIDATA6	I/O	HPI Data Bus
52	HPIDATA5	I/O	HPI Data Bus
53	HPIDATA4	I/O	HPI Data Bus
54	HPIDATA3	I/O	HPI Data Bus
55	HPIDATA2	I/O	HPI Data Bus
56	HPIDATA1	I/O	HPI Data Bus
57	HPIDATA0	I/O	HPI Data Bus
58	NMI	I	Non-maskable Interrupt
59	RSTN	I	Device Reset
60	HOBIB	O	HPI Output Status
61	HRDN	I	Intel Mode Read Strobe / Motorola Mode Data Strobe.
62	HWRN	I	Intel Mode Host Write Strobe / Motorola Data Direction.
63	HCSN	I	Host Chip Select.
64	INT0	I	External Hardware Interrupt
65	GND	P	Package ground slug. Must be connect to GND

Table 4-1   PIN List for SCT3258

5 DPMR and DMR Implementation

SCT3258 supports the physical layer (layer 1), data link layer (layer 2), and call control layer (layer 3) of DPMR and DMR. Annex A of TS 102 490 / TS 102 658 and Annex C of TS 102 361-2 are also implemented. The user is expected to develop the application layer on the external MCU. This is illustrated in the diagram below.
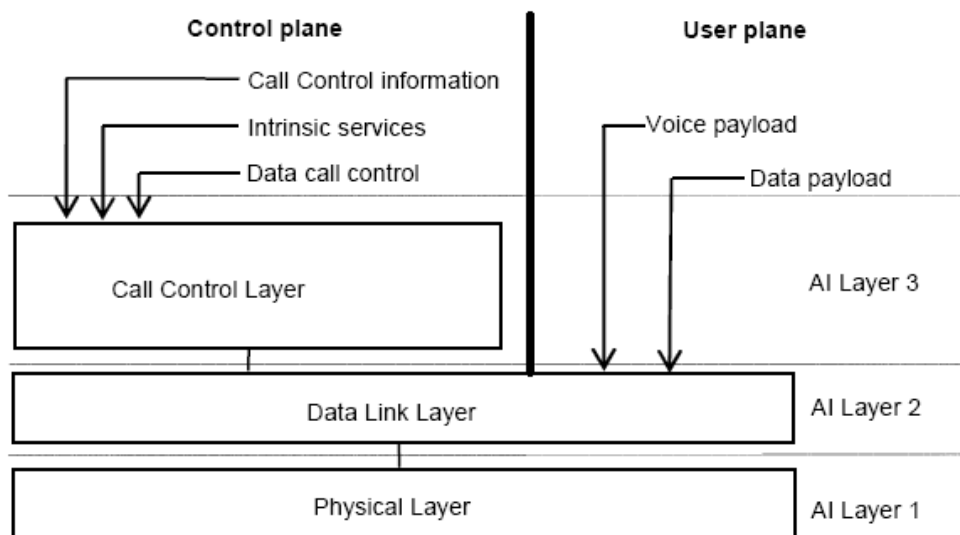
Figure 5-1   DPMR / DMR Protocol Structure

More specifically, the following are implemented in SCT3258 for each of the air interface layer.

Air Interface Physical Layer (Layer 1)

1. 4FSK modulation and demodulation, with programmable modulation index
2. Bit and Symbol definition
3. Frequency and symbol synchronization
4. Transmission burst building and splitting
5. BER test mode complied with O.153

Air Interface Data Link Layer (Layer 2)

1. Channel coding (FEC, CRC)
2. Interleaving, de-interleaving and bit ordering
3. Framing, super frame building and synchronization
4. Burst and parameter definition
5. Link addressing (source and destination)
6. Interfacing of voice applications (vocoder data) with PL
7. Data bearer services
8. Exchange signaling and user data with the CCL

Air Interface Call Control Layer (Layer 3)

1. Establishing, maintaining and termination of calls
2. Individual or group call transmission and receptions
3. Destination addressing
4. Automatic matching of Called ID of incoming call to own ID and group ID
5. Late entry call support

DPMR CSF (Annex A) Support
1. Full support of Standard User Interface (defined in Annex A of TS 102 490/TS 102 658)
2. Allows wild character dialing with "*"
3. Allows abbreviated dialing
4. Allows mask dialing
5. Syntax checking of dialed digits

DMR Dialing Number (Annex C) Support
1. Support of dialing number plan (defined in Annex C of TS 102 361-2)
2. Allows group calls with wild character "*"
3. Syntax checking of dialed digits

5.1   Signal Flow for DPMR / DMR Transmitter

The signal flow of the DPMR / DMR transmitter is shown in the diagram below.
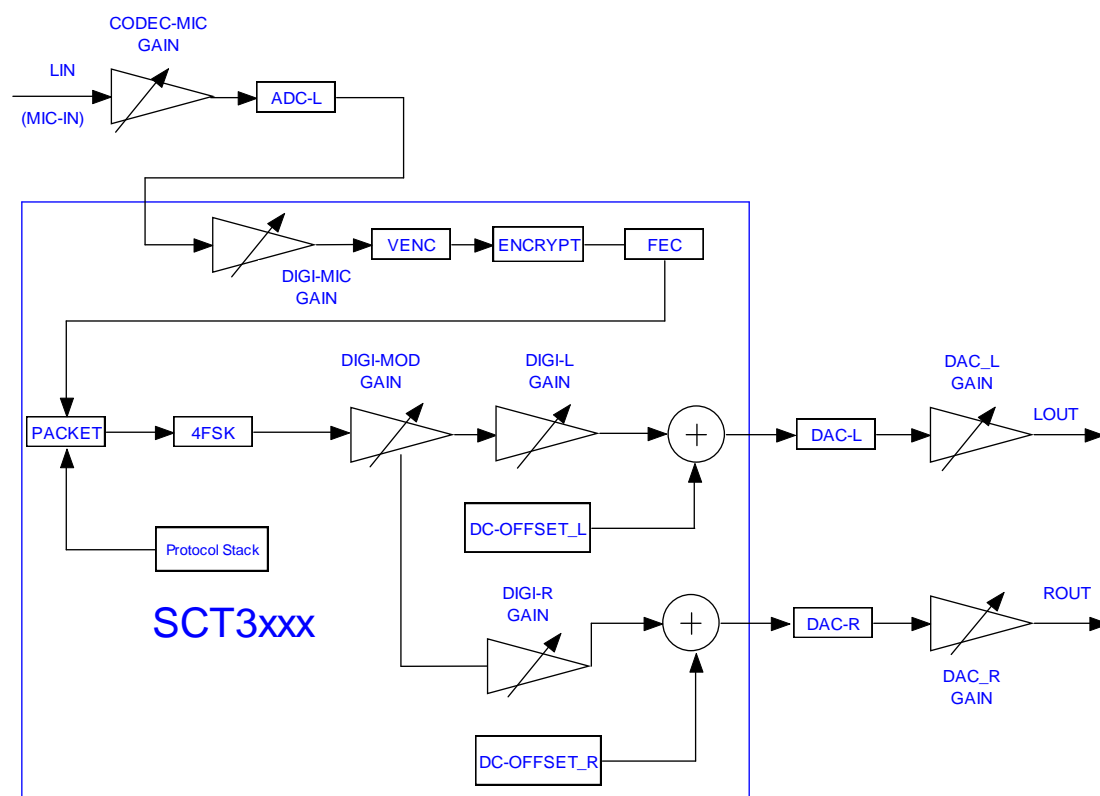

Figure 5-2   Signal Flow for DPMR / DMR Transmitter

The microphone signals are amplified by the VGA (variable gain amplifier) of the codec, and converted into digital form by the external codec and store in the left input channel buffer of SCT3258. The following steps are applied to the digitized signals:

1. Digital microphone gain, which provide a digital gain to the microphone. It is usually an attenuation to prevent microphone being saturated.
2. VENC, the voice encoder, which compress the voice signals into 2400 bps encoded signals
3. ENCRYPT, optional encryption block with configurable key
4. FEC, channel coding block, which adds 1200 bps to form 3600 bps signals for protecting of bit error
5. PACKET, which adds header and control information to form 4800 bps signals
6. 4FSK modulator
7. DIGI_MOD_GAIN, a gain block with linear 16 bit gain, for adjusting the modulation index

The resulting signals are split into left channel and right channel signals for two point modulation. Independent DC offsets and analog and digital gains are applied to the left and the right channels. The left channel control and the right channel control are identical, except that the left channel is multiplexed as speaker output in the RX mode. If DC coupling is used, the right channel is to be connected to VCTCXO input, while the left channel is connected to VCO. If AC coupling is used for VCTCXO control, either left or right channel can be connected to TCXO or VCO.

5.2   Signal Flow for DPMR / DMR Receiver

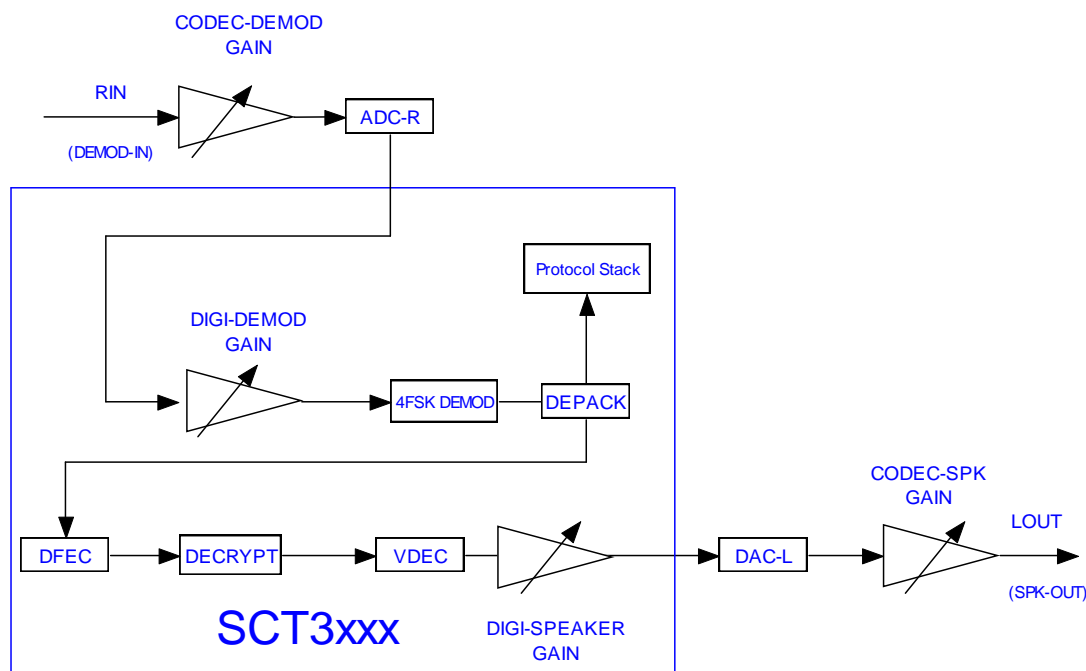The signal flow of the DPMR / DMR receiver is shown in the diagram below.

Figure 5-3 Signal Flow for DPMR / DMR Receiver for FM Demodulated Signal Input
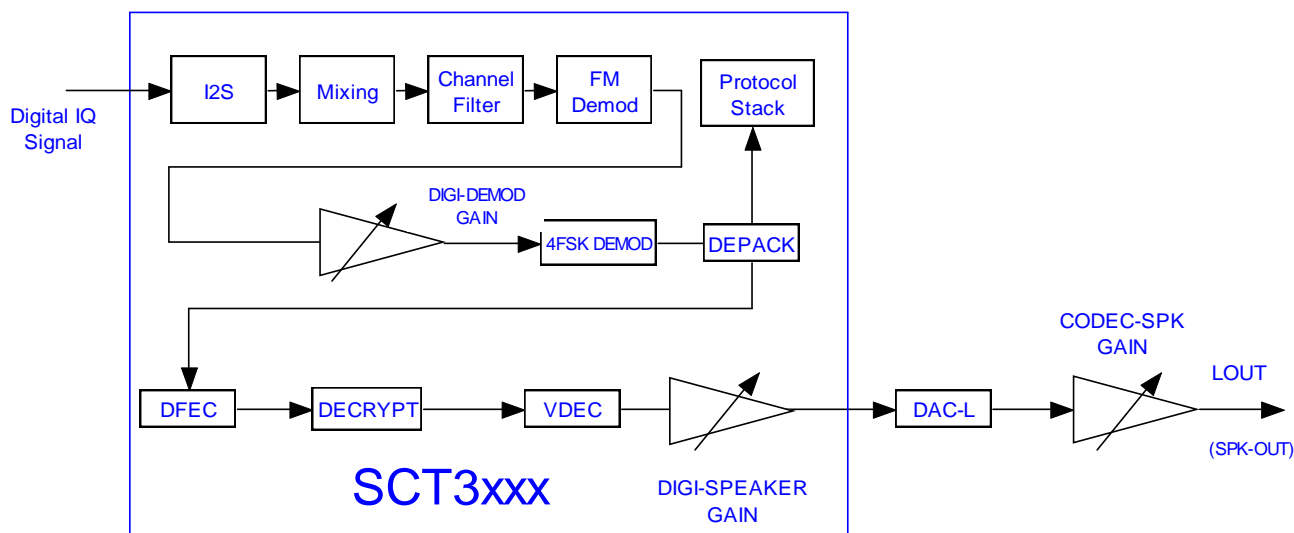
Figure 5-4 Signal Flow for DPMR/DMR Receiver for I/Q Signal Input

The FM demodulated signals are amplified by the VGA (variable gain amplifier) of the codec, and converted into digital form by the external codec and store in the right input channel buffer of SCT3258. The following steps are applied to the digitized signals:

1. DIGI_DEMOD_GAIN, a gain block with linear 16 bit gain
2. 4FSK demodulator
3. DEPACK, which removes header and extracts control and voice information
4. DFEC, channel decoding block, which recovers the encoded voice bits
5. DECRYPT, the optional decryption block with configurable key
6. VDEC, the voice decoder, which reconstructs voice signals
7. Digital Speaker Gain

The reconstructed voice signals are converted into analog form by the external codec and then amplified by the DAC analog gain block CODEC_SPK_GAIN before feeding to the audio PA.

For the I/Q signal case, the I/Q signal can be from digital interface or through an ADC. Additional processing is requires, such as IQ mixing, channel selection filter and FM demodulation. The rest of the process is the same as the demodulated case.

5.3   RF Timing Control for DMR

DMR signal is a two time slot TDMA signal, each slot occupying 30 milliseconds. In the RX mode, SCT3258 acquires timing from the synchronization pattern of the far end base station or mobile station. SCT3258 has an internal Slot Timing Signal (as shown in the diagram below) that is aligned with the FM demodulated signals or the I/Q signals at the input. In the TX mode,

SCT3258 controls the timing of the 4FSK modulation signals so that they are aligned with this internal RF timing signal. At the same time, an external signal is derived from the Slot Timing Signal and output through the RF_TIMING port to control the opening of the RF circuit and PA. The RF_TIMING signal is a square wave signals, with a period of 60 milliseconds. It can be exactly the same as the internal Slot Timing Signal, or offset from the Slot Timing Signal through MCU programming. The high level of RF_TIMING signal corresponds to RF circuit on, while the low level corresponds to RF circuit off. The MCU can derive the timing control signal to drive the RF transceiver or PA through the RF_TIMING signal from SCT3258.
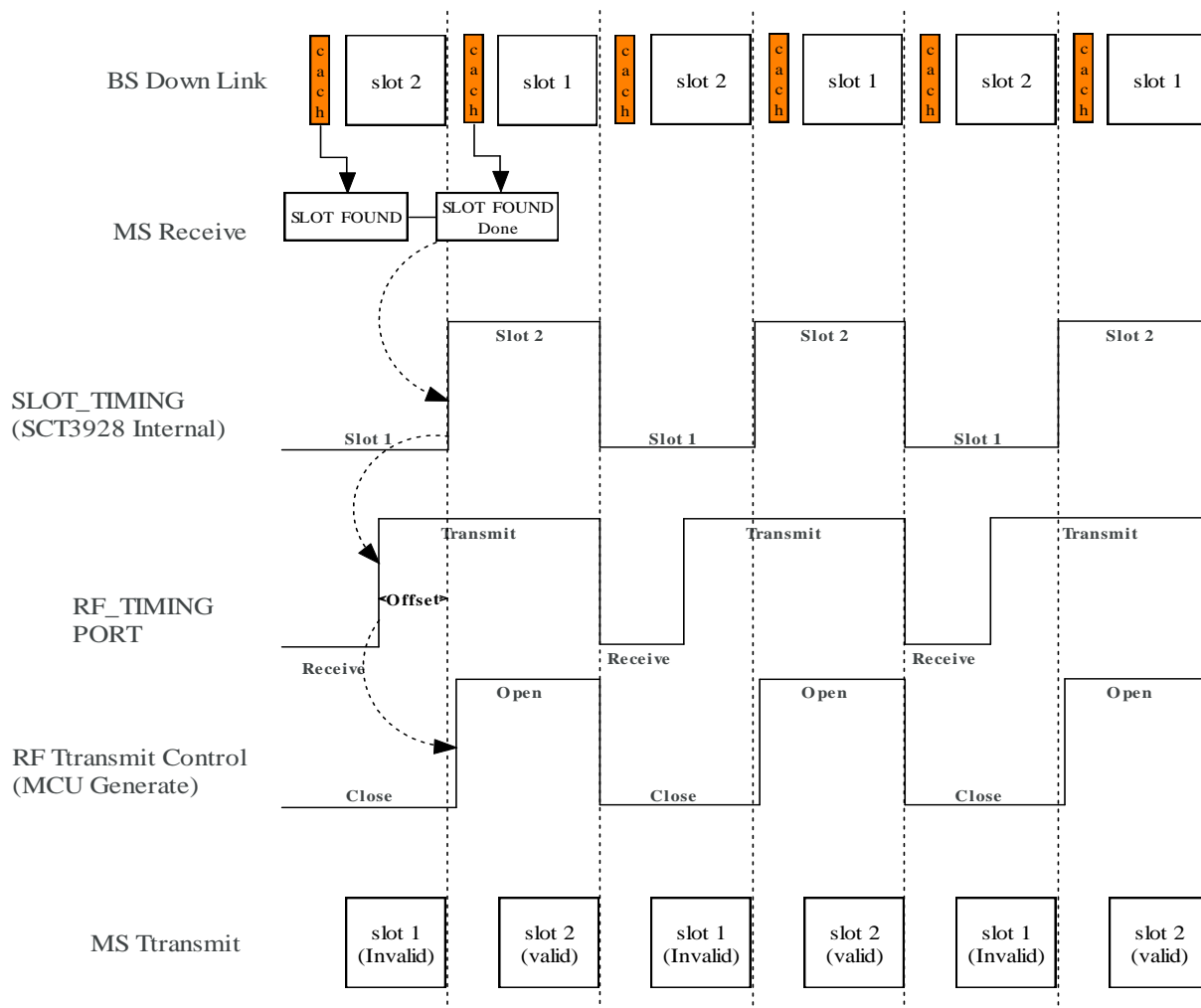
Figure 5-5 TDMA Timing Control of SCT3258

6 Vocoder Support[3]

SCT3258 supports the following vocoders:

- Build-in AMBE + 2 vocoder from DVSI (no security key)
- Build-in AMBE + 2C vocoder from DVSI (no security key)
- Build-in ASELP 1.6 and 1.7 vocoder from Tsinghua University (with 2mm x 1mm security key)
- Support other types of low bit rate vocoder with 3600 bps
- Support 1031 Hz Tone and Silence Test Mode

At factory, it can be configured to support AMBE+2C, or ASELP, or both. With ASELP, a small additional security key is required. The security key is a 2mm x 1mm 6 pin IC from Tsinghua University.

SCT3258 also supports external vocoder connection through its high speed serial port, and is pre-configured to support AMBE3000 from DVSI.

In DPMR mode, the receiver can be configured as automatic vocoder selection mode. In this mode, the receiver check the "Version" bit in the incoming DMPR bit stream and load the correct vocoder accordingly.

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[333] Internal AMBE+2 is the default vocoder supported for DPMR/DMR operation, refer to CML sales representatives for the availability of other vocoder options.

7 Premium Features[4]

Premium features are features specific to SCT3258 but not defined in the DPMR protocol. It won't affect interoperability with other implementation of DPMR protocol. However it provides useful extension to the protocol.

7.1   Encryption

SCT3258 supports 16 bit scrambler for voice encryption. In addition, for DPMR only mode, it also support 64 bit DES and 192 bit triple DES.

7.2   Voice Recording and Play Back

SCT3258 support voice recording and play back. When enabled, the encoded voice bit stream can be passed to the MCU for saving to the flash. Due to the high compression radio of the vocoder, large quantity of speech can be saved efficiently to small size memory. In particular, 40 minutes of speech can be saved in 1 M of flash memory.

Local near end and remote far end speech can be saved. Play back can be local or remote as well. Remote play back is especially useful in broadcasting pre-recorded speech contents.

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[4] Refer to CML sales representatives for the availability of premium feature options.

8 Analog Radio Support

SCT3258 supports tri-mode operation with DPMR, DMR and analog radio. For analog radio, it complies with related standards for analog radio including TIA 603C and ETSI EN-300296.

SCT3258 analog processing blocks include:

- HPF, with stop band at 255 Hz and pass band at 300 Hz
- LPF, with pass band at 2550 Hz or 3000 Hz, and stop band at 6000 Hz
- Compander
- Pre-emphasis filter and de-emphasis filter at 6 dB/octave
- Limiter to limit the maximum frequency deviation
- Sub audio filter with pass band at 255 Hz and stop band at 300 Hz
- CTCSS/DCS generation and detection supporting 38/51 CTCSS code and 83/107 DCS code
- Support blind CTCSS/DCS detection
- Support automatic polarity detection for DCS code
- Support arbitrary CTCSS/DCS code

8.1 Signal Flow for Analog Transmitter

The signal flow of the analog transmitter is shown in the diagram below.
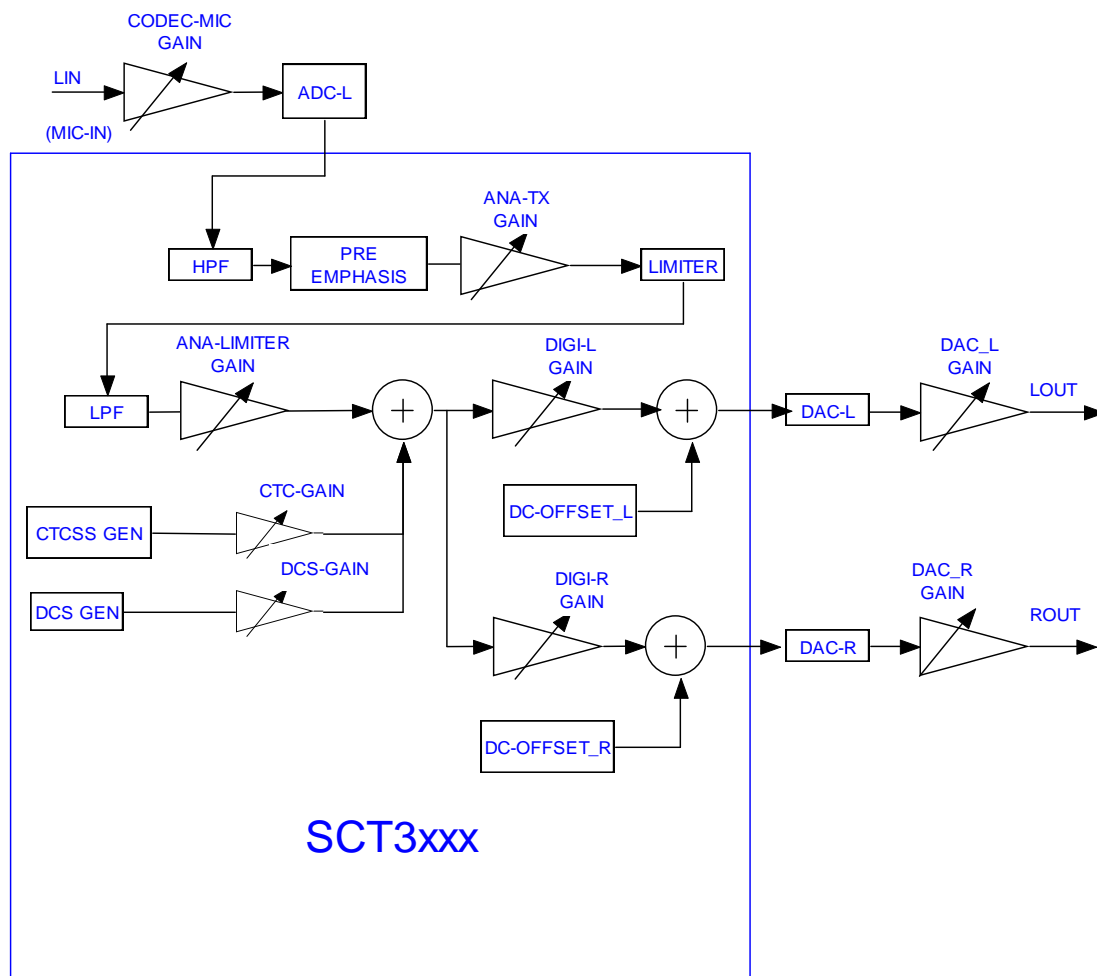
Figure 8-1 Signal Flow for Analog Transmitter

The microphone signals are amplified by the VGA (variable gain amplifier) of the codec, and converted into digital form by the external codec and store in the left input channel buffer of SCT3258. The following steps are applied to the digitized analog signals:

1. HPF, with pass band at 300 Hz, and stop band of 255 Hz.
2. Compressor
3. Pre-emphasis filter, with 6 dB/Octave
4. ANA_TX_GAIN, a gain block with linear 16 bit gain
5. Limiter for limiting the frequency deviation for large signals
6. LPF, with selectable corner of 2.55 kHz or 3kHz.
7. ANA_MOD_GAIN, a gain block with 16 bit gain after the limiter.

Beside the gain blocks, analog features that can be configured in the transmitter include:

1. BYPASS_FILTER: when enabled, all analog filters are by passed. A flat frequency response from 0-12 kHz results.
2. BYPASS_EMP: when enabled, pre-emphasis filter is by passed. A flat frequency response from 300 Hz to 2.55/3 kHz results.
3. CH_SEL: when enabled, the low pass corner is 3 kHz; when disabled, the low pass corner is 2.55 kHz.

The following table shows the composite frequency responses of channel filters based for different settings of BYPASS_FILTER, BYPASS_EMP and CH_SEL.

Frequencies (Hz)	BYPASS_ FILTER = 1 (in dB)	BYPASS_FILTER = 0 (in dB)			
		BYPASS_EMP = 0		BYPASS_EMP = 1	
		CH_SEL = 0	CH_SEL = 1	CH_SEL = 0	CH_SEL = 1
100	0.0	-49.6	-48.6	-46.3	-46.8
250	0.0	-49.6	-47.6	-49.3	-50.3
300	0.0	-10.0	-9.9	0.5	0.5
350	0.0	-8.8	-8.6	0.5	0.5
500	0.0	-5.6	-5.6	0.4	0.4
700	0.0	-2.9	-2.9	0.2	0.2
1000	0.0	0.0	0.0	0.0	0.0
1500	0.0	3.8	3.7	0.3	0.2
2000	-0.1	6.2	6.4	0.3	0.5
2500	0.0	8.1	8.0	0.4	0.2
3000	-0.1	-12.0	9.3	-21.2	0.0
3500	-0.1	-46.1	-21.4	-49.3	-31.3
6000	-0.2	-50.6	-47.6	-50.3	-49.3

Table 8-1 Frequency Response of the Analog Transmitter

An example of frequency response is also shown in the figure below.
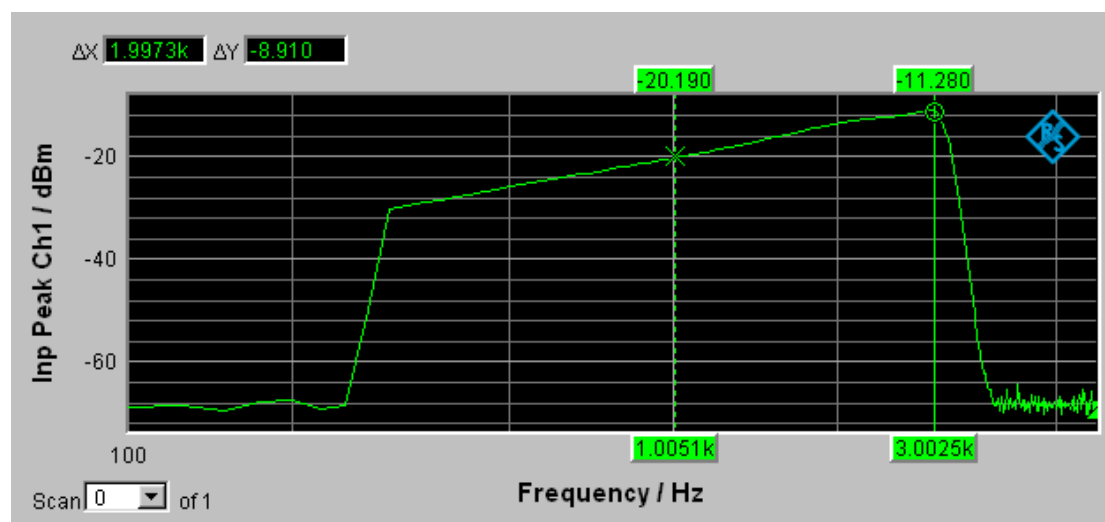
Figure 8-2 Frequency Response of the Transmitter with CH_SEL=0, BYPASS_EMP = 0, BYPASS_FILTER = 0

If CTCSS/DCS is enabled, the internally generated CTCSS/DCS signals are added to the voice signals. The amplitude of the CTCSS/DCS can be modified by CTC_GAIN or DCS_GAIN block.

The resulting signals are split into left channel and right channel signals for two point modulation.

Independent DC offsets and analog and digital gains are applied to the left and the right channels. The left channel control and the right channel control are identical, except that the left channel is multiplexed as speaker output in the RX mode. If DC coupling is used for TCXO control, the right channel is to be connected to VCTCXO input, while the left channel is connected to VCO. If AC coupling is used for VCTCXO control, either left or right channel can be connected to TCXO or VCO.

8.2   Signal Flow for Analog Receiver

The signal flow of the analog receiver is shown in the diagram below.
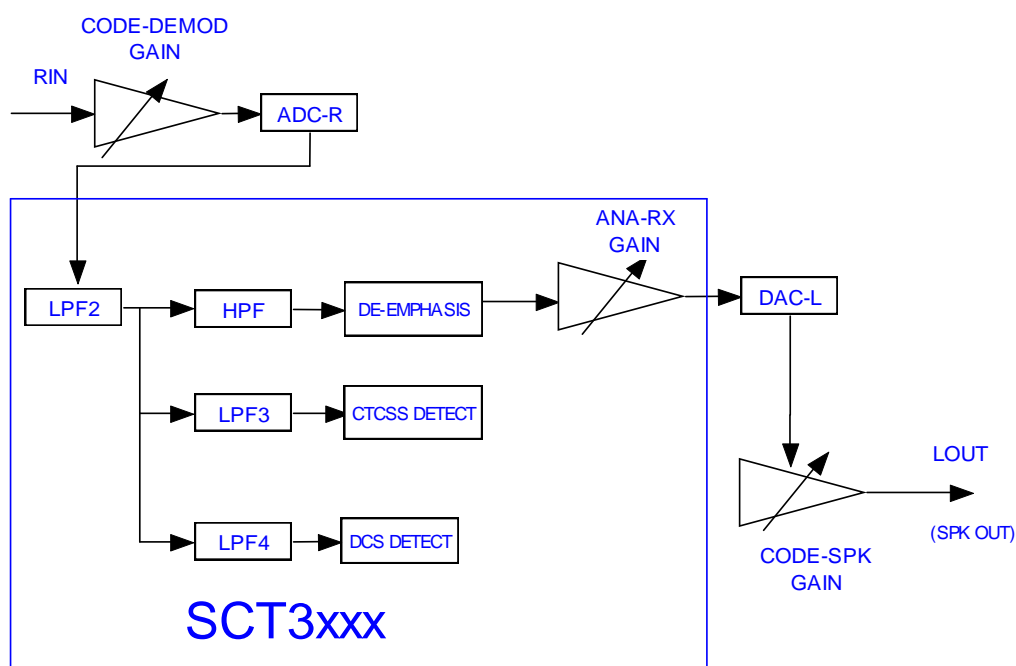
Figure 8-3 Signal Flow for Analog Receiver with FM Demodulated Signal Input
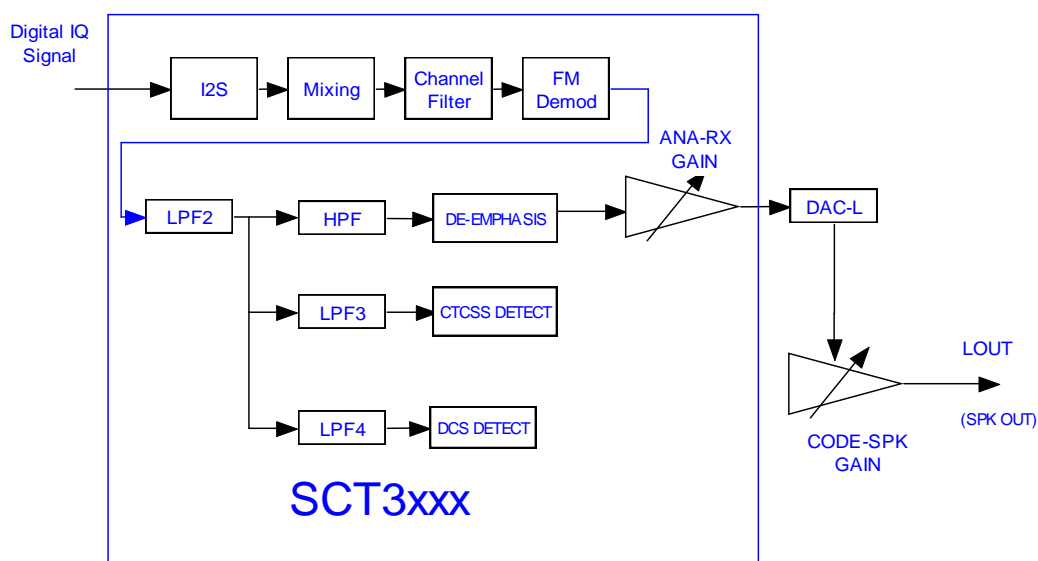
Figure 8-4 Signal Flow for Analog Receiver with IQ Signal Input

The FM demodulated signals are amplified by the VGA (variable gain amplifier) of the codec, and converted into digital form by the external codec and store in the right input channel buffer of SCT3258. The following steps are applied to the digitized analog signals:

1. LPF2, with low pass corner at 3000 Hz
2. HPF, with pass band at 300 Hz, and stop band of 255 Hz.
3. De-emphasis filter, with 6 dB/Octave
4. Expander
5. ANA_RX_GAIN, linear 16 bit gain

The filtered digital signals are converted into analog form by the external codec and then amplified by the DAC analog gain block CODEC_SPK_GAIN before feeding to the audio PA.

Beside the gain blocks, analog features that can be configured in the receiver include:
1. BYPASS_FILTER: when enabled, all analog filters are by passed. A flat frequency response from 0-12 kHz results.
2. BYPASS_EMP: when enabled, de-emphasis filter is by passed. A flat frequency response from 300 Hz to 2.55/3 kHz results.

The following table shows the composite frequency responses of channel filters based for different settings of BYPASS_EMP.

Frequencies (Hz)	BYPASS_FILTER = 1 (in dB)	BYPASS_FILTER = 0 (in dB)	
		BYPASS_EMP = 0	BYPASS_EMP = 1
100	0.0	-39.9	-47.9
250	0.0	-53	-54.3
300	0.0	8.4	0.5
350	0.0	7.6	0.5
500	0.0	5.5	0.4
700	0.0	3.0	0.2
1000	0.0	0.0	0.0
1500	0.0	-3.2	0.2
2000	0.0	-5.4	0.5
2500	-0.1	-7.7	0.2
3000	-0.1	-9.6	0.0
3500	-0.3	-41.6	-31.6
6000	-0.4	-53.5	-54.3

Table 8-2 Frequency Response of the Analog Receiver

An example of frequency response is also shown in the figure below.
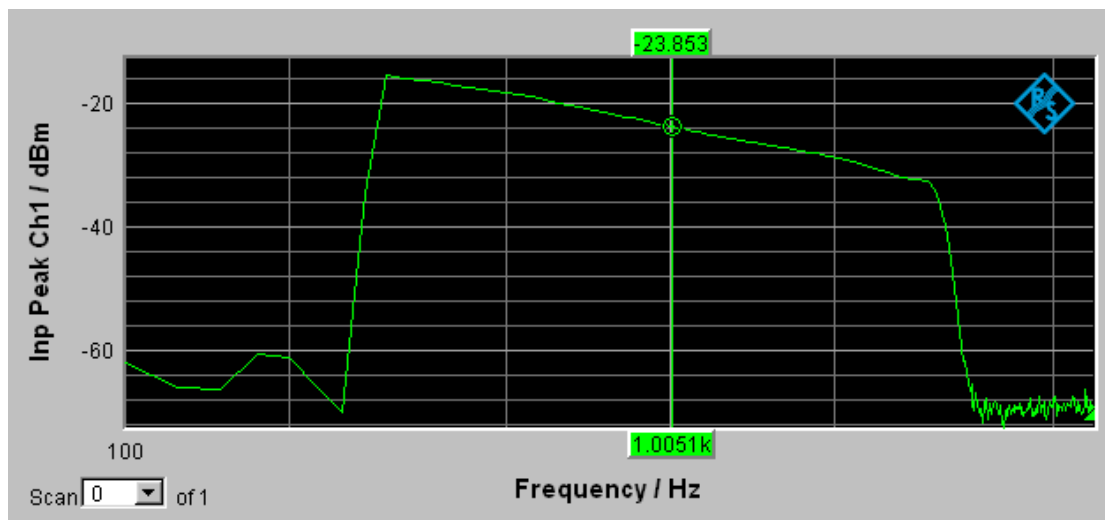
Figure 8-5 Frequency Response of the Transmitter with BYPASS_EMP=0, BYPASS_FILTER=0

Two additional low pass filters are applied to the output of LPF2 to extract CTCSS and DCS signals for detection. The detection results are reported to the MCU though HPI interface.

For the I/Q signal case, the I/Q signal can be from digital interface or through an ADC. Additional processing is requires, such as IQ mixing, channel selection filter and FM demodulation. The rest of the process is the same as the demodulated case.

9 Hardware Interface

9.1 Clock Input

SCT3258 requires a fixed clock input of 12.288 MHz, with a peak to peak voltage of 1.2V to 3.3V. The clock input can be sine wave or square wave.

To comply with DPMR / DMR requirement of 2 ppm on base band timing, the clock input of SCT3258 should be within 2 ppm as well. However, when communicating with another DPMR / DMR terminal also using SCT3258, 20 ppm clock input is sufficient.

However, if DMR TDMA direct mode is to be supported, the clock input requirement is 0.5 ppm, per TS 102 361.

9.2 PLL

SCT3258 integrates a build-in PLL to generate a high frequency processor clock from a slower off-chip clock source. The off-chip clock source is applied to the CLKIN signal.

The PLLBYPASS and PLLSEL2 signals govern the operation of the PLL. When PLLBYPASS is LOW, the PLL is active and generates the processor clock as determined the value of PLLSEL2 signal. When PLLBYPASS is HIGH, the PLL is bypassed, and the external clock source is used directly as the processor clock. In either case, the CLKOUT signal reflects the processor clock.

CLKOUT = CLKIN * PLL_MUL.

PLL_MUL is determined by the PLLSEL2, as shown in the table below:

PLLSEL2	PLL Multiplier
0	5
1	9

Table 9-1 PLL Settings

To avoid potential glitches due to system clock frequency change, it is recommended that the MCU put SCT3258 into a sleep mode before making any changes to PLLBYPASS and PLLSEL2, and then wake up after making the changes. If the MCU need to make changes to both PLLBYPASS and PLLSEL2, it should put SCT3258 into sleep twice and make change one at a time.

9.3 Serial Ports, I2S, McBSP

SCT3258 contains two identical synchronous serial ports (0 and 1) that support 8- or 16-bit

transfers. One of the serial port is configured as I2S for connection with external codec. The other serial port is configured as McBSP port to connect to external vocoder such as AMBE3000. The serial ports are capable of generating their own bit clock and frame sync signals. The maximum transfer rate in either active or passive mode is one-half the processor clock rate.

Serial port 1 is pre-configured to connect to an external codec. Sicomm recommends TLV320AIC3204 from TI or WM8758B from Wolfson and provides the interface codes and schematics for these codecs.

Other codecs can be used, as long as it conforms to the format described in this document.

Serial port 0 is used for flash access.

9.3.1 Serial Port Pins

PIN Name	I/O	Function
S0DI/S1DI	I	Serial Port Data Input. The S0DI and S1DI pins are the data input pins of serial port 0 and serial port 1, respectively.
S0DO/S1DO	O	Serial Port Data Output. The S0DO and S1DO pins are the data output pins of serial port 0 and serial port 1, respectively.
S0RCLK/S1RCLK	I	Serial Port Receive Clock. The S0RCLK and S1RCLK pins are the serial port receive clocks. The maximum frequency for S0RCLK/S1RCLK is one half of the system clock (System clock is reflected on the CLKOUT signal)
S0RFS/S1RFS	I	Serial Port Receive Frame Sync. This signal indicates the beginning of a new word transfer. In burst mode, a frame sync is required every data word (8 or 16 bits); in continuous mode, a frame sync is required for the first data word only.
S0XCLK/S1XCLK	I/O	Serial Port Transmit Clock. The serial port transmit clock is configured as an input or an output by programming the serial port control register. As an input, the signal applied to S0XCLK or S1XCLK is used as the transmit clock. As an output, the transmit clock is generated internally. The transmit clock rat is determined by the processor clock scale by the value in the sp0icd or sp1icd register.
S0XFS/S1XFS	I/O	Serial Port Transmit Frame Sync. The transmit frame sync is configured as an input or an output by programming the serial port control register. As an input, the signal applied to S0XFS or S1XFS is used as the transmit frame sync. As an output, the transmit frame sync is generated internally every data word (8 or 16 its) in burst mode, with a duration of one bit-clock. In continuous mode, the frame sync is

		generated for the first data word only.

<div align="center">**Table 9-2 Serial Pin Descriptions**</div>

9.3.2 Serial Connection to External Codec

In this example, SCT3258 is connected to a stereo codec through serial port 1. TI TLV320AIC3204 is a general purpose, dual-analog, front-end geared toward stereo music applications. It features two 16-bit A-to-D converters and two 16-bit D-to-A converters. Data information pass through the serial port interface, and control is done through I^{2}C interface.

The serial port interface of TLV320ACI3204 features a single shared-transfer bit clock (BCLK), a word clock (WCLK), a serial data output (DOUT), and a serial data in signal (SDI). The signaling interface of TLV320ACI3204 is very flexible and can be configured for left or right-justified, I^{2}S, DSP, or TDM modes. However, it only supports stereo operations. Each of the frames for TLV320ACI3204 has two slots.

To connect TLV320ACI3204 to SCT3258, TLV320ACI3204 should be configured as DSP mode, while SCT3258 is configured as 2-slot TDM mode. Both are configured as 16 bit, MSB first, and frame sync one clock before the first data bit. TLV320ACI3204 provides both the bit clock, and frame sync (word clock) in both TX and RX operations.

Figure 9-1 shows the timing diagram of TLV320ACI3204 in DSP mode, with frame sync one clock before the first data bit.
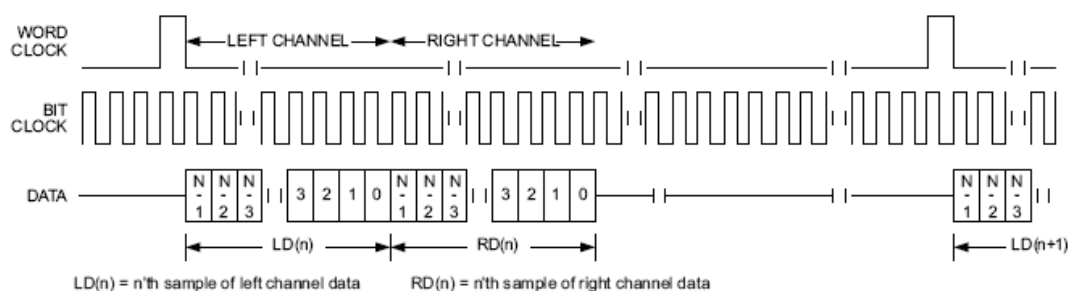

<div align="center">**Figure 9-1 Timing Diagram of TLV320ACI3204 in DSP Mode with Offset = 1**</div>

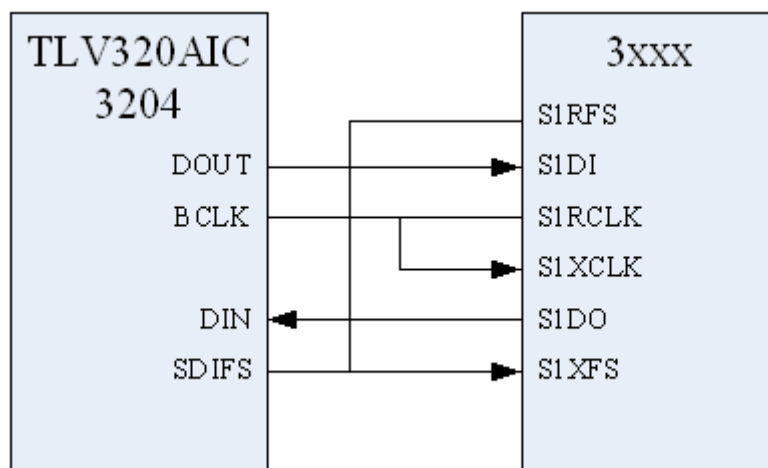Figure 9-2 shows the connection of TLV320ACI3204 to SCT3258.

Figure 9-2 TLV320ACI3204 Connection Diagram

SCT3258 uses two PIO ports (PIO[0:1]) to simulate I^2C and connects to the I^2C interface of TLV320ACI3204 for control.

SCT3258 configures TI codec in 16 bit stereo mode, with a sampling rate of 24 kHz. MSB is transmitted first. The right channel is transmitted immediately after the LSB of the left channel is transmitted. The MSB of the left channel is clocked out at the rising edge of the second clock after the rising edge of the frame SYNC and can be latched in by the falling edge of the clock.

Other codecs can be used with SCT3258, as long as it can be configured to support the format described above, through an I^2C control interface. The I^2C address can be configured by sending command to SCT3258.

9.4   HPI

SCT3258 is connected to the MCU through 8 bit HPI port. The HPI port can be configured as Intel Mode or Motorola Mode.

HPI is first used for downloading a boot loader. After DSP starts execution, the HPI is used for passing the call information and management information between SCT3258 and the MCU.

The HPI is an asynchronous 8-bit parallel port. The port is a slave port only, and all control signals to the HPI port are inputs rather than output. There are many different types of controlling processors, but they have interface protocols that fall into two broad categories. One type communicates with slaves using separate read and write strobes, which is referred to as Intel mode. The other type communicates with slaves using a read/write indicator and a common data strobe. This interface protocol is called Motorola mode.

The HPI supports Intel-style and Motorola-style interfaces, and supports word transfers in both modes. The maximum transfer is 1 byte every three processor clock cycles. The user can program the active level of the status signals and the data strobe.

The HPI contains receive and transmit FIFOs for the HPI. Both FIFOs are 16 bits wide and 64 words deep. The receive FIFO stores write data received from the HPI host. The transmit FIFO stores data destined for the HPI host during a host read operation. FIFOs allow the SCT3258 to store up to 64 words in the transmit buffer when the host is not reading from the SCT3258. This buffer helps the HPI interface to run much faster because the two sides do not need to wait for the other to read/write. The same capability exists in the receive FIFO. A host can write up to 64 words to the SCT3258 without the SCT3258 emptying the HP receive register for each word.

The HPI external bus interface is 8 bits wide. Internally, the HPI port is configured to pack or unpack 16-bit words into 8 bits for bus access. As a result, the HPI interface expects transfers to occur in multiples of two. When the second byte is received / transferred, the internal HPI state is updated. The HPI is also programmed to transfer the most significant byte first.

The HPI contains a control register, transmit register, and receive register. All three registers are memory-mapped and reside in the SCT3258 memory space. The HPI transmit (hpixd) register transfers data from the SCT3258 to the host. The SCT3258 writes to the transmit register, which is coupled to the transmit FIFO. The host then reads from the other end of the FIFO. Writes to the transmit register are ignored if the transmit FIFO is full. From the SCT3258 software perspective, the FIFO is largely invisible. All writes occur to the HPI TX register, and the FIFO is coupled to the TX register through hardware. Status bits in the HPI control (hpictl) register can indicate FIFO status.

The HPI receive register lets the SCT3258 receive data from the host. The HPI bus interface unit accepts data written from the host and stores the data in the receive FIFO. The SCT3258 then reads words from the HPI receive register, which points to the other end of the receive FIFO. Invalid data is transferred if the receive FIFO is full when a host write occurs. The external bit IBF signals the host when the input buffer is full.

An HPI chip select, HCSN, allows for system architectures with multiple devices using the same parallel bus. When HCSN is deasserted, the HPI data bus is placed in the high impedance state and the data strobes are ignored.

The hpictl register is only readable by host. The available bits include:

Bit Position	Bit Name	Descriptions
11	honf	Output FIFO Not Full: When this read-only bit is set, the output FIFO is not full and additional words can be written to the hpixd register. When cleared, the output FIFO is full and no additional words should be written to the hpixd register.
10	hine	Input FIFO Not Empty: When this read-only bit is set, the input FIFO is not empty and additional words can be read from the hpird register. When cleared, the input FIFO is empty and no additional words should be read from the hpird register.

1	hobe	HPI Output Buffer Empty Status:
		This read-only bit indicates when the transmit buffer is empty.
0	hibf	HPI Input Buffer Full Status
		This read-only bit indicates when the input buffer is full.

9.4.1 Intel Mode

In Intel mode, the HPI operates as an Intel-style interface, which is for processors that communicate with slaves using separate read and write strobes. The data strobes are asynchronous to the DSP processor clock. Refer to Section 12.6, "Host Processor Interface (HPI) Timing," for HPI waveforms.

9.4.1.1 Intel Mode Host Reads

Intel mode read cycles can be initiated / ended by either the HRDN read strobe signal or the HCSN chip select signal. To begin the read, HCSN and HRDN must be LOW. The last falling edge determines the starting time of the read cycle. After both HCSN and HRDN are asserted, the HPI drives the contents of the HPI transmit (hpixd) register on the data bus (HPIDATA[7:0]).

An Intel mode read ends when either the HCSN or HRDN signal is deasserted. When the read transaction ends, the processor sets the output buffer empty (hobe) bit in the hpictl register if the transmit FIFO is empty. The output status (HOBIB) signal is also asserted at the end of the read transaction if transmit FIFO is empty. If the transmit FIFO is not empty, the hobe bit is not asserted after the read, and HOBIB signal is not asserted. Refer to Section 12.6, "Host Processor Interface (HPI) Timing," for details on HPI waveforms.

9.4.1.2 Intel Mode Host Writes

Intel mode write cycles can be initiated / ended by either the HWRN write strobe signal or the HCSN chip select signal. To begin the write, HCSN and HWRN must be LOW. The last falling edge determines the starting time of the write cycle. After both HCSN and HWRN are asserted, the data on the HPI data bus (HPIDATA[7:0]) is registered in the HPI receive data register (hpird). Data is registered on a rising edge of every processor cycle for the duration of the access.

An Intel mode write ends when either the HCSN or HWRN signal is deasserted. When the write transaction ends, the processor sets the input buffer full (hibf) bit in the hpictl register if the RX FIFO is full. The output status (HOBIB) signal is also asserted at the end of the write transaction if the RX FIFO is full. If the RX FIFO is not full, the hibf bit in the hpictl register is not asserted, and the HOBIB signal is not driven.

9.4.2 Motorola Mode

In Motorola mode, the HPI operates as a Motorola-style interface, which is for processors that communicate with slaves using a read/write indicator and a common data strobe. The data strobe, which has programmable polarity, is asynchronous to the DSP processor clock. Refer to

Section 12.6, "Host Processor Interface (HPI) Timing," for details on HPI waveforms.

9.4.2.1 Motorola Mode Host Reads

To perform a Motorola mode host read, both the host chip select (HCSN) and data strobe (HRDN) signals must be asserted (in Motorola mode, the HRDN signal operates as the active-LOW data strobe signal.) The last falling edge determines the starting time of the read cycle. The HWRN data direction signal must be HIGH. After both HCSN and HRDN are asserted, the HPI drives the contents of the HPI transmit (hpixd) register on the data bus (HPIDATA[7:0]).

A Motorola mode read ends when either the HCSN or HRDN signal is deasserted. When the read transaction ends, the processor sets the output buffer empty (hobe) bit in the hpictl register if the TX FIFO is empty. The output status (HOBIB) signal is also asserted at the end of the read transaction if transmit FIFO is empty. If the transmit FIFO is not empty, the hobe bit is not asserted after the read, and HOBIB signal is not asserted. Refer to Section 12.6, "Host Processor Interface (HPI) Timing," for details on HPI waveforms.

9.4.2.2 Motorola Mode Host Writes

To perform a Motorola mode host write, both the host chip select (HCSN) and data strobe (HRDN) signals must be asserted. (In Motorola mode, the HRDN signal operates as the active-LOW data strobe signal.) The last falling edge determines the starting time of the write cycle. The HWRN data direction signal must be LOW. After both HCSN and HRDN are asserted, the data on the HPI data bus (HPIDATA[7:0]) is registered in the HPI receive data (hpird) register. Data is registered on a rising edge of every processor cycle for the duration of the access.

A Motorola mode host write ends when either the HCSN or HRDN signal is deasserted. When the write transaction ends, the processor sets the input buffer full (hibf) bit in the hpictl register if the RX FIFO becomes full. The output status (HOBIB) signal is also asserted at the end of the write transaction if the RX FIFO becomes full. If the RX FIFO does not become full after the write, then neither the hibf bit nor the HOBIB signal is asserted.

9.4.3 HPI Pins

PIN Name	I/O	Function
HCSN	I	Host Chip Select. This active-LOW signal enables the HPI. When HCSN is asserted, the HPI is enabled and normal operation can processed. When HCSN is de-asserted, HPIDATA[7:0] is placed in the high impedance state, and the HPI rea/write strobes are ignored.
HOBIB	O	HPI Output Status. It indicates receive buffer full (hibf bit) or transmit buffer empty (hobe bit) status.
HPIDAT[7:0]	I/O	HPI Data Bus. This bi-directional 8-bit bus is the HPI data bus. When idle, this bus retains its previous state. When HCSN is de-asserted, the bus is place in the high-impedance state.
HRDN	I	Intel Mode Read Strobe / Motorola Mode Data Strobe.

		In Intel mode, HRDN is an active-low read strobe that causes SCT3258 to write the contents of the HPI transmit register onto HPIDATA[7:0] for the duration of the access.
HWRN	I	Intel Mode Host Write Strobe / Motorola Data Direction. In Intel mode, HWRN is a write strobe that causes the SCT3258 to latch the data on HPIDATA[7:0] into the HPI receive register during the access clock cycle. In Motorola mode, this signal functions as a read/write select. When HWRN is HIGH, a host read is being performed; when LOW, a host write is being performed. In both cases, this signal must be valid for the duration of the access.

Table 9-3 HPI PIN Descriptions

9.4.4 Use HOBIB for Hand Shaking with Host

The HOBIB signal reflects the status of the hibf (input buffer full) or hobe (output buffer empty) bits in the hpictl register (the logical OR of these flags). It is the logic OR of hibf and hobe, and is active high.

SCT3258 uses interrupt mechanism to handle receiving and transmitting data through the HPI. It is highly unlikely that input buffer would be full unless 64 words (128 bytes) of data are sent at the maximum speed by the host and no interrupt is triggered in SCT3258 to read the data. As a result, HOBIB is reliable indication of hobe. The host can poll HOBIB to know if SCT3258 has data to send. If HOBIB is low, SCT3258 has data to send. The host can then start the host read cycle and read data from SCT3258 till HOBIB is high.

An exception to the above statement is that HOBIB is low at reset even though there is no data at SCT3258 to send to the host. HOBIB won't go high until bootloader is downloaded to SCT3258. In that case, besides checking the level of HOBIB, the host should also check the contents of HPI, until "17 01" or "17 00" is received from SCT3258. "17 01" indicates successful application firmware downloading at SCT3258. "17 00" means that reset is successful, however, no application firmware is downloaded and active in SCT3258. The host needs to download firmware to SCT3258 through HPI.

9.5   Boot Loading

SCT3258 is automatically configured after reset to load a 1024-word block of instructions from the HPI port. SCT3258 then begins executing that instruction block immediately.

The HPI port is configured in 16-bit mode, low-byte first, and either Intel mode or Motorola mode. PIO1 is sampled at the rising edge and used to select either Intel (LOW input) or Motorola (HIGH input).

The host must download exact 1024 words for this boot process to work. Generally the downloaded code contains a second boot loader, allowing the full application program to be

downloaded, either from the host through HPI interface, or directly from the on chip flash.

Note that the boot loader for DPMR mode and DMR mode is different. Depending on the boot loader types, SCT3258 enters DPMR mode or DMR mode. In DPMR mode, commands for DMR only (type 5) are not recognized. In DMR mode, commands for DPMR only (type 3) are not recognized.

After SCT3258 is successfully booted, the user can observe the following:
1. SCT3258 sends a response packet to the host through HPI, with the following contents
   84 a9 61 00 02 20 17 01

10   System Interface

10.1   System Related Signals

This section describes the external system interface signals.

Signal Name	Input/Output	Descriptions
CLKIN	Input	Master Clock Input. This signal accepts the master clock input for the device. The acceptable clock input frequency is 12.288MHz, with a level of 1.2-3.3V.
CLKOUT	Output	Processor Clock Output. This signal directly reflects the processor clock. If PLLBYPASS is high, CLKOUT reflects the clock applied to CLKIN. If PLLBYPASS is LOW, then CLKOUT reflects the PLL output.
INT0	Input	External Hardware Interrupts. The INT0 signal provides an external hardware interrupt source to SCT3258. SCT3258 takes an interrupt when INT0 is asserted. INT0 is edge-triggered; a sampled LOW-to-HIGH transition defines one occurrence of the interrupt. INT0 must be asserted for at least one processor clock period to guarantee the interrupt request is taken. INT0 is always sampled on a rising edge of the processor clock, and transitions are ignored during reset. INT0 is used to wake up SCT3258 when it is in SLEEP mode. If unused, INT0 must be tied LOW.
NMI	Input	Non-maskable Interrupt. NMI is an external hardware interrupt that has the highest priority of all the SCT3258 interrupts. NMI is sampled on the rising edge of the processor clock, and must be asserted for a minimum of one processor clock period. A sampled LOW-to-HIGH transition asserts the NMI interrupt request. The processor branches to address 0. NMI has the same effect of a reset, without code downloading from the flash. If unused, this signal must be tied LOW.
PLLBYPASS	Input	PLL Bypass. This signal enables the on-chip PLL. When PLLBYPASS is HIGH, the PLL is bypassed, and the processor uses CLKIN as the clock source. When PLLBYPASS is LOW, SCT3258 uses the PLL output as the processor clock source. During normal operation, the level of PLLBYPASS must remain constant.
PLLSEL2	Input	PLL Multiplier Select. This signal sets the value of the PLL multiplier, as shown in Table 9-1. During normal operation, the level of PLLSEL2 must remain constant.
RSTN	Input	Device Reset. This signal starts SCT3258 reset process. After the initial

| | | power-up sequence, RSTN must be asserted (LOW) for a minimum of five processor clock cycles to guarantee proper reset of the device. The LOW-to-HIGH transition of this signal causes the processor to download boot loader from the HPI interface and begin execution. |

Table 10-1 SCT3258 System Interface Signals

10.2 Programmable I/O (PIO)

The SCT3258 provides four programmable I/O signals, PIO[3:0]，for general-purpose hardware interfacing. Each of these signals can be individually configured as input or output. The memory-mapped PIO register controls the behavior of these signals.

The SCT3258 preloaded firmware has assigned the PIO with the following functions:

PIO Number	Input/Output	Descriptions
PIO 0 I2C_CLK	Output	SCK, clock signal for I^2C interface
PIO 1 I2C_DATA	Input/Output	SDA, data line for I^2C interface, also as mode PIN for HPI mode select during reset: 0 for Intel Mode and 1 for Motorola Mode
PIO 2	Output	Output signal for resetting external vocoder, e.g. AMBE3000 for SCT3258.
PIO 3 RF_TIMING	Output	"60 ms slot timing, aligned with transmitted or received signals. High level corresponds to slot 1, low level corresponds to slot 2.

Table 10-2 Programmable IO Signals

10.3 Power Management

This section describes the power management features of the SCT3258.

The SCT3258 employs four levels of operations: normal, idle, sleep and halt mode. Table 10-3 summarizes the four modes. In addition, the HPI can be put to sleep separately.

Power level	Description
Normal	All units and clocks active
Idle	DSP device inactive, peripherals active. Any enabled interrupt, NMI, or reset wakes device. PLL retains lock.
Sleep	System clock and peripherals inactive. Any enabled external interrupt (INT0), NMI, or reset wakes device. PLL retains lock.
Halt	System clock and peripheral is inactive. Only NMI or reset wakes device. PLL retains lock.

Table 10-3 SCT3258 Power Levels

In normal mode and all power saving modes, PLL remains locked, which reduces the latency of

returning to full-speed operation. While in any power saving modes, memory and register contents remain intact.

10.3.1 Normal Mode

In normal mode, the processor executes at full speed and all peripherals are active.

10.3.2 Idle Mode

In idle mode, the processor clock is halted, but the I/O clock continues to run. When an interrupt occurs and is serviced, execution begins with the next instruction following the idle instruction.

The host can set SCT3258 into IDLE mode by using HPI command CHIP_LOW_PWR, with Low Power Mode 4. To return to normal mode, the host can send command CHIP_LOW_PWR with Low Power Mode 0. Details can be found in "SCT3258 Packet Interface".

10.3.3 Sleep Mode

In sleep mode, the processor clock and all I/O activity stop. After INT0 or NMI occurs and is serviced, execution resumes with the instruction following the Sleep instruction.

The host can set SCT3258 into SLEEP mode by using HPI command CHIP_LOW_PWR, with Low Power Mode 5. To return to normal mode, the host need to sends an external INT0 interrupt to SCT3258, and then sends command CHIP_LOW_PWR with Low Power Mode 0. Details can be found in "SCT3258 Packet Interface".

10.3.4 Halt Mode

In halt mode, the processor clock and all I/O activity stop. While halted, memory and register contents remain intact, but previous program execution cannot resume. If an NMI wakes up the device from halt mode, a full software reset of SCT3258 is performed without re-downloading the firmware.

The host can set SCT3258 into HALT mode by using HPI command CHIP_LOW_PWR, with Low Power Mode 6. Details can be found in "SCT3258 Packet Interface".

11 Packet Interface

Packet interface is defined above the physical interface (HPI, Serial Port) for communications between SCT3258 and the host MCU. The packet format is identical regardless of physical interfaces. Packet details are defined in a separate document: "SCT3258 Packet Interface".

12 Operation and Timing

This chapter provides timing information for SCT3258 operation. It contains the following sections:

· Section 12.1, "Processor Initialization and Normal operation settings"
· Section 12.2, "Reset and power-on Timing"
· Section 12.3, "Interrupt Timing"
· Section 12.4, "Programmable I/O Timing"
· Section 12.5, "Serial Port Timing"
· Section 12.6, "Host Processor Interface (HPI) Timing"

12.1 Processor Initialization and Normal Operation Settings

The SCT3258 requires a 1.2 V supply for the DSP core and a 2.5-3.3 V supply for the I/O ports. The DSP core power supply should be applied first before the I/O power supply.

During power-up and normal operation, the SCT3258 requires holding some signals at a constant logic level to ensure proper operation while the input clock is applied. Table 12-1 lists the signals and the required logic levels. For information that illustrates the timing for these signals, refer to Section 12.2, "Reset and Power-on Timing".

Signal	Initialization Logic Level	Normal Operation Logic Level
PLLBYPASS	LOW if using on-chip PLL; HIGH if bypassing on-chip PLL	
PLLSEL2	Appropriate multiplier value if using on-chip PLL.	
RSTN	LOW for at least 500 ms after first rising input clock edge; can dessert after 500ms.	HIGH
PIO1	LOW if Intel Mode; HIGH if Motorola Mode	-

Table 12-1 Initialization and Normal Operation Logic Levels

12.2 Reset and Power-On Timing

Figure 12-1 shows the power-on timing sequence for the SCT3258 with the PLL enabled. Table 12-2 describes the relationships in Figure 12-1. DSP should be powered on before I/O is applied.
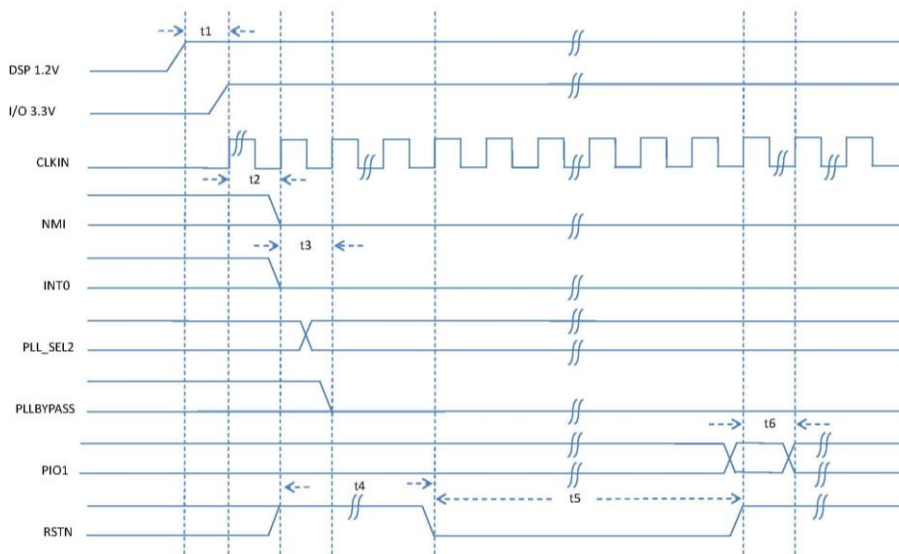

Figure 12-1 Reset / Power-on Timing-PLL Enabled

Reference	Description	Min	Max	Unit
t1	Valid DSP to Valid I/O	0	—	ms
t2	Invalid to Valid Clock	—	—	ms
t3	After Clock Valid to BYPASS Active Low	—	—	ms
t4	RSTN HIGH Width	30	—	ms
t5	RSTN LOW Width	500	—	ms
t6	PIO1 Valid Hold Time	2T		ms

1. T= processor clock period

Table 12-2 Reset / Power-on Timing Values

12.3 Interrupt Timing

External interrupts are edge-triggered and asynchronous. A sampled LOW-to-HIGH transition constitutes a valid interrupt. Figure 12-2 shows external interrupt timing relative to the processor clock. Table 12-3 describes the timing relationships in Figure 12-2.
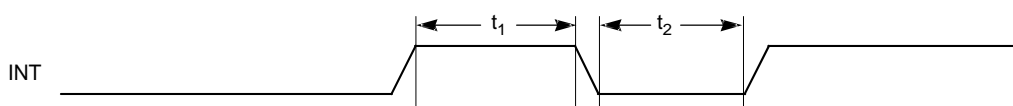

Figure 12-2 Interrupt Timing

Reference	Description	Min	Max	Unit
t1	Interrupt HIGH Pulse Width	T	—	ns
t2	Interrupt LOW Pulse Width	T	—	ns

T=processor clock period

Table 12-3 Interrupt Timing Values

12.4 Programmable I/O Timing

The SCT3258 supports 4 external programmable I/O signals.

Figure 12-3 shows programmable I/O timing relative to the processor clock. Table 12-4 describes the timing relationships in Figure 12-3.
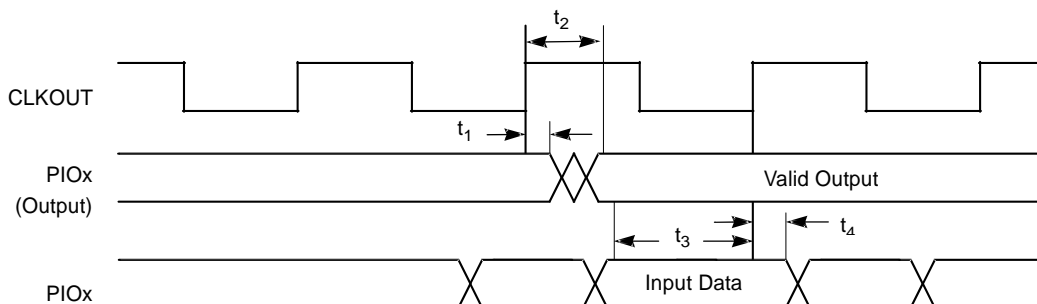

Figure 12-3 Programmable I/O Timing

Reference	Description	Min	Max	Unit
t1	PIOx Output Data Hold Time (HIGH to Invalid)	1	—	ns
t2	PIOx Output Data Delay Time (HIGH to Valid)	—	2	ns
t3	PIOx Input Data Setup Time (Valid to HIGH)	4	—	ns
t4	PIOx Input Data Hold Time (HIGH to Invalid)	0	—	ns

Table 12-4 Programmable I/O Timing values

12.5 Serial Port Timing

The two serial ports in the SCT3258 are identical. But serial ports 0 is pre-configured to work with internal flash, and serial port 1 is pre-configured to work with an external codec.

12.5.1 Connection with External Codec

Serial port 1 is pre-configured to connect to an external codec (e.g, TLV320AIC3204 from TI or WM8758B from Wolfson). In this connection, the external codec provides the clock and frame sync signal. For SCT3258, S1XCLK and S1XFS are both input signals. The serial connection is configured to have the following characteristics.

Sampling Rate	24 kHz
BCLK Rate	768 kHz
Number of time slots	2 (Stereo)
Format	PCM
Number of Bit Per Channel	16
MSB or LSB first	MSB
Frame Sync required for each transfer	Yes

XCLK direction	Input
XFS direction	Input
Level/Edge sensitive	Edge Sensitive
Positive Edge/Negative Edge frame sync	Positive
Number of cycles frames sync is ahead of Data	1

12.5.1.1 Transmit Timing

Figure 12-4 shows the timing waveforms for advance transmit frame sync field (axfs) set to 0b10 (frame sync is one clock cycle before the data bit), used when SCT3258 is connected to an external codec. Table 12-5 shows the timing relations for the signals in the figure.

In Figure 12-4, XFS becomes valid on a rising edge of XCLK, and DO becomes valid on the next rising edge of XCLK.
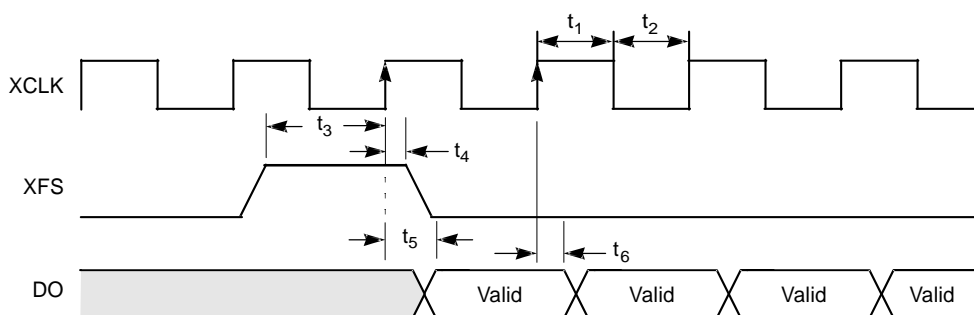

Figure 12-4 Serial Port Transmit Timing for External Codec Connection

Symbol	Parameter	Min	Max	Unit
t1	Clock HIGH	1	—	Processor Clock Periods
t2	Clock LOW	1	—	
t3	XFS Setup Time	4	—	ns
t4	XFS Hold Time	1	—	
t5	Data Out(Do)Propagation Delay	1	4	
t6	Data Out(Do)Hold Time	1	—	

Table 12-5 Serial Port Transmit Timing Values (XCLK and XFS as Inputs)

12.5.1.2 Receive Timing

In codec connection, the serial port receive clock and receive frame sync signals are input signals.

In Figure 12-5, RFS is valid on a failing edge of RCLK, and DI becomes valid on the next falling edge of RCLK. This mode is used when SCT3258 is connected to the external codec chip.
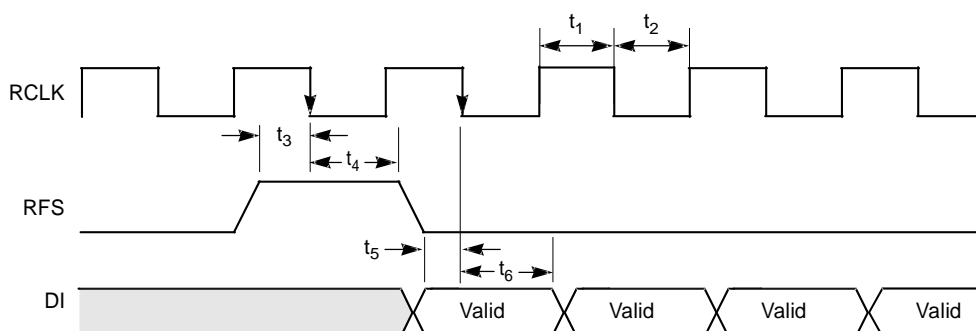

Figure 12-5 Serial Port Receive Timing for External Codec Connection

Symbol	Parameter	Min	Max	Unit
t1	Clock HIGH	1	—	Processor Clock Periods
t2	Clock LOW	1	—	
t3	XFS Setup Time	4	—	ns
t4	XFS Hold Time	1	—	
t5	Data in setup time	4	—	
t6	Data in Hold Time	1	—	

RCLK must maintain a 50% duty cycle

Table 12-6 Serial Port Receive Timing Values

12.5.2   Connection with External Vocoder

Serial port 0 is pre-configured to connect to an external vocoder (AMBE3000 from DVSI). In this connection, the SCT3258 provides the clock and frame sync signal when transmitting (S1XCLK and S1XFS are both output signals). The serial connection is configured to have the following characteristics.

Sampling Rate	115.2 kHz
BCLK Rate	921.6 kHz
Number of time slots	1 (Mono)
Format	PCM
Number of Bit Per Channel	8
MSB or LSB first	MSB
Frame Sync required for each transfer	Yes
XCLK direction	Output
XFS direction	Output
Level/Edge sensitive	Edge Sensitive
Positive Edge/Negative Edge frame sync	Positive
Number of cycles frames sync is ahead of Data	0

12.5.2.1 Transmit Timing

Figure 12-10 shows transmit timing waveforms for the advance frame sync field (afxs) set to 0b00 (frame sync align with the first data bit), used when SCT3258 is connected to AMBE3000. Table

12-7 shows the timing relations for the signals in the figure. In this connection XCLK and XFS are all output signals.
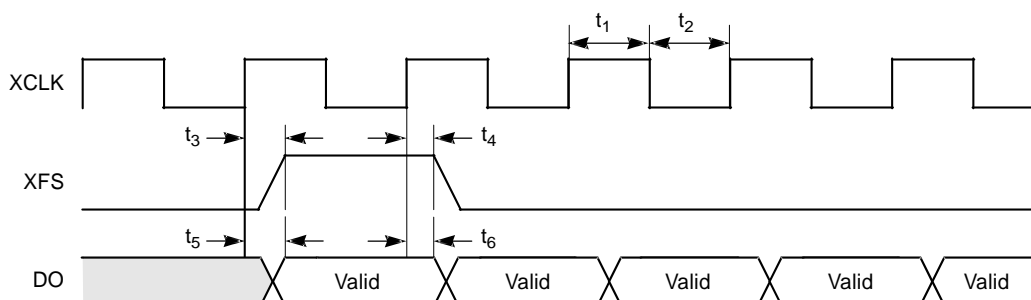

Figure 12-6 Serial Port Transmit Timing for with AMBE3000 Connection

Symbol	Parameter	Min	Max	Unit
T1	Clock HIGH	1	—	Processor Clock Periods
T2	Clock LOW	1	—	
T3	XFS Propagation Delay	1	4	ns
T4	XFS Propagation Delay	1	—	
T5	Data Out Propagation Delay	1	4	ns
T6	Data Out Hold Time	1	—	

Table 12-7 Serial Port Transmit Timing Values

12.5.2.2 Receive Timing

In AMBE3000 connection, the serial port receive clock and receive frame sync signals are input signals.

In Figure 12-10, RFS and DI are valid on the same failing edge of RCLK. This mode is used when SCT3258 is connected with AMBE3000.
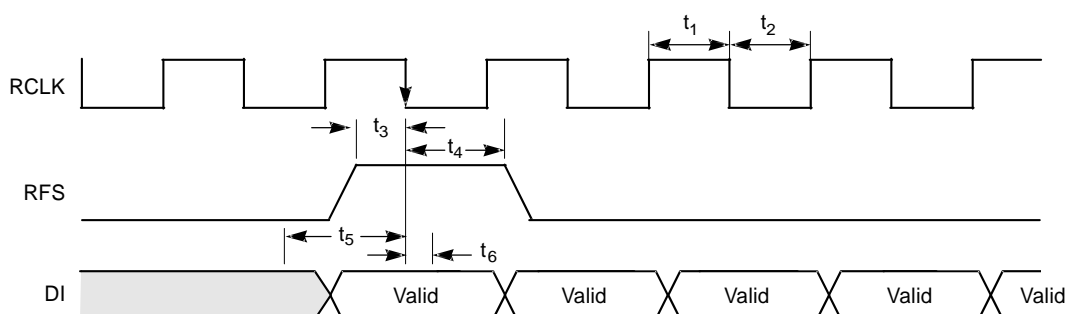

Figure 12-7 Serial Port Receive Timing for AMBE3000 Connection

Symbol	Parameter	Min	Max	Unit
t1	Clock HIGH	1	—	Processor Clock Periods
t2	Clock LOW	1	—	

t3	XFS Setup Time	4	—	ns
t4	XFS Hold Time	1	—	
t5	Data in setup time	4	—	
t6	Data in Hold Time	1	—	

RCLK must maintain a 50% duty cycle

Table 12-8 Serial Port Receive Timing Values

12.6 Host Processor Interface (HPI) Timing

The host processor interface operates in either Intel mode (for Intel-style memory interfaces) or Motorola mode (for Motorola-style memory interfaces). This section includes transmit and receive waveforms for both the Intel modes and the Motorola mode.

The maximum sustained throughput rate is one read cycle every three processor clock. The read signal must have a 50% duty cycle to achieve this rate. Write behavior is similar to read. The maximum rate is one write cycle for every three processor clock. To attain these read/write rates, the internal FIFO must be filled and emptied at the same rate.

Figure 12-10 illustrates the relationship between the processor clock and a read/write cycle.
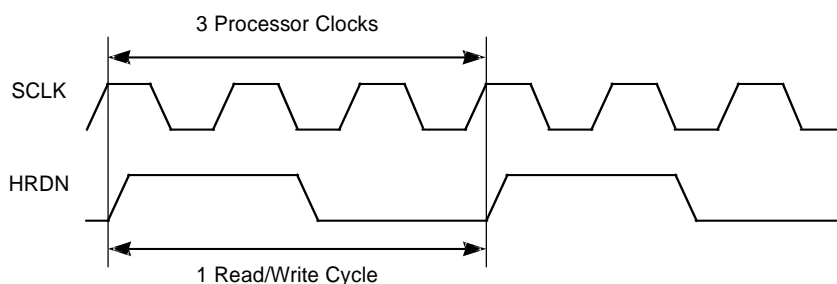

Figure 12-8 Maximum Sustained Read/Write Rates

12.6.1 Intel Mode Reads

In Intel mode, the HCSN and HRDN signals must both be asserted to perform a host read. The read begins when both signals are asserted (go LOW), and the read ends when either HCSN or HRDN is deasserted (goes HIGH). through Figure 12-10 illustrates host reads initiated and completed by HRDN. Table 12-9 describes the timing relationships for the respective illustrations.
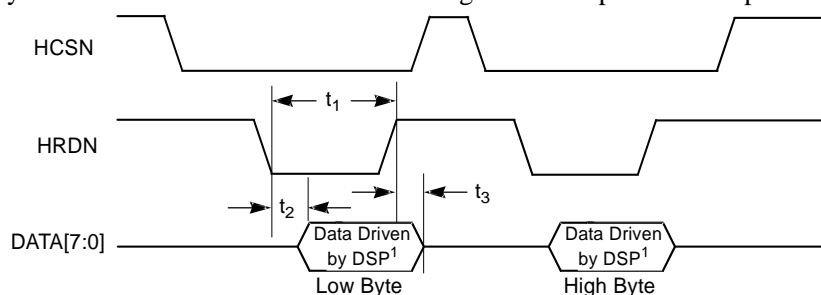

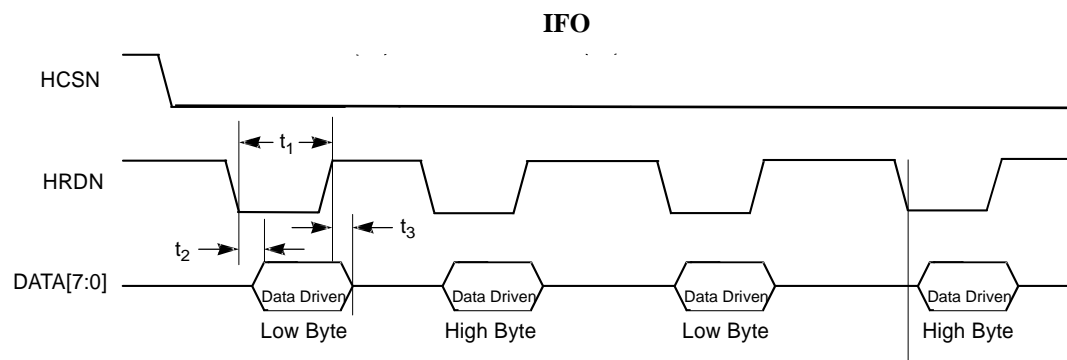**Figure 12-9 Intel Mode 16-Bit Read Timing –One or More Item in FIFO**

IFO

Figure 12-10 Intel Mode Two 16-Bit Read Timing –Two Items in FIFO

Reference	Description	Min	Max	Unit
t1	Read pulse width	1.5T	—	ns
t2	Read data delay time(LOW to Valid)	—	2.5	ns
t3	Read data hold time(HIGH to invalid)	2.5	—	ns

T=processor clock period

Table 12-9 Intel Mode 16 Bit Read Timing Values

12.6.2　Intel Mode Writes

In Intel mode, the HCSN and HWRN signals must both be asserted to perform a host write. The write begins when both signals are asserted (go LOW). The write ends when either HCSN or HWRN is deasserted (goes HIGH). Figure 12-11 through Figure 12-13 illustrate a host write initiated and completed by HWRN. Table 12-10 specifies the timing relationship in the respective figures.
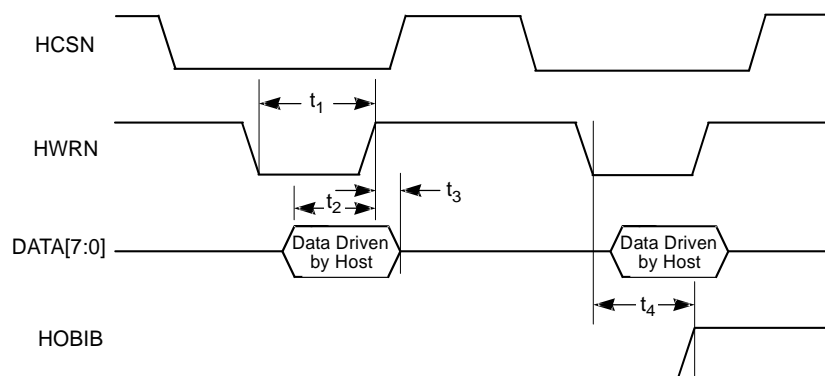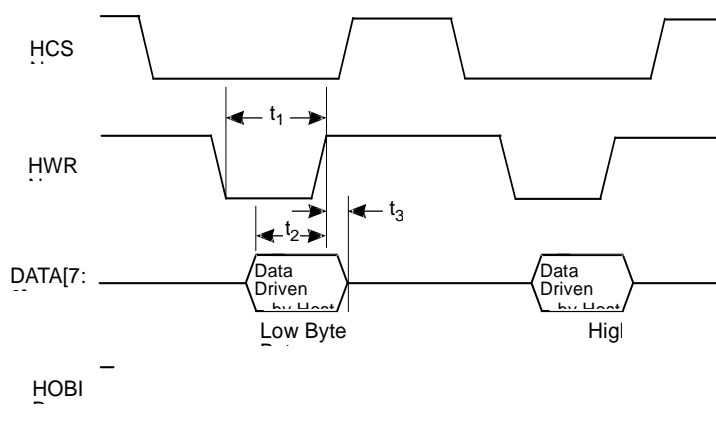

Figure 12-11 Intel Mode 16-Bit Write Timing –One space in FIFO

Note : HOBIB stays LOW because the Input Buffer is not full.

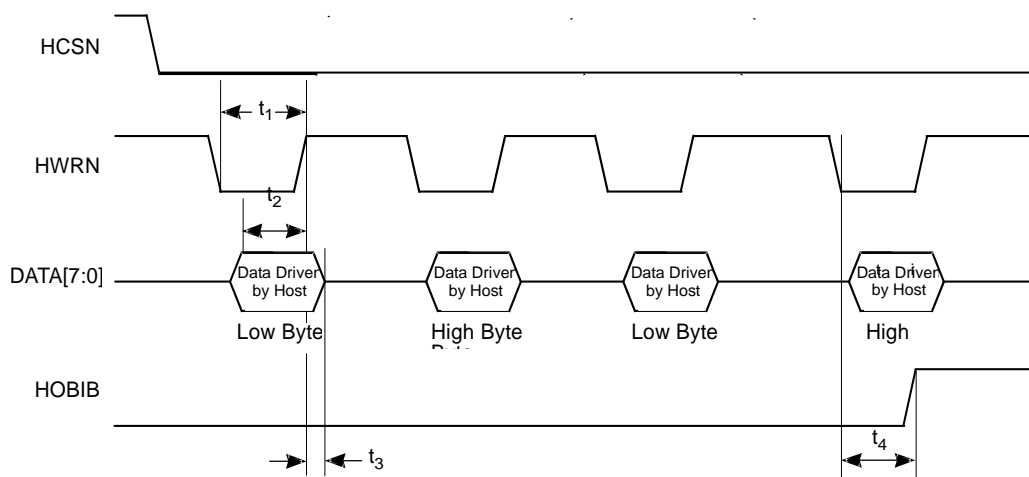**Figure 12-12 Intel Mode 16-Bit Write Timing –More than one space in FIFO**

Figure 12-13 Intel Mode 16-Bit Write Timing –Two spaces in FIFO

Reference	Description	Min	Max	Unit
t1	Write pulse width	1.5T	—	Ns
t2	Write data setup time	2.5	—	Ns
t3	Write data hold time	2.5	—	Ns
t4	ISF delay time for last item in FIFO	2.5	6.5	Ns

T=processor clock period

Table 12-10 Intel Mode 16 Bit Write Timing Values

12.6.3   Motorola Mode Reads

In Motorola mode, the HRDN signal operates as a data strobe for both reads and writes. The HWRN signal determines the data direction. For reads, HWRN must be HIGH. The HCSN and HRDN signals must both be asserted to perform a host read. The read begins when both signals are asserted (go LOW); the read ends when either HCSN or HRDN is deasserted (goes HIGH).

Figure 12-14 through Figure 12-15 illustrate a host read initiated and completed by $\overline{\text{HRDN}}$. Table 12-11 specifies the timing relationship in the respective figures.
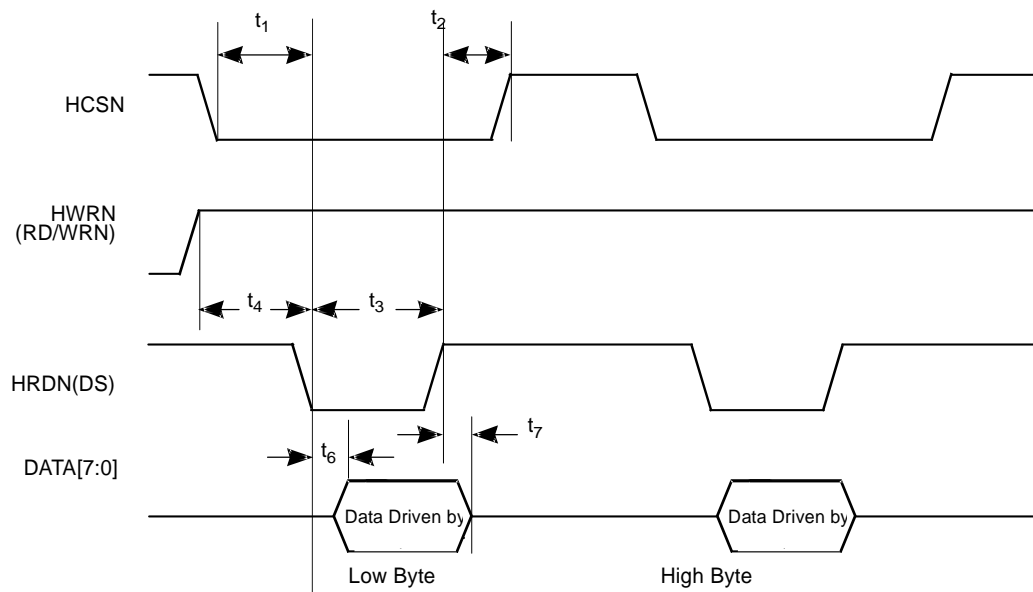

Figure 12-14 Motorola Mode 16-Bit Read Timing –One or More Items in Output FIFO
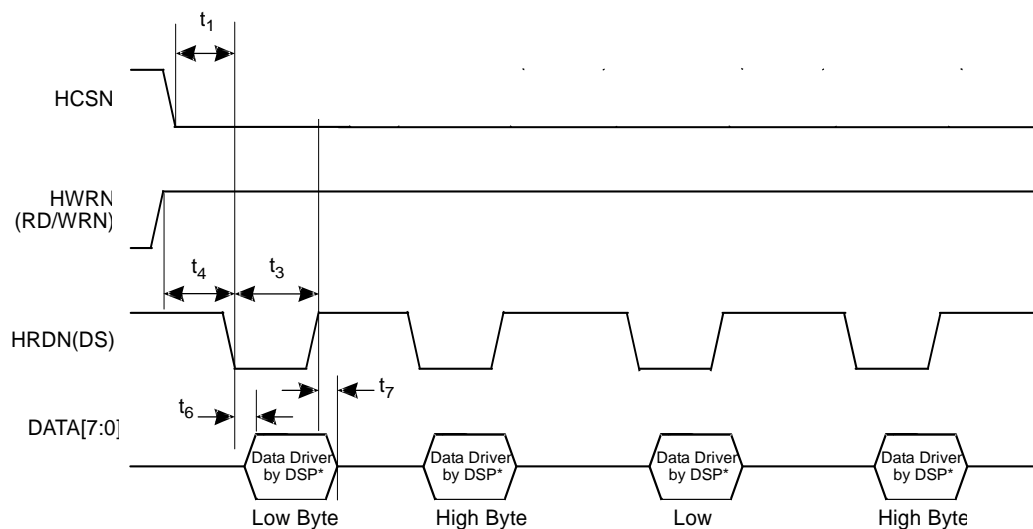
Figure 12-15 Motorola Mode Two 16-Bit Read Timing –Two Item in Output FIFO

Reference	Description	Min	Max	Unit
t1	HCSN to DS setup time(LOW to LOW)	0.5	—	ns
t3	DS pulse width	1.5T	—	ns
t4	RD/WRN to DS setup time(HIGH to LOW)	T	—	ns
t5	DS to RD/WRN hold time	0	—	ns
t6	Read data delay (LOW to valid)	—	2.5	ns
t7	Read data hold(HIGH to invalid)	0	—	ns
t8	HOBE delay time	2.5	6.5	ns

T=processor clock period

48

t5 is not shown in the Figures

Table 12-11 Motorola Mode 16 Bit Read Timing Values

12.6.4   Motorola Mode Writes

In Motorola mode, the HRDN signal operates as a data strobe for both reads and writes. The HWRN signal determines the data direction. For writes, HWRN must be LOW. The HCSN and HRDN signals must both be asserted to perform a host write. The write begins when both signals have been asserted. The write ends when either HCSN or HRDN is deasserted. Figure 12-16 through Figure 12-18 illustrate a host write initiated and completed by HRDN. Table 12-12 specifies the timing relationships in the respective figures.

Figure 12-16 Motorola Mode 16-Bit Write Timing –One space in FIFO

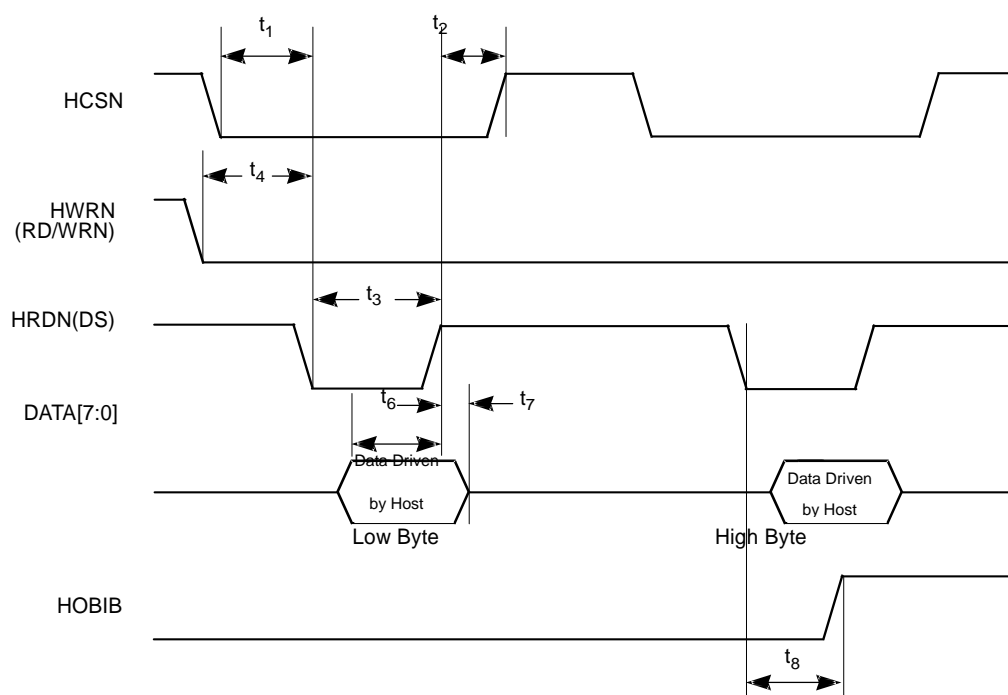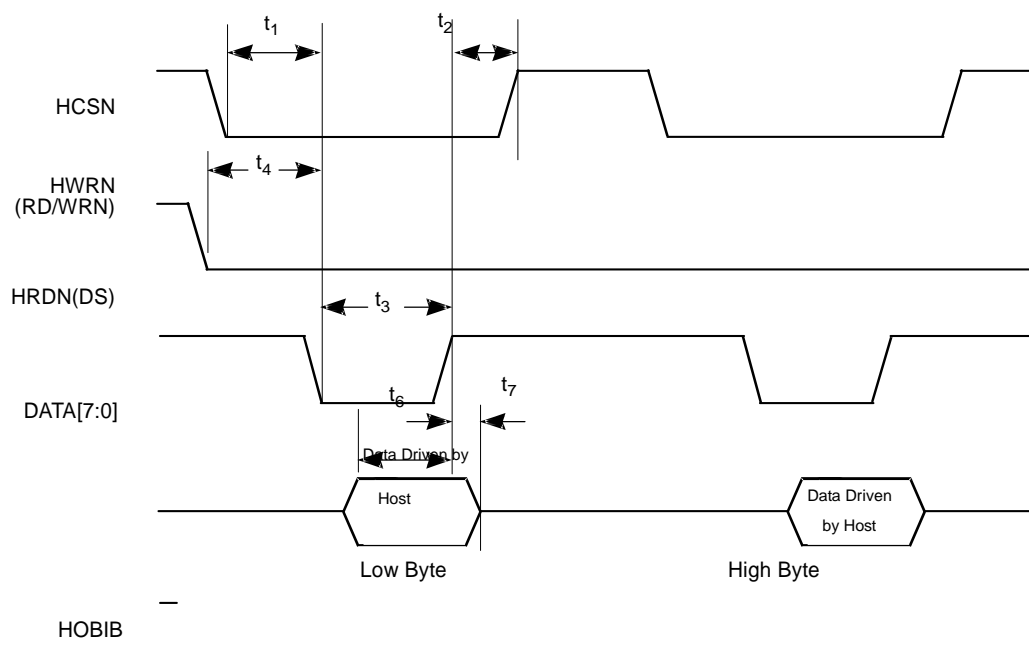Note : HOBIB stays LOW because the Input Buffer is not full.

Figure 12-17 Motorola Mode 16-Bit Write Timing –More than one space in FIFO
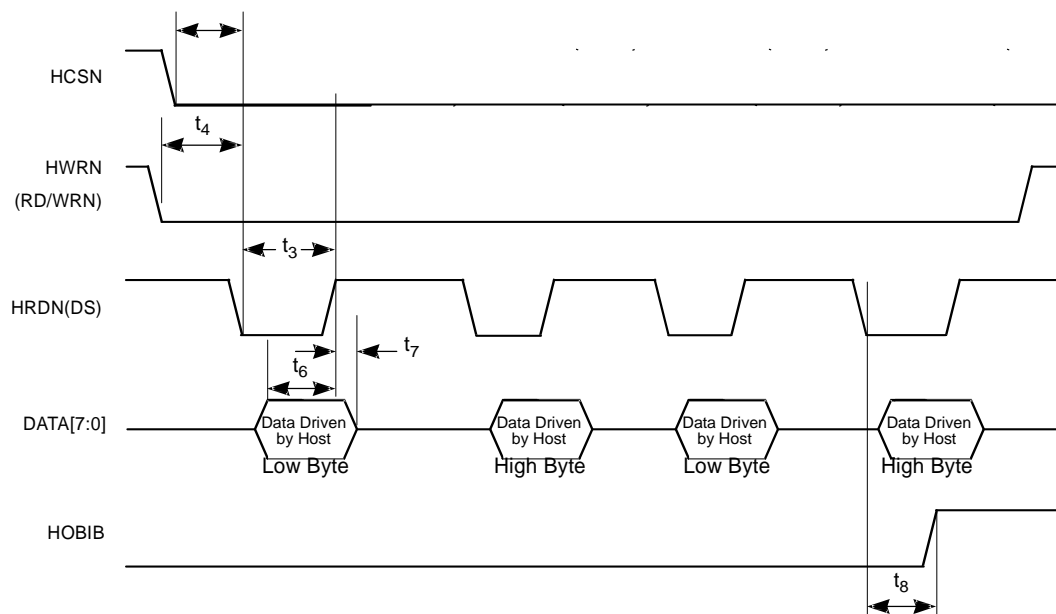
Figure 12-18 Motorola Mode Two 16-Bit Write Timing – Two space in FIFO

Reference	Description	Min	Max	Unit
T1	HCSN to DS setup time(LOW to LOW)	0.5	—	ns
T3	DS pulse width	1.5T	—	ns
T4	RD/WRN to DS setup time(LOW to LOW)	T	—	ns
T5	DS to RD/WRN hold time	0	—	ns
T6	Read data delay (valid to HIGH)	2.5	—	ns
T7	Read data hold(HIGH to invalid)	0	—	ns

| T8 | HOBIB delay time | 2.5 | 6.5 | ns |

1. T=processor clock period

2. t5 is not shown in the Figures

Table 12-12 Motorola Mode 16 Bit Write Timing Values

13   Specifications

13.1 DC Characteristics

Table 13-1 lists the DC characteristics for the SCT3258.

Parameter	Symbol	V_{DD2}=1.2V, PLLVDD=1.2V, V_{DDIO}=2.5-3.3V	
		Minimum	Maximum
Input Voltage Low	V_{IL}	0V	0.8V
Input Voltage High (2.8V I/O Supply)	V_{IH}	2.0V	5.5V
Input Current	I_{IN}	-10uA	10uA
PLL Input Voltage Low	VPLL$_{IL}$	VSS	0.24V
PLL Input Voltage High	VPLL$_{IH}$	0.96V	VDD2
Output LOW Voltage @+2mA(LOW)	V_{OL}	—	0.4
Output High Voltage@-2mA	V_{OH}	2.4	—
Output 3-State Current Low	L_{OZL}	-10uA	10uA
Output 3-State Current High	L_{OZH}	-10uA	10uA

Table 13-1 DC Electrical Characteristics

13.1 Power Consumption

Table 13-2 lists the power dissipation characteristics of SCT3258. Sicomm recommends an I/O supply current rating of 200 mA or greater.

Work Mode	Frequency (MHz)	Power Voltage	Current Dissipation (Typical)
Full Duplex	110.592	1.2 V(Core)	37 mA
		3.3 V (IO)	5.3 mA
Half Duplex	61.44	1.2 V (Core)	22 mA
		3.3 V (IO)	3.3 mA
Idle	110.592	1.2 V (Core)	21 mA
		3.3 V (IO)	5.3 mA
	61.44	1.2 V (Core)	13 mA
		3.3 V (IO)	3.3 mA
	12.288	1.2 V (Core)	3.0 mA
		3.3 V (IO)	1.3 mA
Sleep/Halt	110.592	1.2 V (Core)	3.3 mA
		3.3 V (IO)	4.6 mA
	61.44	1.2 V (Core)	2.8 mA
		3.3 V (IO)	2.9 mA

	12.288	1.2 V (Core)	0.9 mA
		3.3 V (IO)	1.2 mA

Table 13-2 SCT3258 Power Dissipation

13.2 Recommended Operating Conditions

Table 13-3 lists the recommended operating conditions for SCT3258.

Parameter	Symbol	V_{DD2}=1.2V, PLLVDD=1.2V, V_{DDIO}=2.5-3.3V	
		Minimum	Maximum
Core Supply Voltage	V_{DD2}	1.1V	1.3V
PLL Supply Voltage	PLLVDD	1.1V	1.3V
I/O Supply Voltage	V_{DDIO}	2.5V	3.6V
Input Voltage	V_I	0V	V_{DDIO}
Output Voltage	V_O	0V	V_{DDIO}
CLKIN Input Voltage	Vclk	1.2 Vpp	V_{DDIO}
Ambient Temperature (Industrial Operating Conditions)	T_A	-40℃	85℃

Table 13-3 Recommended Operating Conditions

Table 13-4 lists ESD ratings for SCT3258.

CDM	HBM
500V	1000V

Table 13-4 ESD Ratings

13.3 Parametric Performance

All voltage levels given in the table below are given in relative to the full scale value of the ADC. The absolution voltage level can be calculated from the full scale voltage of the ADC. For example, with WM8758B, the full scale ADC voltage with 3.3v analog power supply is 3 Vpp. With Demod input value of -14.5 dBFS, the absolute value is around 560 mVpp.

Parameters	Notes	Minimum	Typical	Maximum	Unit
Route Trip Delay	1		150		Ms
4FSK Input	2, 3,4	-60	-14.5	-1.5	dBFS
4FSK Input Auto calibration Range	2, 3	-37.5		-5.5	dBFS
4FSK Output for VCO	2, 5	-60	-14.5	-1.5	dBFS
4FSK Output for TCXO	2, 5	-60	-14.5	-1.5	dBFS

DPMR Call Match report time with Header Frame	6	75		120	milliseconds
DPMR Call Match report time with Late Entry Time	6	260		520	milliseconds
DPMR Sensitivity Gain over analog call	7		2	3	dB
DMR Call Match report time with FLC Data Frame	6		80		milliseconds
DMR Call Match report time with Late Entry Time	6	380		740	milliseconds
DMR Sensitivity Gain over analog call	7		2	3	dB

Table 13-5 Parametric Performance

1). Route trip delay includes algorithm delays (for vocoders) and buffer delays.

2). Obtained when +3, -3 symbols are transmitted or received,

3). When the analog and digital gain of the ADC are all set to 0 dB.

4). When the analog and digital gain of the ADC are all set to 0 dB. Auto calibration is enabled when DIGI_DEMOD_GAIN = 0;

5). When the analog and digital gain of the DAC are all set to 0 dB. Typical Value are obtained when MOD_GAIN=2048

6). Assume no bit error.

7). Assume 12.5 kHz channel spacing. 4FSK uses frequency deviation of 1944 Hz with +3,-3 symbol patterns. Analog sensitivity uses 12 dB SINAD. Digital Sensitivity uses 5% raw BER.

14   Application Information

The following schematic diagrams show SCT3258 used with conventional RF and with CMX994A/E .
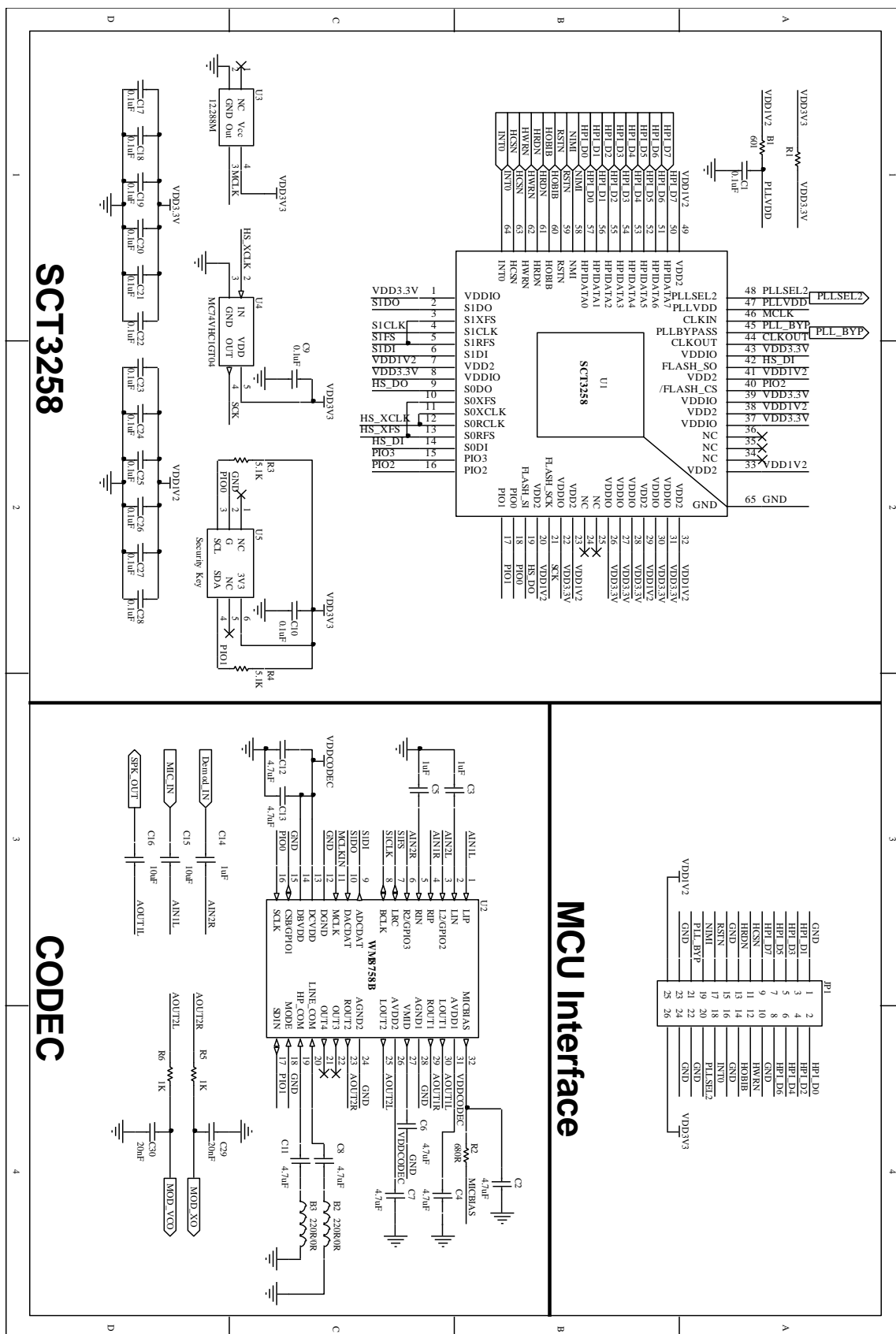
Figure 14-1　SCT3258 Application Circuits with Conventional RF and Wolfson WM8758B
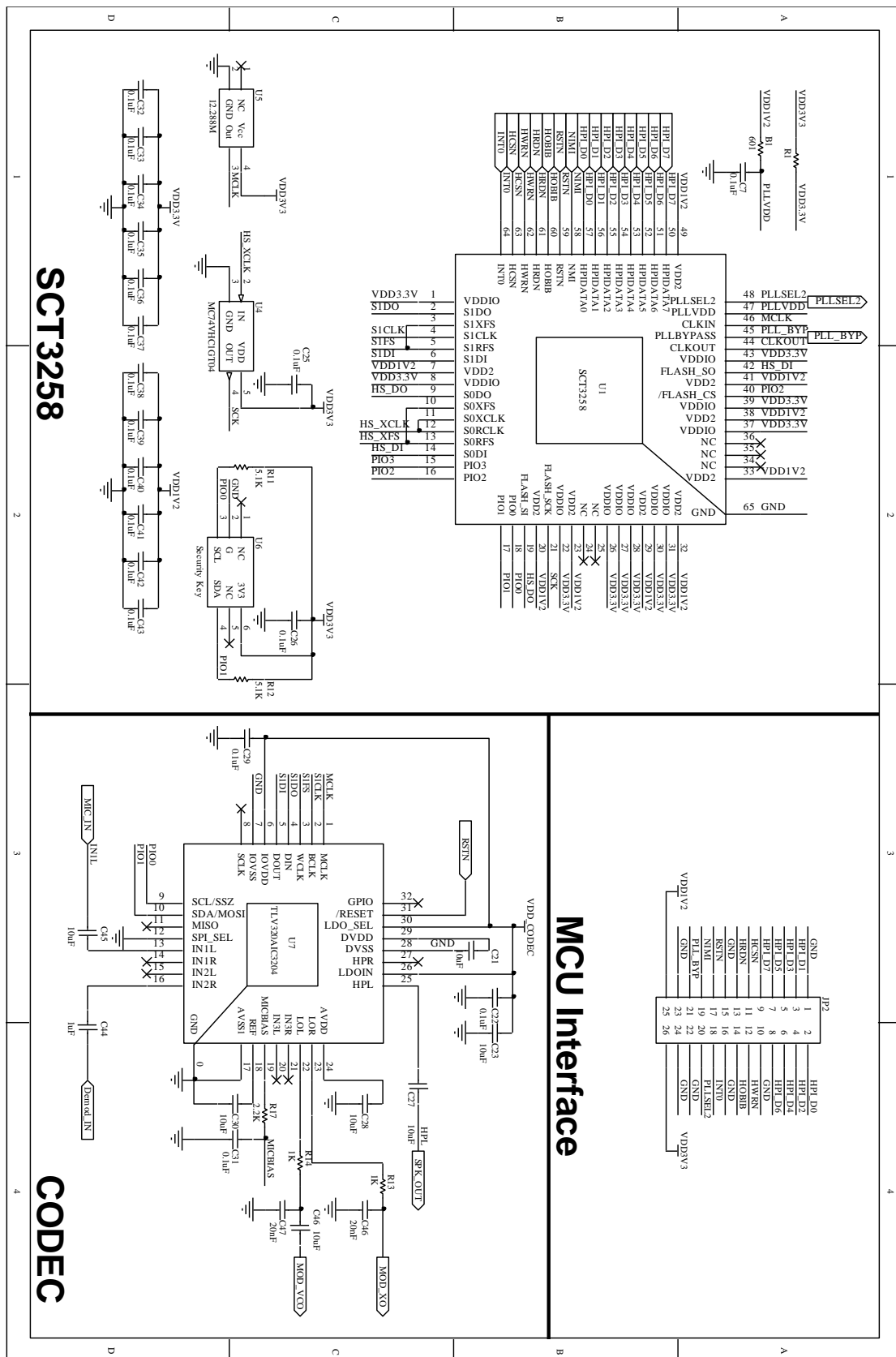
Figure 14-2　SCT3258 Application Circuits with Conventional RF and TI TLV320AIC3204
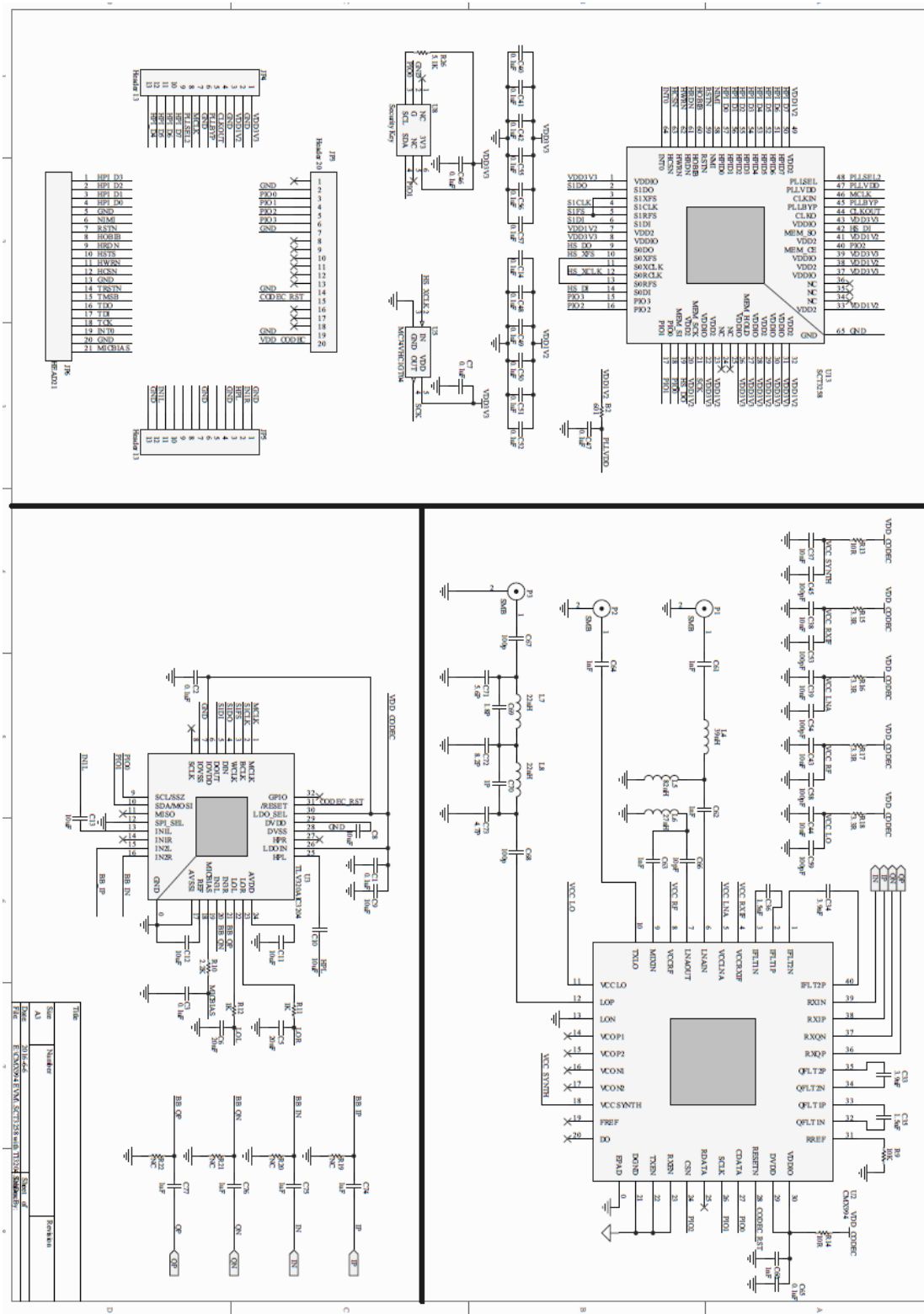
Figure 14-3   SCT3258 Application Circuits with CMX994 and TI TLV320AIC3204
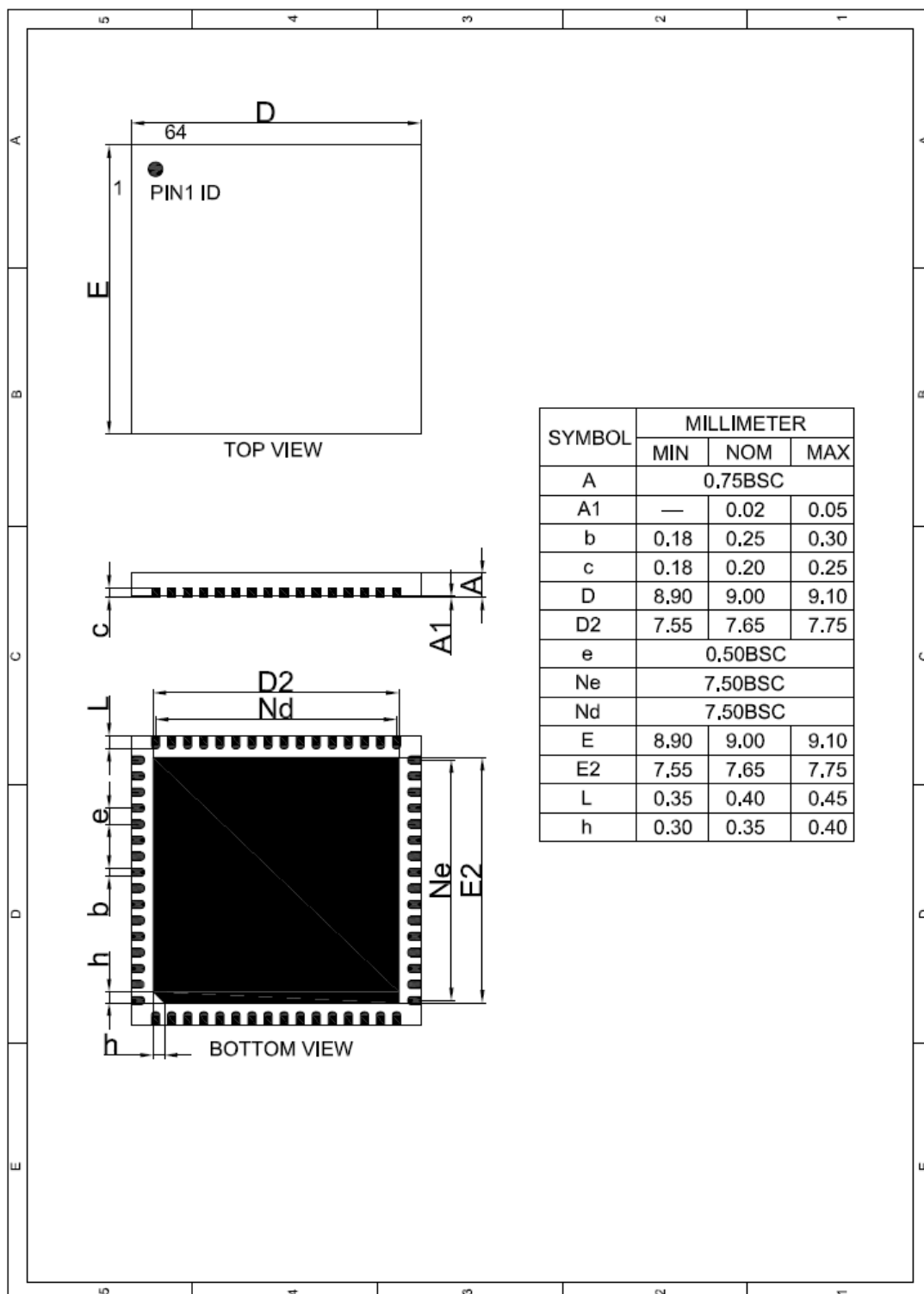
Notes

1. The security key can be omitted if ASELP vocoder is not used.

2. The decoupling capacitor for AOUT2L, (connecting to LOUT2 of WM8758B, or LOR of TLV320AIC3204), has to greater than 10 uF if AC coupling to TXCO is used. DC coupling is

recommended. DC_OFFSET configuration command can be used to match the common voltage level of the DAC and the TCXO.

3. The decoupling capacitor for AOUT1L, (connecting to LOUT1 of WM8758B, or HPL of TLV320AIC3204), has to greater than 10 uF for optimum voice quality.

4. The decoupling capacitor for AIN2R, (connecting to R2 of WM8758B or IN2R of TLV320AIC3204)) can be removed if DC coupling is used. DC_OFFSET configuration command can be used to match the common voltage level of the ADC and the FM demodulator outputs.

5. The HPI Mode Select Circuit (with 2 inverters) is used only to select HPI Intel Mode. The purpose is to keep PIO1 low at low-to-high transition of RSTN (out of reset). The same purpose can be achieved by using an MCU GPIO port, by connecting PIO1 to the GPIO port. The GPIO should be set to output low when resetting SCT3258, and then set to high impedance (or input mode) after the reset.

15 Packaging Information

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.75BSC		
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	8.90	9.00	9.10
D2	7.55	7.65	7.75
e	0.50BSC		
Ne	7.50BSC		
Nd	7.50BSC		
E	8.90	9.00	9.10
E2	7.55	7.65	7.75
L	0.35	0.40	0.45
h	0.30	0.35	0.40

Dimensions shown in millimeters

Figure 15-1   SCT3258 QFN64 Package

16   SCT3258 Naming Conventions

SCT3258 has several variations, depending on protocol, vocoder or special functions settings. As a rule, the name for different variety of SCT3258 follows the format below.

SCT3258XYZ

The means of X, Y and Z are described in the following table.   **Bold text** indicates standard supply options, for the availability of other options please refer to your local CML Sales representative http://www.cmlmicro.com/contact-cml/

X designates the protocol supported.

Value of X	Protocol Supported
P	**Support DPMR**
D	**Support DMR T2**
T	**Support both DPMR and DMR**
R	Support DPMR, support premium features including 64/192 bit encryption and analog recording/ play back

Y designates the vocoder supported.

Value of Y	Vocoder Supported
T	Tsinghua ASELP 1.6 Vocoder
U	Tsinghua ASELP 1.7 Vocoder + encryption dongle
V	Tsinghua ASELP 1.7 Vocoder (no encryption dongle)
D	**DVSI AMBE+2 Vocoder**
C	DVSI AMBE+2C Vocoder
F	Dual vocoder option, ASELP and AMBE+2C
R	ST24 Vocoder
S	F100 Vocoder
N	No vocoder option

Z designates the RF interface supported.

Value of Z	RF Interface Supported
C	**Conventional RF**
D	**CMX994A/E**

Note: The third letter, Z, can be omitted. In that case, it means Z = C, for conventional RF support.