60x Bus

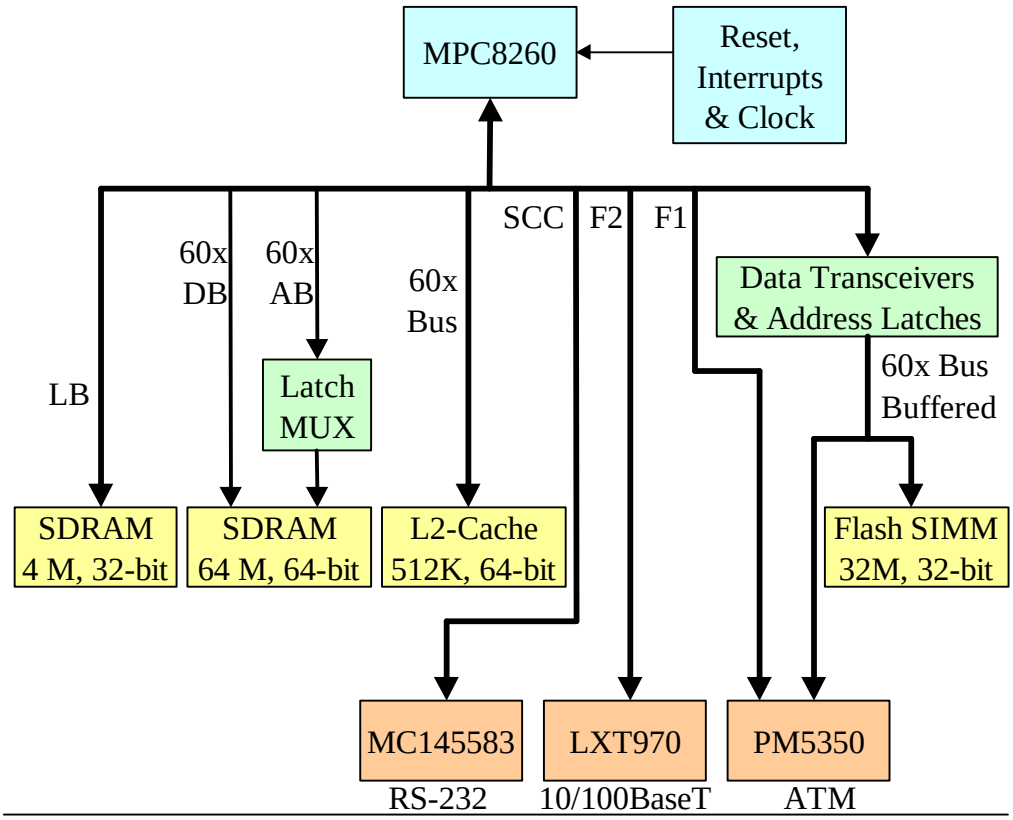
What you will learn

- What are the 60x bus pins?
- What are the 60x bus modes?
- How to Interface to a slave
- How to Interface to a bus master
- How the 60x bus is arbitrated

How to Connect an 8260 System

Introduction — The diagram below shows an example 8260 system configuration.

Example



Description

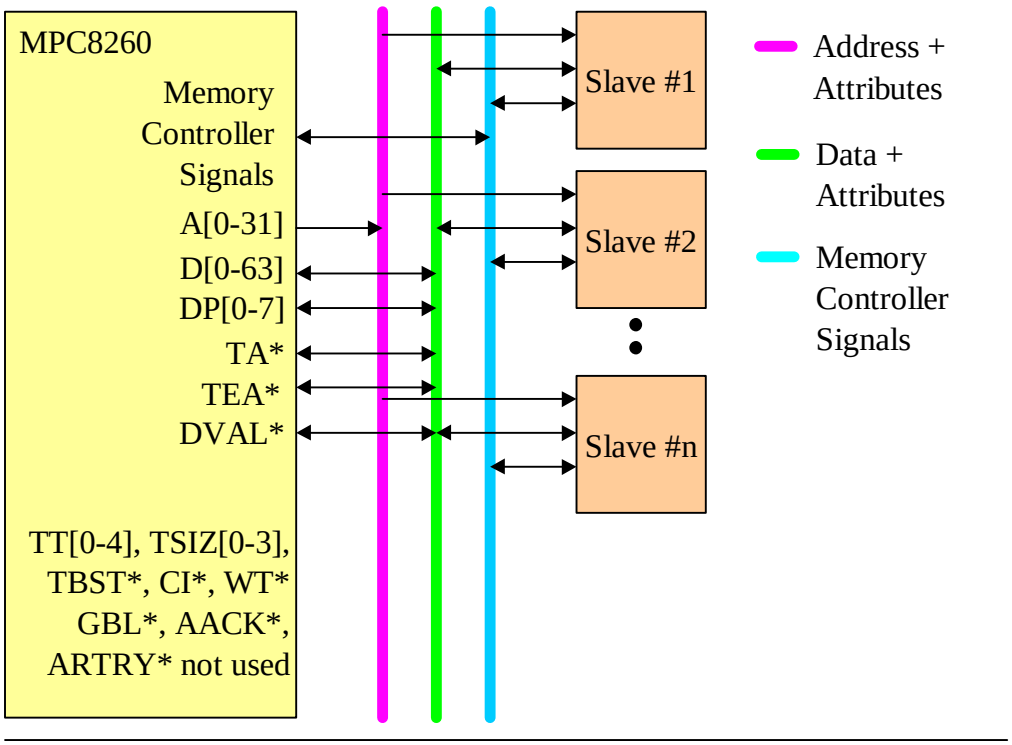
1. The SDRAM connected to 60x bus requires external latches and multiplexing because accesses can have separateaddress and data tenures in 60x bus mode. Latches and multiplexer can be by-passed if L2 cache is not used and MPC8260 is in Single mode.
2. SDRAMs and L2 cache are not buffered to maximize performance. Flash, the ATM PHY, plus other are buffered with no significant impact on performance.
3. FCC1 is ATM, FCC2 is Ethernet, and SCCs are used for RS-232.

What is the Single MPC8260 Bus Mode?

Definition

The single MPC8260 bus mode means the only bus master is the 8260. The memory controller controls all devices on the external pins.

Block Diagram



Description

- The pins shown as not used should not be used for anything.
- BCTL[0-1] are usable.

8260 Single Mode Restrictions

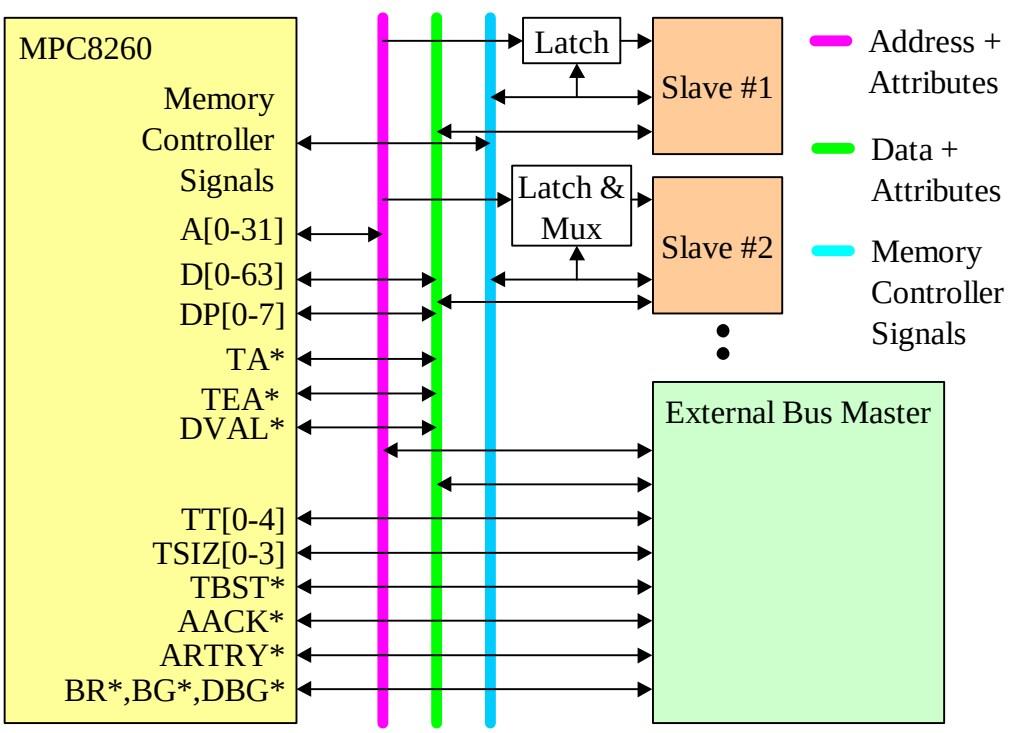
In single 8260 mode, the following is not possible:
1. No other bus masters.
2. No L2 cache.

What is the 60x Compatible Bus Mode?

Definition

The 60x-compatible bus mode can include one or more bus masters including L2 cache.

Block Diagram



Description

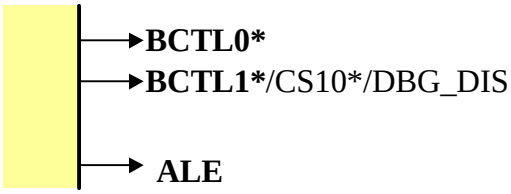
1. If the 8260 is used in no pipeline mode(BCR[PLDP]=1), the latches are not required; however, the multiplexers are. Putting the 8260 in no pipeline mode will typically result in a 10-30% performance reduction.
2. TT[0-4] indicates the transfer type. For example, a basic single-beat read is 0b01010. For a complete description of the TT codes, see page 5-10 in the UM.
3. TSIZ[0-3] and TBST* together indicate the size of the requested data transfer. For example, a transfer of 8 bytes would have TSIZ[0-3]=0000 and TBST*=1. For a complete list of transfer size encodings, see p. 5-13 in the UM.

How to Connect Address and Data Buffers

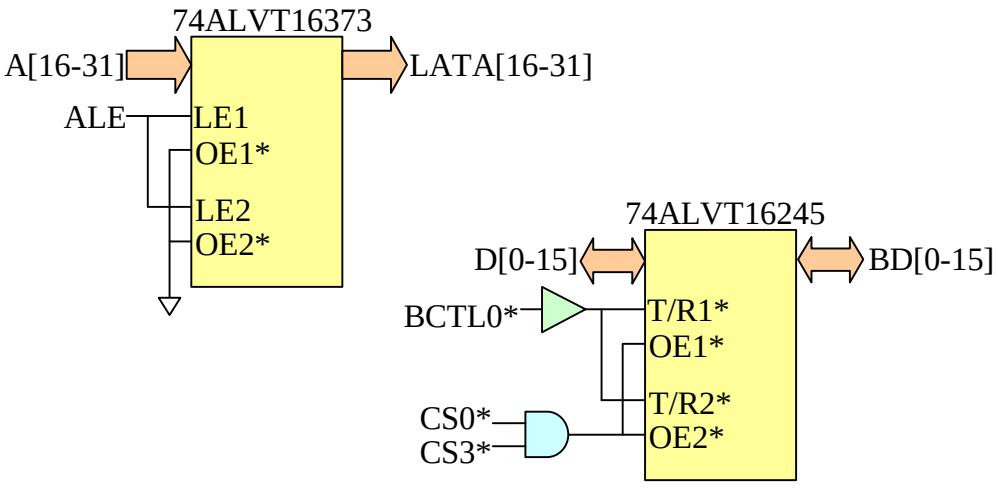
Introduction

The diagram below shows how to connect address and data buffers to the 8260.

Pin Summary



Connect Diagrams




```
pimm->SIUMCR &= 0xFFFCFFFF;
```

Description

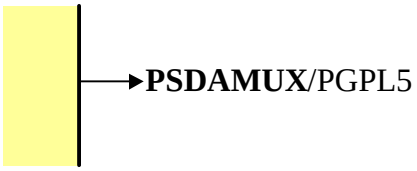
1. The pins, BCTL0 and BCTL1, can be used to control the direction of a buffer on the data bus.
2. ALE can be used to provide the latching enable input on the address latch device.

How to Multiplex Addresses Externally for SDRAM

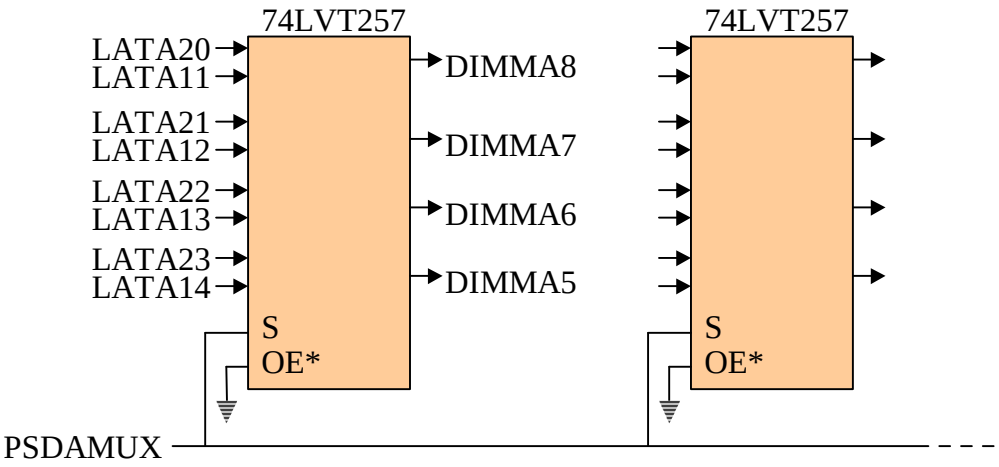
Introduction

The diagram below shows how to multiplex addresses to memory.

Pin Summary



Connect Diagrams



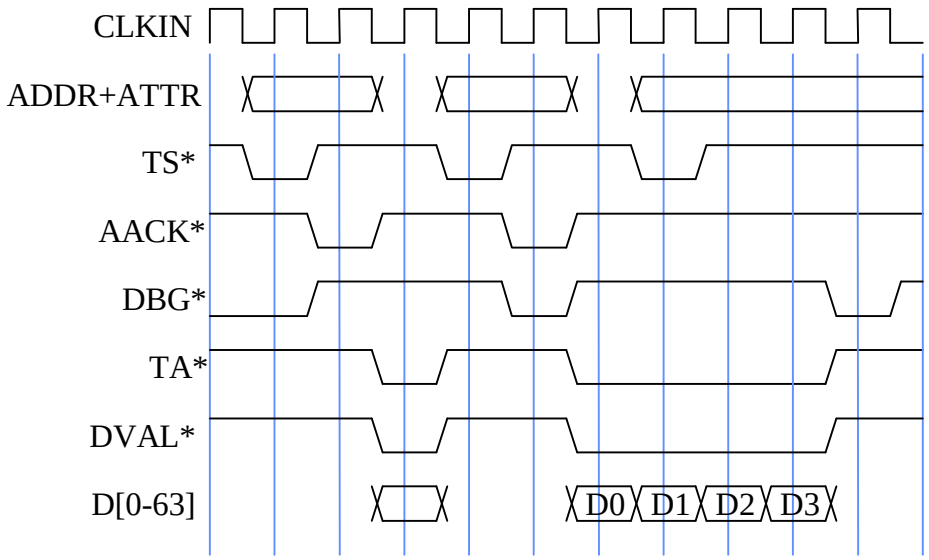
1. PSDAMUX can be the select input to an address multiplexer.

How the 8260 Transfers Single-Beat and Burst, 64-bit Data Bus

Introduction

The diagram below shows the 8260 signals for single and burst accesses.

Timing Diagram



Description

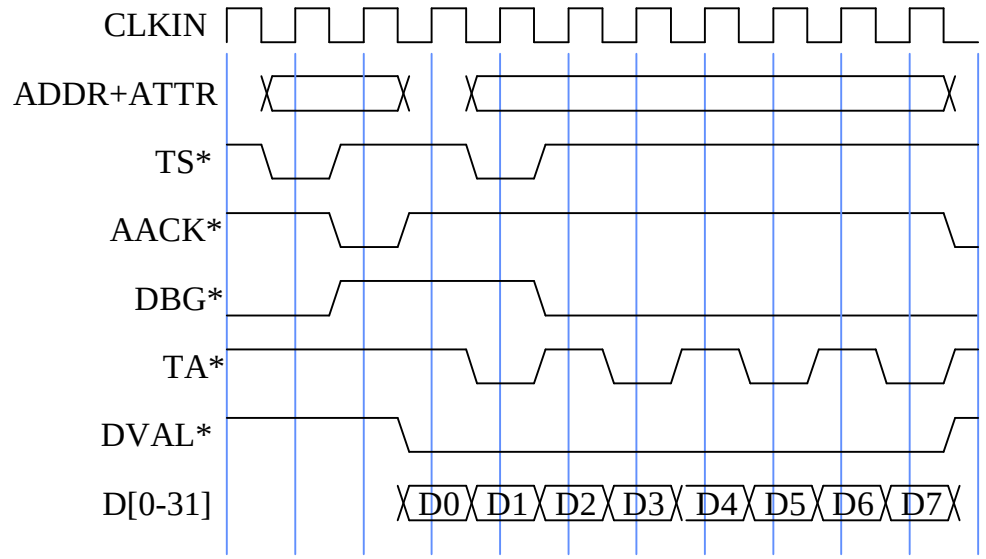
1. On a 64-bit data bus, TA* and DVAL* are the same.
2. A burst transaction is indicated by TBST*.
3. The arbiter samples TS* and TT* to determine if the processor is doing an address only cycle such as “sync.” If not, the arbiter knows the processor will need the data bus and assumes an implied data bus request. It is implied because it is not an address only cycle.

How the 8260 Transfers a Burst, 32-bit Data Bus

Introduction

The diagram below shows the 8260 signals for a burst access on a 32-bit data bus.

Timing Diagram



DVAL*/TA*

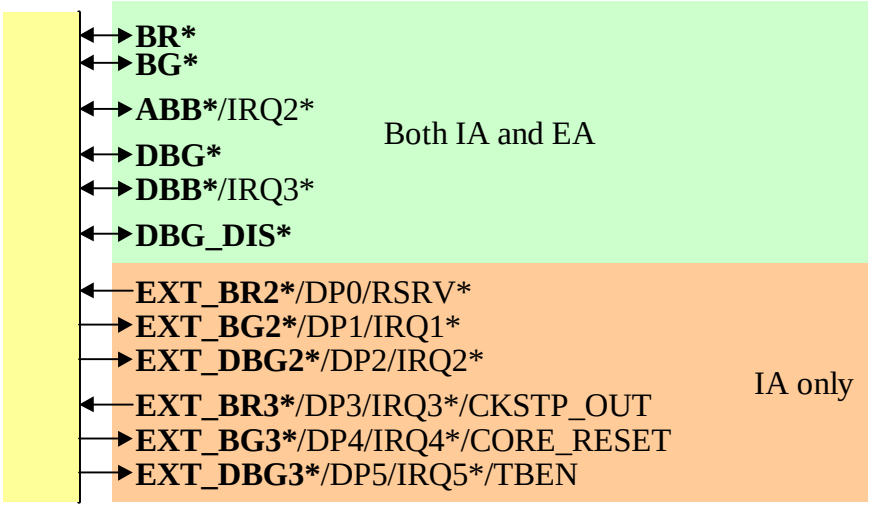
Multiple DVAL*/TA* occurs in the case of transfer width larger than port width.

What are the Bus Arbitration Pins?

Definition

The bus arbitration pins allow other bus masters to gain control of the address and data buses.

Pin Summary



IA and EA

IA = Internal Arbitration
EA = External Arbitration

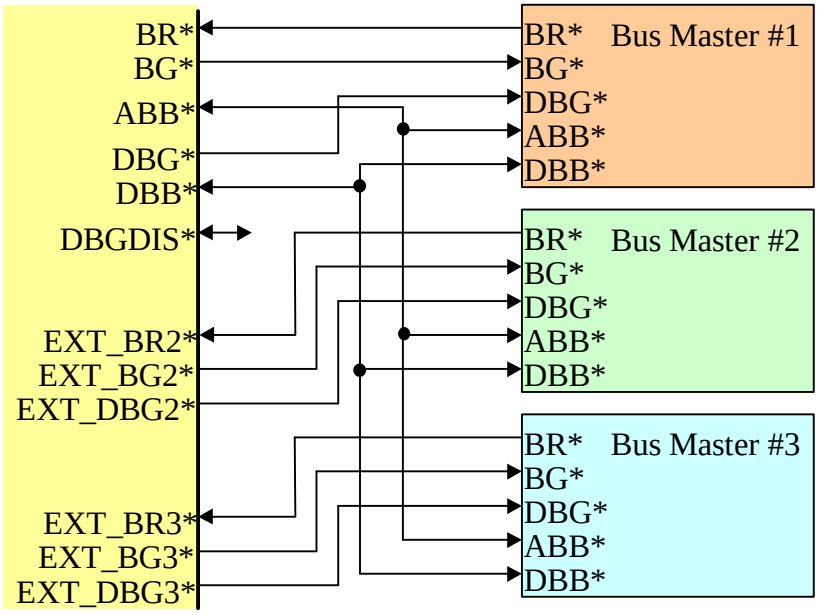
Pin	Input	Output	Description
Bus Request	IA	EA	For IA, external master asserts to request bus. For EA, 8260 asserts to request bus.
Bus Grant	EA	IA	For IA, grants address bus to external master. For EA, grants bus to 8260.
Address Bus Busy	Wants bus	Owns bus	For output, asserts for duration of address tenure. For input, indicates if another master has the address bus.
Data Bus Grant	EA	IA	For IA, grants data bus to external master. For EA, grants data bus to 8260.
Data Bus Busy	Wants bus	Owns bus	For output, asserts for duration of data tenure. For input, indicates if another master has the data bus.
Data Bus Grant Disable	IA	EA	When asserted, all DBG outputs should be negated to prevent bus contention.

How to Connect Three Bus Masters

Introduction

The diagram below shows how to connect three bus masters to the 8260.

Connection Diagram



How to Relatively Prioritize the Bus Masters (1 of 2)

Introduction

The bus masters must be prioritized relative to each other in the 60x Bus Arbitration-Level Registers, PPC_ALRH (level 0-7) and PPC_ALRL (level 8-15).

Priority Matrix

		HiPri							LowP
PPC_ALRH		PF0	PF1	PF2	PF3	PF4	PF5	PF6	PF7
CPM hrl	0000	■							
CPM mrl	0001		■						
CPM lrl	0010			■					
Reserved	0011				■				
Reserved	0100					■			
Reserved	0101						■		
Core	0110							■	
Ex Mstr 1	0111								■
Ex Mstr 2	1000								
Ex Mstr 3	1001								
Reserved	1xxx								
Reset Value Hex		0	1	2	3	4	5	6	7

Description

1. CPM hrl = CPM high request level. These are emergency requests when an FCC, MCC, or SCC is in danger of having an underrun or overrun.
2. CPM mrl = CPM mid request level. Normal requests from an FCC, MCC, or SCC.
3. CPM lrl = CPM low request level. Normal requests from SMC, SPI, and I2C.
4. See p. 11-7 of the MPC8260 User Manual for the specific priority levels.

How to Relatively Prioritize the Bus Masters (2 of 2)

Priority Matrix

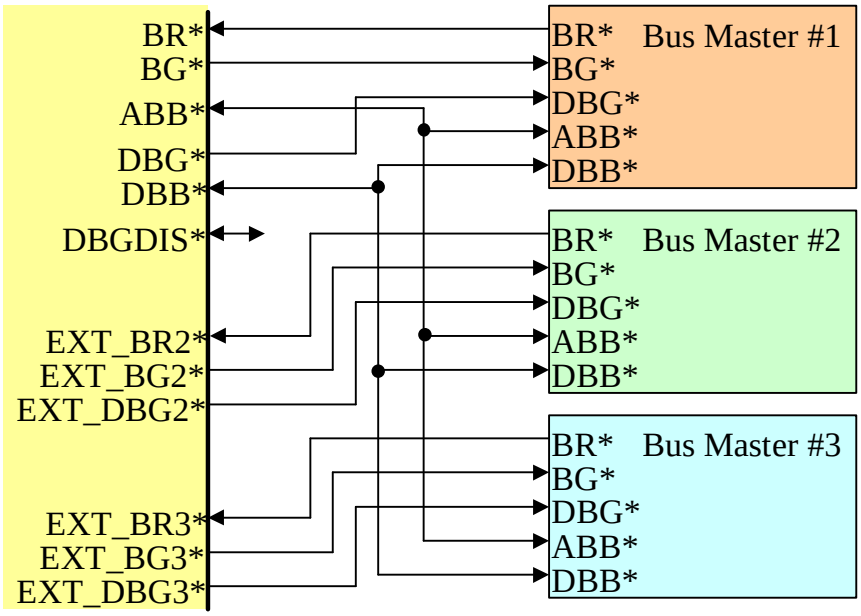
		HiPri							LowP
PPC_ALRL		PF8	PF9	PF10	PF11	PF12	PF13	PF14	PF15
CPM hrl	0000								
CPM mrl	0001								
CPM lrl	0010								
Reserved	0011								
Reserved	0100								
Reserved	0101								
Core	0110								
Ex Mstr 1	0111								
Ex Mstr 2	1000								
Ex Mstr 3	1001								
Reserved	1xxx								
Reset Value Hex		8	9	0xA	0xB	0xC	0xD	0xE	0xF

What is the Parking Master?

Definition

In a multi-processor system, the parking master has the bus if no one else is requesting it. If the parking master subsequently needs the bus, no time is required for arbitration.

Multi-processor System



Example

Initialize the 8260 so that external master 1 is the parking master (see p. 4-27).

```
pimm->PPC_ACR = 0x7;
```

Description

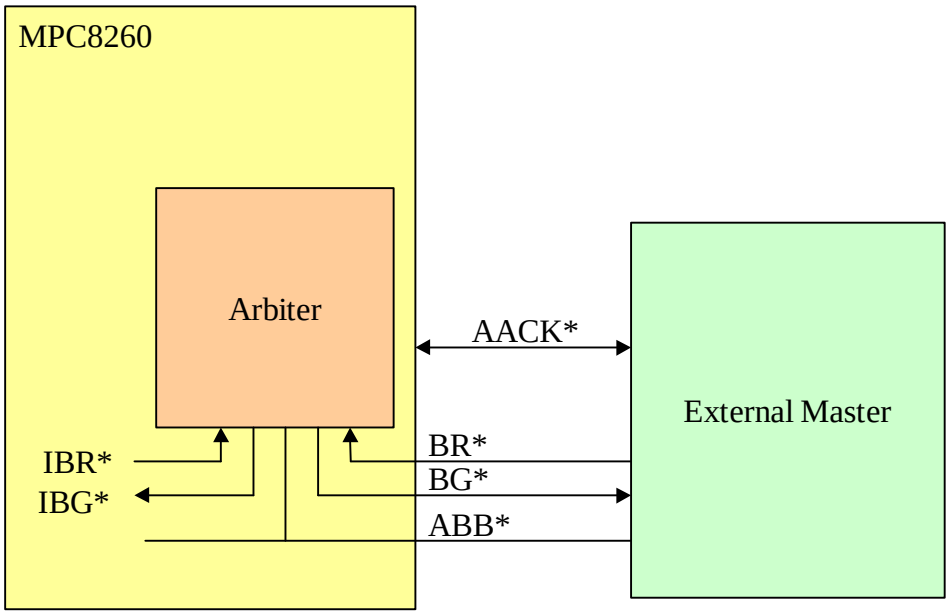
1. If, for example, bus master 1 is the parking master, and if no one is requesting the bus, then its bus grant is asserted.

How the 8260 Arbitrates the 60x Bus (1 of 3)

Introduction

The diagram below shows the arbitration process with one external master.

Block Diagram

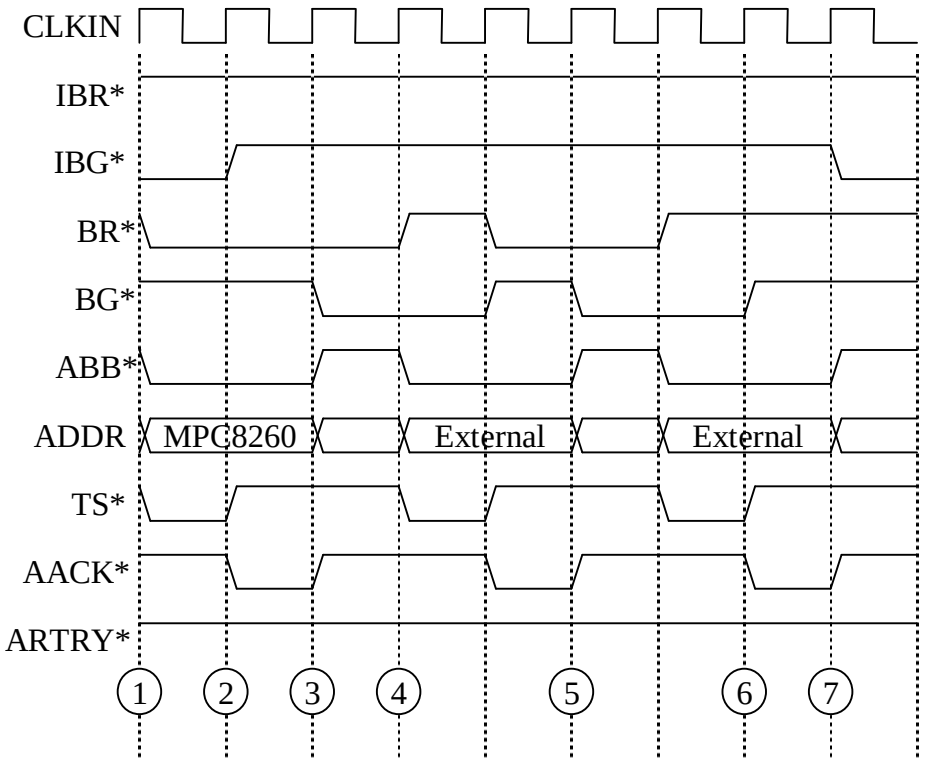


How the 8260 Arbitrates the 60x Bus (2 of 3)

Introduction

The diagram below shows the arbitration process with one external master.

Timing Diagram



Description

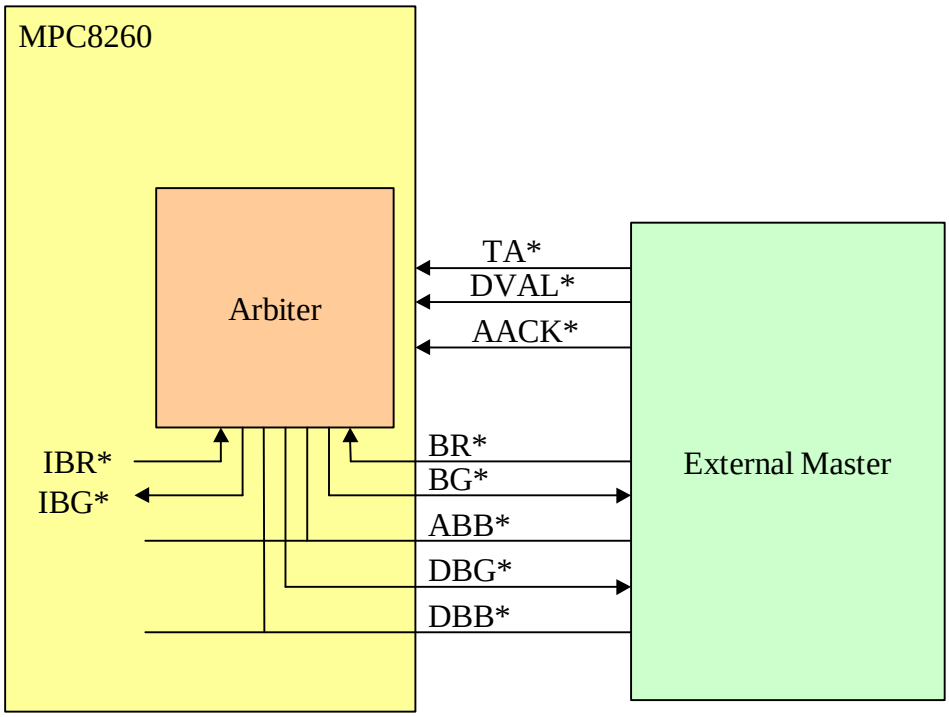
1. The 8260 is parked on the bus. An internal device proceeds to execute an address tenure. During the subsequent clock cycle, the external master asserts BR* to request the 60x bus.
2. AACK* is asserted. BR* is sampled, found asserted, and the arbiter negates IBG*.
3. BG* is asserted, 1 clock after the assertion of AACK*. At this time BG* is asserted while AACK* and ABB* are negated giving the external master a qualified bus grant.
4. The external master asserts ABB* and executes an address transaction.
5. The external master asserts BR* again and a second address transaction is executed.
6. While AACK* is asserted, no bus request is asserted.
7. As the parking master, IBG* is asserted.

How the 8260 Arbitrates the 60x Bus (3 of 3)

Introduction

The diagram below shows the arbitration process with one external master.

Block Diagram

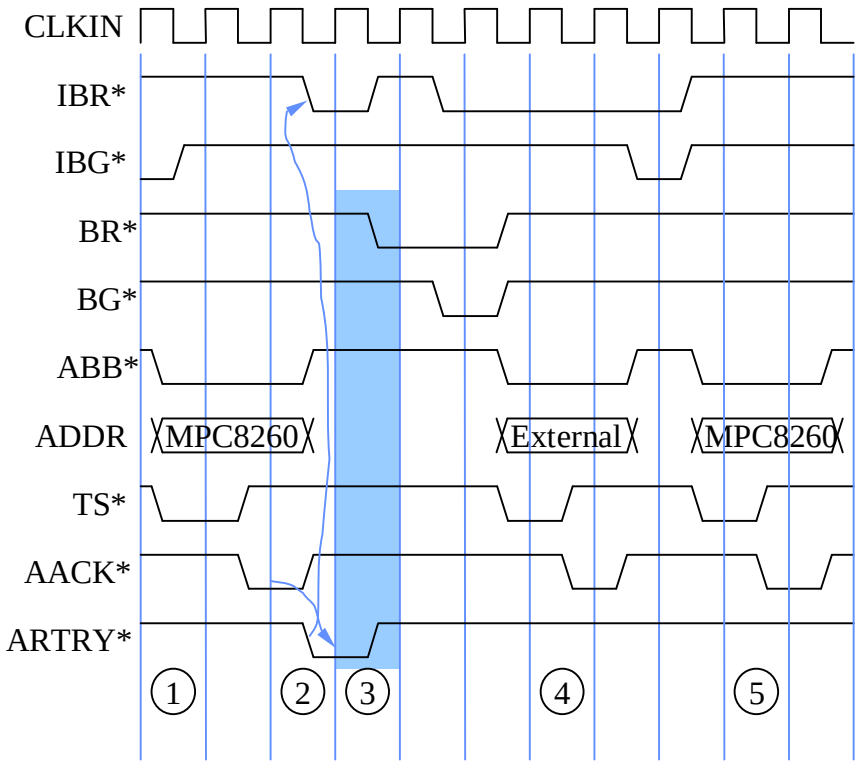


How the 8260 Retries an Address

Introduction

The diagram below shows the 8260 responding to an early ARTRY*.

Timing Diagram



Types of ARTRY*

1. No data tenure has begun - early or qualified ARTRY*
2. Data tenure has begun

Description

1. The 8260 executes an address tenure.
2. On the clock cycle following assertion of AACK*, ARTRY* is asserted by an external master to indicate a snooping master requires the cycle be rerun.
3. During the window of opportunity (in blue), the snooping master (and only the snooping master) asserts BR*. This guarantees the snooping master be granted the bus before the just-retried master can restart its transaction.
4. The external master executes a write to memory to the address snooped.
5. The 8260 regains the bus and reruns the previous address tenure.

Exercises - 60x Bus

Provide the answers to these questions...

The following questions assume that the 8260 is the arbiter.

1. This pin is asserted by another bus master to request the bus: _____
2. This pin indicates to an external master that it has the bus on a qualified basis: _____
3. This pin indicates that a master has the address bus: _____
4. This pin indicates the start of a new address tenure: _____
5. This pin is asserted by the slave to indicate the completion of the address tenure: _____
6. This signal indicates that the bus transaction should be retried by the 60x bus master: _____
7. This pin indicates that a master has the data bus: _____
8. This pin indicates that a data beat is valid on the bus: _____
9. This pin indicates that an operand is complete on the data bus: _____

…from this list...

AACK*
ABB*
ARTRY*
BG*
BR*
DBB*
DBG*
DVAL*
TA*
TS*