Towards a Multi-GHz Open-Source Sampling Oscilloscope

Ted Yapo

Hackaday Superconference

November 17, 2019

State of the Art 1968

mVOLTS/DIV
TYPE S-1
SAMPLING HEAD
$t_r \leq 350$ ps
TEKTRONIX®
LOCK
50Ω
±5V MAX

mVOLTS/DIV
TYPE S-4
SAMPLING HEAD
±5V MAX
CAUTION
$t_r \leq 25$ps
50Ω
TEKTRONIX®
LOCK

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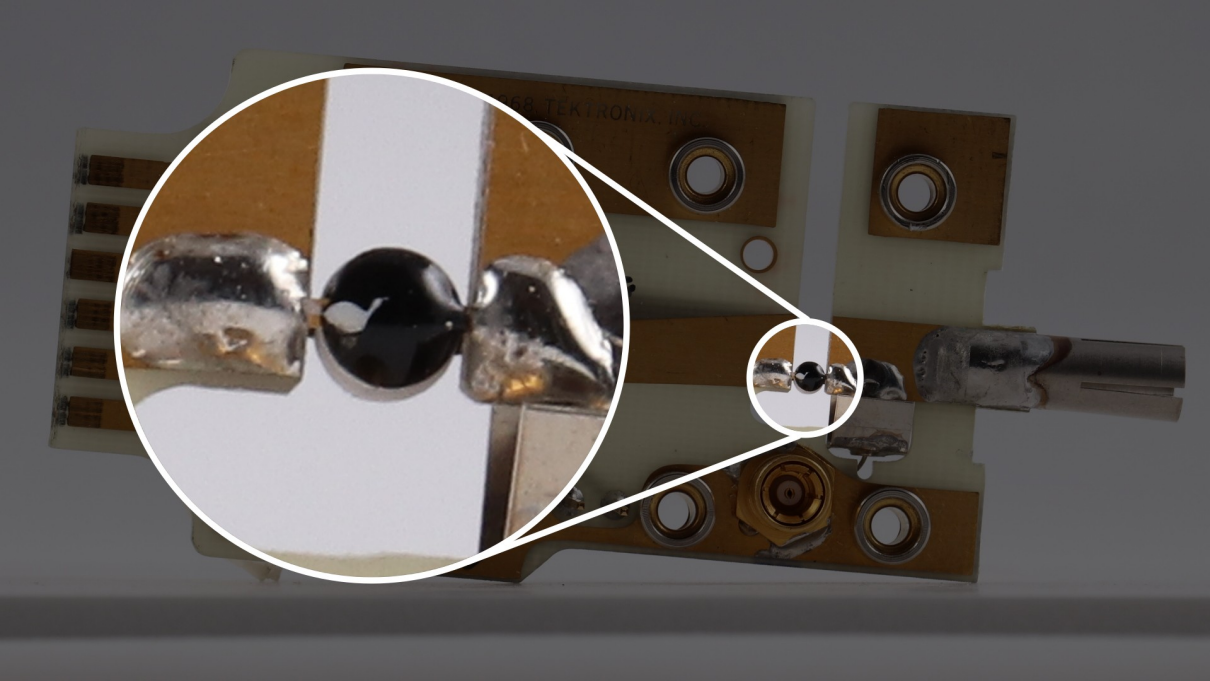
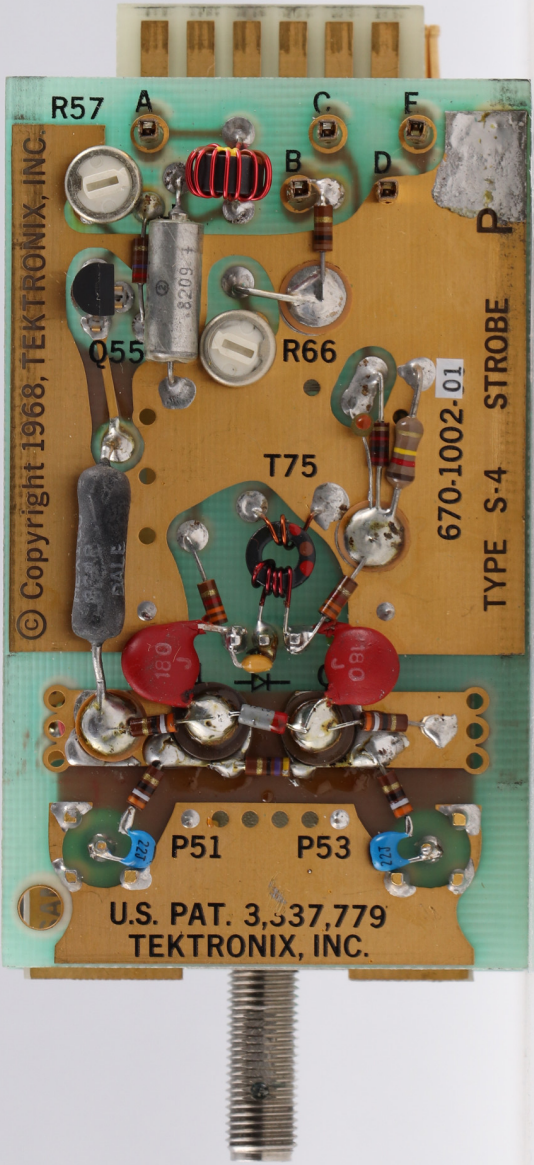
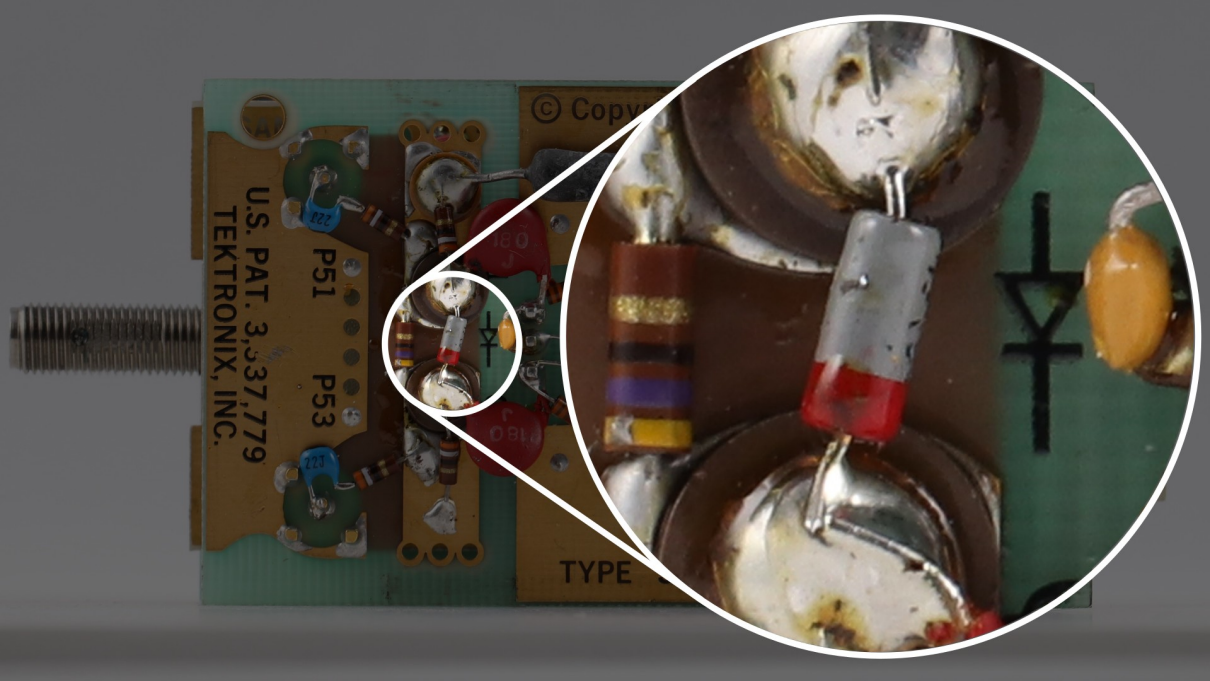
03
-9910-029


TEKTRONIX, INC.


R57
A
C
F
B
D
P
© Copyright 1968, TEKTRONIX, INC.
Q55
R66
T75
670-1002-01
TYPE S-4 STROBE
P51
P53
U.S. PAT. 3,537,779
TEKTRONIX, INC.

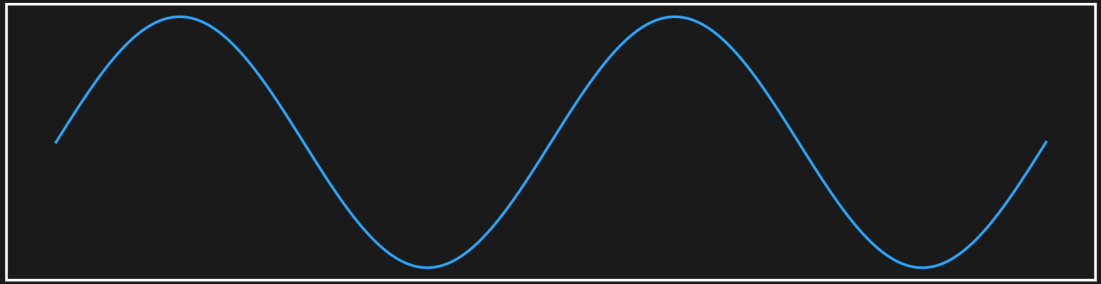

U.S. PAT. 3,537,779
TEKTRONIX, INC.
P51
P53
TYPE

Real Time Sampling

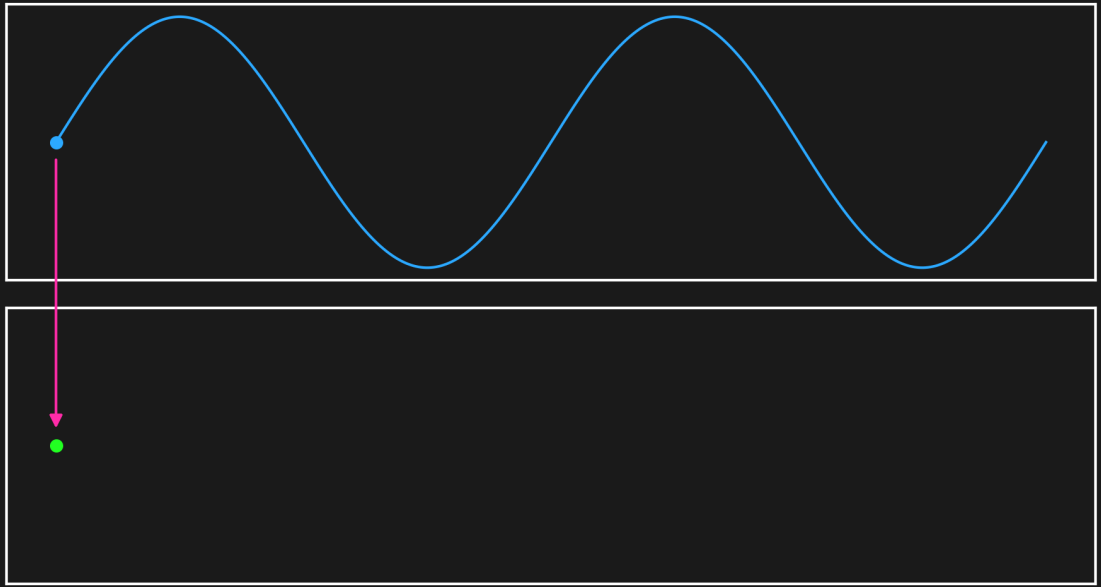
vs

Equivalent Time Sampling

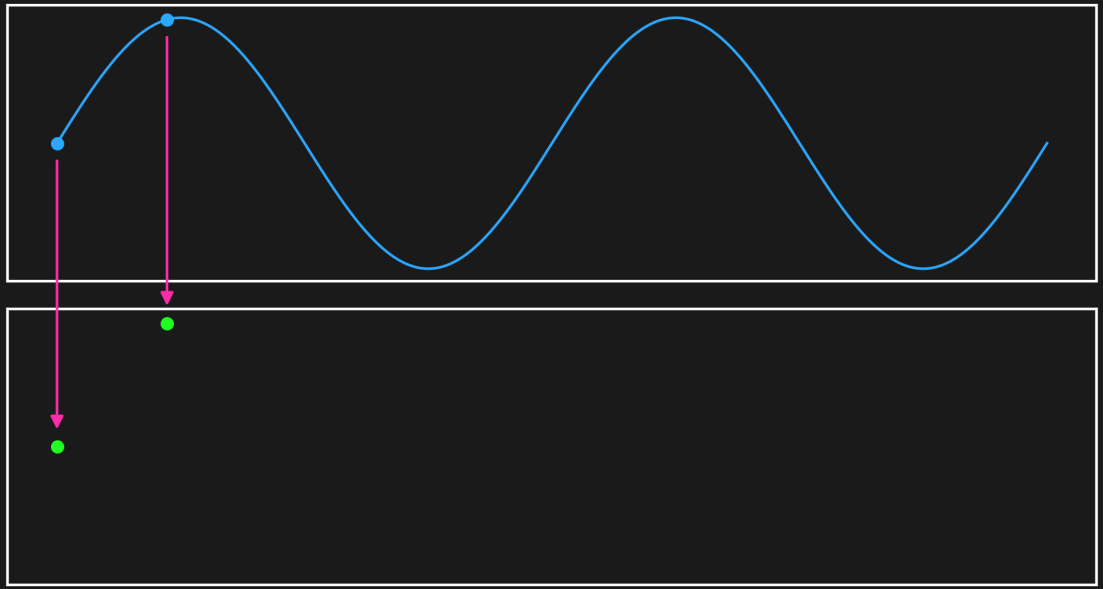
Real-time Sampling



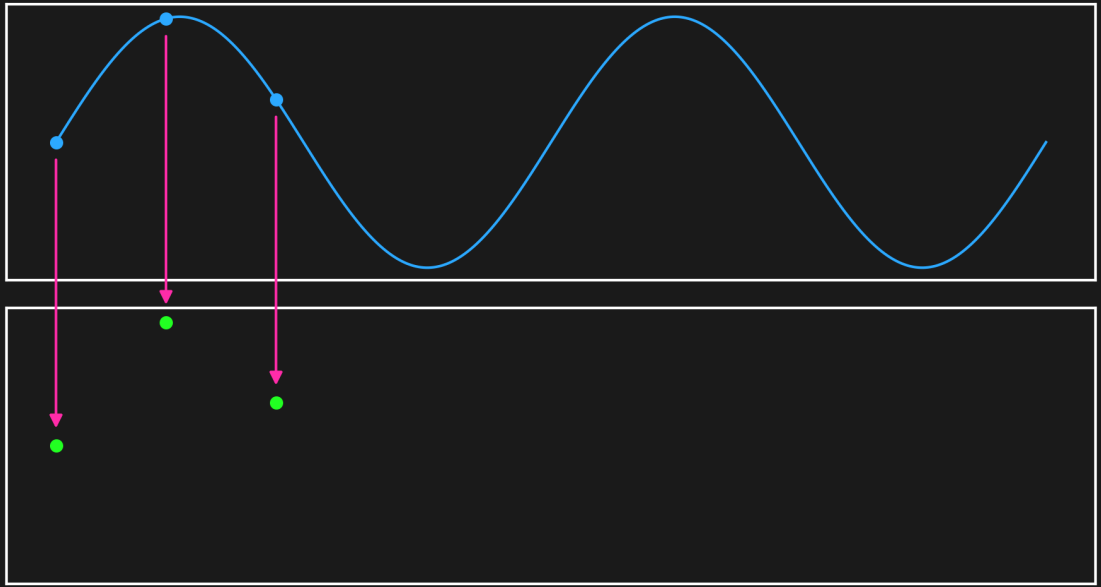
Real-time Sampling



Real-time Sampling



Real-time Sampling



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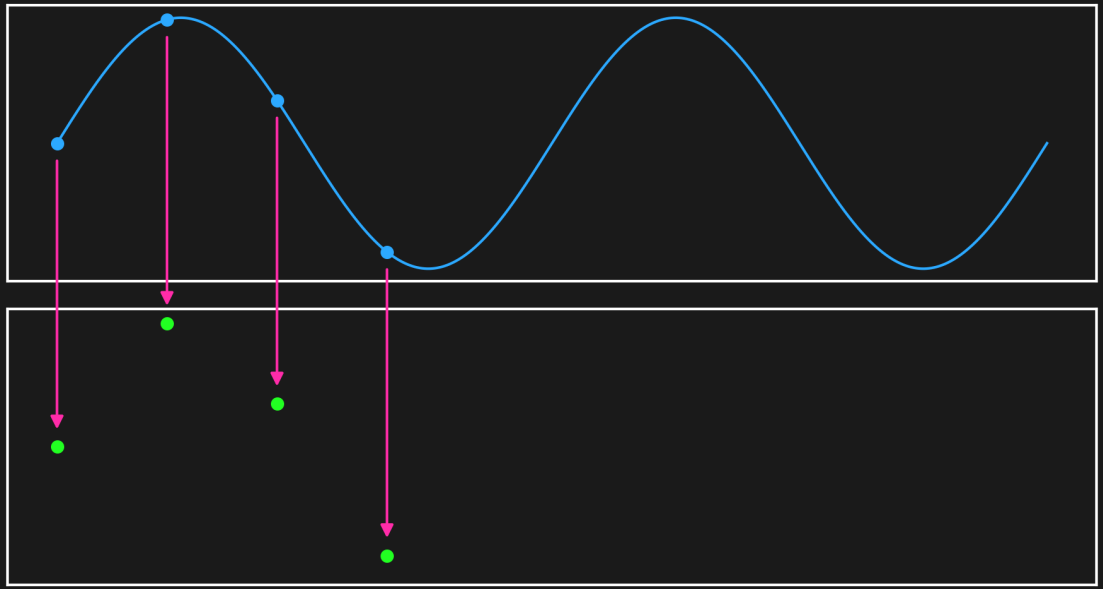

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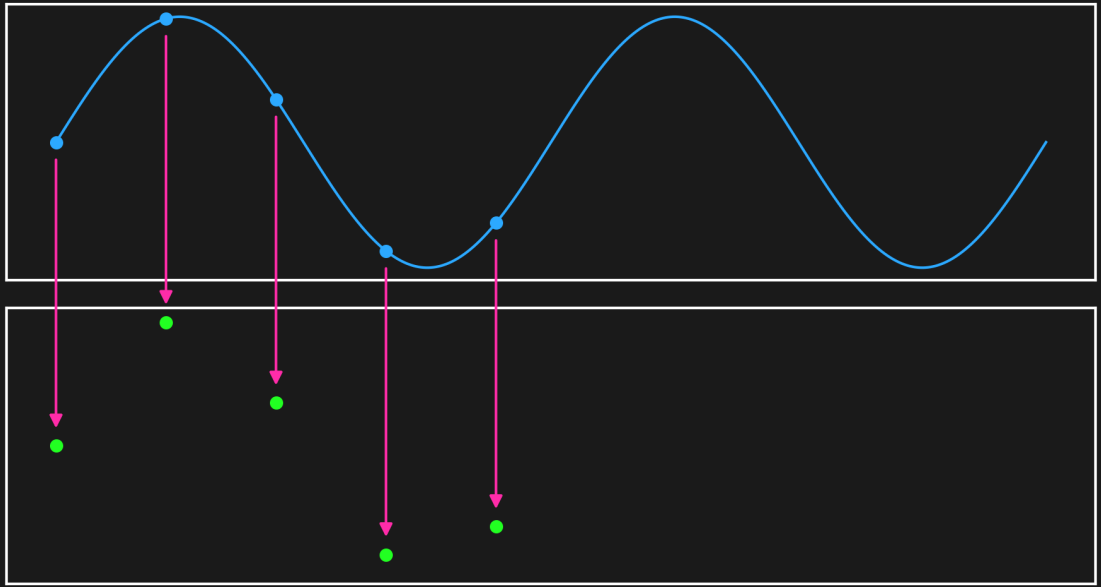

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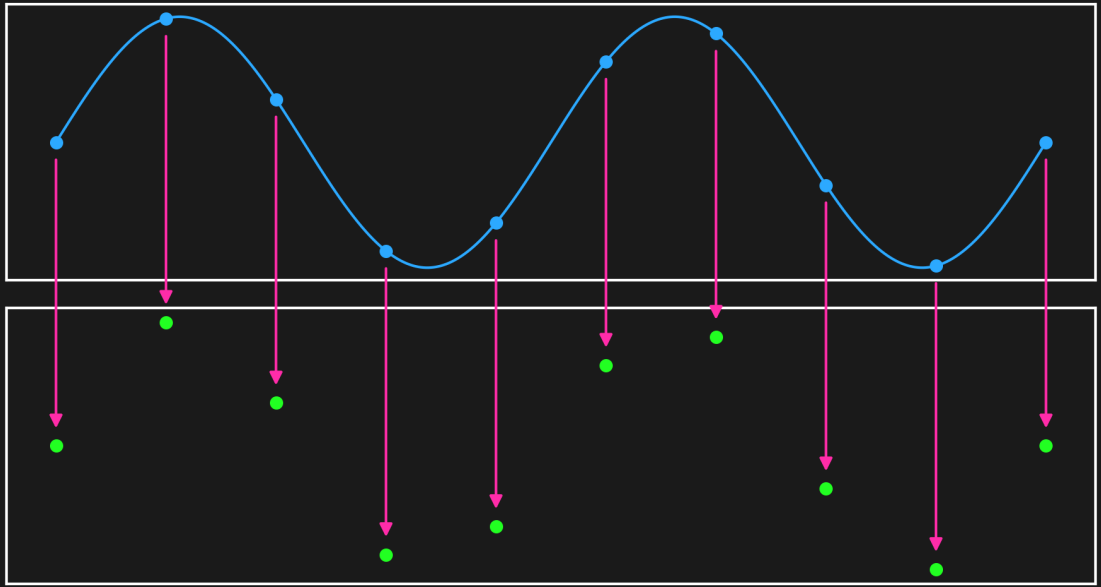

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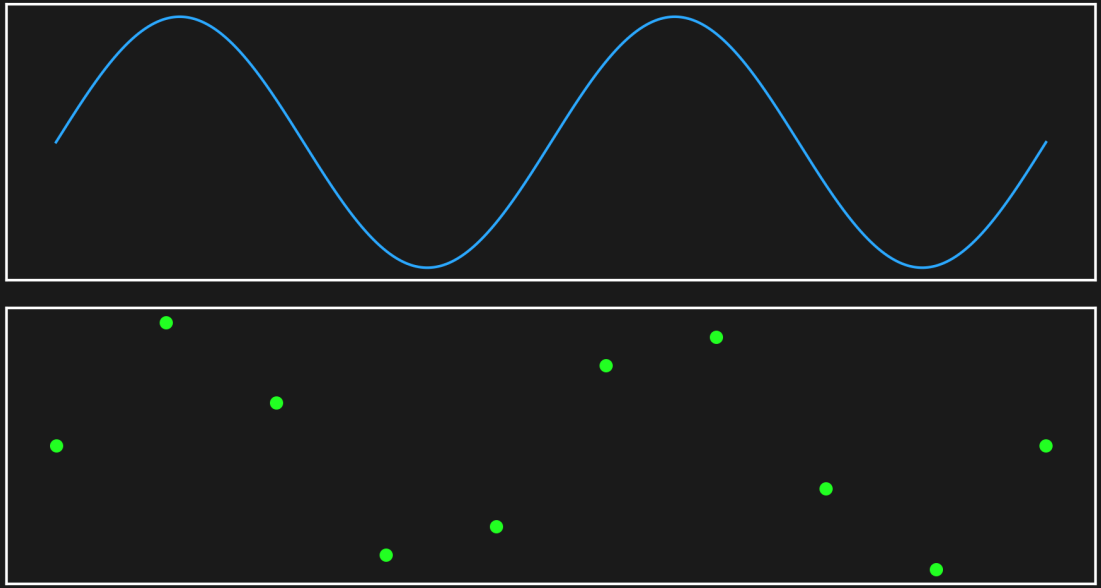
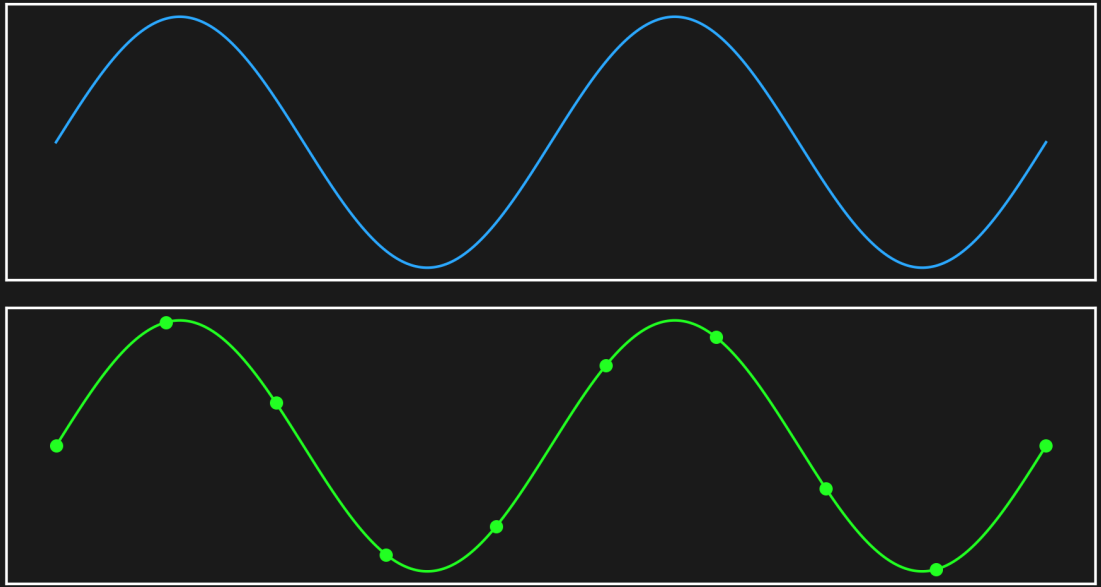
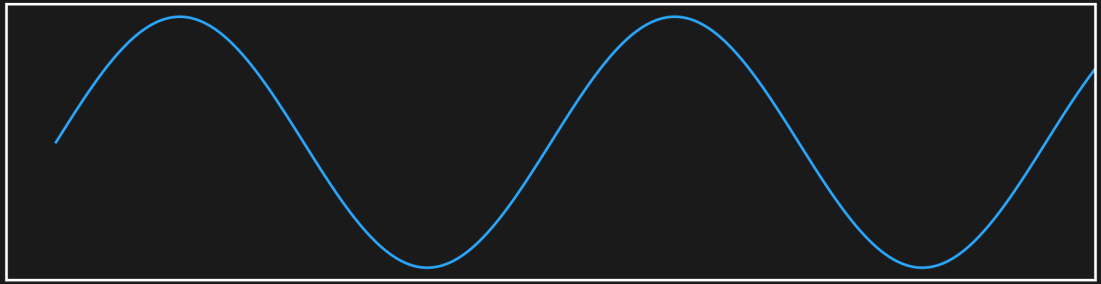


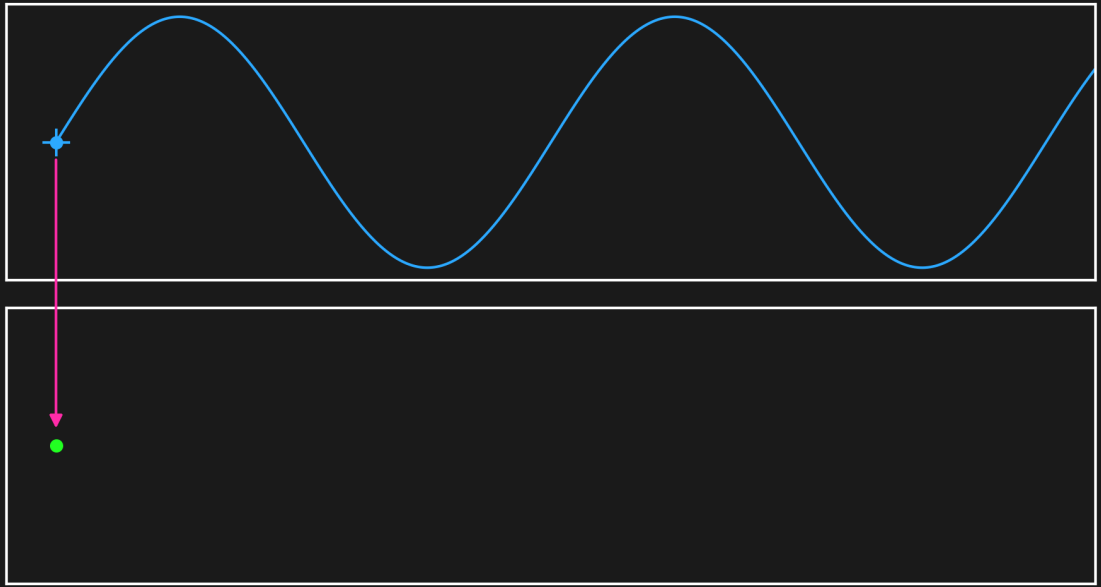
Real-time Sampling



Equivalent-time Sampling



Equivalent-time Sampling



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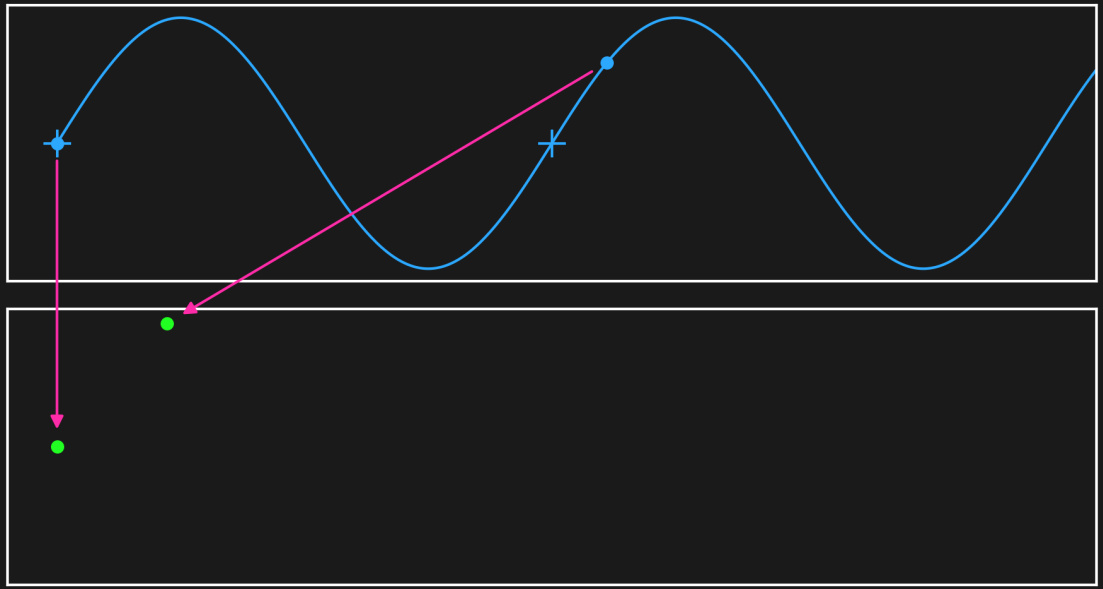

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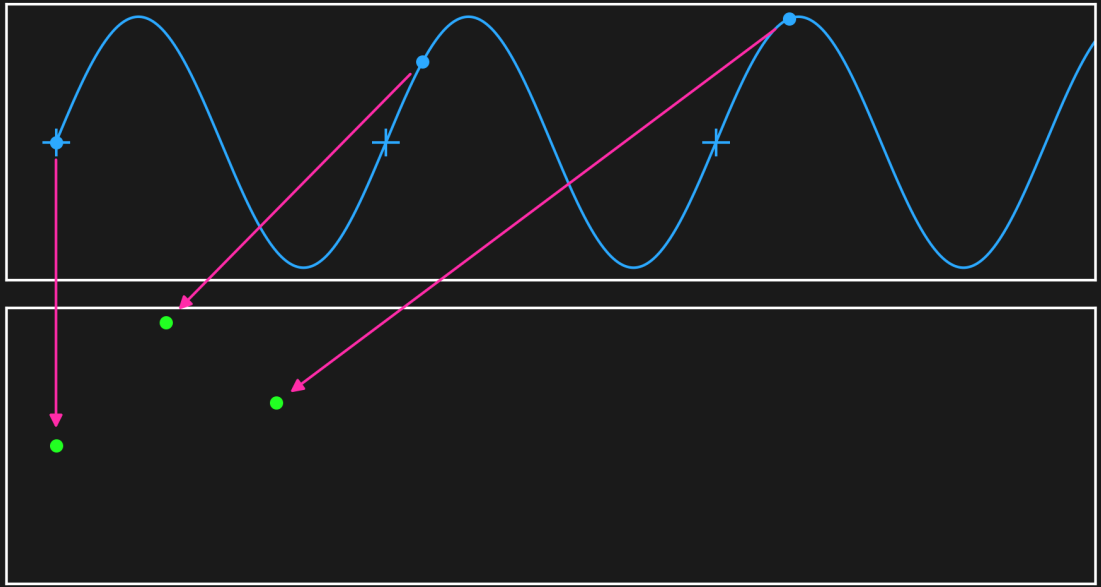

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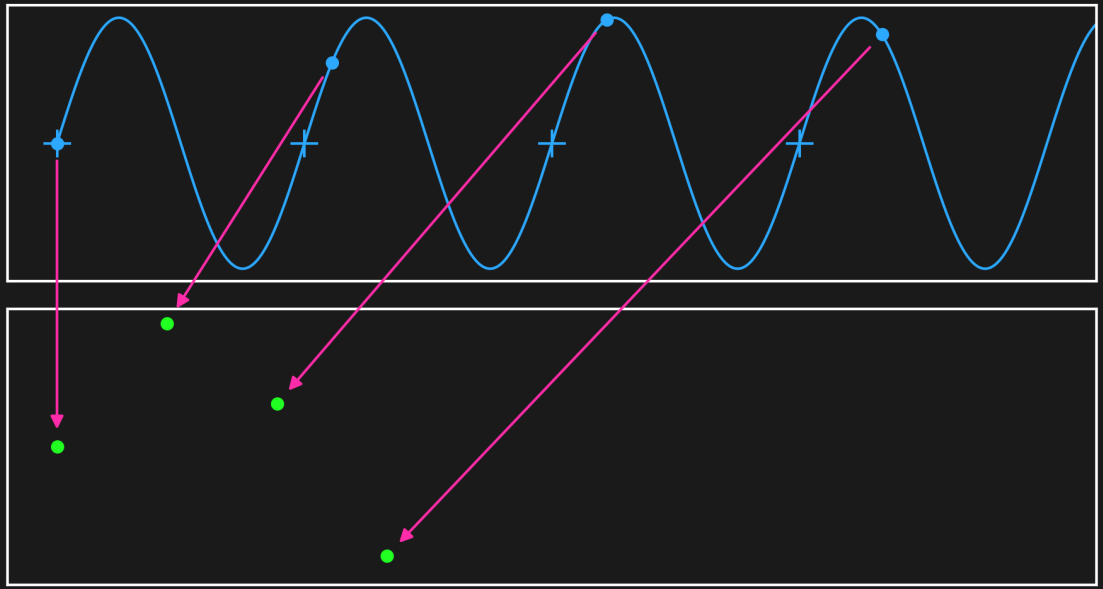
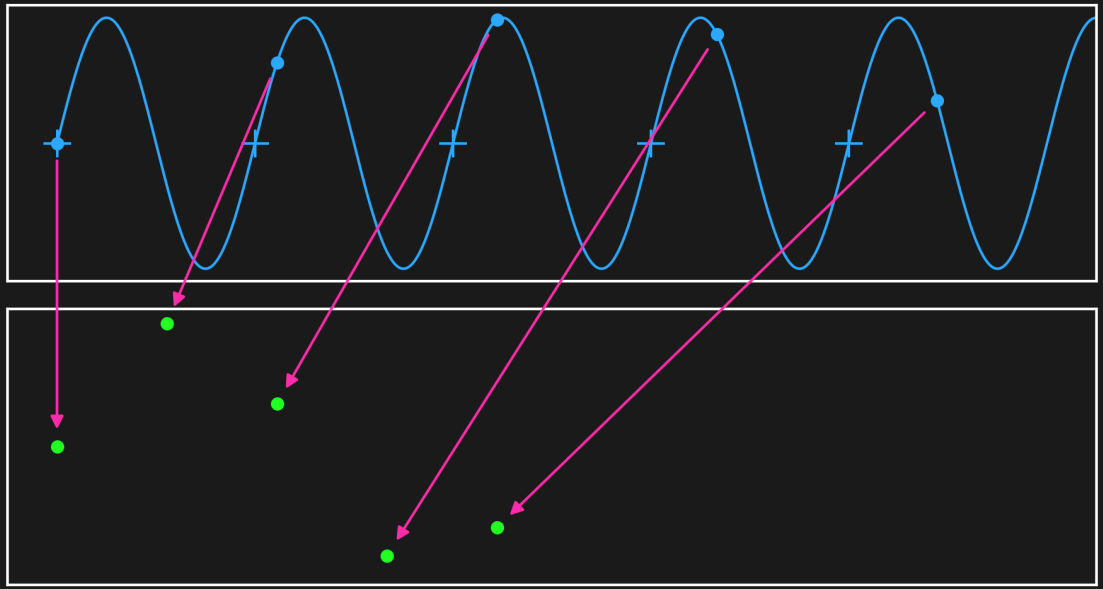


Equivalent-time Sampling



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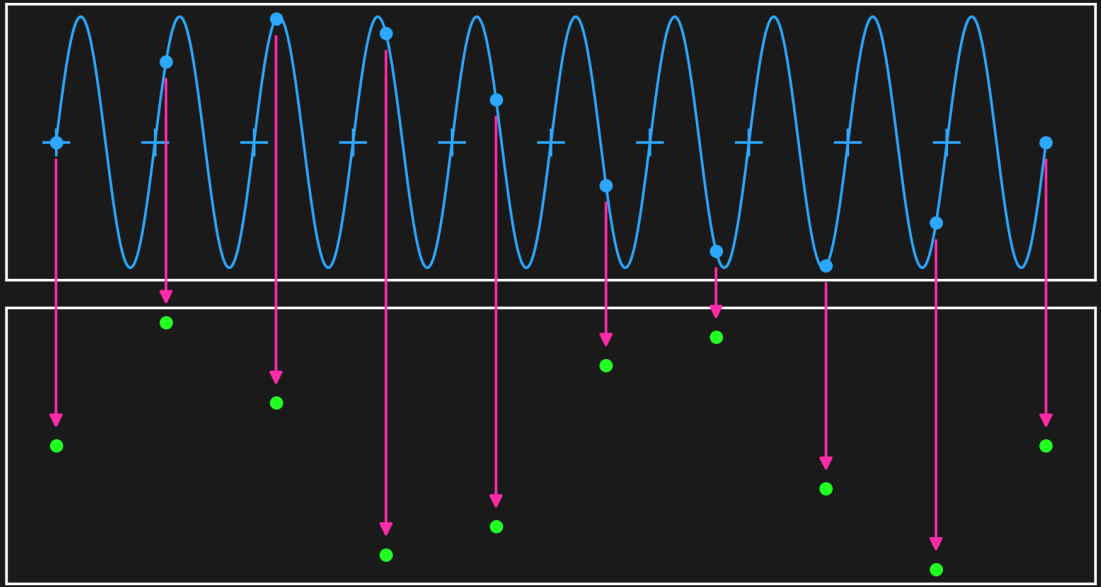

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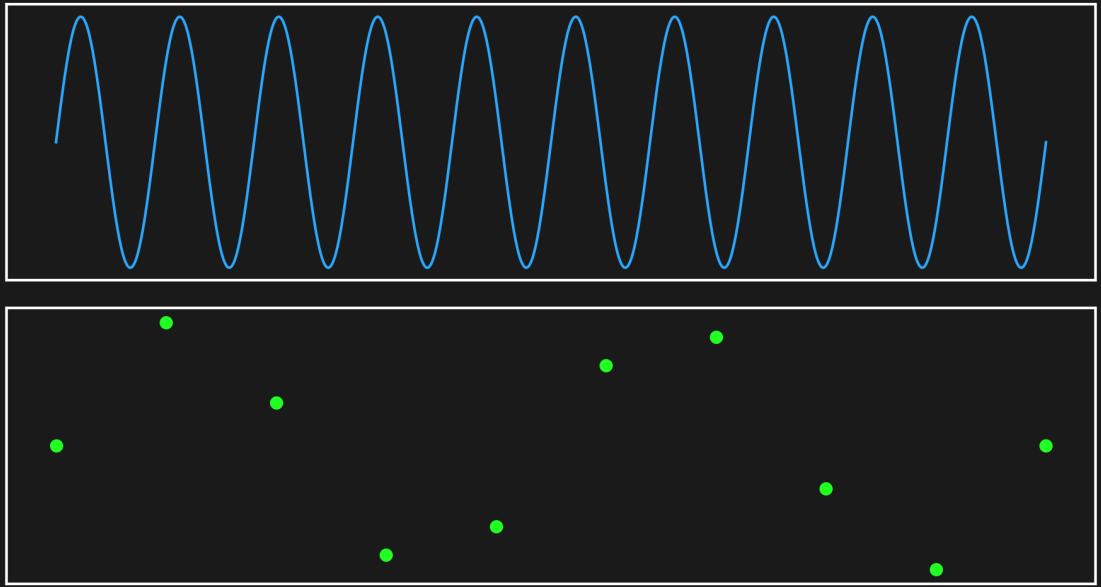
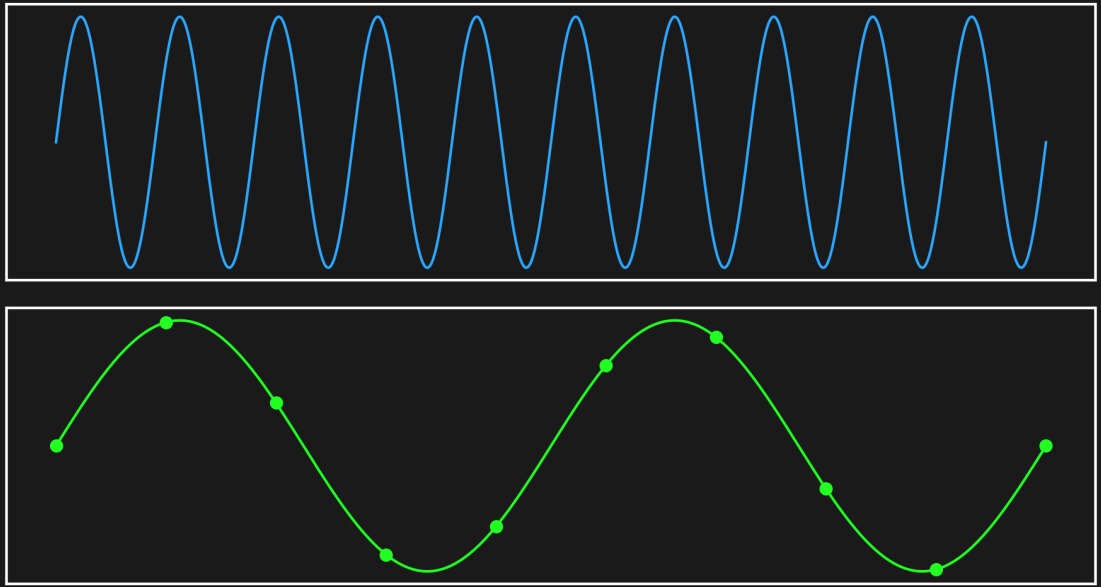
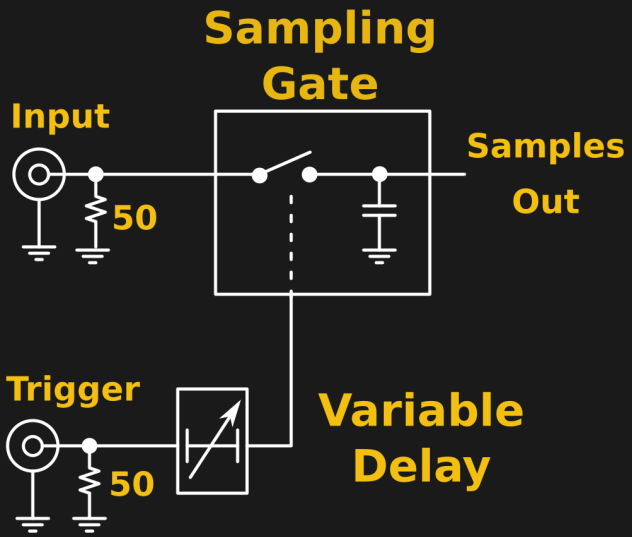
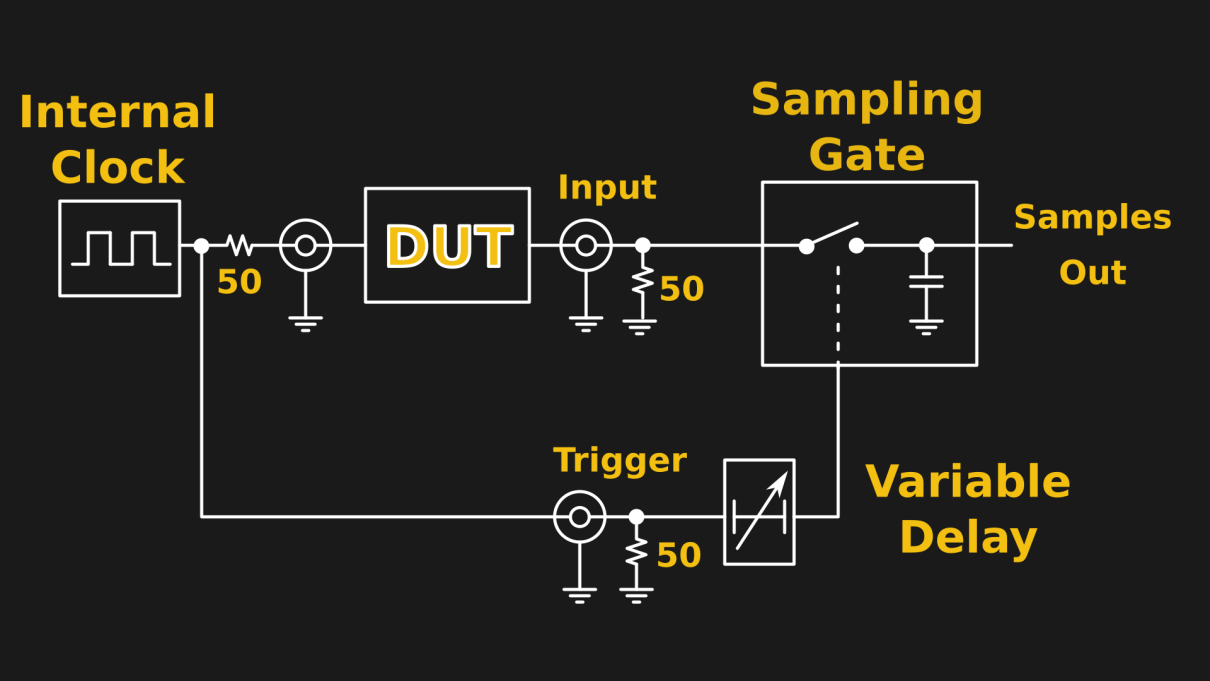


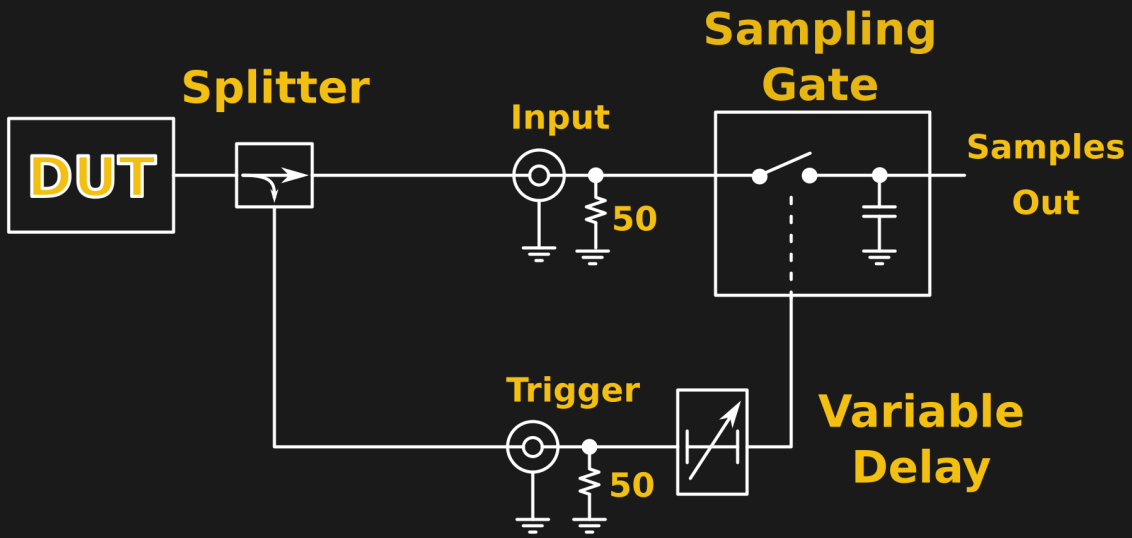
Equivalent-time Sampling

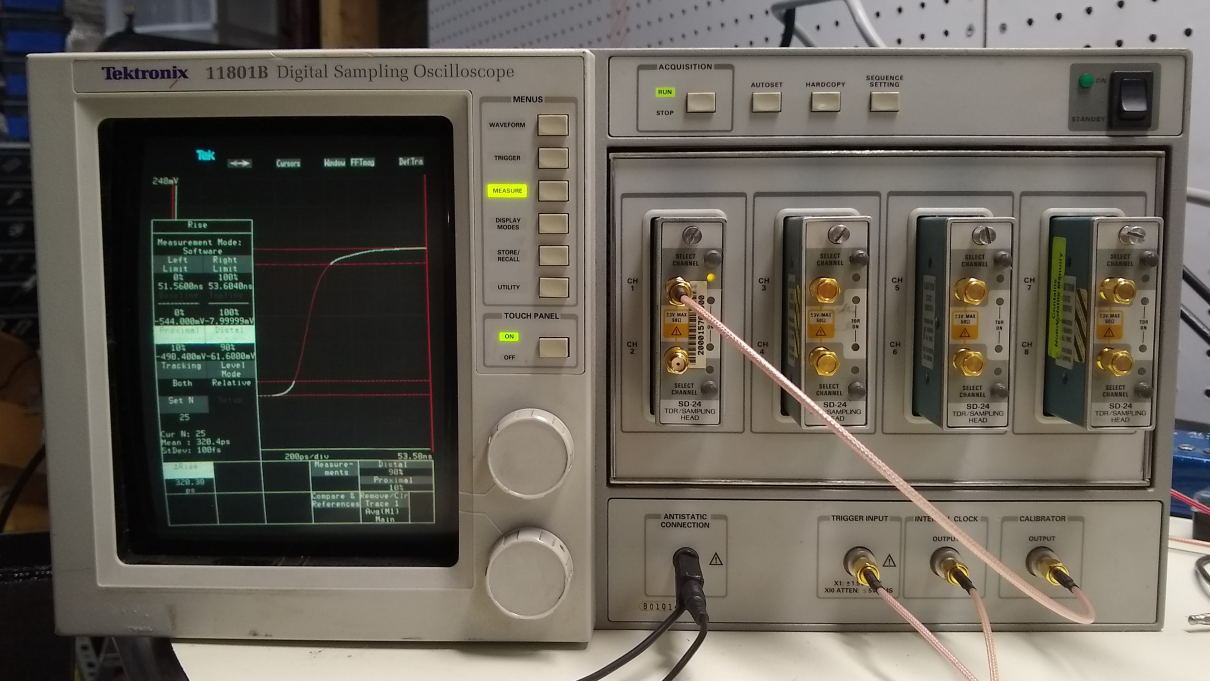


ET Sampling Architecture


Sampling
Gate
Input
Samples
Out
50
Trigger
Variable
Delay
50

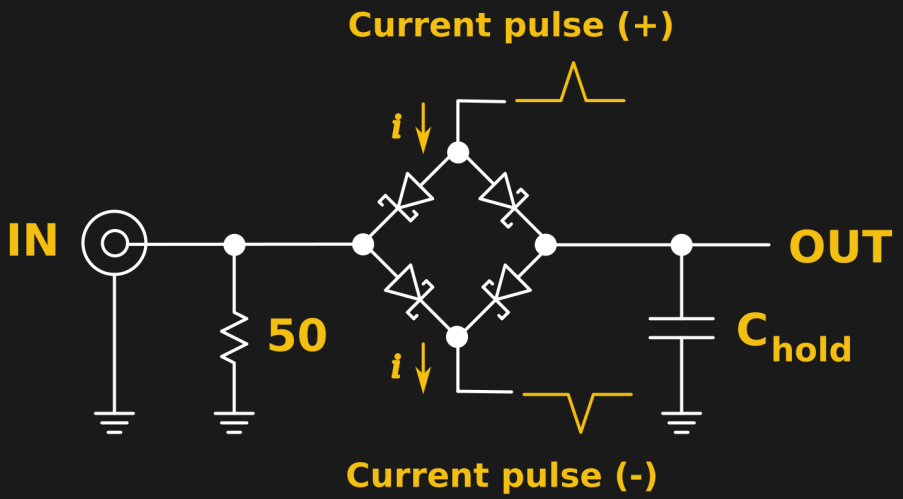

Internal
Clock
50
DUT
Input
50
Sampling
Gate
Samples
Out
Trigger
50
Variable
Delay


Sampling
Gate
Splitter
Input
DUT
50
Samples
Out
Trigger
Variable
Delay
50


Tektronix 11801B Digital Sampling Oscilloscope
MENUS
WAVEFORM
TRIGGER
MEASURE
DISPLAY MODES
STORE/ RECALL
UTILITY
TOUCH PANEL
ON
OFF
ACQUISITION
RUN
STOP
AUTOSET
HARDCOPY
SEQUENCE SETTING
ON
STANDBY
Tek
Cursors
Window
FFTmag
DefTrm
240mV
Rise
Measurement Mode: Software
Left Limit
Right Limit
0%
100%
51.5600ns
53.6040ns
0%
100%
-544.000mV
-7.99999mV
10%
90%
-490.400mV
-61.6000mV
Tracking
Level Mode
Both
Relative
Set N
25
Cur N: 25
Mean : 320.4ps
StDev: 100fs
200ps/div
53.50ns
320.30 ps
Measure-ments
Distal 90%
Proximal 10%
Compare & References
Remove/Clr Trace & Rsl(N1) Main
CH 1
CH 2
CH 3
CH 4
CH 5
CH 6
CH 7
CH 8
SELECT CHANNEL
SD-24 TDR/SAMPLING HEAD
ANTISTATIC CONNECTION
TRIGGER INPUT
X1 ±1V
X10 ATTEN. ±5V MAX
OUTPUT
CALIBRATOR
OUTPUT
80101

The Analog Way

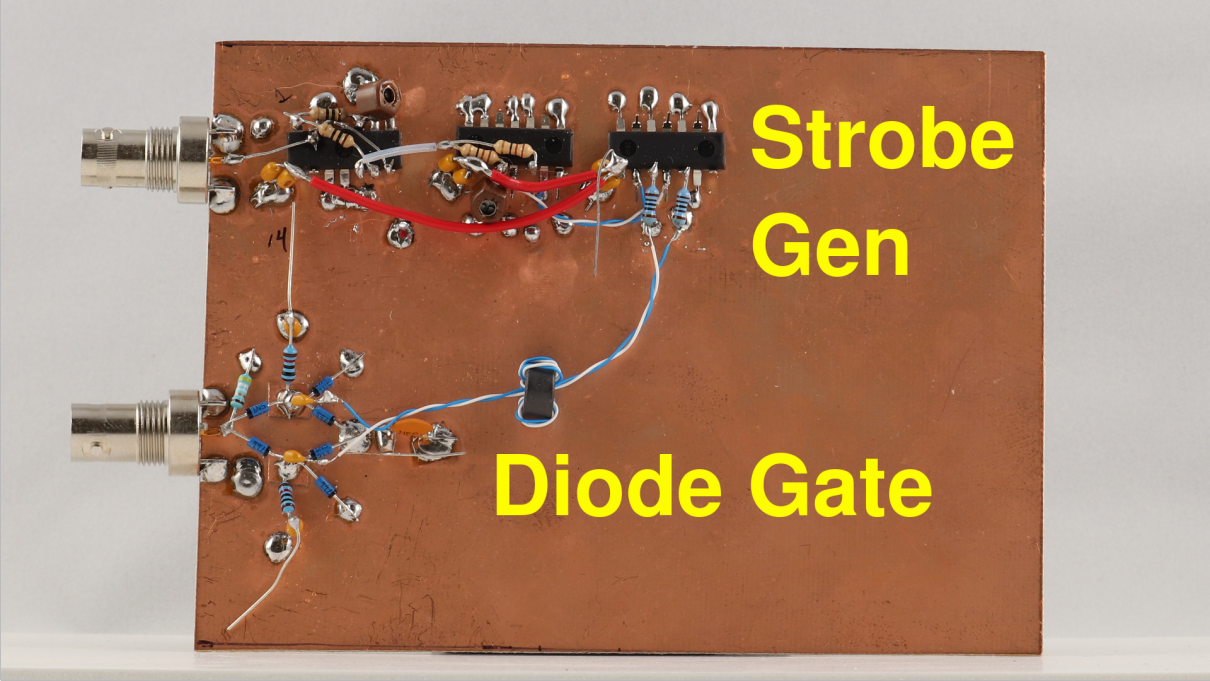
4-Diode Sampler

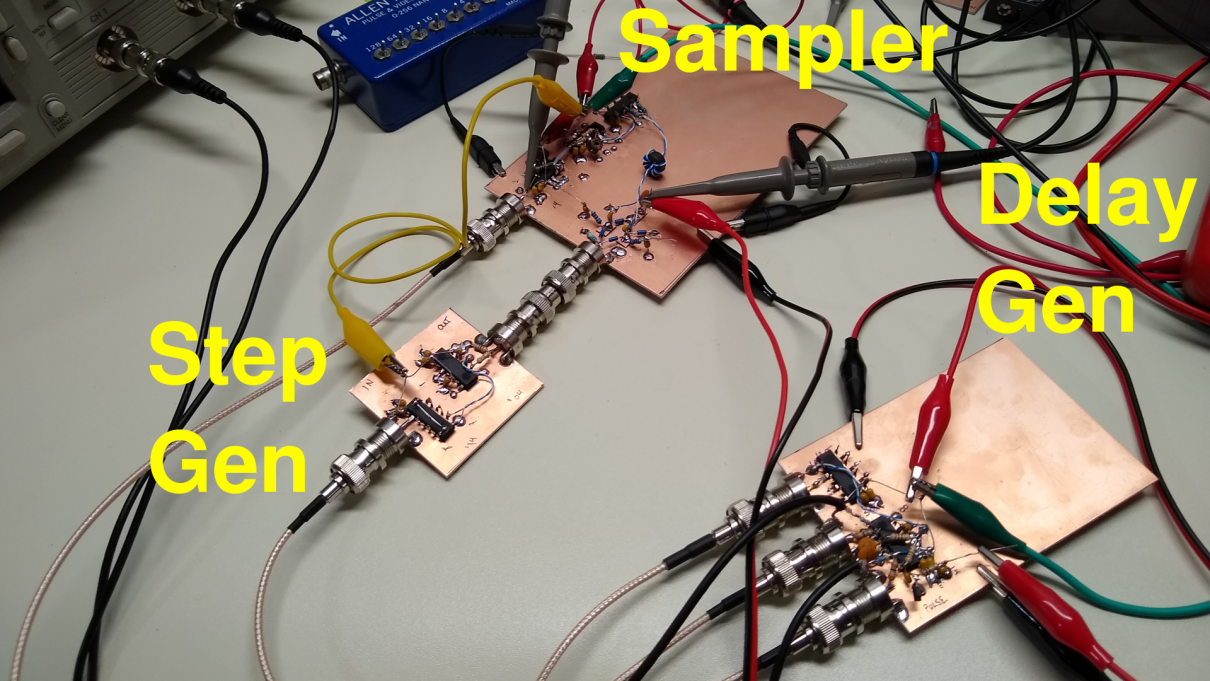


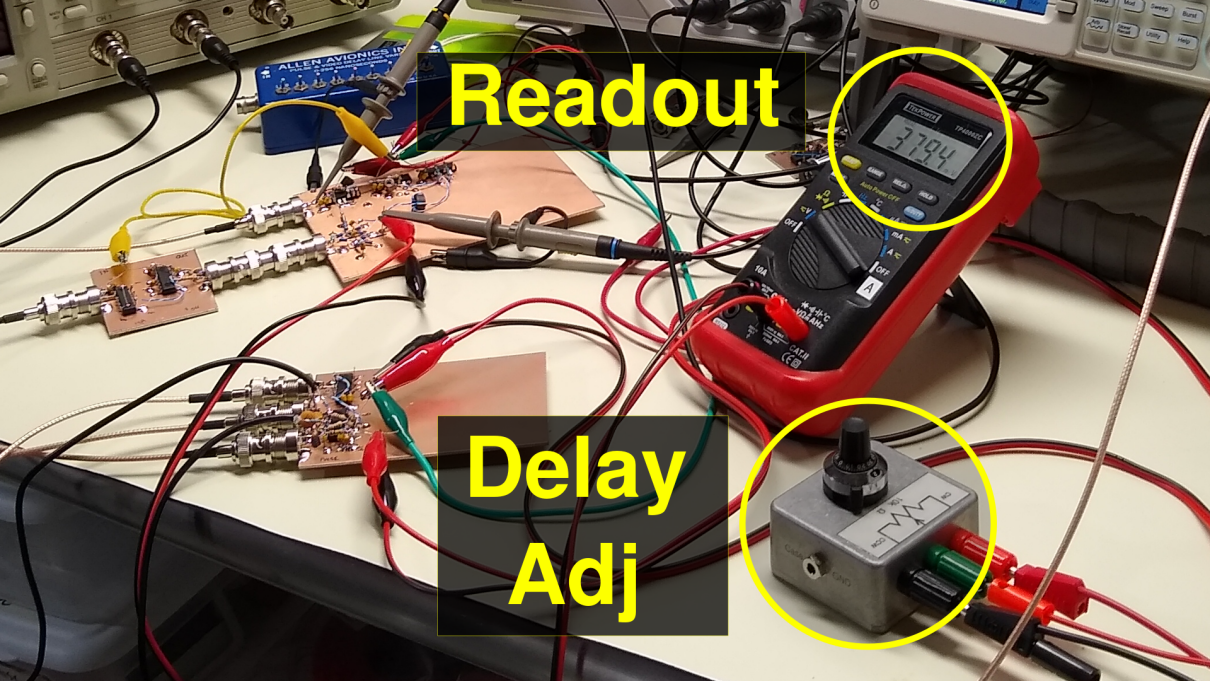
Fast Edges c. 2019

- NE555: 100 ns
- 74HC04: 1.7 ns
- 74AC04: 1 ns
- 74LVC1G04: 500 ps
- ECL Gate: 150 ps
- SiGe Transistors: 75 ps
- CML Comparator: 35 ps (20%-80%)
- CML Gate: 26 ps (20%-80%)
- Limiting Amplifier: 24 ps (20%-80%)
- Laser Diode Driver: ?
- Unobtainium CML Gate: [8 ps]

First Analog Sampler


Strobe
Gen
Diode Gate


Sampler
Delay
Gen
Step
Gen


Readout
Delay
Adj
ALLEN AVIONICS INC
3.794
Auto Power OFF
OFF
A

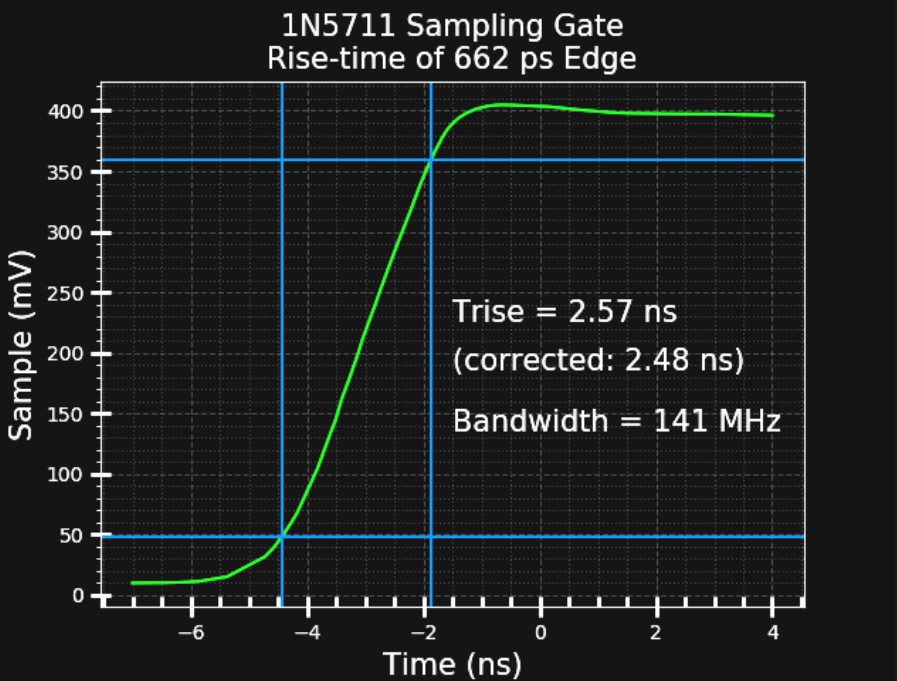
Δt
1.477
1.572
1.655
1.840
1.905
2.017
2.149
2.285
2.390
2.564
2.701
2.808
2.898
2.990
3.155
3.218
3.297
3.393
3.510
3.588
3.685
3.759

Δt	Volt
−1.295	24
−1.185	2
−1.147	2
−1.018	2
−943 ps	2
~~−889~~ 880	2
−730 ps	1
−590 ps	1
−482 ps	1
−329 ps	
−256 ps	
−170 ps	
−10 ps	
61 ps	
155 ps	
345 ps	
470 ps	
~~530~~ 540 ps	
615 ps	
660 ps	
698 ps	
775 ps	
890 ps	
1.018 ns	

MOMENT ~ 685 ps

2/2/19

Time	Voltage	
−6.285	375.6	
−5.952	375.6	
−5.787	375.7	
−5.252	376.5	
−4.994	376.9	
−4.864	377.1	
−4.494	377.4	
−3.323	376.8	
−3.175	376.4	
−3.032	375.6	
−2.883	373.7	
−2.704	370.6	
−2.607	367.7	
−2.504	363.3	
−2.424	359.9	
−2.323	353.9	δ = 33 ps
−2.243	349.2	
−2.107	338.0	26 ps
−1.961	325.2	
−1.845	311.6	
−1.775	306 ~~3.3~~ ~~3.3~~ 306.1	
−1.658	290.1	
−1.498	273.9	45 ps


1N5711 Sampling Gate
Rise-time of 662 ps Edge
Trise = 2.57 ns
(corrected: 2.48 ns)
Bandwidth = 141 MHz
Sample (mV)
Time (ns)
400
350
300
250
200
150
100
50
0
−6
−4
−2
0
2
4

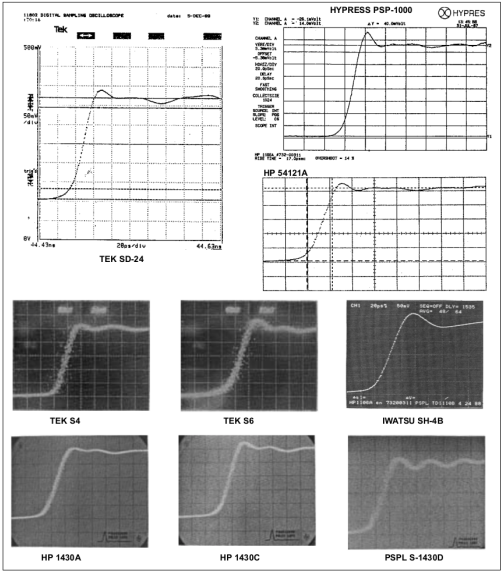


Figure 1: Picosecond Domain Transient Step Responses of 9 Sampling Heads
Input step from HP-1106A TD pulser. 50 mV/div and 20 ps/div.

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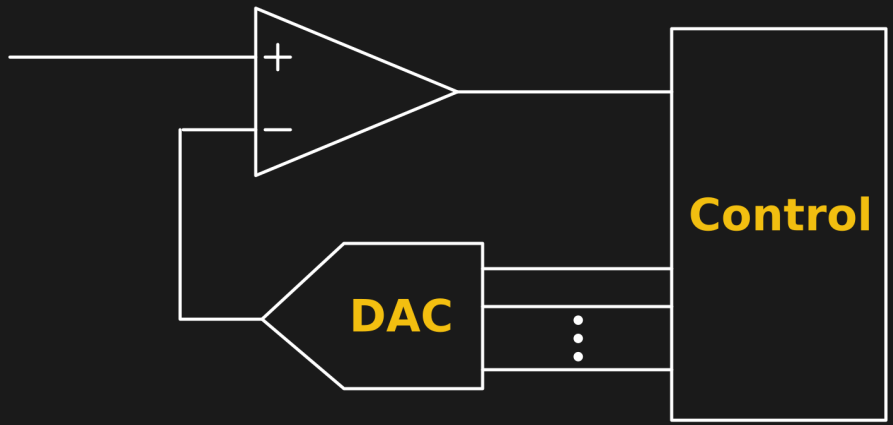
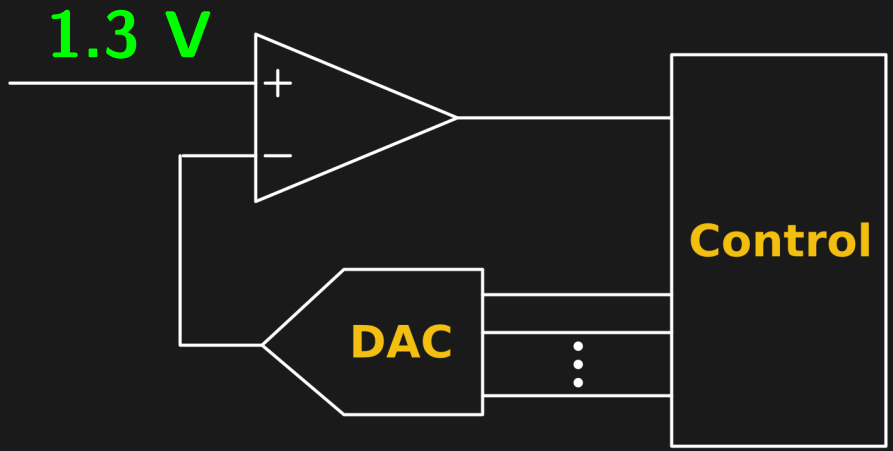
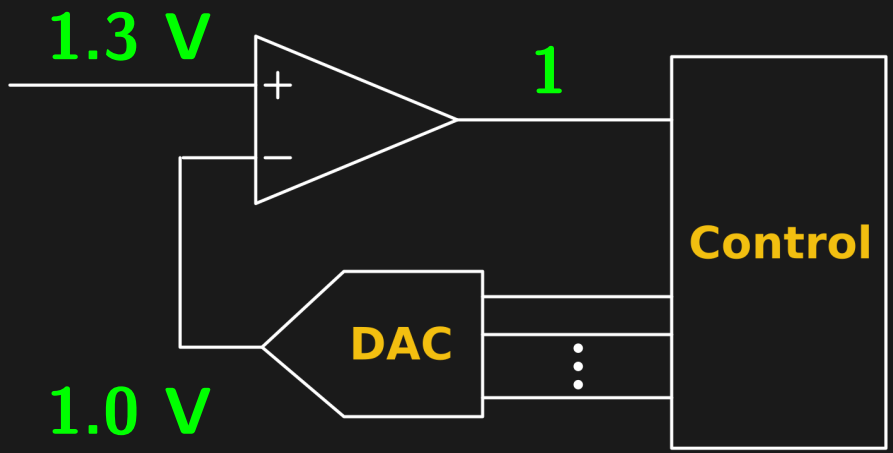
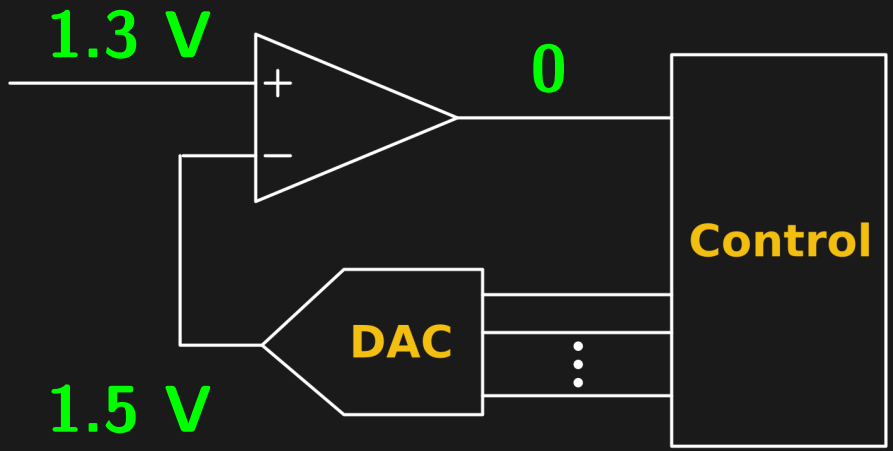
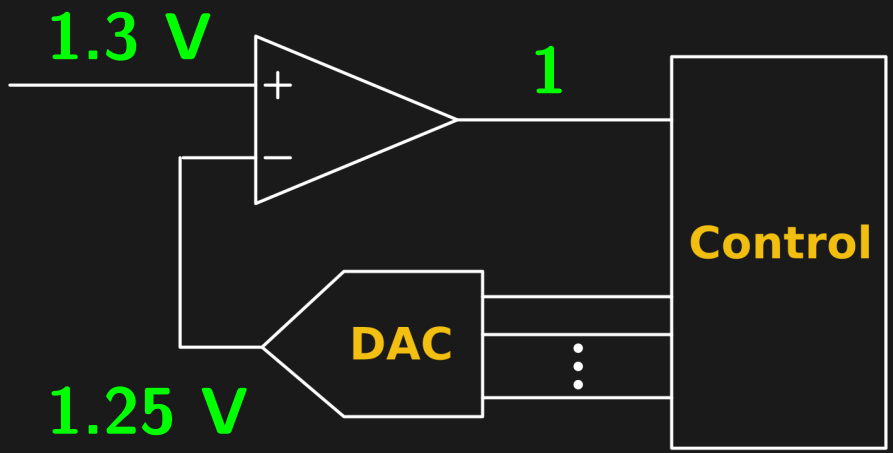
The Digital Way

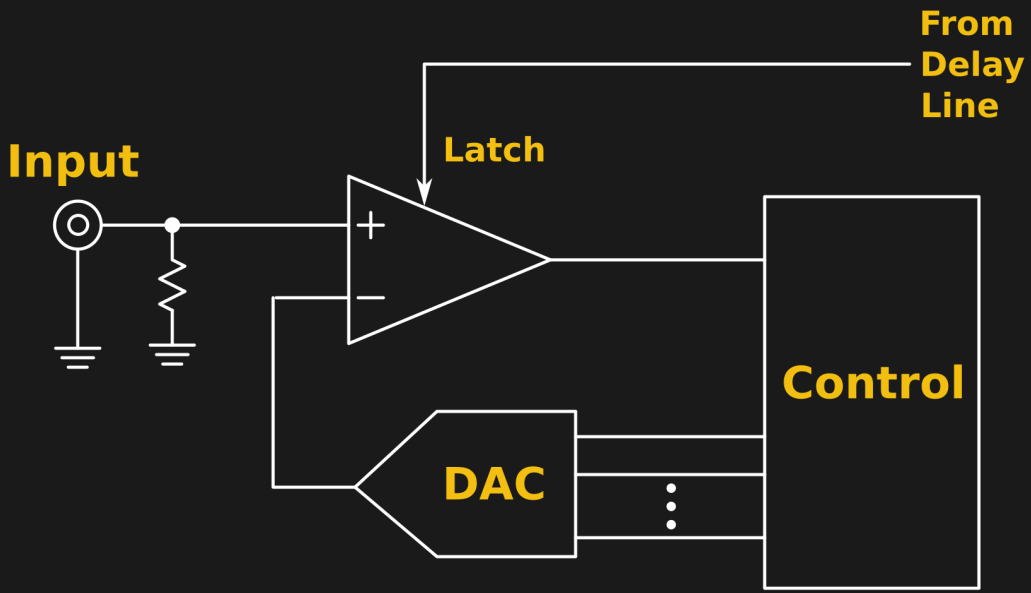

+
−
Control
DAC


1.3 V
+
−
Control
DAC


1.3 V
+
−
1
Control
DAC
1.0 V


1.3 V
+
−
0
Control
DAC
1.5 V


1.3 V
+
−
1
Control
DAC
1.25 V


From
Delay
Line
Latch
Input
+
−
Control
DAC

Comparator Samplers: A Brief History

1975

S. P. McCabe III, "A sampling voltage tracker for analyzing high speed waveforms," M.S. thesis, University of California, Los Angeles.

1987-2008

NIST Sampling Waveform Analyzer

2014

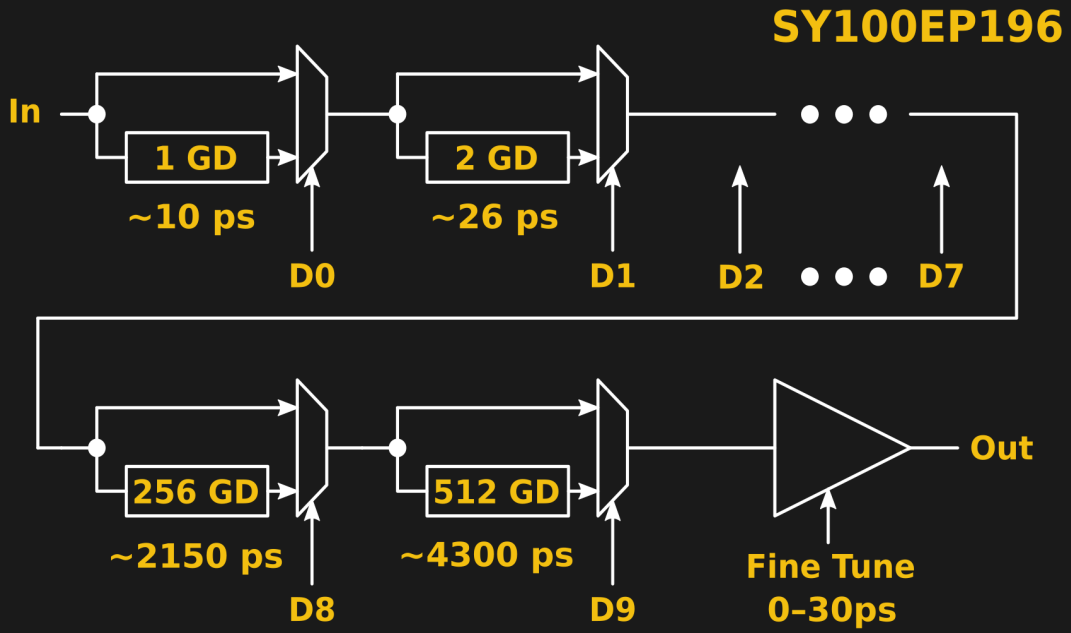
$300 Sampling Scope Kickstarter Campaign (unsuccessful)

Suitable Comparators

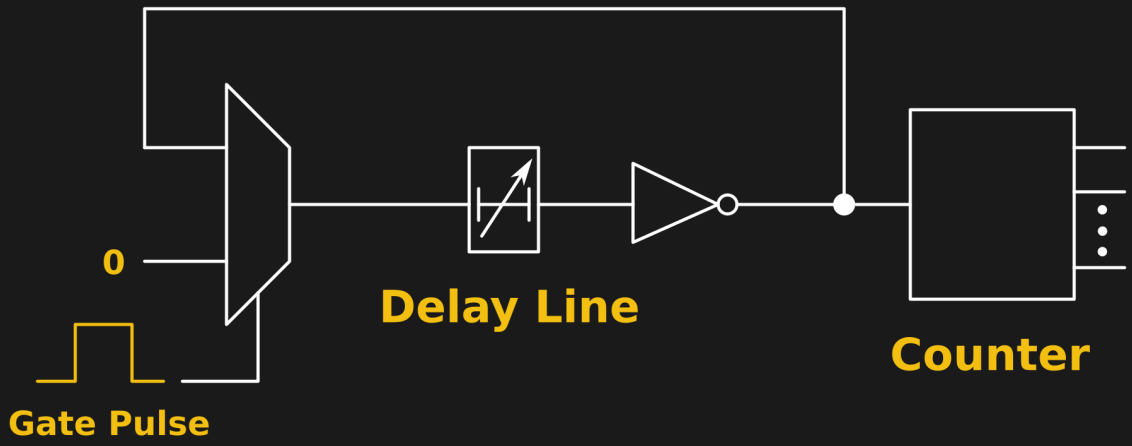
Part	Bandwidth (GHz)*	Cost ($, qty 1)
ADCMP562	1.5	6
ADCMP567	5	8
ADCMP582	8	20
HMC674	9.3	40
HMC874	10	70

Timebase (Delay) Technologies

- Resistor-Varactor
- Voltage Ramp / Comparator
- Gated Ring Oscillator
- FPGA Techniques
- Switched Gate Delays

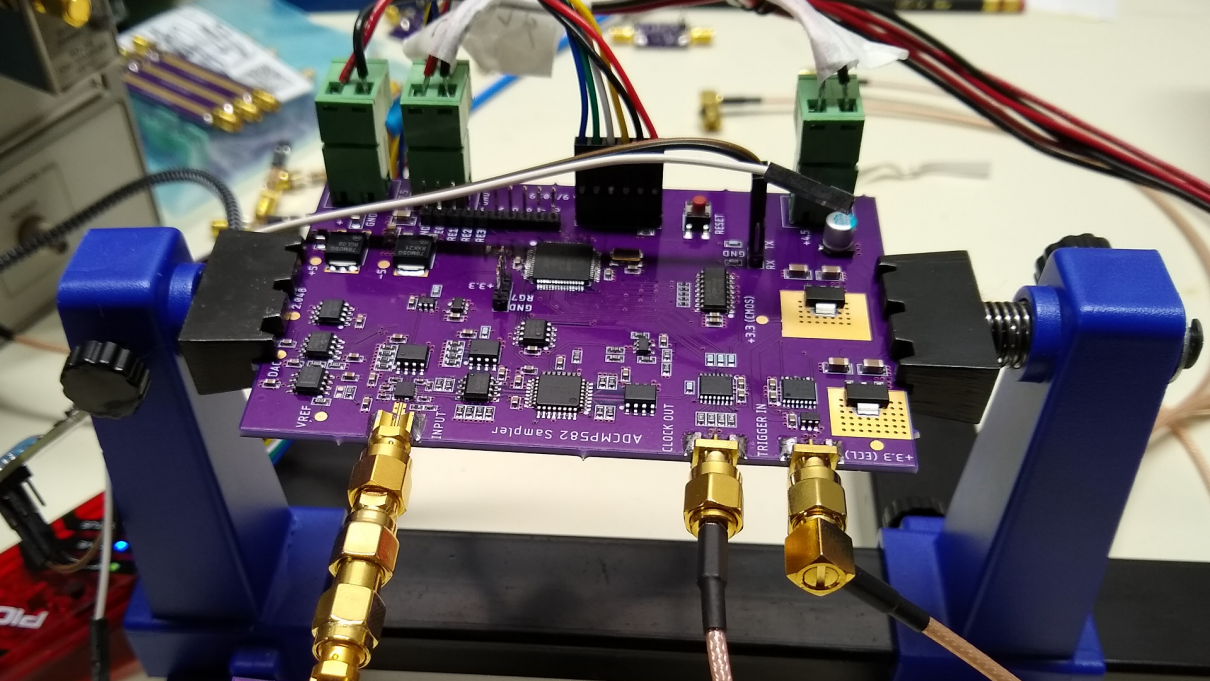

SY100EP196
In
1 GD
~10 ps
D0
2 GD
~26 ps
D1
D2
D7
256 GD
~2150 ps
D8
512 GD
~4300 ps
D9
Out
Fine Tune
0–30ps

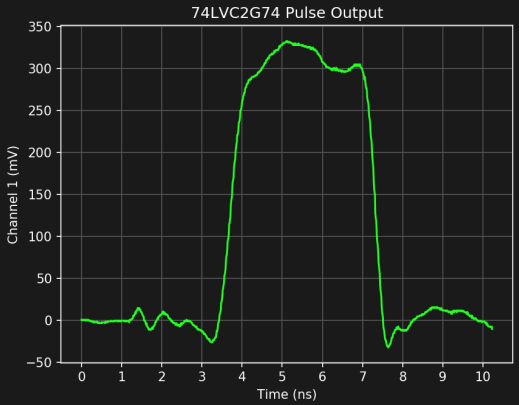
Delay Line Calibration Loop



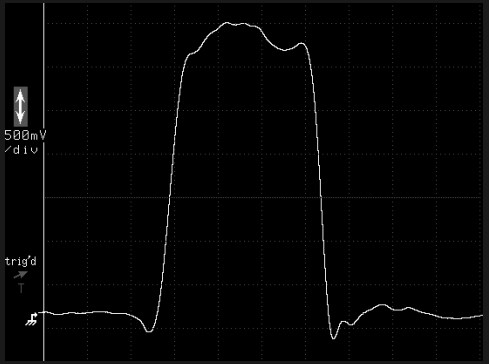
Proto 2

- Input Range: $\pm$ 2 V
- Vertical Resolution: 1 mV
- Rise Time: 48 ps (10%–90%)
- Bandwidth: 7 GHz*
- ET Sample rate: 100 GS/s (500–1000 GS/s ?)
- TDR Resolution: $\approx$5 mm (FR4)
- BOM Cost: $<$ $100 USD

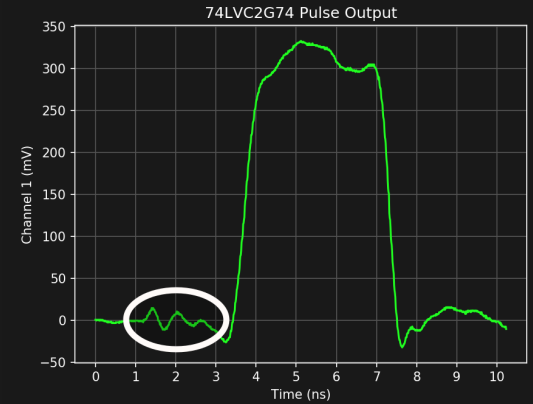

ADCMP582 Sampler
CLOCK OUT
TRIGGER IN
+3.3 (ECL)
+3.3 (CMOS)
RESET
GND
RX
TX
+5
-5
+3.3
GND
R07
R06
R05
R04
R03
R02
R01
R00
VREF
INPUT
DAC
24MB



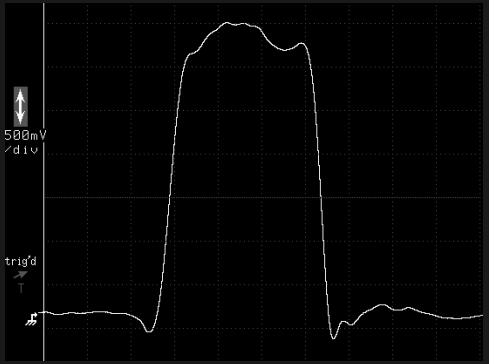
Proto 1



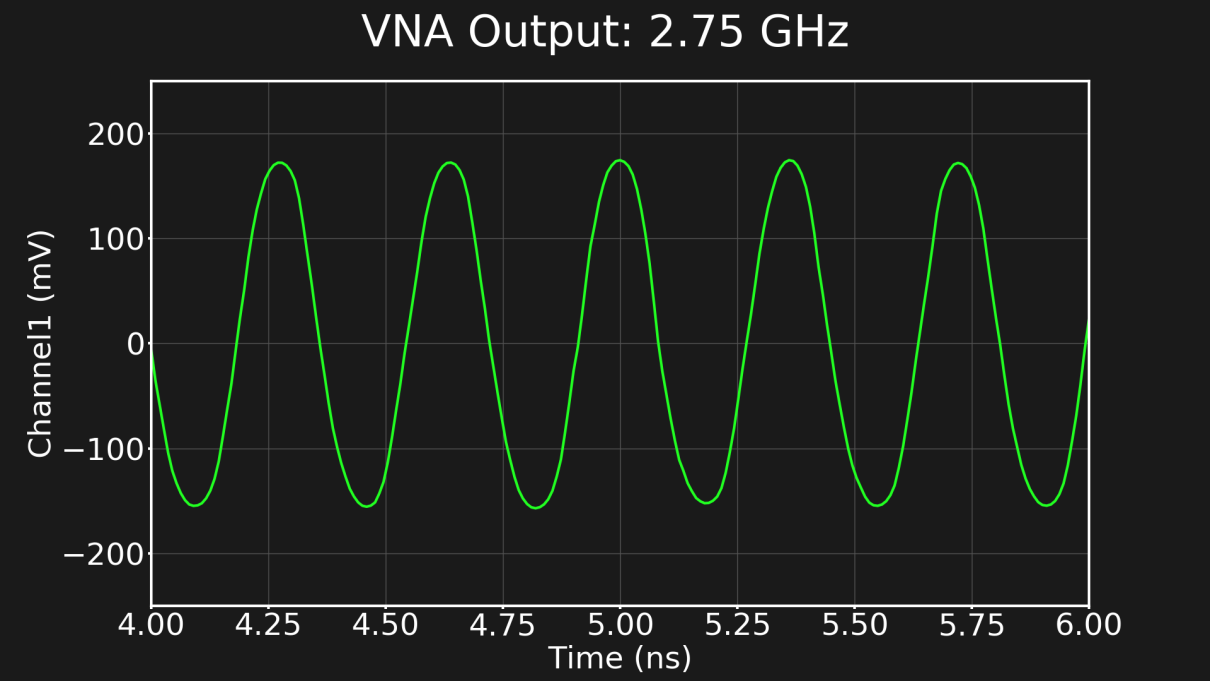
Tek 11801B / SD-24

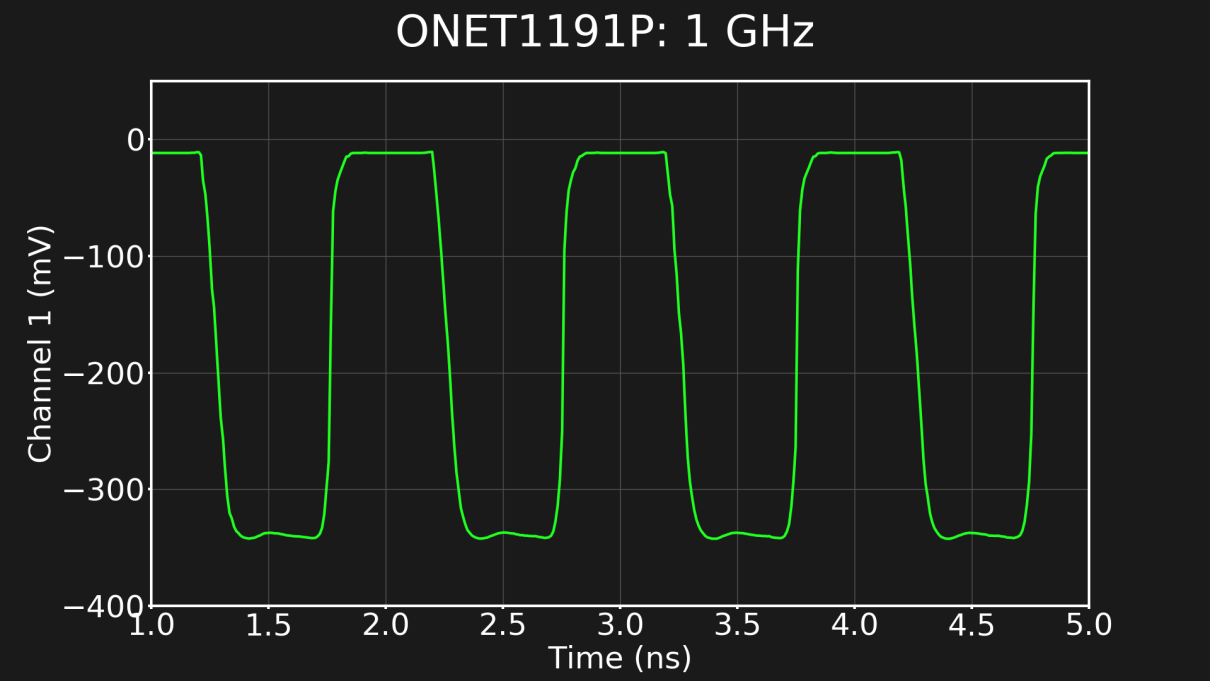


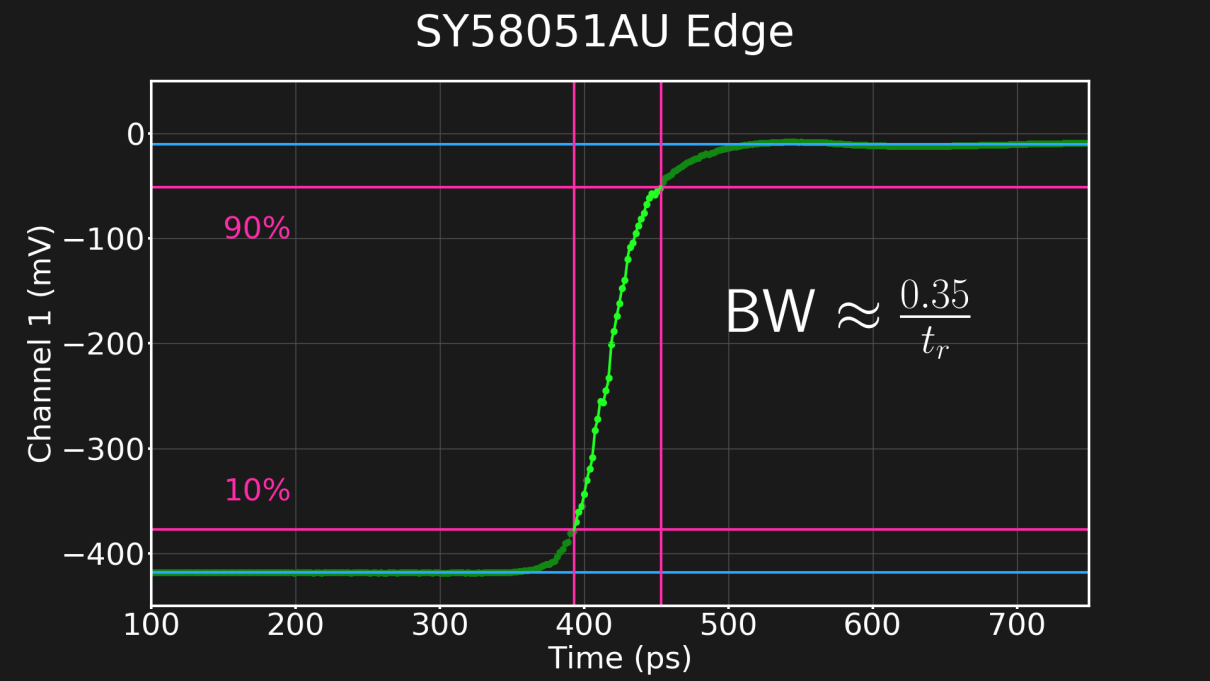
Proto 1

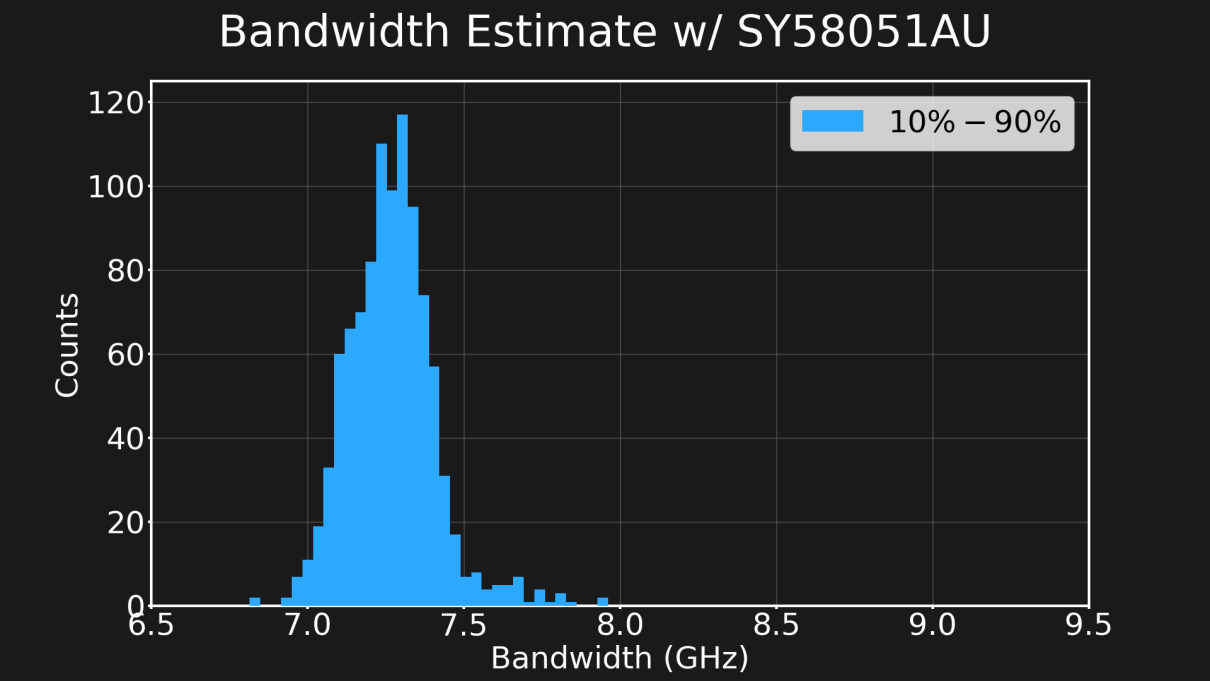


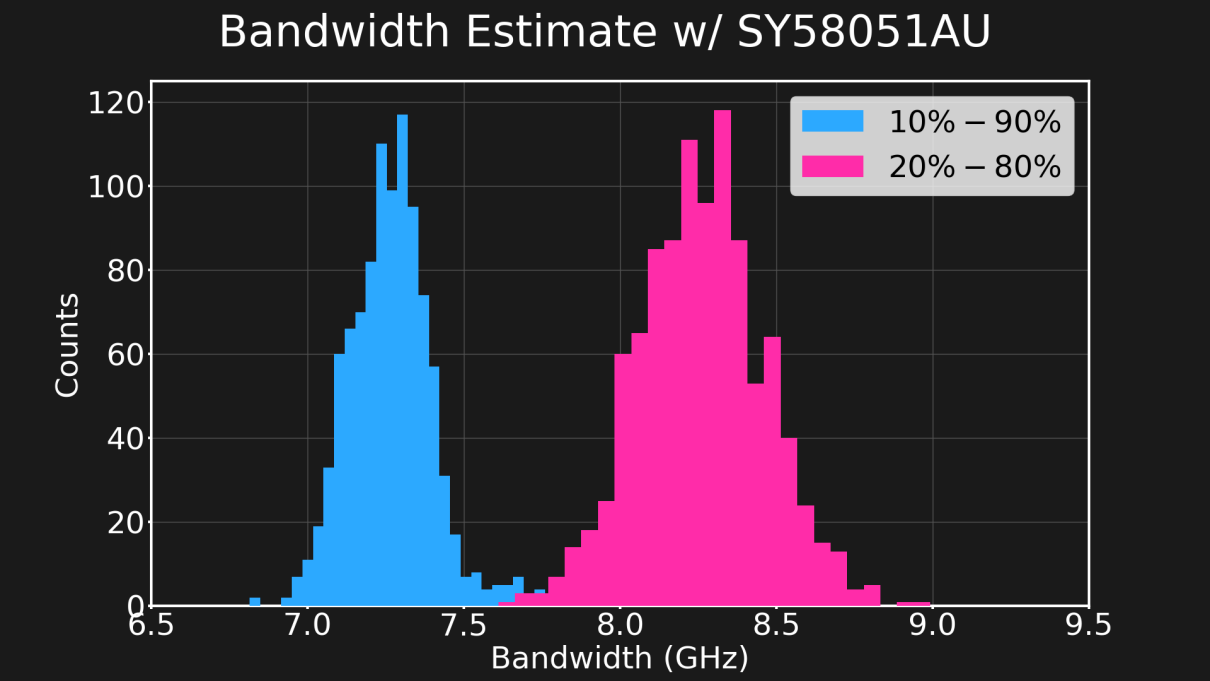
Tek 11801B / SD-24

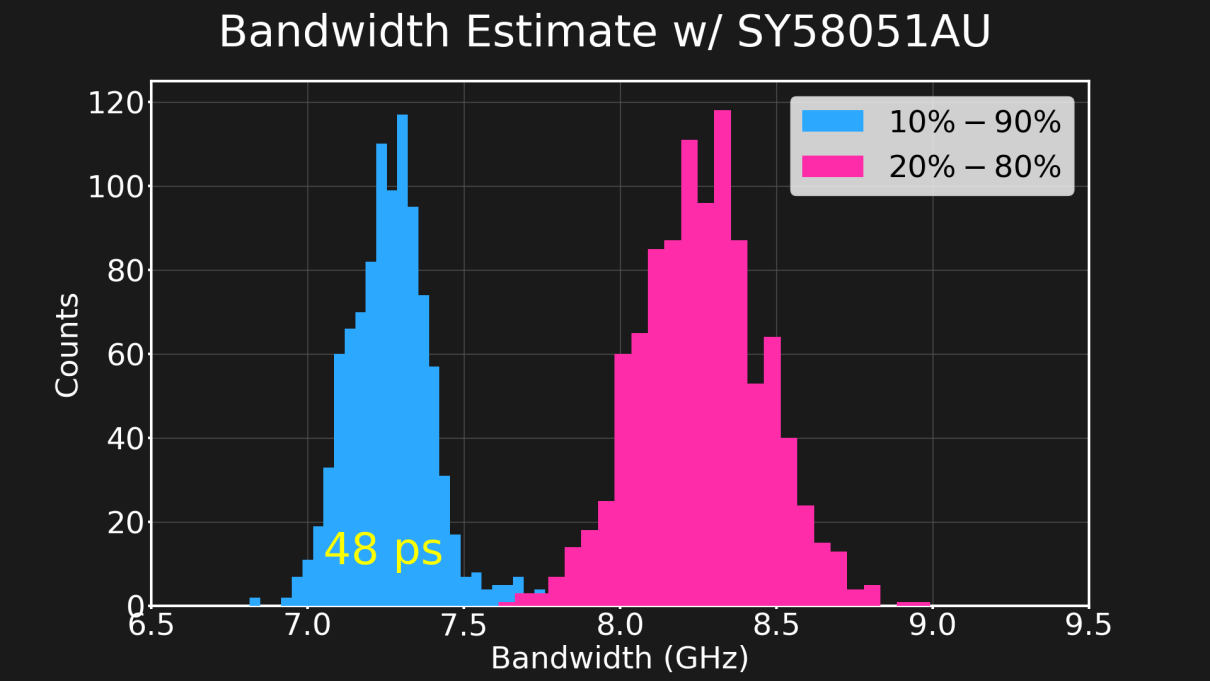

VNA Output: 2.75 GHz
Channel1 (mV)
200
100
0
−100
−200
4.00
4.25
4.50
4.75
5.00
5.25
5.50
5.75
6.00
Time (ns)


ONET1191P: 1 GHz
Channel 1 (mV)
0
−100
−200
−300
−400
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
Time (ns)


SY58051AU Edge
0
−100
−200
−300
−400
Channel 1 (mV)
90%
10%
BW ≈ 0.35 / t_r
100
200
300
400
500
600
700
Time (ps)


Bandwidth Estimate w/ SY58051AU
10% − 90%
Counts
0
20
40
60
80
100
120
6.5
7.0
7.5
8.0
8.5
9.0
9.5
Bandwidth (GHz)


Bandwidth Estimate w/ SY58051AU
10% − 90%
20% − 80%
Counts
0
20
40
60
80
100
120
6.5
7.0
7.5
8.0
8.5
9.0
9.5
Bandwidth (GHz)


Bandwidth Estimate w/ SY58051AU
10% − 90%
20% − 80%
48 ps
Counts
Bandwidth (GHz)
0
20
40
60
80
100
120
6.5
7.0
7.5
8.0
8.5
9.0
9.5

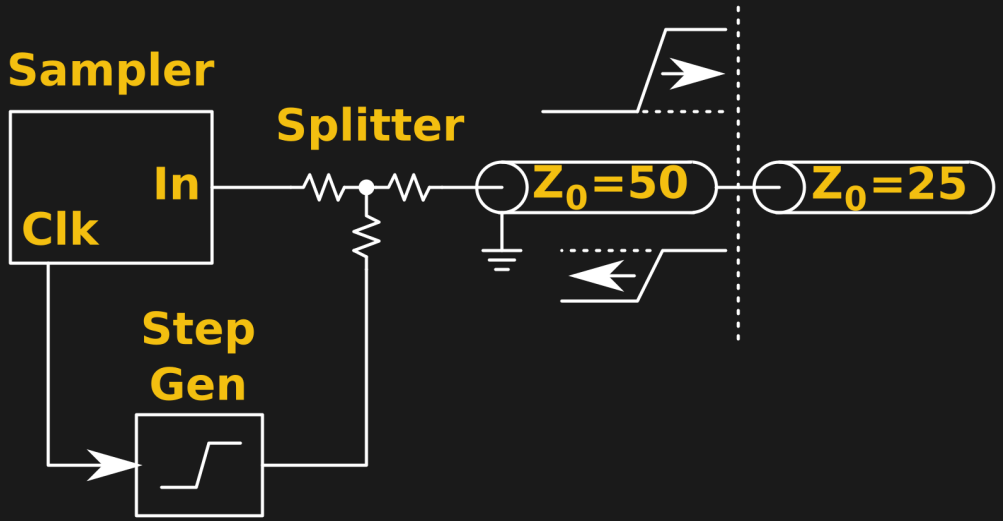
Light travels 14.4 mm in 48 ps

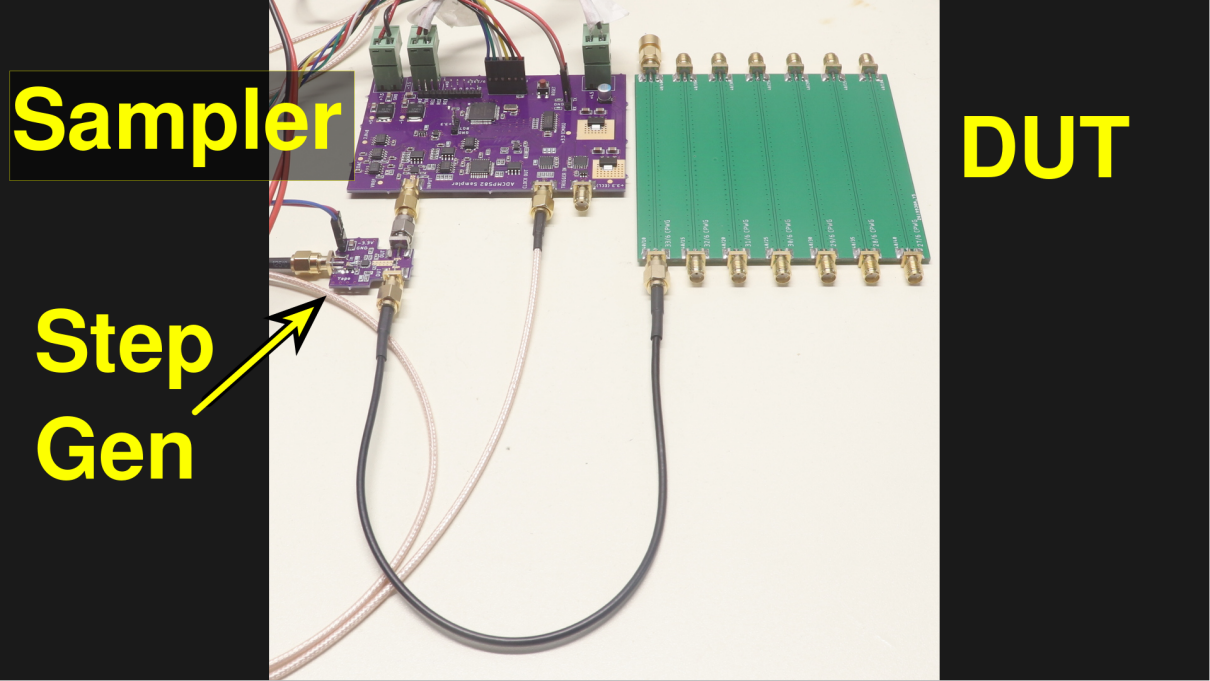
Applications

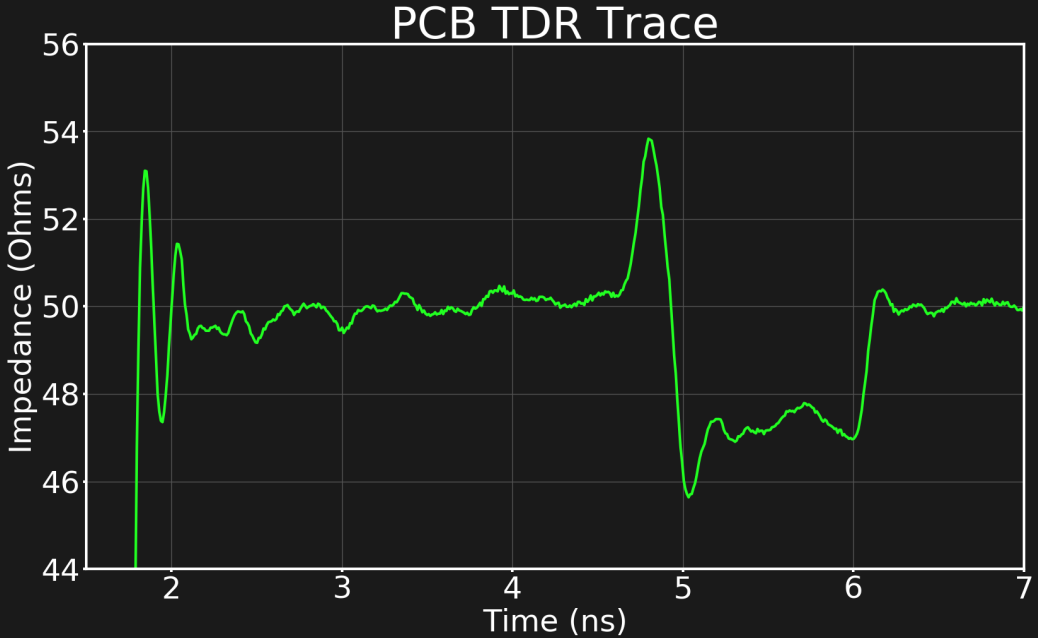
- Time Domain Reflectometry (TDR)
- Eye Diagrams
- Discovery

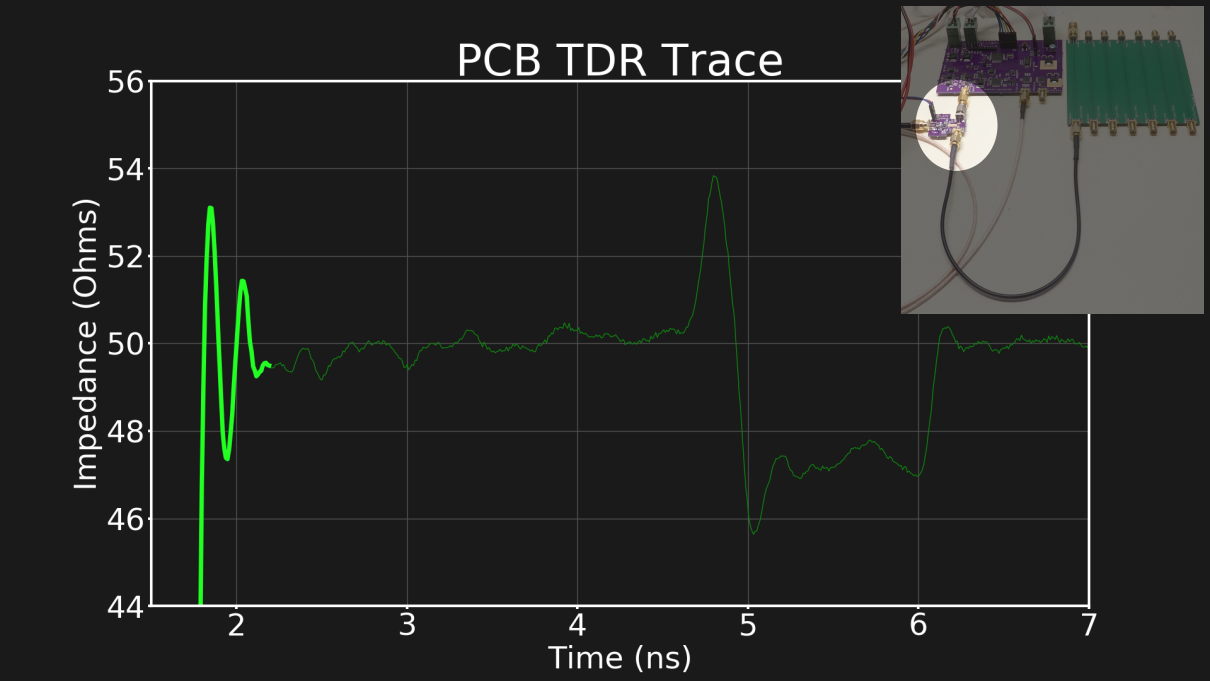
Time Domain Reflectometry (TDR)

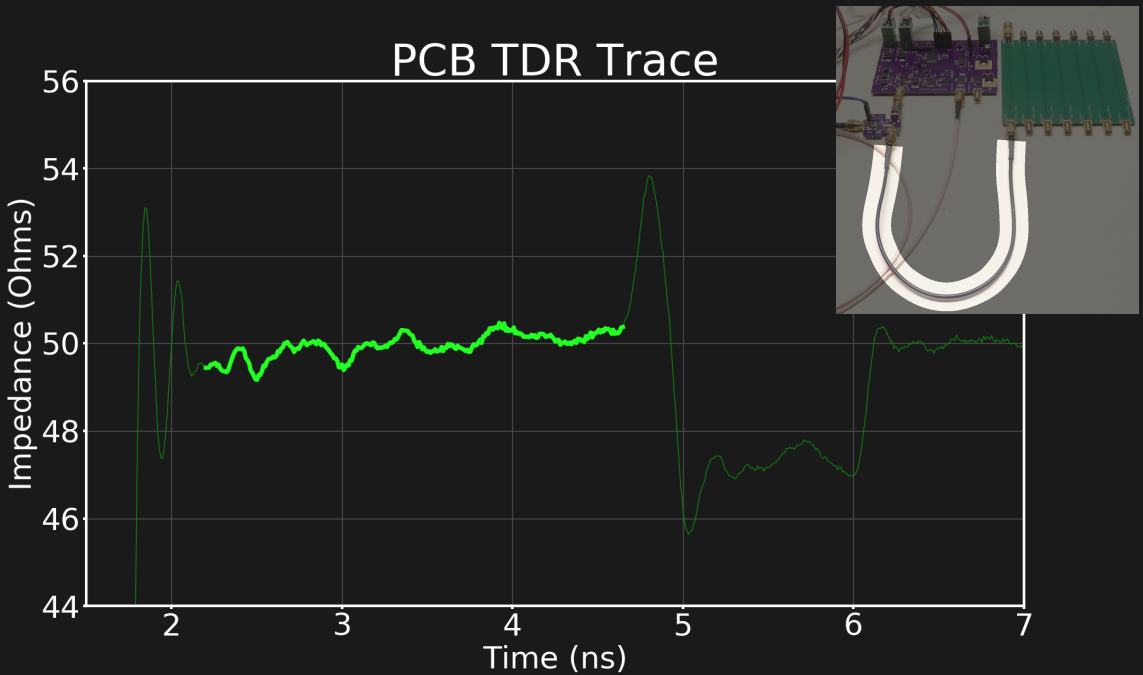
TDR Setup

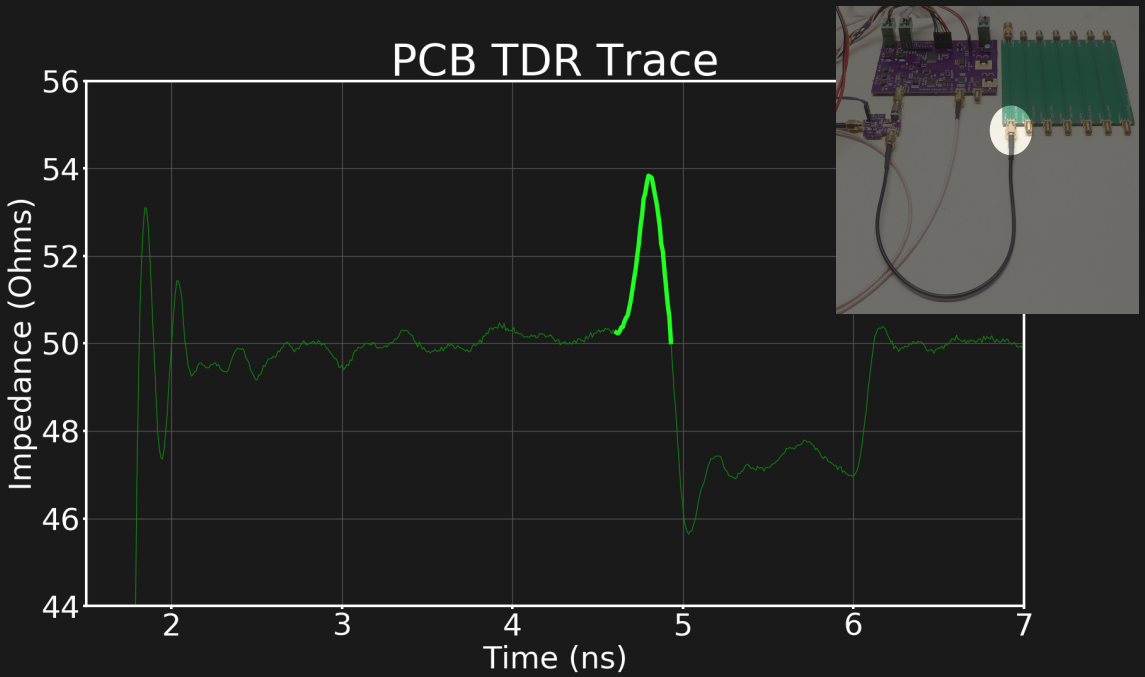


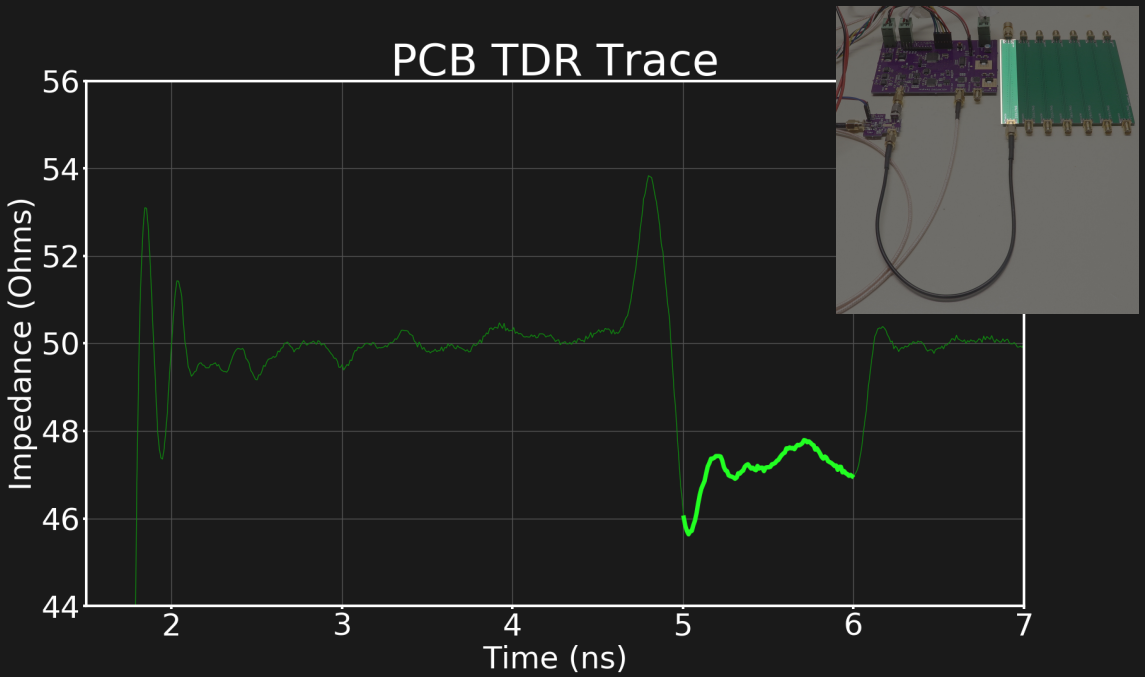

Sampler
DUT
Step
Gen

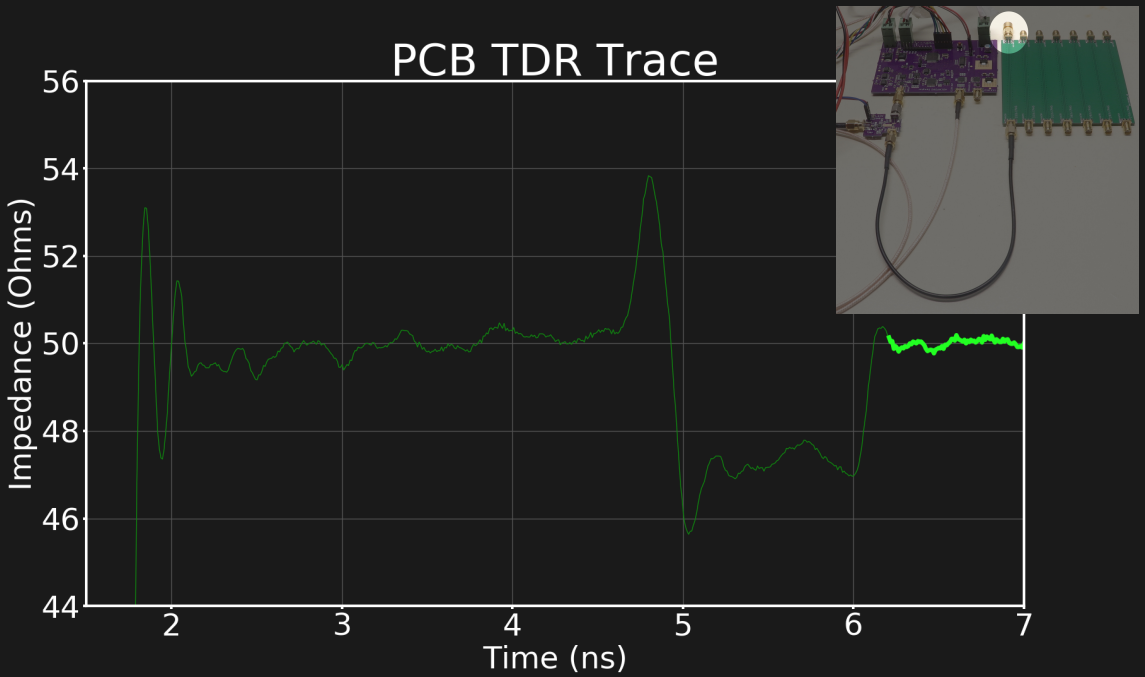

PCB TDR Trace
Impedance (Ohms)
56
54
52
50
48
46
44
2
3
4
5
6
7
Time (ns)


PCB TDR Trace
Impedance (Ohms)
56
54
52
50
48
46
44
2
3
4
5
6
7
Time (ns)


PCB TDR Trace
Impedance (Ohms)
56
54
52
50
48
46
44
2
3
4
5
6
7
Time (ns)


PCB TDR Trace
Impedance (Ohms)
56
54
52
50
48
46
44
2
3
4
5
6
7
Time (ns)


PCB TDR Trace
Impedance (Ohms)
56
54
52
50
48
46
44
2
3
4
5
6
7
Time (ns)


PCB TDR Trace
Impedance (Ohms)
56
54
52
50
48
46
44
2
3
4
5
6
7
Time (ns)

Problem:

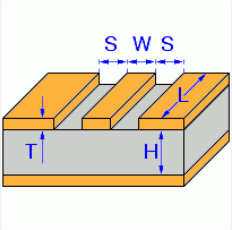
Design a 50-Ohm Coplanar Waveguide

PCB Calculator

Regulators | Track Width | Electrical Spacing | TransLine | RF Attenuators | Color Code | Board Classes

Transmission Line Type:

- Microstrip Line
- Coplanar wave guide
- Coplanar wave guide with ground plane
- Rectangular Waveguide
- Coaxial Line
- Coupled Microstrip Line
- Stripline
- Twisted Pair



Substrate Parameters

Er:	4.5	...
TanD:	0.02	...
Rho:	1.72e-08	...
H:	60	mil
T:	1.4	mil
mu Rel C:	1	

Component Parameters:

Frequency:	1	GHz

Physical Parameters:

W:	32	mil
S:	6	mil
L:	319.67	mil

Analyze | Synthesize

Electrical Parameters:

Z0:	50.0085	Ohm
Ang_l:	14.8861	Degree

Results:

ErEff:	2.33093
Conductor Losses:	0.00865152 dB
Dielectric Losses:	0.016567 dB
Skin Depth:	2.0873 µm

Coplanar Waveguide Calculators

50-Ohm CPWG; OSH Park 2-layer stackup, 6 mil gaps, 50-mil vias

30.5 mil trace

- AppCAD

31.7 mil trace

- TXLINE

32 mil trace

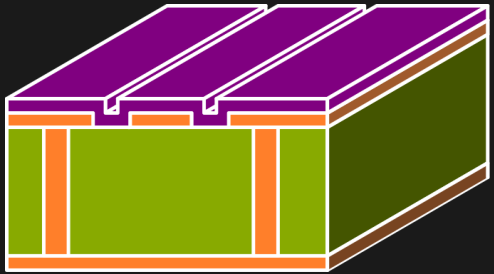
- KiCAD PCB Calculator
- 1 Web Calculator

38.7 mil trace

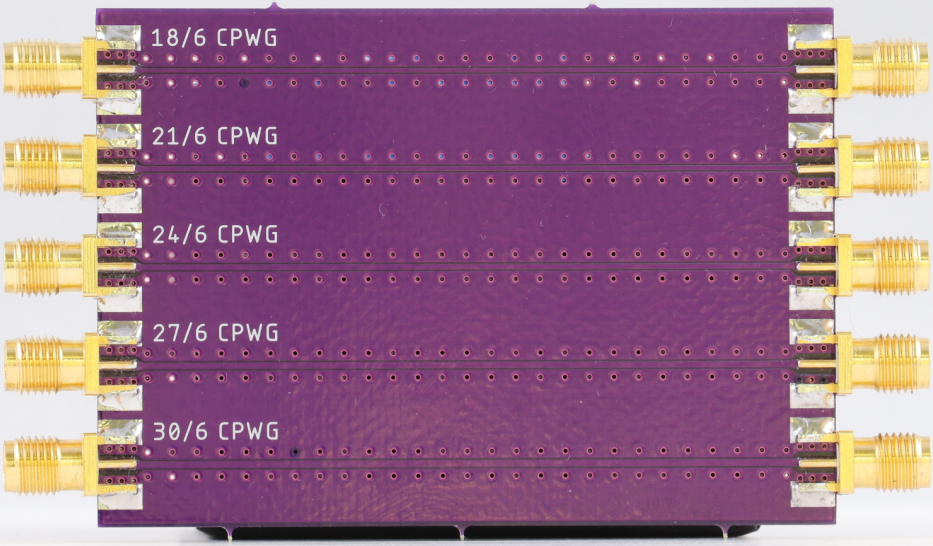
- Sonnet Lite

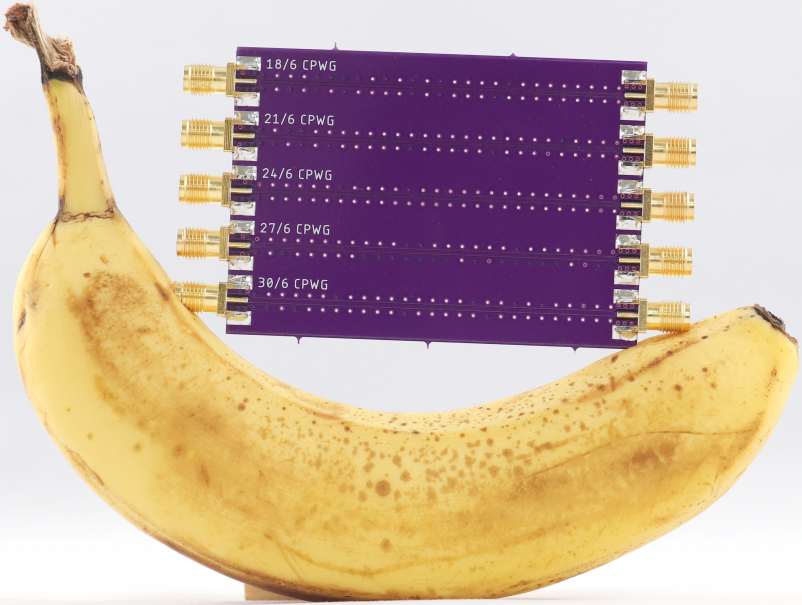
40 mil trace

- Saturn Toolkit
- 4 Web Calculators

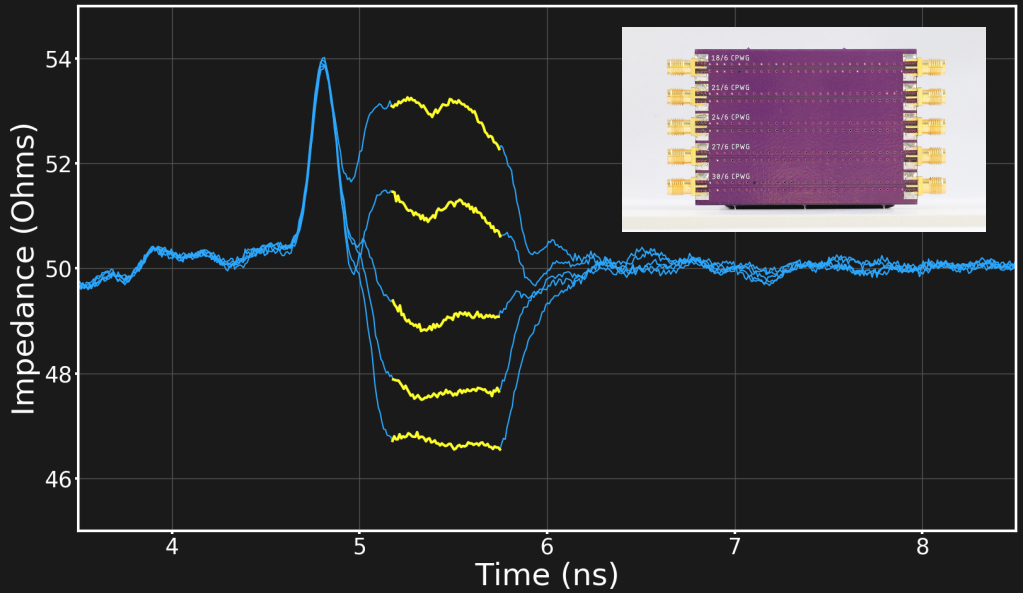


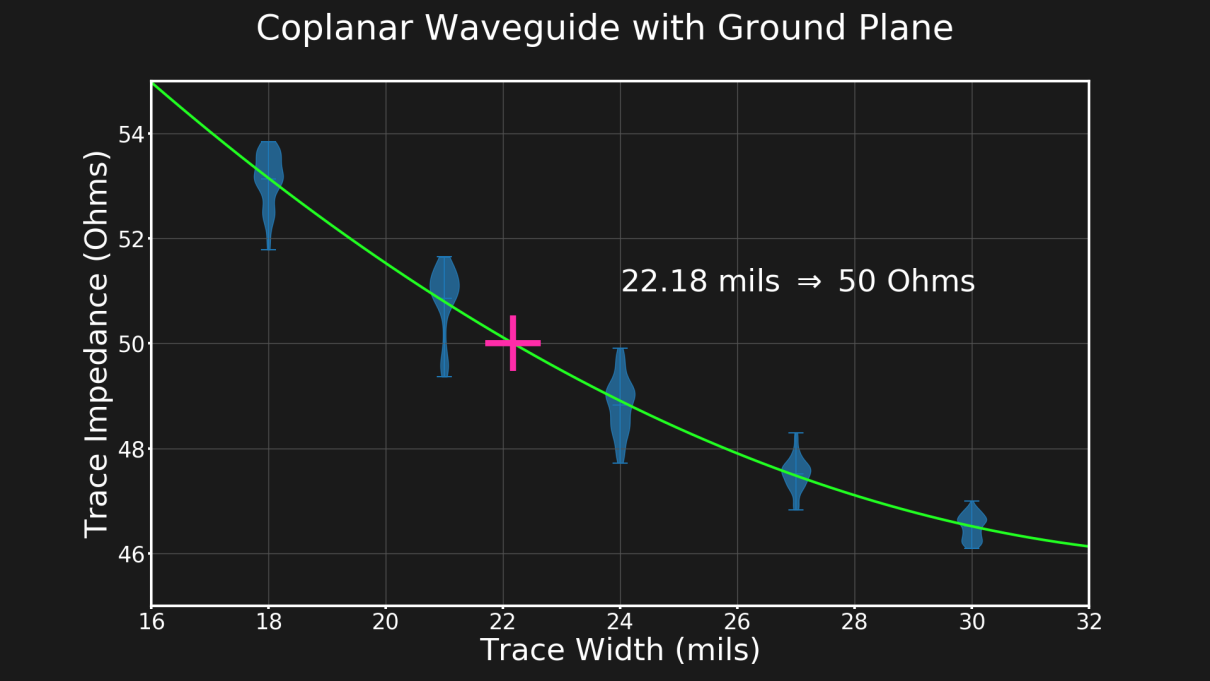
As Designed $\neq$ As Built

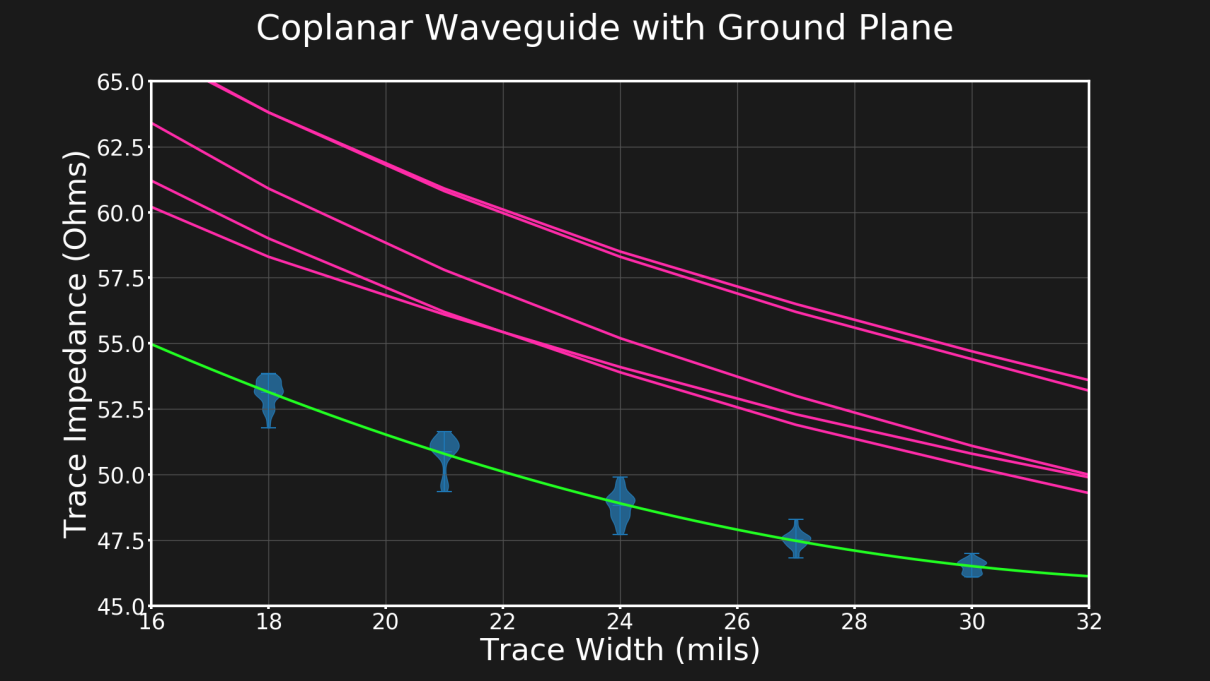

18/6 CPWG
21/6 CPWG
24/6 CPWG
27/6 CPWG
30/6 CPWG


18/6 CPWG
21/6 CPWG
24/6 CPWG
27/6 CPWG
30/6 CPWG

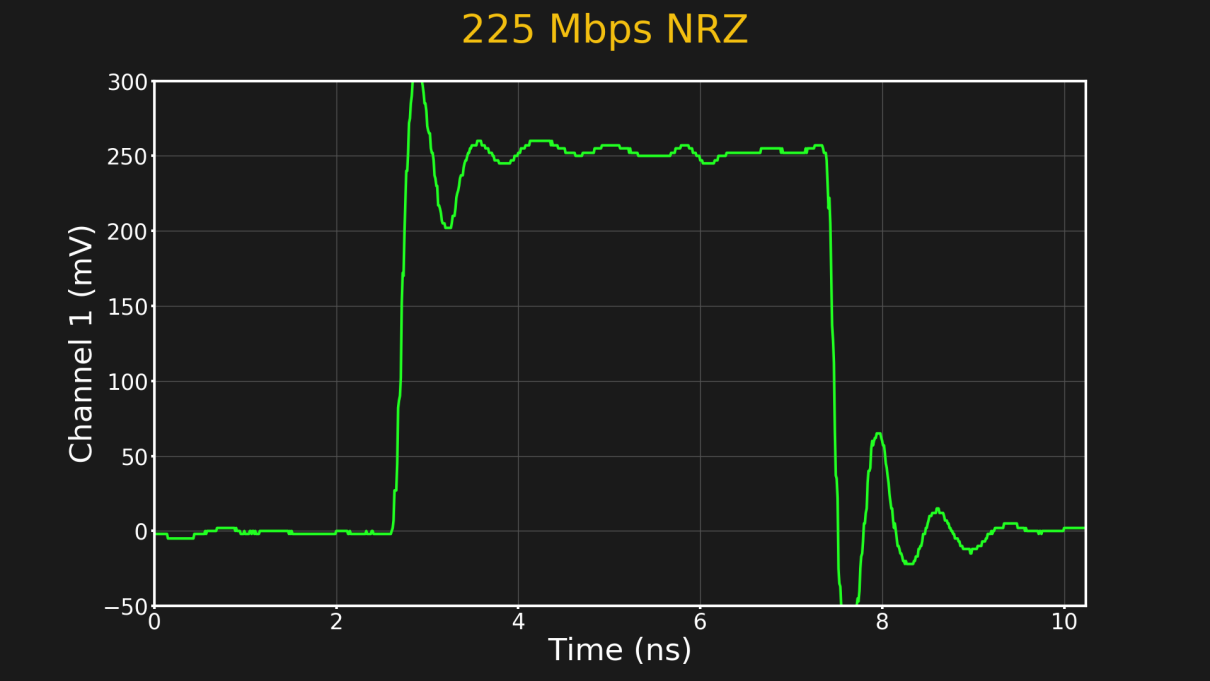
Coplanar Waveguide with Ground Plane



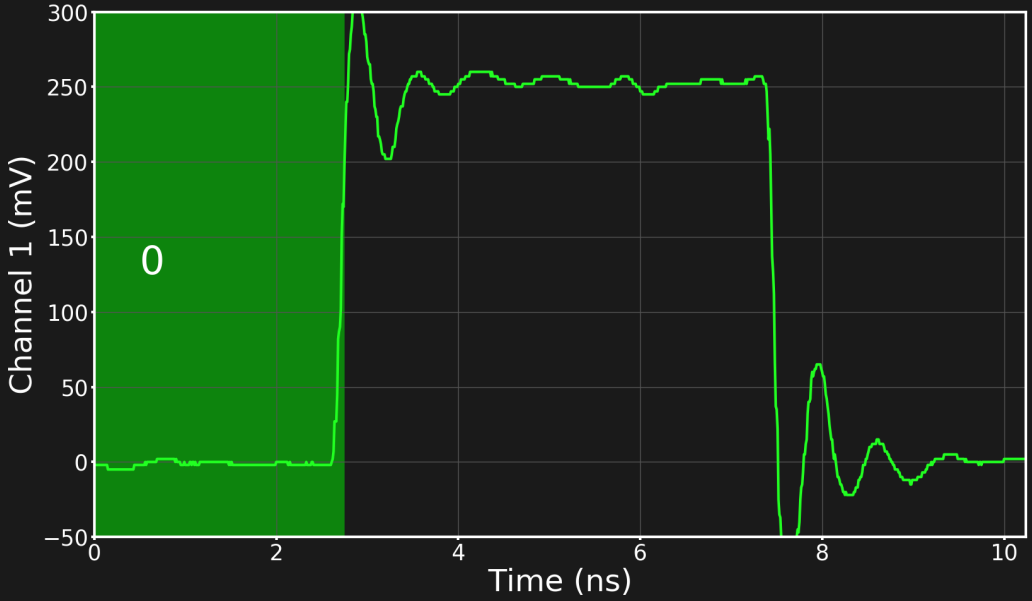

Coplanar Waveguide with Ground Plane
22.18 mils ⇒ 50 Ohms
Trace Impedance (Ohms)
Trace Width (mils)
54
52
50
48
46
16
18
20
22
24
26
28
30
32

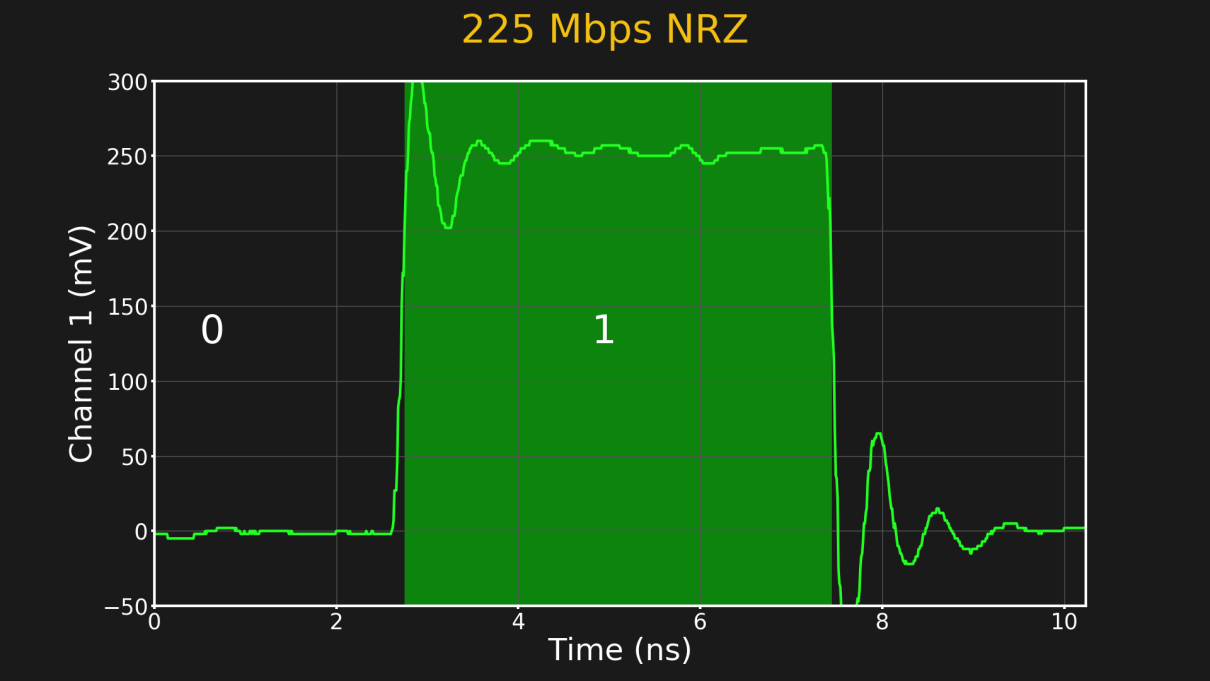

Coplanar Waveguide with Ground Plane
Trace Impedance (Ohms)
65.0
62.5
60.0
57.5
55.0
52.5
50.0
47.5
45.0
16
18
20
22
24
26
28
30
32
Trace Width (mils)

EYE DIAGRAMS

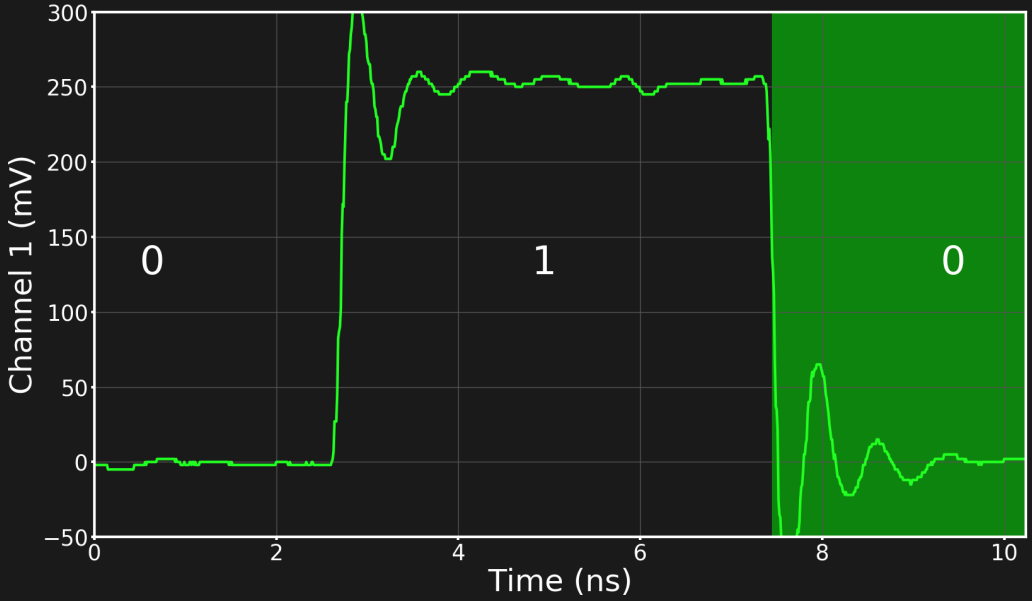

225 Mbps NRZ
Channel 1 (mV)
300
250
200
150
100
50
0
−50
0
2
4
6
8
10
Time (ns)

225 Mbps NRZ

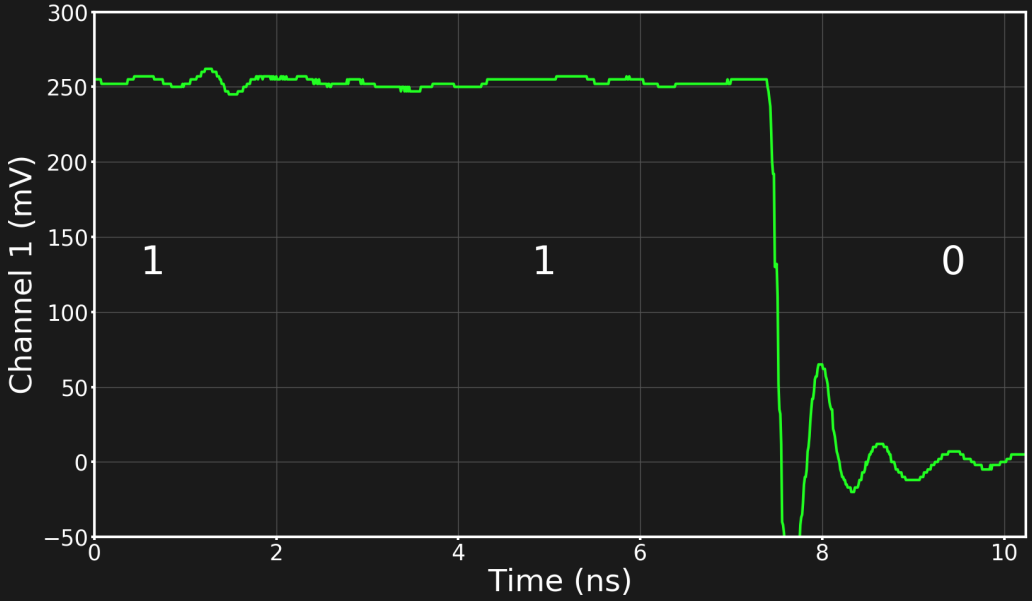



225 Mbps NRZ
Channel 1 (mV)
300
250
200
150
100
50
0
−50
0
1
0
2
4
6
8
10
Time (ns)

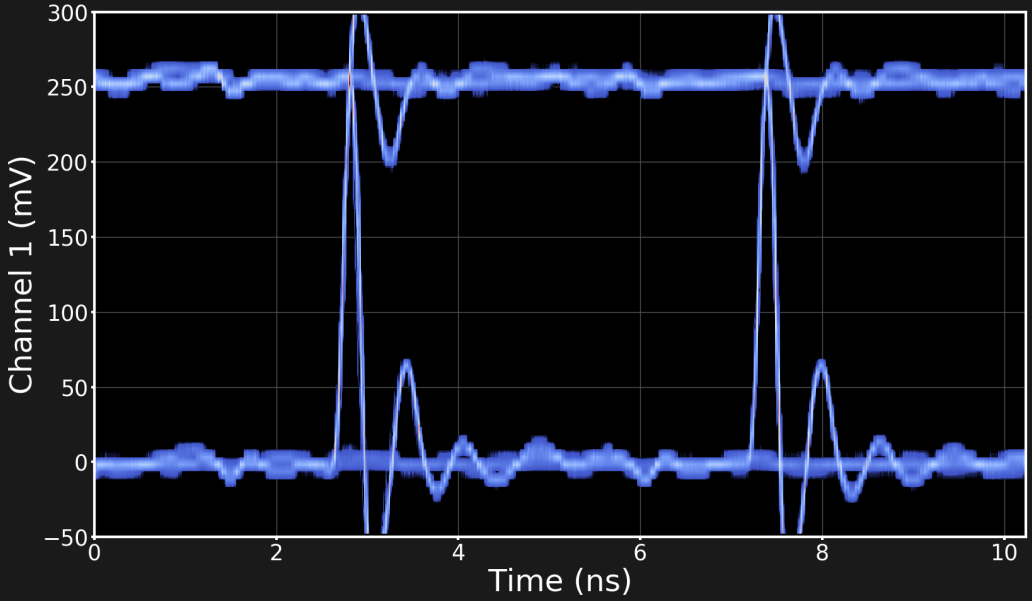
225 Mbps NRZ



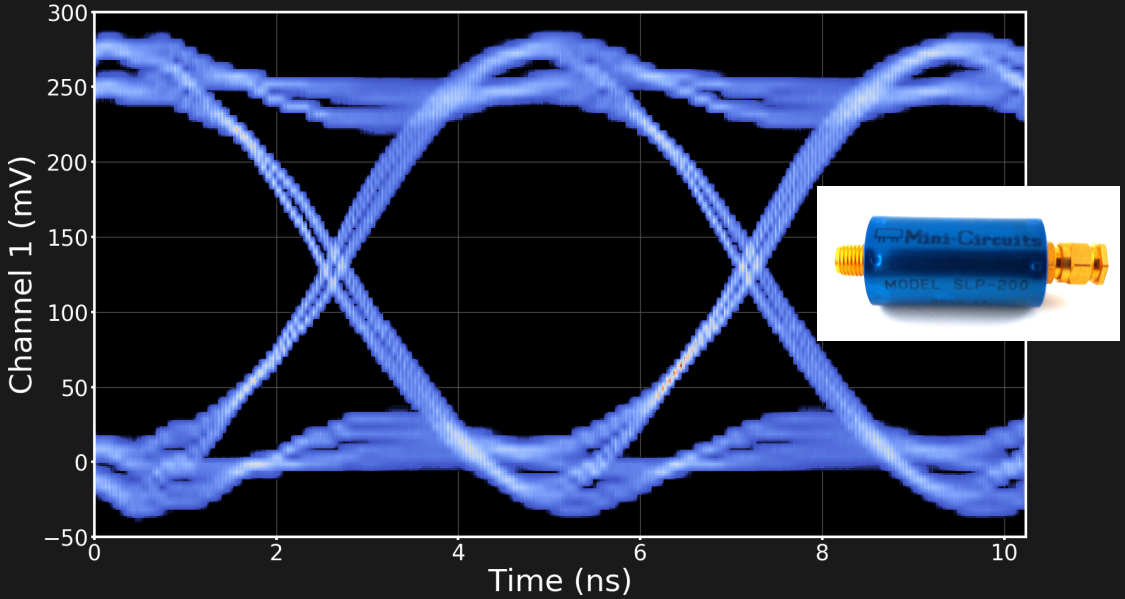
225 Mbps NRZ



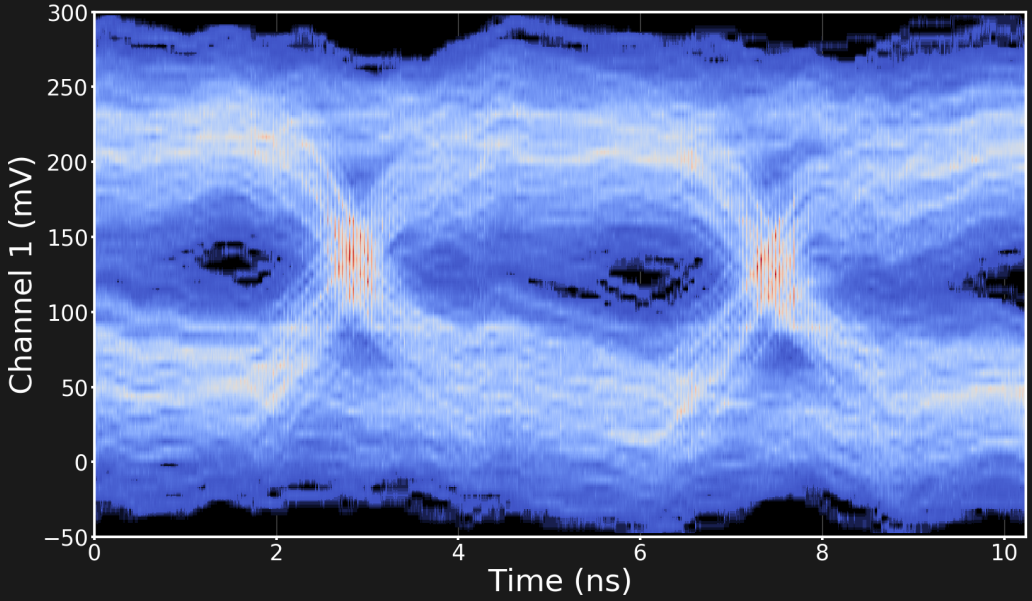
225 Mbps NRZ PRBS-11 (Reference)



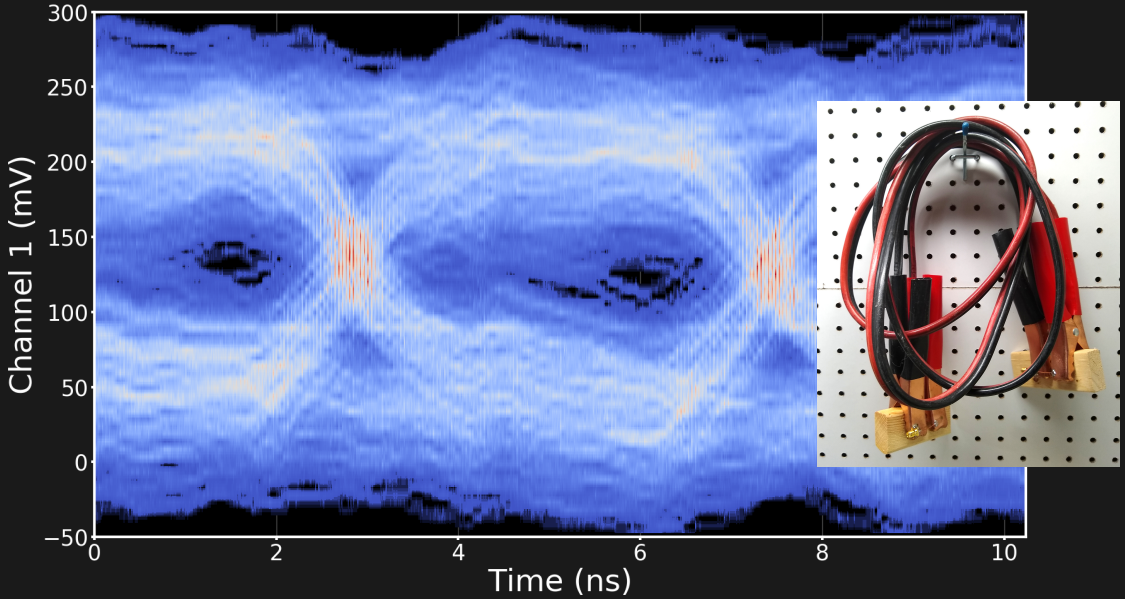
225 Mbps NRZ PRBS-11 (200 MHz LPF)



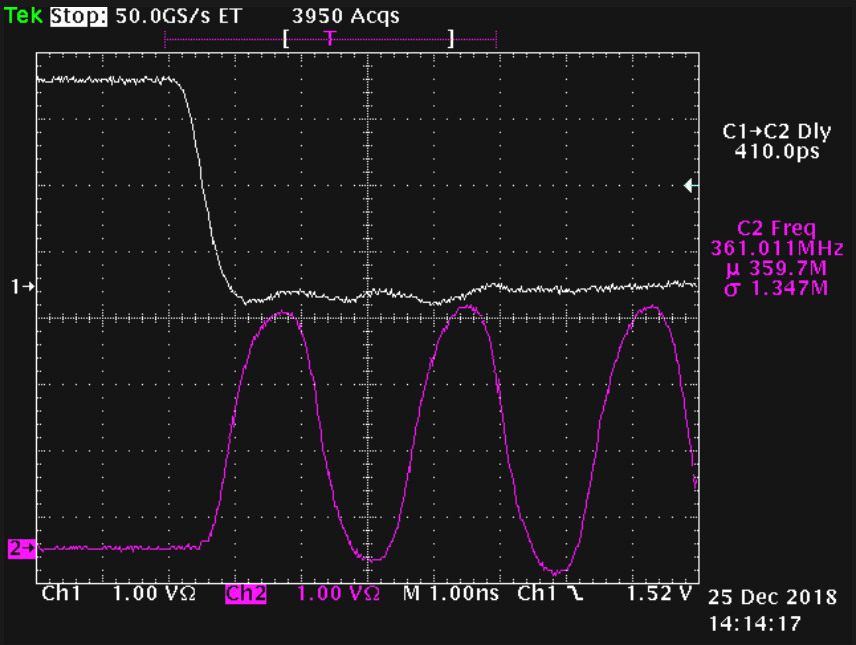
225 Mbps NRZ PRBS-11

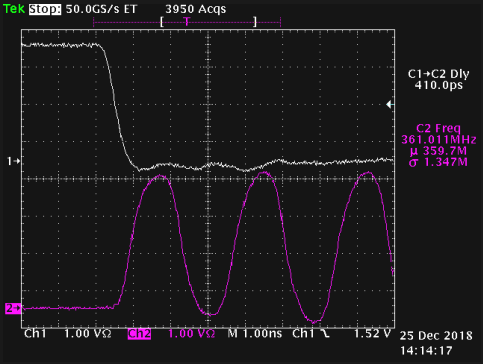


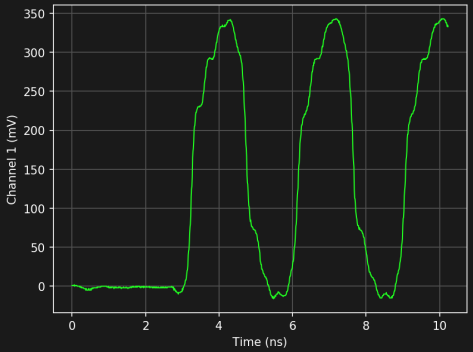
225 Mbps NRZ PRBS-11 (Jumper Cables)

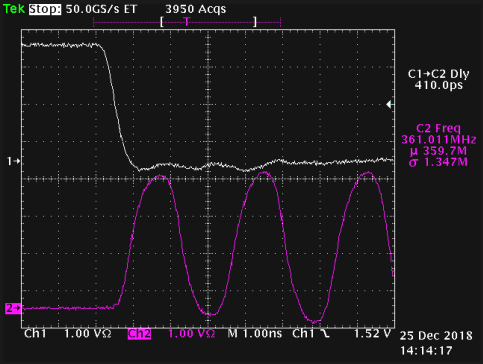


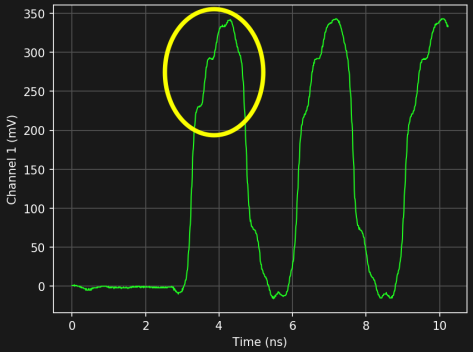
DISCOVERY

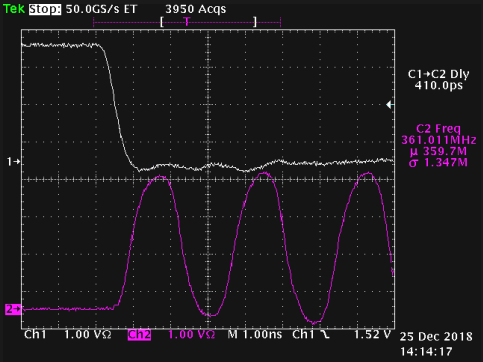

Tek Stop: 50.0GS/s ET 3950 Acqs
C1→C2 Dly
410.0ps
C2 Freq
361.011MHz
μ 359.7M
σ 1.347M
1→
2→
Ch1 1.00 VΩ Ch2 1.00 VΩ M 1.00ns Ch1 ∿ 1.52 V
25 Dec 2018
14:14:17

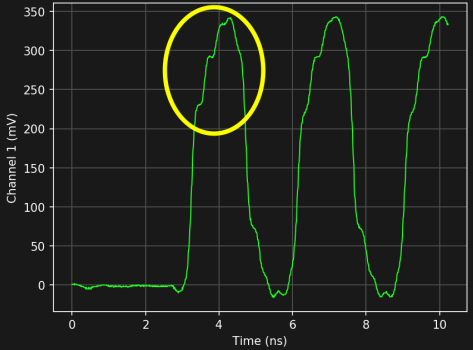

Tek Stop: 50.0GS/s ET 3950 Acqs
C1→C2 Dly
410.0ps
C2 Freq
361.011MHz
μ 359.7M
σ 1.347M
Ch1 1.00 VΩ Ch2 1.00 VΩ M 1.00ns Ch1 ∖ 1.52 V
25 Dec 2018
14:14:17


Channel 1 (mV)
Time (ns)
350
300
250
200
150
100
50
0
0
2
4
6
8
10


Tek Stop: 50.0GS/s ET 3950 Acqs
C1→C2 Dly
410.0ps
C2 Freq
361.011MHz
μ 359.7M
σ 1.347M
Ch1 1.00 VΩ Ch2 1.00 VΩ M 1.00ns Ch1 ∖ 1.52 V
25 Dec 2018
14:14:17


Channel 1 (mV)
Time (ns)
350
300
250
200
150
100
50
0
0
2
4
6
8
10





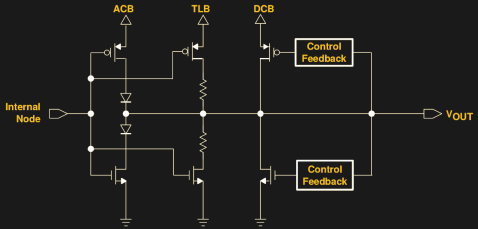


Figure 1. ULTTL Output Structure

Image courtesy of Texas Instruments (SCEA027A)

What Next?

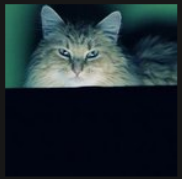
Proto 3

- Better Name
- 32-bit CPU
- Timebase Enhancements
- Integrated Power Supply (USB)
- KiCAD ?

Applications

- UWB RADAR
- LiDAR

Thanks!

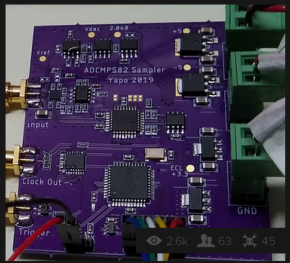


K.C. Lee

Bil Herd

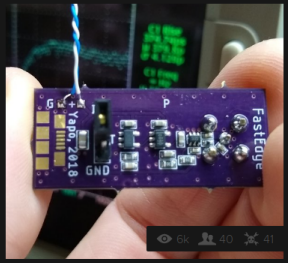
Get In Touch!

hackaday.io/ted.yapo
@tedyapo



8 GHz Sampling Oscilloscope

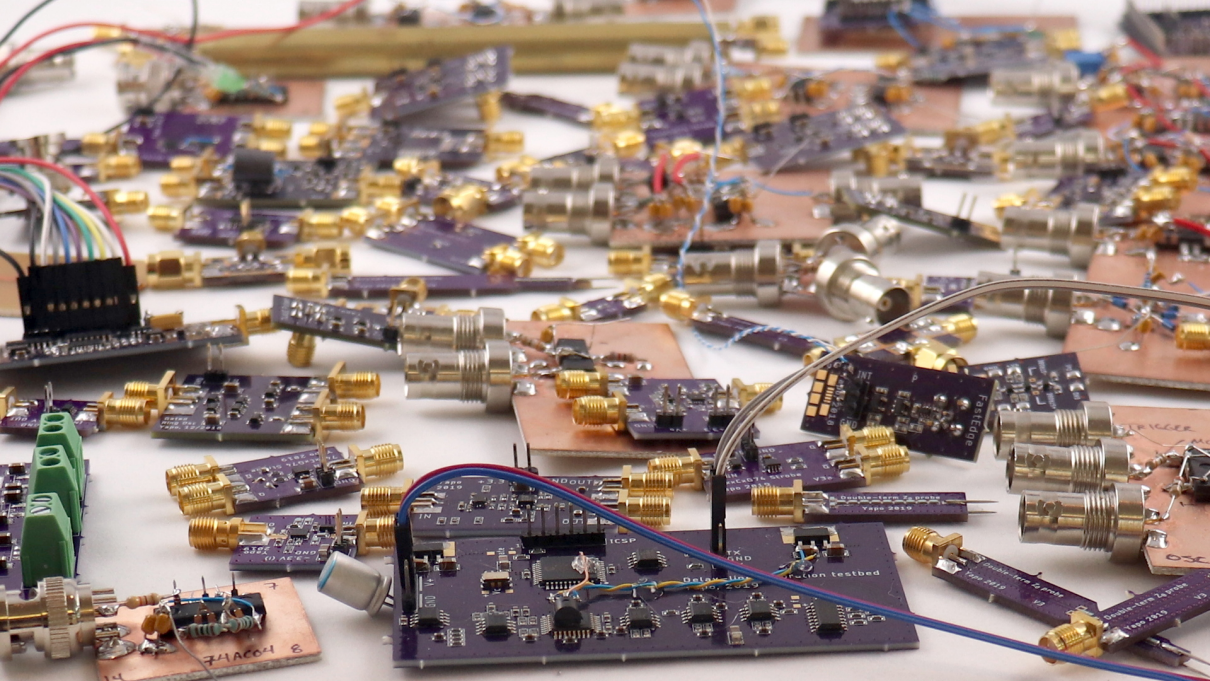
Ted Yapo



The Rise and Fall of Pulses

Ted Yapo

What's the impedance, Kenneth?
CPWG Test
Yapo
20198924
vias: 50 mils
CPWG Test
Yapo 2019
vias: 75 mils
20198828
$0.20
$0.20


ICSP
Delay line
Oscilloscope Z2 probe
Type 2819
FastEdge
TRIGGER
74AC04