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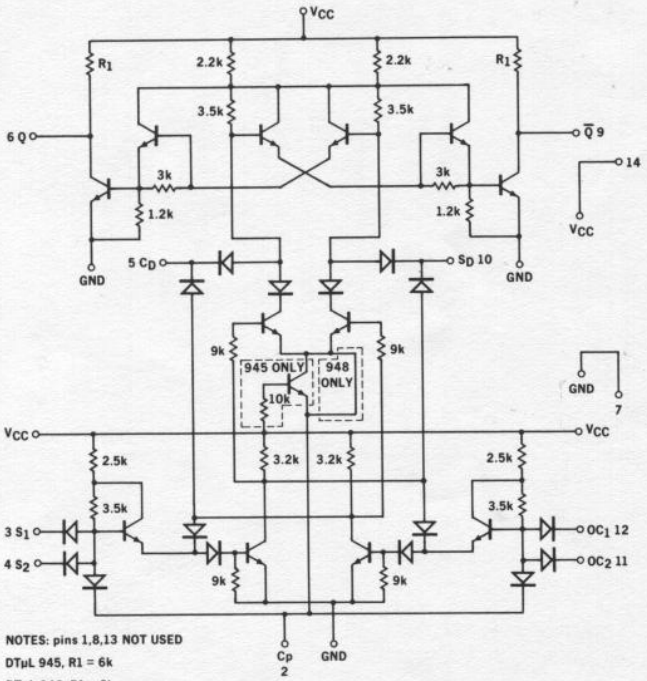
DTμL 945 • DTμL 948 - CLOCKED FLIP - FLOP

The DTμL 945 and DTμL 948 Clocked Flip-Flops are directly-coupled units operating on the "master-slave" principle. Information enters the "master" while the Trigger input voltage is high and transfers to the "slave" when the Trigger input voltage goes low. Since operation depends only on voltage levels, any sort of waveshape having the proper voltage levels may be used as a trigger signal. Rise and fall times are irrelevant.

The DTμL 945 and DTμL 948 have an improved direct Set and Clear design which allows unhampered asynchronous entry irrespective of signals applied to any other inputs. The direct inputs always take precedence, thus simplifying the design of arbitrarily preset ripple-counters and other minimum hardware applications.

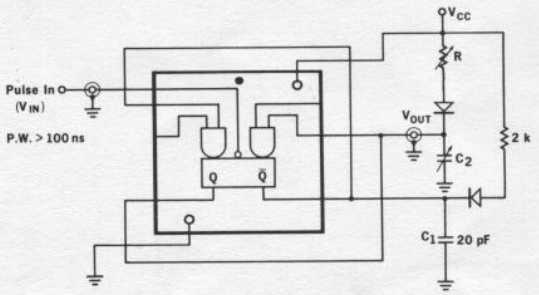
Output buffers provide isolation between the "slave" and the output load, thereby enhancing immunity to signal line noise. The DTμL 945 incorporates the standard 6 k-ohm output pull-up resistor, while the DTμL 948 features a 2 k-ohm output pull-up resistor for improved rise times, and matched delay between rising and falling outputs for capacitive loading up to 100 pF.

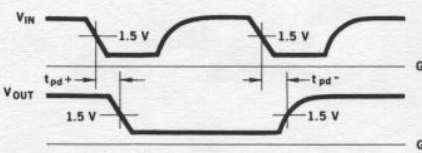
SCHEMATIC DIAGRAM



NOTES: pins 1,8,13 NOT USED
DTμL 945, R1 = 6k
DTμL 948, R1 = 2k

tpd TEST CIRCUIT



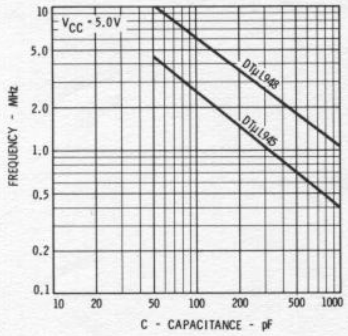


C_1 and C_2 includes Probe and Jig Capacitance

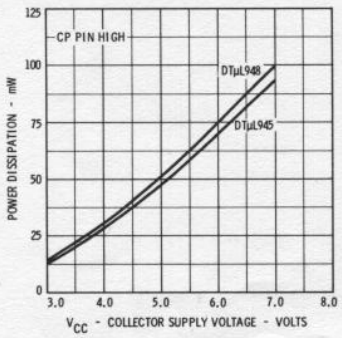
(V_{CC} = 5 V, T = 25°C)

		R	C_2	Min.	Max.
t_{pd+}	945	2.00 k	30 pF	35 ns	75 ns
t_{pd-}	945	330 Ω	30 pF	35 ns	75 ns
t_{pd+}	948	2.00 k	30 pF	20 ns	65 ns
t_{pd-}	948	330 Ω	30 pF	30 ns	75 ns

TYPICAL MAXIMUM BINARY COUNTING RATE VERSUS CAPACITY



TYPICAL POWER DISSIPATION VERSUS V_{CC}



TYPICAL tpd VERSUS CAPACITANCE