

- * Feather M0 – either rx or tx
 - * WS connected to pin 0
 - * CLK connected to pin 1
 - * SD connected to pin 9
 - * (no MCLK)
- * Feather M4 – simultaneous rx and tx
 - * WS connected to pin 10
 - * CLK connected to pin 1
 - * SDI connected to pin 12
 - * SDO connected to pin 11
 - * (MCLK connected to pin 0)
- *STM32F405 – either rx or tx
 - * CLK connected to pin 1/Tx
 - * WS connected to pin 10
 - * SD connected to pin 11
 - * (MCLK connected to pin 6)

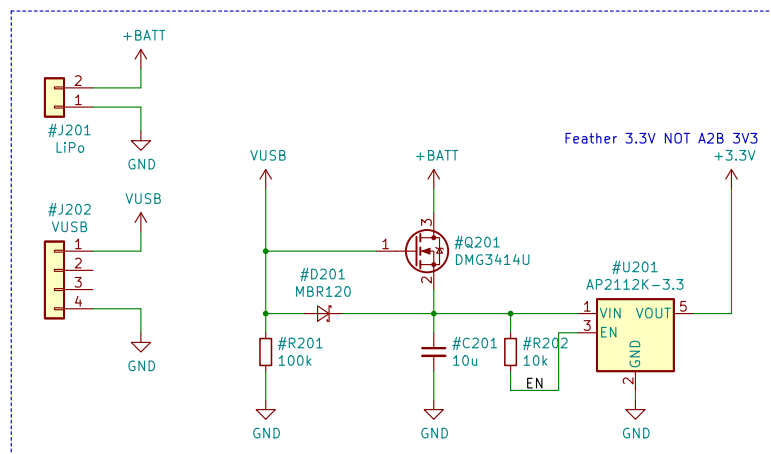
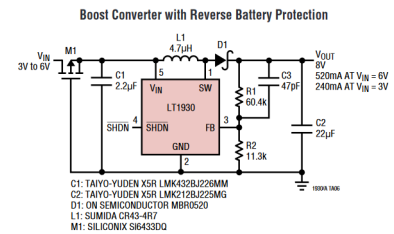
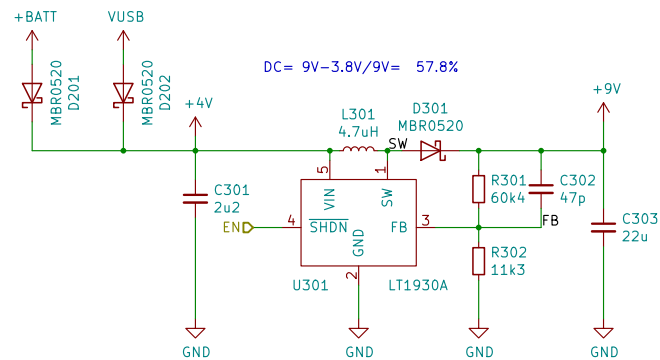
-- I2S Spec --
 - original Spec -
 Official Typical
 "continuous serial clock (SCK)" - "Bitclock (BCLK)"
 "Word Select (WS)" - "left-right clock (LRCLK)" or "frame sync" (FS)
 "Serial Data (SD)" - "SDATA,SDIN,SDOUT,DACDAT,ADCDAT"

- additional lines -
 "Master Clock (MCLK)" - Typical: 256 x WS (LRCLK,FS)

- Bitclock -
 Bitclock is product of sample rate, number of bits, channels.
 e.g. 44.1kHz x 16 x 2 = 1.4112MHz

-WS clock-
 WS clock tells whether channel 0 or channel 1 is being sampled and is typically the sampling frequency e.g. 44.1kHz

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Power Select on Feather (not on this PCB)

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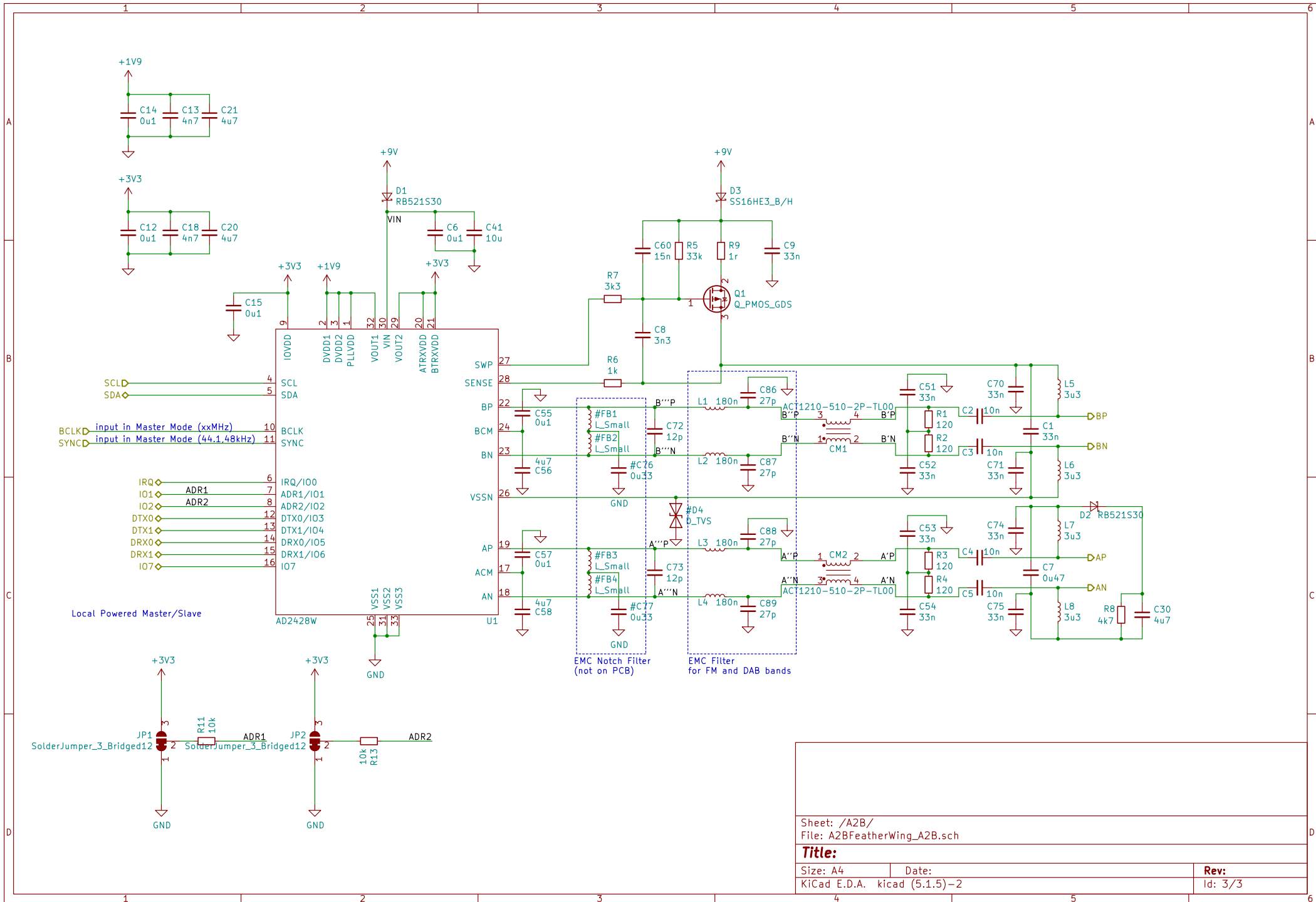
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