

Errata to ADS78xx Devices Running Internal Serial Data Clock Option

1 Associated Devices

Devices covered by this errata document are listed in Table 1.

DEVICE DOCUMENT NUMBER ADS7806 **SBAS021** ADS7807 **SBAS022 ADS7808 SBAS018** ADS7809 **SBAS017** ADS7812 **SBAS042** ADS7813 **SBAS043** ADS7824 **SBAS044** ADS7825 **SBAS045**

Table 1. Covered Devices

2 Indication

The devices listed in Table 1 include an option to use an internal serial data clock, to clock conversion results from the analog-to-digital converter (ADC) to the user host processor or microcontroller. This option is enabled by setting the device to serial mode while holding the EXT/INT pin low. The mechanism that clocks out the serial data is derived from an internal oscillator, and is also used as the conversion clock.

The internal conversion clock may not be active on the first application of the read and convert (R/\overline{C}) pin after initial power up of the device. This condition, if present, does not allow the serial clock output to go active during the first conversion cycle.

3 Hardware and Software Workarounds

The hardware workaround for this condition is to initiate a power-down reset by cycling power to the device. Care must be taken to ensure no input voltages (analog or digital) exceed the stated data sheet limits.

The software work around for this condition is to initialize a dummy conversion cycle by pulsing R/C low during system initialization. Subsequent conversions can begin after a delay of the maximum conversion time followed by the minimum acquisition time of the ADC. The specific timing requirements for conversion and acquisition times are listed in the data sheets shown in Table 1.

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