Using the CD4047A in COS/MOS Timing Applications

by J. Paradise

Many applications exist today for COS/MOS multivibrators– both oscillators and one-shots–in analog and digital circuits. The requirements for these applications vary widely in such parameters as voltage range, temperature stability, power dissipation, drive capability, and external-component cost. No design is optimum for all of the above considerations. However, the RCA-CD4047A Monostable/Astable Multivibrator fulfills the needs of most applications in this timing area. It can function as either an oscillator or one-shot with many additional features, and will meet the power dissipation, stability, and speed requirements of most COS/MOS systems.

This Note compares some simpler types of oscillator circuits with the CD4047A in both theoretical and actual performance, and provides application information on the CD4047A which should prove useful to COS/MOS circuit and system designers.

COS/MOS DISCRETE RC OSCILLATOR

The simplest type of RC-oscillator is shown in Fig. 1. It consists of two inverters (which may be taken from standard

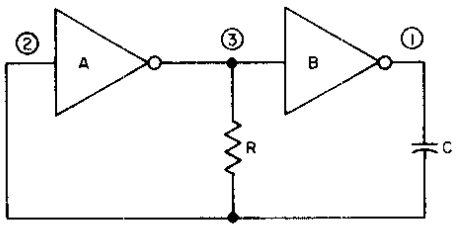

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Fig. 1 – Simplest COS/MOS RC oscillator.

RCA COS/MOS parts, i.e., CD4007A, CD4001A, CD4011A, etc.) and a single resistor and capacitor. The operating waveforms for this circuit are shown in Fig. 2.

The circuit operates as follows: depending on the output levels of inverters A and B, at any instant C will be charging or discharging through R. When the waveform at point (2) in the circuit passes through the transfer voltage of inverter A, this inverter will switch and cause inverter B to switch. Subsequently, the waveform at point (2) would be exponentially

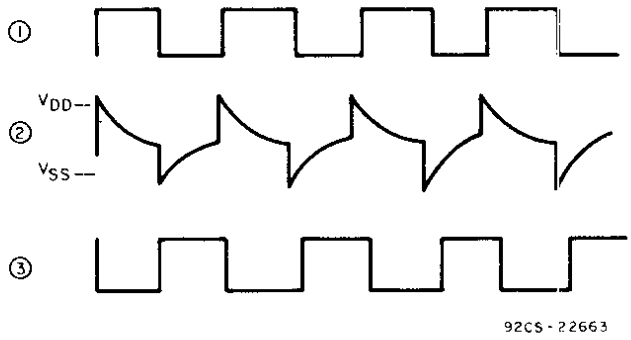

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Fig. 2 – RC-oscillator operating waveforms.

increasing or decreasing with discontinuities equal in magnitude to V_{DD} during the instant of switching. However, since point (2) is protected by a standard input-protection circuit common to COS/MOS devices, the waveform is clamped at one diode voltage drop above V_{DD} and below V_{SS}. (Refer to waveforms in Figs. 2 and A1). The calculations for the period of this multivibrator circuit are shown in Appendix A; the final equation for the period T is

$$T = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_D)^2} \qquad (1)$$

where V_{TR} is the switching or transfer point of the inverter, and V_D is the diode forward voltage drop.

Equation (1) shows that the period of the multivibrator, T, is sensitive to changes in V_{DD}, as illustrated by the graph of time period, T, vs transfer voltage as a function of V_{DD} in Fig. 3. In addition to the strong dependence of actual time period on the V_{DD} chosen, the graph also illustrates that, for a given V_{DD}, a full transfer voltage spread of 30 to 70 per cent of V_{DD} (unit-to-unit worst-case variations) yields a change in time period of about 10 per cent from the nominal 50-per-cent transfer-voltage percentage values.

The above analysis is valid only at low frequencies (i.e., less than 50 kHz). As the multivibrator frequency approaches this value, other considerations must be taken into account:

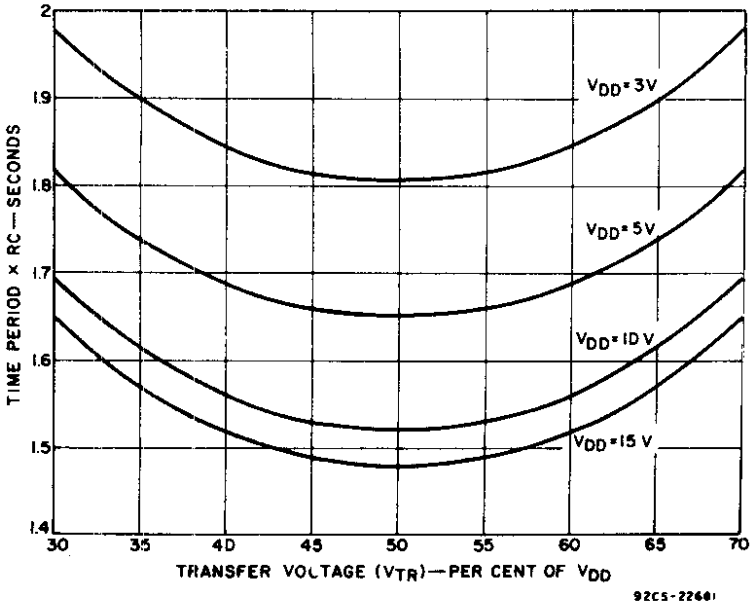

Fig. 3 – Discrete RC-oscillator time period as a function of transfer voltage.

1. The input protection circuit has a V_{DD} diode with a finite resistance and capacitance; the diode will discharge at the rate associated with this small time constant.

2. In the negative direction, there is a diode as well as a series protection resistor (1 to 3 kilohms); the time constant of this diode is even longer than that of the V_{DD} diode.

3. The propagation delay of the inverters used is added to the time period during each charge and discharge cycle. Since the delay is a function of V_{DD}, small changes in V_{DD} at high frequencies will cause the time period to vary.

4. There is a finite output impedance associated with the inverter which is in series with the external timing resistor. Since this output impedance also changes with V_{DD}, at high frequencies where the external resistor becomes small, the multivibrator stability decreases with small variations in V_{DD}.

The negative features of the input protection circuit can be partially compensated for by the addition of a resistor, R_S, in series with the input protection circuit, as shown in Fig. 4. Although the input inverter A is still clamped at one diode drop above V_{DD} or one diode drop below V_{SS}, the waveform at point (4) is allowed to swing well above V_{DD} and below V_{SS}. The larger swing reduces the dependency of transfer-voltage variations upon stability; the variable characteristics of the input protection circuit and their effect upon stability are greatly reduced. An analysis of this circuit is presented in

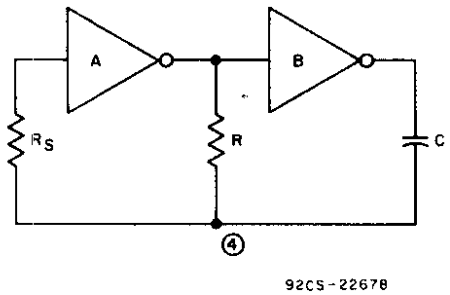

Fig. 4 – RC-oscillator with the addition of R_S.

Appendix B; the equation for the period, T, for this circuit is shown in Eq. 2.

When $K = \frac{R_S}{R}$, T is:

$$\left\{ \begin{array}{l} T = -RC \ln \dfrac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_D)^2} \\ \\ \quad - \dfrac{(K \quad)}{(K+1)} RC \ln \dfrac{K[V_{DD} + V_D]}{K[V_{DD} + V_{TR}] + [V_{TR} - V_D]} \\ \\ \quad - \dfrac{(K \quad)}{(K+1)} RC \ln \dfrac{K[V_{DD} + V_D]}{K[2V_{DD} - V_{TR}] + [V_{DD} - V_{TR} - V_D]} \end{array} \right\} \quad (2)$$

In this form it is easy to see that when K approaches zero, the circuit and associated waveforms are equivalent to those of Fig. A-1. On the other hand, as K approaches infinity, the variation in period as a function of V_{DD} is reduced to zero. This result is shown in Fig. 5, where period as a function of transfer voltage is plotted for different value of V_{DD} and K, and Fig. 6, which shows period as a function of K for different values of V_{DD}. Variation in period with transfer voltage is also reduced as K increases. This variation decreases from 10 per cent for K = 0 to about 5 per cent as K gets large.

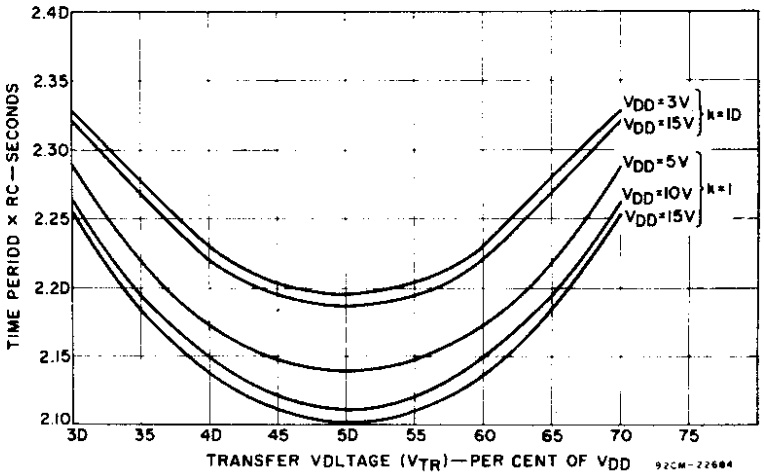

Fig. 5 – Discrete RC-oscillator time period as a function of transfer voltage.

There are some obvious limitations in the value of R_S that can be used. Besides the disadvantages in this circuit if R is to

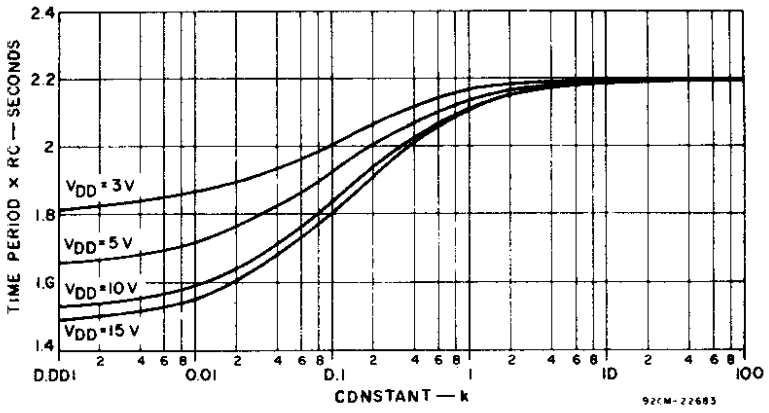

Fig. 6 – Discrete RC-oscillator time period as a function of constant, k.

be made adjustable, the user must be careful with component layout, if R_S is made very large, to take advantage of the improvement in stability. A time constant and phase shift is produced by R_S and stray wiring and breadboard capacitance, see Fig. 7. This shift creates a switching delay in the circuit which changes the time period and, in addition, may cause spurious oscillations and glitches in the multivibrator circuit. A reasonable value for K would be anywhere from 2 to 10, with maximum and minimum values for R_S determined by the above considerations.

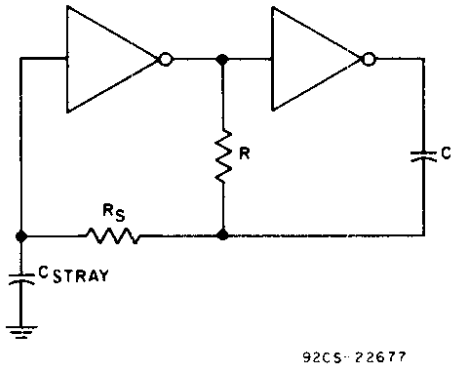

Fig. 7 – RC-oscillator circuit with stray capacitance.

COS/MOS INTEGRATED RC OSCILLATORS

The RCA-CD4047A is an integrated RC oscillator that eliminates most of the disadvantages of the discrete circuits previously discussed. The primary reason for this improved performance is the special input-protection circuit which allows the capacitor charging waveform to swing above V_{DD} and below V_{SS} without the need for an external resistor. This circuit, shown in Fig. 8, has the same time period and stability as the circuit in Fig. 4 for the case where the value of R_S is infinite. However, a resistor is eliminated, as well as the disadvantages of a time constant caused by the resistor.

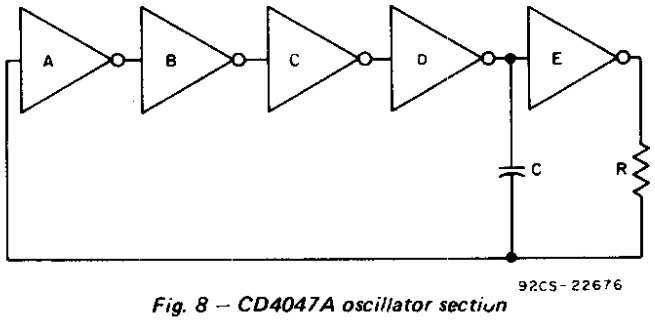

Fig. 8 – CD4047A oscillator section

There are two additional reasons for expected improvement with the CD4047A. First, the transfer-voltage point of the input inverter, A, is tested between 33 and 67 per cent of V_{DD} instead of between 30 and 70 per cent; this narrower test range improves stability by reducing unit-to-unit variations. In addition, large buffers are used for inverters D and E; this practice reduces the effect of changes of device output impedance with period stability. A derivation of period, T, for this circuit is presented in the Appendix C; the final equation for T becomes:

$$T = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_{TR})(2V_{DD} - V_{TR})} \quad (3)$$

Figure 9 shows a graph of stability as a function of transfer voltage based on this equation.

The graph of Fig. 9 shows a maximum variation of 5 per cent between minimum (2.197 RC) and maximum (2.307 RC) time periods. A value of 2.25 RC yields a ± 2.5 per-cent variation. Typical values of period variations at high frequencies and temperature extremes are included in the published data for the CD4047A.[1]

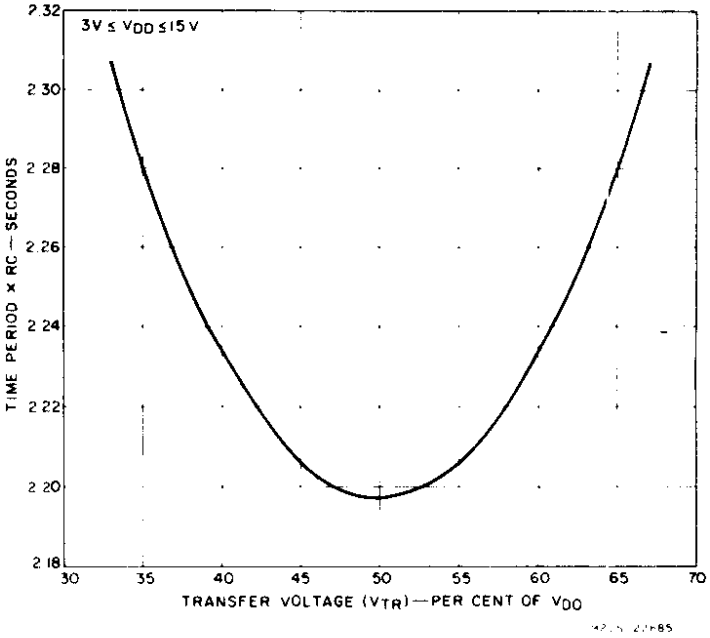

Fig. 9 – CD4047 time period as a function of transfer voltage.

An additional advantage of the CD4047A is a reduction in power dissipation as compared to the discrete multivibrators discussed previously. Inverter A in Fig. 8 is designed with high-impedance components that limit power dissipation during the time that the inverter operates in the middle of its transfer region. Four additional inverters are used to gradually shift from a very-high-impedance inverter at the input to a very-low-impedance driver in series with the external timing resistor. Calculations for power dissipation and a comparison of P_{diss} for the CD4047A and a discrete oscillator are presented in Appendix D; the result is

$$P_{diss} = 2CV^2 f \quad (4)$$

This equation specifies the power dissipated in the external components only. At low frequencies, where most of the power will be dissipated in R, power can be minimized by using a small value of C, since the formula shows the power is a function of C and not R.

Additional power is consumed in the CD4047A chip as a function of frequency. Fig. 10 shows curves for theoretical minimum power dissipation, actual CD4047A oscillator-power dissipation, and discrete oscillator-power dissipation as a function of frequency.

CMOS DISCRETE ONE-SHOTS

Fig. 11 illustrates one of several simple monostable circuits which can be employed in non-critical timing circuits.[2] The

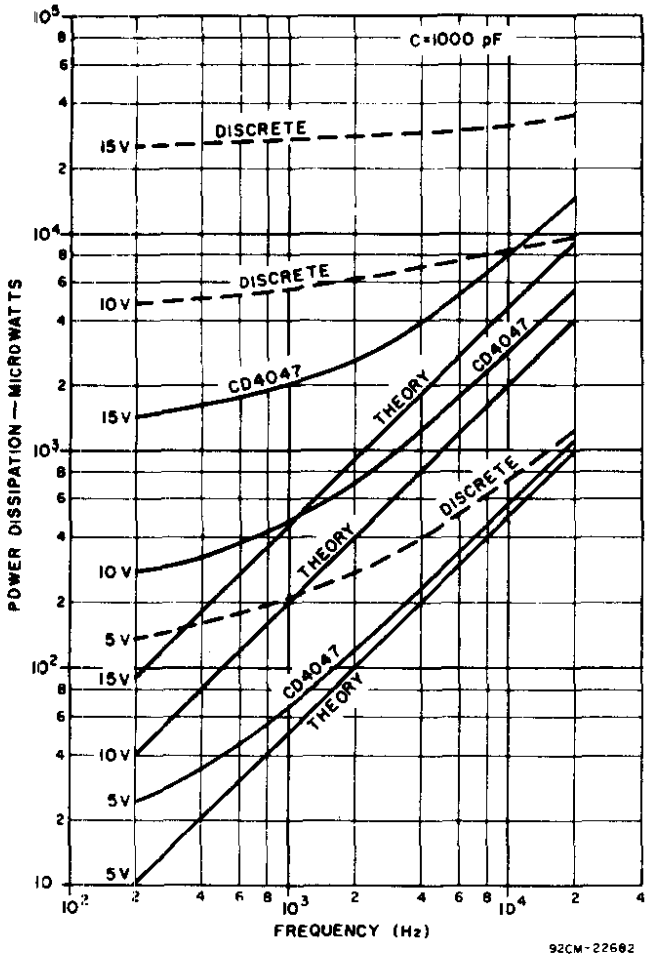

Fig. 10 – Comparison of P_{diss} for discrete oscillator and CD4047 with theory.

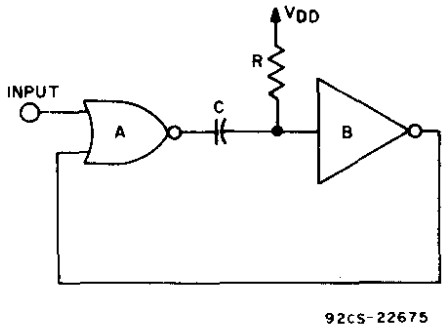

Fig. 11 – COS/MOS monostable circuit.

circuit pulse width is dependent upon the transfer voltage of inverter B as time constant RC charges to V_{DD} from V_{SS}. The pulse width is defined as

$$T = -RC \ln \frac{(V_{DD} - V_{TR})}{(V_{DD})} \quad (5)$$

Fig. 12 shows the variation in pulse width as a function of transfer voltage for this device.

There are several alternatives to the circuit shown in Fig. 12.[2] These alternatives have the advantage of greater stability, but at the expense of two time constants required in circuit and, in some cases, the addition of a diode.

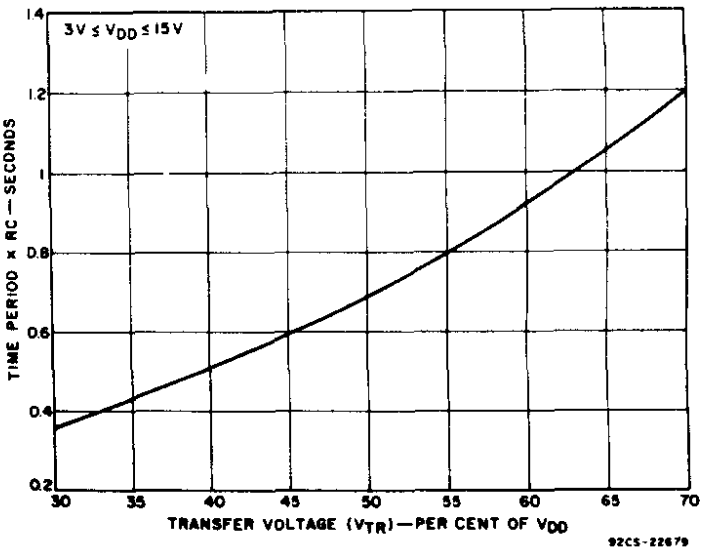

Fig. 12 – Simple one-shot time period as a function of transfer voltage.

COS/MOS INTEGRATED ONE-SHOTS

The CD4047A, when used in the monostable mode, again has several advantages over discrete designs. A high degree of accuracy can be achieved with one time constant, and power dissipation is lower than with discrete designs. Fig. 13 shows that many functions can be achieved with the CD4047A, including leading and trailing-edge triggering, and retriggering.

The pulse width, T_M, is expressed below: its derivation is given in Appendix E.

$$T_M = -RC \ln \frac{(V_{TR})(V_{DD}) - V_{TR})}{(2\,V_{DD})(2\,V_{DD} - V_{TR})} \quad (6)$$

Fig. 14 is a graph of pulse width versus transfer voltage based on the above equation.

The equations for monostable-mode power dissipation are also derived in Appendix E. For a repetitive output on the CD4047A, power dissipation can be expressed by the following equation:

$$P_{diss} = \frac{2.875\,CV_{DD}^2}{T_M} \times (\text{duty cycle}) \quad (7)$$

USING THE CD4047A – SPECIAL CONSIDERATIONS

A number of circuit considerations are explained below which will aid the user of the CD4047A.

A clamping circuit is provided on the chip to reduce the recovery time (tr) that would normally exist in other monostable circuits; see Figs. 15 and 16. Fig. 17 shows a plot of monostable-pulse-width stability as a function of duty cycle for specific R and C external components. Note that there is no appreciable change in pulse width until the duty cycle approaches 100 per cent. A disadvantage to the clamping circuit is that it introduces additional capacitance at the RC common node (Fig. 16), which may be noticeable for short pulse widths in the monostable mode only. Some diffusion capacitance present at the base of the n-p-n transistor is used to quickly

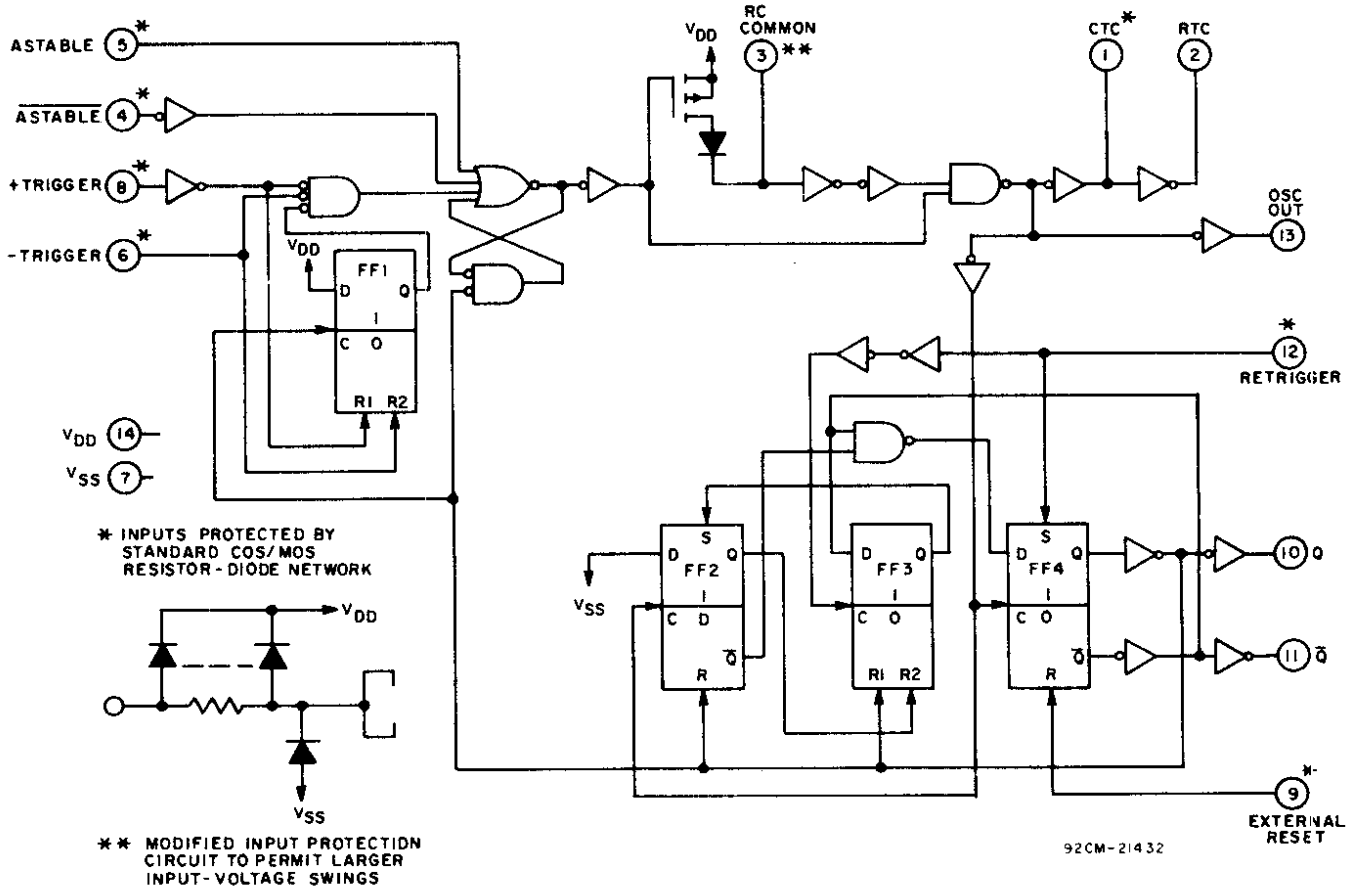

Fig. 13 – CD4047A logic diagram.

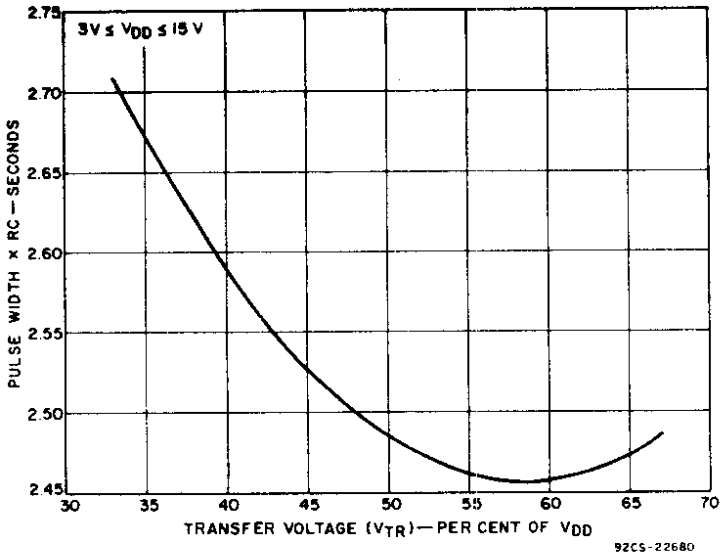

Fig. 14 – CD4047A one-shot pulse width as a function of transfer voltage.

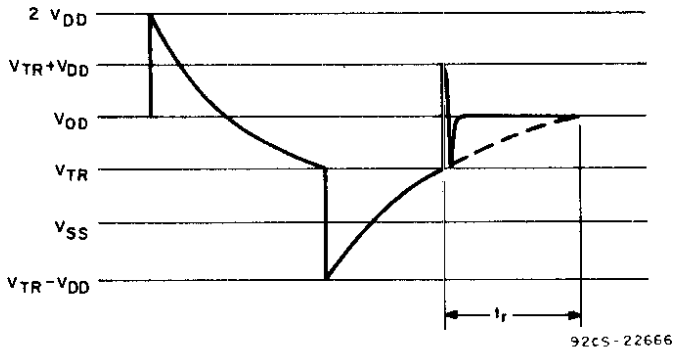

Fig. 15 – CD4047A one-shot RC waveform.

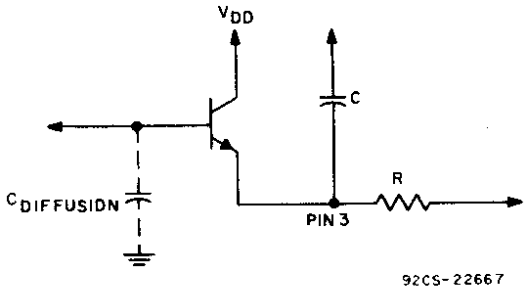

Fig. 16 – CD4047A clamping circuit.

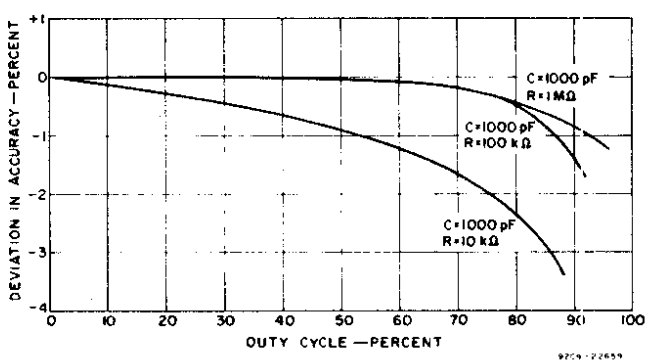

Fig. 17 – CD4047A monostable accuracy as a function of duty cycle.

charge C to V_{DD} after the one-shot cycle has terminated. This capacitance is multiplied by the beta of the transistor, and is in parallel with the external C during the time interval that the transistor is on ($V_{DD} - V_{BE} < t < V_{BE}$). Thus, when values of C less than 1000 picofarads are used, the actual width will be longer than that predicted by the formula. Fig. 18 is a graph of actual, typical pulse widths as a function of external C used under these conditions. Note that the minimum values of C used in the graph are the smallest that can be used in the CD4047A to assure proper operation of the circuit.

The waveform in Fig. 15 shows that two positive transitions are encountered by the control circuitry in the CD4047A. These transitions are necessary to make the output flip-flop at pin 10 toggle properly to produce the single pulse needed in monostable operation. However, at pin 13, the waveform of

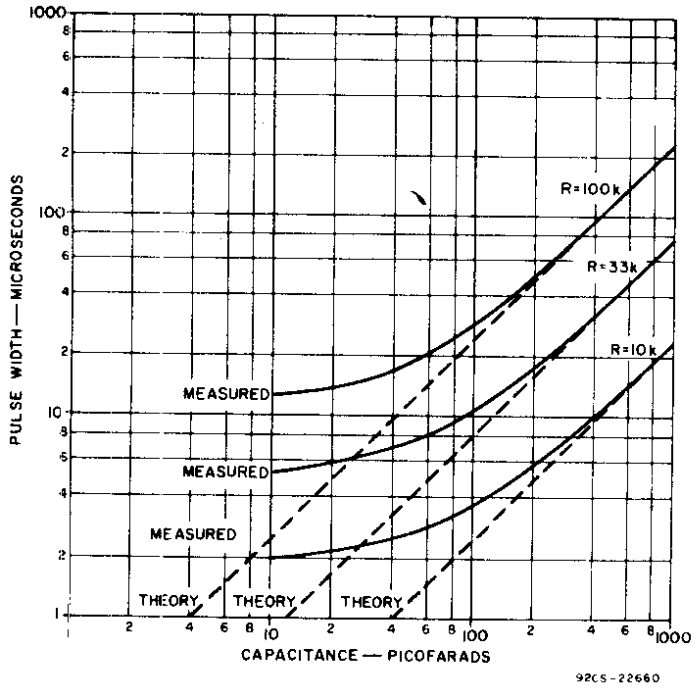

Fig. 18 – CD4047A pulse width as a function of capacitance.

Fig. 19 results; the pulse width of the spike is equivalent to the propagation delay of the circuit. This spike will normally prevent the user from using pin 13 in the monostable mode. In the astable mode, however, pin 13 can be used whenever a 50-per-cent duty cycle and higher drive capability are not

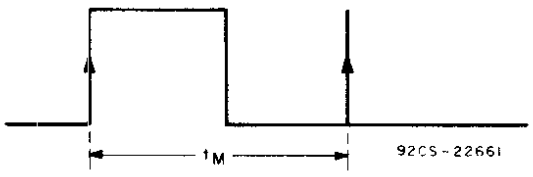

Fig. 19 – CD4047A one-shot output at pin 13.

required. The advantage to the use of pin 13 under these conditions is that the frequency of the waveform at pin 13 is twice that of pin 10 for the same external timing components.

When the CD4047A is used in the retrigger mode, the retrigger input is connected directly to the set input of FF4, as shown in Fig. 13. This connection means that the output at pin 10 will be high during the time that a high level is present on pin 12. Thus, if normal one-shot operation is required at any time that the circuit is in the retrigger mode, the input pulse should be shorter than the expected pulse at the output. Note that in the retrigger mode the output pulse width is not referenced to the last positive-going edge produced at the input because of the asynchronous nature of the circuit. The output actually terminates when two internal-oscillator leading edges have been received by FF4, after the high level present on pin 12 has been removed. The output width variation will then be between one and two time constants referenced to the trailing edge of the input at pin 12, see Fig. 20.

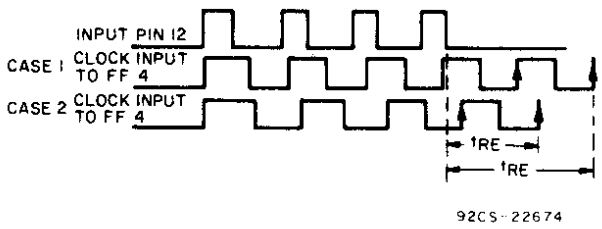

Fig. 20 – CD4047A retrigger-mode waveforms.

A section on timing-component limitations is presented in the CD4047A data sheet.[1] It should be emphasized that it is desirable to use a small value of capacitance wherever possible. The circuit will work well even when the value of R approaches or exceeds 1 megohm. For very low frequencies, where a large value of capacitance is needed, the selection of the capacitor is very important. It must be nonpolarized because there is no reference ground at either of the two pins to which C is connected. The capacitor parallel resistance (i.e., leakage) must also be at least an order of magnitude higher than the external R used. This criterion generally eliminates electrolytic capacitors and those made of materials which could produce greater leakage current than that permitted for proper circuit operation.

Because of the internal circuit construction, there is no guarantee as to what dc level will be present on the output at pin 10 or 11 when power is first turned on. If this condition must be guaranteed, a system-power on pulse input to pin 9 can be made to assure that pin 10 will initially be at a low logic level. The pulse can be generated from one of the circuits shown in Fig. 21.

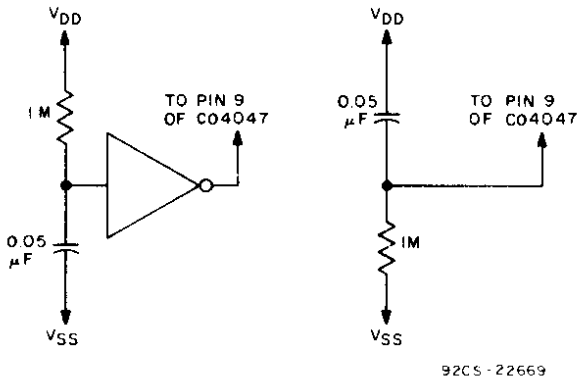

Fig. 21 – CD4047A power-up reset circuits.

Although the CD4047A data sheet calls for a minimum input pulse duration of 200 nanoseconds at 10 volts and 500 nanoseconds at 5 volts, shorter pulses (due to transients, etc.) occur frequently in system applications where the CD4047A is used. Such narrow pulses may not be ignored by the CD4047A, but may instead cause Q to go high permanently or until a reset input occurs. The circuit shown in Fig. 22 eliminates this problem by essentially "lengthening" the trigger pulse by feeding back through R_A and C_A a current pulse when Q goes from 0 to a 1. The particular values shown have been tried and found to work well, even for extremely short input pulses (less than 20 nanoseconds).

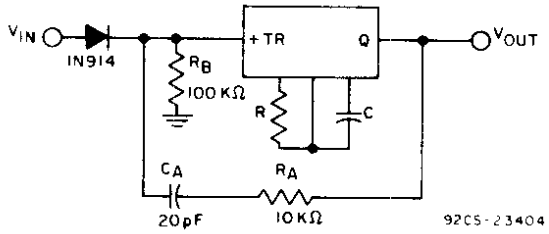

Fig. 22 – Input-pulse stretcher circuit.

APPLICATIONS

NOISE DISCRIMINATOR

Fig. 23 illustrates an application of the CD4047A in a noise-discriminator circuit. By adjusting the external time constant, a pulse width narrower than that determined by the time constant will be rejected by the circuit. The output pulse will

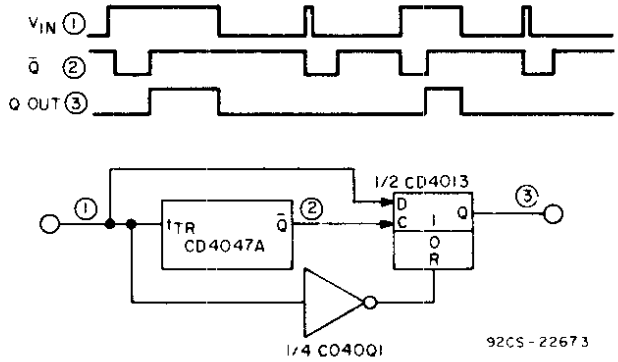

Fig. 23 – Noise-discriminator circuit.

follow the desired input, but the leading edge will be delayed by the selected time constant. Fig. 24 shows typical waveforms with the circuit in operation.

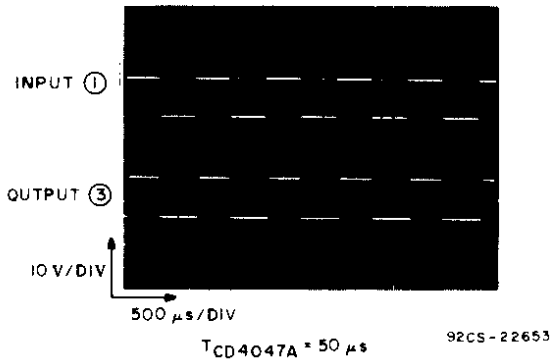

Fig. 24 – Noise-discriminator circuit waveforms.

FREQUENCY DISCRIMINATOR

The CD4047A can be used as a frequency-to-voltage converter, as shown in Fig. 25. A waveform of varying frequency is applied to the +TR input. The one-shot will produce a pulse of constant width for each positive transition on the input. The

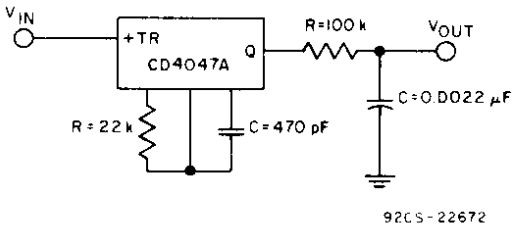

Fig. 25 – Frequency-discriminator circuit.

resultant pulse train is integrated to produce a waveform whose amplitude is proportional to the input frequency. The waveforms of Fig. 26 were taken with the circuit in operation.

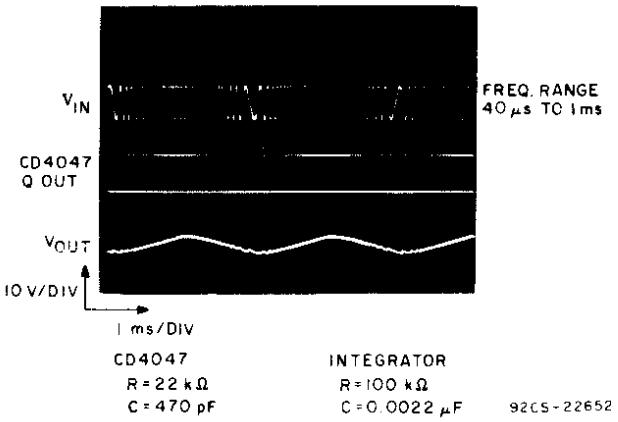

Fig. 26 – Frequency-discriminator-circuit waveforms.

LOW-PASS FILTER

A simple circuit using the CD4047A as a low-pass filter is shown in Fig. 27. The time constant chosen for the multivibrator will determine the upper cutoff frequency for the filter. The circuit essentially compares the input frequency

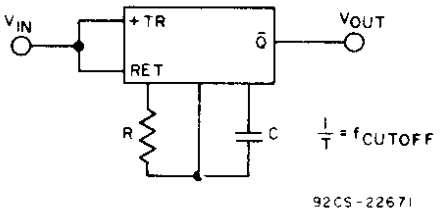

Fig. 27 – Low-pass filter circuit.

with its own reference, and produces an output which follows the input for frequencies less than f_{cutoff}, and a low output for frequencies greater than f_{cutoff}. Figs. 28 and 29 show waveforms with the low-pass filter circuit in operation.

BANDPASS FILTER

Two CD4047A low-pass filters can be employed to construct a bandpass filter, as illustrated by the circuit in Fig. 30.

The pass band is determined by the time constants of the two filters. If the output of filter No. 2 is delayed by C_1, the CD4013A flip-flop will clock high only when the cutoff frequency of filter No. 2 has been exceeded; this point is illustrated in the timing diagram in Fig. 30. The $\overline{Q}$ output of the CD4013A is gated with the output of filter No. 1 to produce the desired output. Typical operation of the circuit is shown in Fig. 31, where the input frequency is swept through the pass band.

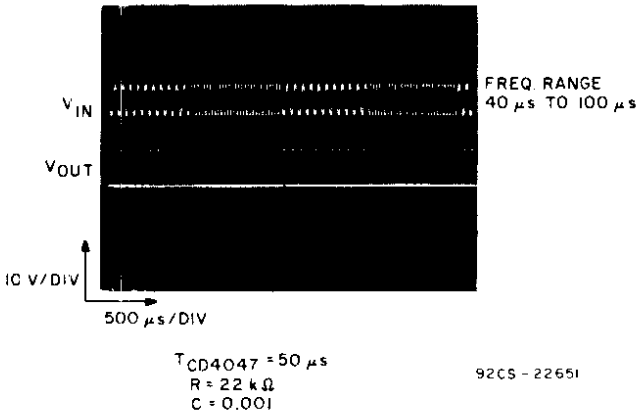

Fig. 28 – Low-pass filter-circuit waveforms.

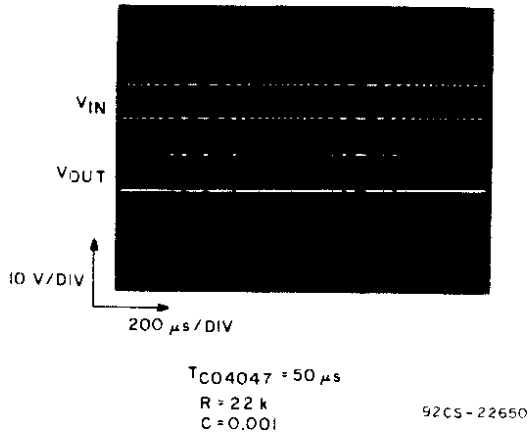

Fig. 29 – Low-pass-circuit waveforms.

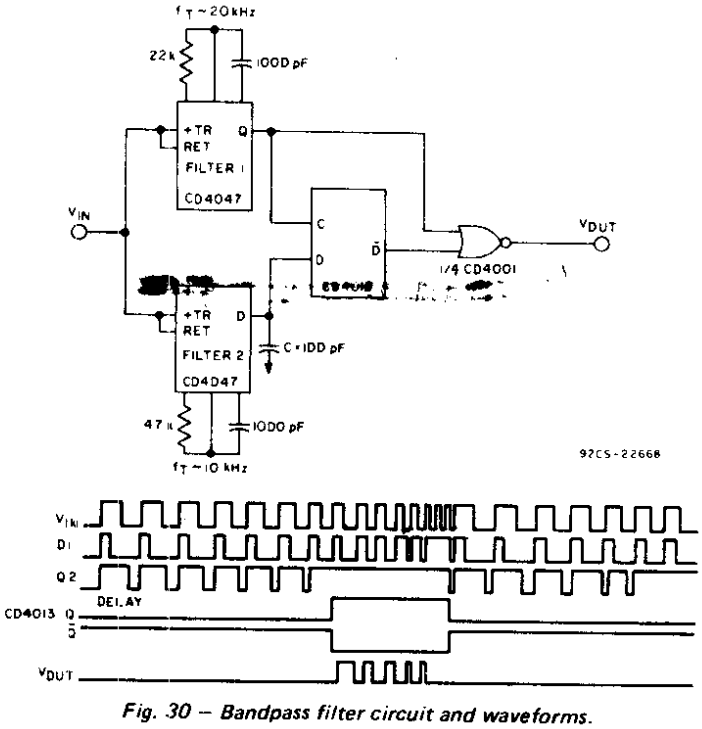

Fig. 30 – Bandpass filter circuit and waveforms.

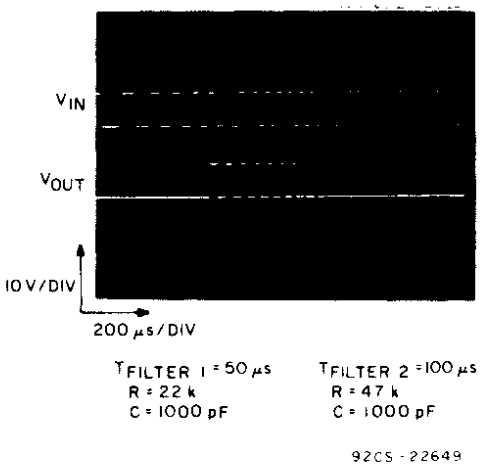

Fig. 31 – Bandpass-filter-circuit waveforms.

ENVELOPE DETECTOR

The CD4047A can be used as an envelope detector by employing it in the retrigger mode, as shown in Fig. 32. The time constant is selected so that the circuit will retrigger at the

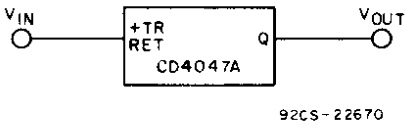

Fig. 32 – Envelope-detector circuit.

frequency of the input pulse burst. A dc level appears at the output for the duration of the input pulse train. Fig. 33 shows waveforms taken with the circuit in operation.

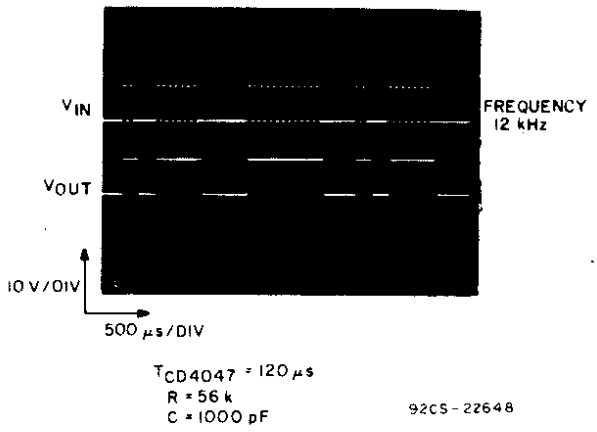

Fig. 33 – Envelope-detector-circuit waveforms.

PULSE GENERATOR

Several CD4047A units can be connected together to produce a general-purpose laboratory pulse generator, as shown in Fig. 34. The circuit shown has variable-frequency and pulse-width control, as well as gating and delayed sync capability.

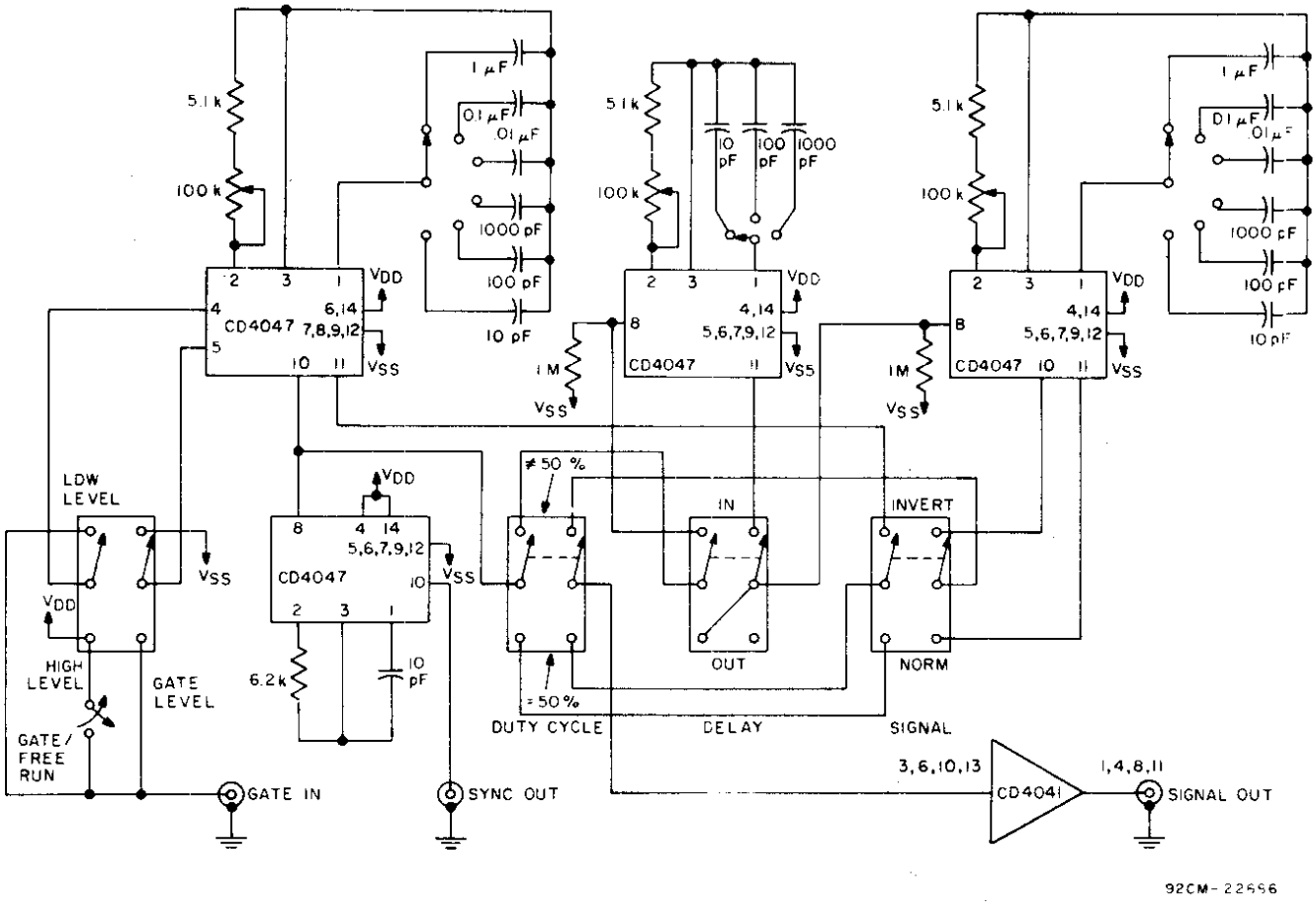

Fig. 34 — Pulse-generator circuit.

Gating can be controlled from a high- or low-level input. Automatic 50-per-cent duty-cycle capability is included, as normal or inverted output.

CD4047A No. 1 is connected as a gated, astable multivibrator, and, with the RC values shown, can produce overlapping ranges of frequencies from 2 Hz to 1 MHz. For free-running operation, the Gate/Free-Run switch is closed, and the Gate Level switch is placed in the **high-level** position. Standby operation can be achieved with the Gate Level switch in the **low-level** position. When gating, the Gate/Free-Run switch is open, and the Gate Level switch is set to the appropriate position. The gate signal is applied to the Gate In jack.

CD4047A No. 2 is triggered from the gated, astable multivibrator, and produces a narrow sync pulse which can trigger an oscilloscope or generator. The sync pulse is obtained from the Sync Out jack.

If a 50-per-cent duty cycle is desired, the Duty Cycle switch is set in the 50-per-cent position, and the output is obtained from CD4047A No. 1. The Signal Polarity switch determines whether the Q and $\overline{Q}$ output is used.

CD4047A No. 3 produces a variable, delayed (from 1.5 microseconds to 250 milliseconds) output with respect to the sync pulse when the Delay switch is in the IN position. This one-shot is bypassed when the Delay switch is in the OUT position (the inherent delay is approximately 400 nanoseconds).

CD4047A No. 4 is a monostable multivibrator which receives trigger pulses from CD4047A No. 1 or No. 3. It can produce overlapping ranges of pulse widths from 1.5 microseconds to 200 milliseconds with the values shown.

The signal output is buffered with the CD4041A to allow the pulse generator to drive any required load. The circuit shown has the advantages of being compact, battery-powered, and COS/MOS compatible. In addition, it is capable of being run from the same power supply as the device under test to assure that the input levels are the same as V_{DD} when the power-supply voltage is varied.

MISCELLANEOUS APPLICATIONS

The basic properties of good stability in the astable mode, and stable pulse delay and width control in the monostable mode, make the CD4047A a useful building block in many systems, such as PMOS clock generation, audio tone generation, semiconductor memory systems, semiconductor memory exercisers, and general-purpose functional-testing systems. This Application Note will serve as a guideline in incorporating the CD4047A in a system design.

Appendix A –

Calculation of the Period of an Astable Multivibrator Using a Single RC Time Constant

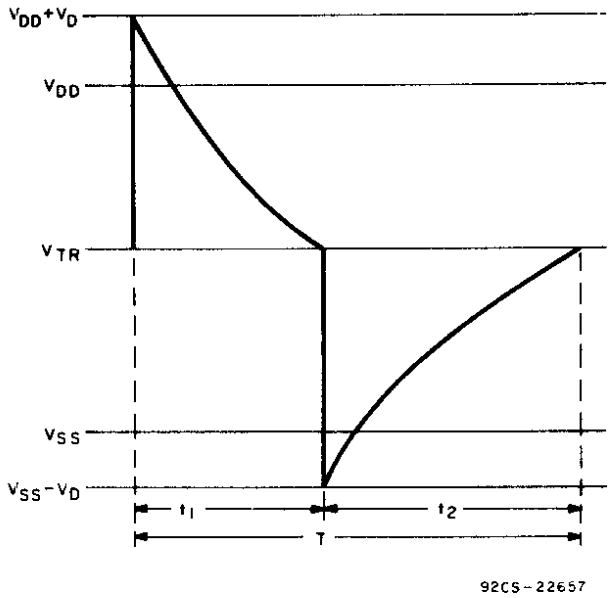

Fig. A-1 – RC oscillator waveform for the circuit of Fig. 1.

In Fig. A-1:

$$t_1: V_{TR} = (V_{DD} + V_D)\, e^{-t_1/RC}$$

$$t_1 = -RC \ln \frac{V_{TR}}{V_{DD} + V_D}$$

$$t_2: V_{DD} - V_{TR} = (V_{DD} + V_D)\, e^{-t_2/RC}$$

$$t_2 = RC \ln \frac{V_{DD} - V_{TR}}{V_{DD} + V_D}$$

And the period of an astable multivibrator using a single RC time constant is:

$$T = t_1 + t_2 = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_D)^2}$$

Appendix B –

Analysis of Circuit Shown in Fig. 4

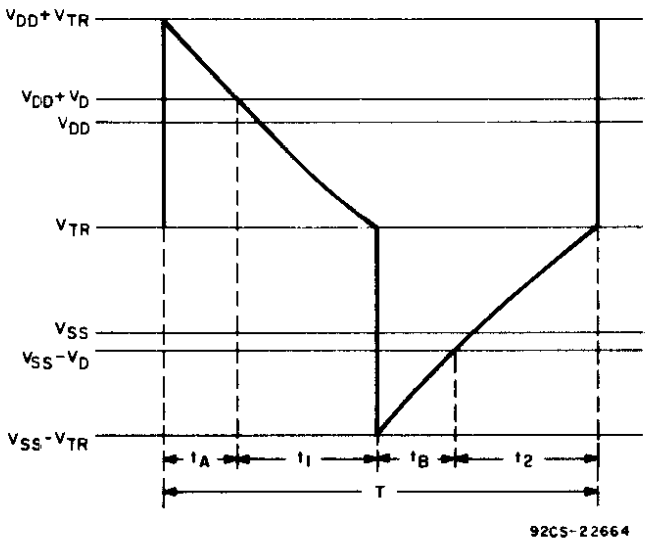

Fig. B-1 – RC waveform for the circuit of Fig. 4.

In Fig. B-1:

$$t_1: V_{TR} = (V_{DD} + V_D)\, e^{-t_1/RC}$$

$$t_1 = -RC \ln \frac{V_{TR}}{V_{DD} + V_D}$$

$$t_2: V_{DD} - V_{TR} = (V_{DD} + V_D)\, e^{-t_2/RC}$$

$$t_2 = -RC \ln \frac{V_{DD} - V_{TR}}{V_{DD} + V_D}$$

t_A

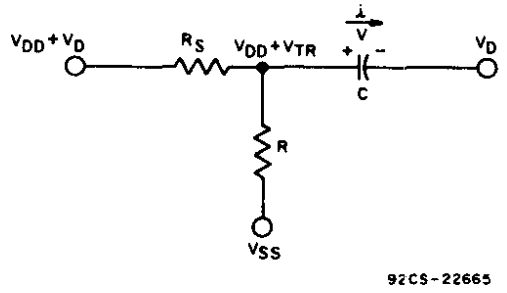

Fig. B-2 – Initial conditions for solving period t_A.

Circuit initial conditions are shown in Fig. B-2. In the figure

$$-C\frac{dv}{dt} = \frac{V + V_{DD}}{R} + \frac{V + V_{DD} - (V_{DD} + V_D)}{R_S} \qquad (B-1)$$

Eq. (B-1) is solved for V; the final voltage across the capacitor is

$$V = C_1 e^{-K_1 t_A} + \frac{K_2}{K_1} \qquad (B-2)$$

where $C_1 = V_{TR}$ = initial voltage across capacitor

$$K_1 = \frac{R_S + R}{R_S RC}$$

$$K_2 = \frac{V_D R - R_S V_{DD}}{R_S RC}$$

By inserting these values into Eq. (B-2) and setting the final voltage across the capacitor, V, to V_D, t_A becomes

$$t_A = -\left[\frac{R_S RC}{R_S + R}\right] \ln \frac{R_S [V_{DD} + V_D]}{R_S [V_{DD} + V_{TR}] + R [V_{TR} - V_D]}$$

t_B

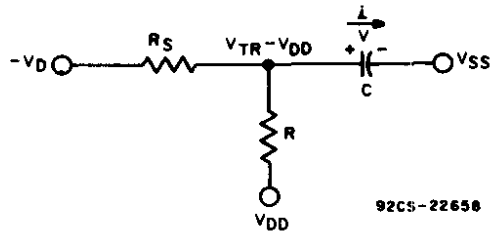

Fig. B-3 – Initial conditions for solving period t_B.

Circuit initial conditions as shown in Fig. B-3. In the figure

$$C\frac{dv}{dt} = \frac{V_{DD} - V}{R} - \frac{V_D + V}{R_S} \qquad (B-3)$$

Solving Eq. (B-3) for V the final voltage across the capacitor, yields

$$V = C_2 e^{-K_1 t_B} - \frac{K_2}{K_1} \qquad (B-4)$$

where $C_2 = V_{TR} - V_{DD}$ = initial voltage across capacitor

K_1, K_2 are same values as for above for t_A.

Insertion of these values into Eq. (B-4), with $V = -V_D$ yields

$$t_B = \left[\frac{R_S RC}{R_S + R}\right] \ln \frac{R_S [V_{DD} + V_D]}{R_S [2 V_{DD} - V_{TR}] + R [V_{DD} - V_{TR} - V_D]}$$

and $T = t_1 + t_2 + t_A + t_B$

The equations for t_A, t_B, and T can be simplified by expressing R_S as a multiple of R. Let $K = \frac{R_S}{R}$ and combining the expressions for t_1 and t_2. The resulting expression for T is

$$T = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_D)^2}$$

$$-\left(\frac{K}{K+1}\right) RC \ln \frac{K [V_{DD} + V_D]}{K [V_{DD} + V_{TR}] + [V_{TR} - V_D]}$$

$$-\left(\frac{K}{K+1}\right) RC \ln \frac{K [V_{DD} + V_D]}{K [2 V_{DD} - V_{TR}] + [V_{DD} - V_{TR} - V_D]}$$

Appendix C –

Calculation for Period of Astable Multivibrator Using Integrated Techniques

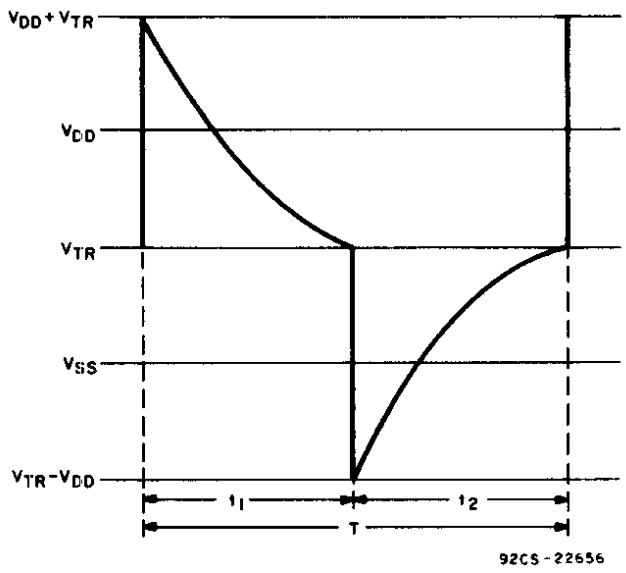

Fig. C-1 – CD4047A RC oscillator waveform.

In Fig. C-1

$$t_1: V_{TR} = (V_{DD} + V_{VTR})\, e^{-t_1/RC}$$

$$t_1 = RC \ln \frac{V_{TR}}{V_{DD} + V_{TR}}$$

$$t_2: V_{DD} - V_{TR} = (V_{DD} + V_{TR})\, e^{-t_1/RC}$$

$$t_2 = -RC \ln \frac{V_{DD} - V_{TR}}{2\,V_{DD} - V_{TR}}$$

And the period of the astable multivibrator using integrated techniques is

$$T = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_{TR})(2\,V_{DD} - V_{TR})}$$

Appendix D –

Power Needed for Charge and Discharge of an External Capacitor During One Cycle

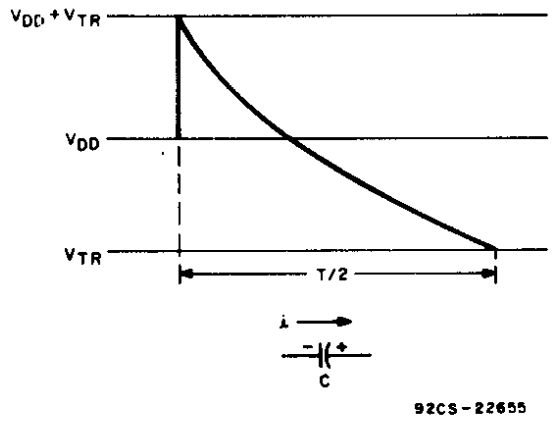

Fig. D-1 – Waveform for calculating power dissipation.

Assume for this calculation that V_{TR} = 50-per-cent V_{DD}, and that T = 2.2 RC. Since charge and discharge cycles are symmetrical, the calculation can be performed by analyzing a discharge cycle only. See Fig. D-1.

$$V = 1.5\, V_{DD}\, e^{-t/RC}$$

$$\frac{dv}{dt} = -\left(\frac{1}{RC}\right)(1.5\, V_{DD})\left(e^{-t/RC}\right)$$

$$P = \frac{1}{(T/2)} \int_0^{T/2} CV \frac{dv}{dt}\, dt$$

$$= \frac{2C}{T} \int_0^{T/2} \left(1.5\, V_{DD}\, e^{-t/RC}\right) \left(\frac{1}{RC}\right)(1.5\, V_{DD})\, e^{-t/RC}\, dt$$

$$= \frac{4.5C}{T} \frac{V_{DD}^2}{RC} \int_0^{T/2} e^{-2t/RC}\, dt$$

$$= -\frac{2.25C\, V_{DD}^2}{T}\, e^{-2t/RC} \Big|_0^{T/2}$$

Substituting T = 2.2 RC

$$P = -\frac{C}{T}(2.25)\, V_{DD}^2 \left[e^{-2.2} - 1\right] = \frac{2.0C}{T} V_{DD}^2$$

$$P = 2\, CV^2 f$$

Appendix E –

Equations for Pulse Width T_M of CD4047A in Monostable Mode

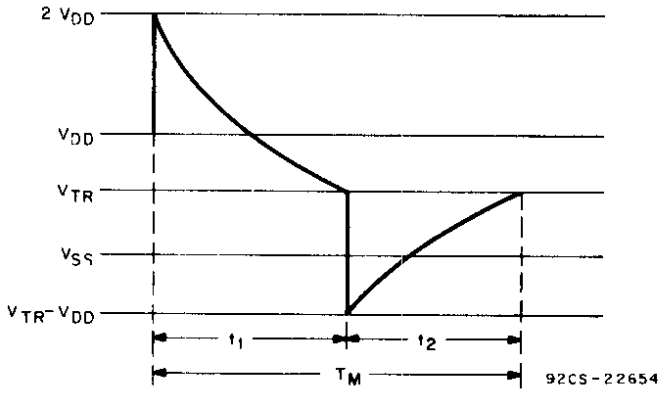

Fig. E-1 – CD4047A RC waveform, monostable mode.

Note that the waveform in Fig. E-1 is not symmetrical because the timing capacitor is initially charged to V_{DD}. In the monostable mode, the circuit goes through one cycle only.

Monostable Power Dissipation

To calculate the power dissipation for the circuit in the monostable mode, refer to Fig. E-1. If it is assumed that V_{TR} = 50-per-cent V_{DD}, Fig. 14 shows that T_M = 2.485 RC. t_2 is the same as in the astable calculation, i.e., t_2 = 1.10 RC and $P_{t2} = CV^2f$ for V_{TR} = 50-per-cent V_{DD}. Thus, t_1 in the monostable mode = 2.485 RC – 1.10 RC = 1.385 RC.

$$P = \frac{1}{T_M}\left[\int_0^{t_1} CV\frac{dv}{dt}\,dt + \int_{t_1}^{t_2} CV\frac{dv}{dt}\,dv\right]$$

$$= \frac{1}{T_M}\int_0^{t_1} CV\frac{dv}{dt}\,dt + \frac{1}{T_M}CV^2$$

where $V = 2V_{DD}\,e^{-t/RC}$ and

$$\frac{dv}{dt} = -\left(-\frac{1}{RC}\right)(2V_{DD})\,e^{-t/RC}$$

$$t_1: V_{TR} = 2V_{DD}\,e^{-t_1/RC}$$

$$t_1 = -RC\ln\frac{V_{TR}}{2V_{DD}}$$

$$t_2: V_{DD} - V_{TR} = (2V_{DD} - V_{TR})\,e^{-t_2/RC}$$

$$t_2 = -RC\ln\frac{V_{DD} - V_{TR}}{2V_{DD} - V_{TR}}$$

And the equation for the pulse width, T_M, of a CD4047A in the monostable mode is:

$$T_M = t_1 + t_2 = -RC\ln\frac{(V_{TR})(V_{DD} - V_{TR})}{(2V_{DD})(2V_{DD} - V_{TR})}$$

$$Pt_1 = \frac{C}{T_M}\int_0^{t_1}\left(2V_{dd}\,e^{-t/RC}\right)\left(\frac{1}{RC}\right)(2V_{dd}\,e^{-t/RC})\,dt$$

$$= \frac{C}{T_M}\,\frac{4V_{dd}^2}{RC}\int_0^{t_1} e^{-2t/RC}\,dt$$

$$= -\frac{C}{T_M}\,2V_{dd}^2\,e^{-2t/RC}\Big|_0^{t_1}$$

Substituting t_1 = 1.385 RC

$$P_{t1} = -\frac{C}{T_M}\,2Vdd^2\,[e^{-2.77} - 1] = \frac{1.875\,C\,Vdd^2}{T_M}$$

$$P = P_{t1} + P_{t2} = (1.875 + 1)\frac{C\,Vdd^2}{T_M} = 2.875\,\frac{C\,Vdd^2}{T_M}$$

For a repetitive output from the CD4047A

$$P = \frac{2.875\,C\,Vdd^2}{T_M} \times \text{duty cycle}$$

REFERENCES

1. **"CD4047A COS/MOS Low-Power Monostable/Astable Multivibrator,"** RCA Data Bulletin, File No. 623
2. **"Astable and Monostable Oscillators Using RCA COS/MOS Digital Integrated Circuits,"** by J. A. Dean and J. P. Rupley, RCA Application Note ICAN-6267

ACKNOWLEDGMENTS

The assistance of R. Vaccarella in the designing of some of the application circuits shown and in obtaining laboratory measurements used in plotting the curves shown in this Note is acknowledged.