Astable and Monostable Oscillators Using RCA COS/MOS Digital Integrated Circuits

by J. A. Dean and J. P. Rupley

COS/MOS integrated logic circuits are being widely used in digital and other applications because of their inherent advantages of high noise immunity, extremely low power dissipation, and tolerance to wide variations in power-supply voltages and operating-temperature ranges. In addition to these features, COS/MOS gates and inverters can provide cost and size reductions in multivibrator circuits because their high input impedance makes it possible to obtain large time constants without the use of large capacitors. This Note describes several techniques which may be used to compensate for the normal threshold variation of MOS devices in the design of stable multivibrator circuits for operation at frequencies up to 1 MHz. The circuits shown can be formed by use of COS/MOS inverters and NAND or NOR gates connected in an inverter configuration. NAND and NOR gates perform the inverter function when all of the gate inputs are tied together. This Note also describes various applications for COS/MOS multivibrator circuits, (i.e., voltage-controlled oscillators, voltage controlled-pulse-width circuits, phased-locked voltage controlled oscillators, frequency multipliers, and modulator/demodulator (envelope detectors). (Note: COS/MOS Hex Buffers CD4009A and CD4049A and Quad Buffer CD4041A are not recommended for use as multivibrators because of the very high power consumption in the linear mode for long time constants. In addition, the Hex Buffers have large imbalance between source and sink current capability which makes oscillator start-up more unpredictable. The COS/MOS General-Purpose Hex Inverter CD4069B is recommended for use in the multivibrator applications illustrated in this Note. The CD4069B is well adapted to MV applications, having balanced output drive capability of ±0.4 milliampere for 5 V operation at an output voltage level of ±0.4 volt. Specific data in this Note relate to the use of "A" series gates as shown; performance using the CD4069B may differ slightly from the data shown herein.

ASTABLE CIRCUITS

Fig. 1(a) shows an astable multivibrator circuit that uses two COS/MOS inverters, and Fig. 1(b) shows the related waveforms. This simple circuit requires only two resistors and one capacitor, and operates in the following manner. When the waveform 1 at the output of inverter B is in a high or "one" state, capacitor C_{tc} becomes charged positive. As a result, the input to inverter A is high and its output is low or "zero". Resistor R_{tc} is returned to the output of inverter A to provide a path to ground for discharge of capacitor C_{tc}.

As long as the output of A is low, the output of inverter B is high. As capacitor C_{tc} discharges, however, the voltage generated [waveform 2 in Fig. 1(b)] approaches and passes through the transfer voltage point of inverter A. At the instant that this crossover occurs, the output of A becomes high; as a result, the output of B becomes low and the capacitor C_{tc} is charged negative (or low). The resistor R_{tc} connected to the output of A then provides a charge path to a supply voltage. Capacitor C_{tc} begins to charge to this voltage, and again the voltage approaches and passes through the transfer voltage point of inverter A. At that instant, the circuit again changes state (the output of A becomes low and that of B high) and the cycle repeats.

Because of the input-diode protection circuits included in the COS/MOS IC, shown in Fig. 2, the generated drive waveform

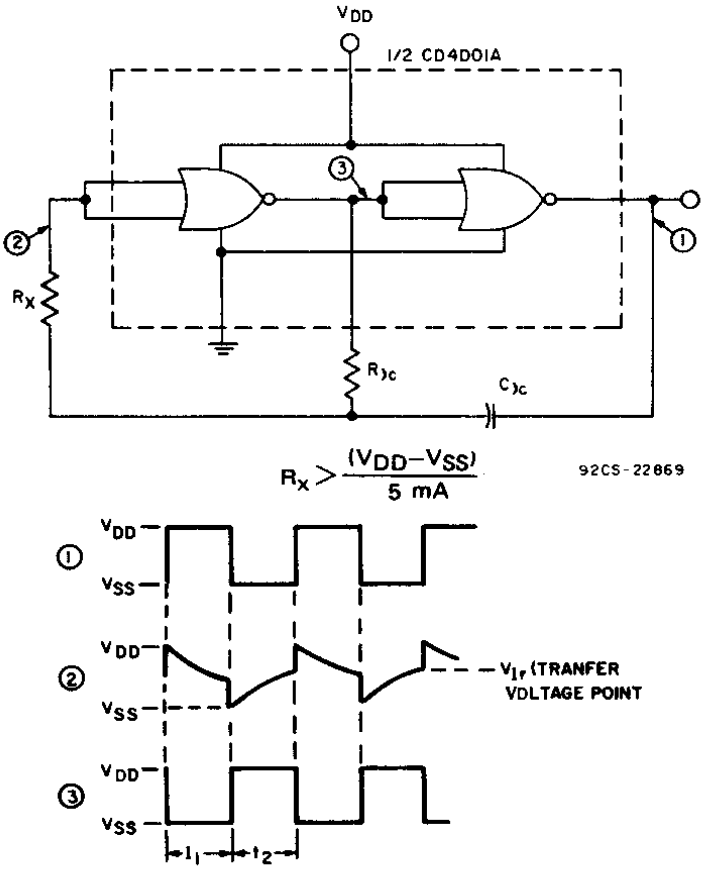


Fig. 1 - Circuit diagram and voltage waveforms for astable multivibrator circuit that uses two COS/MOS inverters.

is clamped between V_{DD} and V_{SS}. Consequently, the time to complete one cycle is approximately 1.4 times the RC time constant because one time constant is used to control the switching of both states of the multivibrator circuit. Resistor R_X (Fig.1) limits the current through D1 (Fig.2) to a safe level. Switching occurs when the charge or discharge reaches the transfer voltage level, or when the time period reaches 70.7 per cent of its discharge. As shown in waveform 2 of Fig.1(b), the transfer voltage point V_{tr} is the same for t_1 and t_2. The time period T for one cycle can be computed as follows:

$$T = t_1 + t_2$$

$$t_1 = -RC \ln \frac{(V_{DD} - V_{tr})}{V_{DD}}$$

$$t_2 = -RC \left[\ln \frac{V_{tr}}{V_{DD}} \right]$$

$$T = -RC \left[\ln \frac{(V_{DD} - V_{tr})}{V_{DD}} + \ln \frac{V_{tr}}{V_{DD}} \right] \quad (1)$$

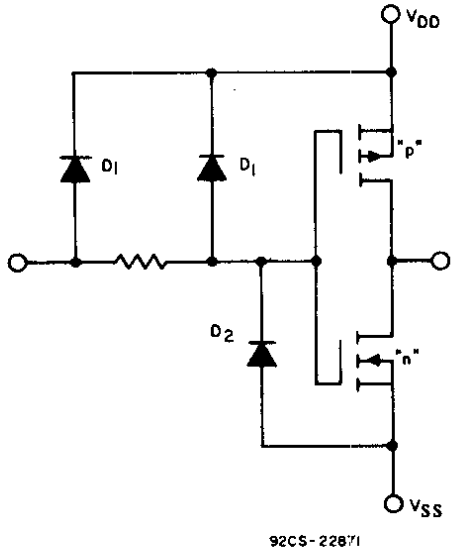


Fig. 2 - Diode protection circuit.

If the time constant is assumed to be 1×10^{-6} second and the transfer voltage V_{tr} is allowed to vary from 33 to 67 per cent of V_{DD}, the period T varies from 1.4 microseconds at a value of V_{tr} equal to half of V_{DD} to 1.5 microseconds at either the 33 or 67 per cent value of V_{DD}. Therefore, the maximum variation in the time period T is only 9 per cent with a ±33-per-cent variation in transfer voltage from unit to unit.

The oscillator can be made independent of supply-voltage variations by use of a large resistance in series with the input lead to inverter A, shown in Fig.3(a). This resistor R_S should be at least twice as large as the resistor R_{tc} of the time constant to allow the voltage waveform generated at the junction of R_s, R_{tc}, and C_{tc} to rise to $V_{DD} + V_{tr}$. The waveform is still clamped at the input between V_{DD} and V_{SS}, as shown by the waveforms in Fig. 3(b). The use of resistor R_s provides several advantages in the circuit. First, because the RC time constant controls the frequency, the over-all maximum variations in the time period are reduced to less than 5 per cent with variations in transfer voltage, as determined by the following equation:

$$T = -RC \left[\ln \frac{V_{tr}}{(V_{DD} + V_{tr})} + \ln \frac{(V_{DD} - V_{tr})}{2V_{DD} - V_{tr}} \right] \quad (2)$$

The resistor R_s also makes the frequency independent of supply-voltage variations. Table I shows data measured on typical units with and without the resistor

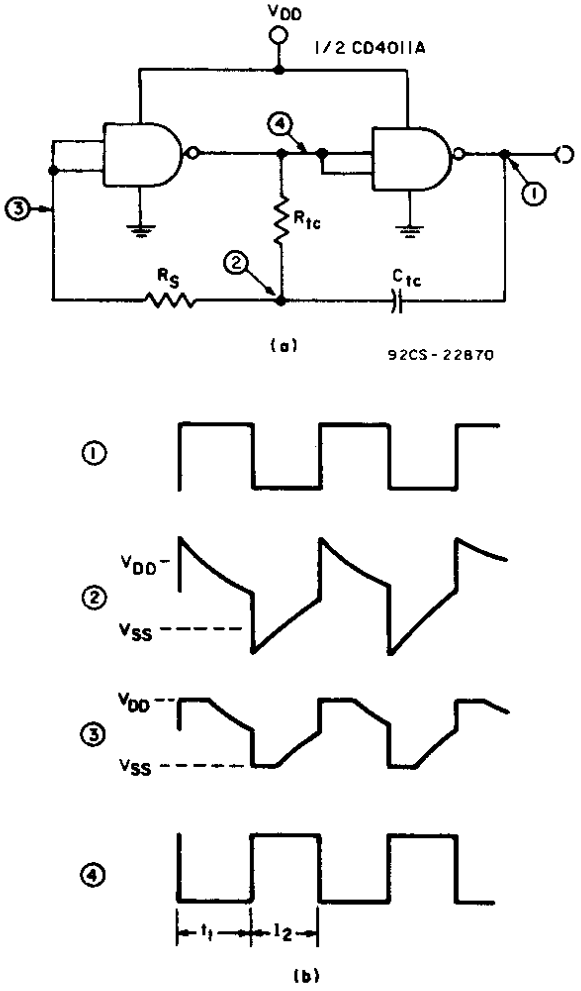


Fig. 3 - Addition of resistor in series with input to one COS/MOS inverter to make oscillator circuit independent of supply-voltage variations: (a) circuit diagram; (b) voltage waveforms.

Fig. 4 shows a typical transfer characteristic as a function of temperature. It can be seen that there is very little change in the characteristic from low to high temperature. Because the oscillator can also tolerate changes in the transfer characteristic without frequency instability, it requires no thermal compensation. The frequency at -55°C is the same as at +125°C. Table II shows data measured on typical units at temperature extremes.

Table I - Frequency variations of astable multivibrator with and without series resistor.

Unit No.	V_{tr} @ V_{DD} = 10V (V)	Period Without Rs - (ms)			Period With Rs - (ms)		
		V_{DD} = 6V	V_{DD} = 10V	V_{DD} = 14V	V_{DD} = 6V	V_{DD} = 10V	V_{DD} = 14V
2	4.77	0.735	0.66	0.645	1.04	1.00	1.02
6	5.78	0.715	0.665	0.63	1.06	1.04	1.03
11	5.58	0.695	0.66	0.625	1.03	1.02	1.03
13	5.00	0.70	0.665	0.64	1 03	1.01	1.02
20	5.56	0.70	0.665	0.64	1.04	1.03	1.03

R_{tc} = 0.4 megohm, C_{tc} = 1000pF, R_S = 0.8 megohm

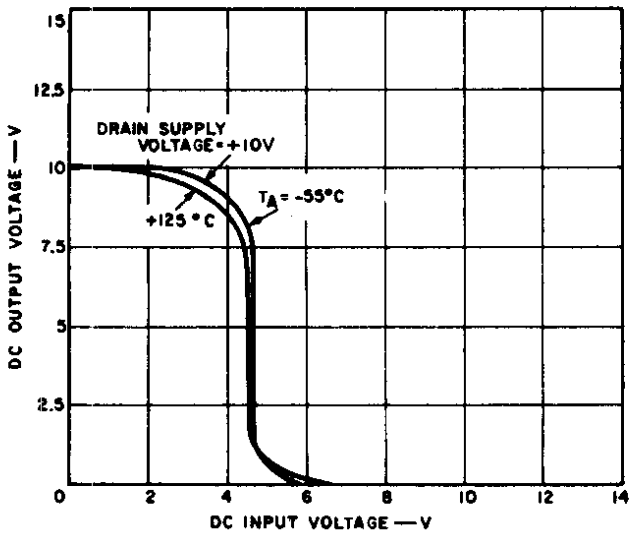


Fig. 4 - Transfer characteristic as a function of temperature.

The astable multivibrator shown in Fig.1 can be gated on the off by use of a NOR gate as the first inverter, as shown in Fig.5.

Table II - Frequency variations of astable multivibrator at temperature extremes.

Unil No.	Period - (ms)					
	V_{DD} = 6V		V_{DD} = 10V		V_{DD} = 14V	
	-55°C	+125°C	-55°C	+125°C	-55°C	+125°C
2	1.04	1.04	1.02	1.01	1.03	1.02
6	1.06	1.07	1.06	1.04	1.04	1.03
11	1.03	1.03	1.04	1.02	1.04	1.01
13	1.02	1.02	1.02	1.02	1.03	1.01
20	1.04	1.03	1.04	1.03	1.04	1.02

R_{tc} = 0.4 megohm, C_{tc} = 1000pF, R_S = 0.8 megohm

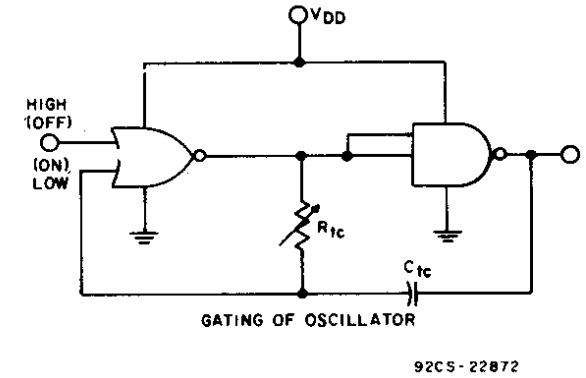


Fig.5 — Astable multivibrator in which a NOR gate is used as the first inverter to permit gating of the multivibrator. The NOR and NAND gates can also be reversed with suitable change in control polarity.

COMPENSATION FOR 50-PER-CENT DUTY CYCLES

The variation in transfer voltage described above affects the output-pulse duty cycle, as shown in Fig. 6. A true square-wave pulse is obtained only when the transfer voltage

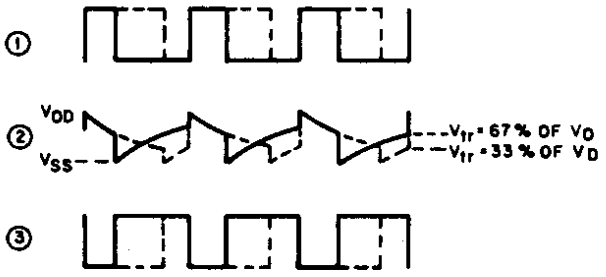


Fig. 6 - Waveforms showning effects of transfer voltage on multivibrator frequency.

occurs at the 50-per-cent point. However, the duty cycle can be controlled if part of the resistance in the RC time constant is shunted out with a diode, as shown in Fig. 7. Because adjustment of this diode shunt to obtain a specific pulse duty factor causes the frequency of the circuit to vary, a frequency control R_3 is added to compensate for this variation. It may also be necessary to reverse the diode to obtain the desired duty factor. The frequency of any of the circuits shown can be made variable by use of a potentiometer for resistor R_{tc}.

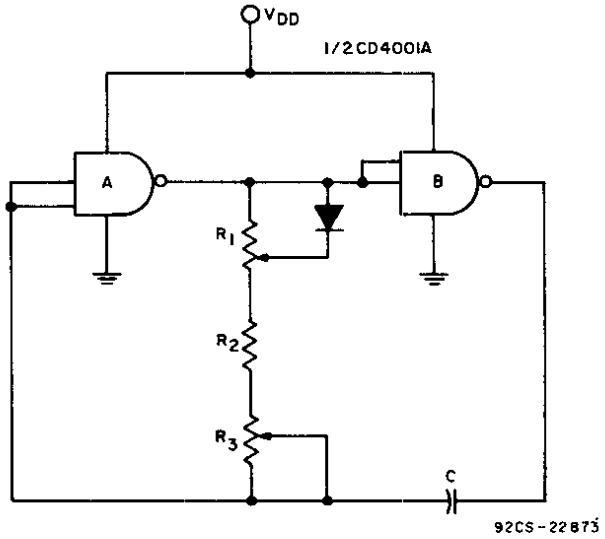


Fig. 7 - Astable multivibrator in which a duty-cycle control is added.

MONOSTABLE CIRCUITS

Basic Configuration. Fig. 8(a) shows a basic "one-shot" circuit that uses a single RC time constant. This circuit operates well provided it is adjusted to the particular COS/MOS unit used. If no adjustment is made, however, the period T can vary from unit to unit by as much as -40 per cent to +60 per cent if the transfer voltage varies by ±33 per cent, as shown by the waveforms in Fig. 8(b).

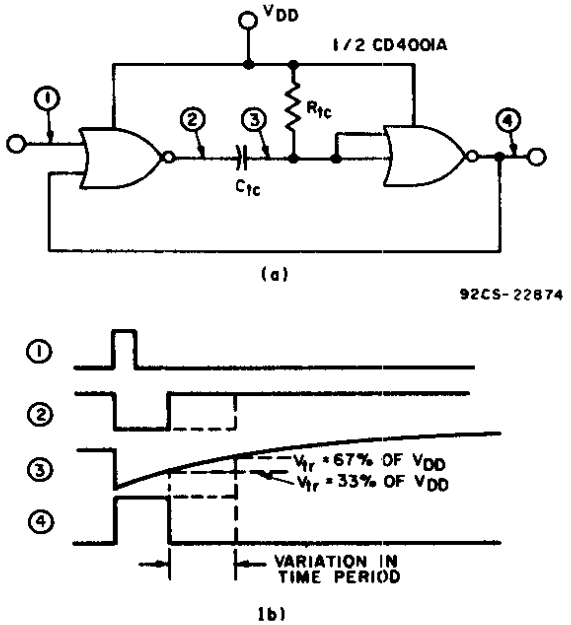


Fig. 8 - Basic one-shot multivibrator circuit: (a) circuit diagram; (b) waveforms.

Compensated Monostable Circuit. Fig. 9 shows a compensated monostable multivibrator type of circuit that can be triggered with a negative-going pulse (V_{DD} to ground). In the quiescent state, the input to inverter A is high and the output low; therefore, the output of inverter B is high. When a negative-going pulse or spike is introduced into the circuit, as

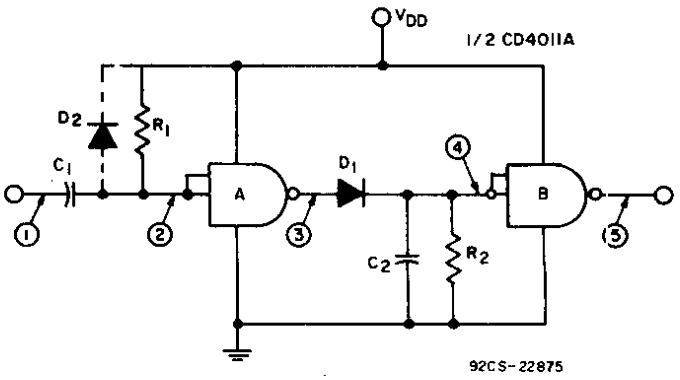


Fig. 9 - Compensated monostable multivibrator circuit.

shown in the waveforms of Fig. 10, capacitor C_1 becomes negatively charged to ground and the output of inverter A becomes high. Capacitor C_2 then charges to V_{DD} through the diode D_1 and inverter A, and the output of inverter B becomes low. As capacitor C_1 discharges negatively, it charges through resistor R_1 to V_{DD} (waveform 2). The output of inverter A remains high until the voltage waveform generated by the charge of C_1 passes through the transfer voltage of inverter A; at that instant its output becomes low. Diode D_1 temporarily prevents the discharge of capacitor C_2, which was charged when inverter A was high (waveform 3). Capacitor C_2 then commences to discharge to ground through resistor R_2 (waveform 4). The output of inverter B remains low until the waveform generated by the discharge of C_2 passes through the transfer voltage point of inverter B; at that point the output returns to its high state (waveform 5).

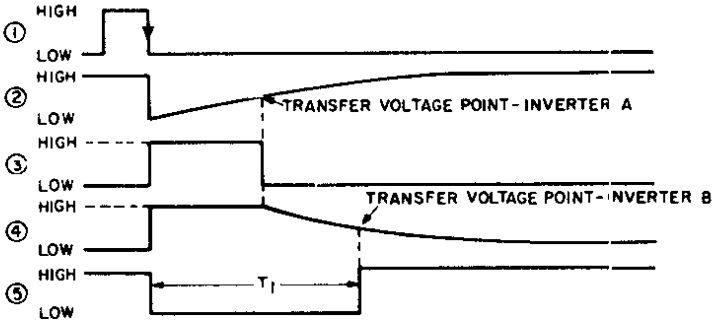


Fig. 10 - Voltage waveforms for monostable multivibrator circuit when a negative-going trigger pulse is applied.

The advantage of using two gates connected as inverters fabricated on the same chip is that they have similar transfer voltages. When two equal RC time constants are used (R_1C_1 equals R_2C_2), the effects of variations in transfer voltage from device to device are effectively cancelled out, as shown in Fig.11. By use of Eq.(1) derived for the astable oscillator, it can be shown that the maximum variation in the time period T is less than 9 per cent. The total time for one period T_1 is approximately 1.4 times the R_1C_1 time constant.

Unlike the astable circuit, which shows no variation in frequency over the temperature range from-55°C to +125°C,

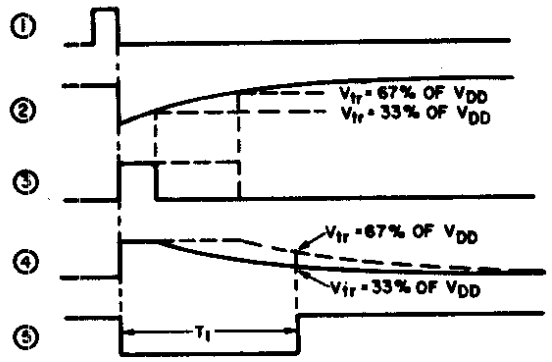


Fig. 11 - Waveforms showing the cancelling effects of transfer-voltage variations of the two COS/MOS inverters when two equal time constants are used.

the monostable multivibrator shows some change in time period. The variation is less than 10 per cent. Table III shows data measured on five units over the temperature range. At 25°C, the variation in the time period T from unit to unit is quite small, usually less than 5 per cent at a V_{DD} of 10 volts.

The output from inverter B can be held in the low or zero state as long as the R_2 C_2 time constant is recharged by another triggering pulse before the discharge waveform it generates passes through the transfer voltage of inverter B.

Table III - Frequency variations of monostable multivibrator at three temperatures.

Unit No.	Period @ V_{DD} = 10V - (ms)		
	-55°C	+25°C	+125°C
2	1.06	1.08	1.00
6	1.015	1.03	0.99
11	1.00	1.02	0.98
13	1.01	1.03	0.97
20	1.02	1.02	0.99

$R_1 = R_2 = 1$ megohm, $C_1 = C_2 = 0.001\mu F$

Diode D_2 in Fig. 9 is internal to the COS/MOS circuit. As discussed for the astable oscillator, it is part of the input protection circuit shown in Fig. 2, and serves to clamp the input at V_{DD}.

Figs. 12 and 13 show two variations of the monostable circuit, together with their associated waveforms. The circuit of Fig. 12 triggers on the negative-going excursions of the input pulse, in the same manner as the circuit of Fig. 9. The output pulse is positive-going and is taken from the first inverter. This circuit does not need an external diode. The circuit of Fig. 13 triggers on the positive-going excursion of the input pulse, and then locks back on itself until the RC time constants complete their discharge. The circuits of Figs. 12 and 13 cannot be retriggered until they return to their quiescent states.

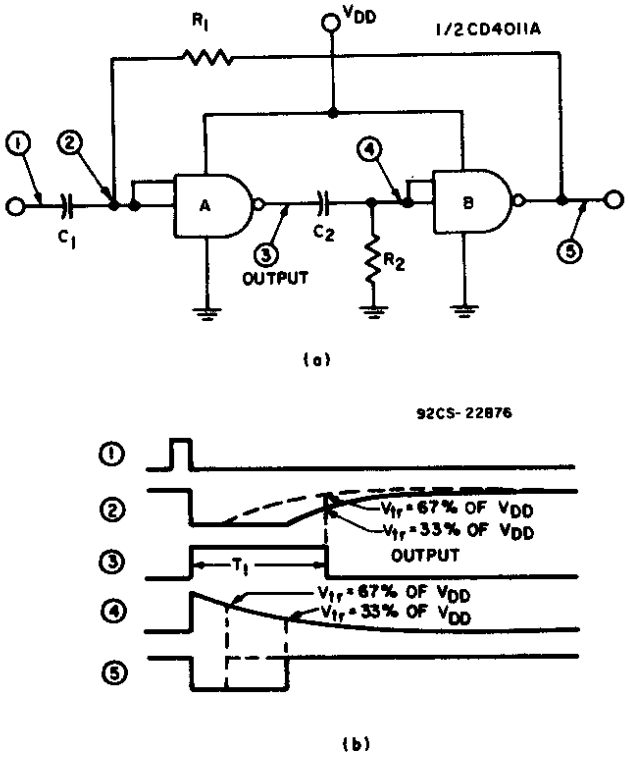


Fig. 12 - Monostable multivibrator that is triggered by a negative-going input pulse: (a) circuit diagram; (b) waveforms.

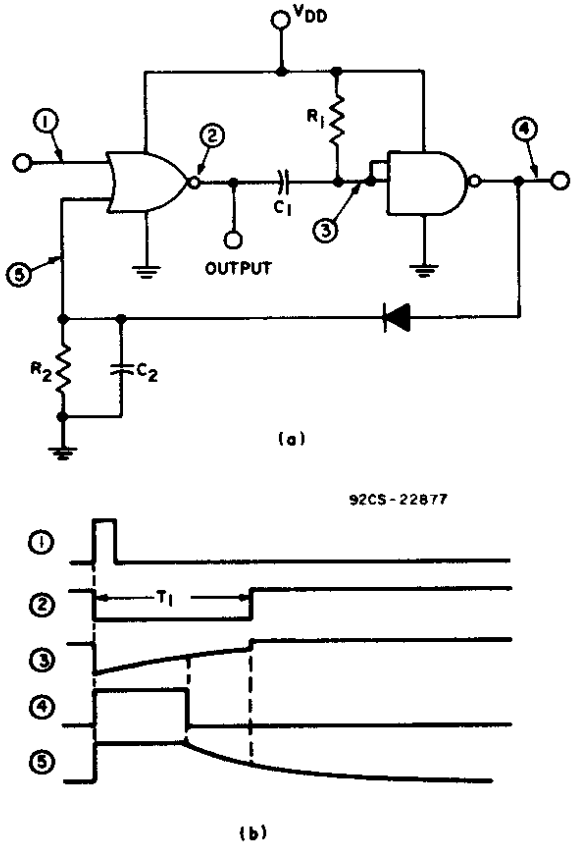


Fig. 13 - Monostable multivibrator that is triggered by a positive-going input pulse: (a) circuit diagram; (b) waveforms.

Low-Power Monostable Circuit. The monostable circuits discussed thus far dissipate some power because one or both of the inverters are on during the charging or discharging of the RC time constants. This power dissipation will be extremely low provided the "one-shot" pulse width is short compared to the over-all cycle time. Fig. 14 shows the current waveform associated with the circuit of Fig. 9. This

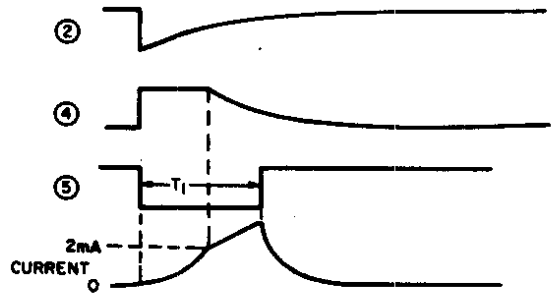


Fig. 14 - Current waveforms for the diode-compensated multivibrator shown in Fig. 9.

waveform is quite wide at the base, and some current flows for approximately twice the time period. Fig. 15(a) shows a circuit using the CD4007A which dissipates much less power than the other circuits shown, but does not have the same stability. This circuit operates as shown by the waveforms in Fig.15(b). In the quiescent state, the p-channel transistor of the first inverter is biased off, while the n-channel transistor (which derives its control from the output of the second inverter) is biased on. Therefore, the output at C is low, and that at D is high. When a negative-going pulse is introduced into the circuit through capacitor C_1, the R_1C_1 time constant becomes negatively charged, and the p-channel device is turned on. Capacitor C_2 then charges to V_{DD}, the output at D becomes low, and the n-channel device of the first inverter is turned off. Capacitor C_1 immediately begins to charge to V_{DD} through R_1 (waveform B). The p-channel transistor remains on, keeping capacitor C_2 charged to V_{DD}, until the waveform generated passes through its threshold voltage level and turns it off. The n-channel transistor of the first inverter is still off because the output of the second inverter (waveform D) is still low. When the p-channel device of the first inverter turns off, capacitor C_2 begins to discharge through resistor R_2 (waveform C) to ground. As it discharges, it passes through the threshold voltage of the second p-channel transistor so that it begins to turn on. The voltage waveform at D then begins to rise, and the n-channel device of the first inverter turns on and provides a second discharge path for the capacitor C_2. As a result, the output waveform changes state from low to high quite rapidly to complete the cycle.

The major advantage of the circuit of Fig. 15 is its low power dissipation. Because the circuit depends on the p-channel transistor threshold, the time period T varies from unit to unit or with temperature variations. Some compensation can

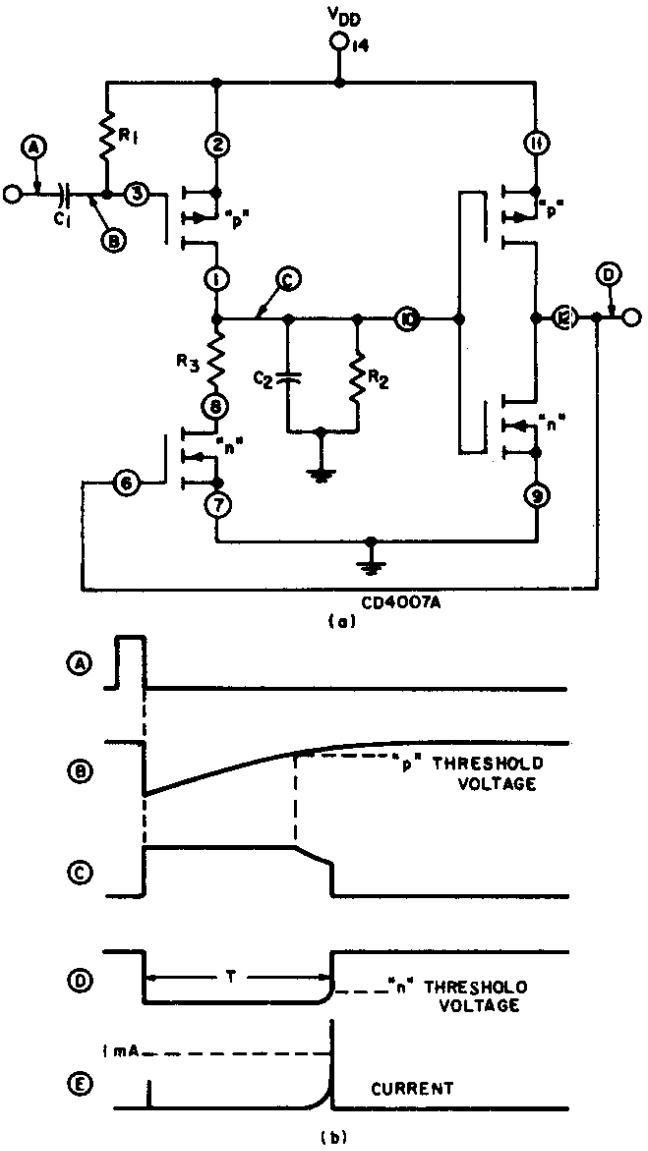


Fig. 15 - Low-power monostable multivibrator: (a) circuit diagram; (b) waveforms.

be provided if the R_2C_2 time constant is made approximately 3 times larger than the R_1C_1 time constant, as shown in Table IV.

Table IV - Frequency variations of monostable multivibrator with temperature when R_2C_2 time constant is increased.

Unit No.	Period with V_{DD} = 10V - (μs)		
	-55°C	+25°C	+125°C
553	1090	1120	1160
554	1060	1090	1120
810	1030	1030	1020
900	1000	1020	990
939	1080	1100	1050

R_1 = 0.35 megohm, C_1 = 0.001μF

R_2 = 1 megohm, C_2 = 0.001μF

R_2C_2 is approximately 3 times the time constant R_1C_1

R_3 = 4700 ohms

For minimum current in the circuit of Fig. 15, capacitor C_2 can be removed so that only stray capacitance is present at the input of the second inverter. A comparison of time-period variations under this condition is shown in Table V. Again, the variations from unit to unit are caused by differences in p-channel transistor threshold.

Table V - Frequency variations of monostable multivibrator with temperature when C_2 consists of stray capacitance only.

Unit No.	Period with V_{DD} = 10V - (μs)		
	-55°C	+25°C	+125°C
553	878	948	1820
554	900	978	1058
810	900	1000	1088
988	818	880	968
939	788	850	928

R_1 = 8.62 megohm, C_1 = 0.001 μF
R_2 = 1 megohm, C_2 = strays

Applications

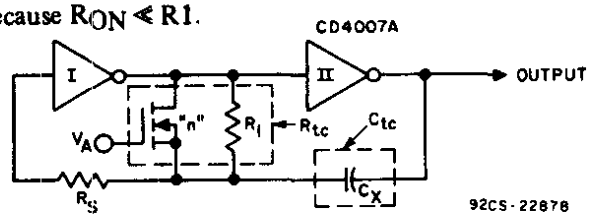
Fig. 16 shows a circuit similar to the circuit in Fig. 3a. C_{tc} is variable (by adjustment of C_X) and R_{tc} is variable (by adjustment of V_A). The value of R_{tc} varies from $\approx$ 1kΩ to 10kΩ. These limits are determined by the parallel combination of R1 (10kΩ) and the n-channel device resistance. This varies from 1kΩ (R_{ON}) to $\approx 10^9\Omega$ (R_{OFF}).

When $V_A = V_{SS}$, the n-channel device is "OFF" and $R_{tc} = R_{OFF}/\!/R1 \approx R1 = 10k\Omega$

because $R_{OFF} \gg R1$.

When $V_A = V_{DD}$, the n-channel device is fully "ON.. and $R_{tc} = R_{ON}/\!/R1 \approx R_{ON} = 1k\Omega$

because $R_{ON} \ll R1$.



NOTE:
INVERTERS AND n-CHANNEL DEVICE ARE AVAILABLE IN A SINGLE COS/MOS PACKAGE: CD4007A[1]

TYPICAL VALUES:
R_1 = 10 kΩ C_X = 0.001 - 0.004 μF
R_S = 100 kΩ $0 \le V_A \le V_{DD}$

* USE PROPER SUFFIX TO DENOTE PACKAGE REQUIRED - SEE APPENDIX

Fig. 16 – Voltage-controlled oscillator.

The oscillator center frequency is varied by adjustment of C_X. Table VI shows a comparison of the period of the output waveform as a function of V_{DD} and V_A.

Table VI - Period of Output as a function of Va and V_{DD} - V.C.O. of Fig. 16.

V_A	Period (μsec)		
	V_{DD} = 5V	V_{DD} = 10V	V_{DD} = 15V
0	120	54	48
5	115	45	41
10	---	32	30
15	---	---	24

Voltage-Controlled Pulse-Width Circuit

Fig. 17a shows a further modification of the circuit of Fig. 3a which modulates the pulse width (by varying V_A) only if R_X is sufficiently high. As an example; if C = 0.0022μF, then $R_X \approx 35k\Omega$. Lower values of R_X cause the frequency to be affected. If $R_X < 10k\Omega$, there is a value of V_A which will cause the oscillator to cut off. Table VII lists values of pulse width (B in Fig. 17b) for various values of V_A and V_{DD}. Fig. 17b shows the output waveform for the circuit described.

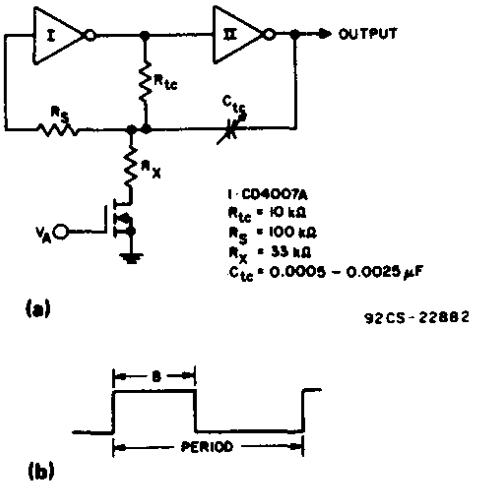


Fig. 17 - (a) V.C. pulse-width circuit; (b) output waveform.

Table VII - Pulse Width as a Function of V_A and V_{DD}.

V_A	Pulse Width (B) μsec		
	V_{DD} = 5V Period-41.5	V_{DD} = 10V Period-35	V_{DD} = 15V Period-33
0	23	19.3	17
5	20	17.7	16.2
10	---	16.2	15.5
15	---	---	14.3
C_{tc} = 0.0015μF			

Phase Locked VCO

The voltage controlled oscillator can be operated as a phase locked oscillator by the application of a frequency controlled voltage to the gate of the n-channel device. Fig. 18 shows the block diagram an FM discriminator using the phase locked VCO. Block A is the same circuit as Fig. 16. The output of the phase comparator is fed to the gate of the n-channel device (V_A). If the two inputs to the phase comparator are different, the change of V_A causes the output frequency of the VCO to change. This change is divided by 2^N and fed back to the phase comparator.

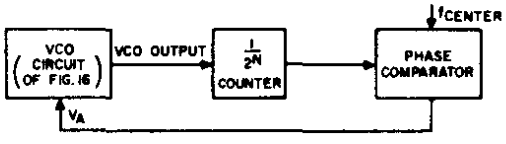


Fig. 18 – VCO used in phase-locked loop.

Frequency Multipliers

Fig. 19a shows a frequency doubler. A 2^N multiplier can be realized by cascading this circuit with N-1 other identical circuits. The leading edge of the input signal is differentiated by R1 and C1, applied to the input No. 1 of the NAND gate, and produces a pulse at the output. The trailing edge of the input pulse, after having been inverted, is differentiated, applied to the input No. 2 of the NAND gate, and produces the second output pulse from the NAND gate. The waveforms for 5 points in the circuit are shown in Fig. 19b.

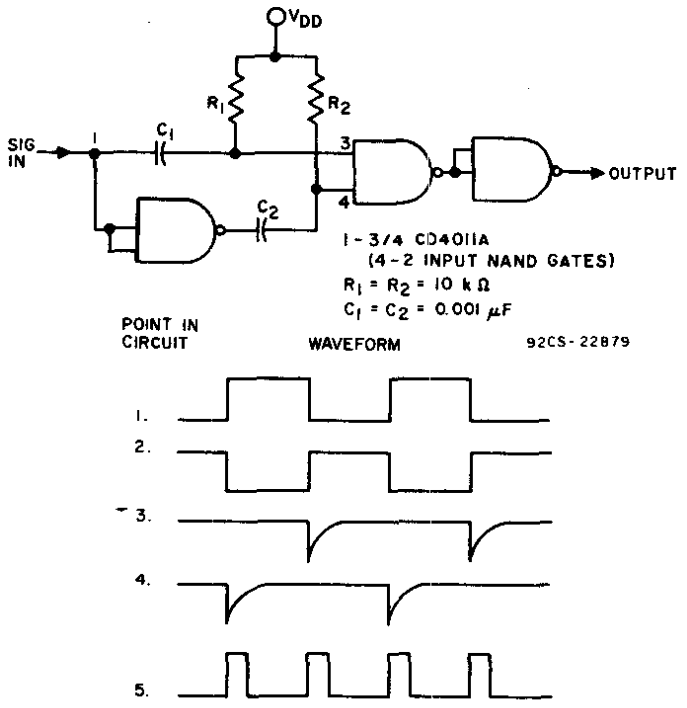
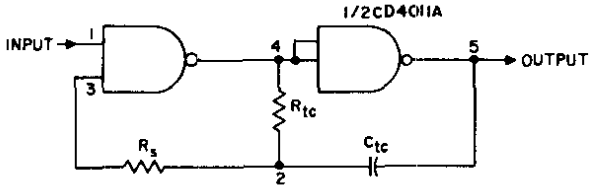


Fig. 19 - (a) Frequency doubler schematic; (b) waveforms.

Modulation/Demodulation (Envelope Detection).

Pulse modulation may be accomplished by use of the circuit shown in Fig. 20a. This circuit is a variation of Fig. 3. The oscillator is gated ON or OFF by the signal input No. 1 to the NAND gate. The waveforms are shown in Fig. 20b.



Demodulation or envelope detection of pulse modulated waves is performed by the circuit shown in Fig. 21a. The carrier burst is inverted (by Inverter A), and its first negative transition at point 2, turns on the diode (D) to provide a charging path for C_{tc} through the n-channel resistance to ground. On the positive transition of the signal (at point 2), the diode is cut off and C_{tc} discharges through R_{tc}. The discharge time constant (R_{tc} C_{tc}) is much greater than the time of the burst duration. Point 3, therefore, never reaches the switch point of inverter B until the burst has ended. The waveforms for 4 points in the circuit are shown in Fig. 21b.

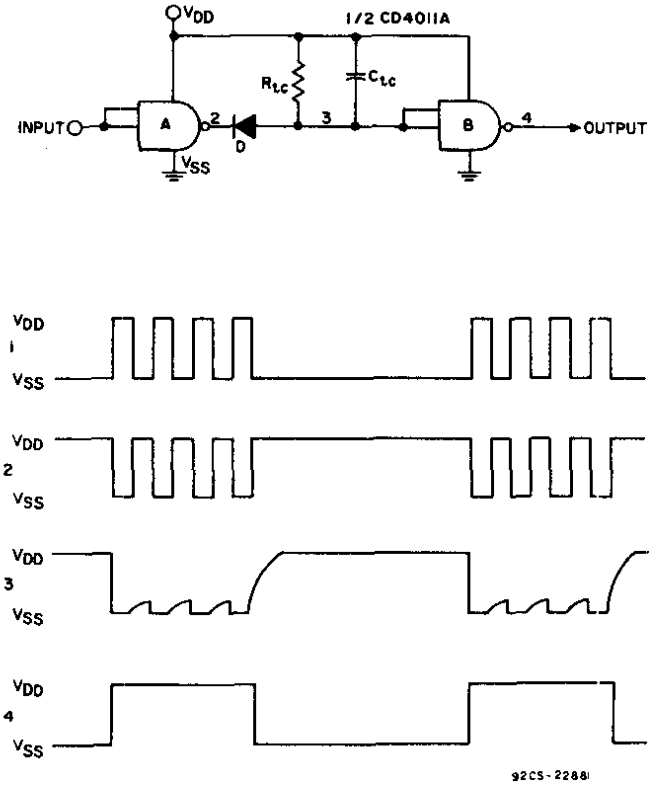


Fig. 21 - (a) Demodulator circuit; (b) waveforms.

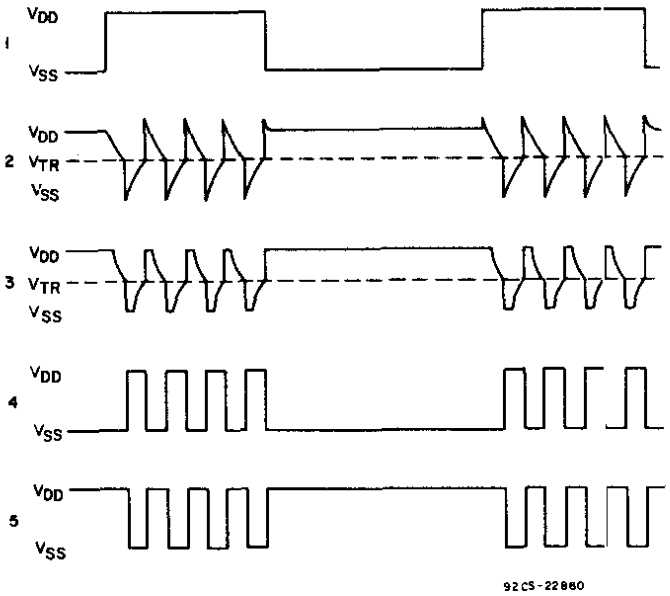


Fig. 20 - (a) Modulator circuit; (b) waveforms.