SBC-85 8085 Single Board Computer

This user's guide describes the SBC-85 Single Board Computer

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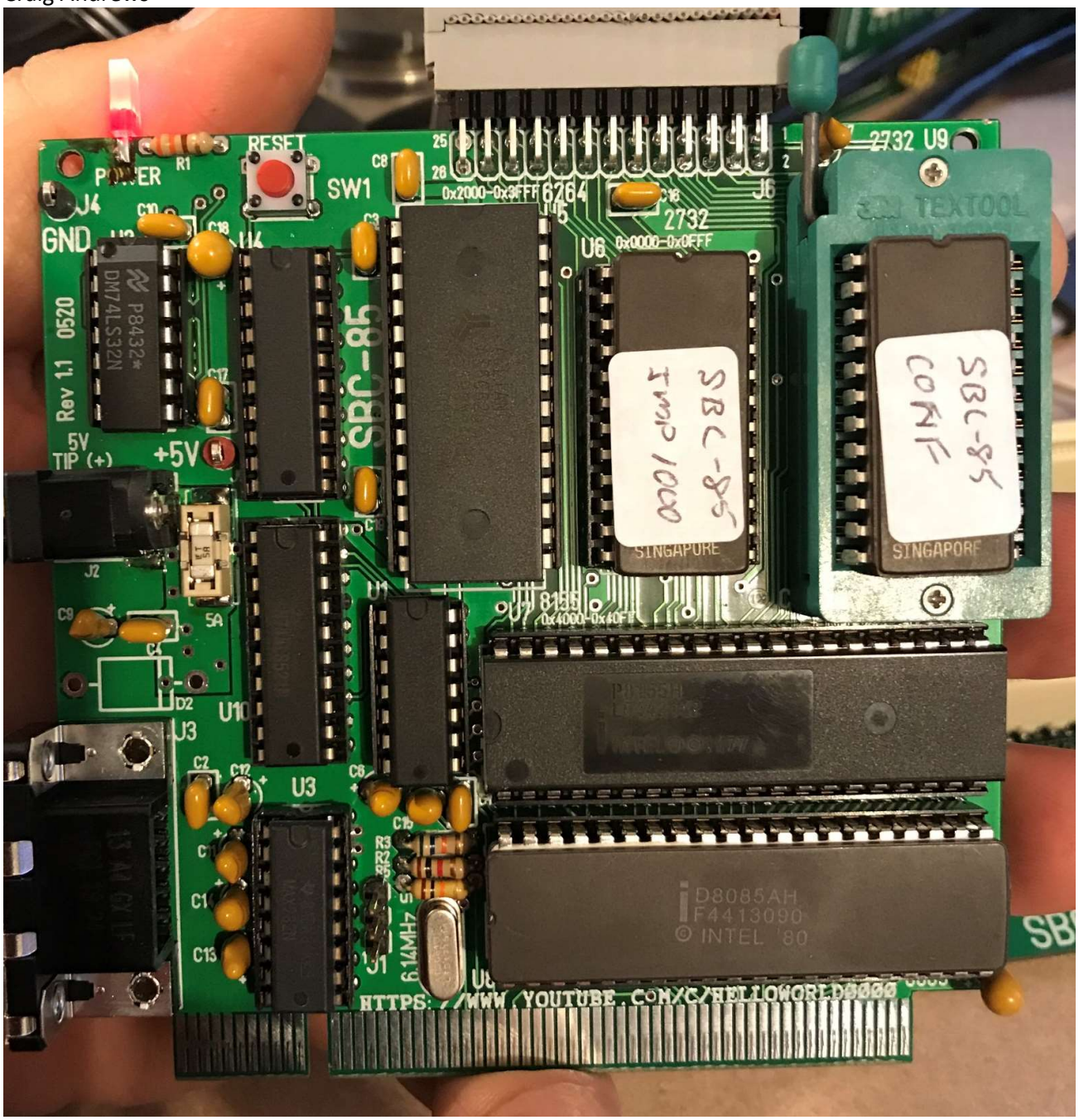


Notation:

Pin numbers. Pin numbers are given as ***ID.pin***. for example, Pin 5 of connector X3 is given as ***X3.5***. IC7 pin 21 is given as ***IC7.21***.

Logic Levels. Lines having a signal that is active low is given with either an asterisk or a slash following the signal name. For example, **CS8/** and **CS11*** both refer to signals that is active when at 0V or logic low.

Terminology:

Most abbreviations will be spelled out when they are first used. However, the more commonly used terms are described in the ***Definitions of Terms and Notations*** at the end of the document.

SBC-85 DESCRIPTION

The SBC-85 is an 8085 based Single Board Computer. As such, it contains all elements required for stand-alone operation including the processor, Random Access Memory (RAM) and Read Only Memory (ROM or EPROM). The SBC-85 also includes an RS232 Serial port with a female DB9 connector for communication. Finally, the board includes an expansion bus for insertion into a backplane.

The primary components on the SBC-85 are as follows:
U8 - 8085 Microprocessor operating at 3MHz
U6 – Base EPROM
U9 – Expansion EPROM ZIF socket
U5 – 6264 64Kbit RAM (address 0x2000 thru 0x3FFF)
U7 – 8155 RAM, I/O, Timer (address 0x4000 thru 0x4500)
U3 – MAX232 TTL / RS232 Level Shifter

Additional 'glue logic' includes the following:
U2 – 74LS32 Quad 2-input OR gate for address decoding
U4 – 74HCT573 Octal Latch for AD0-AD7 latching to form A0-A7
U10 – 74HCT521 or 74LS682 (version dependent) Equality Comparator 8155 address decoder

CIRCUIT DESCRIPTION

8085

The 8085 microprocessor needs only +5VDC and a oscillator input to operate. On the SBC-85, the oscillator input is provided by Q1 which is a 6.144MHz crystal. The 8085 immediately begins fetching instructions from address 0x0000 upon power up, however the power up must be somewhat controlled to allow the 8085's internal charge pump to build sufficient charge before the CPU fetches its first instruction. Because of this, the 8085 needs a slight delay in the release of its ResetIN* after power up. This is accomplished by the RC circuit which is a 56K (R2) bleed into a 1uF (C15) capacitor. After power is applied, this circuit takes around 80 uS to reach a logic high on RESETIN*, and releasing the CPU from reset.

Once out of reset, the CPUs operation is controlled by its READY, HOLD, and TRAP inputs. The READY is primarily intended as a means of an external circuit pausing the CPUs operation so it can "catch-up", e.g., so slow memory or a slow I/O port can stop the CPU until it can complete a requested action. Therefore, for the CPU to operate the READY must be TRUE, or logic one. This is accomplished by (10k) pull-up resistor R7. The HOLD input is a similar means of stopping the CPU, but its use is to stop the 8085 from operating in order to allow another device to take control of the system. This is commonly used in systems having multiple CPUs or sub-circuits that operate autonomously such as Direct Memory Access (DMA), Disk Drive Interfaces, etc. Like the READY, the HOLD must be held inactive but in this case that is logic zero and is accomplished by a (10k) pull down resistor R5. Finally, the 8085's operation can be interrupted by hardware inputs, namely the TRAP, RST7.5, RST6.5, and RST5.5. Of these all are disabled when the processor first starts except for the TRAP which cannot be masked or turned off. The TRAP input to the 8085 must be held low to prevent the CPU from attempting to fetch an instruction from the memory location 0x0024. This is accomplished by R6 (10k) pull down resistor. **Therefore, for the 8085 to operate the R5, R6, and R7 must be installed.**

ADDRESS LATCH

The 8085 has 16 address lines and can therefore access 2^{16} locations or 65536 address (a.k.a. 64KB) of memory. During each memory access the 8085 first puts all 16 addresses onto the output bus, but the lower 8-bits (AD0-AD7) are only held for a short period before those eight lines are used to transfer the data byte. While the lower address byte is transient, most components require that the lower 8 address bits be continuously available throughout the

machine instruction. This is accomplished by U4 which is an 8-bit (octal) latch which takes the transient input of AD0-AD7 and creates a sustained A0-A7. AD0-AD7 are latched on the falling edge of the 8085's Address Latch Enable (ALE) signal. In operation, the 8085 puts the lower address byte on AD0-AD7 and raises the ALE signal and the AD0-AD7 logic levels exit the latch on Q1-Q8 onto the A0-A7 address lines. After enough time is given for these signals to propagate and stabilize, the 8085 lowers the ALE signal and the values are latched onto the A0-A7 signals. When combined with the A8-A15 signals, which the 8085 is still holding, the rest of the system now has a sustained A0-A15 address.

ADDRESS DECODING

As the 8085 microprocessor outputs addresses for memory locations or I/O ports, a portion of the circuit known as an *address decoder* determines which addresses are in which component. As its name implies, the address decoder uses the address output from the 8085 onto the A0-A15 address bus and compares this address to the system *address map*. As the result of the comparison, while there may be several components connected to the same data bus, only a single device will be selected to communicate with the CPU.

☞ BIG, BIG WARNING. THIS WILL TRIP SOMEONE UP- Note that the IO or Memory (IO/M*) signal from the 8085 is not used in the address decoding on any version of the CPU board. This means that there *must* be no overlap for I/O ports and Memory (except for devices such as the 8155 which decode the IO/M* signal themselves). On the 8085 the I/O port number is duplicated on the low and high bytes of the address, i.e., without the IO/M* line Port 32H is decoded the same as address 3232H. Make sure all I/O ports are placed in memory holes that are not decoded and selected by the SBC-85 CPU. See *Memory Mapped I/O* and *I/O Mapped I/O* in the definitions for additional explanation.

V2.x ADDRESS DECODING

SBC-85 CPU v2.x memory and I/O is decoded as shown in the following table.

MEMORY ADDRESS MAP																			
					Address Line														
ID	**Type**	**Range**	**Start**	**End**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
U6	2732	0<4K	0x0000	0x0FFF	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X
U9		4K<8K	0x1000	0x1FFF	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X
U6	2764	0<8K	0x0000	0x1FFF	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X
U9		8K<16K	0x2000	0x3FFF	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X
U6	27128	0<16K	0x0000	0x3FFF	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X
U9		16K<32K	0x4000	0x7FFF	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X
U9	27256	0<32K	0x0000	0x7FFF	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
U5	6264	32K<40K	0x8000	0x9FFF	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X
U7	8155	40K<41K	0xA000	0xA0FF	1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	X
		C/S	0xA0		1	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0
		I/O Port A	0xA1		1	0	1	0	0	0	0	1	1	0	1	0	0	0	0	1
		I/O Port B	0xA2		1	0	1	0	0	0	1	0	1	0	1	0	0	0	1	0
		I/O Port C	0xA3		1	0	1	0	0	0	1	1	1	0	1	0	0	0	1	1
		Timer LSB	0xA4		1	0	1	0	0	1	0	0	1	0	1	0	0	1	0	0
		Timer MSB	0xA5		1	0	1	0	0	1	0	1	1	0	1	0	0	1	0	1

6264 RAM Selection

The description of the decoding circuit will begin with the 6264 RAM. To completely decode the 64kbits inside this chip requires 13 address lines as shown on the schematic as A0-A12. Since these 13 lines are required to decode the contents *inside* the chip, there are only three address lines left to decode the address space used *by* this chip. These address lines are A15, A14, and A13. The above table shows that the 6264 has been placed in the address space where A15-13 are 1, 0, and 0 respectively, so any address where the first three address lines are 100, i.e., 100x xxxx where the 'x' are address lines that are used to decode the specific byte inside the chip. In other words, the 6264 needs to be enabled whenever A15=1 and the other two are equal to logic '0'. As can be seen in the schematic, A13 and A14 are inputs to U2A, 2-input OR logic gate whose output will only be a logic low when the two inputs are at logic low. The output of this gate creates the 6264_CE* signal that is connected to the 6264 CE1* which is U5.20 so the 6264 will not be enabled unless this is low, which only occurs when A13 and A14 are low. The final requirement is that A15 be at logic one which is easily accomplished by connecting A15 to CE2 pin U5.26. Since CE1* and CE2 must both be active for the 6264 to be enabled, this completes the required decoding for U5.

In operation, when the address beginning with 100 is placed onto the bus, U5 becomes enabled and as the lower byte of the address is latched with the ALE signal the RAM then writes the data into memory at the completion of the WR* strobe or it reads from memory and places onto the AD bus during the RD* strobe.

8155 RAM and I/O Selection

The 8155 is decoded using address matching of A15-A11 by U10 74LS682 8-bit equality detector. This device is hardwired to match any address with the pattern 1010 0xxx xxxx xxxx, i.e., any address within the range from 0xA000 through 0xA7FF. The IOM* line is used directly by the 8155 so the ports within the 8155 are I/O mapped I/O (see definitions).

EPROM Selection

With the more flexible memory options of version 2.x, a new address decoding scheme needed to be developed. A fundamental goal is to have the EPROM memory contiguous for any of the four EPROM configurations. V2.x has two address decoding jumpers which must be set depending on which EPROM is being used on the SBC. Note that when two EPROMs are used, both EPROMs must be the same size, i.e., both 2732s, both 2764s, or both 27128s. When a 27256 is used it must be used alone and placed in the ZIF socket U9.

Jumpers JP3 and JP4 are both 1-of-four configuration with a common post in the center and the four options located at the four cardinal directions. As noted on the back silkscreen, jumper JP3 and JP4 in the top position for 2732, right for 2764, bottom for 27128, and left for 27256 EPROMS.

JP3 uses A15, A14, and A13 to decode ***if either*** EPROM is selected and JP4 utilizes A14, A13, and A12 to determine ***which*** of the two EPROM is selected (if any).

For the second part of this (*which* EPROM), the selection between the base and expansion EPROM is provided by the 2-input OR gates U2C and U2D. Both of these gates have one input driven by the U2B output. The second input of one gate is driven directly by the selection of JP4 and the second input of the other gate driven by the inverted selection of JP4. In this manner, the chip select for the base or expansion EPROMs are complementary, i.e., whenever the U2B signal is enabled (low) one and only-one EPROM is selected according to JP4 output.

2732

When JP3 is placed in the 2732 position, U2A and U2B require that all of A15, A14, and A13 be low to enable the EPROMs. This places both EPROMS at address 000x and below. The selection between the 2732As is provided when JP4 selects A12 as the deciding factor between the base and expansion EPROM. As described in the previous paragraph, A12 into U2C along with the output of U2B enables the base EPROM when A12 is low (0x0000-0x0FFF) and A12 is inverted by U1A to enable the expansion EPROM when A12 is high (0x1000-0x1FFF).

2764

When JP3 is placed in the 2764 position, A15 and A14 must both be low (A13=don't care) to select an EPROM, placing the memory anywhere from 0x0000-0x3FFF. JP4 uses A13 to select which of the two EPROMs is selected with A13=0 selecting the base (0x0000-0x1FFF) and A13=1 selecting the expansion (0x2000-0x3FFF)

27128

When JP3 is placed in the 27128 position only A15 is used to select an EPROM (A14 & A13= Don't care), placing the memory anywhere from 0x0000-0x7FFF. JP4 uses A14 to select which of the two EPROMs is selected with A14=0 selecting the base (0x0000-0x3FFF) and A14=1 selecting the expansion (0x4000-0x7FFF)

27256

Only a single 27256 can be used, the base EPROM socket must be unpopulated. Since the total memory of the 27256 is the same as the pair of 27128s, the address decoding is nearly the same as the previous paragraph. When JP3 is placed in the 27256 position only A15 is used to select the EPROM (A14 & A13= Don't care), placing the memory anywhere from 0x0000-0x7FFF. JP4 is always taken high so the base EPROM chip select is always low and only the expansion EPROM chip select is controlled by A15. Therefore, the expansion ZIF socket is always selected from 0x0000 through 0x7FFF.

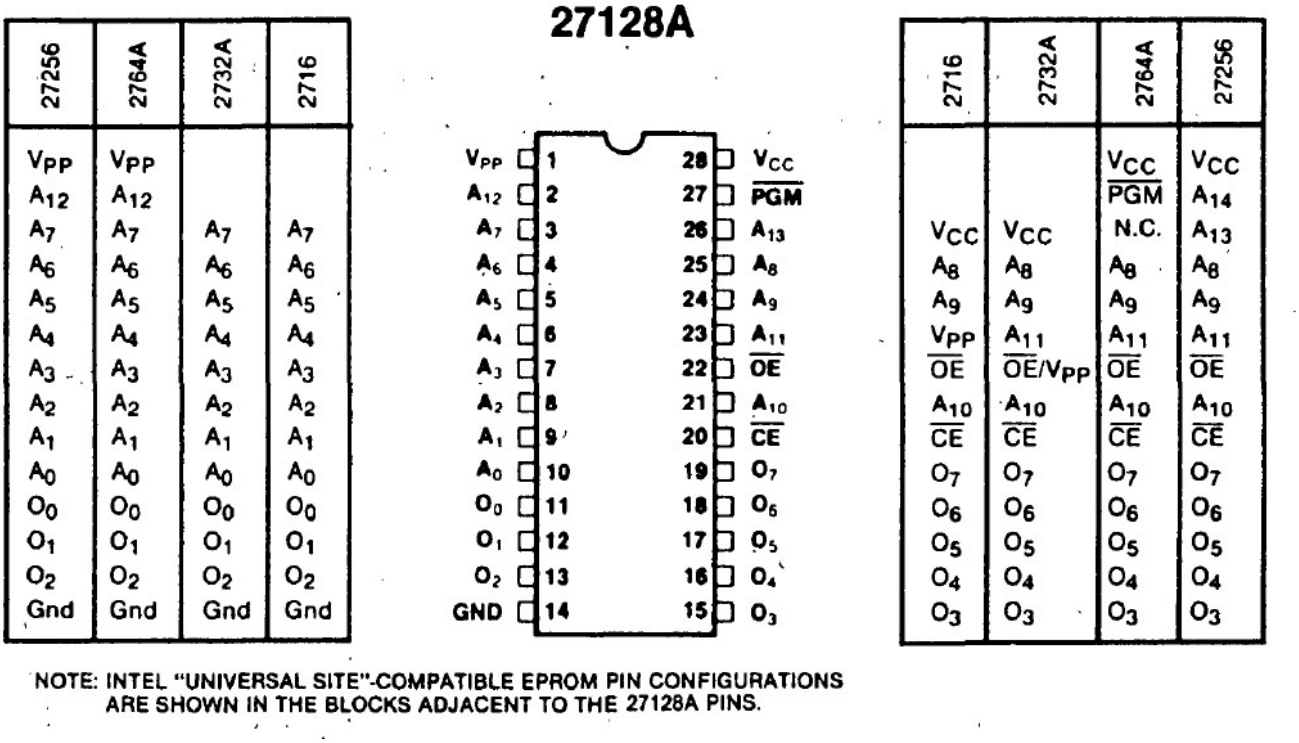
The EPROM address selection is summarized in the following table.

	EPROM TYPE			
JUMPER	**2732②**	**2764②**	**27128②**	**27256③**
JP3① & JP4①	2-1	2-4	2-3	2-5
JP5	2-3	NA	2-1	2-1

JP6	NA	2-3	2-3	2-1
NOTES: ①JP3 and JP4 MUST be in the same configuration ② U6 and U9 must be the same type of EPROM ③ Only one 27256 and must be in U9				

V2.x UNIVERSAL EPROM SOCKETS

Nearly from the very beginning, the industry recognized that the ever-increasing availability of larger and larger ROM devices was going to be problematic if a standard was not adopted. The design scheme resulted in the "Universal Site" Socket concept in-which all future ROMs, PROMs, and EPROMs would have pin mapping such that, with minor adjustments, the different sizes of EPROMS were compatible if bottom justified in the socket. The following graphic (lifted from the 1984 Intel Memory Components Handbook) is a typical example. The 27128 is shown in the center and the function of each pin on the left and the right is shown in the corresponding table on each side.



NOTE: INTEL "UNIVERSAL SITE"-COMPATIBLE EPROM PIN CONFIGURATIONS ARE SHOWN IN THE BLOCKS ADJACENT TO THE 27128A PINS.

For example, pin 28 (top right) is not present on the 2716 or 2732, is the power input on the 2764, 27128, and 17256 whereas pin 26 (third from top right) is actually pin 24 on a 2716 or 2732 which it is their power input.

☞UNIVERSAL SITES ARE BOTTOM JUSTIFIED- When a memory device having fewer pins than the socket, it must be bottom justified, i.e., pin 1 of the EPROM is placed in pin 3 of the socket.

JP5 and JP6 are located on the top left of the PCB near the reset switch. **WARNING**: The orientation of JP5 and JP6 changed with version 2.0a. On earlier boards, these two jumpers have pin 1 down (towards the fingers), pin 2 is the center (common pin) and pine 3 is near the top edge of the board. On v2.0b pin 1 is at the top of the board to make the orientation of JP5 and JP6 consistent with other jumpers.

Using the above universal site graphic, jumpers JP5 and JP6 can be seen to satisfy the 'minor adjustment' issues as follows.

JP5 pin 26 Power or A13

JP5 is installed in position 2-3 to connect pins 26 in both EPROM sockets to +5V, i.e., to connect pin 24 of the 2732 to power. When using 2764s, pin 26 is unused and the jumper is removed entirely. When using 27128s or a 27257 the jumper is installed between 1-2 to connect address line A13 to U6.16 and U9.26.

JP6 pin 27 ground or A14

Since pin 27 is not connected in a 2732, the actual position of JP6 is not applicable for a 2732. For a 2764 and 27128 pin 27 is the Program* pin which must be taken to ground for normal reads so JP6 is installed 2-3 to connect pins 27 in both EPROM sockets to ground. When using 27256 in U9, JP6 is used to connect address line A14 to U9.27 as required to internally decode the EPROM.

V1.0 – V1.2 ADDRESS DECODING

On the SBC-85 this address decoding is accomplished in two ways; logic gates and an equality detector. The logic gates formed by the 2-input OR perform the simple operation of breaking the address into segments. U2b determines that if both A14 and A15 are at logic low, then the selected address is below the 16KB boundary, i.e., between 0x0000 and 0x3FFF. This signal (A0<16K*) is logically ORed (U2d) with A13 and creates an output that indicates the address is below the 8KB boundary (A0<8K*). This output is, again, ORed (U2a) with A12 to form the signal indicating that the address is below the 4kB boundary (A0<4K*). Finally, the A0<8K* signal is ORed with the inverted A12 signal (i.e., A12*) to create the final signal indicating that the address is below the 8K boundary but is above the 4K boundary, i.e., A4<8K*. Note that all of these signals are inverted, i.e., they are TRUE when at a low level. Address decoders often work with inverted logic simply because the chip select (CS*) inputs to most devices are active low.

The outputs of this address decoder is used (sometimes with other signals) to select either the 6264 RAM, the base 2732 EPROM, or the expansion 2732 EPROM. Starting with the base 2732, this device uses 4K of addresses starting at 0x0000 and ending at 0x0FFF. The A0<4K* signal is directly connected to U6.18 chip enable (CE*) input. The expansion 2732 operates in the next higher 4K address space so the A4<8K* address decoder signal is connected to U9.18 chip enable (CE*) input to select that device in this memory space.

The 6264 RAM occupies 8K of address space beginning right above the 8K address space used by the two 2732 EPROMs, i.e., from address 0x2000 thru 0x3FFF. To select the 6264 in this address space the A0<16K* signal is connected to U5.20 (CE1*). However, this alone would enable the 6264 during any address below the 16K boundary and cause bus contention where it overlaps with the two 2732s. Therefore a second (in this case active high) chip select input (CE2) is connected to A13. In effect, this combination creates an A8<16K* signal that is used to enable the 6264.

The 8155 needs 256 address locations for its RAM and an additional six address locations for its input/output and internal timer. This could have been assigned a large address block, for example, by simply using A14 to select this chip. However, that is incredibly wasteful since it would dedicate 16KB of address space to a chip that is only using a few hundred. Therefore, the address decoder for the 8155 uses a targeted approach to claim the minimum amount of address space with an 8-bit equality detector. This equality detector (U10) 74LS521 has one output that goes low when the two 8-bit inputs match. For the SBC-85, the 8155 is placed in the address space right above the RAM and extending for 2K up to 0x47FF. The 8155 only uses addresses up to 0x4545 but excluding the relatively small space between 0x4545 and 0x47FF is not worth the trouble. Using the equality detector, the 8155 is enabled anytime the upper bits of the address (A15-A11) are 01000, between addresses 0x4000 and 0x7FF. Note that the reason the 8155 needs such a large address space even while it only uses 262 bytes is because during port access the port number is output not only on the low address byte but is also duplicated on the high address byte. For example, to access port 41 (8155 port A) the 8085 will place 0x4141 on the address bus.

The final address map is as shown in the following table:

MEMORY ADDRESS MAP																				
					ADDRESS LINE															
ID	**Type**	**Range**	**Start**	**End**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
U6	**2732**	**0 < 4K**	0x0000	0x0FFF	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X
U9	**2732**	**4K < 8K**	0x1000	0x1FFF	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X
U5	**6264**	**8K < 16K**	0x2000	0x3FFF	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X
U7	**8155**	**16K < 16.5K**	0x4000	0x47FF	0	1	0	0	0	0	0	0	X	X	X	X	X	X	X	X
		C/S Register	0x40		0	1	0	0	0	0	0	0	X	X	X	X	X	0	0	0
		I/O Port A	0x41		0	1	0	0	0	0	0	1	X	X	X	X	X	0	0	1
		I/O Port B	0x42		0	1	0	0	0	0	1	0	X	X	X	X	X	0	1	0
		I/O Port C	0x43		0	1	0	0	0	0	1	1	X	X	X	X	X	0	1	1
		Timer LSB	0x44		0	1	0	0	0	1	0	1	X	X	X	X	X	1	0	1
		Timer MSB	0x45		0	1	0	0	0	1	0	1	X	X	X	X	X	1	1	0

SERIAL INTERFACE (all versions)

The utility of any single board computer is severely limited if it does not have a means of communication with a terminal or external device. For this reason, Intel included two serial communication lines in the base 8085, eliminating the need for an additional UART or USART component. These are the Serial Output Data (SOD) and Serial Input Data (SID) lines. Depending on the preferred communication standard, code is used in the 8085 to create a serial stream. In the case of the SBC-85, this is RS-232 which is a bipolar serial stream consisting of a starting bit, data bits, stop bit, and parity bit. No other hardware handshaking is used on the SBC-85. To create the bipolar output, a MAX232 (U3) is used which contains an internal charge pump to create the +/- rails necessary to meet the RS232 standard (+/- 14V typical for the MAX232). The 8085 SID and SOD lines pass through the MAX232 which inverts and level shifts the signals as required by RS232. With rails in the +/-12V range, the RS232 port on the SBC-85 will eat any TTL device connected to J3. If you want to use a TTL signal on J3, then remove U3 and jumper U3.10 to U3.8 and U3.9 to U3.7.

It does not affect the operation, but beginning with v2.x the RS232 circuit has been slightly updated so it could be used with either TI or Maxim MAX232 components. This is because the Texas Instruments MAX232 perfers the capacitor on pin 2 connected to be connected to ground but it will still work if connected to +5V. The Maxim part, on the other hand, must have this capacitor connected to +5V and can be damaged if connected to ground. Beginning with v2.x the negative lead of C12 on the MAX232 was connected to +5 rather than ground to prevent damaging the Maxim part.

A jumper (J1) is provided if the user desires to connect the 8085 RST7.5 to the SID line. When connected, this would allow the 8085 to handle incoming SID signals with an interrupt handler. To connect the SID to RST7.5 a jumper should be installed between J1.1 to J1.2. To connect RST7.5 to the expansion bus a jumper should be installed between J1.2 and J1.3. If J1 is left uninstalled, RST7.5 should be masked since is disconnected. RST7.5 is a rising edge latched interrupt and will probably float high and eventually cause some confusion. If you are worried about it and are not using it on either the SID or the expansion bus, use wire wrap to connect it to ground somewhere.

EXPANSION BUS

To maximize the utility and flexibility of the SBC-85 it is provided with an expansion bus with the mechanical dimensions of a 120-pin PCI connector. This bus does not meet and, besides the physical connector, has nothing in common with the PCI interface. This format was chosen simply because PCI connectors are mass produced and therefore incredibly inexpensive. As seen on the schematic, this expansion bus has 10 pins dedicated to +5V and another 10 pins dedicated to ground. All other 8085 signals are brought out to this bus including the latched addresses A0-A7. Since the inverted ALE signal (ALE*) is often more convenient that ALE, it too is brought out. All of these signals use only half of the connector so the remaining are reserved for future use or for the user to wire as desired. These may be used for board to board signals in an expansion bus or patched to various signals on the SBC-85 to your heart's desire.

The mating card edge connector is a 120 pin PCI connector, e.g., TE Connectivity AMP PN 5145167-8. When facing the component side and the fingers down, pin 1 is on the top right and pin 60 is on the top (component side) left. In this same orientation, pin 61 is on the right back (solder side, i.e., behind pin 1) and pin 120 is on the backside left.
Expansion bus signals are shown by the following table:

Expansion Bus Pinout							
Pin	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**
1	Ground	31	RESET*	61	+5V	91	R91
2	Ground	32	R32	62	+5V	92	R92
3	Ground	33	R33	63	+5V	93	R93
4	Ground	34	READY	64	+5V	94	R94
5	Ground	35	CLK	65	+5V	95	R95
6	A8	36	HLDA	66	AD7	96	R96
7	A9	36	HOLD	67	AD6	97	R97
8	A10	38	ALE*	68	AD5	98	R98
9	A11	39	R39	69	AD4	99	R99
10	A12	40	R40	70	AD3	100	R100
11	A13	41	R41	71	AD2	101	R101
12	A14	42	R42	72	AD1	102	R102
13	A15	43	R43	73	AD0	103	R103
14	A0	44	R44	74	INTA*	104	R104
15	A1	45	R45	75	S0	105	R105
16	A2	46	R46	76	INTR	106	R106
17	A3	47	R47	77	ALE	107	R107
18	A4	48	R48	78	RST 5.5	108	R108
19	A5	49	R49	79	WR*	109	R109
20	A6	50	R50	80	RST 6.5	110	R110
21	A7	51	R51	81	RD*	111	R111
22	R22	52	R52	82	RST 7.5	112	R112
23	R23	53	R53	83	S1	113	R113
24	R24	54	R54	84	TRAP	114	R114
25	R25	55	R55	85	IO/M*	115	R115
26	R26	56	Ground	86	SID	116	+5V
27	R27	57	Ground	87	SOD	117	+5V
28	R28	58	Ground	88	R88	118	+5V
29	R29	59	Ground	89	R89	119	+5V
30	RESET	60	Ground	90	R90	120	+5V
Note: All "R" signals are reserved for user							

POWER INPUT

All components on the SBC-85 are TTL of one family or another and operate on +5VDC. The SBC-85 is fitted with a 2.1mm x 5.5mm barrel connector with the tip positive. A well regulated +5VDC power supply should be used to power the SBC-85 either through the barrel connector or through the expansion bus. Vcc specifications on the 8085 are

+5VDC +/- 10%. Depending on how much current is going out the I/O port and onto the bus, the SBC-85 will take about 1A of current.

The power input is fused at 5 Amps and has a basic reverse polarity protection. Rather than face the continuous voltage drop across an input diode, the SBC-85 uses a reverse biased diode and fuse as a simple crowbar circuit. If a reverse voltage is applied to the input, ideally the diode will create a short circuit and blow the fuse well before the system voltage gets high enough (reversed) to damage any of the components. Therefore, if you are confident in your power supply and expect that you are immune from these mistakes, D2 can be eliminated and F1 can be shorted. However, if D2 is not installed fill the via with solder since it is used to pass the bulk of the current from the fuse outlet (on the top of the board) to the +5V rail on the solder side of the board.

COMPONENTS

FUSE

F1 5-amp Socketed Surface Mount Fuse

JUMPERS AND CONNECTORS
J1 Allows the RST7.5 interrupt to be connected to the SID or to the expansion bus.
J2 +5VDC power inlet barrel connector. Tip positive
J3 RS-232 DB9.
J4 Ground test point
J5 +5V bus test point
J6 8155 port connector

LEDs

D1 Board +5V power indicator

RESISTORS

R7, R8, R9, 10k pull up resistors for READY, WR*, RD*

SWITCHES

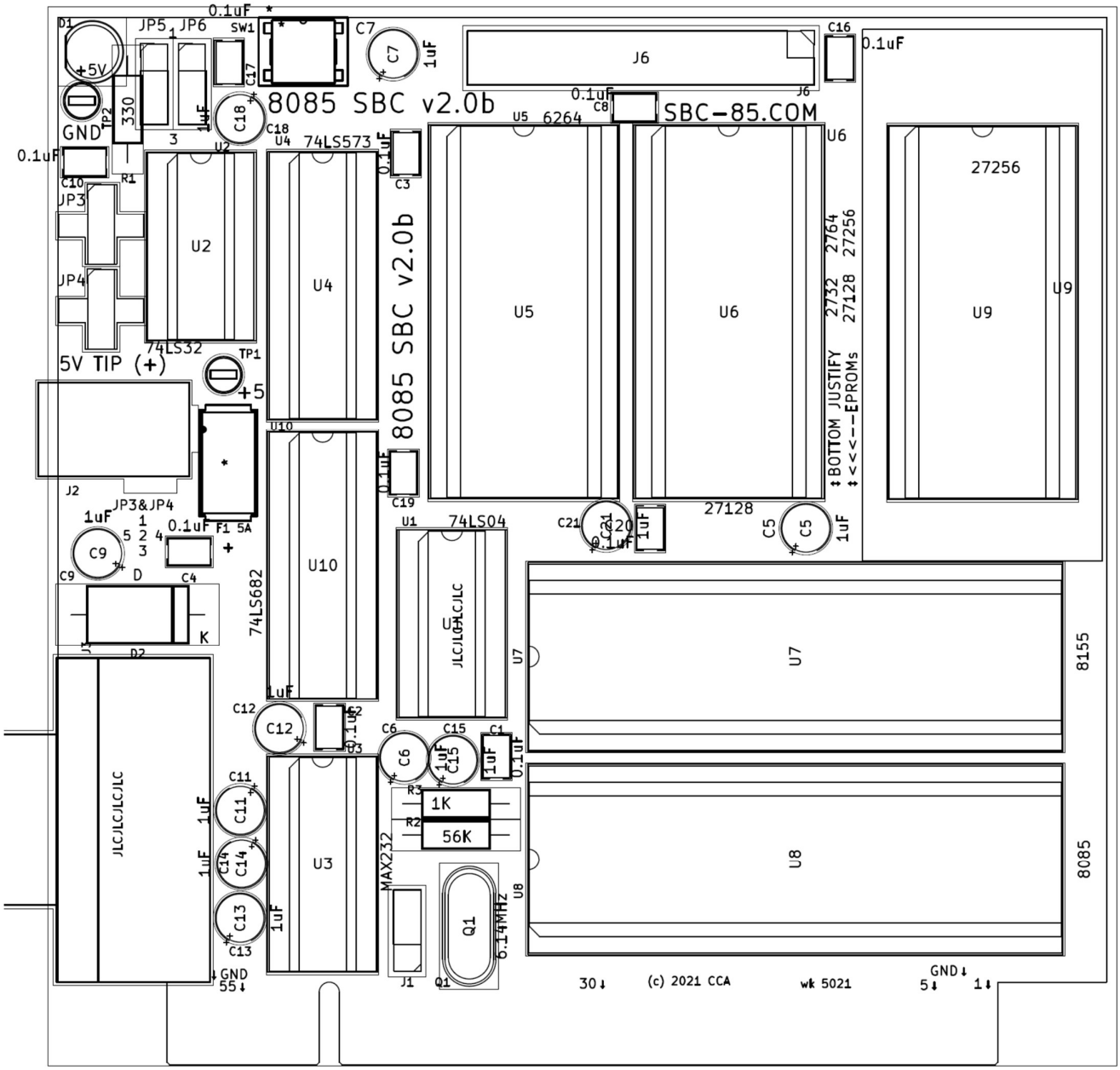
SW1 Resets the CPU by taking the RESET IN* to ground

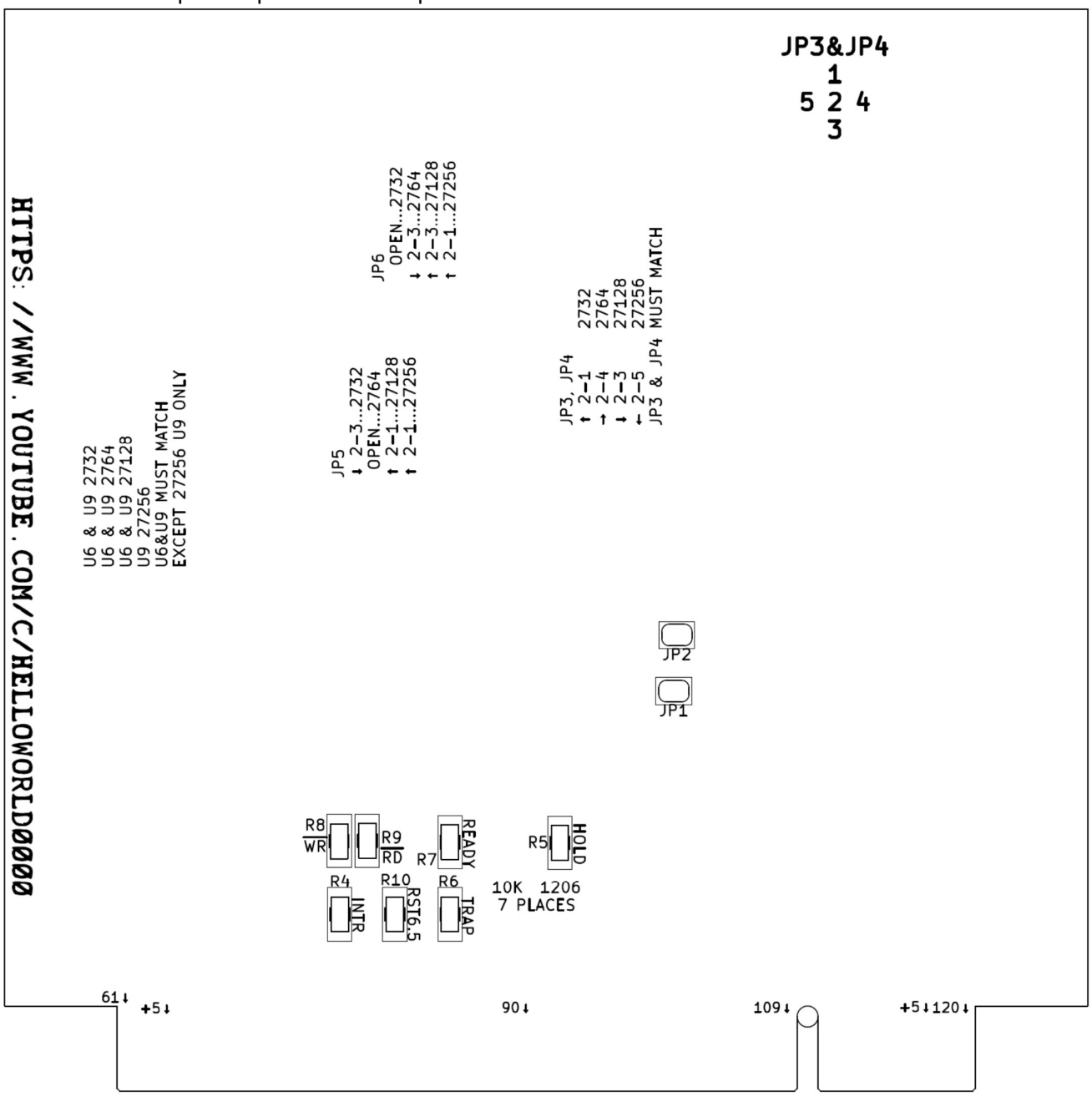
UNUSED

74LS04 hex inverter: U1d, U1e, U1f

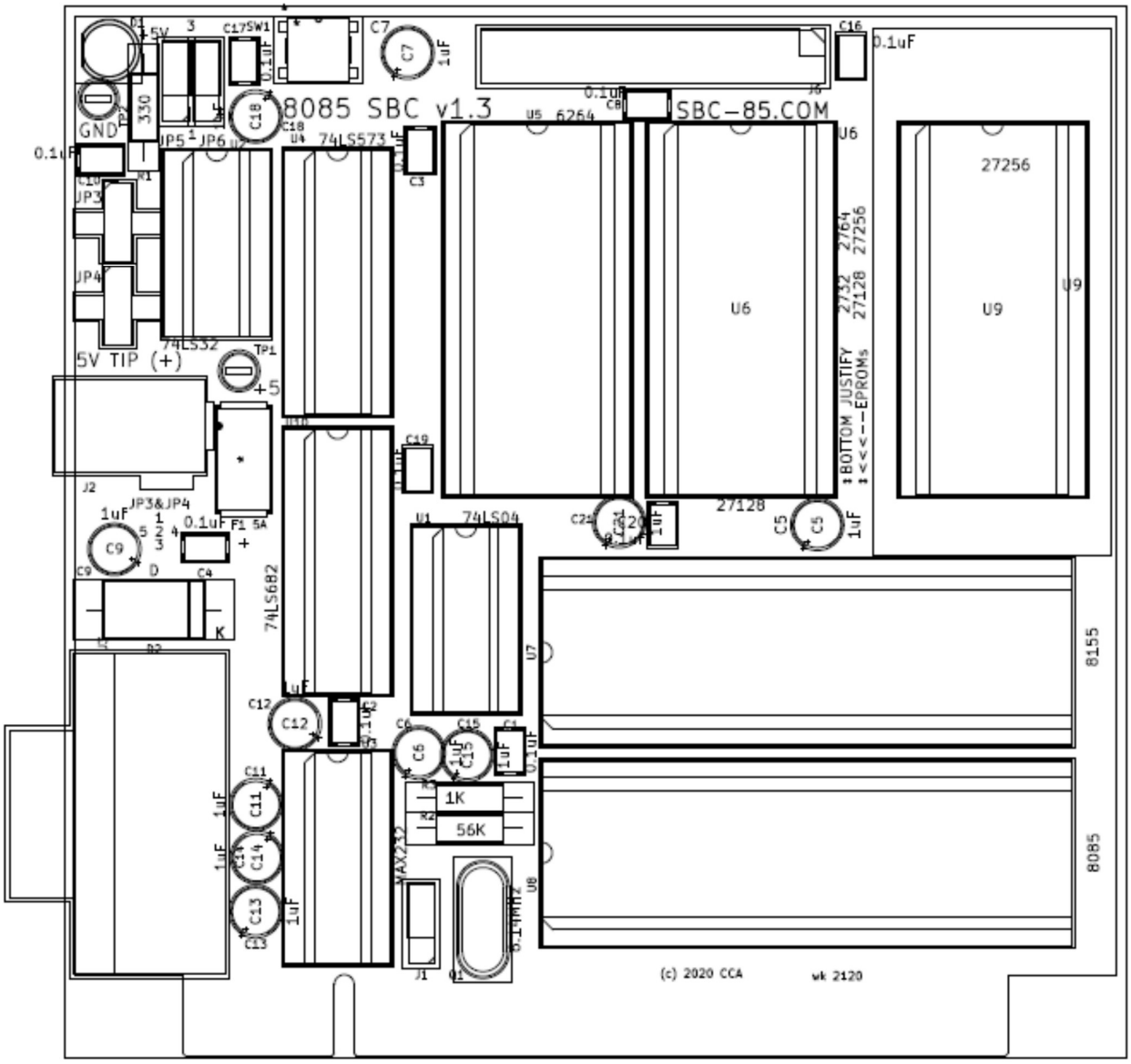
COMPONENT PLACEMENT

Version 2.0b component placement Component Side

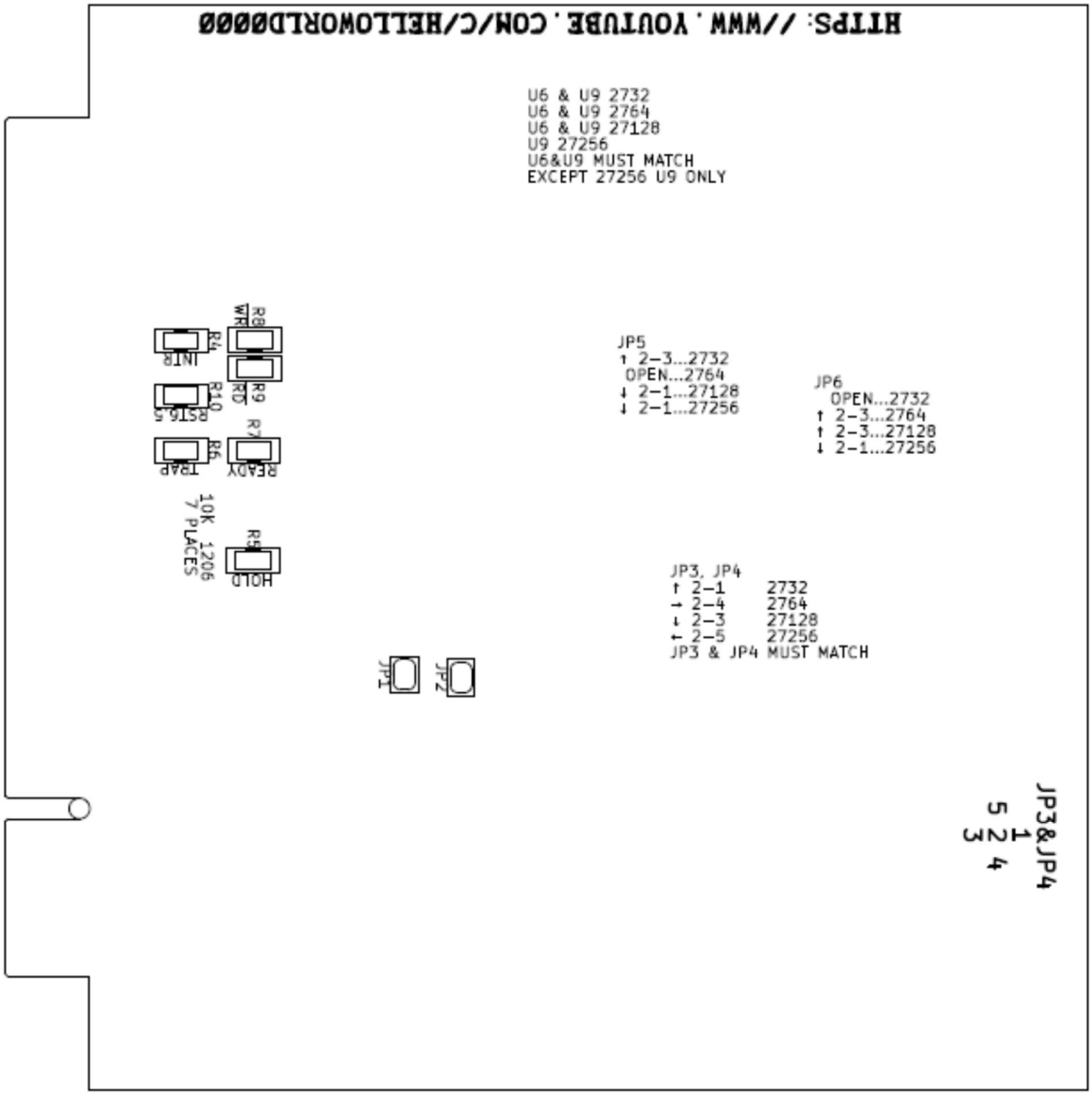



JP3&JP4
1
5 2 4
3
HTTPS://WWW.YOUTUBE.COM/C/HELLOWORLD0000
U6 & U9 2732
U6 & U9 2764
U6 & U9 27128
U9 27256
U6&U9 MUST MATCH
EXCEPT 27256 U9 ONLY
JP5
2-3...2732
OPEN...2764
2-1...27128
2-1...27256
JP6
OPEN...2732
2-3...2764
2-3...27128
2-1...27256
JP3, JP4
2-1 2732
2-4 2764
2-3 27128
2-5 27256
JP3 & JP4 MUST MATCH
JP2
JP1
R8 WR
R9 RD
R7
READY
R5
HOLD
R4
INTR
R10
RST6.5
R6
TRAP
10K 1206
7 PLACES
61
+5
90
109
+5
120

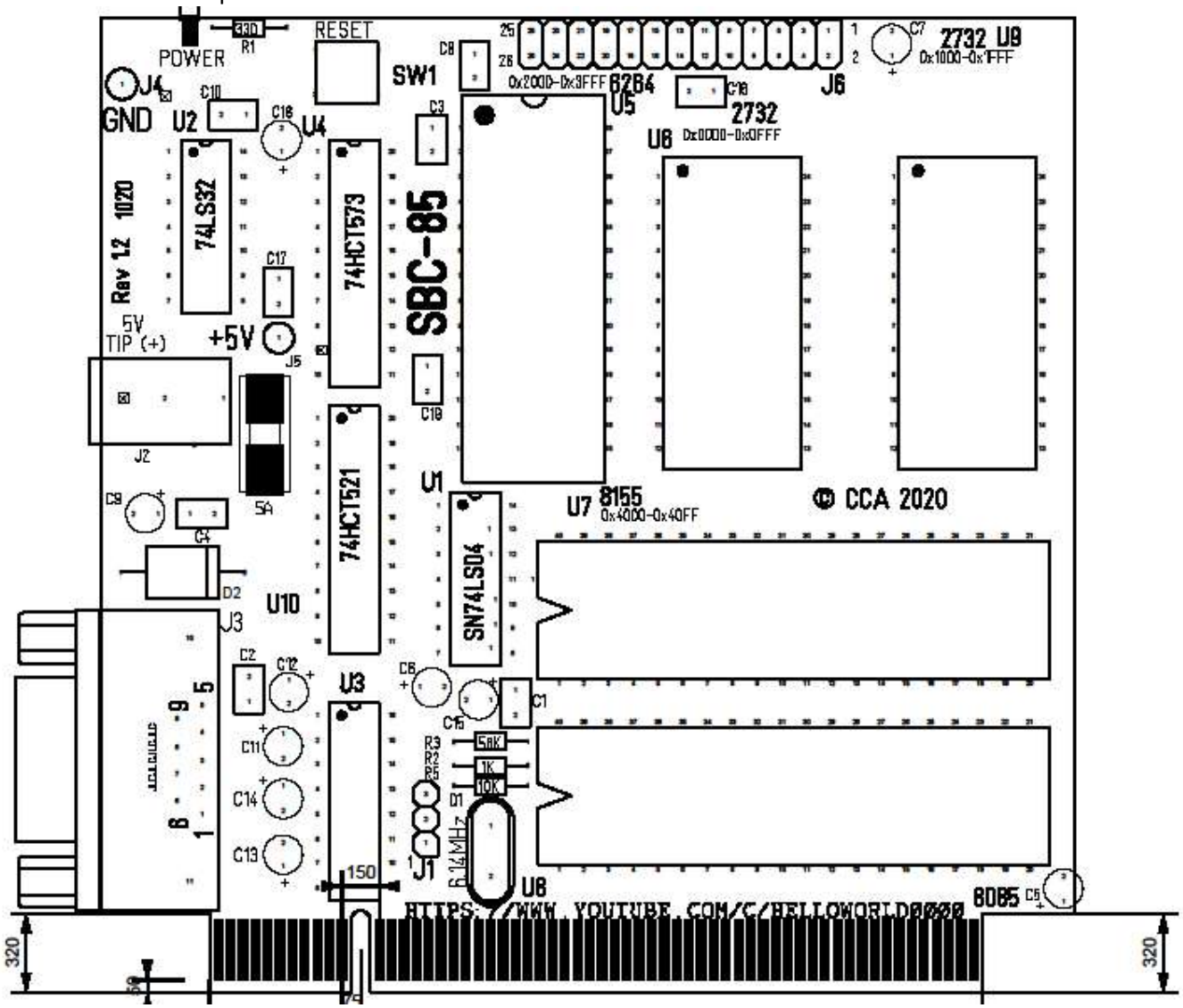
Version 1.3 component placement Component Side



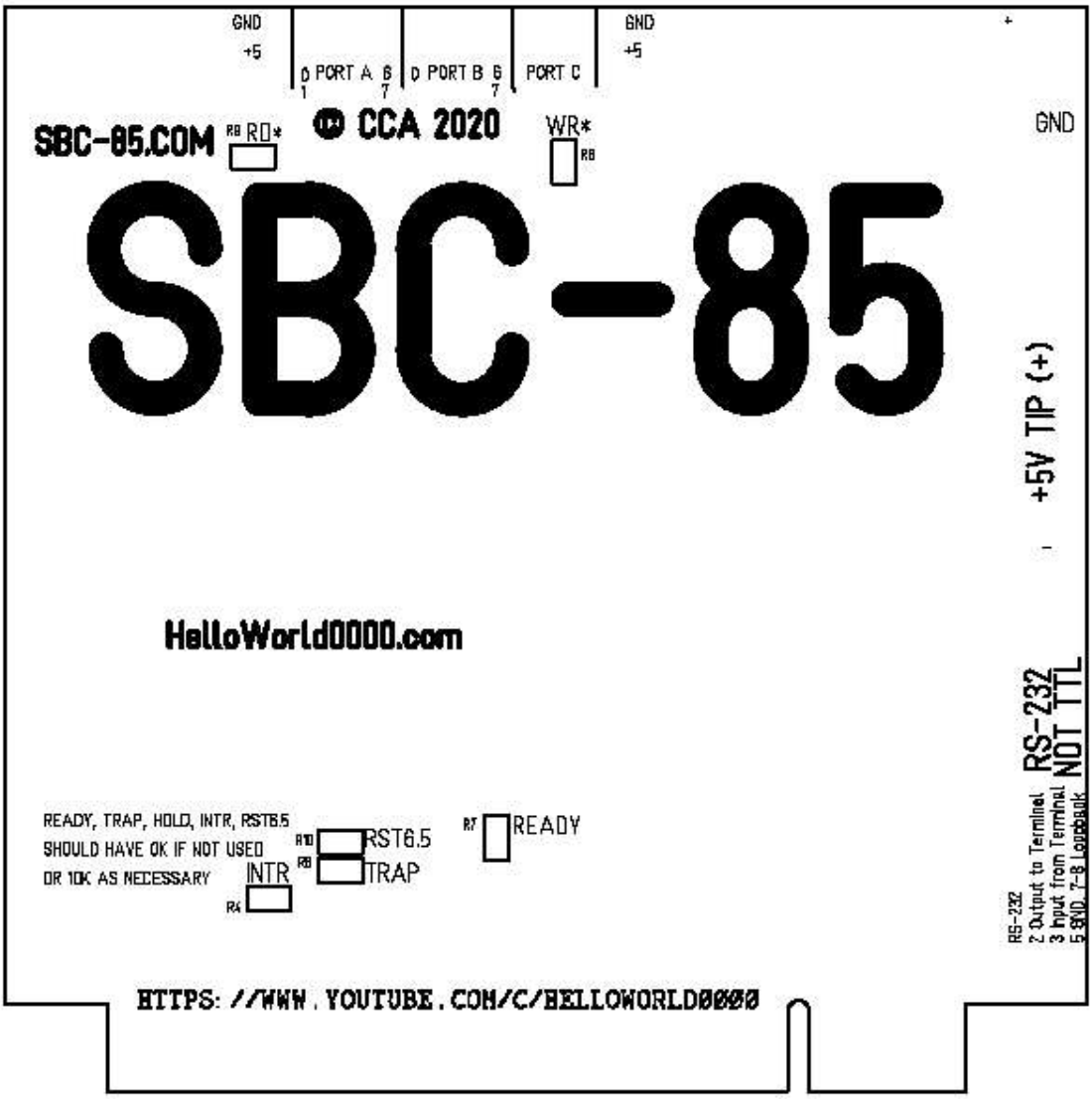
Version 1.3 component placement Solder Side



Version 1.0 -1.2 Component Side

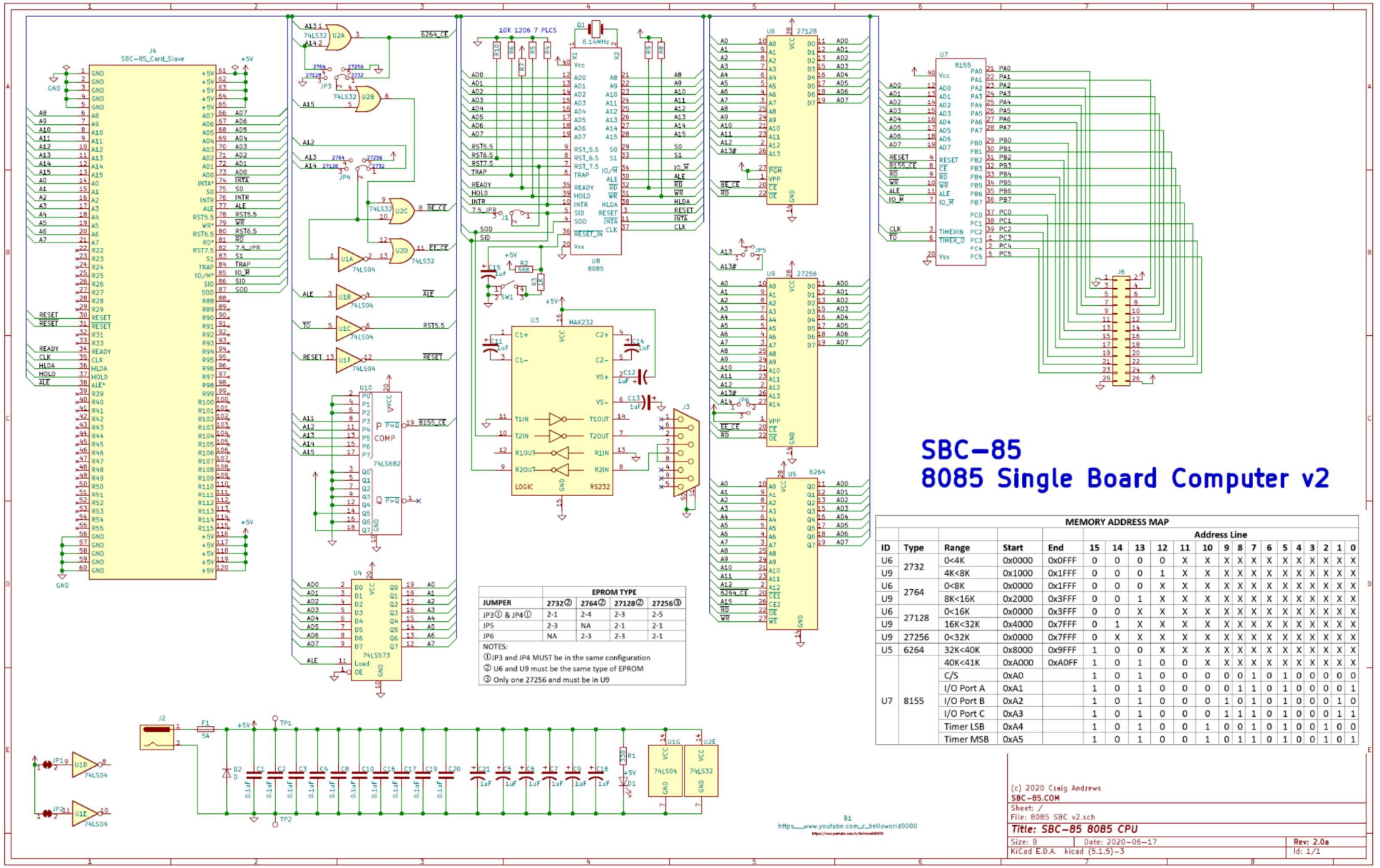


Version 1.0 -1.2 Solder Side



SCHEMATICs

Schematics for versions in reverse chronological order are shown on the following pages. Higher resolution PDF schematics are available on the SBC-85.COM project website. Note that U6 and U9 are 'universal sites' and the actual EPROM used is bottom justified if the chip has fewer pins than the socket. This means for a 2732, for example, 2732 pin 1 is in pin 3 of the socket, 2732 pin 24 is in pin 26 of the socket. Each pin on the IC is two pins higher when looking at the schematic. The graphic in an earlier section titled v2.x *Universal EPROM Sockets* may be a useful reference.



MEMORY ADDRESS MAP

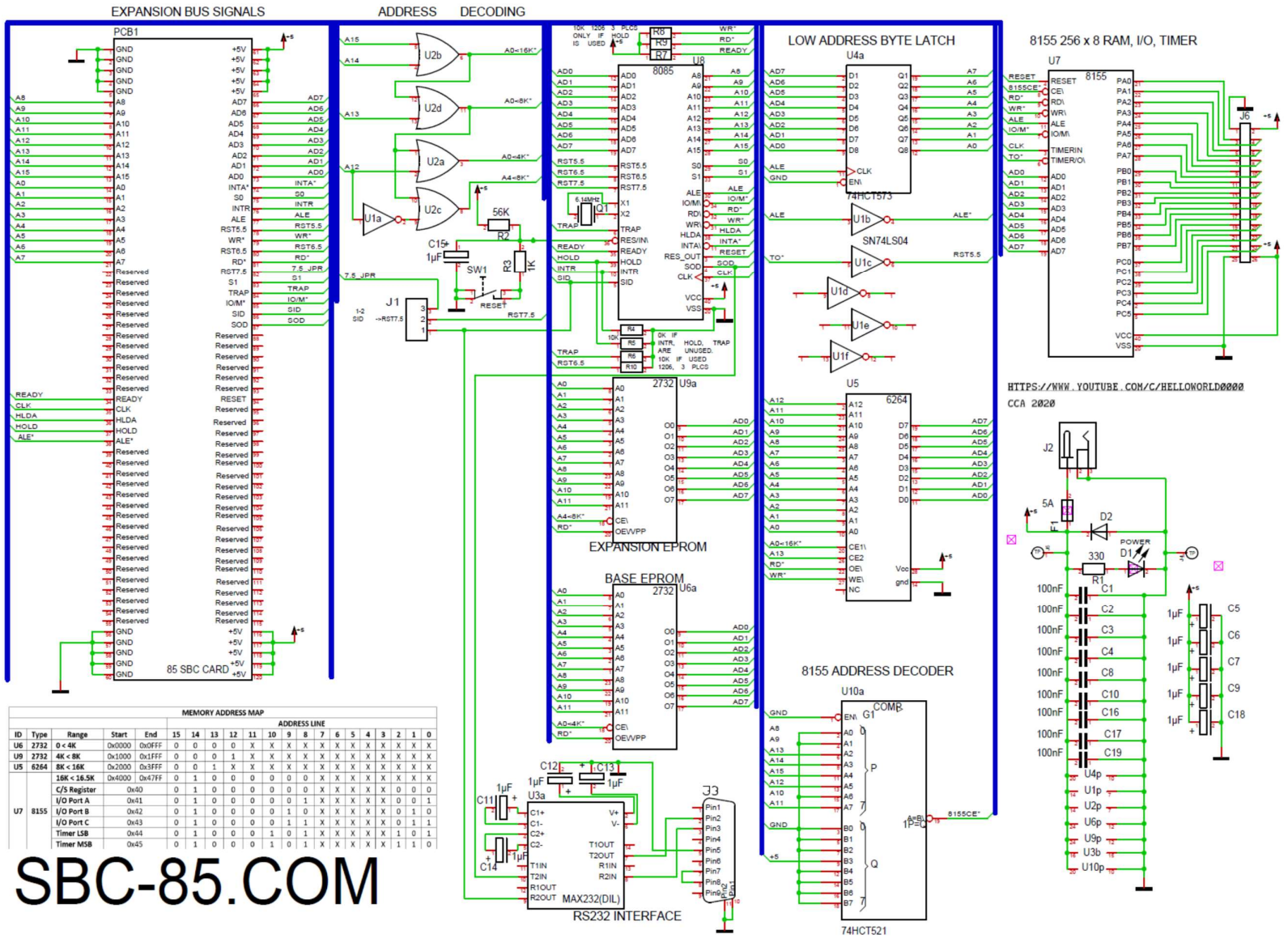
					Address Line											
ID	Type	Range	Start	End	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U6	2732	0<4K	0x0000	0x0FFF	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X
U9		4K<8K	0x1000	0x1FFF	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X
U6	2764	0<8K	0x0000	0x1FFF	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X
U9		8K<16K	0x2000	0x3FFF	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X
U6	27128	0<16K	0x0000	0x3FFF	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X
U9		16K<32K	0x4000	0x7FFF	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X
U9	27256	0<32K	0x0000	0x7FFF	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
U5	6264	32K<40K	0x8000	0x9FFF	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X
		40K<41K	0xA000	0xA0FF	1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	X
U7	8155	C/S	0xA0		1	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0
		I/O Port A	0xA1		1	0	1	0	0	0	0	1	1	0	1	0	0	0	0	1
		I/O Port B	0xA2		1	0	1	0	0	0	1	0	1	0	1	0	0	0	1	0
		I/O Port C	0xA3		1	0	1	0	0	0	1	1	1	0	1	0	0	0	1	1
		Timer LSB	0xA4		1	0	1	0	0	1	0	0	1	0	1	0	0	1	0	0
		Timer MSB	0xA5		1	0	1	0	0	1	0	1	1	0	1	0	0	1	0	1

EPROM TYPE				
JUMPER	2732②	2764②	27128②	27256③
JP3① & JP4①	2-1	2-4	2-3	2-5
JP5	2-3	NA	2-1	2-1
JP6	NA	2-3	2-3	2-1

NOTES:
①JP3 and JP4 MUST be in the same configuration
② U6 and U9 must be the same type of EPROM
③ Only one 27256 and must be in U9

SBC–85.COM
Sheet: /
File: 8085 SBC v2.sch
Title: SBC–85 8085 CPU
Size: B | Date: 2020–05–17 | Rev: 2.0a
KiCad E.D.A. kicad (5.1.5)–3 | Id: 1/1

SBC-85 CPU v1.1-v1.2

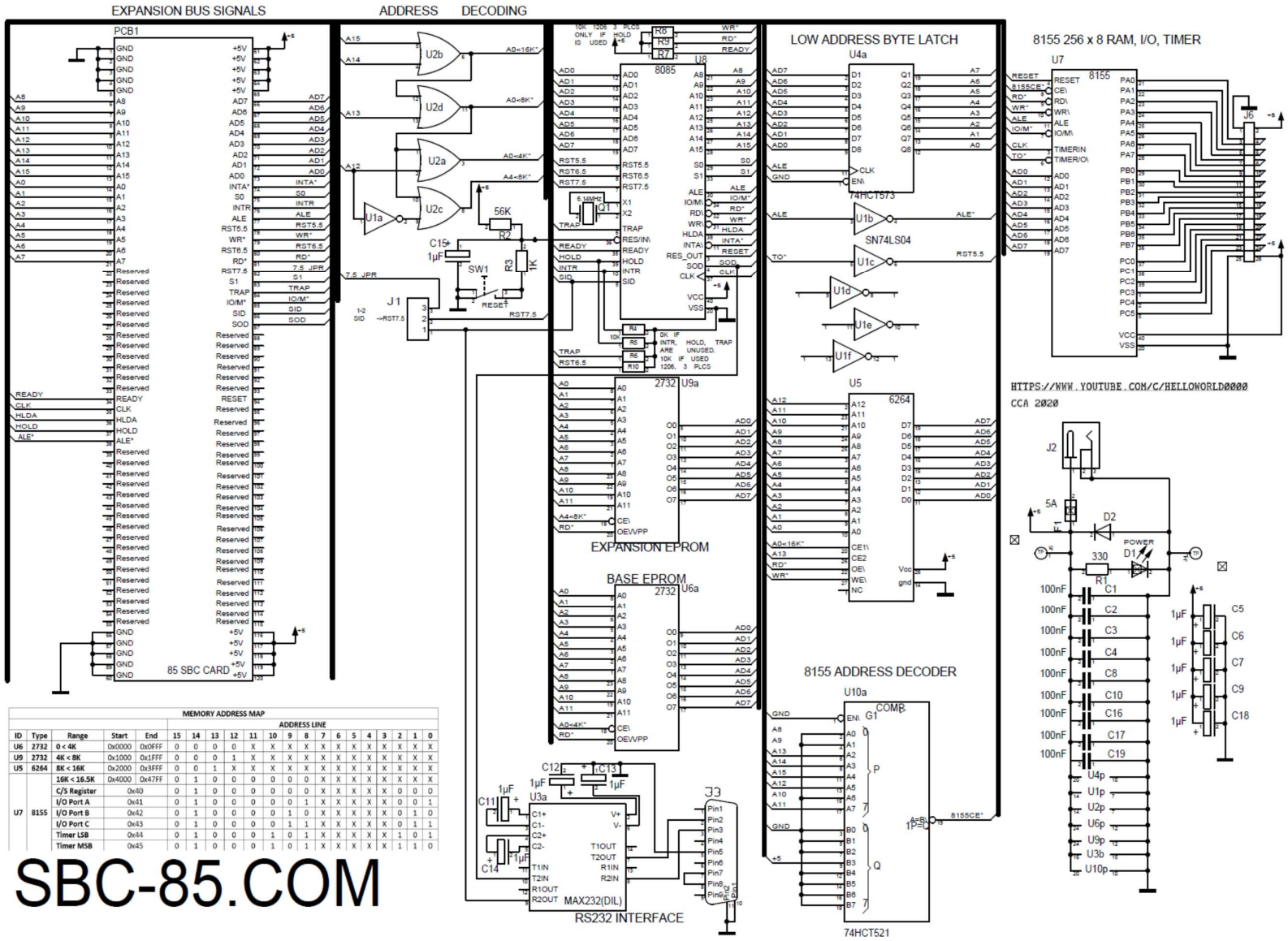


MEMORY ADDRESS MAP

ID	Type	Range	Start	End	ADDRESS LINE 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U6	2732	0 < 4K	0x0000	0x0FFF	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X
U9	2732	4K < 8K	0x1000	0x1FFF	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X
U5	6264	8K < 16K	0x2000	0x3FFF	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X
		16K < 16.5K	0x4000	0x47FF	0	1	0	0	0	0	0	0	X	X	X	X	X	X	X	X
		C/S Register		0x40	0	1	0	0	0	0	0	0	X	X	X	X	X	0	0	0
		I/O Port A		0x41	0	1	0	0	0	0	0	1	X	X	X	X	X	0	0	1
U7	8155	I/O Port B		0x42	0	1	0	0	0	0	1	0	X	X	X	X	X	0	1	0
		I/O Port C		0x43	0	1	0	0	0	0	1	1	X	X	X	X	X	0	1	1
		Timer LSB		0x44	0	1	0	0	0	1	0	0	X	X	X	X	X	1	0	0
		Timer MSB		0x45	0	1	0	0	0	1	0	1	X	X	X	X	X	1	1	0

SBC-85.COM

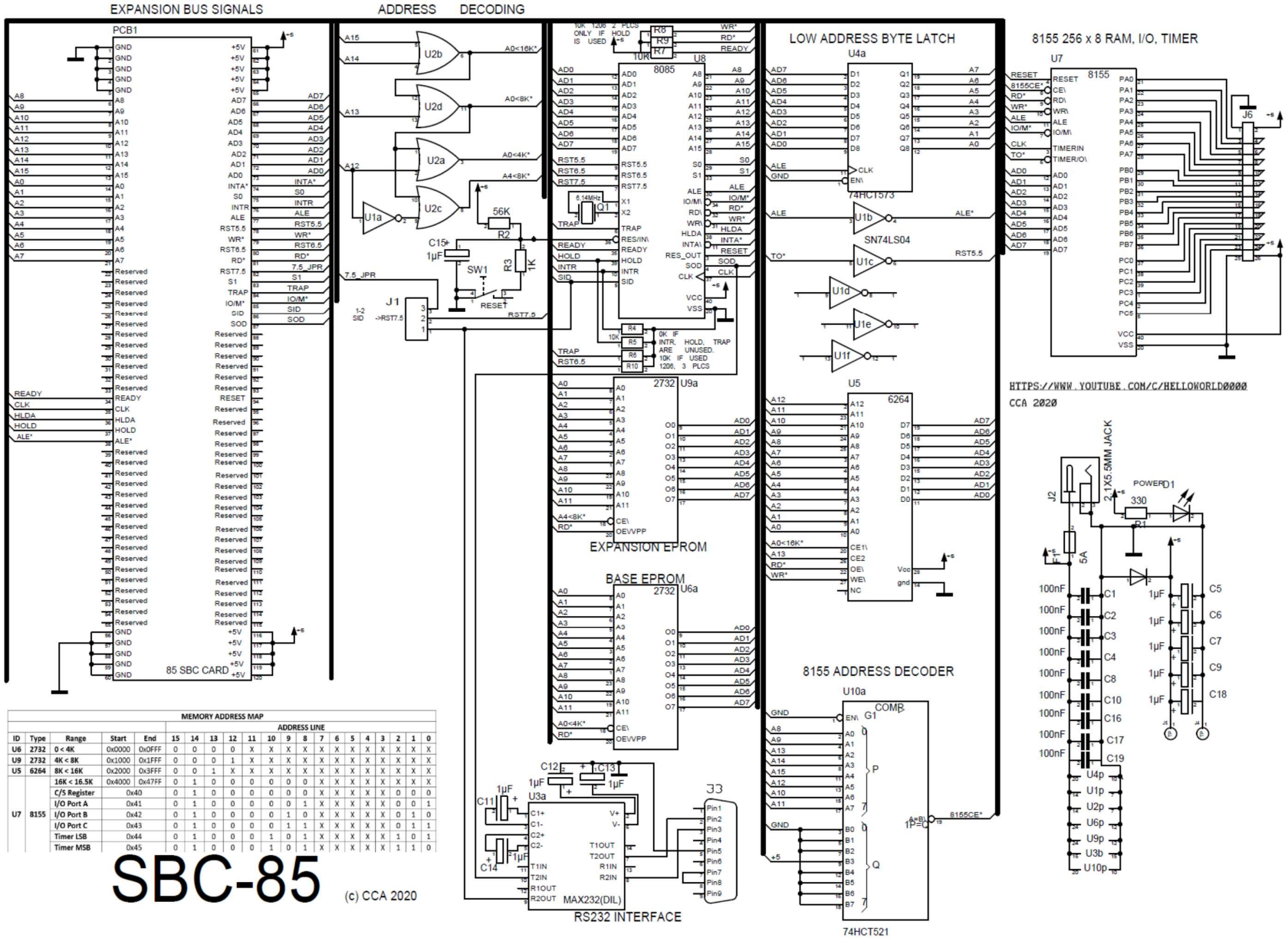
SBC-85 CPU v1.1-v1.2



MEMORY ADDRESS MAP

					ADDRESS LINE														
ID	Type	Range	Start	End	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U6	2732	0 < 4K	0x0000	0x0FFF	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X
U9	2732	4K < 8K	0x1000	0x1FFF	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X
U5	6264	8K < 16K	0x2000	0x3FFF	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X
		16K < 16.5K	0x4000	0x47FF	0	1	0	0	0	0	0	0	X	X	X	X	X	X	X	X
		C/S Register	0x40		0	1	0	0	0	0	0	0	X	X	X	X	X	0	0	0
		I/O Port A	0x41		0	1	0	0	0	0	0	1	X	X	X	X	X	0	0	1
U7	8155	I/O Port B	0x42		0	1	0	0	0	0	1	0	X	X	X	X	X	0	1	0
		I/O Port C	0x43		0	1	0	0	0	0	1	1	X	X	X	X	X	0	1	1
		Timer LSB	0x44		0	1	0	0	0	1	0	1	X	X	X	X	X	1	0	1
		Timer MSB	0x45		0	1	0	0	0	1	0	1	X	X	X	X	X	1	1	0

SBC-85.COM



MEMORY ADDRESS MAP

ID	Type	Range	Start	End	ADDRESS LINE 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U6	2732	0 < 4K	0x0000	0x0FFF	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X
U9	2732	4K < 8K	0x1000	0x1FFF	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X
U5	6264	8K < 16K	0x2000	0x3FFF	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X
U7	8155	16K < 16.5K	0x4000	0x47FF	0	1	0	0	0	0	0	0	X	X	X	X	X	X	X	X
		C/S Register	0x40		0	1	0	0	0	0	0	0	X	X	X	X	X	0	0	0
		I/O Port A	0x41		0	1	0	0	0	0	0	1	X	X	X	X	X	0	0	1
		I/O Port B	0x42		0	1	0	0	0	0	1	0	X	X	X	X	X	0	1	0
		I/O Port C	0x43		0	1	0	0	0	0	1	1	X	X	X	X	X	0	1	1
		Timer LSB	0x44		0	1	0	0	0	1	0	1	X	X	X	X	X	1	0	1
		Timer MSB	0x45		0	1	0	0	0	1	0	1	X	X	X	X	X	1	1	0

v1.0

REVISIONS

v1.0 First produced board week 0120
- 1.01 Hole added to power inlet barrel connector for nib
- 1.01 Power inlet connector moved further from serial connector
- 1.01 serial connector changed from male to female
- 1.01 U10 i8155 decoder pins 2, 4, 15 taken to ground to ignore A8, A9, A10
- 1.02 Reset switch changed to smaller and low-profile footprint
- 1.03 J6 moved further away from ZIF handle
- 1.04 Power LED moved to top of board

v1.1 Second manufactured board week 0520
- 1.1.1 Power inlet barrel connector did not render properly as obrounds. Change back to circles
- 1.1.2 Removed fill on back side between fingers and edge of board

V1.2 Changed power inlet from too small round to obround.

V2.0 First manufactured the week 2120. Changes implemented:
- Change EPROM sockets to 28-pin 'universal site' with jumpers to utilize EPROMs from 2732 to 27256
- Change address decoding to match EPROM universal size
- Move RAM address to begin at 0x8000
- Texas Instruments MAX232 like the capacitor on pin 2 connected to ground but will still work if connected to +5V. The Maxim part must have this capacitor connected to +5V and can be damaged if connected to ground. Change C12 on MAX232 negative lead to +5 rather than ground to prevent damaging the Maxim part.
- Take the unused input T1 of the MAX232 U3 to ground.
- Connect the Reset to P30 of the backplane and Reset* to pin 31
- Tie all unused inputs using solder bridges on solder side

V2.0a First manufactured the week 2320. Changes implemented:
- Vertical flip of JP5 and JP6 for consistency with JP3 and JP4. Pin 1 is now up (near edge).
- Add finger numbers and finger +5V / GND to silkscreen
- Connect SID to backplane.

V2.0b First manufactured the week 50-21. Changes implemented:
- Corrected floating ground problem on DB9. Pin 5 connected to ground.

Possible future revision requests

- Place selection jumper on 8155 Timer Input and bring to backplane
- Make 8155 TIMEROUT to RST_7.5 patch or jumper possible

ASSEMBLY NOTES AND PROCEDURES – Most of these are important

- On version 2 boards prior to v2.0b the common on the DB9 COM port was left floating. This needs to be taken to ground with a patch wire.
- If you receive a board that does not have gold fingers, the sharp finger corner will damage the contacts on the backplane. This can be accomplished using a utility knife followed by filing or sanding (sand paper on a flat surface) to create a 45° chamfer on both edges. **If you insert the sharp edge into the PCI connectors on the backplane, it WILL damage the connector**. Video
- For most footprints on the PCB, pin 1 is identified as the square pad.
- When buying components, this is my general advice—in almost all cases I design for the 74LS family. If you can find components in the 74LS, great. If not, try the 74ALS family, 74F, or 74HCT which are all TTL compatible with the 74LS. (Note that the 74HC is NOT TTL).
- Tantalum capacitors in KiCAD have pin 1 of the footprint as the positive terminal, however footprints for LEDs are the opposite and have pin 2 as positive. For both LEDs and the polarized capacitors, if one lead is longer than the other that is the positive lead (anode on LEDs).
- For the power LED, the cathode is on the solder side (back) of the board. It may not be clearly marked on earlier versions. Remember that the longer lead on LEDs is the Anode – "in the anode, out the cathode".
- Do not forget the surface mount resistors on the back of the board. It will not run if these are not installed since the CPU will immediately enter a WAIT state.

- For versions before v2.x, the MAX232 must be from Texas Instruments. Starting with version 2.0 it can be from either TI or Maxim. Sorry.

MODIFICATIONS to UPDATE REVISIONS

V2.0 TO v2.0a

To make version 2.0 equivalent to versions 2.0a the following revisions or adaptations are necessary

- Patch SID to backplane. Easiest from U8.5 to pin 86.
- JP5 and JP6 are vertically reflected on v2.0a for consistency with JP3 and JP4

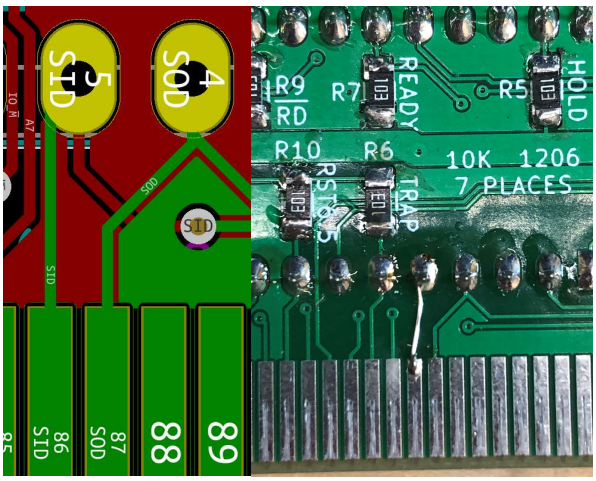
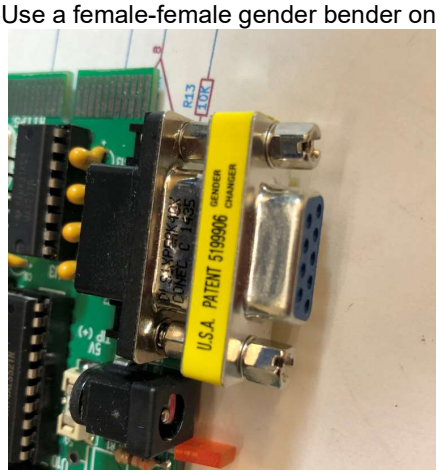


Figure 1 v2.0 to 2.0a patch to connect SID to backplane. Pin U8.5 to finger 86

v1.0 TO v1.1-v1.2

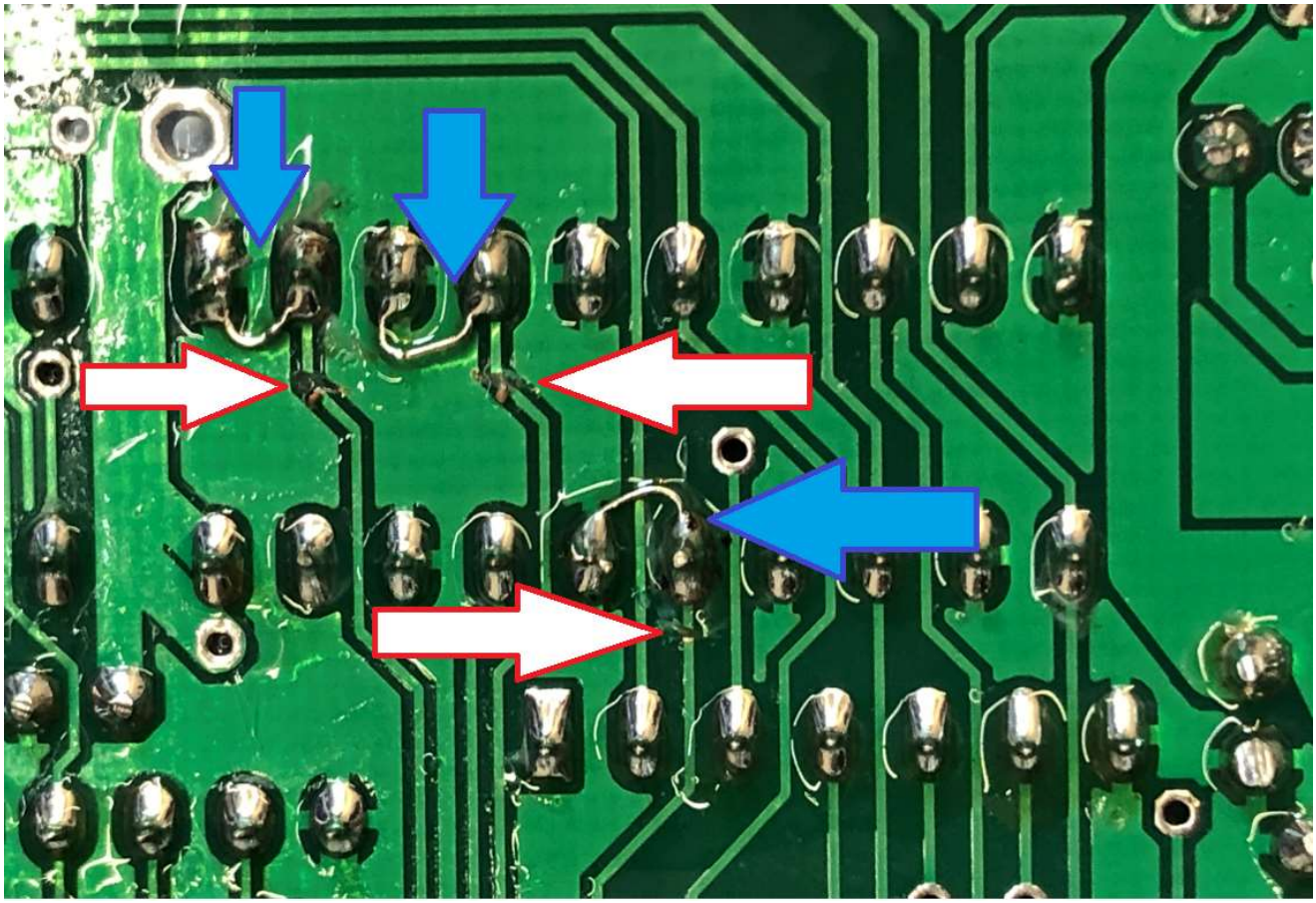
To make version 1.0 equivalent to versions 1.1 and 1.2 the following revisions or adaptations are necessary.

Use a female-female gender bender on the serial port



Addresses A8, A9, and A10 need to be taken to 0V on the equality detector U10. On the back of the board, three traces need to be cut and the loose pins tied to ground on U10.
Cut the traces shown by the red arrows on pins 2, 4, 15 to match the photograph. The photograph orientation is such that the serial port is towards the top. Note the large, unused via that is for the big voltage input reverse protection diode is right by pin 1. There is no need to dig a hole halfway through the board, but it is good to test them to make sure the trace is broken. I use a utility knife blade to cut the trace but I could have flicked the left over piece of copper trace off the end better.

After cutting and testing the traces, these loose pins need to be tied to ground by placing a jumper to the adjacent pins which happens to be tied to 0V, so jumper 1-2, 3-4, 15-16 as shown by the blue arrows.



v1.1 TO v1.2

There are no significant differences between v1.1 and v1.2. The holes on the power inlet barrel connector were corrected to be obrounds rather than the undersized hole. To assemble the power inlet barrel connector on v1.1 the input tabs on the barrel connector need to be cut off and butt soldered to the pads. With v1.2 this is not necessary.

DIAGNOSTIC NOTES

Hot or Dead MAX232-

- Check the charge pump capacitors are correctly installed (polarized)
- Board versions prior to v2.0 required a Texas Instruments MAX232 part

BOMs

SBC-85 8085 CPU v2.0 BOM

QTY	Name	Value	Package/description	Manufacturer	Manufacturer PN	DIGI KEY PN
10	C1, C2, C3, C4, C8, C10, C16, C17, C19, C20	100nF	CAP CER 0.1UF 50V Z5U RADIALKEMET	kemet	C315C104M5U5TA	399-4151-ND
11	C5, C6, C7, C9, C11, C12, C13, C14, C15, C18, C21	1µF	1µF Conformal Coated Tantalum Capacitors 35V Radial 8Ohm	avx	TAP105M035SCS	478-5812-ND
1	D1	LED AMBER DIFF RECT 2MMX5MM T/H			SSL-LX2573AD	67-1045-ND
1	D2	GENERAL PURPOSE CROWBAR DIODE		ON Semiconductor	1N5817G	1N5817GOS-ND
1	F1	5A	FUSE BRD MNT 5A 125VAC/VDC 2SMD	Littelfuse	0154005.DRT	F1310CT-ND
1	J1	CONN HEADER VERT 3POS 2.54MM	PREC003SAAN-RC	Sullins connector Solution		S1012EC-03-ND
1	J2	Power Barrel Connector Jack 2.10mm ID (0.083"), 5.50mm OD (0.217") Through Hole, Right Angle		CUI	PJ-050AH	CP-050AH-ND
1	J3	CONN D-SUB RCPT 9POS R/A SOLDER	9 Position D-Sub Receptacle, Female Sockets Connector	Amphenol ICC	D09S13A4GX00LF	609-1484-ND
1	J4	PC TEST POINT .065 HOLE COMPACT BLACK		keystone electronics	5006	36-5006-ND
1	J5	PC TEST POINT .065 COMPACT RED		keystone electronics	5005	36-5005-ND
1	J6	CONN HEADER R/A 26POS 2.54MM		Sullins connector Solution	PREC013DBAN-M71RC	S2112EC-13-ND
4	Alternate for all jumpers	Header, snap	Connector Header Through Hole 40 position 0.100"	Sullins Connector	PREC040SAAN-RC	S1012EC-40-ND
The following are easier but more expensive alternates for cutting 'snap header' into individual units						
4 alt	JP5, JP6 (2 each)	1x1 header	Vertical Pin Header Through Hole 1x1 0.100"	Adam Tech	PH1-01-UA	2057-PH1-01-UA-ND
4 alt	JP3, JP4, JP5, JP6	1x3 header	Vertical Pin Header Through Hole 1x3 0.100"	Würth Elektronik	61300311121	732-5316-ND
NOTE: when creating the 1-of-4 jumpers from components, to maintain alignment insert a shorting jumper before soldering						
1	PCB1	8085 SBC-85 CPU v2.0 PCB		SBC-85.COM		
1	Q1	6.14MHz	HC49/US	CTS frequency controls	ATS061B	CTX899-ND
1	R1	330	RES 330 OHM 1/4W 5% AXIAL	stackpole	CF14JT330R	CF14JT330RCT-ND
1	R2	56K	RES 56K OHM 1/4W 5% AXIAL	stackpole	CF14JT56K0	CF14JT56K0CT-ND
1	R3	1K	RES 1K OHM 1/4W 5% AXIAL	stackpole	CF14JT1K00	CF14JT1K00CT-ND

SBC-85 8085 CPU v2.0 BOM

QTY	Name	Value	Package/description	Manufacturer	Manufacturer PN	DIGI KEY PN
7	R4, R5, R6, R7, R8, R9, R10	10KOHM 1206	RES 10K SMD 1206	yageo	RC1206JR-0710KL	311-10KERCT-ND
1	SW1	Tactile Switch SPST-NO Top Actuated Through Hole	SWITCH PUSH SPST-NO 0.1A 32V	TE Connectivity ALCOSWITCH	1825910-7	450-1804-ND
1	U1	SN74LS04	DIL14	Texas Instruments	SN74LS04N	296-1629-5-ND
1	U10	74LS682	DIL20	Texas Instruments	SN74LS682N	296-14898-5-ND
1	U2	74LS32	DIL14	Texas Instruments	SN74LS32N	296-1658-5-ND
1	U3	MAX232(DIL)	IC TRANSCEIVER FULL 2/2 16DIP	Texas Instruments	MAX232N	296-1402-5-ND
1	U4	74HCT573	DIL20	Texas Instruments	SN74HCT573N	296-1621-5-ND
1	U5	6264	DIL28_WB15,24_P2,54	Alliance Memory	AS6C6264-55PCN	1450-1036-ND
2	U6, U9	2732, 2764, 27128, 27512				
1	U7	8155	DIL40			
1	U8	8085	DIL40			
2	U1, U2	14-pin DIP Socket				
1	U3	16-pin DIP Socket				
2	U5, U6	28-pin DIP Socket				
1	U9	28-pin ZIF DIP socket				
2	U7, U8	40-pin DIP Socket				
1		AC/DC DESKTOP ADAPTER 5V 20W	Power Supply 2.1mm x 5.5mm 5V 20W TIP Positive	phihong USA	PSAC30U-050L6	993-1343-ND

SBC-85 8085 CPU v1.1 - v1.2 BOM

QTY	Name	Value	Package/description	Manufacturer	Manufacturer PN	DIGI KEY PN
9	C1, C2, C3, C4, C8, C10, C16, C17, C19	100nF	CAP CER 0.1UF 50V Z5U RADIALKEMET	kemet	C315C104M5U5TA	399-4151-ND
10	C5, C6, C7, C9, C11, C12, C13, C14, C15, C18	1µF	1µF Conformal Coated Tantalum Capacitors 35V Radial 8Ohm	avx	TAP105M035SCS	478-5812-ND
1	D1	LED AMBER DIFF RECT 2MMX5MM T/H			SSL-LX2573AD	67-1045-ND
1	D2	4A GENERAL PURPOSE DIODE		ON semiconductor	MUR460RLG	MUR460RLGOSCT-ND
1	F1	5A	FUSE BRD MNT 5A 125VAC/VDC 2SMD	Littelfuse	0154005.DRT	F1310CT-ND
3	J1, JP5, JP6	CONN HEADER VERT 3POS 2.54MM	PREC003SAAN-RC	Sullins connector Solution		S1012EC-03-ND

SBC-85 8085 CPU v1.1 - v1.2 BOM

QTY	Name	Value	Package/description	Manufacturer	Manufacturer PN	DIGI KEY PN
1	J2	Power Barrel Connector Jack 2.10mm ID (0.083"), 5.50mm OD (0.217") Through Hole, Right Angle		CUI	PJ-050AH	CP-050AH-ND
1	J3	CONN D-SUB RCPT 9POS R/A SOLDER	9 Position D-Sub Receptacle, Female Sockets Connector	Amphenol ICC	D09S13A4GX00LF	609-1484-ND
1	J4	PC TEST POINT .065 HOLE COMPACT BLACK		keystone electronics	5006	36-5006-ND
1	J5	PC TEST POINT .065 COMPACT RED		keystone electronics	5005	36-5005-ND
1	J6	CONN HEADER R/A 26POS 2.54MM		Sullins connector Solution	PREC013DBAN-M71RC	S2112EC-13-ND
2	JP3, JP4	Connector Header Through Hole 9 position. Remove 4 corner pins		Samtec Inc.	TSW-103-07-T-T	TSW-103-07-T-T-ND
1	PCB1	8085 SBC-85 CPU v1.1 or v1.2 CARD		SBC-85		
1	Q1	6.14MHz	HC49/US	CTS frequency controls	ATS061B	CTX899-ND
1	R1	330	RES 330 OHM 1/4W 5% AXIAL	stackpole	CF14JT330R	CF14JT330RCT-ND
1	R2	56K	RES 56K OHM 1/4W 5% AXIAL	stackpole	CF14JT56K0	CF14JT56K0CT-ND
1	R3	1K	RES 1K OHM 1/4W 5% AXIAL	stackpole	CF14JT1K00	CF14JT1K00CT-ND
5	R4, R6, R7, R8, R9, R10	10KOHM 1206	Resistor 10K SMD 1206 package	yageo	RC1206JR-0710KL	311-10KERCT-ND
1	R5	10KOHM	RES 10K OHM 1/4W 5% AXIAL	stackpole		
1	SW1	Tactile Switch SPST-NO Top Actuated Through Hole	SWITCH PUSH SPST-NO 0.1A 32V	TE Connectivity ALCOSWITCH	1825910-7	450-1804-ND
1	U1	SN74LS04	DIL14	Texas Instruments	SN74LS04N	296-1629-5-ND
1	U10	74HCT521	DIL20	Texas Instruments	SN74F521N	296-33912-5-ND
1	U2	74LS32	DIL14	Texas Instruments	SN74LS32N	296-1658-5-ND
1	U3	MAX232(DIL)	IC TRANSCEIVER FULL 2/2 16DIP	Texas Instruments	MAX232N	296-1402-5-ND
1	U4	74HCT573	DIL20	Texas Instruments	SN74HCT573N	296-1621-5-ND
1	U5	6264	DIL28_WB15,24_P2,54	Alliance Memory	AS6C6264-55PCN	1450-1036-ND
2	U6, U9	2732	DIL24_SOT101-1			
1	U7	8155	DIL40			
1	U8	8085	DIL40			
2	U1, U2	14-pin DIP Socket				
1	U3	16-pin DIP Socket				
1	U5	28-pin DIP Socket				
1	U6	24-pin DIP Socket				
1	U9	24-pin ZIF DIP socket				
2	U7, U8	40-pin DIP Socket				
5		CONN JUMPER SHORTING .100"			QPC02SXGN-RC	S9337-ND

SBC-85 8085 CPU v1.1 - v1.2 BOM

QTY	Name	Value	Package/description	Manufacturer	Manufacturer PN	DIGI KEY PN
1		AC/DC DESKTOP ADAPTER 5V 20W	Power Supply 2.1mm x 5.5mm 5V 20W TIP Positive	phihong USA	PSAC30U-050L6	993-1343-ND

SBC-85 8085 CPU v1.0 BOM

QTY	Name	Value	Package/description	Manufacturer	Manufacturer PN	DIGI KEY PN
9	C1, C2, C3, C4, C8, C10, C16, C17, C19	100nF	CAP CER 0.1UF 50V Z5U RADIALKEMET	kemet	C315C104M5U5TA	399-4151-ND
10	C5, C6, C7, C9, C11, C12, C13, C14, C15, C18	1µF	Conformal Coated Tantalum Capacitors 35V Radial	avx	TAP105M035SCS	478-5812-ND
1	D1	LED AMBER DIFF RECT 2MMX5MM T/H			SSL-LX2573AD	67-1045-ND
1	D2	4A GENERAL PURPOSE DIODE		ON semiconductor	MUR460RLG	MUR460RLGOSCT-ND
1	F1	5A	FUSE BRD MNT 5A 125VAC/VDC 2SMD	Littelfuse	0154005.DRT	F1310CT-ND
1	J1	CONN HEADER VERT 3POS 2.54MM	PREC003SAAN-RC	Sullins connector Solution		S1012EC-03-ND
1	J2	Power Barrel Connector Jack 2.10mm ID (0.083"), 5.50mm OD (0.217") Through Hole, Right Angle	DC power input jack	CUI		CP-050AH-ND
1	J3	CONN D-SUB RCPT 9POS R/A SOLDER	9 Position D-Sub Receptacle, Female Sockets Connector	Amphenol ICC	D09S13A4GX00LF	609-1484-ND
1	J4	TEST POINT COMPACT BLACK	TEST POINT .065 HOLE	keystone electronics	5006	36-5006-ND
1	J5	TEST POINT COMPACT RED	TEST POINT .065 HOLE	keystone electronics	5005	36-5005-ND
1	J6	CONN HEADER R/A 26POS 2.54MM		Sullins connector Solution	PREC013DBAN-M71RC	S2112EC-13-ND
1	PCB1	85 SBC CARD	85 SBC CARD			
1	Q1	6.14MHz	HC49/US	CTS frequency controls	ATS061B	CTX899-ND
1	R1	330	RES 330 OHM 1/4W 5% AXIAL	stackpole	CF14JT330R	CF14JT330RCT-ND
1	R2	56K	RES 56K OHM 1/4W 5% AXIAL	stackpole	CF14JT56K0	CF14JT56K0CT-ND
1	R3	1K	RES 1K OHM 1/4W 5% AXIAL	stackpole	CF14JT1K00	CF14JT1K00CT-ND
5	R4, R6, R8, R9, R10	R_10KOHM_1206	1206	yageo	RC1206JR-0710KL	311-10KERCT-ND
5	R4, R6, R8, R9, R10	R_0OHM_1206	1206	yageo	RC1206JR-070RL	311-0.0ERCT-ND
2	R5, R7	10K	RES 10K OHM 1/4W 5% AXIAL	stackpole	CF14JT10K0	CF14JT10K0CT-ND
1	SW1	SPST MOMENTARY SWITCH	SWITCH PUSH SPST-NO 0.1A 32V	C&K	D6C40 F1 LFS	401-1966-ND
1	U1	SN74LS04	DIL14	Texas Instruments	SN74LS04N	296-1629-5-ND
1	U10	74ALS521	DIL20	Texas Instruments	SN74F521N	296-33912-5-ND
1	U2	74LS32	DIL14	Texas Instruments	SN74LS32N	296-1658-5-ND
1	U3	MAX232(DIL)	IC TRANSCEIVER FULL 2/2 16DIP	Texas Instruments	MAX232N	296-1402-5-ND
1	U4	74ALS573	DIL20	Texas Instruments	SN74ALS573N	296-1621-5-ND
1	U5	6264	DIL28_WB15,24_P2,54	Alliance Memory	AS6C6264-55PCN	1450-1036-ND

SBC-85 8085 CPU v1.0 BOM

QTY	Name	Value	Package/description	Manufacturer	Manufacturer PN	DIGI KEY PN
2	U6, U9	2732	DIL24_SOT101-1			
1	U7	8155	DIL40			
1	U8	8085	DIL40			
		CONN JUMPER SHORTING .100"			QPC02SXGN-RC	S9337-ND
1		AC/DC DESKTOP ADAPTER 5V 20W	Power Supply 2.1mm x 5.5mm 5V 20W	phihong USA	PSAC30U-050L6	993-1343-ND
For the 74xxx you are unlikely to find LS versions so use ALS or HCT whichever you can find.						

Definitions of Terms and Notation

0xF

Hex Interpretation of 4 binary bits (nibble), in this example HEX F which is 1111 in binary

0xFF

Hex Interpretation of 8 binary bits (byte), in this example HEX FF which is 1111 1111 in binary

0xFFFF

Hex Interpretation of 16 binary bits or Word (two bytes). In this example HEX FFFF is the interpretation of the binary value 1111 1111 1111 1111

Address Decoding

The process (decoding) or part of the circuit (decoder) that determines which addresses are assigned to which memory or I/O device and, typically, results in the enabling of one specific memory or I/O device on the board or system.

A*n*

Individual Address Line where n is 0-15

AD*n*

Individual Multiplexed Address / Data line where n is 0-8

BOM

Bill of Materials

Buffer (also driver)

A device that 're-drives' or buffers a signal to unload (or separate from) the original signal. One direction (see also transceiver)

Byte

8-bits

Component Side

The 'top' of the PC board where the components are mounted. On the SBC-85 this is the side with the bulk of the silkscreen and the component numbers and footprints.

Contention (e.g., bus contention or signal contention)

A condition where two or more devices are simultaneously attempting to drive the same signal or bus. Technically, I suppose 'contention' only occurs when they disagree as to what the status of the signal or bus should be, e.g., one is pulling high while the other is pulling low but neither is enjoying the situation.

CS/ or CS*

Chip Select (reverse, a.k.a., negative logic) where a logic LOW (0v) is active

Decoding (Memory or I/O)

The process of determining which specific device should be enabled given any memory or I/O address.

EPROM

Erasable Programmable, Read Only Memory. A non-volatile memory device that can repeatedly be erased (generally by exposing to a UV light source) and field programmed. Compare to ROM, PROM, and EEPROM

EEPROM

Electrically Erasable Programmable, Read Only Memory. A non-volatile memory device that can repeatedly be erased and programmed, typically in-circuit. Compare to ROM, PROM, and EPROM

JEDEC Socket

Joint Electron Device Engineering Council standardized memory socket that can be configured to accept any JEDEC compliant memory chip within the design range of the socket.

I/O

Input / Output

I/O Mapped I/O

An address decoding scheme where the I/O ports are mapped using the address lines AND requiring that the *IO/M* signal be at logic LOW*. In this configuration, a port instruction such as OUT 23H would write only to the I/O port that decodes to address 23H. The instruction LDA 2323H will only read from the memory location at 2323H. See also *Memory Mapped I/O*.

LSB

Least Significant Byte. On a multibyte word this is the byte with the least weight, i.e., the furthest towards the right. E.g., the '34' in the word 0x1234

LSBit

Least Significant Bit. The bit with the least weight, i.e., the furthest towards the right. E.g., in the byte 11111110 the least significant bit is the '0'

Memory Mapped I/O

An address decoding scheme where the I/O ports are intermixed and use the same addresses as memory and the *IO/M* signal is not used*. In this configuration, there is no differentiation between memory and I/O. As an example, a port instruction such as OUT 23H will write not only to the I/O port that decodes to address 23H but it would write to the memory location at 2323H. Likewise, the instruction LDA 2323H will read the contents of Port 23H. The advantage of memory mapped I/O is that any memory instructions can be used to access I/O ports. The disadvantage is that I/O port addresses must be set to not overlap with any memory locations. See also *I/O Mapped I/O*.

MSB

Most Significant Byte. On a multibyte word this is the byte with the highest weight, i.e., the furthest towards the left. E.g., the 'AB' in the word 0AB12 Be careful not to confuse a

leading zero as the MSB such as in the byte 0A3H where the leading zero is required for many assemblers

MSBit

Most Significant Bit. The bit with the most weight, i.e., the furthest towards the left. E.g., in the byte 10000000 the most significant bit is the '1'.

Nibble

4-bits, half a byte.

OBP

On Board Port.

On

Logic TRUE or active. May be HIGH (+5V) or LOW (0V)

Off

Logic FALSE or inactive. May be HIGH (+5V) or LOW (0V)

o.c. (Open Collector or Open Drain)

A form of device output where the driving device can only pull the logic level low (e.g., to 0V in TTL). Since no output can drive the circuit, multiple open collector outputs can be tied together. Typically a pull-up resistor takes the circuit to logic one (+5V) if none of the open collector outputs are actively pulling the circuit low.

PROM

Programmable Read Only Memory. A non-volatile memory device that can be field programmed, and is typically One Time Programmable (OTP). Compare to ROM, EPROM, and EEPROM

ROM

Read Only Memory. A non-volatile memory device that is (typically) factory masked to create its internal bit pattern. Compare to PROM, EPROM, and EEPROM

Sandbox

An expansion or protype area for free-range creators to play and express themselves.

SBC

Single Board Computer, i.e, a system which contains the processor and any memory (RAM & ROM) required to fully operate.

STD Bus

Standard Bus. A backplane based bus created by Pro-Log and Mostek, primarily for process control.

SW*n*

Switch were n is the switch identifier

SID

Serial Input Data (8085 pin 5)

SOD

Serial Output Data (8085 pin 4)

Solder Side

The 'bottom' of the PC board

Transceiver

A bi-directional buffer, i.e., a device that 're-drives' or buffers a signal to unload (or separate from) the original signal. The transceiver can either drive the signal from A to B or from B to A depending upon the state of the direction input (usually labelled something obvious like *DIR* or *A->B*). See also *buffer*.

Tri-State (or 3-state)

A form of device output where the output can be released into the high-impedance state where it is not driven high or low by the output device. When an output is in the tri-state mode, that device output is no longer controlling the output circuit which then allows another device to control the circuit.

U*n*

Integrated Circuit ID n. *Un.m* would be pin *m* on IC *n*.

UART

Universal Asynchronous Receiver Transmitter. A serial port controller that autonomously handles asynchronous serial communication e.g., RS232

Universal Site

A term used to reference a socket (usually memory) that can be used with multiple devices.

USART

Universal Synchronous Asynchronous Receiver Transmitter. A serial port controller that autonomously handles either synchronous or asynchronous serial communication e.g., RS232