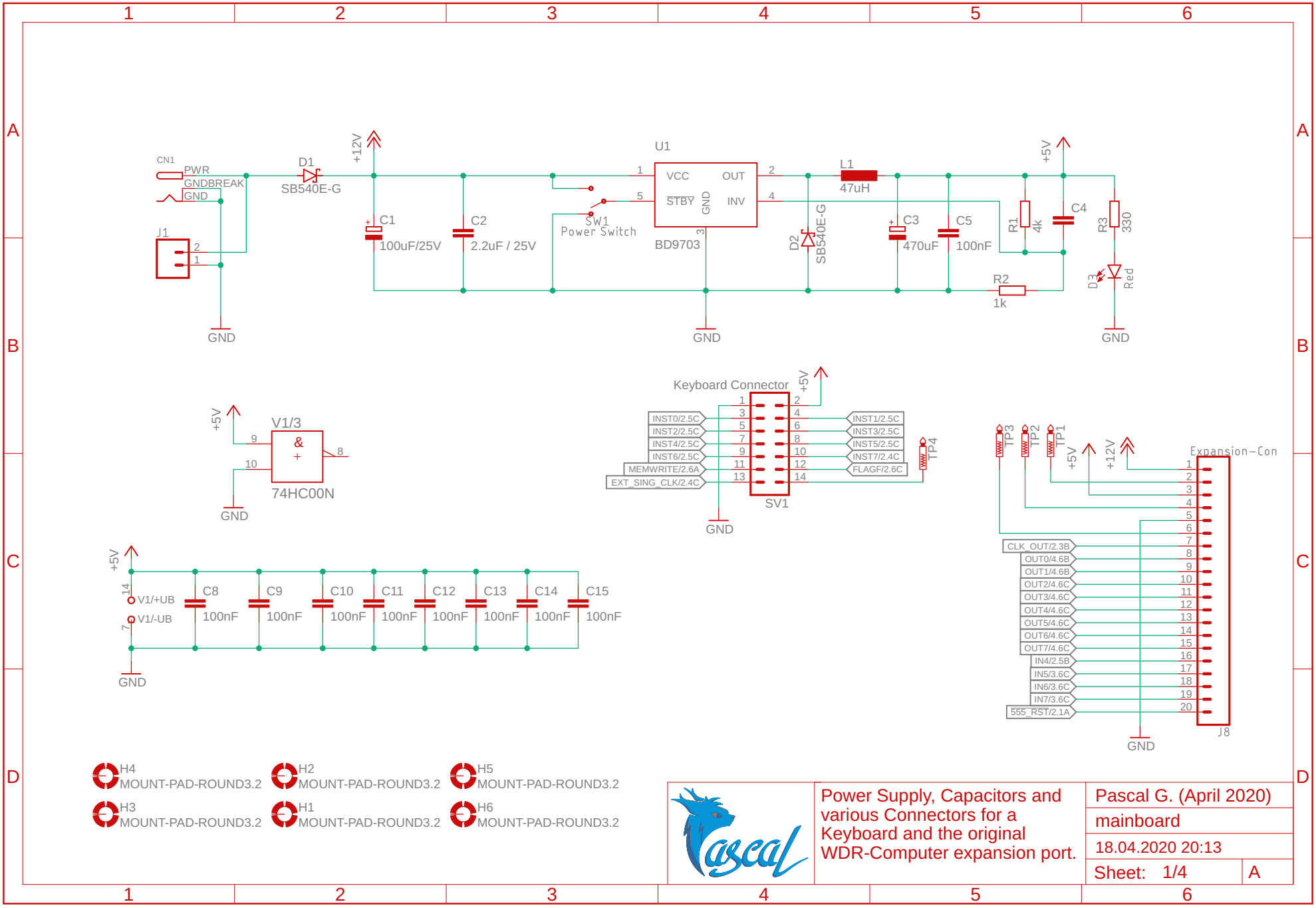
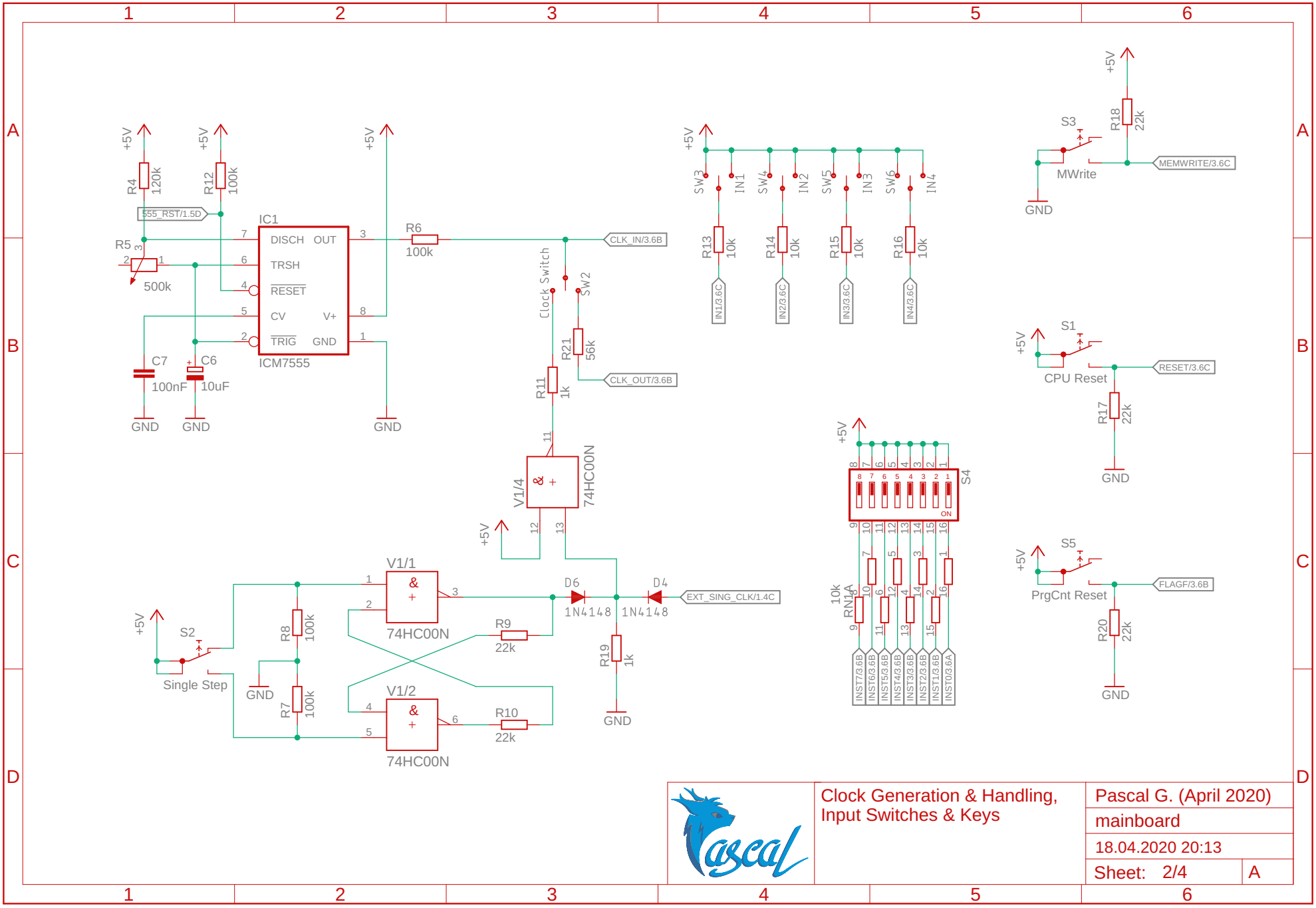
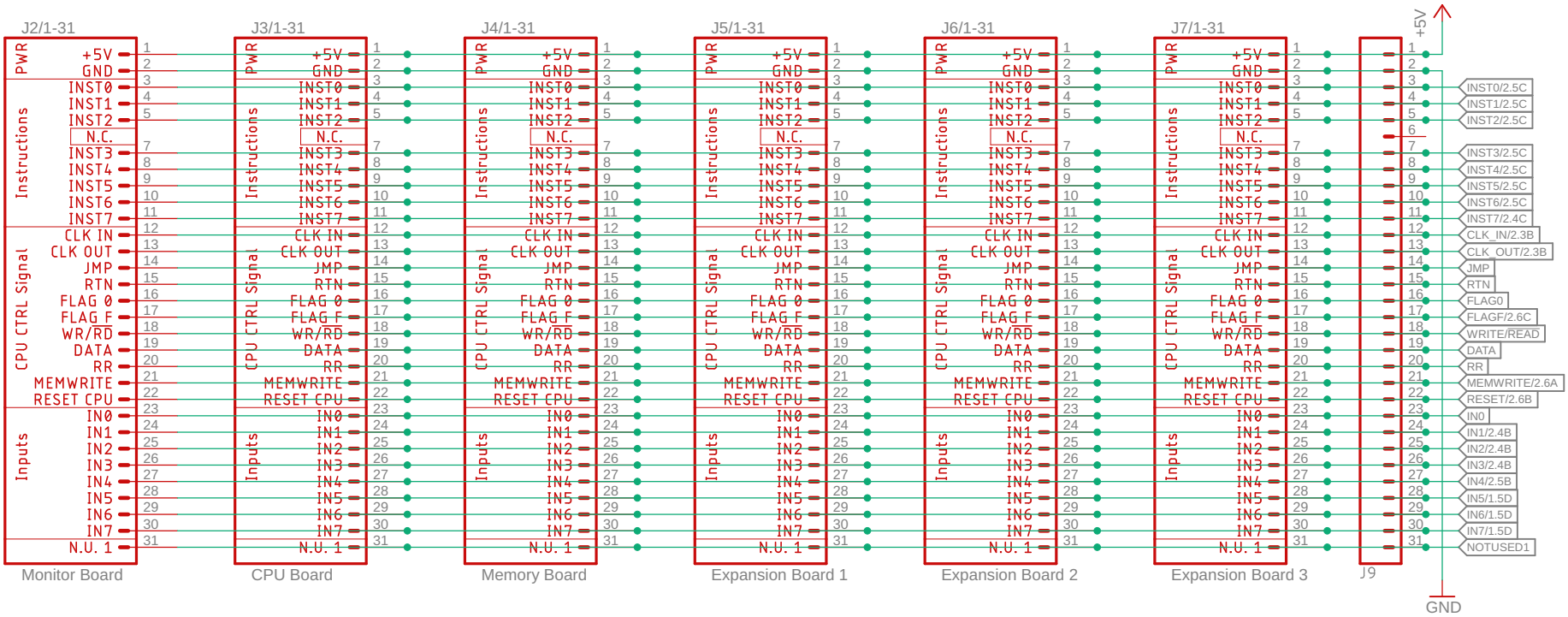


Power Supply, Capacitors and various Connectors for a Keyboard and the original WDR-Computer expansion port.

Pascal G. (April 2020)	
mainboard	
18.04.2020 20:13	
Sheet: 1/4	A


1
2
3
4
5
6
A
B
C
D
+5V
R4
120k
R12
100k
555_RST/1.5D
IC1
DISCH
OUT
TRSH
RESET
CV
V+
TRIG
GND
ICM7555
R5
500k
C7
100nF
C6
10uF
R6
100k
CLK_IN/3.6B
Clock Switch
SW2
R21
56k
CLK_OUT/3.6B
R11
1k
V1/4
74HC00N
V1/1
V1/2
R8
100k
R7
100k
R9
22k
R10
22k
D6
D4
1N4148
1N4148
EXT_SING_CLK/1.4C
R19
1k
S2
Single Step
SW3
SW4
SW5
SW6
IN1
IN2
IN3
IN4
R13
10k
R14
10k
R15
10k
R16
10k
IN1/3.6C
IN2/3.6C
IN3/3.6C
IN4/3.6C
S3
MWrite
R18
22k
MEMWRITE/3.6C
S1
CPU Reset
R17
22k
RESET/3.6C
S4
ON
10k
RN1A
INST7/3.6B
INST6/3.6B
INST5/3.6B
INST4/3.6B
INST3/3.6B
INST2/3.6B
INST1/3.6B
INST0/3.6A
S5
PrgCnt Reset
R20
22k
FLAGF/3.6B
Clock Generation & Handling,
Input Switches & Keys
Pascal G. (April 2020)
mainboard
18.04.2020 20:13
Sheet: 2/4
A



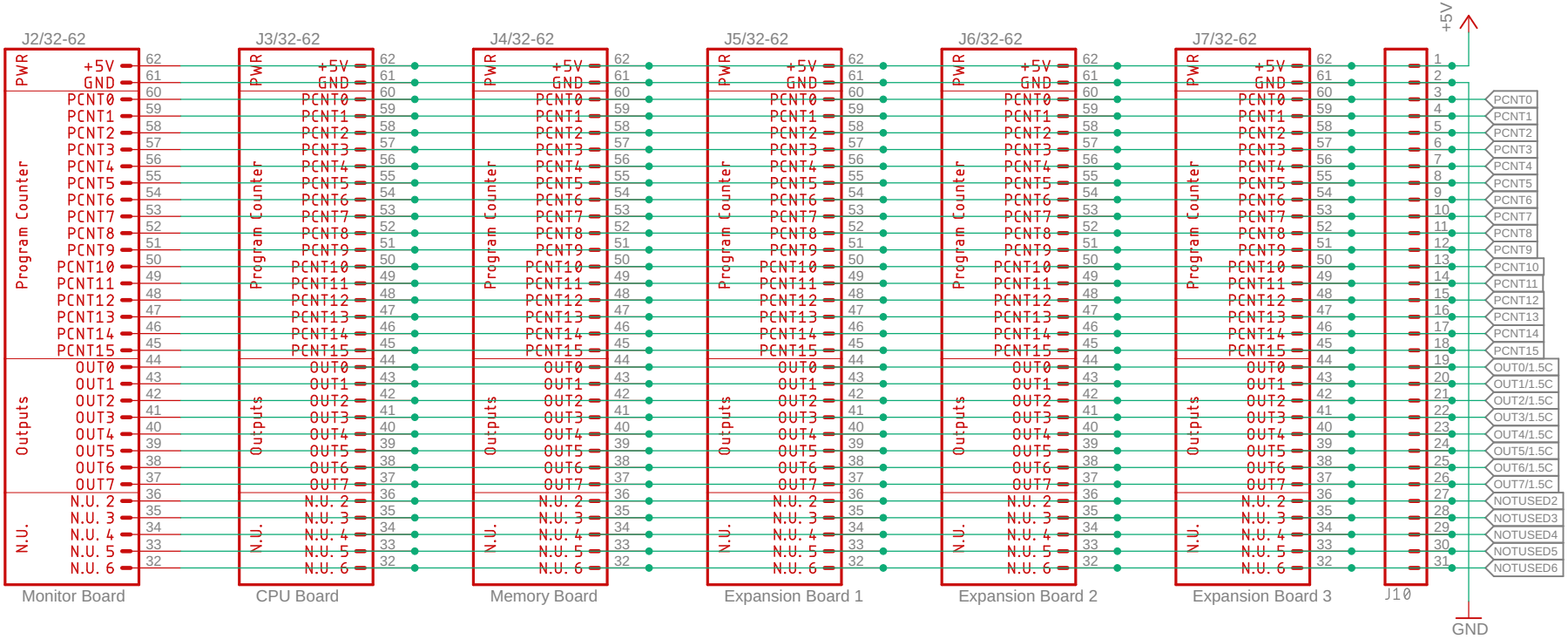
Bottom-Row Connections of the Card-Edge-Connector (1-Bit BUS)

Pascal G. (April 2020)

mainboard

18.04.2020 20:13

Sheet: 3/4 A



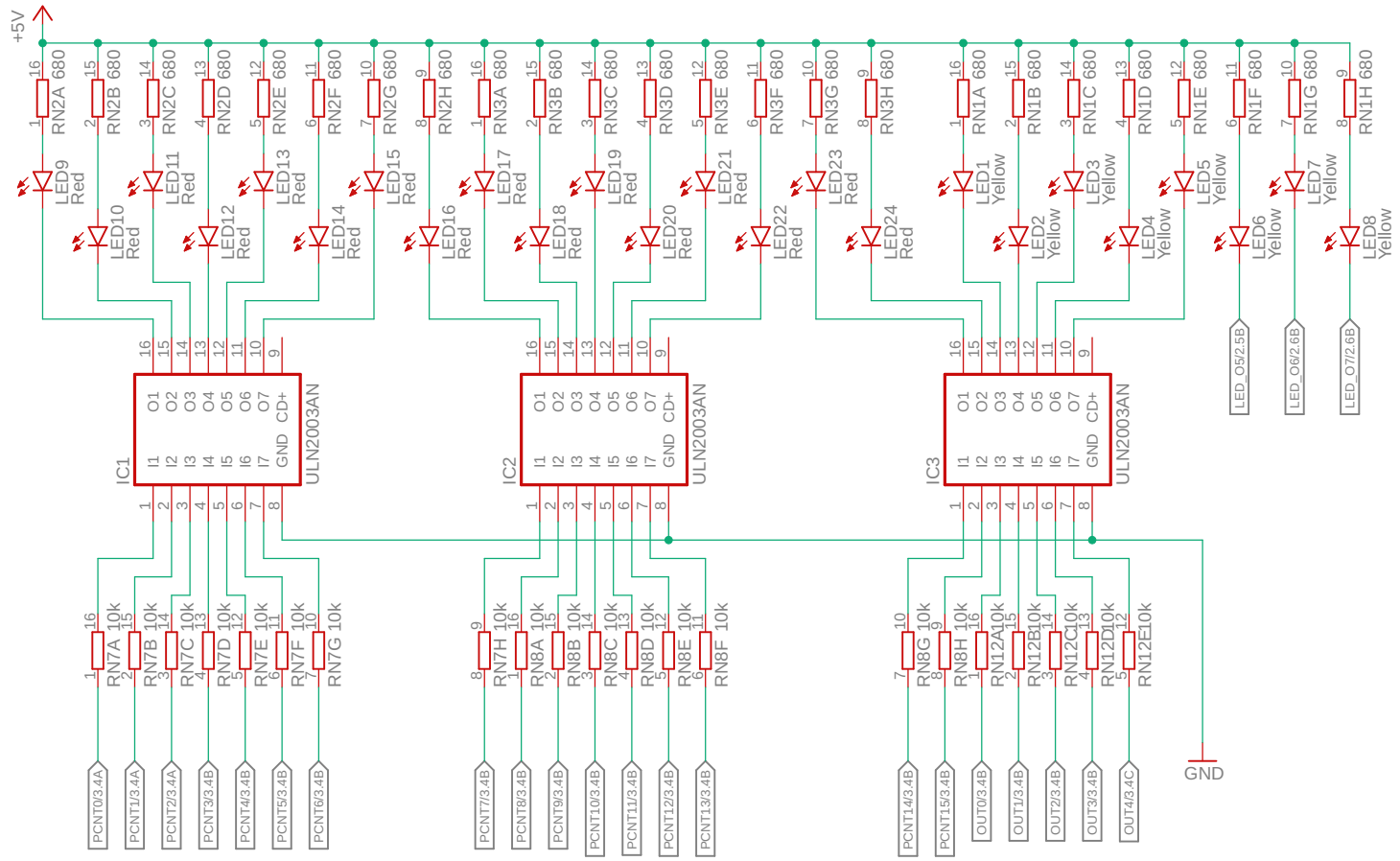
Bottom-Row Connections of the Card-Edge-Connector (1-Bit BUS)

Pascal G. (April 2020)

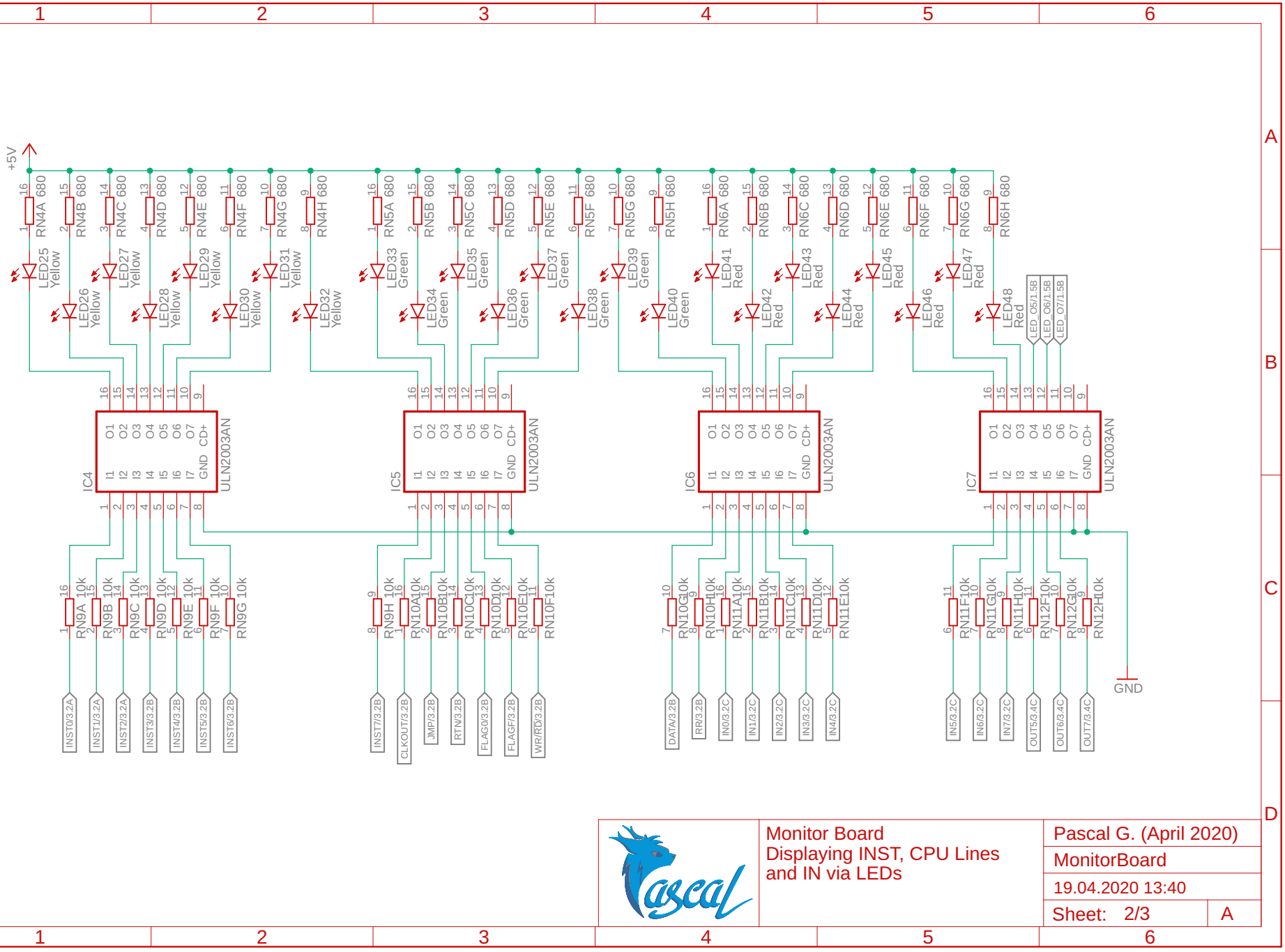
mainboard

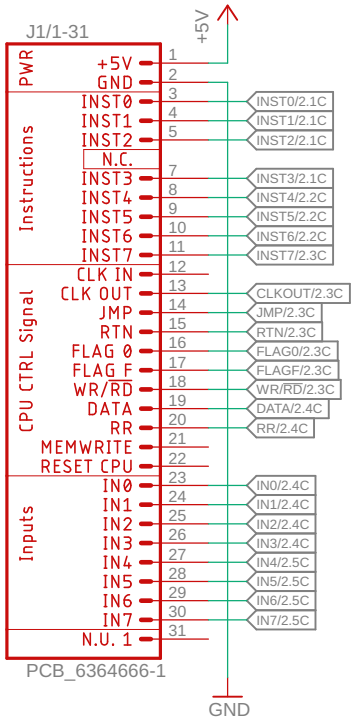
18.04.2020 20:13

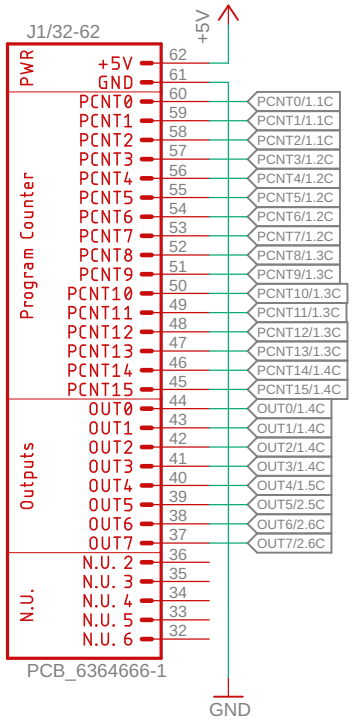
Sheet: 4/4 A



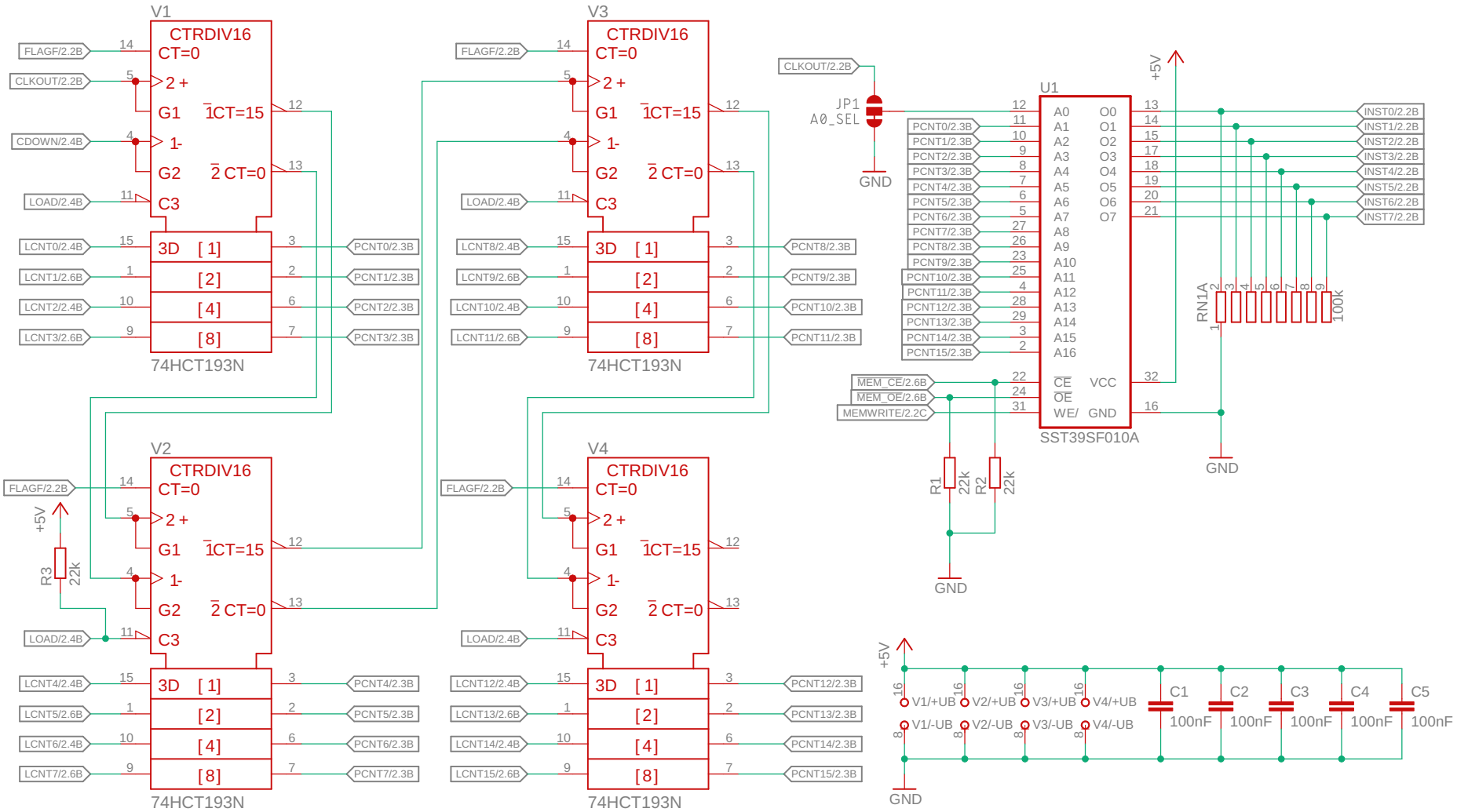
Monitor Board Displaying OUT and PCNT via LEDs	Pascal G. (April 2020)	
	MonitorBoard	
	19.04.2020 13:40	
	Sheet: 1/3	A

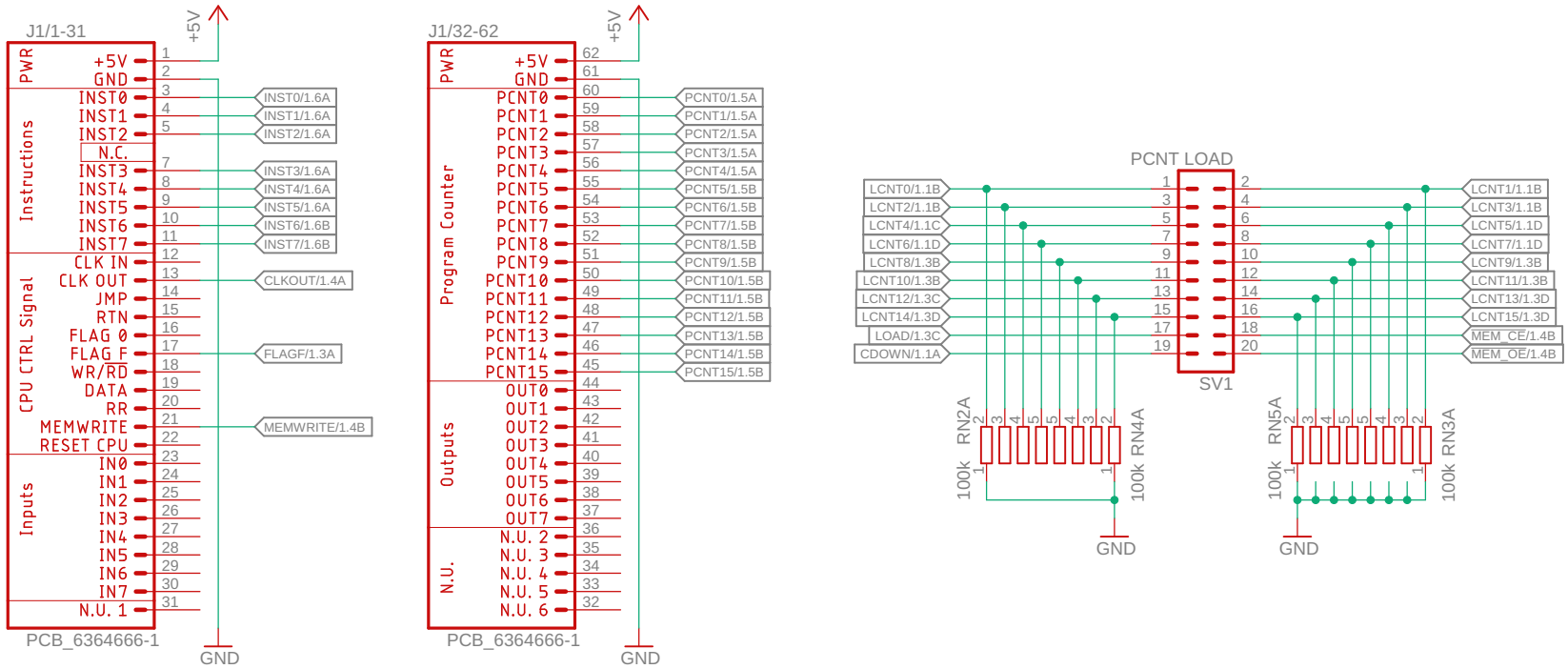

+5V
RN4A 680
RN4B 680
RN4C 680
RN4D 680
RN4E 680
RN4F 680
RN4G 680
RN4H 680
RN5A 680
RN5B 680
RN5C 680
RN5D 680
RN5E 680
RN5F 680
RN5G 680
RN5H 680
RN6A 680
RN6B 680
RN6C 680
RN6D 680
RN6E 680
RN6F 680
RN6G 680
RN6H 680
LED25 Yellow
LED26 Yellow
LED27 Yellow
LED28 Yellow
LED29 Yellow
LED30 Yellow
LED31 Yellow
LED32 Yellow
LED33 Green
LED34 Green
LED35 Green
LED36 Green
LED37 Green
LED38 Green
LED39 Green
LED40 Green
LED41 Red
LED42 Red
LED43 Red
LED44 Red
LED45 Red
LED46 Red
LED47 Red
LED48 Red
LED_O5/1.5B
LED_O6/1.5B
LED_O7/1.5B
IC4
IC5
IC6
IC7
ULN2003AN
RN9A 10k
RN9B 10k
RN9C 10k
RN9D 10k
RN9E 10k
RN9F 10k
RN9G 10k
RN9H 10k
RN10A 10k
RN10B 10k
RN10C 10k
RN10D 10k
RN10E 10k
RN10F 10k
RN10G 10k
RN10H 10k
RN11A 10k
RN11B 10k
RN11C 10k
RN11D 10k
RN11E 10k
RN11F 10k
RN11G 10k
RN11H 10k
RN12F 10k
RN12G 10k
RN12H 10k
INST0/3.2A
INST1/3.2A
INST2/3.2A
INST3/3.2B
INST4/3.2B
INST5/3.2B
INST6/3.2B
INST7/3.2B
CLKOUT/3.2B
JMP/3.2B
RTN/3.2B
FLAG0/3.2B
FLAGF/3.2B
WR/RD/3.2B
DATA/3.2B
RR/3.2B
IN0/3.2C
IN1/3.2C
IN2/3.2C
IN3/3.2C
IN4/3.2C
IN5/3.2C
IN6/3.2C
IN7/3.2C
OUT5/3.4C
OUT6/3.4C
OUT7/3.4C
GND
Monitor Board
Displaying INST, CPU Lines
and IN via LEDs
Pascal G. (April 2020)
MonitorBoard
19.04.2020 13:40
Sheet: 2/3
A



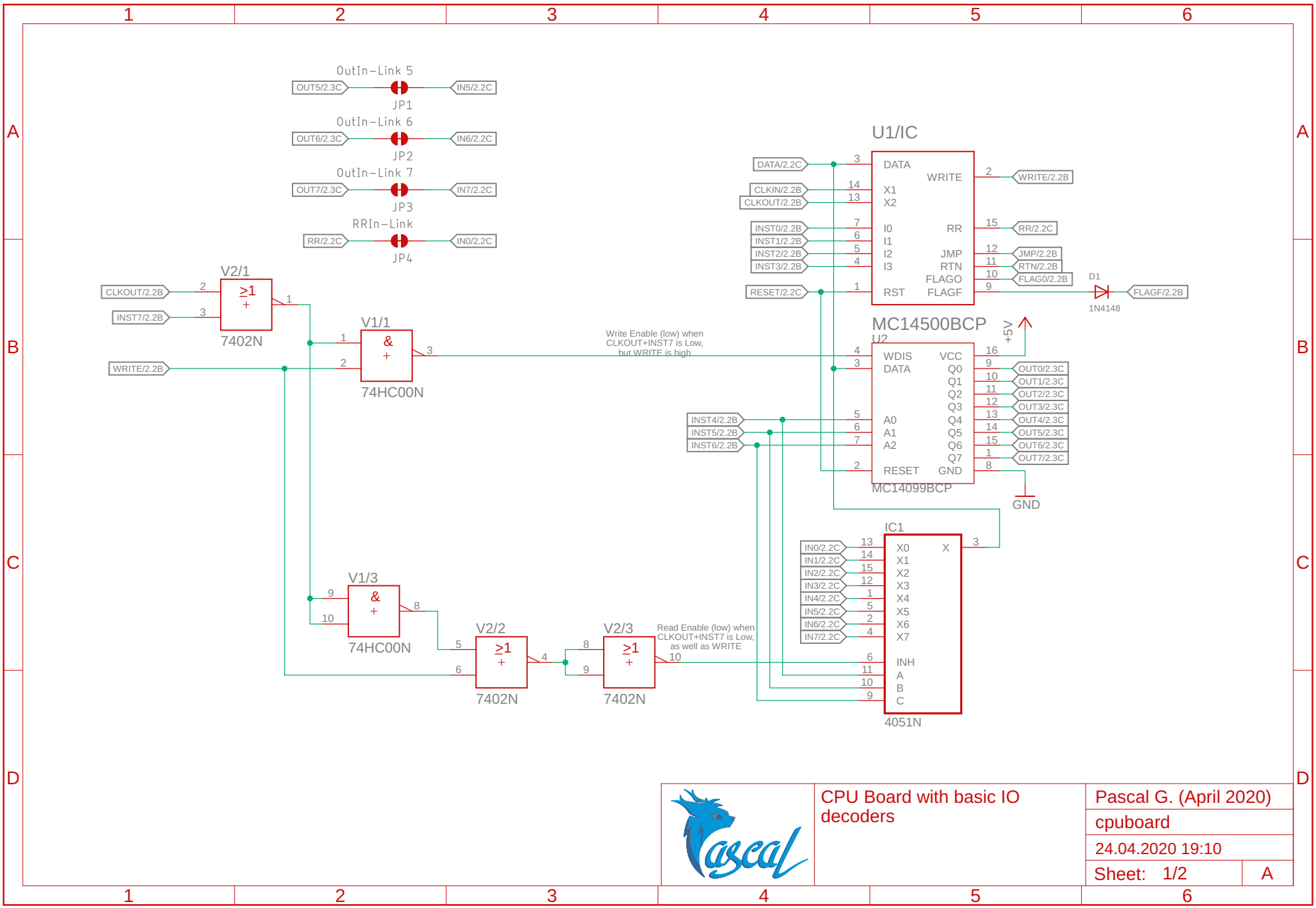


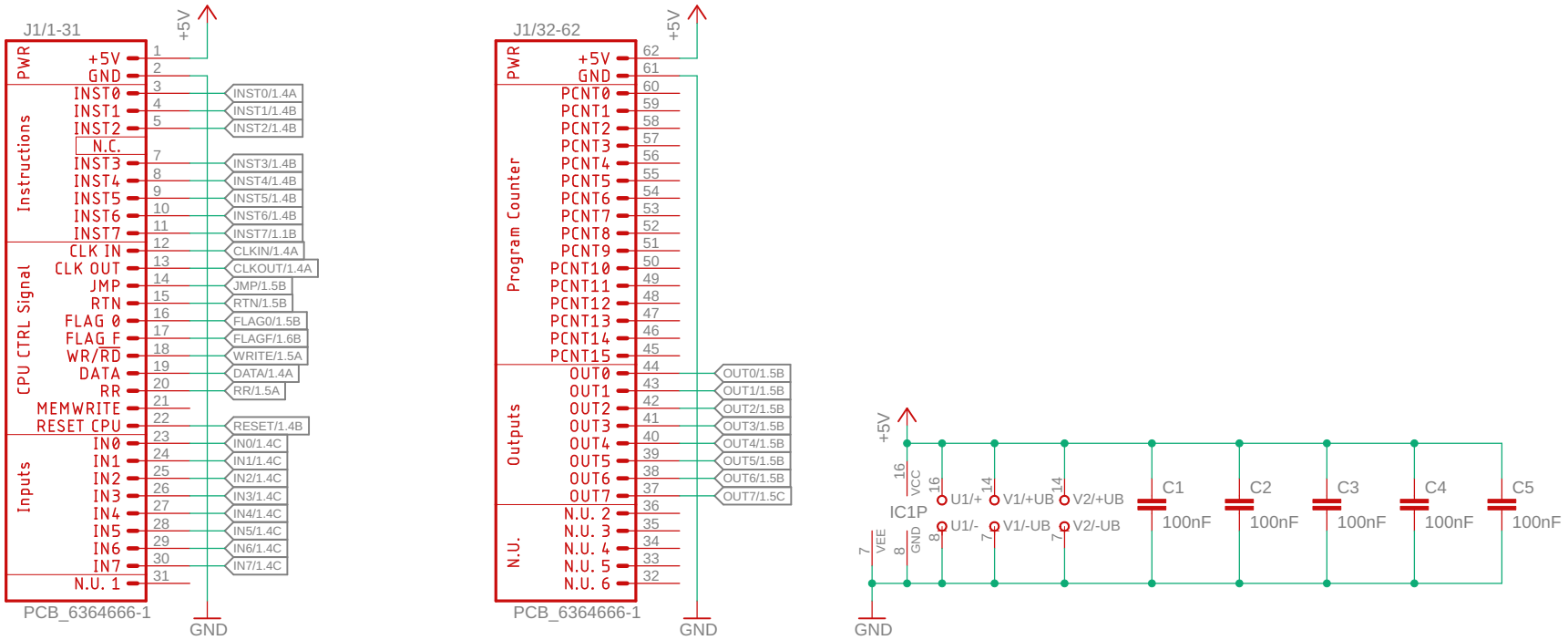
Pascal G. (April 2020)	
MonitorBoard	
19.04.2020 13:40	
Sheet: 3/3	A


V1
CTRDIV16
CT=0
74HCT193N
V2
CTRDIV16
CT=0
74HCT193N
V3
CTRDIV16
CT=0
74HCT193N
V4
CTRDIV16
CT=0
74HCT193N
JP1
A0_SEL
U1
SST39SF010A
RN1A
100k
R1
22k
R2
22k
R3
22k
C1
100nF
C2
100nF
C3
100nF
C4
100nF
C5
100nF
+5V
GND
Memory Board with 64k x 8Bit
Jumper J1 allows to experiment
with interlaced memory, turning it
into a 64k x 16Bit system
(12Bit IO Address range)
Pascal G (April 2020)
memory
13.04.2020 00:31
Sheet: 1/2
A



	BUS Connector and Program Counter LOAD Connector (Allows to implement proper Jumps in the future maybe)	Pascal G (April 2020)
		memory
		13.04.2020 00:31
		Sheet: 2/2 | A


OutIn-Link 5
OUT5/2.3C
IN5/2.2C
JP1
OutIn-Link 6
OUT6/2.3C
IN6/2.2C
JP2
OutIn-Link 7
OUT7/2.3C
IN7/2.2C
JP3
RRIn-Link
RR/2.2C
IN0/2.2C
JP4
U1/IC
DATA/2.2C
CLKIN/2.2B
CLKOUT/2.2B
INST0/2.2B
INST1/2.2B
INST2/2.2B
INST3/2.2B
RESET/2.2C
DATA
WRITE
X1
X2
I0
I1
I2
I3
RST
RR
JMP
RTN
FLAGO
FLAGF
WRITE/2.2B
RR/2.2C
JMP/2.2B
RTN/2.2B
FLAG0/2.2B
D1
1N4148
FLAGF/2.2B
V2/1
CLKOUT/2.2B
INST7/2.2B
≥1
7402N
V1/1
&
74HC00N
WRITE/2.2B
Write Enable (low) when
CLKOUT+INST7 is Low,
but WRITE is high
MC14500BCP
U2
WDIS
DATA
A0
A1
A2
RESET
VCC
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
GND
+5V
OUT0/2.3C
OUT1/2.3C
OUT2/2.3C
OUT3/2.3C
OUT4/2.3C
OUT5/2.3C
OUT6/2.3C
OUT7/2.3C
MC14099BCP
INST4/2.2B
INST5/2.2B
INST6/2.2B
V1/3
&
74HC00N
V2/2
≥1
7402N
V2/3
≥1
7402N
Read Enable (low) when
CLKOUT+INST7 is Low,
as well as WRITE
IC1
IN0/2.2C
IN1/2.2C
IN2/2.2C
IN3/2.2C
IN4/2.2C
IN5/2.2C
IN6/2.2C
IN7/2.2C
X0
X1
X2
X3
X4
X5
X6
X7
X
INH
A
B
C
4051N
CPU Board with basic IO decoders
Pascal G. (April 2020)
cpuboard
24.04.2020 19:10
Sheet: 1/2
A



	CPU Board with basic IO decoders	Pascal G. (April 2020)
		cpuboard
		24.04.2020 19:10
		Sheet: 2/2 A