Sheet: power

File: power.sch

Sheet: fpga_power

File: fpga_power.sch

Sheet: fpga_cfg

File: fpga_cfg.sch

Sheet: fpga_io

File: fpga_io.sch

Sheet: hyperram

File: hyperram.sch

Sheet: ftdi

File: ftdi.sch

H101 MountingHole

H103 MountingHole

H102 MountingHole

H104 MountingHole

LOGO101

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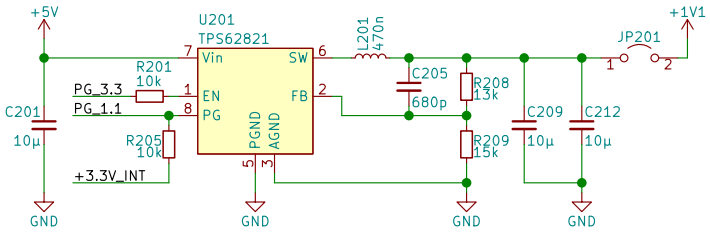
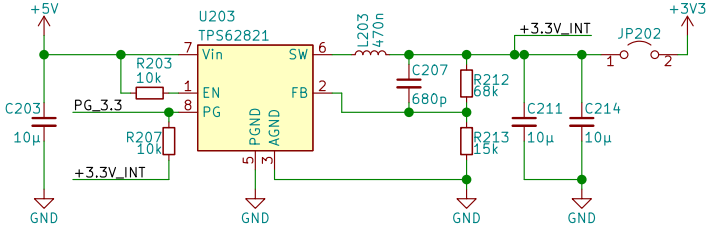
Sheet: /

File: fusbee5.sch

Title: Overview – FUSBee5

Size: A4	Date: 27.03.2020	**Rev: v1a**
KiCad E.D.A. kicad (5.1.5-81-g5fdc42420)		Id: 1/7



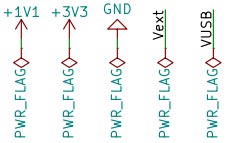


Dividers:
68/15 → 3.32V
30/15 → 1.8V
12/15 → 1.08V
13/15 → 1.12V

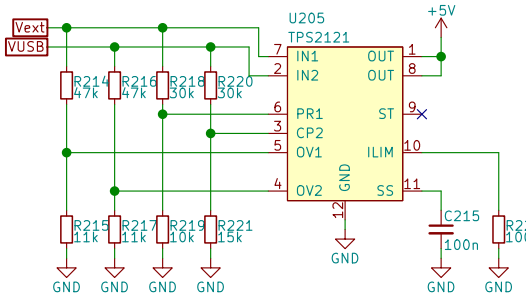
Inductors:
Murata: DFE201610E-R47M OR DFE201210S-R47M

Optional feed-forward capacitor:
Cff = 12µs / R2 = 12µs / 15k = 800p → 680p

Power sequencing:
Vccio8 is required to reach Vih of an external SPI flash before Vcc and Vccaux are ramped up to Vporup, if the FPGA operates as SPI master!



Automatic 5V power source selection and overvoltage protection

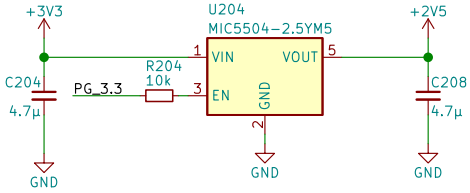


11k → 22k||22k
ILIM=65.2/(R/1000)^0.861 → 1.24A@100k
tss=6.41ms@100nF

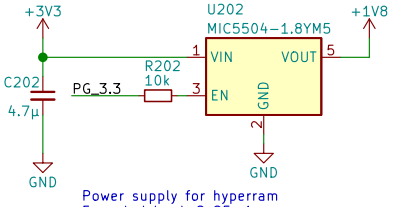
CP2<Vref && PR1>Vref → IN1
CP2>Vref && PR1<Vref → IN2

CP2>Vref && PR1>Vref && PR1>CP2 → IN1
CP2>Vref && PR1>Vref && PR1<CP2 → IN2

OPTIONAL: PR1=GND && CP2=GND
IN1>IN2 → IN1
IN1<IN2 → IN2

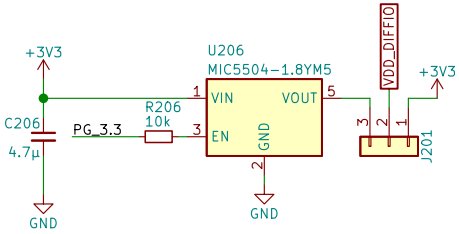


Power supply for FPGA Vaux



Power supply for hyperram
Expected load: 2x25mA

If hyperram with VDD=3.3V is used, bridge this LDO.



Power supply for differential IO banks

For any voltage other than 1.8V, chose a suitable pincompatible LDO.

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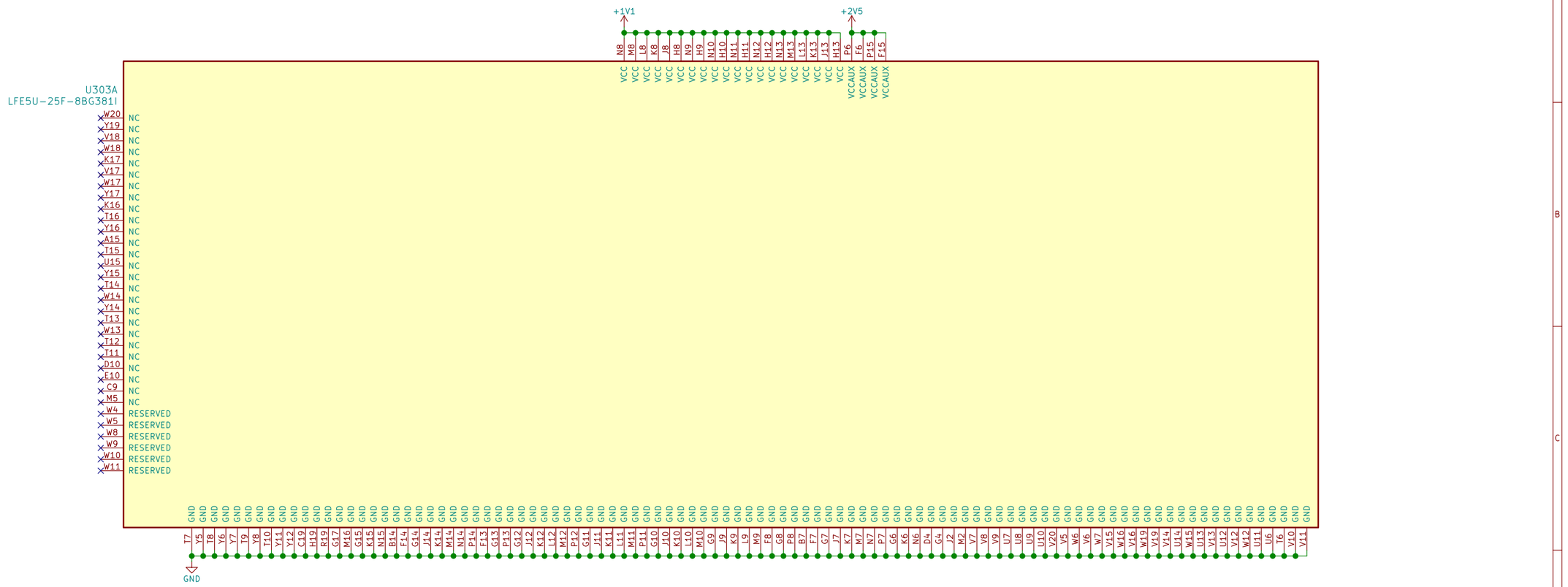
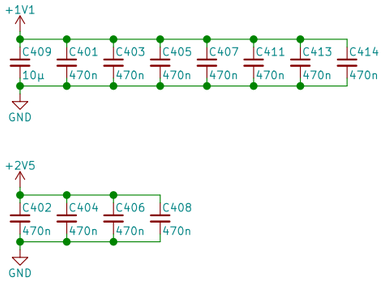
Sheet: /power/
File: power.sch

Title: Power Supply (FPGA/USB/RAM)

Size: A4	Date: 27.03.2020	**Rev: v1a**
KiCad E.D.A. kicad (5.1.5-81-g5fdc42420)		Id: 2/7





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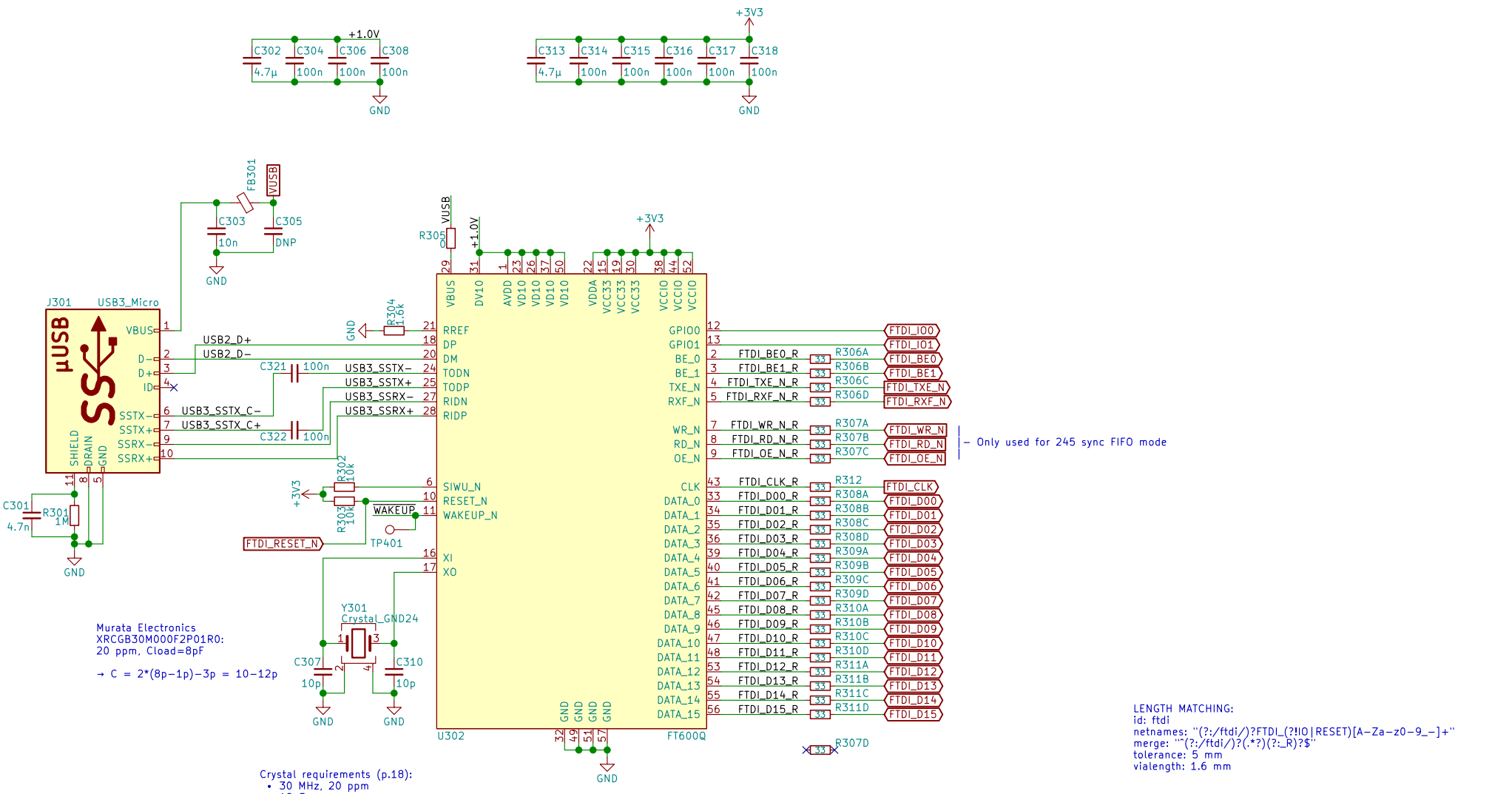
Sheet: /fpga_power/
File: fpga_power.sch

Title: FPGA Power Supply

Size: A3	Date: 27.03.2020	**Rev: v1a**
KiCad E.D.A. kicad (5.1.5-81-g5fdc42420)		Id: 3/7



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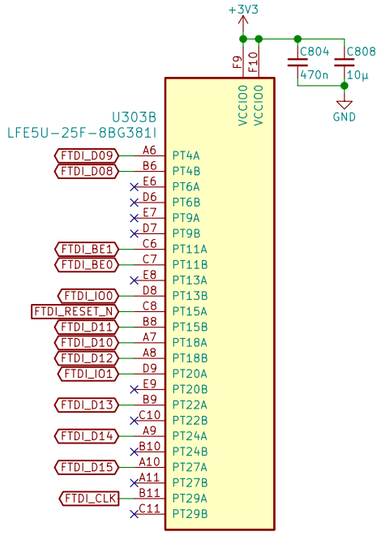
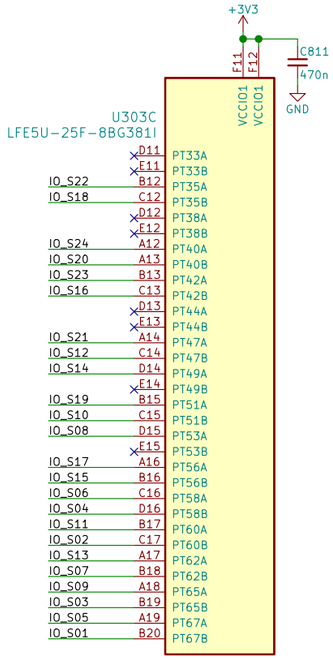
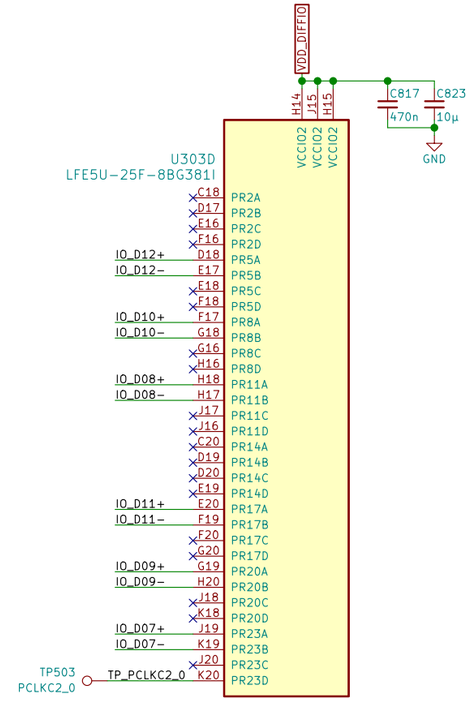
Sheet: /ftdi/
File: ftdi.sch

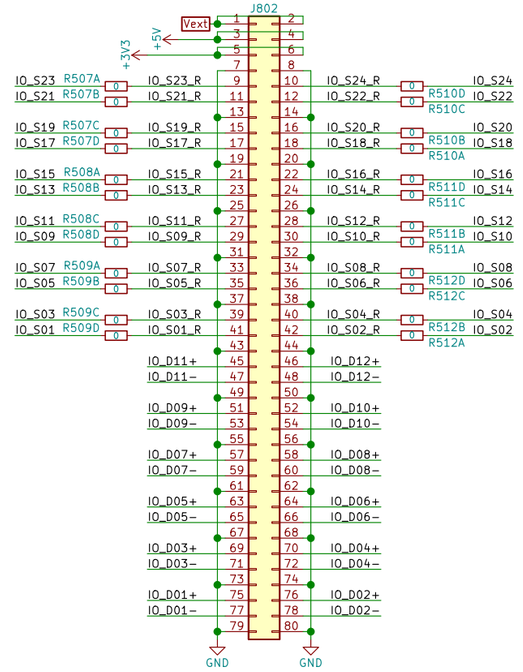
Title: USB 3.0 Interface

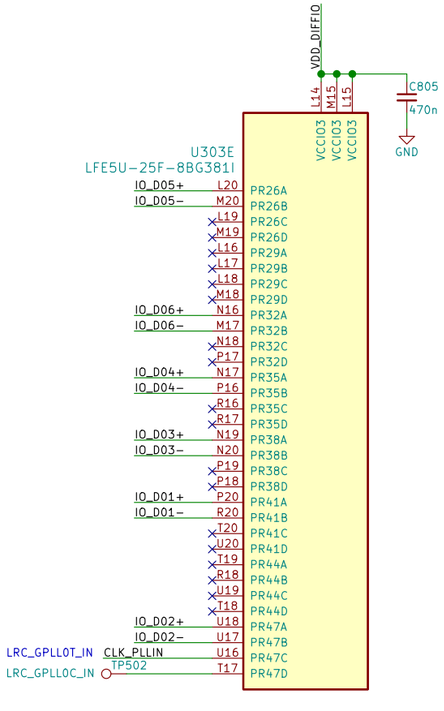
Size: A4	Date: 27.03.2020	**Rev: v1a**
KiCad E.D.A. kicad (5.1.5−81−g5fdc42420)		Id: 4/7

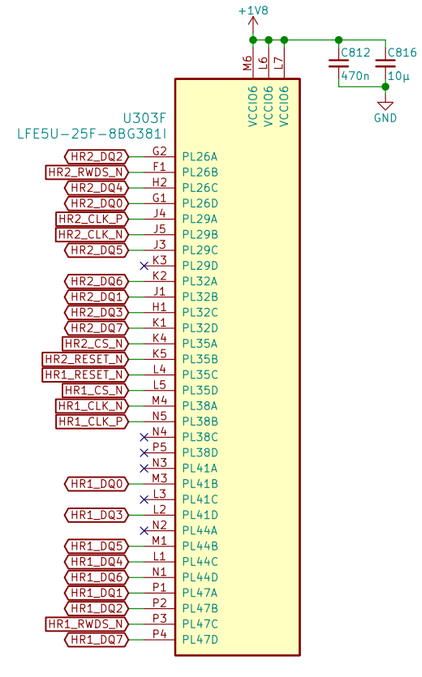


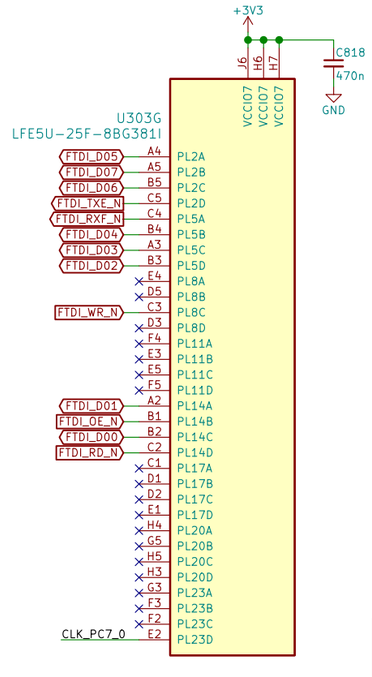


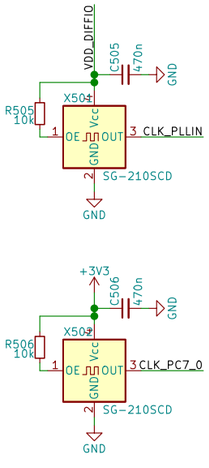












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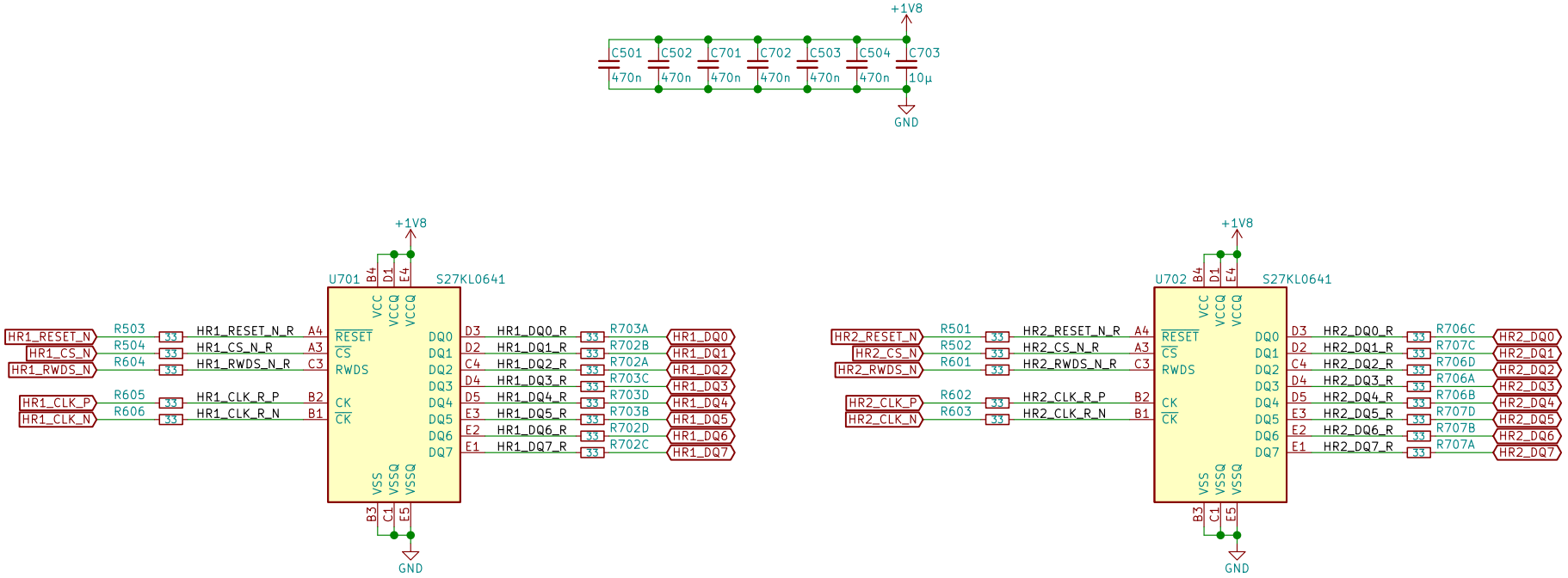
Sheet: /fpga_io/
File: fpga_io.sch

Title: FPGA IO-Banks

Size: A3	Date: 27.03.2020	**Rev: v1a**
KiCad E.D.A. kicad (5.1.5-81-g5fdc42420)		Id: 5/7



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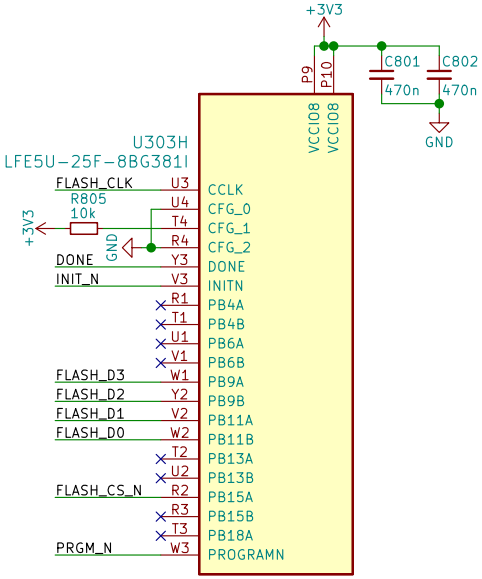
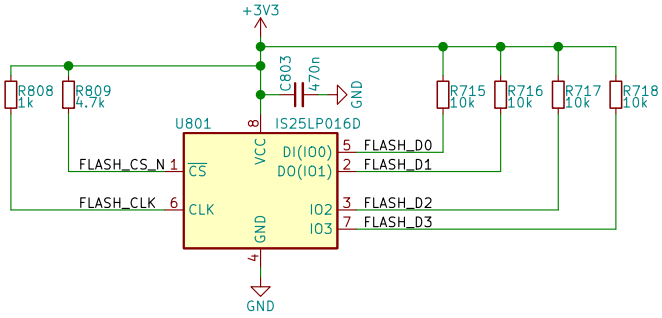
Sheet: /hyperram/
File: hyperram.sch

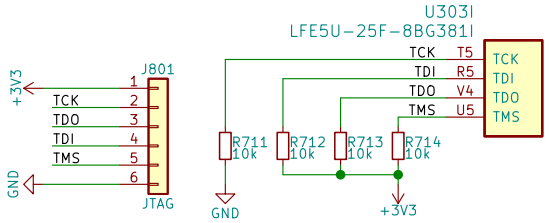
Title: Hyperram

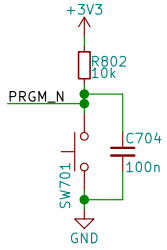
Size: A4	Date: 27.03.2020	**Rev: v1a**
KiCad E.D.A. kicad (5.1.5-81-g5fdc42420)		Id: 6/7

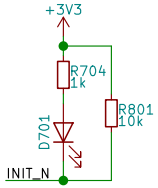
CFG_[0..2] = 0b010 → Master SPI Mode (1/2/4-bit)
PROGRAMN → Active-low input that initiates a device configuration
INITN → Open-drain IO that is low while the configuration SRAM is eraded; can be held low to prevent loading a configuration
DONE → Open-drain IO that indicates the FPGA is in user mode; can be held low to prevent FPGA from entering user mode

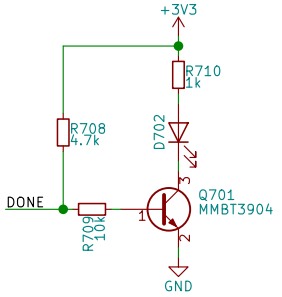












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Sheet: /fpga_cfg/
File: fpga_cfg.sch

Title: FPGA Configuration/Programming

Size: A4	Date: 27.03.2020	**Rev: v1a**
KiCad E.D.A. kicad (5.1.5-81-g5fdc42420)		Id: 7/7