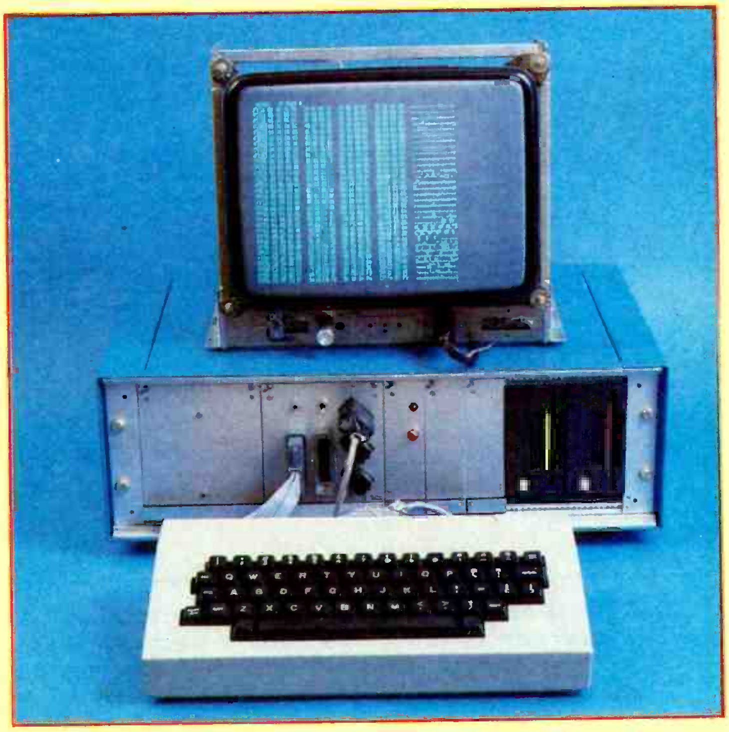
SC84 Micro-computer



This second section of the SC84 professional microcomputer for engineers and enthusiasts — the input/output interface — provides control for any floppy-disc drive, three parallel ports, an RS232 serial port and more.

by J.H. Adams

As well as providing basic serial, parallel, keyboard and disc input/output, this board also provides some system control and special facilities. At its heart is the Mostek STI, the MK3801N-6. This device is one of several types recently introduced which provide a set of peripheral facilities; for those familiar with Z80 peripherals, it combines a CTC, a PIO, an SIO and an interrupt controller. As befits the complexity of most Z80 peripherals, it has 24 internal registers, 16 of which are directly addressable and eight of which are indirectly addressable, and 16 sources of interrupts.

The STI comprises an eight-bit parallel port, a universal synchronous/asynchronous receiver transmitter (usart) for serial i/o, and four counter/timers, two of which are able to provide delays, count events and measure pulse widths, and two of which are only capable of providing delays. In delay mode, each timer switches the state of an individual output pin at precise intervals so the generators may be used to generate accurate frequency signals up to 500kHz — even four-part music. The two limited capability timers provide internal timing and/or determine usart bit rates.

The parallel i/o port has three features. It can be used just as an i/o port and as such each line may be configured as an input or output. Alternatively, some pins have special functions. Two are event and pulse-measurement inputs for the timers and two are 'handshake' lines for the usart. Thirdly, each line of the port may be used as a Z80 interrupt line. This is especially useful as the Z80 interrupt system is excellent but difficult to use with non-Z80 i.cs, a good example of this being control of a floppy disc drive. There is no Z80 disc controller and yet interrupts are really useful in a disc interface because of high data-transfer rates. The STI is the answer to this, providing 16 distinct interrupts each with its own priority. These could be integrated into a larger system, but the STI is so versatile that it is the only Z80 peripheral i.c. in the basic computer. If there is a blemish in the STI design it is that usart receiver and transmitter handshake lines are both outputs, presumably for compatibility with another rather odd Z80 device. This is unfortunate as logic would dictate that handshaking signals pass in the opposite direction to the data they are controlling, but the STI signals indicate that either the receiver or transmitter in the usart is empty. The former signal correctly warns external devices that the receiver is not ready but the latter is the wrong way round, the handshake being required from the external device to the STI and not away from it. As a result, these signals are disabled in this design and their i/o port lines provide handshaking in the conventional manner. It's a pity that this option was not designed into the chip.

Floppy-disc drive interfacing is handled by a Fujitsu MB8877A which is an improved and yet cheaper version of the common 1793 controller. The Fujitsu device only requires a +5V supply but for readers with a 1793 to hand, +12V is available on the p.c.b. so either part may be used. To the Z80, the controller looks like a specialized microcontroller with its own instruction set, comprising instructions to reset the system (i.e. move the head of the selected drive to the outermost track, track zero, as a means of getting the head over a known track), move the head to a particular track on the disc, and read or write one or more sectors or a complete track. Inside the con-

Table 1. Signal connections for typical drives.

Signal	Sony D32 3.5in	Std 34 way for 5.25in	Std 50 way for 8in
READY	26	6	22
RDDATA	24	30	46
WPRT	22	28	44
TR00	20	26	42
INDEX	18	8	20
SIDE	16	32	14
HLD	14, 1	16, 2	18
WG	12	24	40
WD	10	22	38
LC	—	—	—
STEP	8	20	36
DIRC	6	18	34
SEL1	4	12	28
SEL0	2	10	26
GND	7-25	1-33	1-49

The 5.25in pattern is used on BASF, Canon, Shugart and Tandon drives and the 8in pattern is used on DRE 7100 and 7200 types. Many other drives conform to these standards, but connections should be confirmed before the drive is used. Ground connections are joined over the range of odd-numbered pins indicated.

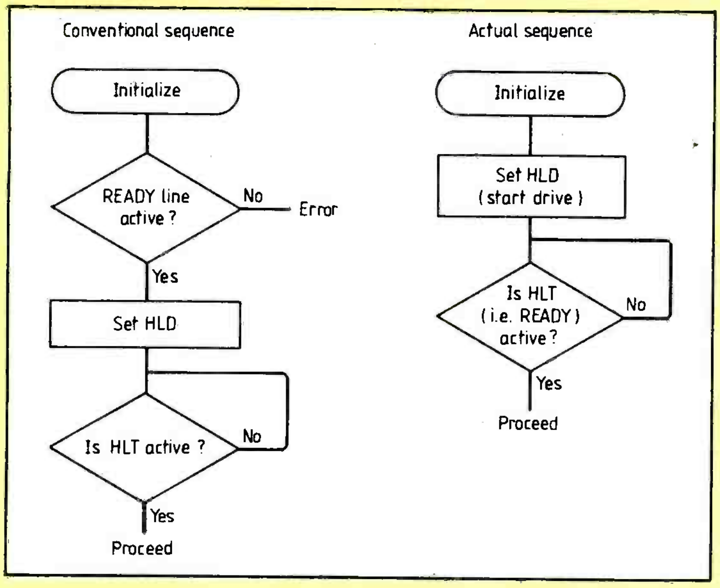


Fig.3. **Floppy-disc controller read/write execution sequence.**

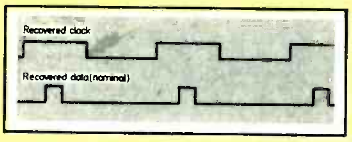


Fig.1. **The only requirements on disc data pulses are that they should not start within 40ns of a clock edge and that they must be entirely within one clock half cycle or must not be longer than 300ns for 8in double density or 600ns for 8in single density. This gives a wide margin of error in data recovery.**

Fig.2. **Floppy-disc, serial and parallel input/output are provided by this section (far right). Heart of the circuit is the 3801, containing a parallel port, a usart for serial communications, four counter/timers and an interrupt controller.**

troller there are several parameter registers which are loaded with the track and sector numbers required before a command is executed and read from or written to during data transfers between disc and Z80. The controller has two interrupt channels to the Z80 through the STI. One, DRQ, indicates that the controller is ready for data transfer, the other, INTRQ, that the controller has completed a command. In response to the second type, the system can read a status register within the controller to determine whether or not command execution ended satisfactorily, or whether an error pre-empted the command, e.g. the sector could not be found, or a write operation was attempted on a protected disc. The circuit handles both single and double density for all sizes of floppy disc. Switch S_{201} selects double density when closed and S_{202} is shown in the 5.25in, 3.25in and 3.5in/300rev/min drive position (the other is for 3.5in/600rev/min and 8in.

The MB8877A does not provide all of the facilities required for interfacing disc drives to a system. Data separation and regeneration of the data clocking signal is achieved by the SMC9216B (the B version, which is more expensive, only being required for double density) and write precompensation by the 74LS195. It is possible to get all of these facilities in one i.c. but at considerably greater expense and complexity.

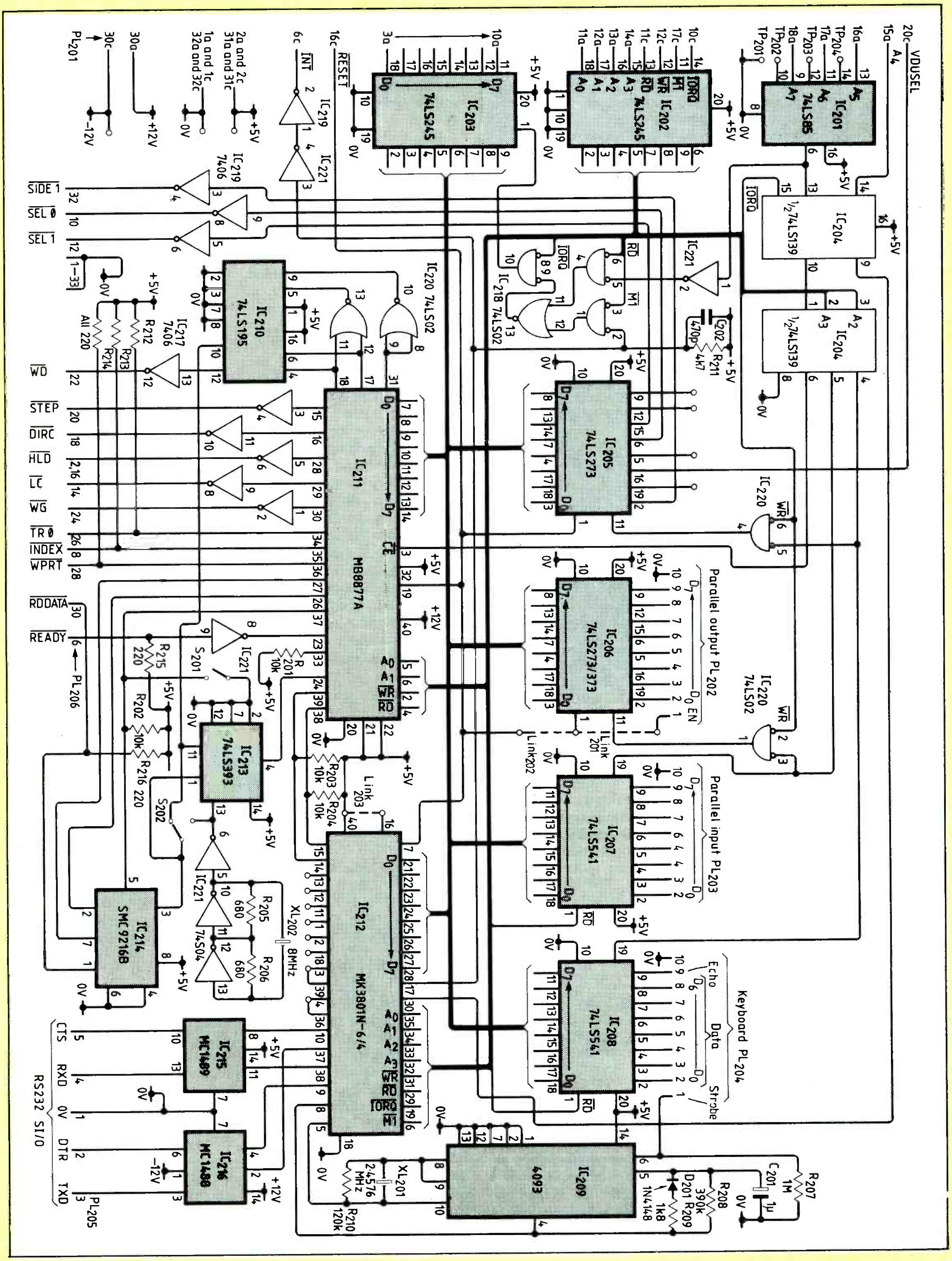
Data is recorded on disc by converting the stream of data bytes into serial form and recording the occurrence of binary 'ones' by reversing the sense of the flux recorded on the disc. The rate at which these flux reversals are made, and hence the amount of data stored, is limited by the calibre of the disc and recording head in the same way that higher frequencies are limited in audio systems. On playback these transitions are sensed, amplified and returned to digital form. Different systems have drives running at different speeds; discs change shape and data may consist of long strings of binary zeros, leaving long intervals where no transitions come from the disc. Thus additional and more regular information must be written on the disc to keep the playback process in step with the original recording rate. For this reason, extra flux transitions are inserted into the recording; for single-density recording an extra transition is inserted between every data bit period, making sure that there is a lot of synchronizing information available during playback but reducing the amount of data transferred by half. In double density recording, extra transitions are only inserted between bit periods corresponding to two adjacent zeros in the data bit stream, ensuring that an all-zeros sequence still contains some synchronizing data but, by being inserted in a natural gap in the bit stream, retaining the speed of the ideal system and not asking for a recording density, i.e. a frequency response, greater than that needed for single density. One method gives easier decoding at the expense of storage capacity, the other optimises storage at the expense of decoding complexity. Note that the physical requirement on the drive is the same for both methods so descriptions of some drives as being 'suitable for double density' — and the price premium — can be misleading.

Two data input signals are required by the controller. One is raw data from the disc drive, the other a clock signal derived from the data. The relationship between these two is that each half cycle of the clock signal is a window in which a data pulse must lie. There are two approaches to recovering the original clock signal — analogue and digital. The analogue technique uses a phase-locked loop with a fast lock-up time. This is an effective technique but requires adjustment of components for correct working and a fair amount of circuitry, not the least because the recovered frequency differs between densities and disc size. The digital technique used here requires just one, albeit rather expensive, eight-pin i.c. which extracts the clock signal from all permutations of density and disc size without adjustment. It works by dividing an 8MHz signal to the nominal clock rate — 125kHz for 5in single density up to 500kHz for 3.5in/8in double density — and adding or dropping a divider count to keep incoming data pulses two counts short of the maximum divider count. This roughly phase-locks data pulses to the counter rate, i.e. data pulses definitely fall within a window framed by the state of the most-significant counter bit. The data pulse is not centralized within the window as it would be ideally, but more than adequately meets controller-input specifications.

As hinted earlier, to get more data on a disc requires better and hence more expensive discs and drive heads. In practice the head in particular will not be grossly over-specified. Adjacent flux changes interact. As flux changes become closer together, the effect of this interference becomes more noticeable and transitions appear to be displaced on the disc and hence in time. Fortunately, the sense of the error is predictable, although its magnitude varies from drive type to type, so a correction — write precompensation — can be made before data is written on the disc. The algorithm sensing whether a pulse should be written late, on time or early is implemented in the controller, and the 74LS195 parallel-loading shift register produces a compensation of 250ns, 0 or —250ns, these being values shown to suit most drives. Again, the digital solution is preferred, the write pulse loading a single bit into a shift register being clocked every 250ns. The bit lines come from the controller EARLY and LATE pins and from a gate which derives a NOMINAL signal (logically *not early or late*). At the output of the register a bit appears for one clock period, 250ns, which is either late, 250ns later or 250ns

Table 2. Formatted capacities for single-sided drives.

Disc size	Tracks	Single density	Double density
3.5"	70	140K	350K
3.5"	80	160K	400K
5.25"	35	70K	175K
5.25"	40	80K	200K
5.25"	80	160K	400K
8"	77	250K	616K


IC201 74LS85
IC202 74LS245
IC203 74LS245
IC204 ½74LS139
IC205 74LS273
IC206 74LS273/373
IC207 74LS541
IC208 74LS541
IC209 4093
IC210 74LS195
IC211 MB8877A
IC212 MK3801N-6/4
IC213 74LS393
IC214 SMC9216B
IC215 MC1489
IC216 MC1488
IC217 7406
IC218 74LS02
IC219 7406
IC220 74LS02
IC221 74LS04
Parallel output PL202
Parallel input PL203
Keyboard PL204
RS232 SI/O
PL205
PL206
PL201
VDUSEL
RESET
INT
SIDE 1
SEL 0
SEL 1
WD
STEP
DIRC
HLD
LC
WG
TR0
INDEX
WPRT
RDDATA
READY
CTS
RXD
DTR
TXD
XL201 2.4576 MHz
XL202 8MHz
Link 201
Link 202
Link 203
Echo
Data
Strobe

I/O board specification

Serial i/o

Speed	1 to 38 400 baud, separate receiver and transmitter clocks
Format	synchronous 5-8 bit, auto-search and sync. asynchronous 5-8 bit, 1, 1.5 or 2 stop bits
Control	RTS (ready to send) and CTS (clear to send)
System	RS232C, +12V and −12V levels

Parallel i/o

Input	8-bit port, 1 low-power Schottky t.t.l. load, schmitt buffered.
Output	8-bit port, t.t.l. compatible, 5 t.t.l. loads

Special i/o

3 mos i/o lines operating event counters, pulse timers and Z80 interrupts.

Disc i/o

Output lines can sink 40mA. Input lines terminated with 220Ω to +5V. Bus lines are active low but have the following specification.

Signal	Direction	Function
READY	Input	Implies disc in drive and rotating at correct speed
RDDATA	Input	Raw data consisting of (nominally) 250ns pulses
WPRT	Input	Indicates disc in drive is write protected
INDEX	Input	Pulses once every disc revolution
TR00	Input	Indicates that head is over the outermost track
WG	Output	Enables disc write circuitry
WD	Output	Data to be written to disc
LC	Output	Indicates that the write current should be reduced
HLD	Output	Loads drive head against disc
DIRC	Output	Sets direction of head stepping. Active means step in
STEP	Output	Steps head one track in direction set by DIRC
SEL0	Output	Selects Drive 0
SEL1	Output	Selects Drive 1
SIDE	Output	Selects Side 1

A listing of SC84's machine-code operating system — MCOS — can be obtained by sending an s.a.e. to *Wireless World* SC84, Room L303, Quadrant House, The Quadrant, Sutton, Surrey SM2 5AS. Details of how to obtain other software including the disc operating-system and Basic were given last month together with a source of p.c.bs and newsletter information.

John Adams has recently designed a switch-regulated p.s.u. for SC84 and we hope to publish its design in the near future. He also plans to provide SC84's two eproms ready programmed; for details send an s.a.e. to the author at 5 The Close, Radlett, Herts.

V.D.U. interfacing, memory and control are detailed in the next article following a description of parallel i/o options and keyboard input.

later still, this being an effective method of simulating early, nominal or late write pulses.

Interfacing to the drives is standard in its signals although you will see that the READY line from the drive, generally indicating that there is a disc in the drive and that it is rotating at the required speed, is not taken to the READY input of the controller (which is instead wired permamently active) but to the HLT (head-loaded test) input of the controller i.c. — an input usually driven by a monostable device triggered by the leading edge of the HLD (head load) signal coming from the controller. Part of the algorithm followed by the controller when executing one of its read or write commands is shown in the flow diagrams. One can see that if READY is used conventionally, extra software and hardware must be provided to start up the disc motors (unless they are left continuously running, which will shorten the life of both disc and drive motor) and then wait for the speed to stabilize before attempting to execute a controller command. In this system the drive motor is turned on by the HLD signal, drive connections labelled Head load and Motor on, or the like, being connected together. READY being inactive does not abort the command; the controller simply starts the drive and waits for READY. What of the time delay between sensible data coming from the disc and the missing pause normally inserted by the monostable device to give the head time to load, and is it a good idea to accelerate the disc with the head already loaded against it? Some drives such as the Tandon TM100 do not have a separate head-loading mechanism and those machines that do usually gate READY with the loading signal within drive so the head will not load until the disc is up to speed. Head loading and settling delay and the time taken to get up to speed amount to less than one revolution, and as the controller has to have counted five revolutions before it gives up attempting a command, this system optimizes the delay between a command being issued and its completion while using the barest minimum of hardware and software. As an example, the disc operating system loads and the directory is scanned and noted in just over 1s when using double density.

Some drives do not give a READY signal, if so, leave the READY input to the computer open or wire it to the 5V supply. Also, some drives have optional links on their circuit boards, one of which offers the choice of head loading being solely controlled by the drive-select line or by a combination of drive select and head load inputs. If so, use the latter option. Advice on using different types of drive will be available through the users' group.

Nominal allocation of drives is that there are two drives designated A and B by the disc operating system, dos, hardware selection being by control lines SEL0 and SEL1 respectively. If double-sided drives are used, the reverse side of drive A will be designated C and that of drive B, D. This is nominal as the selection of each logical drive surface can be altered temporarily.* Open-collector drivers are used between the interface and drive. It is important that the total length of the cable does not exceed 3m (less for the 3.5in drives) and preferably as short as possible. Where more than one drive is used, drive-signal connectors are wired in parallel, from the computer to the nearest drive, then from this drive to the next etc. The only exceptions to this are the SEL signals which are individual to each drive although possibly carried by the same cable. You will find that 5.25in and 8in drives contain a pack of resistors usually in a dual-in-line package plugged into an i.c. socket wired to the signal connectors and probably labelled 220/330Ω. These packs must be removed from all but the physically furthest drive from the computer. It is good practice to provide a separate, well-rated, power supply for the drives. Disc drives tend to take large amounts of current when the drive motor starts and when the head loads. This can momentarily overload the supply with devastating results if the computer shares the same power source. Also the ground lead between the drive and interface, which should be substantial, is happier when it only carries signals.

Table 1 gives connections to widely used disc drives. There are many second-hand drives around at the moment; buying such drives is rather like buying a second-hand car — there are bargains but there is also rubbish. In particular, I would advise personal inspection and that you watch out for incomplete drives (large areas of p.c.b. without any components) unless they are a bargain and information on the missing parts is available, worn down head pads (the pad that pushes the disc onto the head) and, at least in the U.K., for drives with 110V and/or 60Hz motors. *Caveat emptor.* I would recommend that you obtain a drive with a distinct head-loading mechanism (usually a solenoid) rather than one that puts the head to the disc as soon as the door of the drive is closed. As to the choice between two single-sided drives and one double-sided one, there are many advantages to using two drives, such as the ease with which back-up copies of discs can be made, reduced head replacement costs and that the computer remains useful when one drive is out of action. Many types of drive — Sony, Canon/BASF, DRE, Shugart and CDC — have been used with the computer and the names given in the table are not intended as an indication of merit. Table 2 gives some typical capacities for drives used in single and double density modes.

**or permanently — Ed.*