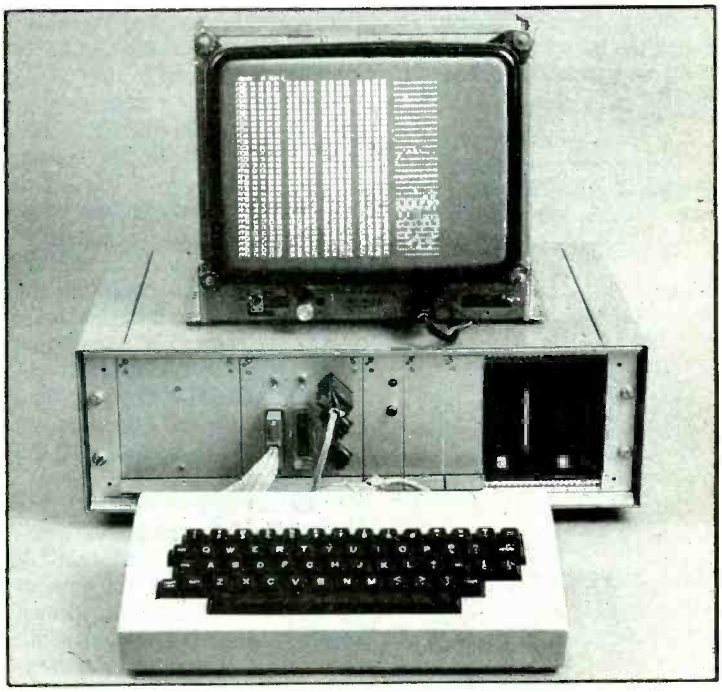
SC84 Micro-computer



These constructor's tips for SC84 — a professional Z80 microcomputer for engineers and enthusiasts described over the past three months — include notes on connecting various disc drives, and MCOS command syntax.

by J.H. Adams M.Sc.

The SC84 microcomputer has been designed as a series of Eurocards plugged into a common backplane and there are many suppliers of frames into which these cards may be fitted. The standard width for such frames is 19in with a capacity, to use the 'Euro measure', of 84E (1E is 0.2in). Vero produce narrower frames, down to 24E. ETL produce basic, but low-cost, 84E frames in plastic. For guidance, you should allow 6 or 7E for the power, v.d.u. and c.p.u. cards and from 12 to 24E for the i/o card, depending upon the number of connectors to be mounted on the front of the unit and assuming that recommended components are used. For a compact system, two 3.5in drives require 20E of space, two 5.25in drives 42E of space. I recommend wire-wrapping sockets together as a means of forming the backplane for the cards but, if the flexibility of wiring is not required — or for initial experimentation — long and short backplane p.c.bs are available from various sources.

To aid construction, a set of three printed-circuit boards and sets of components are available (details at end of article). I recommend use of these p.c.bs as the wiring can be critical — frequencies up to 36MHz being significant — and requires r.f. construction techniques.

With the exception of eproms, i.cs should not be socketed unless high quality sockets (e.g. turned-pin types) are used. By using cheap sockets you will be building in unreliability. In particular, dynamic memory i.cs $IC_{110-117}$ should be soldered in directly. Using sockets makes fault finding easier but may itself be the source of the trouble. General points to note are that 100nF decoupling capacitors should be mounted with as short leads as possible. Even a few extra millimetres of lead can lessen their decoupling efficiency — particularly with those between the dynamic memory i.cs. Crystals on the c.p.u. and i/o p.c.bs stand upright on the board and I recommend that a fillet of silicone rubber (not the acid-based type) is set around their bases to absorb vibration. The crystal on the v.d.u. board can be laid flat, a double-sided adhesive pad being a suitable anchoring device. Note that the crystal and e.p.r.o.m. on the board shown on the May issue front cover differ from those on the production processor board.

Since the processor board was designed, high-speed c.m.o.s. has become widely available and builders of the SC84, particularly those who intend using processors even faster than the Z80B, might like to use a 74HC04 for IC_{123}. The Z80 requires a clock signal which rises rapidly to at least 4.4V — it is not a normal t.t.l. signal. This is achieved in the original circuit by using a low-value pull-up resistor on the output of the 74S04 gate. This resistor, R_{103}, should be left out when using a 74HC04, as the cmos i.c. can more than meet the required signal specification, and R_{101} and R_{102} should be increased to 2.2kΩ. It may be necessary to connect a pull-up resistor to pin five of the 74HC04. The eprom supplied with the mos kit is a 2764. Although only 2Kbytes of the eprom are programmed, an 8Kbyte eprom is supplied to meet Z80B speed requirements. Theoretically, the eprom should be a 200ns device but the standard 250ns one will normally suffice. The philosophy behind this computer is that it is disc-based and as little rom software as possible should be used. Nevertheless, the 2764 gives scope for extra firmware and, as a 27128 may be used without any modifications — and a 27256 or 27512 with just a couple — the computer can easily be changed into a 'silicon system'.

It is only feasible to test individual boards by substitution in a working machine. The only reason for any of the protype units not working was that solder joints had been missed so it is worth inspecting the boards for unsoldered joints or solder bridges between adjacent points. The only shorts which are potentially dangerous are those to the supplies, so it is a good idea to check that supplies on the board only go where they should.

Power supply should be checked with a representative load to make sure that it performs correctly. Suitable loads are 47Ω, 4W resistors for the two 12V supplies and a 2.7Ω, 10W resistor for the +5V supply. It would be galling if a faulty power supply were to destroy working computer boards. To test the system, set

Table 1. Connections from i/o p.c.b. to female D-type connector for serial printer.

i/o p.c.b. pin	25-way D connector
1	7
2	5
3	3
4	2
5	20

SC84's processor, i/o and v.d.u. sections are described in the May, June and July issues of *E&WW* respectively. Addresses and prices for p.c.bs, the SciDOS CP/M compatible disc-operating system, Basic and the SC84 user group have been given. A power supply suitable for SC84 is described in this issue. John Adams, writer and supplier of SC84 software, can supply all parts for the three boards except t.t.l. i.cs, 64-way edge connectors and the disc-drive connector; John Hodson (SC84 User Group founder) can supply all t.t.l. parts and other hardware (excluding cases) at reasonable prices (stocks are limited). Their addresses are 5 The Close, Radlett, Hertfordshire and 12 Broughton Road, Basford, Newcastle-under-Lyme, Staffordshire ST5 0PQ, respectively. John Adams is also offering a repair service for SC84 modules built on p.c.bs from Combe Martin Electronics. Please send an s.a.e. and specify details required.

John Adams' next article describes SC84's machine-code operating system, MCOS.

Adresses of enclosure manufacturers mentioned are ETL Ltd, Unit G, Southhampton airport, Southampton SO2 2HG, and BICC-Vero Electonics Ltd, Unit 5, Industrial Estate, Flanders Rd, Head End, Southampton SO3 3LG.

the preset resistor on the processor board fully clockwise to its minimum, assemble the three boards and power supply, connect a monitor to the v.d.u. card and switch on. If the system works, the display will consist of 32 rows of 96 characters each. The lower 31 lines will consist of random characters and the top lines will be blank except for the word READY and a flashing cursor in the form of an underlining dash. If the screen is stable but there is no READY display, adjust the height control of the monitor, just in case the top line is off the top of the screen.

The display consists of 288 scan lines, each comprising a display period of 48μs, and should fit on a standard monitor without adjustment. If it doesn't, most displays have height and width controls (often on the tube neck) and horizontal shift may be achieved by adjusting the line hold. If the picture is rolling vertically or 'tearing' across the screen and cannot be held steady by adjustment of the hold controls, try altering S_{305} and/or S_{308} respectively as you may not be supplying correct sync. polarity. This should correct any synchronizing problems as the computer produces 625-line-compatible signals (624-line, actually). If the monitor is well out of adjustment it may be necessary to adjust both the vertical (frame) and horizontal (line) hold controls.

If nothing at all happens, try pressing and releasing the system reset button. If the system still doesn't work, check for unsoldered joints or a faulty backplane. Experience has shown that unsoldered joints are the prime cause of failure in these types of boards and that once these are rectified, it is very likely that the system will work first time. Apart from checking for the presence of supplies and short circuits there is little that can be done in the way of fault finding without an oscilloscope with a bandwidth of at least 10MHz.

A fault-finding service is available from me (only for systems built on E&WW p.c.bs) but for readers who can service the boards, first check the various oscillators and the devices they drive. After this, all bus signal should be inspected for signals not falling within the definitions of t.t.l. highs and lows, i.e. below 0.5V or above 2.4V. Note that this refers to signals; there will be periods when the data bus is in its third state and thus floating. Permanently floating lines may indicate an unsoldered joint. Lines sitting at the wrong levels will almost certainly be due to a short-circuit.

Readers who are new to microprocessor servicing should be wary of simple answers based on observations. If you have no screen display it doesn't necessarily mean that the fault is on the v.d.u. board. If the c.p.u. board is not working it will not load the c.r.t. controller with the information it needs to work properly. If the i/o board is faulty it may not be possible to access the v.d.u., access being controlled by a bit in the control port, IC_{205}. Do not waste too much time trying to define the fault from the current state of the system. If you know the system well you may get somewhere but it is more effective to work around the circuit repeatedly, accumulating evidence of simple, localized problems. Also note that low-capacity attenuating probes must be used with the oscilloscope and that what you see on the oscilloscope screen will not really be a true representation of the signals if their frequencies are more than one fifth of the oscilloscope bandwidth. Even then, the rise and fall times of the waves will be altered by the probe and the oscilloscope rise time. These points are not intended to be discouraging, merely to encourage realism. Experience has to be gained somewhere and if you have the time, fault finding is a good way of learning how the system works.

If the computer displays READY and the flashing cursor, the keyboard should be connected to the i/o board and the system switched on again. The keyboard strobe signal must be one that goes high when a key is pressed and stays there until it is released, and the 'echo' line must be connected or grounded. A sign of the strobe being wrong is that random characters will begin to fill the screen. If the echo line is high, only one character may be typed before the system freezes, waiting for the as yet non-existent printer to say that it is ready for an echoed character.

If it is possible to type in characters, press system reset and type LIST followed by a space and then 0000, i.e. the four letters, a space, then the four digits. The computer should now list an area of its memory, starting at address 0000, and then return to the READY state. If this occurs, connect a printer set for 9600 baud, eight-bit word, no parity and one stop-bit. The same listing operation may then be attempted with the echo line switched low. The printer should echo the listing which appears on the v.d.u. Note that the listing may not be as fast, or may pause before the screen is compeltely full as the computer paces the printer and its buffer capacity. Table 1 shows RS232C connections suitable for an Epson printer. These should suit other printers although it may be necessary to activate and/or interconnect other lines. For details refer to the printer manual.

All that remains is to connect the disc drives to the i/o board as described earlier. Many drives offer options. It would be impossible to describe all of the options available as they are different for each drive both in quantity and nature. Some drives (Canon, BASF) use jumpers to link pairs of pins, some (old DRE) use wire links that look like unmarked resistors. SC84 assumes what are generally the default settings of these links. The exception worth investigating is that most drives offer the option of loading the drive head whenever the drive is selected, or only when it is selected and another input line called Head Load, Radial Load or Option is active. Where possible, the second option should be used as although the system would work in the default mode, discs and the drive heads will last longer if the heads are loaded separately.

Some drives do not have a READY output, in which case wire the computer's READY input low. When using second-hand drives it is necessary to check the options with greater care as they may already have been altered for their original application. In particular, some 8in drives have an option link connected so that they use the two head-positioning control lines as 'step in' and 'step out' rather than as 'step' and 'direction'.

Many types of drive, new and second-hand, have been used with SC84 and with the Scientific Computer and the same problems have been faced and overcome due to the interface's inherent flexibility. Option details for various drives already used with SC84 appear in the users' group newsletter.

When more than one disc drive is used, the control cables are fed to one drive and then on to the next, all control and ground lines being wired in parallel. The drive will have some means of setting which drive-select signal it responds to. Once again, this varies from drive to drive but usually consists of an option area which connects one of the drive select pins on the drive interface connector to the drive electronics. Exceptions are Sony D31 and D32 drives where a four position slide switch does the selection. To use two drives set one switch to position two and the other to position three. A feature found on most drives (not Sony) is a pack of terminating resistors connected to the drive control lines. When more than one drive is to be used these resistor packs — usually in the form of a dil package — must be removed from all but the drive at the end of the interface cable.

When initially testing the disc drive(s) it is advisable to have the mechanism fully exposed so that its action can be observed. Apply power to the drive and computer. Set the switches on the i/o board for the type and density of disc used, insert a write-protected* SciDOS system disc in the drive selected by select-line one and type control S or control D (i.e. type S or D while holding down the key marked control or CTRL), depending on whether the disc is single or double density. Except for drives with mains motors — which should already be running — the drive motor should start. The head carriage in the drive should retract to the outermost position on the disc and the head should be loaded against the disc. In the mean time the computer will have cleared the display and should then load SciDOS from the disc and display '3.5in DOUBLE DENSITY DISC SYSTEM — Version 1.0A' or something similar on the top line of the v.d.u., followed by an 'A>' prompt. After about a second, the drive head is lifted from the disc and the drive stopped. If so, type the three letters DIR followed by the return key.

If the drive motors are running or the head is loaded before you type control S or D, press reset and try again. If you can, switch off the drive power and manually wind the head carriage towards the centre of the disc. This is quite simple with 8 and 5.25in drives and will ensure that you can observe any head motion. Apply power again, press reset and retype control D or S. If the head carriage doesn't move out as described earlier you may not be selecting the drive, either through an interface-wiring or option-selecting error. To force drive select, connect only one drive to the computer, temporarily ground all of its drive-select pins and repeat the operation. This will not harm the interface circuit as all its lines are open-collector types. With the drive forcibly selected thus, pressing system reset should make the head carriage move a short distance towards the outermost position, even if nothing else works. If not you should completely recheck the interface wiring for faults.

Use an oscilloscope to check that there is a short negative-going pulse on pin 19 of IC_{211} when system reset is pressed and released. If there isn't, trace this line to backplane line 16a. If the pulse is there, check IC_{211}, pin 21 for +5V, pin 24 for a 1 or 2MHz clock (depending upon the density, single or double, respectively) and then pin 15 and drive interface line 20 for up to 256 short pulses (positive going at the i.c., negative going on the interface) whenever system reset is operated. These pulses are part of IC_{211}'s reset procedure and should make the head of the selected drive step outward. The presence or absence of these pulses will give some guidance as to whether it is the i/o board, the interface cable or the drives which are not responding.

Once the disc reading function of the interface is confirmed by loading SciDOS, test disc writing by running the format program. To be on the safe side, when the program asks you on which drive code you want to format take out the system disc, even if it isn't the drive you intend using for the formatting operation, and insert a non write-protected blank disc in one of the drives then continue with the formatting operation (for fuller details, refer to the manual supplied with SciDOS). Once formatting is complete, press reset and type the three letters NEW followed by a space. This wipes the computer memory so that there is no chance of an undiscovered system bug reactivating the format program — which would otherwise still be in memory. Insert your system disc, load SciDOS as before, replace the system disc with the one you have just formatted and type the three letters DIR followed by the return key. If the message NOT FOUND appears within a second or two all is well as the system is reporting that it can read the disc directory but there is nothing in it — as one would expect with a newly formatted disc. If, after several seconds, a message beginning 'BDOS error' appears, you have a writing fault. To simulate the error message, try the DIR operation on an unformatted disc. Once you have a formatted disc, use the

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MCOS operating syntax.

LIST <start address> lists 496 bytes of memory in hexadecimal form and in ascii starting from <start address>. Line format during list comprises the starting address of that line's code then the hexadecimal values of the contents of 16 consecutive memory locations starting at that address. At the end of the line the ascii representation of the 16 bytes is given, any bytes not in the normal ascii range (020 to 07E) being display as a period.

LOAD <start address> loads hexadecimal data into memory, starting at the specified address. LOAD formats the input code in the same way as that used during the LIST operation. If a mistake is made in entering a byte, the error may be corrected by completing the byte and then pressing DEL or DELETE. This decrements the memory pointer by one for each press as well as backspacing the cursor position to the peviously input data. Deletions attempting to place the cursor on a previous line of loaded code are processed by repeating that line's format on the current v.d.u. line. To exit from a LOAD, press the space bar.

ALT <address> <byte> alters the location specified to the given byte. After doing this it relists the memory area last listed. As you will have probably listed the area you are to alter before using ALT, the effect of this will be to re-display the same area with the alteration made. ALT re-enters itself to let you continue alterations. To terminate the ALT command use the soft reset or type any non-hexadecimal character — in which case MCOS will exit ALT and use this letter as the first of the next command.

FIND <bytes> searches the memory for the string of hex. bytes entered in the command line and lists the starting address of each occurrence. The maximum number of bytes is approximately 80, the string being terminated by pressing the ESC (or Control [) key.

MOD <start address> <end address> <to> <from> changes all occurrences of the byte <from> to the byte <to> over the memory range <start address> to <end address> — 1.

FILL <address> fills memory from <address> to the end of the page in which <address> falls with the byte 0FF (a page being 256 locations sharing the same higher order address byte, e.g. 08900 to 089FF). FILL is usually used in clearing areas of memory to make code you are using stand out when listed or to prepare areas of memory which are not to be altered when you are preparing to partially program an eprom (programming 0FF into an eprom location has no effect upon that location).

NEW is an extension of FILL which fills the memory from address 00000 up to 0F7FF with byte 0FF and then rewrites the RST information. Used for similar purposes to FILL.

COMP <address 1> <address 2> compares on a byte-by-byte basis the two blocks of code starting at <address 1> and <address 2>. If any pair is found to differ, the address of the byte in block 1 is displayed. This command is terminated by a soft reset.

MOV <start address> <end address> <destination address> copies the block of code from <start address> up to <end address> — 1 to the area of memory starting with <destination address>. Care must be taken in using MOV when the destination is within the block to be moved as this will result in replication rather than a clean block move as code is moved, moved again, moved again and so on. In fact this can be quite useful for creating large blocks of the same n bytes. If you need to move a block backwards, for example to insert an extra instruction, use BACK.

BACK <start address> <end address> <count byte> moves the block of code <start address> to <end address> — 1 back <count byte> locations. A count of 00 corresponds to a move back of 256 locations which is the maximum possible in one BACK command.

RUN <start address> begins execution at <start address>.

Press CTRL @ for soft reset.

Some readers have run into problems through using the wrong dynamic rams. These i.cs must be those specified on page 39 of the May issue. If in doubt, contact the author (address on previous page).

*Notch in the disc envelope covered for 5.25in, uncovered for 8in and window open on 3.5in discs.

wider below the full recording level, it should not be exceeded.

There is no need for a VU or other level meter; once the output level from the f.s.k. modulator and the input level to the record amplifier have been set they do not need to be readjusted. In fact, one or other of the level controls can be removed. I suggest that the 10kΩ level control of the record amplifier be replaced with a fixed 10kΩ resistor. The input sensitivity of the record amplifier is about 50mV r.m.s., for a full recording level output of 2.25V r.m.s., at 660Hz, from IC_2. At higher frequencies the sensitivity will be even greater due to the high-frequency pre-emphasis circuit.

The record/playback electronics will operate very well with the record/playback and erase heads supplied with the solenoid-operated cassette deck. However, to get the best high-frequency response out of the system, it is recommended that the HS16 stereo record/play head is bought for use with the deck instead of that supplied. (No equivalent mono head as good as the HS16 is as yet available.) Stereo record/playback circuitry is, of course, not required in this application. There is, however, a good reason for recording the f.s.k. signals onto both halves of the tape. Both halves of the stereo head may be readily driven from the single output of IC_2 — simply provide an additional 1µF capacitor and 39kΩ resistor in series with the other half of the head. It is *not* recommended that the two halves of the stereo head should be paralleled for playback. Rather it should be possible to select which half is used for playback. The precise way by which this may be done is left to the constructor. If this technique is adopted, two recordings will always be made of the microcomputer programs or data. If one half is not recorded entirely correctly, there is a good chance that the other half will be.

To set the record/playback electronics to a satisfactory condition for recording the f.s.k. signals, three controls need to be adjusted. They are the signal level input, the magnitude of the high-frequency pre-emphasis (470Ω pre-set), and the bias level (100kΩ pre-set). To do this an a.c. voltmeter with a frequency response up to that of the bias oscillator's frequency is needed. Firstly, the bias voltage on the record head should be adjusted to about 7V r.m.s. measured across the record head with a suitable low-capacitance h.f. probe. With the value of the 470Ω resistor adjusted for maximum resistance, adjust the input signal level from the f.s.k. modulator (at the higher frequency) for an output of 2.25V r.m.s. measured at the output of IC_2.

Applying logic 0 and 1 levels at the input of the modulator, record the resulting audio signals for a time sufficient for a subsequent analysis of the recorded signals. Rewind and replay the recorded signals. The amplitude of the replayed signals should be around 400mVs r.m.s. and there should be no significant difference in the amplitude of the two frequencies. If the amplitude of the higher frequency is more than 3dB below that of the lower frequency, repeat the recording process having first adjusted the 470Ω preset for a lower value of resistance. It should be possible to arrive at a setting that produces very little difference between the amplitudes of the two frequency signals.

If a large difference between the amplitude of the two frequency signals still exists after attempts at adjusting the preset, it may be worth altering the bias voltage setting, remembering that the higher the bias voltage, the greater the attentuation effect upon the higher frequency. When the best possible settings are found, do try the replayed signals on the demodulator; it is very non-critical of amplitude and amplitude differences.

To be continued

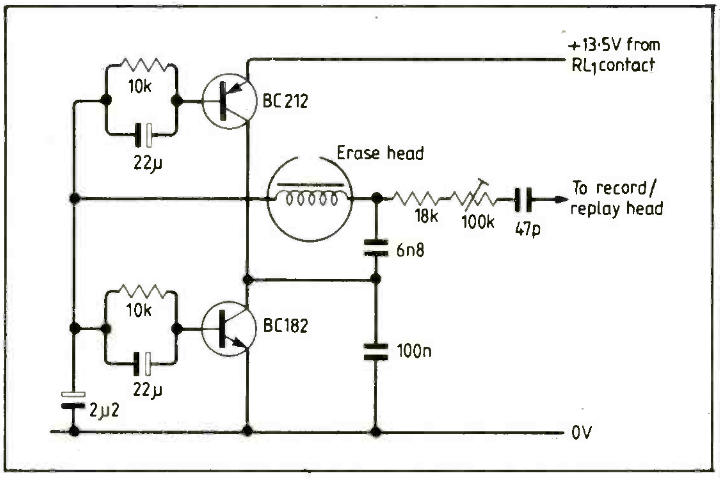

Fig.11. **Bias and erase oscillator.**

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COPY program to create a working copy of your master disc and then file the latter for safe keeping.

There are two preset adjustments in the computer, neither of which is critical. The potentiometer on the processor board adjusts the length of the RAS pulse applied to dynamic memory. By adjusting this potentiometer it is possible to use relatively low-speed dynamic memories in a high-speed system. With the high-speed memories supplied in the kits, the potentiometer can be set to its minimum. The trimming capacitor on the v.d.u. board, C_{301}, allows the crystal frequency to be trimmed to an exact value. The purpose of this is to allow the frame frequency generated by the c.r.t. controller to be set to exactly 50Hz.

Back in 1932, Baron von Ardenne was experimenting with variable-speed scanning tv. The theory was that if the scanning beam could travel slowly over the light areas of the subject and quickly over the dark, there would be no need to modulate the intensity of the beam. His experimental equipment used as a telecine to transmit films is shown in these pictures which are examples from the many historical photos held in the *E&WW* archives. These are available to outside users at a very moderate fee. Details from Quadrant Picture Library, Quadrant House, Sutton, Surrey. Telephone: 01-661 3427.