Half-megabyte memory for SC84

by J.H. Adams, M.Sc.

'Silicon disc' using 256K dynamic memory chips has novel refresh system.

I use a microcomputer primarily as a means of developing software and of writing long documents, such as this article. My SC84 computer gives better performance than many other computers but the discs don't go round any faster than anyone else's. When working back and forth between the ends of large files with Wordstar or when performing a major assembly, disc operations take a lot of time.

The reason for this is clear when one watches the process. In both cases the computer is operating with more than one file. In word processing, the computer memory acts as a 'window' into the file. As this window moves up and down a file larger than the free memory available in the computer, temporary files are created to store the data ahead of and behind the window.

In program development, assembly means getting data from the source file and sending data into object and listing files. Switching between the files takes time as the drive head has to traverse the disc surface many times. There's wear and tear on the drive and the computer operator, both of which can be eliminated by the use of what has become known as a 'silicon disc'.

Silicon disc is a large memory used either as a buffer into which the working disc's contents are loaded or, as in this case, treated as a pseudo disc. The system described consists of a 512Kbyte memory, accessed as one of 256 2Kbyte 'pages'.

Pages are selected by writing an 8bit value into a register on the silicon disc unit. This is rather like writing to the track-number register of a floppy disc controller. Once selected, the page may be accessed directly or by 'mapping'. In mapping, a block of memory can be made to substitute itself for an equivalent block of system memory. SC84, as with any other good computer design, has a mapping facility. The advantage of mapping is that areas of system memory are not permanently committed to transient facilities (the v.d.u. in SC84 is a good example of this). One must choose the mapping area carefully though as it is obviously not possible for code executing in the area of system memory to be mapped out to access the mapped area. For this reason, switches allow the unit to be permanently allocated or to be mapped to any 2Kbyte block within an 18bit address range. The silicon disc is seen as an adjunct to the disc operating system and so, for SC84, the mapping is over the section of memory even more fundamental than Scidos itself, the resident operating system Mcos.

The half-megabyte memory is in the form of 16 256Kbit dynamic memories, although the unit can be built with only half of this capacity. Thought has been given to making the silicon disc as versatile as possible. As such it relies on only two system signals; one indicates that a memory cycle is taking place and the other that a read operation is occuring. In a Z80 system these would be MREQ and RD; in an 8086 system they would be a combination of ALE and IO/M and the RD signal.

Note that no reference is made to external refreshing. The RFSH input shown on the circuit diagram is offered as a means of reducing unnecessary power consumption in Z80 systems. Refreshing of the memory is achieved by a combination of some rather clever facilities provided in the memories specified and the way in which the silicon disc is used.

An explanation of the design philosophy behind multiplexed-address dynamic memory was given in my recent series on the SC84 computer*. Suffice to say that in addressing dynamic memories, the address of the locations to be accessed is latched into the memory in two parts — a row address and a column address. This saves pins and thus cost on a 256Kbit device which otherwise would need 18 address pins. It also allows refreshing of the entire memory by regular access-

* SC84 is a 4/6MHz Z80-based computer running the Scidos operating system for CP/M software, described in the May, June, July, September and October 1984 issues. The three-Eurocard circuit board set for this project is still available.

Specification and performance

Memory capacity is 512Kbyte organised as 256 'tracks' of 2Kbyte each and power requirement is +5V at up to 0.5A, depending on the system cycle rate.

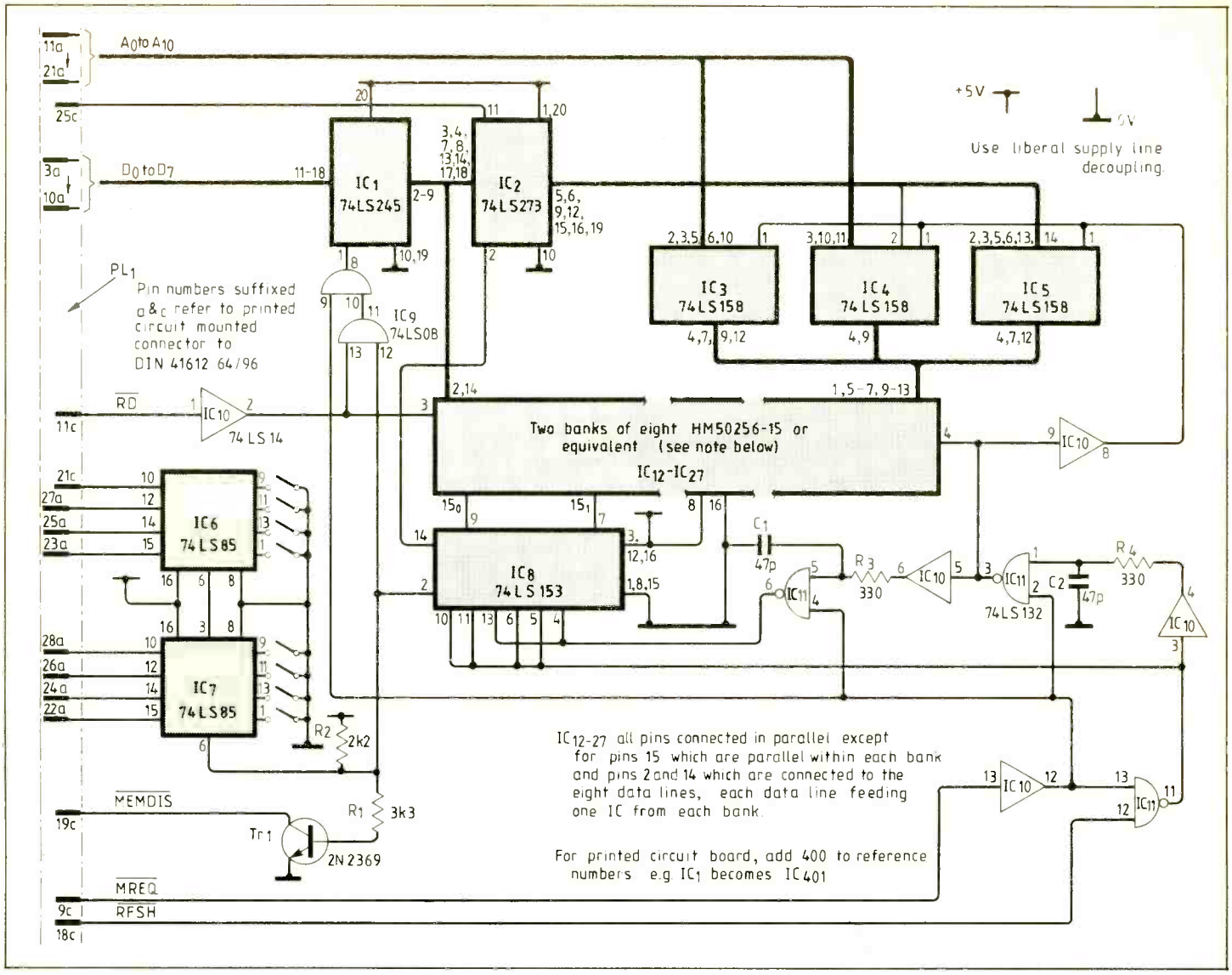
To test the performance of the 'silicon disc' compared with a conventional system, I used Wordstar to edit a 120Kbyte source file. The procedure was to perform a global alteration through the file, to save the file using ↑KS to move to the end of the file using ↑QC and then to move back to the start using ↑QR.

Timings for these operations on SC84 with and without the silcon disc and for a DEC Rainbow are shown in the table. As shown over extra time taken depends very much on the distance moved by the drive head during the magnetic disc tests, the SC84 and DEC tests were carried out under optimum conditions, i.e. with only the source file on the disc.

The fourth column in the table indicates how long a computer would take with a typically full disc. During the alteration, screen update was suppressed by pressing ESC as otherwise the test would have reflected the speed of screen update rather than of disc access — a factor which would have considerably increased the DEC timing.

The final test was to assemble a 20Kbyte Z80 source file to produce an intermediate file which would result in approximately 2Kbyte of object code, and a listing file. The assembler used was M80.

These tests are reasonably representative of typical uses of the silicon disc. Other advantages, particularly noticeable when using Wordstar, are that messages and overlays load and present themselves instantly and noiselessly.



Half-megabyte memory expansion circuit. Pins 15 of the three LS158 multiplexers are connected to ground.

Kits and p.c.bs

Memory board kits excluding p.c.b. are £92 inclusive from John Adams at 5 The Close, Radlett, Hertfordshire WD7 8HA. This price is £93 for readers in other parts of Europe and £94.50 for those outside.

Plated-through-hole p.c.bs for this project are £16 including UK or overseas postage from Combe Martin Electronics, Kings Street, Combe Martin, North Devon EX34 0AD.

ing of all rows.

The Z80 has an inbuilt refresh generator consisting of a control line and a seven-bit counter which is regularly incremented and output during a period when the Z80 doesn't need the external bus. While memories were addressed seven bits by seven bits (16Kbits) this was acceptable. When 64Kbit devices appeared, most were made to be actually seven bits by nine internally, although addressed as eight bits followed by another eight. This meant that a Z80 could still refresh these devices but it did make the i.cs more difficult to fabricate.

Some device manufacturers attempted to make their 64Kbit chips more versatile by building an equivalent of the Z80 refresh generator, but with 8 bits, into their dynamic memories and providing a pin to implement the refreshing process. This was a good idea as it allowed other refreshing techniques such as standby refreshing to be implemented but it took away a much needed pin. When 256Kbit i.cs were designed, this pin went to provide the ninth address line but in certain devices the internal refreshing mechanism has survived.

As mentioned, the address is latched into the memory in two parts by means of a negative transition on one of two control lines, row-address strobe RAS and column-address strobe CAS. The standard operating sequence for a dynamic memory of this type would be as follows. Begin with both RAS and CAS high, apply the row address, switch RAS low, apply the column address, switch CAS low. After this a read, write, or read-then-write operation may take place on the addressed bit, depending upon the WR control line. Strobe RAS may be taken high again a short period after CAS has gone low and, as a variation, CAS may then be repeatedly pulsed to latch in the addresses of, and therefore access, other bits within the same row.

What never happens in a conventional addressing situation, and what is exploited in the devices under review, is that RAS should go low while CAS is low. My words are carefully chosen as the data sheets for most 64Kbit devices do show a mode called 'hidden refresh', where after CAS has gone low and data is being accessed (RAS goes high), the address of a row to be refreshed is applied and RAS goes low, forcing a form of refresh. The differ-

Test	Silicon disc	SC84	DEC rainbow	SC84 typical
Alteration	43	170	179	182
KS	2	18	17	22
QR	12	47	62	160
Assembly	22	110	102	115

Continued on page 93

Communications receivers

Some additions to last month's survey

Philips have launched two multi-band synthesized portables, each covering 150kHz-30MHz plus the f.m. broadcast band.

The D2935 (£170), styled as a portable, is a double-superhet with a liquid-crystal display, key-pad frequency selection giving storage for up to nine stations, a b.f.o. for s.s.b. or c.w. reception and an r.f. gain control. It can run on mains or battery power and it weighs 2.45kg.

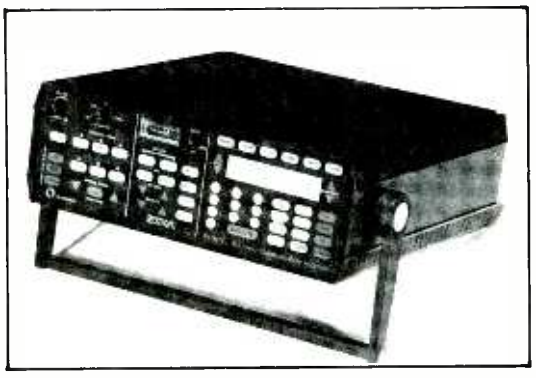
Among the additional features offered by the D2999 (£300) are three-speed electronic tuning using a knob as an alternative to the keypad, a digital field-strength meter, seven more memories, a search-tuning facility and a switchable dual loudspeaker system. This model, which is described as a transportable, weighs 4.11kg.

The Danish manufacturer **Eska** is returning to the market after a reorganization, and among the h.f. products announced by the company is the RX99PL transportable receiver.

Frequency coverage is 15kHz to 29.999MHz plus a.v.h.f. range of 144-176MHz and an unusually wide f.m. broadcast band of 60-109.9MHz. Modes available are s.s.b., f.m. (broad and narrow-band), radio-teleprinter, a.m. and phase-locked a.m., with true passband tuning. This versatile set has a two-line, 20-character alpha-numeric l.c.d. read-out, 99 memory channels, scanning, four independently-selectable a.g.c. time constants and nine receiver bandwidths ranging from 500Hz to 240kHz. Remote control and data transfer are possible via a passive 20mA current loop.

Also from Eska is a modification kit for the JRC NRD-515 receiver pictured last month. The kit includes extra filters to improve the set's selectivity and is claimed to increase the signal-to-noise ratio by 10dB. It also provides a phase-locked a.m. detector for distortion-free reception of a.m. stations even during severe fading and interference. Eska Communications Systems A/S, Frederikssundsvej 274D, DK2700 Brønshøj, Denmark.

The D2935 from Philips



Eska's RX99 PL receiver

From page 36

ence here is that in the newer devices there is no onus on the system to provide the refresh address.

This 'CAS-before-RAS' signal mechanism — just one of the advances being made in dynamic memory development — requires the slightly more complex RAS signal.

To keep the system simple, no code is executed within the silicon disc memory; it is purely a store into which and from which data is transferred. This means that access to it will always be interleaved with access to other areas of memory.

The timing controller generating RAS and CAS for the silicon disc produces conventional memory cycles when the disc is actually being accessed. It generates CAS-before-RAS cycles whenever accesses at other addresses occur or when the silicon disc is mapped out of the system. Thus refreshing is guaranteed while the microprocessor runs and yet minimal control signals are required.

Component IC_1 buffers the data bus to and from the host system. It is permanently active and normally faces off the system bus toward the silicon disc. Page selecting latch IC_2 is treated as an i/o port clocked by an external signal which, in the case of the SC84, comes from the i/o board through pin c25. The lower seven bits stored in this latch combine with the lower 11 bus address lines to form inputs to a nine channel two - input multiplexer, IC_{3-5}, providing row and column addresses to the dynamic memory array.

It doesn't matter which address lines are paired up, or which multiplexer outputs go to which dynamic memory address inputs. Upper system address lines A_{11} to A_{17} go into an eight-bit comparator formed from $IC_{6,7}$ which gives an active output when the address matches the switch settings and the SDSEL line is active. This line is the signal which maps the silicon disc into memory and may be selected to be active high or low by switch S_8. Output of the comparator is used to gate the inverted RD signal into the dynamic memory W pins.

In SC84 an inverted read signal rather than the conventional write one was used as the write strobe to the memories. The advantage of this is that an 'early write' is always generated. This type of write cycle is particularly useful in that the write operation for these dynamic memories can take two forms, dependent on the state of the W line when CAS goes low.

Most microprocessors still have their write signals high at the point when CAS goes low, so a conventional cycle is generated where the memory outputs the present state of the bit, i.e. the cycle begins as a read one. By setting W low before CAS goes low an 'early write' cycle occurs in which the output pin of the memory stays in a high impedance state throughout the cycle. This allows the data input and output pins on the memory to be connected together without any fears of bus contention — an arrangement which suits the bidirectional system data bus.

The main control signal indicating a memory cycle passes through buffering and a series of time delays to produce a slightly delayed version for the RAS signal. A further delayed version switches the address-line multiplexer and a yet further delayed one acts as the conventional CAS. Note that these signals are all gated with the original one so that all signals go to their inactive state promptly at the end of the memory cycle.

The memory control signal also feeds forward, bypassing the delay chain. This is the early version of CAS, made available for the 'CAS-before-RAS' refresh cycles mentioned earlier. Selection of the CAS type takes place in a dual 4-to-1-line multiplexer, IC_8. Here the comparator output and the higher order bit from the page register combine to select which type of CAS, early or conventional, is passed to which 256Kbyte memory block.

In using a silicon disc, one rule must be adhered to. Remember that the 'disc' is silicon and not magnetic and so should the power fail you will lose all of the data. The rule is to regularly make back-up copies of any master files on magnetic disc.

A version of the SC84 operating system, version 2.1D, is available which treats the silicon disc as drive E. For readers patching their own CP/M Bios, a DPB exists. The DPB sets the number of sectors per track as 16 (sixteen 128 byte sectors yields the 2Kbyte of page/track) and zero offset, i.e. no tracks reserved for system use as you would never boot the system from a silicon disc! Other parameters are by choice, although the system uses a block and 16 checked directory entries.