Noritake itron

VACUUM FLUORESCENT DISPLAY

MODULE

SPECIFICATION

MODEL :CU20029ECPB-W1J

SPECIFICATION NO. DS-758-0000-03

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1. General Description

1.1 Application:

Readout of computer, micro-computer, communication terminal and automated instruments.

1.2 Construction:

Single board display module consists of 40 characters (2 x 20) VFD, one chip controller driver which has character generator ROM and RAM, and DC/DC converter.

1.3 Scope

Interface level is TTL-8/4 bit parallel and the module can be connected to the CPU bus directly. +5V single power supply is required.

2. Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Power Supply Voltage	V_{CC}	0	—	5.5	V_{DC}	—
Logic Input Voltage	V_I	0	—	V_{CC}	V_{DC}	—

3. Electrical Ratings

Conditions:Ta=25℃

Parameter		Symbol	Min.	Typ.	Max.	Unit	Condition
Logic Input Voltage	"H"	V_{IH}	2.0	—	V_{CC}	V_{DC}	V_{CC}=5.0V
	"L"	V_{IL}	0	—	0.8		
Reset Input Voltage	"H"	VRH	3.75	—	V_{CC}	V_{DC}	V_{CC}=5.0V
	"L"	VRL	0	—	0.8		
Power Supply Voltage		V_{CC}	4.75	5.00	5.25	V_{DC}	—

4. Electrical Characteristics

Conditions:Ta=25℃,VCC=5.0V

Parameter		Symbol	Min.	Typ.	Max.	Unit	Condition
Logic Output Voltage	"H"	V_{OH}	V_{CC}－0.4	—	—	V_{DC}	I_{OH}=－1.60mA
	"L"	V_{OL}	—	—	0.4		I_{OL}=1.60mA
Power Supply Current 1		I_{CC}1	—	0.4	0.6	A	Display ON
Power Supply Current 2		I_{CC}2	—	2	10	mA	Display OFF

Note : ICC shows the current, when all dots are turned on.

Slow rise up power supply may cause a failure of Power-on reset which is explained in "8.2

Power-on reset". Less than 50ms power rising time is recommended.

After V_{CC} rise at 4.75V, it takes more than 100ms for Power-on reset.

ICC might be anticipated twice as usual at power on rush.

5. Optical Characteristics

Number of Characters	: 40 (2 lines x 20 chars)
Matrix format	: 5 x 8 dots
Display area	: 102.6 x 18.8 mm (X × Y)
Character size	: 3.8 x 9.2 mm (X × Y)
Character pitch	: 5.2 mm
Line pitch	: 9.6 mm
Dot size	: 0.6 x 0.975 mm (X × Y)
Dot pitch	: 0.8 x 1.175 mm (X × Y)
Luminance	: 350 cd/m^2 (100fL) Min.
Color of illumination	: Blue-Green

6. Environmental Conditions

Operating temperature	: -40 to +85℃
Storage temperature	: -50 to +85℃
Operating humidity	: 20 to 80 R.H (Non condensation)
Vibration (Non operating)	: 10 to 55 to10 Hz (Frequency), 1.0mm (Total Amplitude) 30 min. (During) X,Y,Z each direction
Shock	: 539 m/s^2 , 10ms

7. Function Descriptions

7.1 Instruction table

Instruction	CODE										Cycle Time	Description
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Display Clear	0	0	0	0	0	0	0	0	0	1	2.3ms Max.	Clears all display and sets DD RAM address 0 in the address counter.
Cursor Home	0	0	0	0	0	0	0	0	1	*	1*tCYC	Sets DD RAM address 0 in the address counter. Also returns the display being shifted to the original position. DD RAM contents remain unchanged.
Entry Mode set	0	0	0	0	0	0	0	1	I/D	S	1*tCYC	Sets the cursor direction and specifies display shift. These operations are performed during writing/reading data.
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	1*tCYC	Sets all display ON/OFF(D),cursor ON/OFF(C),cursor blink of character position(B).
Cursor or Display shift	0	0	0	0	0	1	S/C	R/L	*	*	1*tCYC (2*tCYC)	Shifts display or cursor, keeping DD RAM contents.
Function Set	0	0	0	0	1	IF	*	*	*	*	1*tCYC	Sets data length(IF).
Brightness control	1	0	*	*	*	*	*	*	BR1	BR0	1*tCYC	Accepts 1 byte data of just after “Function set” as brightness control data.
CG RAM address setting	0	0	0	1	ACG						1*tCYC (2*tCYC)	Sets the CG RAM address
DD RAM address setting	0	0	1	ADD							1*tCYC (2*tCYC)	Sets the DD RAM address
Busy flag & address reading	0	1	BF	ACC							1*tCYC	Reads busy flag(BF) and address counter.
Data writing to CG or DD RAM	1	0	Data writing								1*tCYC	Writes data into CG RAM or DD RAM.
Data reading from CG or DD RAM	1	1	Data reading								1*tCYC	Reads data from CG RAM or DD RAM.
			I/D =1:Incriment I/D =0:Decriment S =1:Display shift enabled S =0:Cursor shift enabled S/C =1:Display shift S/C =0:Cursor move R/L =1:Shift to the right R/L =0:Shift to the left				IF =1: 8-bits IF =0: 4-bits BF =1: Busy BF =0: Not busy BR1,BR0 = 00:100% 01:75% 10:50% 11:25%					DD RAM: Display Data RAM CG RAM: Character Generator RAM ACG:CG RAM address ADD:DD RAM address ACC: Address Counter

Note * :don’t care

tCYC :tCYC is read/write cycle (Min.1 μ s) of HOST SYSTEM.

() :IF RAM read is a next operation, needs execution time indicated by “()”.

7.2 Display clear

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	0	0	1	01H

RS=0

This instruction
1. Files all locations in the display data (DD) RAM with 20H (Blank character).
2. Clears the contents of the address counter to 0H.
3. Sets the display for zero character shift.
4. Sets the address counter to point to the DD RAM.
5. If the cursor is displayed, moves the cursor to the left most character in the top line (line1).
6. Sets the address counter to increment on each access of DD RAM or CG RAM.

7.3 Cursor Home

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	0	1	*	02H to 03H

RS=0 *:don't care

This instruction
1. Clears the contents of the address counter to 0H.
2. Sets the address counter to point to the DD RAM.
3. Sets the display for zero character shift.
4. If the cursor is displayed, moves the most character in the top line (line1).

7.4 Entry Mode Set

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	1	I/D	S	04H to 07H

RS=0

The I/D bit selects the way in which the contents of the address counter are modified after every access to DDRAM or CGRAM.

I/D=1:The address counter is incremented.
I/D=0:The address counter is decremented.

The S bit enables display shift, instead of cursor shift, after each write or read to the DDRAM.

S=1:Display shift enabled.
S=0:Cursor shift enabled.

The direction in which the display is shifted is opposite in sense to that of the cursor.
For example if S=0 and I/D=1, the cursor would shift one character to the right after a CPU writes to DD RAM. However if S=1 and I/D=1,the display would shift one character to the left and the cursor would maintain its position on the panel.

The cursor will already be shifted in the direction selected by I/D during reads of the DD RAM, irrespective of the value of S. Similarly reading and writing the CG RAM always shifts the cursor. Also both lines are shifted simultaneously.

Cursor move and display shift by the “Entry Mode Set”.

I/D	S	After writing DD RAM data	After reading DD RAM data
0	0	The cursor moves one character to the left.	The cursor moves one character to the left.
1	0	The cursor moves one character to the right.	The cursor moves one character to the right.
0	1	The display shifts one character to the right without cursor’s move.	The cursor moves one character to the left.
1	1	The display shifts one character to the left without cursor’s move.	The cursor moves one character to the right.

7.5 Display ON/OFF

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	1	D	C	B	08H to 0FH

RS=0

This instruction controls various features of the display.
The D bit turns the entire display on or off.

D=1:Display on
D=0:Display off

Note : When display is turned off, power converter also inhibited and reduce a power Consumption

The C bit turns the cursor on or off.

C=1:Cursor on
C=0:Cursor off

The B bit enables blinking of the character the cursor coincides with.

B=1:Blinking on
B=0:Blinking off

Blinking is achieved by alternating between a normal and all on display of a character.
The cursor blinks with a frequency of about 1.1 Hz and DUTY 50%.

7.6 Cursor/Display Shift

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	1	S/C	R/L	*	*	10H to 1FH
RS=0								*:don't care

This instruction shifts the display and/or moves the cursor, on character to the left or right, without reading nor writing DD RAM.
The S/C bit selects movement of cursor or movement of both the cursor and the display.

S/C=1:Shift both cursor and display.
S/C=0:Shift cursor only.

The R/L bit selects left ward or right ward movement of the display and/or cursor.

R/L=1:Shift one character right.
R/L=0:Shift one character left.

Cursor moves and Display shift by the "Cursor/Display Shift"

S/C	R/L	Cursor Shift	Display Shift
0	0	Move one character to the left	No shift
0	1	Move one character to the right	No Shift
1	0	Shift one character to left with display	Shift one character to the left
1	1	Shift one character to right with display	Shift one character to the right

7.7 Function Set

This command sets width of data bus line by itself, and sets screen brightness by following one byte data.

7.7.1 Function Set Command

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	1	IF	*	*	*	*	20H to 3FH
RS=0								*:don't care

This instruction initializes the system, and must be the first instruction executed after power-on.
The IF bit selects between an 8-bit or a 4-bit bus width interface.

IF=1:8-bit CPU interface using DB7 to DB0
IF=0:4-bit CPU interface using DB7 to DB4

7.7.2 Brightness Control

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
*	*	*	*	*	*	BR1	BR0	00H to 03H
RS=1								*:don't care

One byte data (RS=1) which follows the "Function Set Command" is considered as brightness data. When a command (RS=0) is written after the "Function Set Command", the brightness control function is not initiated. Screen brightness is as follows;

BR1	BR0	Brightness
0	0	100%(Default)
0	1	75%
1	0	50%
1	1	25%

7.8 Set CG RAM Address

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	1	ACG						40H to 7FH
RS=0								

This instruction
1. Loads a new 6-bit address into the address counter.
2. Sets the address counter to address CG RAM.

Once "Set CG RAM Address" has been executed, the contents of the address counter will be automatically modified after every access of CG RAM, as determined by the "7.4 Entry Mode Set" Instruction. The active width of the address counter, when it is addressing CG RAM, is 6-bits so the counter will wrap around to 00H from 3FH if more than 64 bytes of data are written to CG RAM.

7.9 Set DD RAM Address

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
1	ADD							80H to A7H(1 line)
RS=0								C0H to E7H (2lines)

This instruction
1. Loads a new 7-bit address into the address counter.
2. Sets the address counter to point to the DD RAM.

Once the "Set DD RAM Address" instruction has been executed, the contents of the address counter will be automatically modified after each access of DD RAM, as selected by the "7.4 Entry Mode Set" instruction.

Valid DD RAM Address Ranges

	Number of Characters	ADR
1 st line	40	00H to 27H
2 nd line	40	40H to 67H

7.10 Write Data

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
DATA WRITE								00H to 27H

RS=1

This instruction writes the data in DB7 to DB0 either the CG RAM or DD RAM. The RAM space (CG or DD), and the address in that is accessed depends on whether a “Set CG RAM Address” or a “Set DD RAM Address” instruction was last executed, and on the parameters of that instruction. The contents of the “7.4 Entry Mode Set”. When data is written to the CG RAM, the DB7, DB6 and DB5 bits are not displayed as characters.

7.11 Read Data

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DATA READ							

RS=1

This instruction reads data from either CG RAM or DD RAM, depending on the type of “Set RAM Address” instructions last sent. The address in that space depends on the “Set RAM Address” instructions parameters. Immediately before executing “Read Data”, “Set CG RAM Address” or “Set DD RAM Address” must be executed. The contents of the address counter are modified after each “Read Data”, as determined by the “7.4 Entry Mode Set”. Display shift is not executed, as described at of the “7.4 Entry Mode Set”.

7.12 Read Busy Flag/Address Counter

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
BF	ACC						

RS=0

Reading the instruction register yields the current value of the address counter and the busy flag. This instruction must be executed prior to any other instructions. ACC, the address counter value, will point to a location in either CG RAM or DD RAM, depending on the type of “Set RAM Address” instruction last sent.
In “Busy Flag Check” immediately after executing “Write Data” instruction, a valid address counter value can be ready as soon as BF goes low. The BF bit shows the status of the busy flag.

BF=1: Busy
BF=0: ready for next instruction, command receivable.

8. Other features

8.1 CG RAM

The display module equips CG RAM as user's are 320 bit = (5x8 bit/char) x8 chars of store user definable character fonts. The character fonts consists of 5 x 7 dots with underline. The number 1 ～ 36 corresponds to character fonts.

Character code	CG RAM address						CG RAM data (character pattern)							
	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
00H or (08H)	0	0	0	0	0	0	*	*	*	1	2	3	4	5
	0	0	0	0	0	1	*	*	*	6	7	8	9	10
	0	0	0	0	1	0	*	*	*	11	12	13	14	15
	0	0	0	0	1	1	*	*	*	16	17	18	19	20
	0	0	0	1	0	0	*	*	*	21	22	23	24	25
	0	0	0	1	0	1	*	*	*	26	27	28	29	30
	0	0	0	1	1	0	*	*	*	31	32	33	34	35
	0	0	0	1	1	1	*	*	*	36	0	0	0	0
01H or (09H)	0	0	1	0	0	0	*	*	*	1	2	3	4	5
	0	0	1	0	0	1	*	*	*	6	7	8	9	10
	0	0	1	0	1	0	*	*	*	11	12	13	14	15
	0	0	1	0	1	1	*	*	*	16	17	18	19	20
	0	0	1	1	0	0	*	*	*	21	22	23	24	25
	0	0	1	1	0	1	*	*	*	26	27	28	29	30
	0	0	1	1	1	0	*	*	*	31	32	33	34	35
	0	0	1	1	1	1	*	*	*	36	0	0	0	0

REMARKS;"*" :Don't care "0":Turned off "1":Turned on.

Dot assignment

1	2	3	4	5
6	7	8	9	10
11	12	13	14	15
16	17	18	19	20
21	22	23	24	25
26	27	28	29	30
31	32	33	34	35
		36		

・Remarks

The 36th dot is five.

Use those dots as underline.

8.2 Power-on reset

Internal status of the module is initialized, when controller detect rising power supply up.
The status are as follows;

1. Display clear
   Fills the DD RAM with 20 Hex (space code).
   During executing of "Display Clear" (Max 410 internal clock), the busy flag(BF) is "1".

2. Sets the address counter to 0H.
   Sets the address counter to point the DD RAM.

3. Display ON/OFF
   D=0: Display OFF
   C=0: Cursor OFF
   B=0: Blink OFF
4. Entry Mode Set
   I/D=1: increment
   S=0: No display shift
5. Function Set
   IF=1: 8-bit interface
6. Brightness Control
   BR0=BR1=0: 100%

・Remarks
There is a possibility that reset doesn't work by slow start power supply causes.
Therefore the initializing by commands needs.

8.3 CPU interface

The display module is capable to communicate some different type of bus systems such as i80 or M68, 8-bit or 4-bit data.

8.3.1 Select CPU

The module is able to connected to bus of i80 type or M68 type CPU, by setting JP2 jumper.
Refer to "8.5 Jumper" for detail.

8.3.2 4-bit CPU interface

If 4-bit interface is used, the 8-bit instruction are written nibble by nibble: the high-order nibble being written first, followed by low-order nibble. It is not necessary to check the busy flag between writing separate nibbles of individual instructions.

See "7.7.1 Function Set Command "for more information.

8.4 Test Mode

Self test functions built into the display module. The test mode is initiated by connecting 2 and 3 pin of 3pin connector(CN1) and power up.
In the test mode, checker patterns are displayed on all character position.
In the future, there is a possibility to remove a 3pin connector (CN1).

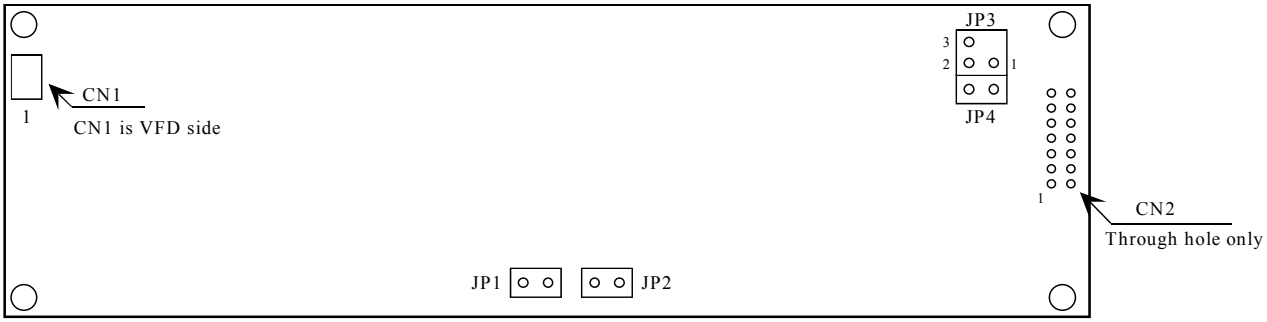
No.	Terminal
1	Vcc
2	Test
3	GND

3pin connector(CN1) is for the factory forwarding or the test mode.
As for the place of CN1, look at chapter 8.5.

8.5 Jumper

Some jumper are prepared on the PCB board, to set operating mode of the display module.
A soldering iron is required to short jumper.
No.2 and No.3 of the jumper "JP3" is used to reset of module.
You can reset the module by shorting No.2 and No.3 of the jumper "JP3" for some interval which is longer than 10 μ s.
The following figure shows the location of each jumper.

Location



The following table shows the function of No.1 and No.2 of JP3, JP2.
CU20029ECPB-W1J is no reset inputs from third hole of 14 through holes and M68 CPU bus interface. Reset input signal is active when it is low.

Table of No.1 and No.2 of JP3 setting

No.1 and No.2 of JP3	Third hole of 14 throrgh holes
Open	N.C
Short	$\overline{\text{RESET}}$

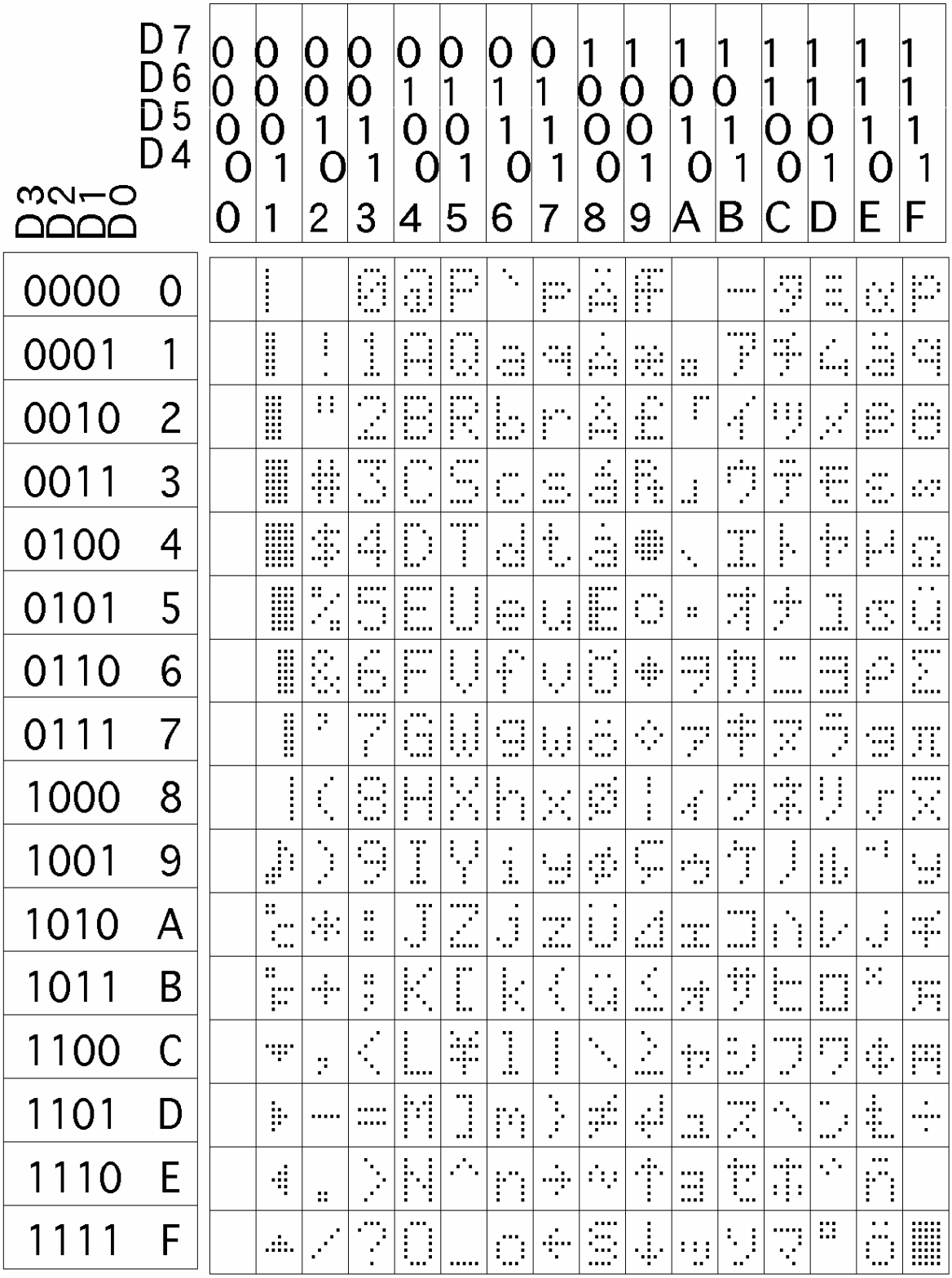
N.C: no connection

Table of JP2 setting

JP2	CPU bus mode	Control Signals
Open	M68 type	E,R/$\overline{\text{W}}$
Short	i80 type	$\overline{\text{WR}}$, $\overline{\text{RD}}$

JP1 and JP4 is factory use only.

9. Character Font

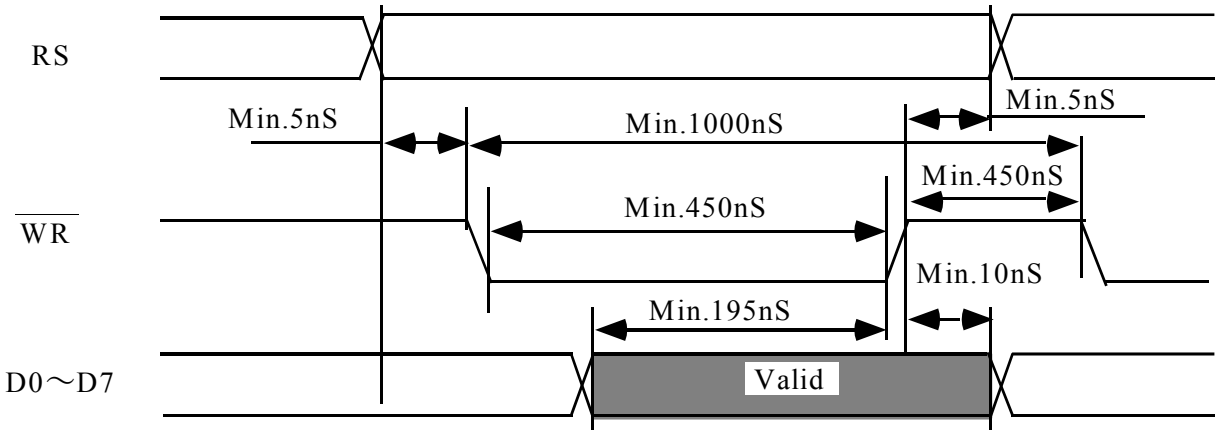


Character Table 0
[CG57103]

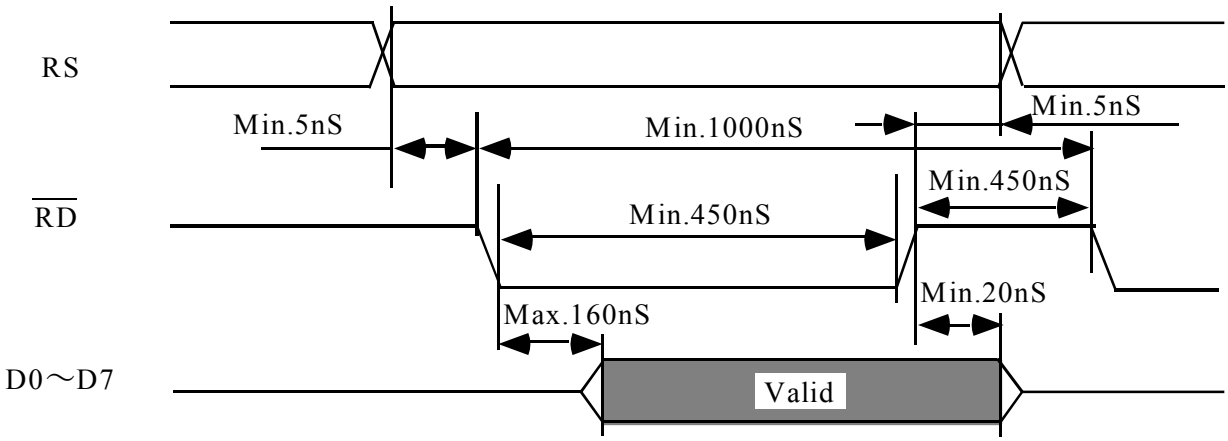
Note: Font number 00～07Hex(08～0FHex) is UDF.

10. Timing

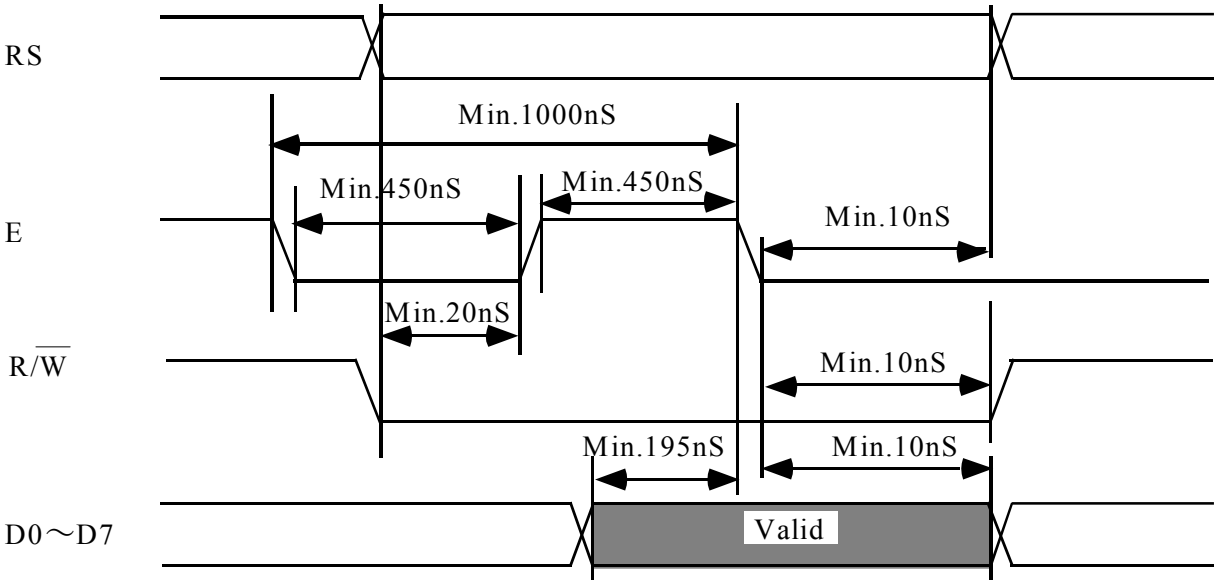
10.1 CPU bus write timing (i80 type)



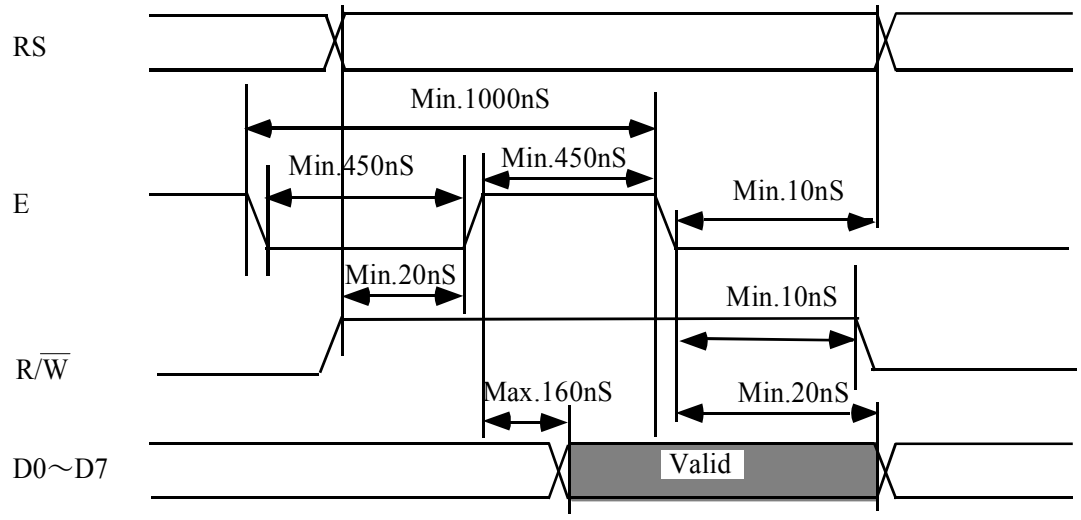
10.2 CPU bus read timing (i80 type)



10.3 CPU bus write timing (M68 type)

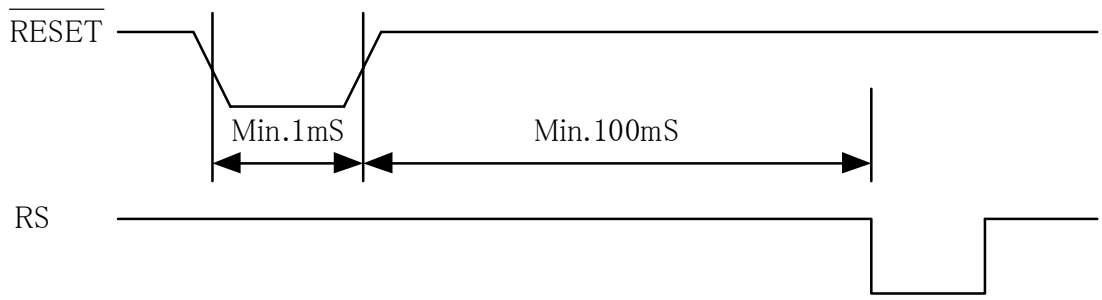


10.4 CPU bus read timing (M68 type)



10.5 External Reset Timing

Following chart shows the external reset timing.
Reset pulse (active low) should be longer than 1mS.
It is required at least 100mS to accept the data after reset pulse rises up.



11.Connector Pin assignment

11.1 14pin Connector (CN2)

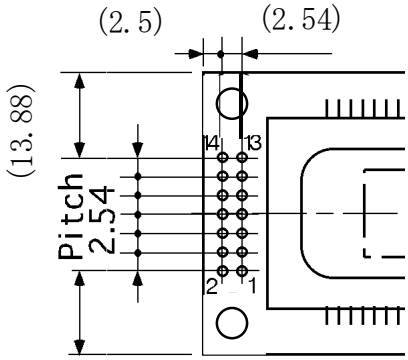
Fourteen (14) of through holes are prepared for power supply and data communications.
A connector or pins may be able to soldered to the holes.

No.	Terminal	No.	Terminal
1	GND	8	DB1
2	Vcc	9	DB2
3	※NC	10	DB3
4	RS	11	DB4
5	R/$\overline{W}$ ($\overline{WR}$)	12	DB5
6	E ($\overline{RD}$)	13	DB6
7	DB0	14	DB7

NC: no connection

Location and dimensions (Diameter of holes is 1.0 mm.)

※The third through hole is for reset input when No.1 and No.2 of JP3 are short.



Unit : mm

11.2 3pin Connector (CN1)

A three (3) pin connector on the board is factory use only, and may be removed in future.

11. Outline dimension