Clocks

MM5370, MM5371 digital alarm clocks

general description

The MM5370 and MM5371 digital alarm clocks are monolithic MOS integrated circuits utilizing P-channel low-threshold, enhancement mode and ion-implanted depletion mode devices. They provide all the logic required to build several types of clocks and timers. Three display modes (time, alarm and sleep) are provided to optimize circuit utility. The circuits interface simply with 7-segment gas discharge displays. The timekeeping function operates from either a 60 Hz (MM5370) or 50 Hz (MM5371) input, and the display format may be either 12 hours (with leading-zero blanking and AM/PM indication) or 24 hours. Outputs consist of display drives, alarm enable and sleep (e.g., timed radio turn off). Power failure indication is provided to inform the user that incorrect time is being displayed. Setting the time cancels this indication. These clocks are packaged in 28-pin dual-in-line packages.
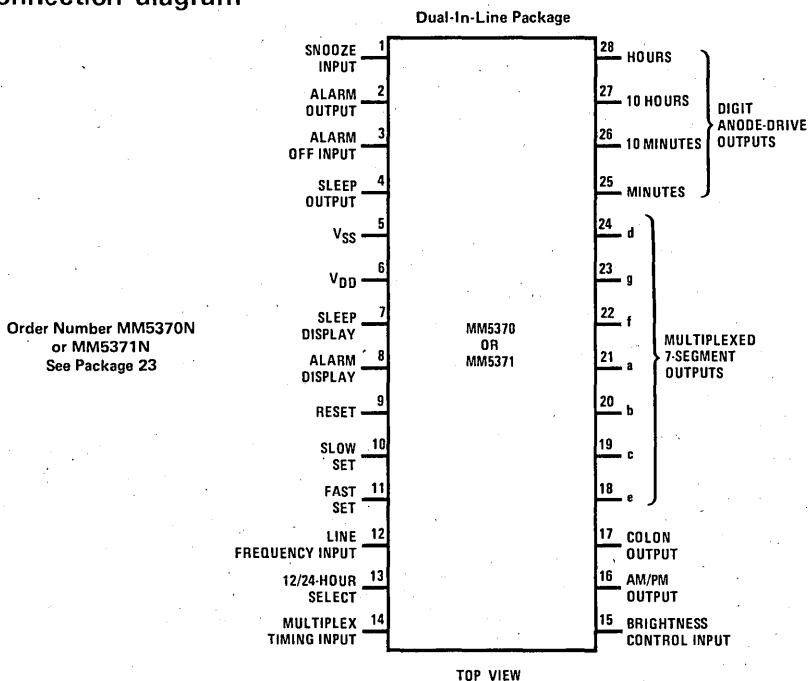
- AM/PM drive output in 12-hour format
- Leading-zero blanking in 12-hour format
- 24-hour alarm setting
- All counters are resettable
- Fast and slow set controls
- Power fail indication
  Blinking colon—12-hour or 24-hour mode
  Blinking AM/PM indicators—12-hour only
- Brightness control capability
- Simple interface to gas discharge display
- Presettable 59-minute sleep timer
- 9-minute snooze timer

applications

- Alarm clocks
- Desk clocks
- Clock/radios
- Automobile clocks
- Industrial clocks
- Appliance timers

features

- Single power supply
- Low power dissipation
- 12 or 24-hour display format
- Colon drive output

connection diagram

Dual-In-Line Package

Order Number MM5370N
or MM5371N
See Package 23

Pin	Signal		Pin	Signal	
1	SNOOZE INPUT		28	HOURS	DIGIT ANODE-DRIVE OUTPUTS
2	ALARM OUTPUT		27	10 HOURS	
3	ALARM OFF INPUT		26	10 MINUTES	
4	SLEEP OUTPUT		25	MINUTES	
5	V$_{SS}$		24	d	
6	V$_{DD}$		23	g	
7	SLEEP DISPLAY		22	f	MULTIPLEXED 7-SEGMENT OUTPUTS
8	ALARM DISPLAY		21	a	
9	RESET		20	b	
10	SLOW SET		19	c	
11	FAST SET		18	e	
12	LINE FREQUENCY INPUT		17	COLON OUTPUT	
13	12/24-HOUR SELECT		16	AM/PM OUTPUT	
14	MULTIPLEX TIMING INPUT		15	BRIGHTNESS CONTROL INPUT	

MM5370 OR MM5371

TOP VIEW

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3V to V_{SS} − 29V
Voltage at Any Display Output Pin	V_{SS} + 0.3V to V_{SS} − 55V
Operating Temperature	−25°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics T_A within operating range, V_{SS} = 0V, V_{DD} = −21V to −29V unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage					
Functioning Clock	No Output Loads	−8.0	−25	−29	V
Outputs Driving Display		−21		−29	V
Power Supply Current	No Output Loads, (See "Power Supply" Section)			5.0	mA
60 Hz (or 50 Hz) Input Frequency					
MM5370		dc		30k	Hz
MM5371		dc		30k	Hz
60 Hz (or 50 Hz) Input Voltage					
Logical High Level		V_{SS}−1.0	V_{SS}	V_{SS}	V
Logical Low Level		V_{DD}	V_{DD}	V_{DD}+1	V
Brightness Control Voltage					
Logical High Level		V_{SS}−2.0	V_{SS}	V_{SS}	V
Logical Low Level		V_{DD}	V_{DD}	V_{SS}−4.0	V
All Other Input Voltages					
Logical High Level		V_{SS}−1.0	V_{SS}	V_{SS}	V
Logical Low Level	Internal Depletion Load to V_{DD}	V_{DD}	V_{DD}	V_{DD}+2.0	V
Multiplex Frequency	Determined by Ext. RC	500		60k	Hz
	Driven by Ext. Time Base	dc		60k	Hz
Power Failure Detect Voltage	(V_{DD} Voltage)	−3.0		−8.0	V
Output Currents	V_{DD} = −21V to −29V, V_{SS} = 0V				
Digit Anode Outputs					
Logica High Level, ("ON")	V_{OH} = V_{SS} − 5V	8.0			mA
Logical Low Level, ("OFF")	V_{OL} = V_{SS} − 45V			40	μA
Segment Cathode Outputs					
Logical High Level, ("OFF")	V_{OH} = V_{SS} − 5V	2.0			mA
Logical Low Level, ("ON")	V_{OL} = V_{SS} − 45V			10	μA
Alarm and Sleep Outputs					
Logical High Level, ("ON")	V_{OH} = V_{SS} − 2V	1.5			mA
Logical Low Level, ("OFF")	V_{OL} = V_{DD} + 2V	−10			μA

functional description

A block diagram of the MM5370 and MM5371 clocks is shown in *Figure 1*. The various display modes provided by these clocks are listed in Table I. The functions of the controls are listed in Table II. A connection diagram for these devices is shown on page 1. Unless indicated otherwise, the following discussions are based on *Figure 1*.

Power Supply: Even though these clocks do not require a regulated supply, and operate over a wide voltage range, certain factors should be remembered. Power supply voltages between −8V and −21V will provide all functions of the clocks (proper counting, etc.) except output drive capabilities. In order to ensure proper output levels and breakdown voltages it is necessary to provide supply voltages between −21V and −29V. At some point between −7V and −3V, the power fail latch becomes "set". All counters will then hold their count at least 0.5V below this point. This ensures power failure indication before any count is lost. For proper power failure indication, power supply rise time should not exceed 10 V/ms, since faster rise times may be faster than propagation delays within the latch circuitry.

functional description (Continued)

Line Frequency Input (pin 12): A shaping circuit is provided to square the 60 Hz (MM5370) or 50 Hz (MM5371) input. This circuit allows use of a sinewave input. The Schmitt Trigger shaper *(Figure 2)* is designed to provide approximately 6V of hysteresis. A simple RC filter, such as shown in *Figure 8*, should be used to remove possible line-voltage transients that could cause the clock to gain time or damage the device. The shaper output drives a counter chain which performs the time-keeping function. A prescale counter divides the line input frequency to obtain a 1 pps timebase.

Display Mode Select Inputs (pins 7 and 8): In the absence of either of these inputs, the display drivers output time-of-day information to the display. Internal pull-down (to V_{DD}) depletion loads allow use of simple SPST switches for connecting these inputs to V_{SS}, thereby selecting alternate display modes. If more than one mode is simultaneously selected, the priorities are are noted in Table I. As shown in *Figure 1* the multiplexed code converter receives time, alarm and sleep information from appropriate points in the clock circuitry. The display mode select inputs control the gating of the desired data to the multiplexed code converter inputs and ultimately (via output drivers) to the display.

Time Setting Inputs (pins 10 and 11): Both fast and slow setting inputs are provided. These inputs are applied either singly or in combination to obtain the control functions listed in Table II. Again, internal pull-down depletion loads are provided; application of V_{SS} to these pins effects the control functions. Note that the control functions proper are determined by the selected display mode. An optional hold-time control function can be obtained as shown in *Figure 8.*

Reset Input (pin 9): Applying V_{SS} to this input results in resetting the timekeeping function of the clock; a pull-down depletion load is provided at this input. Time is reset to 12:00 AM in the 12-hour format, or 00:00 in the 24-hour format. See Table II.

12 or 24-Hour Select Input (pin 13): By leaving this pin unconnected, the clock is programmed to provide a 12-hour display format. This format provides for zero-blanking the most significant display digit (ten's of hours). An internal pull-down depletion load is again provided; connecting this pin to V_{SS} programs the 24-hour display format. (See *Figure 8*).

Output Multiplexer Operation: Depending upon the selected display mode (see Table I), outputs from the appropriate internal counter are time division multiplexed to provide digit-sequential access to the data. Thus, instead of requiring 28 leads to interconnect a 4-digit clock and its display (7-segments per digit), only 11 output leads are required. Note that the MM5370 and MM5371 actually provide 13 outputs (4-digit anode drive outputs plus 9 "segment" cathode drive outputs). The two additional "segment" drives are provided to accommodate displays which feature a colon and/or AM/PM indication. (See sections on pin 16 and pin 17). The multiplexed code converter and output drivers are controlled by a multiplex oscillator. The oscillator and external timing components set the

frequency of the multiplexing function. Each digit anode is sequentially enabled for a time equal to the period of one cycle of the multiplex oscillator frequency.

When driving gas discharge displays which enclose more than one digit in a common gas envelope, it is necessary to either (1) inhibit the segment drive voltage(s) for a short time during inter-digit transitions, or (2) avoid physically adjacent inter-digit transitions. The MM5370 and MM5371 clocks utilize an interlaced output sequence to eliminate the need for inter-digit blanking circuitry and to prevent display arcing problems. The digit sequence is: (1) digit no. 1 (ten's of hours), (2) digit no. 3 (ten's of minutes), (3) blank for one digit time, (4) digit no. 2 (unit hours), (5) digit no. 4 (unit minutes), (6) blank for one digit time, etc. The two blanking intervals are provided to recharge level-translating capacitors located in the display segment drive lines (see *Figure 8*). Both segment data and digit enables are blanked. *Figure 3* is a timing diagram which illustrates output timing.

Multiplex Timing Input (pin 14): The multiplex oscillator is shown in *Figure 4*. Adding an external resistor and capacitor to this circuit via the multiplex timing input produces a relaxation oscillator. The waveform at this input is a quasi-sawtooth that is squared by the shaping action of the Schmitt Trigger in *Figure 4. Figure 5* provides guidelines for selecting the external components relative to the desired multiplex frequency. *Figure 6* illustrates a method of synchronizing or driving the multiplex oscillator with an external timebase. The external RC timing components may be omitted and this input driven by an external timebase; the required logic levels are the same as the 60 Hz or 50 Hz input.

Output Circuits: All display output drivers are open-drain devices with sources common to V_{SS} (pin 5), see *Figure 7*. *Figure 8* illustrates interfacing the clock outputs and a gas discharge display.

Brightness Control Input (pin 15): Since display brightness is a function of cathode segment current, a capability of interrupting this current for a variable percentage of the digit interval results in a brightness control. Connecting this Schmitt Trigger input (see *Figure 2*) to V_{DD} places all cathode segment drive voltages at the high level, thereby inhibiting the display. Conversely, V_{SS} applied to this input enables the cathode segment drives. The Schmitt Trigger shaper provides approximately 1V of hysteresis, which facilitates using a waveform such as a sawtooth with a variable slope (or variable dc component) to effect the shaper output duty cycle and, therefore, the display brightness. The control waveform should be derived from the multiplex frequency; a circuit is included in *Figure 8*.

Alarm Operation and Output (pin 2): An alarm comparator (see *Figure 1*) senses coincidence between the alarm counters (the alarm setting) and the time counters (real time). The comparator output is used to set a latch in the alarm and sleep circuits. This latch enables the alarm output driver (see *Figure 7*), the output of which is used to control the external alarm sound generator. The alarm latch remains set for 59 minutes, during which the alarm will sound if the latch output is not

functional description (Continued)

temporarily inhibited by another latch set by the snooze input (pin 1) or reset by the alarm "OFF" input (pin 3). Alarm time setting and resetting are outlined in Table II. When initially powered, alarm is in "OFF" state.

Alarm "OFF" Input (pin 3): Momentarily connecting this pin to V_{SS} resets the alarm latch and thereby silences the alarm. This input is also returned to V_{DD} by an internal depletion load. The momentary alarm "OFF" input also readies the alarm latch for the next alarm comparator output; the alarm will sound again in 24 hours (or at a new alarm setting). If it is desired to silence the alarm for a day or more, the alarm input should remain at V_{SS}.

Snooze Timer Input (pin 1): Momentarily connecting this pin to V_{SS} inhibits the alarm output for between 8 and 9 minutes, after which the alarm will again be sounded. This input is pulled to V_{DD} by an internal depletion load. The snooze feature may be repeatedly used during the 59 minutes in which the alarm latch remains set.

Sleep Timer and Output (pin 4): The sleep output at pin 4 can be used to turn off a radio (or other appliance) after a desired time interval of up to 59 minutes. The time interval is chosen by selecting the

sleep display mode (see Table I) and setting the desired time interval (see Table II). This automatically results in a current-source output via pin 4 which can be used to turn on a radio. When the sleep counter, which counts downwards, reaches 00 minutes a latch is reset and the sleep output drive current is removed, thereby turning off the radio. This turn off also may be manually controlled (at any time in the count-down) by a momentary V_{SS} connection to the snooze input (pin 1). This input is also returned to V_{DD} by a depletion load. The output circuitry is the same as the alarm output (see Figure 7).

AM/PM Cathode Output (pin 16): Current with this writing, gas-discharge clock displays are available with two types of AM/PM indications, (1) AM and PM indicators common to digits 3 and 4 respectively; and (2) a PM only indication common to digit 1. Figure 3 illustrates an AM/PM cathode drive output that is compatible with both display types. Note that this same output also provides a non-blinking (steady) colon drive common to digit two. Power failure is shown by turning off this output at a 1 Hz rate.

Colon Cathode Output (pin 17): As an optional indication of clock operation, some users may prefer to display a 1 Hz activity. As shown in Figure 3, a cathode drive output is provided to facilitate a blinking colon.
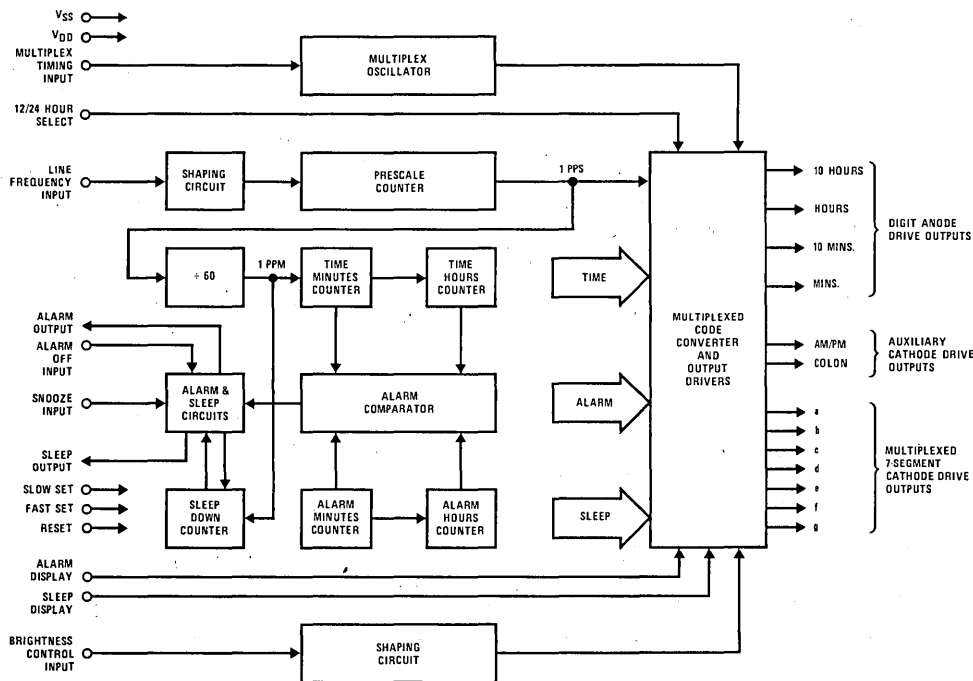

FIGURE 1. MM5370 and MM5371 Digital Alarm Clock, Block Diagram

functional description (Continued)

TABLE I. MM5370 and MM5371 Display Modes

*SELECTED DISPLAY MODE	DIGIT NO. 1	DIGIT NO. 2	DIGIT NO. 3	DIGIT NO. 4
Time	10's of Hours	Unit Hours	10's of Minutes	Unit Minutes
Alarm	10's of Hours	Unit Hours	10's of Minutes	Unit Minutes
Sleep	Blanked**	Blanked	10's of Minutes	Unit Minutes

*If more than one display mode input is applied, the display priorities are in the order of Sleep (overrides all others), Alarm, Seconds, Time (no other mode selected).

**F segment is lit in 12-hour display mode. This may be eliminated by using circuit shown in *Figure 9*.

Table II. MM5370 and MM5371 Setting Control Functions

SELECTED DISPLAY MODE	CONTROL INPUT	CONTROL FUNCTION
Time*	Slow	Minutes Advance at 2 Hz Rate
	Fast	Minutes Advance at 60 Hz Rate
	Both	Minutes Advance at 60 Hz Rate
	Reset	Time Resets to 12:00 AM (12-hour format)
	Reset	Time Resets to 00:00 (24-hour format)
Alarm	Slow	Alarm Minutes Advance at 2 Hz Rate
	Fast	Alarm Minutes Advance at 60 Hz Rate
	Both	Alarm Resets to 12:00 AM (12-hour format)
	Both	Alarm Resets to 00:00 (24-hour format)
Sleep	Slow	Subtracts Count at 2 Hz Rate
	Fast	Subtracts Count at 60 Hz Rate
	Both	Subtracts Count at 60 Hz Rate

*When setting time sleep minutes will decrement at rate of time counter, until the sleep counter reaches 00 minutes (sleep counter will not recycle).
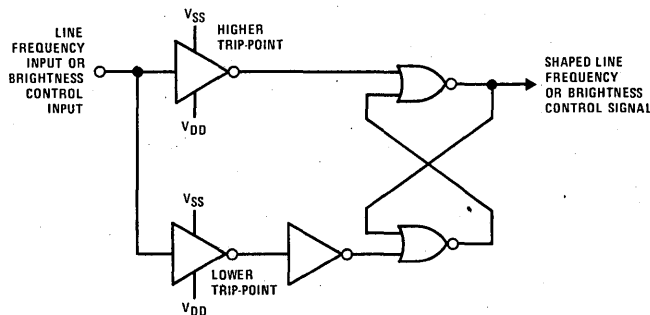

FIGURE 2. 60 Hz (or 50 Hz) Input (or Brightness Control Input) Shaping Circuit

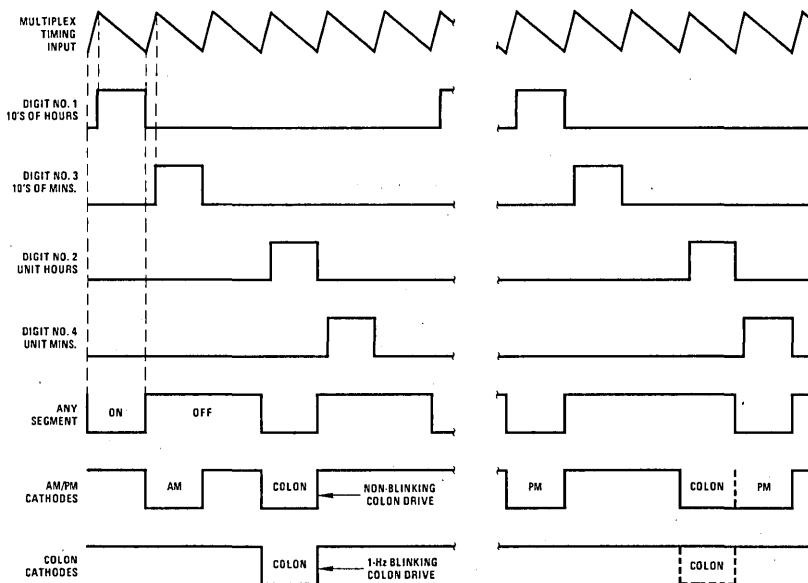## functional description (Continued)

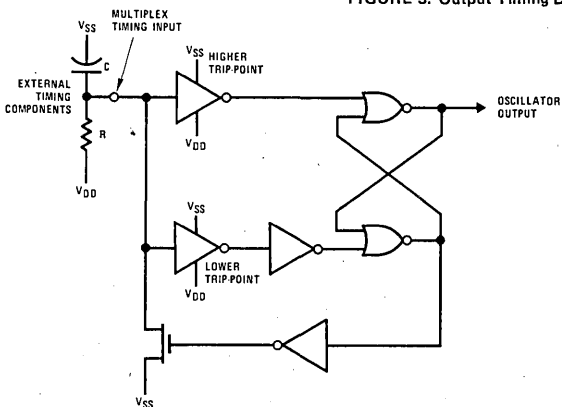FIGURE 3. Output Timing Diagram
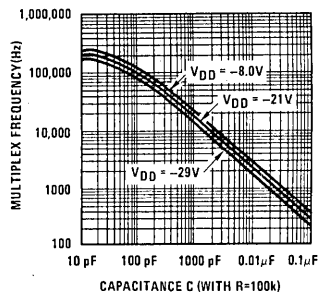

FIGURE 4. Multiplex Oscillator Circuit

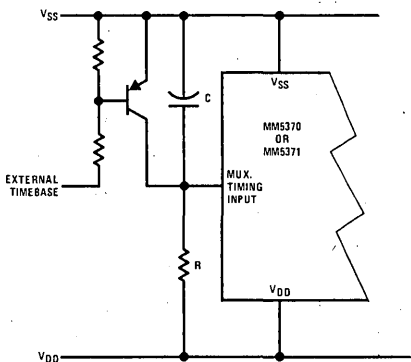FIGURE 5. Multiplex Timing Component Selection Guide (Typical Only)

FIGURE 6. Synchronizing or Driving Multiplex Oscillator

Note 1: For synchronizing, free running period should be set to run slightly longer than external timebase over temperature.

Note 2: For driving, timing capacitor should be deleted.
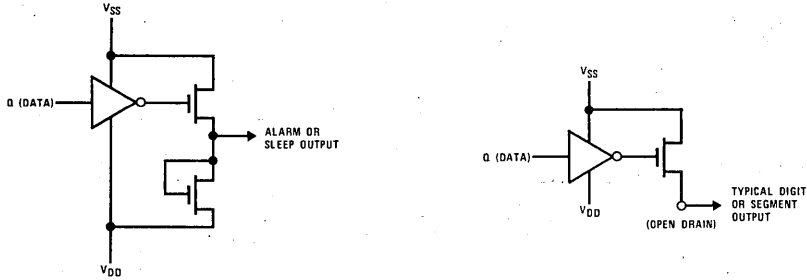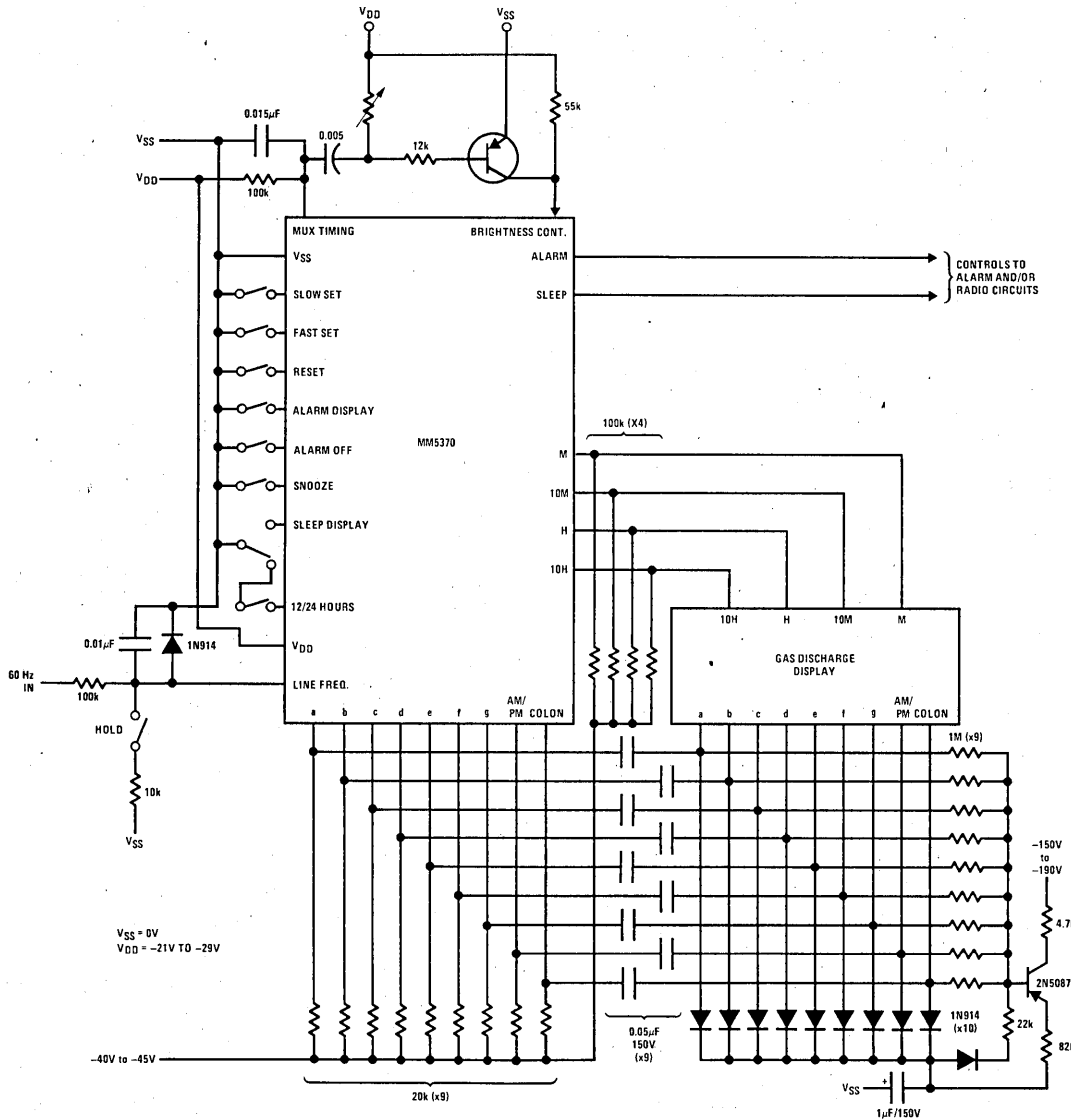
functional description (Continued)

FIGURE 7. Output Circuits

FIGURE 8. Recommended Application