1/21/21

FTDI

Kompakt #

CLK G

RTS Invert

DO

Z80 input P.U.'s

Z80 / SRAM

Z80 Status LEDS

+ CLOCK (running)

Z80 ADDR, DATA, OUT LEDS

A15-A0 Switches

(8) Control Switches

A15-A0 Switch Enable Logic

Control Switches SR

OUT-LED Latch + Logic

All AT328P Setup

AT328P D2-D9/A0-A5

Z80 Clock DO

Z80 Reset logic

DBus Serialization ('165 / '595)

uUSB → CP2110 → TX/RX

DTR + Switches → AT328 RESET

DO

LiPo charge

5V Boost

Power Switch + LED

DO

Edge connectors?

(+) '328 D10-D13 access @edge

Usable?

TEST

SPI flash / D10-D13

+3.3V (CP2110)

+ level shifters

No

Glue Logic

De-spiking Caps DO

Pull-up control switches

X Switches → GND ~~~!

fuse & ferrite bead?

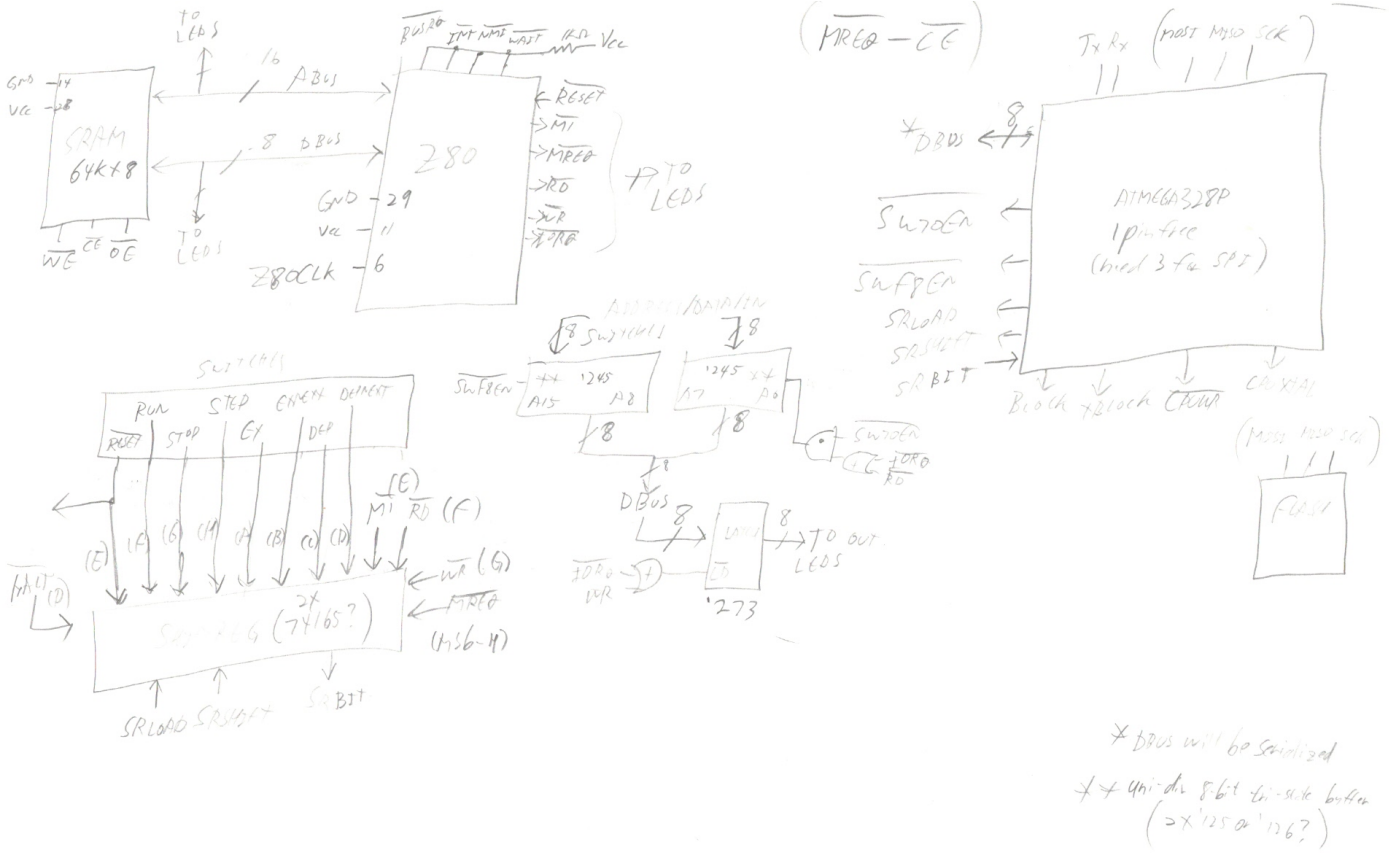
locators for pins?

* fix power-up hangs (don't Sleep@ P.U.?)

Current TO-DO

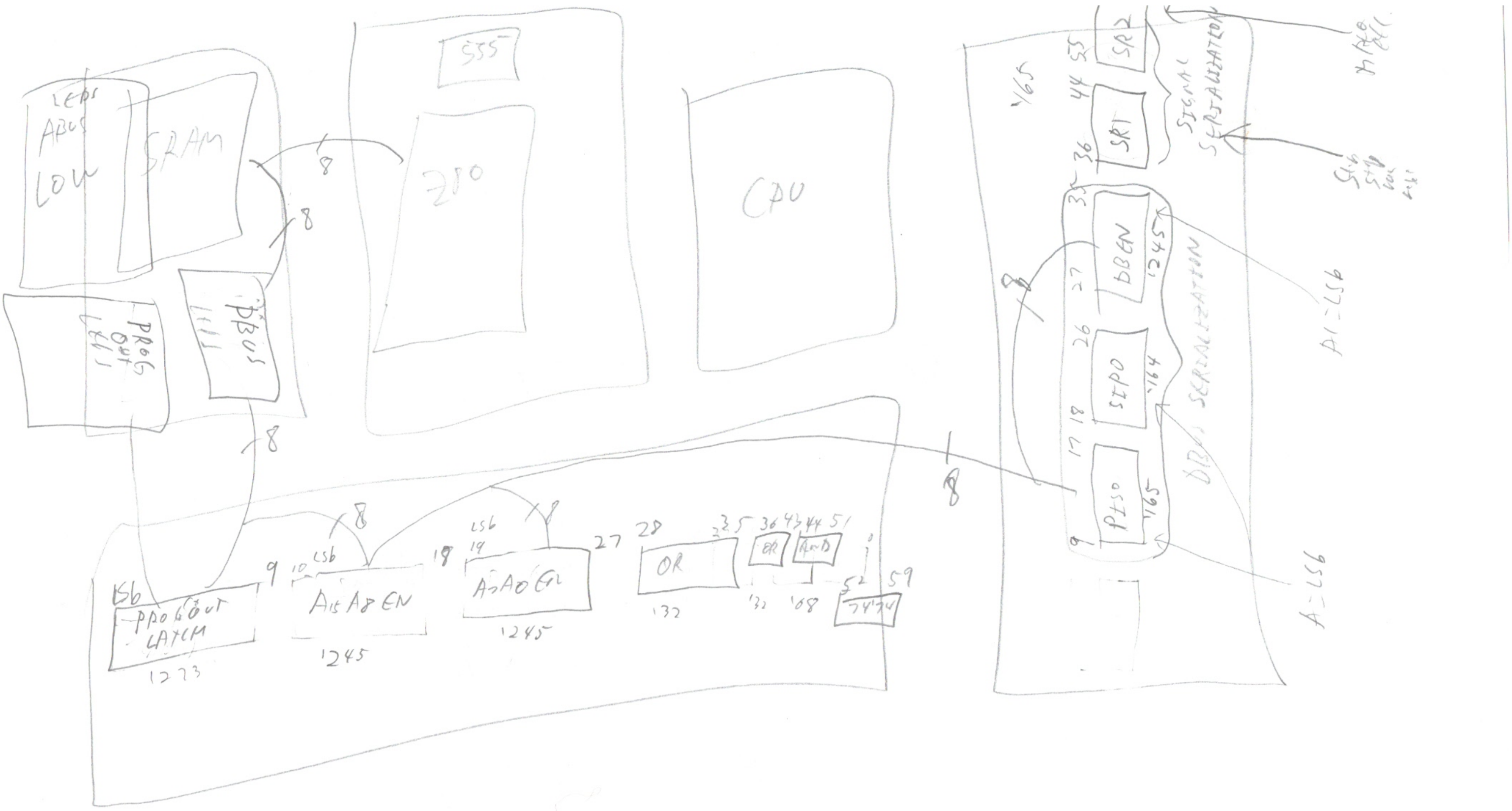
1/26/21

- ~~Try using FT230 for CLK6, DTR# (and KEEP_AWAKE#) & 3.3V out~~
  ~~(get rid of 74LS DTR logic + Xtal oscillator + 555)~~
  → ~~FT231~~
- ~~Reset/programming switches for AT328P~~ ← pick switch
- ~~Clocking for Z80~~
- ~~LiPo charge / load sharing / boost / power switch / power status LEDs / fuse / ferrite bead (2)~~ / battery holder ③
- ~~Edge connectors for D10–D13 (do they work?)~~
- De-spiking caps / expose VCC/GND ①
- ~~No ~~ from address switches → GND~~
- ~~Add pin1 marks for all chips~~ ②
- Shove components around to improve ratsnest
- ~~NET CLASSES (for VCC & GND)?~~
- ERC/DRC ④



* DBUS will be serialized

** Unidir 8-bit tri-state buffer (=x'125 or '126?)



KEEP ✓

OE ✓, WR, A15-A0 Switches ✓

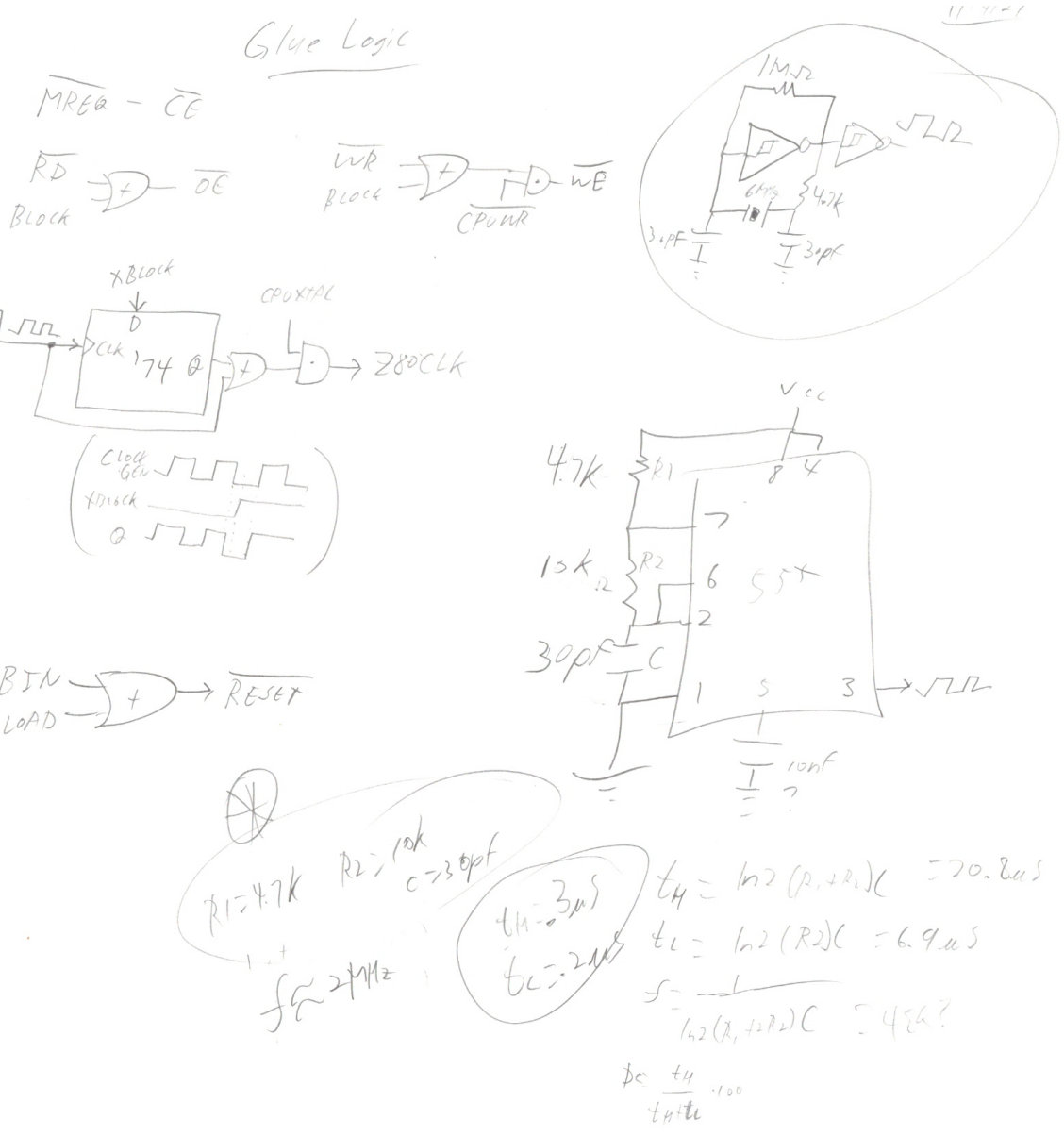
✓ 12-bit SR
✓ SW--EN (X2) LSB

✓ PROG OUT LATCH
✓ Z80CLK
✓ DBUS SERIALIZATION

RESET

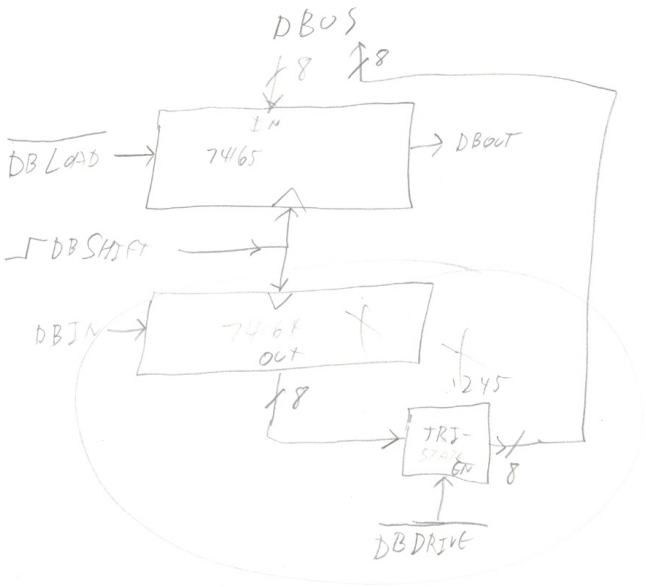
STATUS LIGHTS
FLASH
LIPO
V BOOST

Glue Logic


MREQ - CE
RD
BLOCK
OE
IWR
BLOCK
WE
CPUWR
1M Ω
4.7K
6PFD
3.3PF
3.3pF
XBLOCK
CLOCK GEN
CLK
'74
Q
D
CPUXTAL
Z80CLK
CLOCK GEN
XBLOCK
Q
DBIN
SRLOAD
RESET
Vcc
4.7K
R1
10K Ω
R2
30pF
C
555
8
4
7
6
2
1
5
3
10nF
?
R1=4.7K
R2=10K
C=30pF
f≈2MHz
tH=3μS
tL=2μS
tH = ln2 (R1+R2)C = 20.8μS
tL = ln2 (R2)C = 6.9μS
f = 1 / ln2(R1+2R2)C ≈ 45K?
DC = tH / (tH+tL) ·100

11/7/21

DATABUS SERIALIZATION



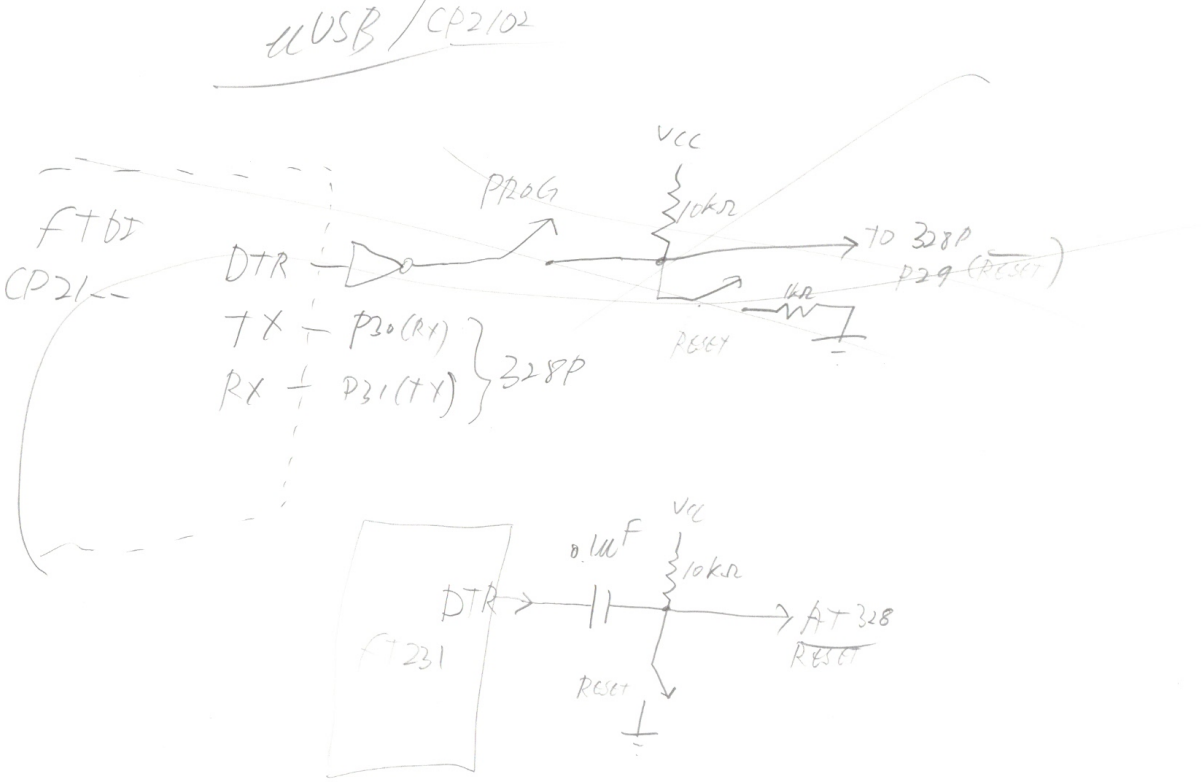
Shift in
MSb first

shift out
MSb first

ATMEGA 328P PINOUT

1/17/21

		328P
D0	Rx	30
D1	Tx	31
D2	$\overline{\text{DBLOAD}}$	32
D3	DBSHIFT	1
D4	DBOUT	2
D5	DBIN	9
D6	$\overline{\text{DBDRIVE}}$	10
D7	$\overline{\text{SRLOAD}}$	11
D8	SRSHIFT	12
D9	SROUT	13
D10	Sel	14
D11	MOST	15
D12	MISO	16
D13	Sck	17
A0	BLOCK	23
A1	$\overline{\text{CPUHR}}$	24
A2	XBLOCK	25
A3	CPUXTAL	26
A4	$\overline{\text{SWIFTEN}}$	27
A5	$\overline{\text{SWJOEN}}$	28


uUSB / CP2102
FTDI
CP21--
DTR
TX → P30(RX)
RX ← P31(TX)
328P
P20(G
VCC
10kΩ
TO 328P
P29 (RESET)
RESET
FT231
0.1uF
DTR
AT328
RESET

1/24/21

CHOICES (POWER)

	COMPLEXITY	RELIABILITY	OTHER
LiPo → System Bus	73831	3.7V & 280???	If discharge > charge, USB power will eventually be insufficient
LiPo+Boost → System Bus	73831 / Booster / Big Inductor	PERFECT ✓	Higher discharge rate; USB power may not suffice } for level shifters?
LiPo + Load Share ↳ Better stability	73871	3.7V & 280? But can plug in	USB power always an option
(*) LiPo + Boost + Load Share ↳ Better stability	73871 / Booster / Big Inductor	PERFECT ✓	USB Power always an option } for level shifters?

CHOICES (SERIAL)

	COST	AVAIL	PKG	~~DONE~~	EXTERNAL XTAL
CP2102	$$$	*	QFN	NO	NO
CH340	$	**	SOIC	YES	YES
FT23X	$$	***	SOIC	NO	NO

(231?)

230 no DTR
232 Lots of pins

6.2 Self Powered Configuration

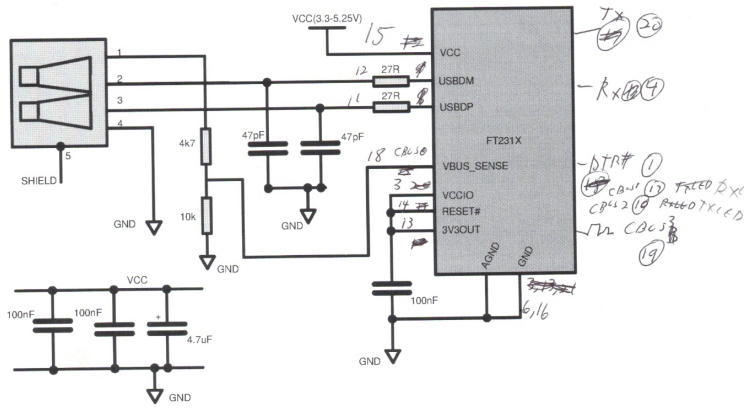


Figure 6.2 Self Powered Configuration

Figure 6.2 illustrates the FT231X in a typical USB self powered configuration. A USB self powered device gets its power from its own power supply, VCC, and does not draw current from the USB bus. The basic rules for USB self powered devices are as follows –

i) A self powered device should not force current down the USB bus when the USB host or hub controller is powered down.
ii) A self powered device can use as much current as it needs during normal operation and USB suspend as it has its own power supply.
iii) A self powered device can be used with any USB host, a bus powered USB hub or a self powered USB hub.

The power descriptor in the internal MTP memory of the FT231X should be programmed to a value of zero (self powered).

In order to comply with the first requirement above, the USB bus power (pin 1) is used to control the VBUS_Sense pin of the FT220X device. When the USB host or hub is powered up an internal 1.5kΩ resistor on USBDP is pulled up to +3.3V, thus identifying the device as a full speed device to the USB host or hub. When the USB host or hub is powered off, VBUS_Sense pin will be low and the FT220X is held in a suspend state. In this state the internal 1.5kΩ resistor is not pulled up to any power supply (hub or host is powered down), so no current flows down USBDP via the 1.5kΩ pull-up resistor. Failure to do this may cause some USB host or hub controllers to power up erratically.

Figure 6.2 illustrates a self powered design which has a +3.3V to +5.25V supply.

Note:

1. When the FT231X is in reset, the UART interface I/O pins are tri-stated. Input pins have internal 200kΩ pull-up resistors to VCCIO, so they will gently pull high unless driven by some external logic.

10 Layout

10.1 Layout Guidelines

As for all switching power supplies, especially those running at high switching frequency and high currents, layout is an important design step. If the layout is not carefully done, the regulator could suffer from instability and noise problems. To maximize efficiency, switch rise and fall time are very fast. To prevent radiation of high frequency noise (for example, EMI), proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize interplane coupling. The input capacitor needs not only to be close to the VIN pin, but also to the GND pin in order to reduce input supply ripple.

The most critical current path for all boost converters is from the switching FET, through the rectifier FET, then the output capacitors, and back to ground of the switching FET. This high current path contains nanosecond rise and fall time and must be kept as short as possible. Therefore, the output capacitor not only must be close to the VOUT pin, but also to the GND pin to reduce the overshoot at the SW pin and VOUT pin.

For better thermal performance, TI suggest to make copper polygon connected with each pin bigger.

10.2 Layout Example

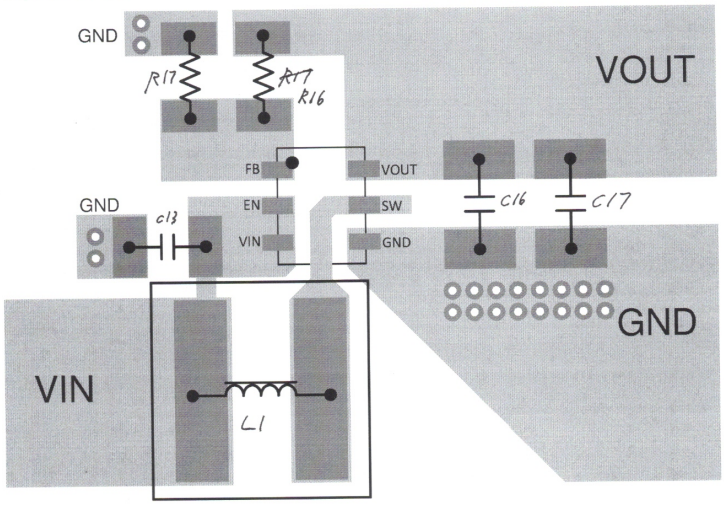
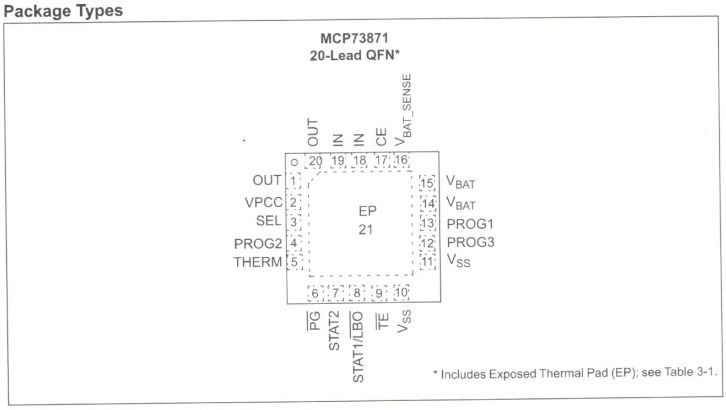
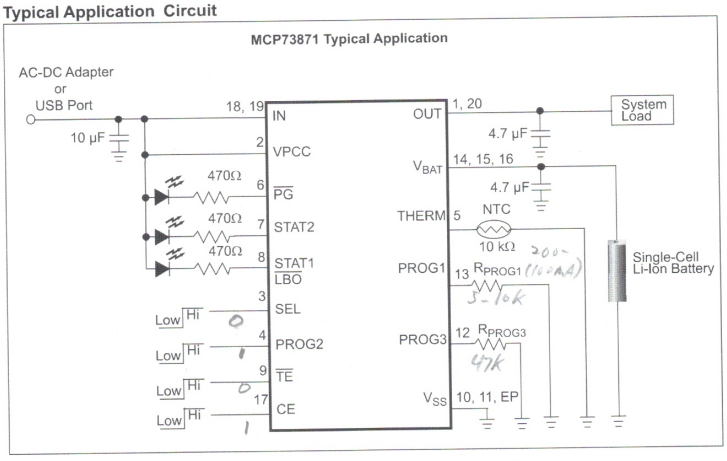


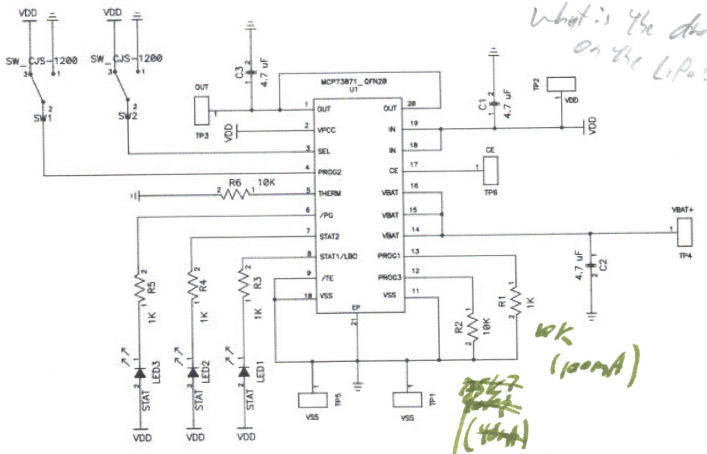
Figure 10-1. Layout Example

Package Types



Typical Application Circuit




VDD
SW_CJS-1200
SW1
SW2
C3
4.7 uF
MCP73871_QFN20
OUT
VPCC
SEL
PROG2
THERM
/PG
STAT2
STAT1/LBO
/TE
VSS
EP
IN
CE
VBAT
PROG1
PROG3
C1
TP2
TP3
TP6
R6
10K
VBAT+
TP4
C2
R5
R4
R3
R2
10K
R1
1K
LED3
LED2
LED1
STAT
TP5
TP1