

Product Specification

5.5" 256*64 SOG25664A2

OLED Module



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Reference Controller Datasheet

SSD1322

1. FUNCTIONS & FEATURES

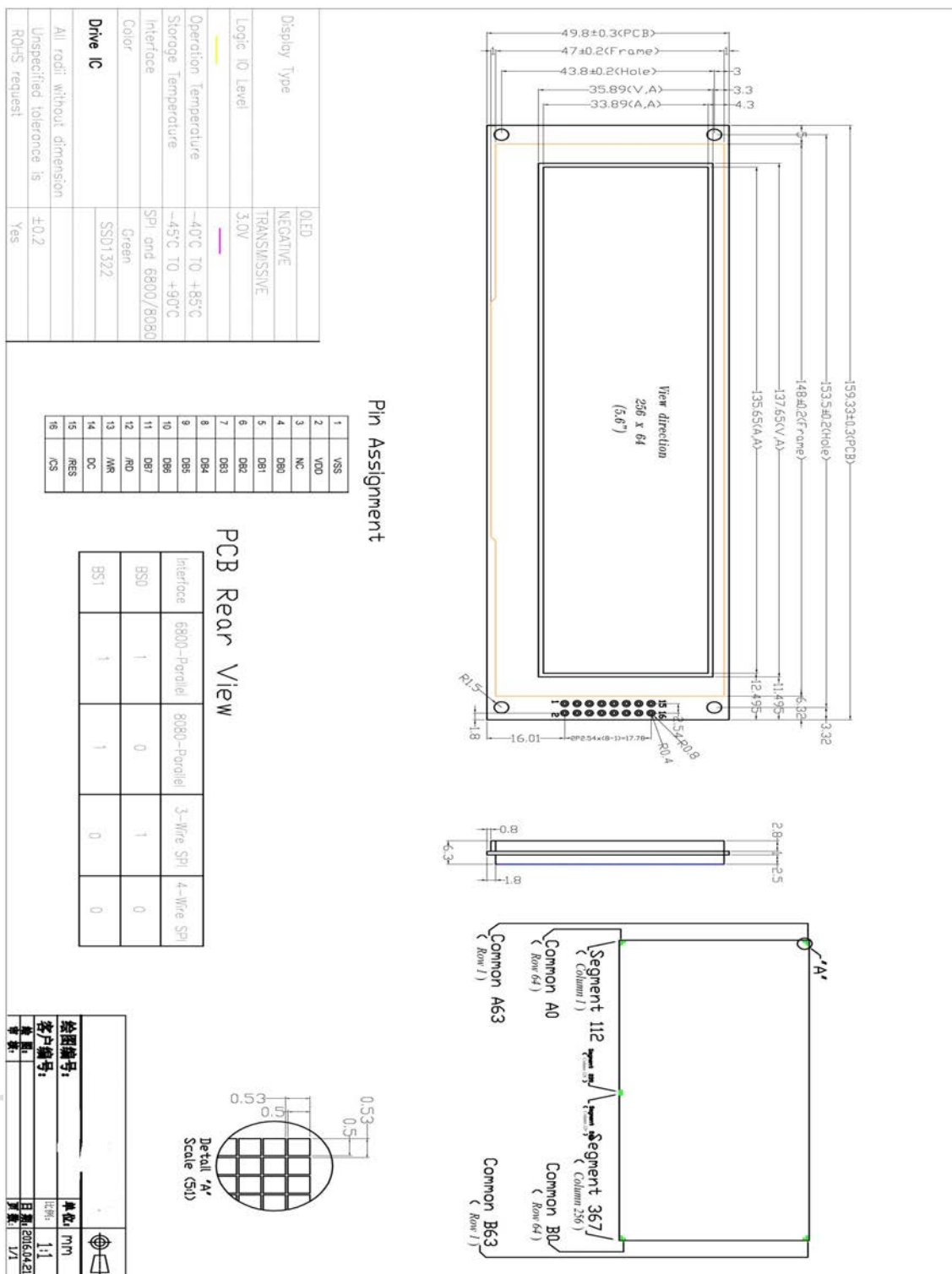
Features

- 256X64 dots
- Font Color: YELLOW/WHITE/GREEN
- Driver IC:SSD1322
- 8-BIT 68XX/80XX Parallel,4-wire SPI,3-wire SPI

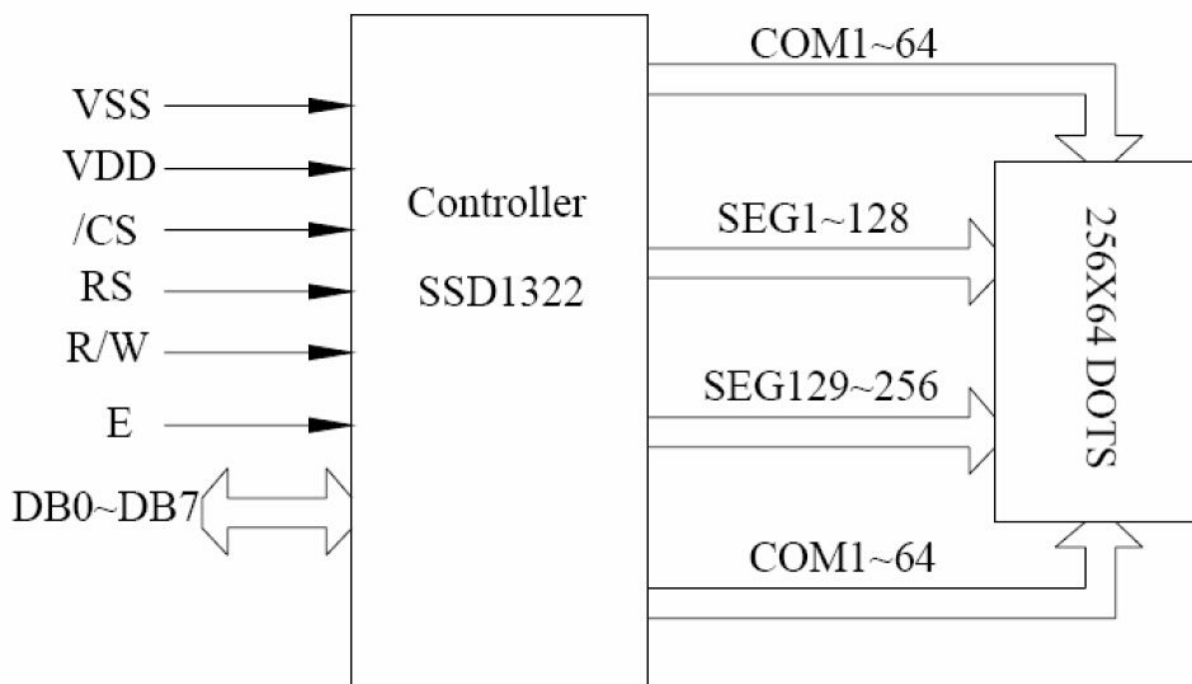
2. MECHANICAL SPECIFICATIONS

ITEM	SPECIFICATIONS	UNIT
Module Size	159.33L×49.8W×6.3H	mm
View Area	137.65×35.89	mm
Effective Area	256×64	dots
Pixel Size	0.28×0.28	mm
Pixel Pitch	0.30×0.30	mm

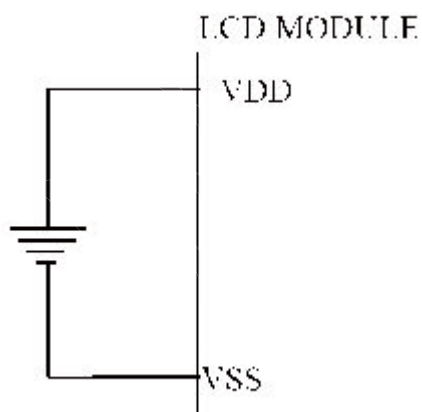
3. EXTERNAL DIMENSIONS



4. BLOCK DIAGRAM



5. POWER SUPPLY



6. PIN DESCRIPTION

Parallel Interface(8080): (R18,R21 USE; R19,R20 NO USE)

ITEM	SYMBOL	LEVEL	FUNCTION
1	GND	0V	Power Ground
2	VDD	+3.3~+5.0V	Power Supply For Logic
3	NC	-	No connect
4~11	D0~D7	H/L	Data Bus

12	RD	H/L	8080: Active LOW Read signal
13	WR	H/L	8080:Active LOW Write signal
14	D/C(RS)	H/L	H: Data L: Command
15	/RST	H/L	Active LOW Reset signal
16	/CS	L	Chip Select

Parallel Interface(6800): (R18,R20 USE; R19,R21 NO USE)

ITEM	SYMBOL	LEVEL	FUNCTION
1	GND	0V	Power Ground
2	VDD	+3.3~+5.0V	Power Supply For Logic
3	NC	-	No connect
4~11	D0~D7	H/L	Data Bus
12	RD	H/L	6800:Operation enable signal. Falling edge triggered.
13	WR	H/L	6800:Read/Write select signal, R/W=1: Read R/W: =0: Write
14	D/C(RS)	H/L	H: Data L: Command
15	/RST	H/L	Active LOW Reset signal
16	/CS	L	Chip Select

4-SPI: (R19,R21 USE; R18,R20 NO USE)

ITEM	SYMBOL	LEVEL	FUNCTION
1	GND	0V	Power Ground
2	VDD	+3.3~+5.0V	Power Supply For Logic
3	NC	-	No connect
4	SCLK(D0)	H/L	Serial Clock signal
5	SDIN(D1)	H/L	Serial Data input signal
6	NC(D2)	-	No connect
7~11	D3~D7	0V	Power Ground
12	RD	0V	Power Ground
13	WR	0V	Power Ground
14	D/C(RS)	H/L	H: Data L: Command
15	/RST	H/L	Active LOW Reset signal
16	/CS	L	Chip Select

3-SPI : (R19,R20 USE; R18,R21 NO USE)

ITEM	SYMBOL	LEVEL	FUNCTION
1	GND	0V	Power Ground
2	VDD	+3.3~+5.0V	Power Supply For Logic
3	NC	-	No connect

4	SCLK(D0)	H/L	Serial Clock signal
5	SDIN(D1)	H/L	Serial Data input signal
6	NC(D2)	-	No connect
7~11	D3~D7	0V	Power Ground
12	RD	0V	Power Ground
13	WR	0V	Power Ground
14	D/C(RS)	0V	Power Ground
15	/RST	H/L	Active LOW Reset signal
16	/CS	L	Chip Select

MCU Interface assignment under different bus interface mode:

Pin Name Bus Interface	Data/Command Interface								Control Signal				
	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W#	CS#	D/C#	RES#
8-bit 8080	D[7:0]								RD#	WR#	CS#	D/C#	RES#
8-bit 6800	D[7:0]								E	R/W#	CS#	D/C#	RES#
3-wire SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		CS#	Tie LOW	RES#
4-wire SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		CS#	D/C#	RES#

7. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V _{dd}	3.3	5	V	1, 2
Supply Voltage for Display	V _{cc}	0	15	V	1, 2
Operating Temperature	T _{op}	-40	85	°C	-
Storage Temperature	T _{st}	-45	90	°C	-

Note 1: All the above voltages are on the basis of “VSS = 0V”.

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3.

“Optics & Electrical Characteristics”. If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

8. ELECTRICAL CHARACTERISTICS

Items	Symbol	Condition	Min	TY	Max	Unit
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				P		
Operating Temperature Range	Top	Absolute Max	-40	—	+85	C
Storage Temperature Range	Tst	Absolute Max	-45	—	+90	C
Supply Voltage	Vdd		2.8	3.0	3.3	V
Supply Current (logic)	Idd	Ta=25°C, VDD=3.3V	—	180	300	μA
Supply Current (display)	ICC	50% ON, VDD=3.3V	—	62	70	mA
		100% ON, VDD=3.3V	—	113	120	mA
Sleep Mode Current	IDD+ICCS LEEP		—	3	15	μA
“H” Level input	Vih		0.8*VDD	—	VDD	V
“L” Level input	Vil		VSS	—	0.2*VDD	V
“H” Level output	Voh		0.9*VDD	—	VDD	V
“L” Level output	Vol		VSS	—	0.1*VDD	V

9 . Optical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Viewing Angle – Top	AV		—	80	—	
Viewing Angle – Bottom	AV		—	80	—	
Viewing Angle – Left	AH		—	80	—	
Viewing Angle – Right	AH		—	80	—	
Contrast Ratio	Cr		2000:1	—	—	—
Response Time (rise)	Tr	—	—	10	—	us
Response Time (fall)	Tf	—	—	10	—	us
Brightness		50% checkerboard	100	120	—	cd/m2
Lifetime		Ta=25°C, 50% checkerboard	10,000	—	—	Hrs

Note: Lifetime at typical temperature is based on accelerated high - temperature operation. Lifetime is tested at average 50% pixels on and is rated as Hours until Half - Brightness. The Display OFF command can be used to extend the lifetime of the display.

Luminance of active pixels will degrade faster than inactive pixels. Residual (burn - in) images may occur. To avoid this, every pixel should be illuminated uniformly.

10. COMMAND TABLE

Built - in SSD1322 controller.



SSD1322

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0	00	0	0	0	0	0	0	0	0	Enable Gray Scale table	This command is sent to enable the Gray Scale table setting (command B8h)
0 1 1	15 A[6:0] B[6:0]	0 * *	0 A ₆ B ₆	0 A ₅ B ₅	1 A ₄ B ₄	0 A ₃ B ₃	1 A ₂ B ₂	0 A ₁ B ₁	1 A ₀ B ₀	Set Column Address	Set Column start and end address A[6:0]: Start Address. [reset=0] B[6:0]: End Address. [reset=119] Range from 0 to 119
0	5C	0	1	0	1	1	1	0	0	Write RAM Command	Enable MCU to write Data into RAM
0	5D	0	1	0	1	1	1	0	1	Read RAM Command	Enable MCU to read Data from RAM
0 1 1	75 A[6:0] B[6:0]	0 * *	1 A ₆ B ₆	1 A ₅ B ₅	1 A ₄ B ₄	0 A ₃ B ₃	1 A ₂ B ₂	0 A ₁ B ₁	1 A ₀ B ₀	Set Row Address	Set Row start and end address A[6:0]: Start Address. [reset=0] B[6:0]: End Address. [reset=127] Range from 0 to 127
0 1 1	A0 A[7:0] B[4]	1 0 *	0 0 *	1 A ₅ 0	0 A ₄ B ₄	0 0 0	0 A ₂ 0	0 A ₁ 0	0 A ₀ 1	Set Re-map and Dual COM Line mode	A[0]=0b, Horizontal address increment [reset] A[0]=1b, Vertical address increment A[1]=0b, Disable Column Address Re-map [reset] A[1]=1b, Enable Column Address Re-map A[2]=0b, Disable Nibble Re-map [reset] A[2]=1b, Enable Nibble Re-map A[4]=0b, Scan from COM0 to COM[N-1] [reset] A[4]=1b, Scan from COM[N-1] to COM0, where N is the Multiplex ratio A[5]=0b, Disable COM Split Odd Even [reset] A[5]=1b, Enable COM Split Odd Even B[4], Enable / disable Dual COM Line mode 0b, Disable Dual COM mode [reset] 1b, Enable Dual COM mode (MUX ≤ 63) Note ⁽¹⁾ COM Split Odd Even mode must be disabled (A[5]=0b) when enabling the Dual COM mode (B[4]=1b) Details refer to Section 10.1.6
0 1	A1 A[6:0]	1 *	0 A ₆	1 A ₅	0 A ₄	0 A ₃	0 A ₂	0 A ₁	1 A ₀	Set Display Start Line	Set display RAM display start line register from 0-127 Display start line register is reset to 00h after RESET

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description																																		
0 1	A2 A[6:0]	1 *	0 A ₆	1 A ₅	0 A ₄	0 A ₃	0 A ₂	1 A ₁	0 A ₀	Set Display Offset	Set vertical scroll by COM from 0-127 The value is reset to 00H after RESET																																		
0	A4~A7	1	0	1	0	0	X ₂	X ₁	X ₀	Set Display Mode	A4h = Entire Display OFF, all pixels turns OFF in GS level 0 A5h = Entire Display ON, all pixels turns ON in GS level 15 A6h = Normal Display [reset] A7h = Inverse Display (GS0 → GS15, GS1 → GS14, GS2 → GS13, ...)																																		
0 1 1	A8 A[6:0] B[6:0]	1 0 0	0 A ₆ B ₆	1 A ₅ B ₅	0 A ₄ B ₄	1 A ₃ B ₃	0 A ₂ B ₂	0 A ₁ B ₁	0 A ₀ B ₀	Enable Partial Display	This command turns ON partial mode. The partial mode display area is defined by the following two parameters, A[6:0]: Address of start row in the display area B[6:0]: Address of end row in the display area, where B[6:0] must be ≥ A[6:0]																																		
0	A9	1	0	1	0	1	0	0	1	Exit Partial Display	This command is sent to exit the Partial Display mode																																		
0 1	AB A[0]	1 0	0 0	1 0	0 0	1 0	0 0	1 0	1 A ₀	Function Selection	A[0]=0b, Select external V _{DD} A[0]=1b, Enable internal V _{DD} regulator [reset]																																		
0	AE~AF	1	0	1	0	1	1	1	X ₀	Set Sleep mode ON/OFF	AEh = Sleep mode ON (Display OFF) AFh = Sleep mode OFF (Display ON)																																		
0 1	B1 A[7:0]	1 A ₇	0 A ₆	1 A ₅	1 A ₄	0 A ₃	0 A ₂	0 A ₁	1 A ₀	Set Phase Length	A[3:0] Phase 1 period (reset phase length) of 5~31 DCLK(s) clocks as follow: <table border="1"><thead><tr><th>A[3:0]</th><th>Phase 1 period</th></tr></thead><tbody><tr><td>0000</td><td>invalid</td></tr><tr><td>0001</td><td>invalid</td></tr><tr><td>0010</td><td>5 DCLKs</td></tr><tr><td>0011</td><td>7 DCLKs</td></tr><tr><td>0100</td><td>9 DCLKs [reset]</td></tr><tr><td>:</td><td>:</td></tr><tr><td>1111</td><td>31 DCLKs</td></tr></tbody></table> A[7:4] Phase 2 period (first pre-charge phase length) of 3~15 DCLK(s) clocks as follow: <table border="1"><thead><tr><th>A[7:4]</th><th>Phase 2 period</th></tr></thead><tbody><tr><td>0000</td><td>invalid</td></tr><tr><td>0001</td><td>invalid</td></tr><tr><td>0010</td><td>invalid</td></tr><tr><td>0011</td><td>3 DCLKs</td></tr><tr><td>:</td><td>:</td></tr><tr><td>0111</td><td>7 DCLKs [reset]</td></tr><tr><td>:</td><td>:</td></tr><tr><td>1111</td><td>15 DCLKs</td></tr></tbody></table>	A[3:0]	Phase 1 period	0000	invalid	0001	invalid	0010	5 DCLKs	0011	7 DCLKs	0100	9 DCLKs [reset]	:	:	1111	31 DCLKs	A[7:4]	Phase 2 period	0000	invalid	0001	invalid	0010	invalid	0011	3 DCLKs	:	:	0111	7 DCLKs [reset]	:	:	1111	15 DCLKs
A[3:0]	Phase 1 period																																												
0000	invalid																																												
0001	invalid																																												
0010	5 DCLKs																																												
0011	7 DCLKs																																												
0100	9 DCLKs [reset]																																												
:	:																																												
1111	31 DCLKs																																												
A[7:4]	Phase 2 period																																												
0000	invalid																																												
0001	invalid																																												
0010	invalid																																												
0011	3 DCLKs																																												
:	:																																												
0111	7 DCLKs [reset]																																												
:	:																																												
1111	15 DCLKs																																												

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description																										
0	B3	1	0	1	1	0	0	1	1	Set Front Clock Divider / Oscillator Frequency	A[3:0] [reset=0], divide by DIVSET where																										
1	A[7:0]	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		<table><tr><td>A[3:0]</td><td>DIVSET</td></tr><tr><td>0000</td><td>divide by 1</td></tr><tr><td>0001</td><td>divide by 2</td></tr><tr><td>0010</td><td>divide by 4</td></tr><tr><td>0011</td><td>divide by 8</td></tr><tr><td>0100</td><td>divide by 16</td></tr><tr><td>0101</td><td>divide by 32</td></tr><tr><td>0110</td><td>divide by 64</td></tr><tr><td>0111</td><td>divide by 128</td></tr><tr><td>1000</td><td>divide by 256</td></tr><tr><td>1001</td><td>divide by 512</td></tr><tr><td>1010</td><td>divide by 1024</td></tr><tr><td>>=1011</td><td>invalid</td></tr></table>	A[3:0]	DIVSET	0000	divide by 1	0001	divide by 2	0010	divide by 4	0011	divide by 8	0100	divide by 16	0101	divide by 32	0110	divide by 64	0111	divide by 128	1000	divide by 256	1001	divide by 512	1010	divide by 1024	>=1011	invalid
A[3:0]	DIVSET																																				
0000	divide by 1																																				
0001	divide by 2																																				
0010	divide by 4																																				
0011	divide by 8																																				
0100	divide by 16																																				
0101	divide by 32																																				
0110	divide by 64																																				
0111	divide by 128																																				
1000	divide by 256																																				
1001	divide by 512																																				
1010	divide by 1024																																				
>=1011	invalid																																				
										A[7:4] Oscillator frequency, frequency increases as level increases [reset=0101b]																											
0	B4	1	0	1	1	0	1	0	0	Display Enhancement A	A[1:0] = 00b: Enable external VSL																										
1	A[1:0]	1	0	1	0	0	0	A ₁	A ₀		A[1:0] = 10b: Internal VSL [reset]																										
1	B[7:3]	B ₇	B ₆	B ₅	B ₄	B ₃	1	0	1		B[7:3] = 11111b: Enhanced low GS display quality B[7:3] = 10110b: Normal [reset]																										
0	B5	1	0	1	1	0	1	0	1	Set GPIO	A[1:0] GPIO0: 00 pin HiZ, Input disabled 01 pin HiZ, Input enabled 10 pin output LOW [reset] 11 pin output HIGH																										
1	A[3:0]	*	*	*	*	A ₃	A ₂	A ₁	A ₀		A[3:2] GPIO1: 00 pin HiZ, Input disabled 01 pin HiZ, Input enabled 10 pin output LOW [reset] 11 pin output HIGH																										
0	B6	1	0	1	1	0	1	1	0	Set Second Precharge Period	A[3:0] Second Pre-charge period																										
1	A[3:0]	*	*	*	*	A ₃	A ₂	A ₁	A ₀		0000b 0 dclk 0001b 1 dclk 1000b 8 dclks [reset] 1111b 15 dclks																										

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																	
0	B8	1	0	1	1	1	0	0	0	Set Gray Scale Table	The next 15 data bytes define Gray Scale (GS) Table by setting the gray scale pulse width in unit of DCLK's (ranges from 0d ~ 180d)																	
1	A1[7:0]	A1 ₇	A1 ₆	A1 ₅	A1 ₄	A1 ₃	A1 ₂	A1 ₁	A1 ₀		A1[7:0]: Gamma Setting for GS1,																	
1	A2[7:0]	A2 ₇	A2 ₆	A2 ₅	A2 ₄	A2 ₃	A2 ₂	A2 ₁	A2 ₀		A2[7:0]: Gamma Setting for GS2,																	
1	.	.	.	.	.	.	.	.	.		:																	
1	.	.	.	.	.	.	.	.	.		A14[7:0]: Gamma Setting for GS14,																	
1	.	.	.	.	.	.	.	.	.		A15[7:0]: Gamma Setting for GS15																	
1	A14[7:0]	A14 ₇	A14 ₆	A14 ₅	A14 ₄	A14 ₃	A14 ₂	A14 ₁	A14 ₀																			
1	A15[7:0]	A15 ₇	A15 ₆	A15 ₅	A15 ₄	A15 ₃	A15 ₂	A15 ₁	A15 ₀																			
Note ⁽¹⁾ 0 ≤ Setting of GS1 < Setting of GS2 < Setting of GS3..... < Setting of GS14 < Setting of GS15 Refer to Section 8.8 for details ⁽²⁾ The setting must be followed by the Enable Gray Scale Table command (00h)																												
0	B9	1	0	1	1	1	0	0	1	Select Default Linear Gray Scale table	The default Linear Gray Scale table is set in unit of DCLK's as follow GS0 level pulse width = 0; GS1 level pulse width = 0; GS2 level pulse width = 8; GS3 level pulse width = 16; : : GS14 level pulse width = 104; GS15 level pulse width = 112 Refer to Section 8.8 for details																	
1	A[4:0]	*	*	*	A ₄	A ₃	A ₂	A ₁	A ₀																			
0	BB	1	0	1	1	1	0	1	1	Set Pre-charge voltage	Set pre-charge voltage level.[reset = 17h]																	
1	A[4:0]	*	*	*	A ₄	A ₃	A ₂	A ₁	A ₀		<table><tr><th>A[4:0]</th><th>Hex code</th><th>pre-charge voltage</th></tr><tr><td>00000</td><td>00h</td><td>0.20 x V_{CC}</td></tr><tr><td>:</td><td>:</td><td>:</td></tr><tr><td>11111</td><td>1Fh</td><td>0.60 x V_{CC}</td></tr></table>	A[4:0]	Hex code	pre-charge voltage	00000	00h	0.20 x V _{CC}	:	:	:	11111	1Fh	0.60 x V _{CC}					
A[4:0]	Hex code	pre-charge voltage																										
00000	00h	0.20 x V _{CC}																										
:	:	:																										
11111	1Fh	0.60 x V _{CC}																										
0	BE	1	0	1	1	1	1	1	0	Set V _{COMH}	Set COM deselect voltage level [reset = 04h]																	
1	A[2:0]	*	*	*	*	0	A ₂	A ₁	A ₀		<table><tr><th>A[2:0]</th><th>Hex code</th><th>V_{COMH}</th></tr><tr><td>000</td><td>00h</td><td>0.72 x V_{CC}</td></tr><tr><td>:</td><td>:</td><td>:</td></tr><tr><td>100</td><td>04h</td><td>0.80 x V_{CC} [reset]</td></tr><tr><td>:</td><td>:</td><td>:</td></tr><tr><td>111</td><td>07h</td><td>0.86 x V_{CC}</td></tr></table>	A[2:0]	Hex code	V _{COMH}	000	00h	0.72 x V _{CC}	:	:	:	100	04h	0.80 x V _{CC} [reset]	:	:	:	111	07h
A[2:0]	Hex code	V _{COMH}																										
000	00h	0.72 x V _{CC}																										
:	:	:																										
100	04h	0.80 x V _{CC} [reset]																										
:	:	:																										
111	07h	0.86 x V _{CC}																										
0	C1	1	1	0	0	0	0	0	1	Set Contrast Current	A[7:0]: Contrast current value, range:00h~FFh, i.e. 256 steps for I _{SEG} current [reset = 7Fh]																	
1	A[7:0]	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																			

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0 1	C7 A[3:0]	1 *	1 *	0 *	0 *	0 A ₃	1 A ₂	1 A ₁	1 A ₀	Master Contrast Current Control	A[3:0] = 0000b, reduce output currents for all colors to 1/16 0001b, reduce output currents for all colors to 2/16 : 1110b, reduce output currents for all colors to 15/16 1111b, no change [reset]
0 1	CA A[6:0]	1 *	1 A ₆	0 A ₅	0 A ₄	1 A ₃	0 A ₂	1 A ₁	0 A ₀	Set MUX Ratio	A[6:0]: Set MUX ratio from 16MUX ~ 128MUX A[6:0] = 15d represents 16MUX : A[6:0] = 127d represents 128MUX [reset]
0 1 1	D1 A[5:4] 20	1 1 0	1 0 0	0 A ₅ 1	1 A ₄ 0	0 0 0	0 0 0	0 1 0	1 0 0	Display Enhancement B	A[5:4] = 00b: Reserved A[5:4] = 10b: Normal [reset]
0 1	FD A[2]	1 0	1 0	1 0	1 1	1 0	1 A ₂	0 1	1 0	Set Command Lock	A[2]: MCU protection status [reset = 12h] A[2] = 0b, Unlock OLED driver IC MCU interface from entering command [reset] A[2] = 1b, Lock OLED driver IC MCU interface from entering command Note ⁽¹⁾ The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command

Note

⁽¹⁾ “*” stands for “Don’t care”.

For detailed instruction information, see SSD1322 datasheet .

11 . MPU Interface

Table 13-2 : 6800-Series MCU Parallel Interface Timing Characteristics

($V_{DD} - V_{SS} = 2.4$ to $2.6V$, $V_{DDIO} = 1.6V$, $V_{CI} = 3.3V$, $T_A = 25^\circ C$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read)	120	-	-	ns
	Chip Select Low Pulse Width (write)	60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read)	60	-	-	ns
	Chip Select High Pulse Width (write)	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 13-1 : 6800-series MCU parallel interface characteristics

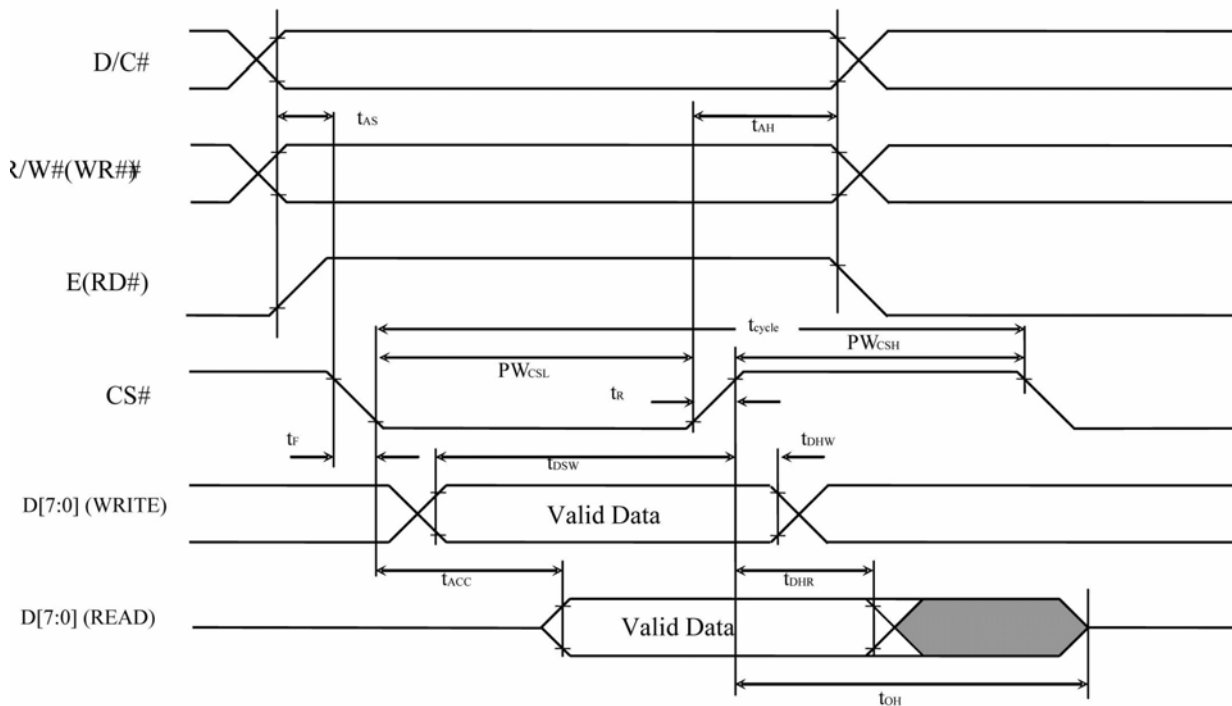


Table 13-3 : 8080-Series MCU Parallel Interface Timing Characteristics

($V_{DD} - V_{SS} = 2.4$ to $2.6V$, $V_{DDIO} = 1.6V$, $V_{CI} = 3.3V$, $T_A = 25^\circ C$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
$t_{PWL R}$	Read Low Time	150	-	-	ns
$t_{PWL W}$	Write Low Time	60	-	-	ns
$t_{PWH R}$	Read High Time	60	-	-	ns
$t_{PWH W}$	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Figure 13-2 : 8080-series MCU parallel interface characteristics

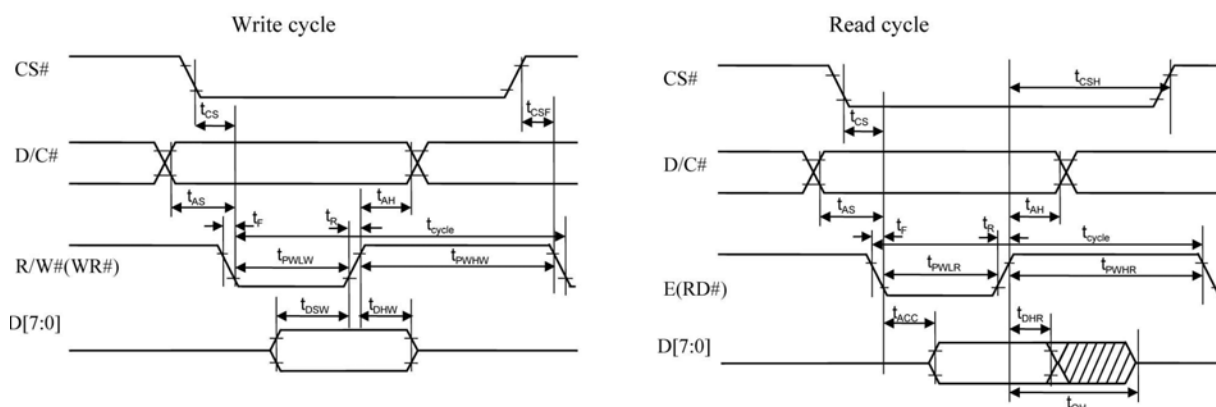


Table 13-4 : Serial Interface Timing Characteristics (4-wire SPI)

($V_{DD} - V_{SS} = 2.4$ to $2.6V$, $V_{DDIO} = 1.6V$, $V_{CI} = 3.3V$, $T_A = 25^{\circ}C$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cyle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 13-3 : Serial interface characteristics (4-wire SPI)

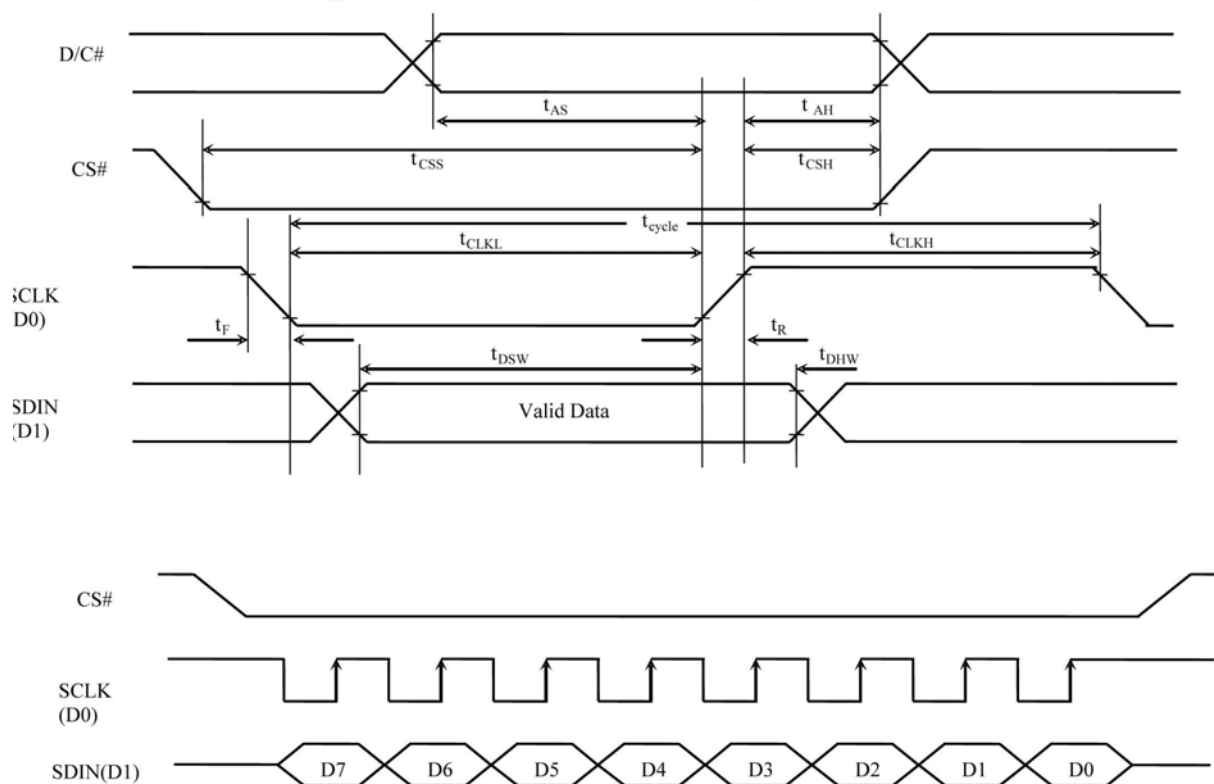
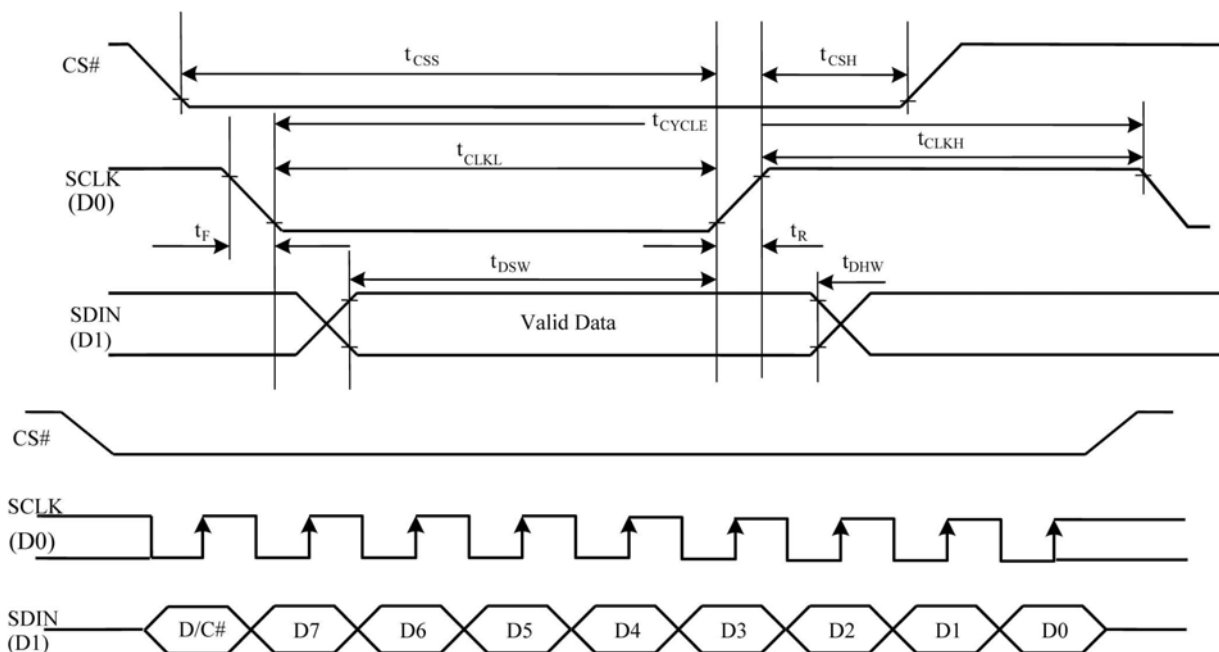


Table 13-5: Serial Interface Timing Characteristics (3-wire SPI)

($V_{DD} - V_{SS} = 2.4$ to $2.6V$, $V_{DDIO} = 1.6V$, $V_{CI} = 3.3V$, $T_A = 25^\circ C$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cyle}	Clock Cycle Time	100	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 13-4: Serial interface characteristics (3-wire SPI)



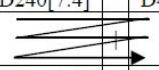
12. GDDRAM

12.1 GDDRAM structure in Gray Scale mode

The GDDRAM address map in Table 8-6 shows the GDDRAM in Gray Scale mode. Since in Gray

Scale mode, there are 16 gray levels. Therefore four bits (one nibble) are allocated for each pixel. For example D30480[3:0] in Table 8-6 corresponds to the pixel located in (COM127, SEG2). So the lower nibble and higher nibble of D0, D1, D2, ..., D30717, D30718, D30719 in Table 8-6 represent the 480x128 data nibbles in the GDDRAM.

Table 8-6 : GDDRAM in Gray Scale mode (RESET)

		SEG0	SEG1	SEG2	SEG3		SEG476	SEG477	SEG478	SEG479	SEG Outputs
		00		00			77		77		RAM Column address (HEX)
COM0	00	D1[3:0]	D1[7:4]	D0[3:0]	D0[7:4]		D239[3:0]	D239[7:4]	D238[3:0]	D238[7:4]	
COM1	01	D241[3:0]	D241[7:4]	D240[3:0]	D240[7:4]		D479[3:0]	D479[7:4]	D478[3:0]	D478[7:4]	
COM126	7E										
COM127	7F	D30481[3:0]	D30481[7:4]	D30480[3:0]	D30480[7:4]		D30719[3:0]	D30719[7:4]	D30718[3:0]	D30718[7:4]	
COM Outputs	RAM Row Address (HEX)										

Corresponding to one pixel

12.2 Data bus to RAM mapping

Table 8-7 : Data bus usage

Read / Write Data		Data bus D[7:0]							
Bus width	Input order	D7	D6	D5	D4	D3	D2	D1	D0
8 bits	1 st	3	3	3	3	2	2	2	2
	2 nd	1	1	1	1	0	0	0	0

Corresponding to one pixel

14 . DESIGN AND HANDING PRECAUTION

14.1 The LCD panel is made by glass. Any mechanical shock (eg. Dropping form high place) will damage the LCD module. Do not add excessive force on the surface of the

display, which may cause the Display color change abnormally.

14.2 The polarizer on the LCD is easily get scratched. If possible, do not remove the LCD protective film until the last step of installation.

14.3 Never attempt to disassemble or rework the LCD module.

14.4 Only Clean the LCD with Isopropyl Alcohol or Ethyl Alcohol. Other solvents (eg. water) may damage the LCD.

14.5 When mounting the LCD module, make sure that it is free from twisting, warping and distortion.

14.6 Ensure to provide enough space(with cushion) between case and LCD panel to prevent external force adding on it, or it may cause damage to the LCD or degrade the display result

14.7 Only hold the LCD module by its side. Never hold LCD module by add force on the heat seal or TAB.

14.8 Never add force to component of the LCD module. It may cause invisible damage or degrade of the reliability.

14.9 LCD module could be easily damaged by static electricity. Be careful to maintain an optimum anti-static work environment to protect the LCD module.

14.10 When peeling of the protective film from LCD, static charge may cause abnormal display pattern. It is normal and will resume to normal in a short while.

14.11 Take care and prevent get hurt by the LCD panel edge.

14.12 Never operate the LCD module exceed the absolute maximum ratings.

14.13 Keep the signal line as short as possible to prevent noisy signal applying to LCD module.

14.14 Never apply signal to the LCD module without power supply.

14.15 IC chip (eg. TAB or COG) is sensitive to the light. Strong lighting environment could possibly cause malfunction. Light sealing structure casing is recommend.

14.16 LCD module reliability may be reduced by temperature shock.

14.17 When storing the LCD module, avoid exposure to the direct sunlight, high humidity, high temperature or low temperature. They may damage or degrade the LCD module

The Following User Manual is for 5.5" 256*64 OLED Panel

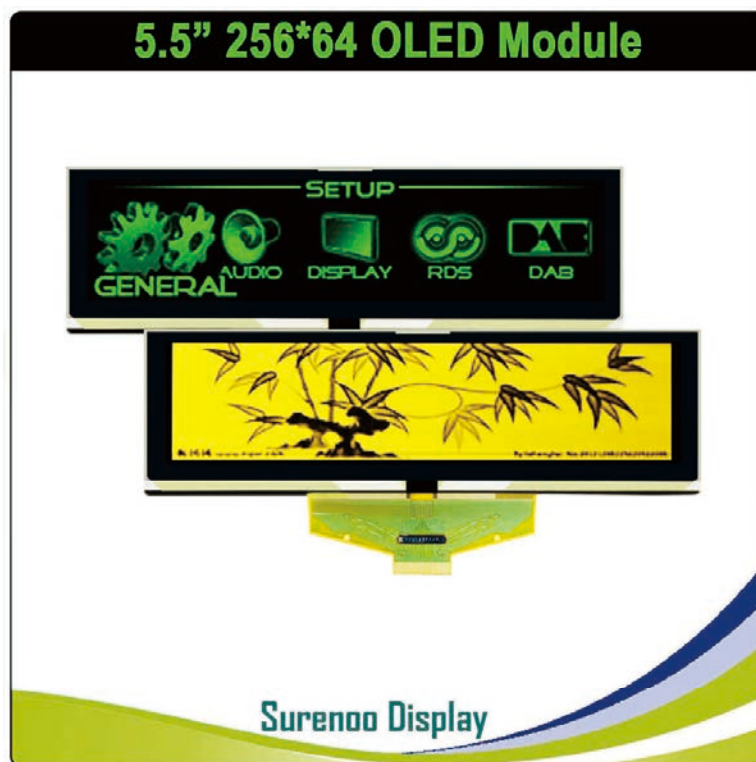
Product Specification

(Preliminary)

Part Name: OEL Display Module

Part ID: UG-5664ASGGF01 / 5664ASYGF01

Doc No.: SAS1-E024-A



Part Number	Revision	Revision Content	Revised on
UG-5664ASGGF01	A	New	August 25, 2009

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1. Basic Specifications

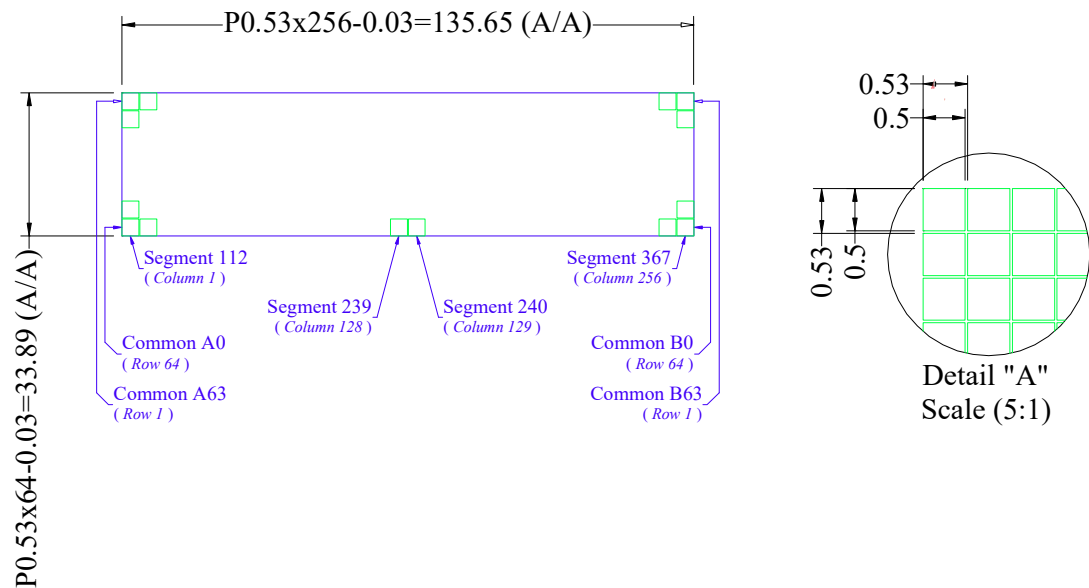
1.1 Display Specifications

- 1) Display Mode: Passive Matrix
- 2) Display Color: Monochrome (Green(Yellow)) / 16 Gray Scales)
- 3) Drive Duty: 1/64 Duty

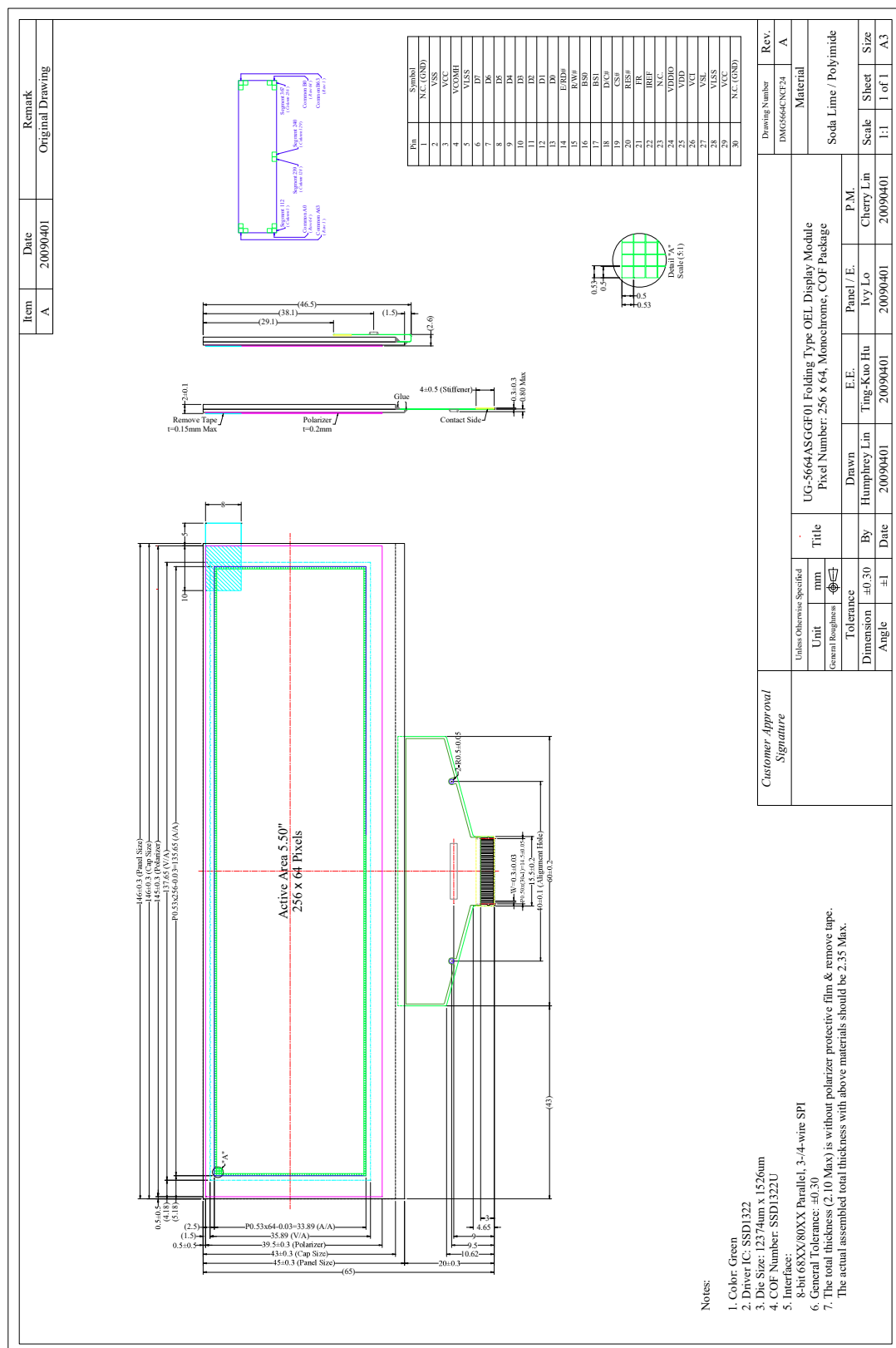
1.2 Mechanical Specifications

- 1) Outline Drawing: According to the annexed outline drawing
- 2) Number of Pixels: 256×64
- 3) Panel Size: $146.00 \times 45.00 \times 2.00$ (mm)
- 4) Active Area: 135.65×33.89 (mm)
- 5) Pixel Pitch: 0.53×0.53 (mm)
- 6) Pixel Size: 0.50×0.50 (mm)
- 7) Weight: 27.1 (g)

1.3 Active Area & Pixel Construction



1.4 Mechanical Drawing



1.5 Pin Definition

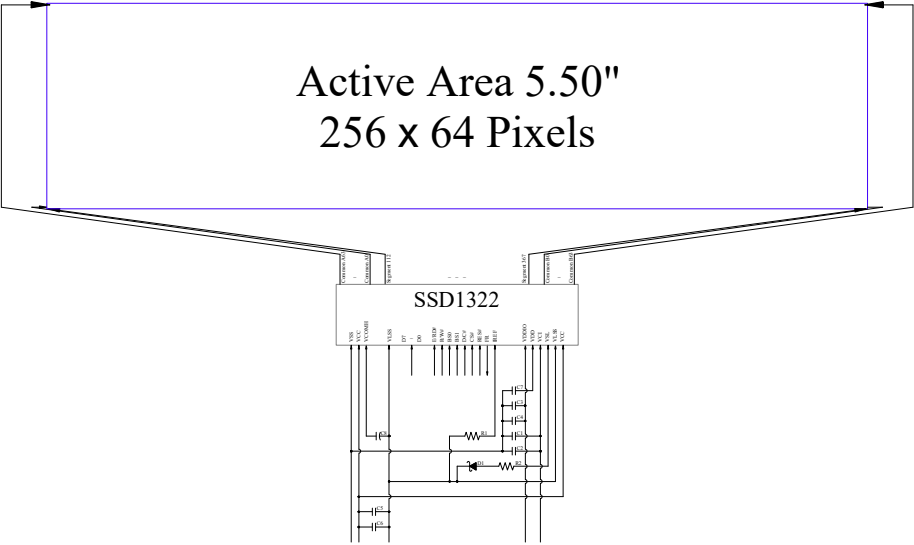
Pin Number	Symbol	Type	Function
Power Supply			
26	VCI	P	Power Supply for Operation This is a voltage supply pin. It must be connected to external source & always be equal to or higher than VDD & VDDIO.
25	VDD	P	Power Supply for Core Logic Circuit This is a voltage supply pin. It can be supplied externally (within the range of 2.4~2.6V) or regulated internally from VCI. A capacitor should be connected between this pin & VSS under all circumstances.
24	VDDIO	P	Power Supply for I/O Pin This pin is a power supply pin of I/O buffer. It should be connected to VDD or external source. All I/O signal should have VIH reference to VDDIO. When I/O signal pins (BS0~BS1, D0~D7, control signals...) pull high, they should be connected to VDDIO.
2	VSS	P	Ground of Logic Circuit This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground.
3, 29	VCC	P	Power Supply for OEL Panel These are the most positive voltage supply pin of the chip. They must be connected to external source.
5, 28	VLSS	P	Ground of Analog Circuit These are the analog ground pins. They should be connected to VSS externally.
Driver			
22	IREF	I	Current Reference for Brightness Adjustment This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current lower than 10uA.
4	VCOMH	P	Voltage Output High Level for COM Signal This pin is the input pin for the voltage output high level for COM signals. A tantalum capacitor should be connected between this pin and VSS.
27	VSL	P	Voltage Output Low Level for SEG Signal This is segment voltage reference pin. When external VSL is not used, this pin should be left open. When external VSL is used, this pin should connect with resistor and diode to ground.
Testing Pads			
21	FR	O	Frame Frequency Triggering Signal This pin will send out a signal that could be used to identify the driver status. Nothing should be connected to this pin. It should be left open individually.

1.5 Pin Definition (Continued)

Pin Number	Symbol	I/O	Function		
<i>Interface</i>					
16 17	BS0 BS1	I	<i>Communicating Protocol Select</i> These pins are MCU interface selection input. See the following table:		
				BS0	BS1
			3-wire SPI	1	0
			4-wire SPI	0	0
			8-bit 68XX Parallel	1	1
			8-bit 80XX Parallel	0	1
20	RES#	I	<i>Power Reset for Controller and Driver</i> This pin is reset signal input. When the pin is low, initialization of the chip is executed.		
19	CS#	I	<i>Chip Select</i> This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.		
18	D/C#	I	<i>Data/Command Control</i> This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.		
14	E/RD#	I	<i>Read/Write Enable or Read</i> This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low. When serial mode is selected, this pin must be connected to VSS.		
15	R/W#	I	<i>Read/Write Select or Write</i> This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to “High” for read mode and pull it to “Low” for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low. When serial mode is selected, this pin must be connected to VSS.		
6~13	D7~D0	I/O	<i>Host Data Input/Output Bus</i> These pins are 8-bit bi-directional data bus to be connected to the microprocessor’s data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. Unused pins must be connected to VSS except for D2 in serial mode.		

1.5 Pin Definition (Continued)

Pin Number	Symbol	I/O	Function
<i>Reserve</i>			
23	N.C.	-	<i>Reserved Pin</i> The N.C. pin between function pins are reserved for compatible and flexible design.
1, 30	N.C. (GND)	-	<i>Reserved Pin (Supporting Pin)</i> The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground.



MCU Interface Selection: BS0 and BS1
Pins connected to MCU interface: D7~D0, E/RD#, R/W#, D/C#, CS#, and RES#

C1, C3, C5: 0.1 μ F
C2, C4: 4.7 μ F
C6: 20 μ F
C7: 1 F
C8: 4.7 μ F / 25V Tantalum Capacitor
R1: 910k Ω , R1 = (Voltage at IREF – VSS) / IREF
R2: 50 Ω , 1/4W
D1: $\leq$ 1.4V, 0.5W

D1: $\leq 1.4V, 0.5W$

2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Operation	V_{CI}	-0.3	4	V	1, 2
Supply Voltage for Logic	V_{DD}	-0.5	2.75	V	1, 2
Supply Voltage for I/O Pins	V_{DDIO}	-0.5	V_{CI}	V	1, 2
Supply Voltage for Display	V_{CC}	-0.5	16	V	1, 2
Operating Current for V_{CC}	I_{CC}	-	80	mA	1, 2
Operating Temperature	T_{OP}	-30	70	°C	-
Storage Temperature	T_{STG}	-40	80	°C	-

Note 1: All the above voltages are on the basis of “VSS = 0V”.

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. “Optics & Electrical Characteristics”. If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

3. Optics & Electrical Characteristics

3.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	With Polarizer (Note 3)	60	80	-	cd/m ²
C.I.E. (Green)	(x) (y)	Without Polarizer	0.27 0.58	0.31 0.62	0.35 0.66	
Dark Room Contrast	CR		-	>2000:1	-	
View Angle			>160	-	-	degree

* Optical measurement taken at $V_{CI} = 2.8V$, $V_{CC} = 15V$.
Software configuration follows Section 4.4 Initialization.

3.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Operation	V_{CI}		2.4	2.8	3.5	V
Supply Voltage for Logic	V_{DD}		2.4	2.5	2.6	V
Supply Voltage for I/O Pins	V_{DDIO}		1.65	1.8	V_{CI}	V
Supply Voltage for Display	V_{CC}	Note 3	14.5	15	15.5	V
High Level Input	V_{IH}		$0.8 \times V_{DDIO}$	-	V_{DDIO}	V
Low Level Input	V_{IL}		0	-	$0.2 \times V_{DDIO}$	V
High Level Output	V_{OH}	$I_{out} = 100\mu A, 3.3MHz$	$0.9 \times V_{DDIO}$	-	V_{DDIO}	V
Low Level Output	V_{OL}	$I_{out} = 100\mu A, 3.3MHz$	0	-	$0.1 \times V_{DDIO}$	V
Operating Current for V_{CI}	I_{CI}		-	1.8	2.25	mA
Operating Current for V_{CC}	I_{CC}	Note 4	-	39.8	49.8	mA
		Note 5	-	64.0	80.0	mA
Sleep Mode Current for V_{CI}	$I_{CI, SLEEP}$		-	1	5	μA
Sleep Mode Current for V_{CC}	$I_{CC, SLEEP}$		-	1	5	μA

Note 3: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.

Note 4: $V_{CI} = 2.8V$, $V_{CC} = 15V$, 50% Display Area Turn on.

Note 5: $V_{CI} = 2.8V$, $V_{CC} = 15V$, 100% Display Area Turn on.

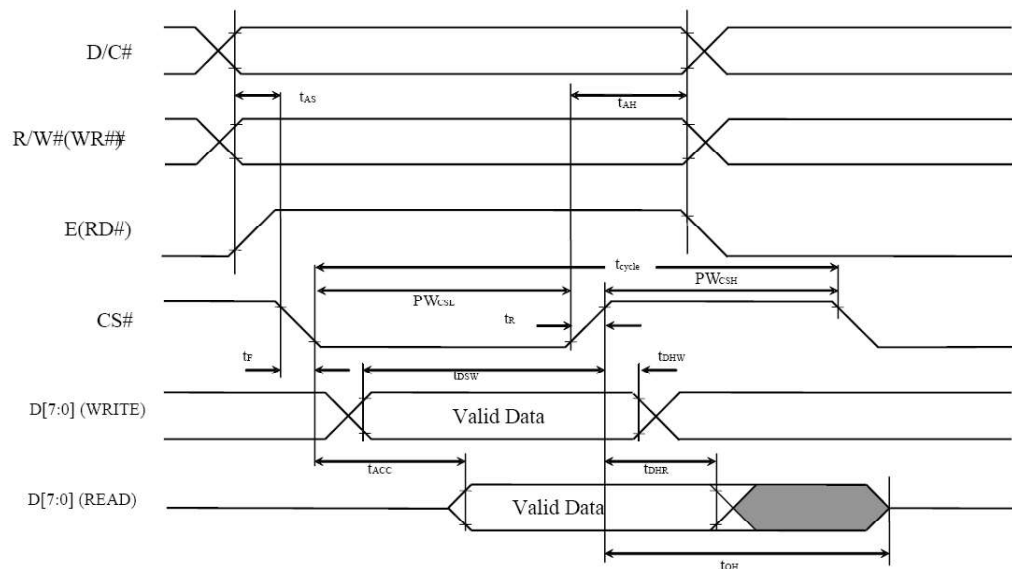
* Software configuration follows Section 4.4 Initialization.

3.3 AC Characteristics

3.3.1 68XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read)	120	-	ns
	Chip Select Low Pulse Width (Write)	60		
PW_{CSH}	Chip Select High Pulse Width (Read)	60	-	ns
	Chip Select High Pulse Width (Write)	60		
t_{R}	Rise Time	-	15	ns
t_{F}	Fall Time	-	15	ns

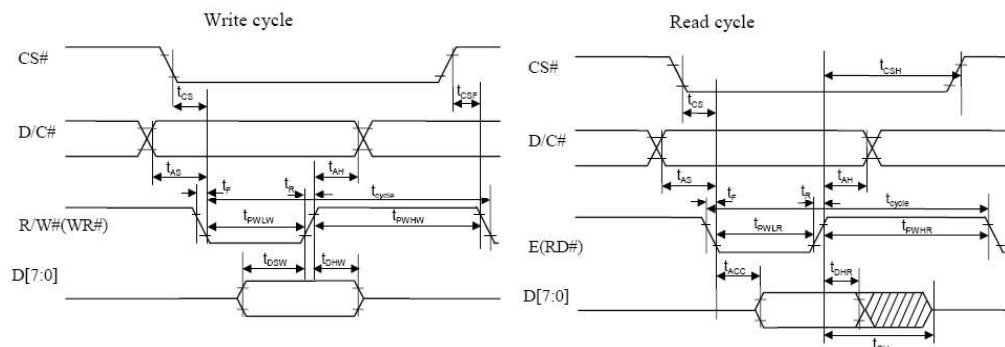
* ($V_{\text{DD}} - V_{\text{SS}} = 2.4\text{V to } 2.6\text{V}$, $V_{\text{DDIO}} = 1.6\text{V}$, $V_{\text{CI}} = 2.8\text{V}$, $T_{\text{a}} = 25^{\circ}\text{C}$)



3.3.2 80XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
t_{PWLR}	Read Low Time	150	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_{R}	Rise Time	-	15	ns
t_{F}	Fall Time	-	15	ns

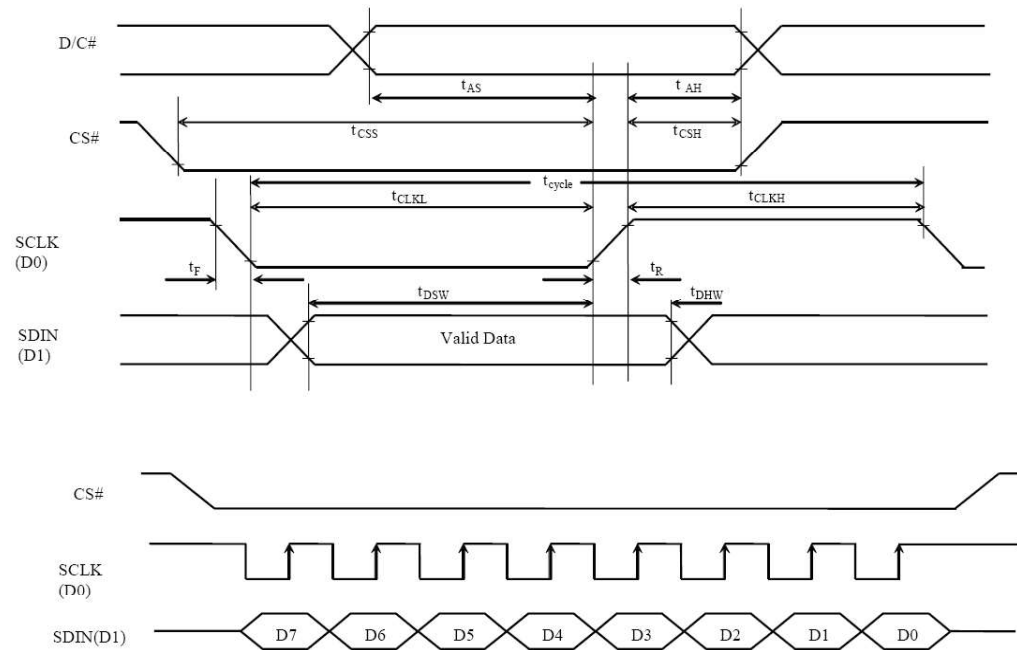
* ($V_{\text{DD}} - V_{\text{SS}} = 2.4\text{V}$ to 2.6V , $V_{\text{DDIO}} = 1.6\text{V}$, $V_{\text{CI}} = 2.8\text{V}$, $T_{\text{a}} = 25^{\circ}\text{C}$)



3.3.3 Serial Interface Timing Characteristics: (4-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_{R}	Rise Time	-	15	ns
t_{F}	Fall Time	-	15	ns

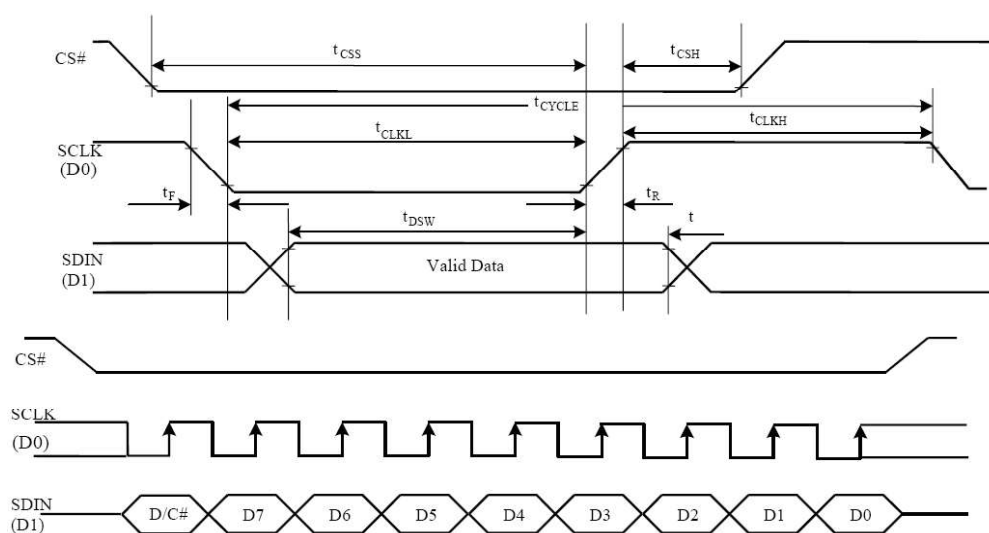
* ($V_{\text{DD}} - V_{\text{SS}} = 2.4\text{V to } 2.6\text{V}$, $V_{\text{DDIO}} = 1.6\text{V}$, $V_{\text{CI}} = 2.8\text{V}$, $T_{\text{a}} = 25^{\circ}\text{C}$)



3.3.4 Serial Interface Timing Characteristics: (3-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_{R}	Rise Time	-	15	ns
t_{F}	Fall Time	-	15	ns

* ($V_{\text{DD}} - V_{\text{SS}} = 2.4\text{V to } 2.6\text{V}$, $V_{\text{DDIO}} = 1.6\text{V}$, $V_{\text{CI}} = 2.8\text{V}$, $T_{\text{a}} = 25^{\circ}\text{C}$)



4. Functional Specification

4.1. Commands

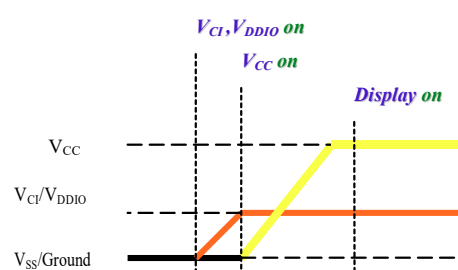
Refer to the Technical Manual for the SSD1322

4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

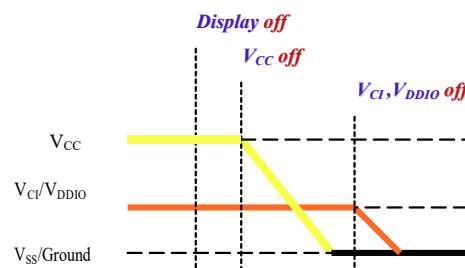
4.2.1 Power up Sequence:

1. Power up V_{CI} & V_{DDIO}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms
(When V_{CC} is stable)
7. Send Display on command



4.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
(When V_{CC} is reach 0 and panel is completely discharges)
4. Power down V_{CI} & V_{DDIO}



4.3 Reset Circuit

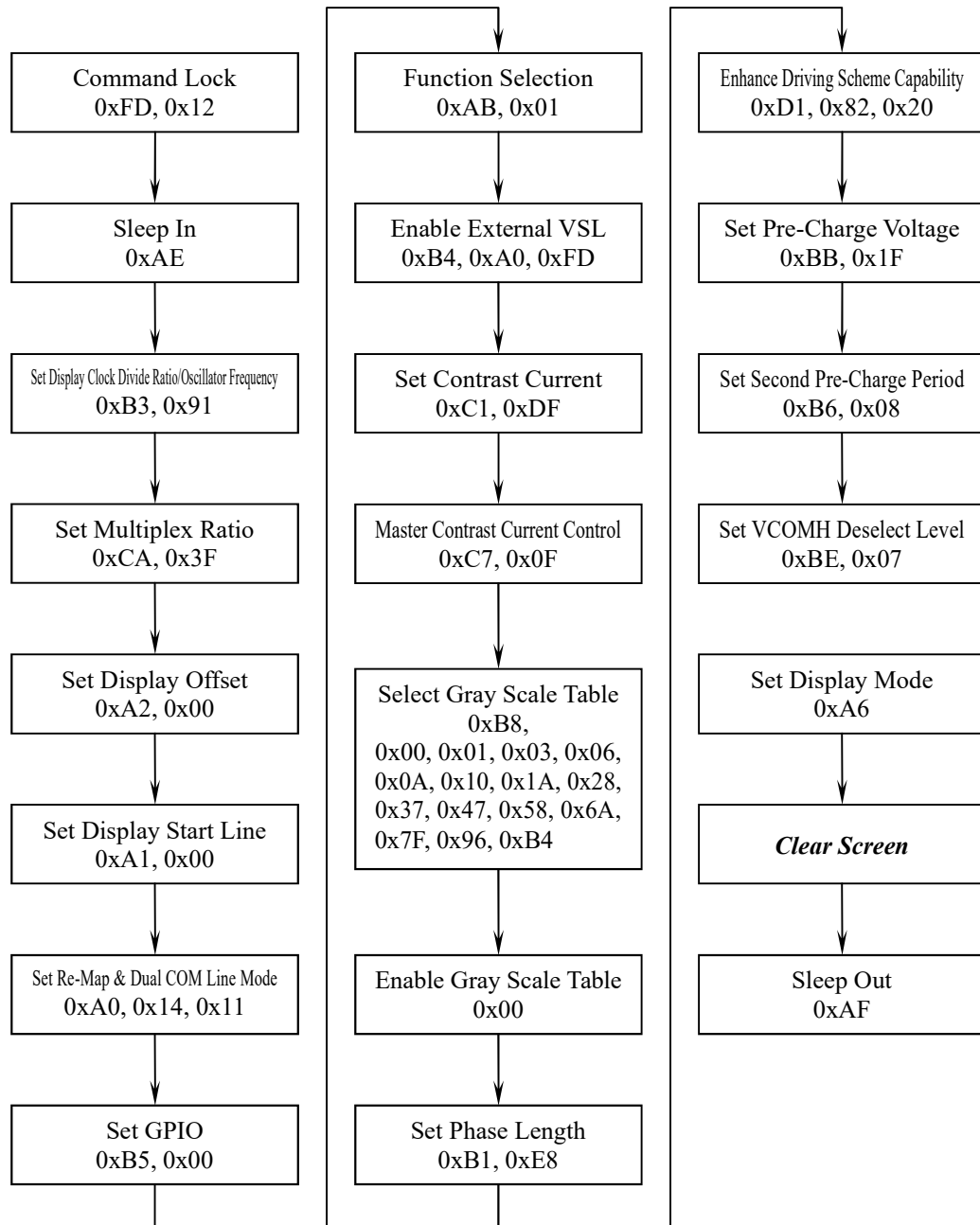
When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 480×128 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Display start line is set at display RAM address 0
5. Column address counter is set at 0
6. Normal scan direction of the COM outputs
7. Contrast control registers is set at 7Fh

4.4 Actual Application Example

Command usage and explanation of an actual example

<Initialization>



If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

5. Reliability

5.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	70°C, 240 hrs	The operational functions work.
Low Temperature Operation	-30°C, 240 hrs	
High Temperature Storage	80°C, 240 hrs	
Low Temperature Storage	-40°C, 240 hrs	
High Temperature/Humidity Storage	60°C, 90% RH, 120 hrs	
Thermal Shock	-40°C $\leftrightarrow$ 85°C, 24 cycles 60 mins dwell	

- * The samples used for the above tests do not include polarizer.
- * No moisture condensation is observed during tests.

5.2 Lifetime

End of lifetime is specified as 50% of initial brightness reached.

Parameter	Min	Max	Unit	Condition	Notes
Operating Life Time	40,000	-	hr	80 cd/m ² , 50% Checkerboard	6

Note 6: The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

5.3 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

6. Outgoing Quality Control Specifications

6.1 Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	$23 \pm 5^{\circ}\text{C}$
Humidity:	$55 \pm 15\% \text{RH}$
Fluorescent Lamp:	30W
Distance between the Panel & Lamp:	$\geq 50\text{ cm}$
Distance between the Panel & Eyes of the Inspector:	$\geq 30\text{ cm}$
Finger glove (or finger cover) must be worn by the inspector.	
Inspection table or jig must be anti-electrostatic.	

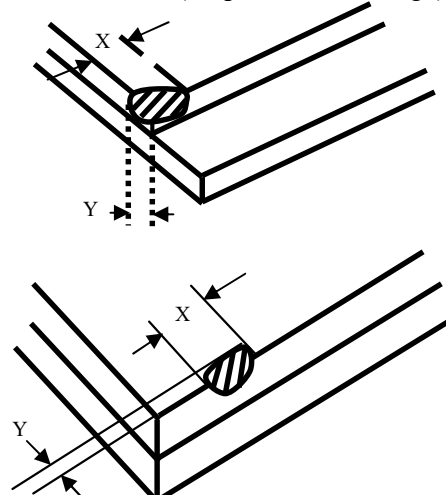
6.2 Sampling Plan

Level II, Normal Inspection, Single Sampling, MIL-STD-105E

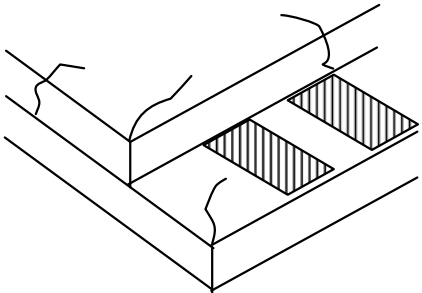
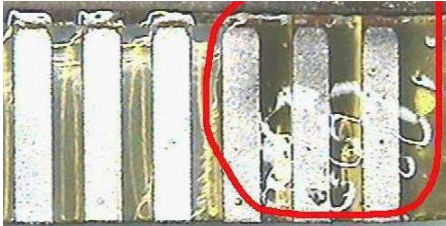
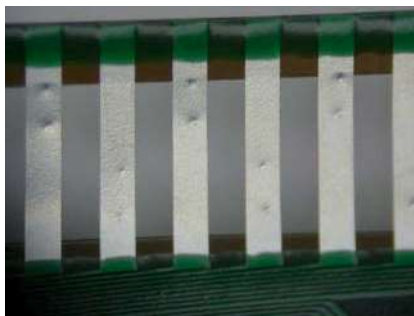
6.3 Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

6.3.1 Cosmetic Check (Display Off) in Non-Active Area

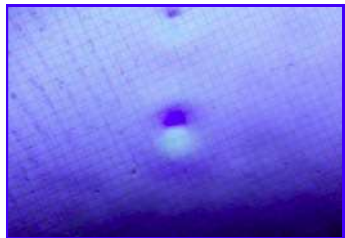
Check Item	Classification	Criteria
Panel General Chipping	Minor	$X > 10\text{ mm}$ (Along with Edge) $Y > 1.5\text{ mm}$ (Perpendicular to edge) 

6.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable.  A 3D perspective diagram of a rectangular panel. A diagonal crack runs across the top surface. Another crack runs along the edge of the panel. A third crack runs across the side surface.
Copper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	 A close-up photograph of a yellow circuit board. A small, circular, white, ring-like defect is visible on the surface, likely representing a hole or damage in the film or trace.
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol)	Minor	 A photograph of several vertical pins or leads. A red circle highlights a specific pin that is covered in a thick, white, irregular substance, likely glue or contamination.
Terminal Lead Prober Mark	Acceptable	 A photograph of several vertical terminal leads. The leads are white and have small, dark, circular marks at the top, which are identified as prober marks.
Ink Marking on Back Side of panel (Exclude on Film)	Acceptable	Ignore for Any

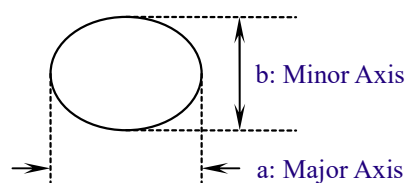
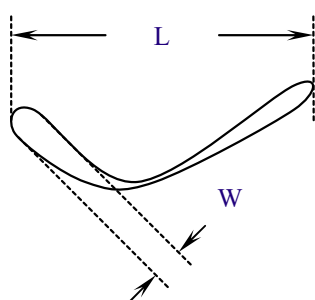
6.3.2 Cosmetic Check (Display Off) in Active Area

It is recommended to execute in clear room environment (class 10k) if actual in necessary.

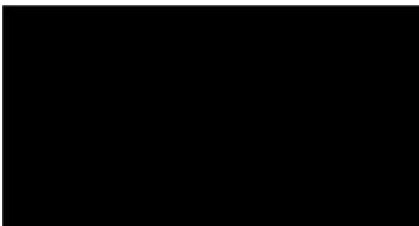
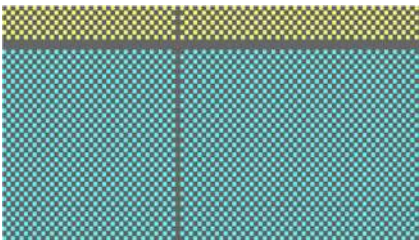
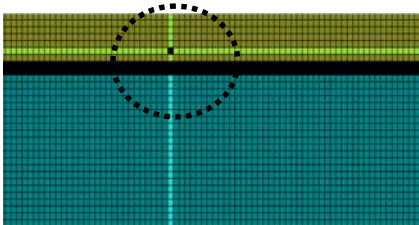
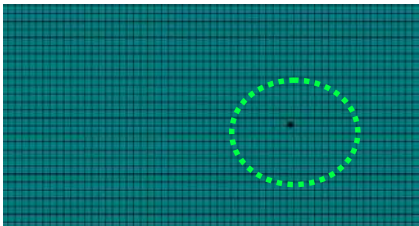
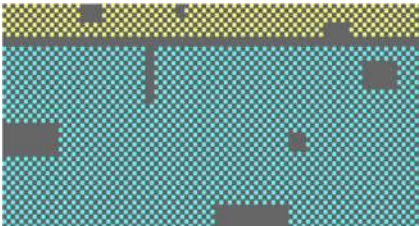
Check Item	Classification	Criteria
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore for not Affect the Polarizer
Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	$W \leq 0.1$ Ignore $W > 0.1, L \leq 2$ $n \leq 1$ $L > 2$ $n = 0$
Dirt, Black Spot, Foreign Material, (On Polarizer)	Minor	$\Phi \leq 0.1$ Ignore $0.1 < \Phi \leq 0.25$ $n \leq 1$ $0.25 < \Phi$ $n = 0$
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	$\Phi \leq 0.5$ → Ignore if no Influence on Display $0.5 < \Phi$ $n = 0$ 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not Allowable

* Protective film should not be tear off when cosmetic check.

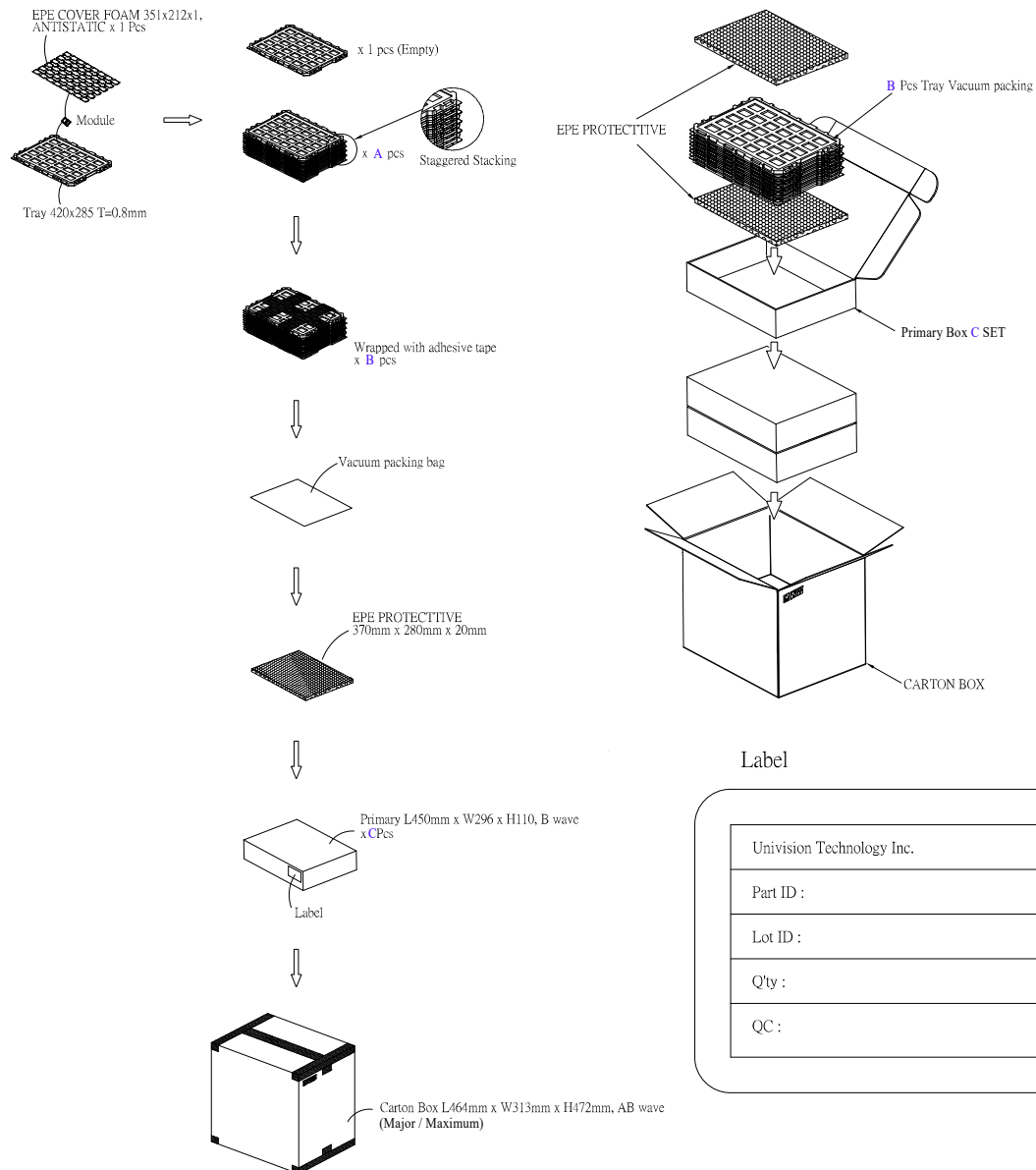
** Definition of W & L & Φ (Unit: mm): $\Phi = (a + b) / 2$



6.3.3 Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	

7. Package Specifications



Item		Quantity	
Holding Trays	(A)	15	per Primary Box
Total Trays	(B)	16	per Primary Box (Including 1 Empty Tray)
Primary Box	(C)	1~4	per Carton (4 as Major / Maximum)

8. Precautions When Using These OEL Display Modules

8.1 Handling Precautions

- 1) Since the display panel is being made of glass, do not apply mechanical impacts such as dropping from a high position.
- 2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
- 3) If pressure is applied to the display surface or its neighborhood of the OEL display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
- 4) The polarizer covering the surface of the OEL display module is soft and easily scratched. Please be careful when handling the OEL display module.
- 5) When the surface of the polarizer of the OEL display module has soil, clean the surface. It takes advantage of by using following adhesion tape.

* Scotch Mending Tape No. 810 or an equivalent

Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.

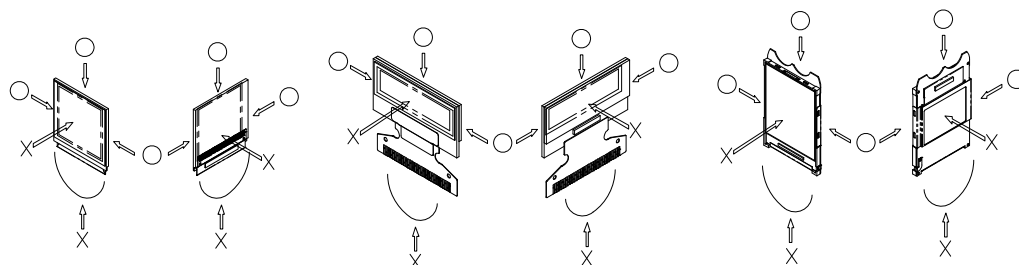
Also, pay attention that the following liquid and solvent may spoil the polarizer:

* Water

* Ketone

* Aromatic Solvents

- 6) Hold OEL display module very carefully when placing OEL display module into the system housing. Do not apply excessive stress or pressure to OEL display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



- 7) Do not apply stress to the LSI chips and the surrounding molded sections.
- 8) Do not disassemble nor modify the OEL display module.
- 9) Do not apply input signals while the logic is off.
- 10) Pay sufficient attention to the working environments when handing OEL display modules to prevent occurrence of element breakage accidents by static electricity.
 - * Be sure to make human body grounding when handling OEL display modules.
 - * Be sure to ground tools to use or assembly such as soldering irons.
 - * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
 - * Protective film is being applied to the surface of the display panel of the OEL display module. Be careful since static electricity may be generated when exfoliating the protective film.
- 11) Protection film is being applied to the surface of the display panel and removes

the protection film before assembling it. At this time, if the OEL display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).

- 12) If electric current is applied when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

8.2 Storage Precautions

- 1) When storing OEL display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps. and, also, avoiding high temperature and high humidity environment or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Univision Technology Inc.)

At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.

- 2) If electric current is applied when water drops are adhering to the surface of the OEL display module, when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

8.3 Designing Precautions

- 1) The absolute maximum ratings are the ratings which cannot be exceeded for OEL display module, and if these values are exceeded, panel damage may be happen.
- 2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
- 3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
- 4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
- 5) As for EMI, take necessary measures on the equipment side basically.
- 6) When fastening the OEL display module, fasten the external plastic housing section.
- 7) If power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.
- 8) The electric potential to be connected to the rear face of the IC chip should be as follows: SSD1322
 - * Connection (contact) to any other potential than the above may lead to rupture of the IC.

8.4 Precautions when disposing of the OEL display modules

- 1) Request the qualified companies to handle industrial wastes when disposing of the OEL display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

8.5 Other Precautions

- 1) When an OEL display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur. Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.
- 2) To protect OEL display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OEL display modules.
 - * Pins and electrodes
 - * Pattern layouts such as the COF
- 3) With this OEL display module, the OEL driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OEL driver is exposed to light, malfunctioning may occur.
 - * Design the product and installation method so that the OEL driver may be shielded from light in actual usage.
 - * Design the product and installation method so that the OEL driver may be shielded from light during the inspection processes.
- 4) Although this OEL display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
- 5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.