A2Z instruction set

15		13	12	11			8	7							0
MICRO_INSTR			8/16	ALU_OP				MICRO_ADDRESS							

MICRO_INSTR							
→ X				X →			
100	0x8	WRITE →X	8b ; X ; DATA	000	0x0	MOVE_TO_C	8b ; X
101	0xA	MOVE_C_TO →X	8b ; X	001	0x2	MOVE_TO_B	8b ; X
110	0xC	COND_WRITE→X	8b ; X ; DATA	010	0x4	ALU (X,B) →C	8b ; OP ; X
111	0xE	COND_MOVE_C_TO →X	8b ; X	011	0x6	ALU_CONS (X, IMM)→C	8b ; OP ; X ; DATA

MICRO_ADDRESS							
Registre	Addr bin	hexa				→X	X →
				8b	16b	MOVE_C_TO WRITE	MOVE_TO_C MOVE_TO_B ALU
(C)					X		
B	(0)1111	0x78	1		X	X	
ext_A	(0)0000	0x00	2	X	X	X	X
ext_B	(0)0001	0x08	2	X	X	X	X
addr_A_H	(0)0101	0x28	3		X	X	
addr_A_L	(0)0100	0x20	4		X	X	
addr_B_H	(0)0111	0x38	5		X	X	
addr_B_L	(0)0110	0x30	6		X	X	
PC_H	(0)1001	0x48	7		X	X	
PC_L	(0)1000	0x40	8		X	X	
CONFIG	(0)1100	0x60	9		X	X	
LOOP COUNTER	(0)1110	0x70	10		X	X	
STATUS	(0)1101	0x68			X		X
CACHE	(1)XXXX		0		X	X	X

ALU_OP → C								
bin	**hex**	**Cond**	**operation**	**bin**	**hex**	**Cond**		
0000	0x0		SUBS X – B → C	1000	0x8	X	X==B	aeb
0001	0x1		ADD X + B → C	1001	0x9	X	X> B	agb
~~0010~~	~~0x2~~		~~SUBS2 B – X →C~~	1010	0xA	X	X>=B	ageb
0011	0x3		MULT_H	1011	0xB	X	X< B	alb
0100	0x4		MULT_L	1100	0xC	X	X<=B	aleb
0101	0x5		DIV_Q	1101	0xD	X	X!=B	aneb
0110	0x6		DIV_R	1110	0xE	X	X AND B	AND
0111	0x7	X	NOT	1111	0xF	X	X OR B	OR

CONFIG register			
7	Not used	3	Increment A + 2
6	Do not write if zero	2	Increment A + 1
5	Increment B + 2	1	Loop counter
4	Increment B + 1	0	Halt

ADDRESSES				
PERIPHERAL	**Read/Write 8bit /16 bits**	**ADDRESS RANGE**		**Details for SRAM**
SRAM (2MB)	R/W 8/16b	5F FF FF … 40 00 00	5F FF FF 50 00 00	Data
			4F FF FF 4E 00 00	Program (other than OS)
			4D FF FF 4D 00 00	FAT (File Allocation Table)
			4C FF FF 4C 00 00	Operating System
			4B 3F 7F 45 A0 00	Frame buffer 2
			45 9F 7F 40 00 00	Frame buffer 1 (default)
Frame selection	W 8b	00 9x xx		
Displayed frame	R 8b	00 8x xx		
GPIO OUT	W 8b	00 7x xx		
GPIO IN	R 8b	00 6x xx		
SPI IN/OUT	R/W 8b	00 5x xx		
Keyboard flag	R 8b	00 3x xx		
Keyboard data	R 8b	00 2x xx		
TEXT (4kB)	W 8b	00 1F FF 00 10 00		
BOOT (2kB)	R 8/16b W 16b	00 07 FF 00 00 00		

RAM TEXT				
	C0	**C1**	**…**	**C79**
L0	00 10 00	00 10 01		00 10 4F
L1	00 10 80	00 10 81		00 10 CF
…				
L28	00 1E 00	00 1E 01		00 1E 4F
L29	00 1E 80	00 1E 81		00 1E CF

RAM GRAPH (frame buffer 1)				
	C0	**C1**	**…**	**C639**
L0	40 00 00	40 00 01		40 02 7F
L1	40 03 00	40 03 01		40 05 7F
…				
L478	45 9A 00	45 9A 01		45 9C 7F
L479	45 9D 00	45 9D 01		45 9F 7F

RAM GRAPH (frame buffer 2)				
	C0	**C1**	**…**	**C639**
L0	45 A0 00	45 A0 01		45 A2 7F
L1	45 A3 00	45 A3 01		45 A5 7F
…				
L478	4B 3A 00	4B 3A 01		4B 3C 7F
L479	4B 3D 00	4B 3D 01		4B 3F 7F