

Sheet: /  
File: logic\_ds1302.sch

**Title:**

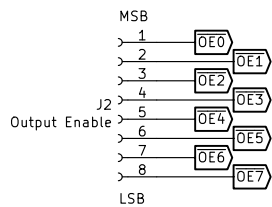
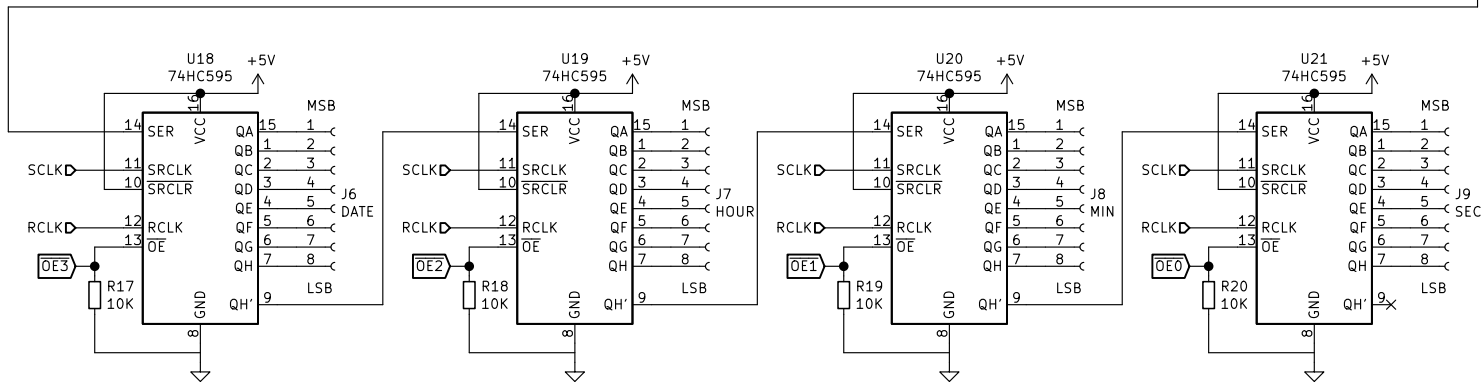
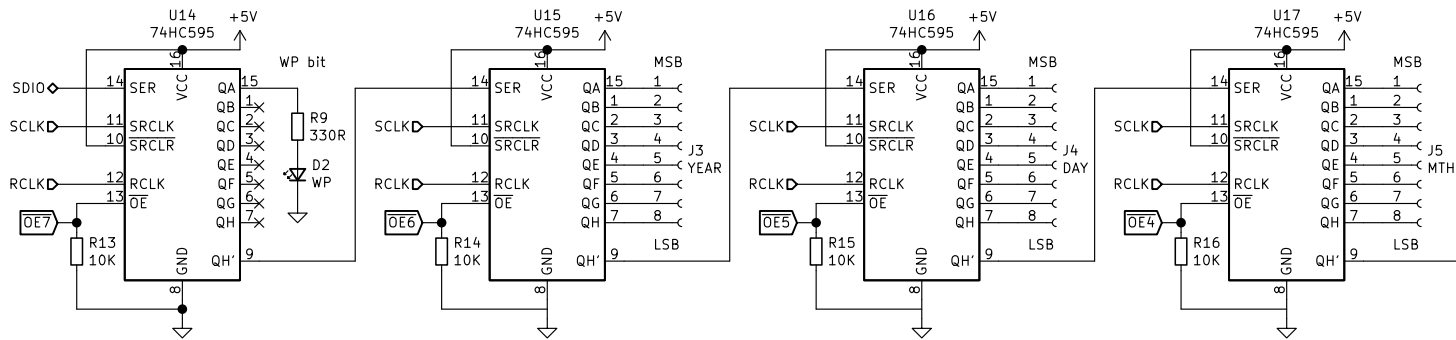
Size: A4

Date:

KiCad E.D.A. kicad (5.1.10)-1

Rev:

Id: 1/7

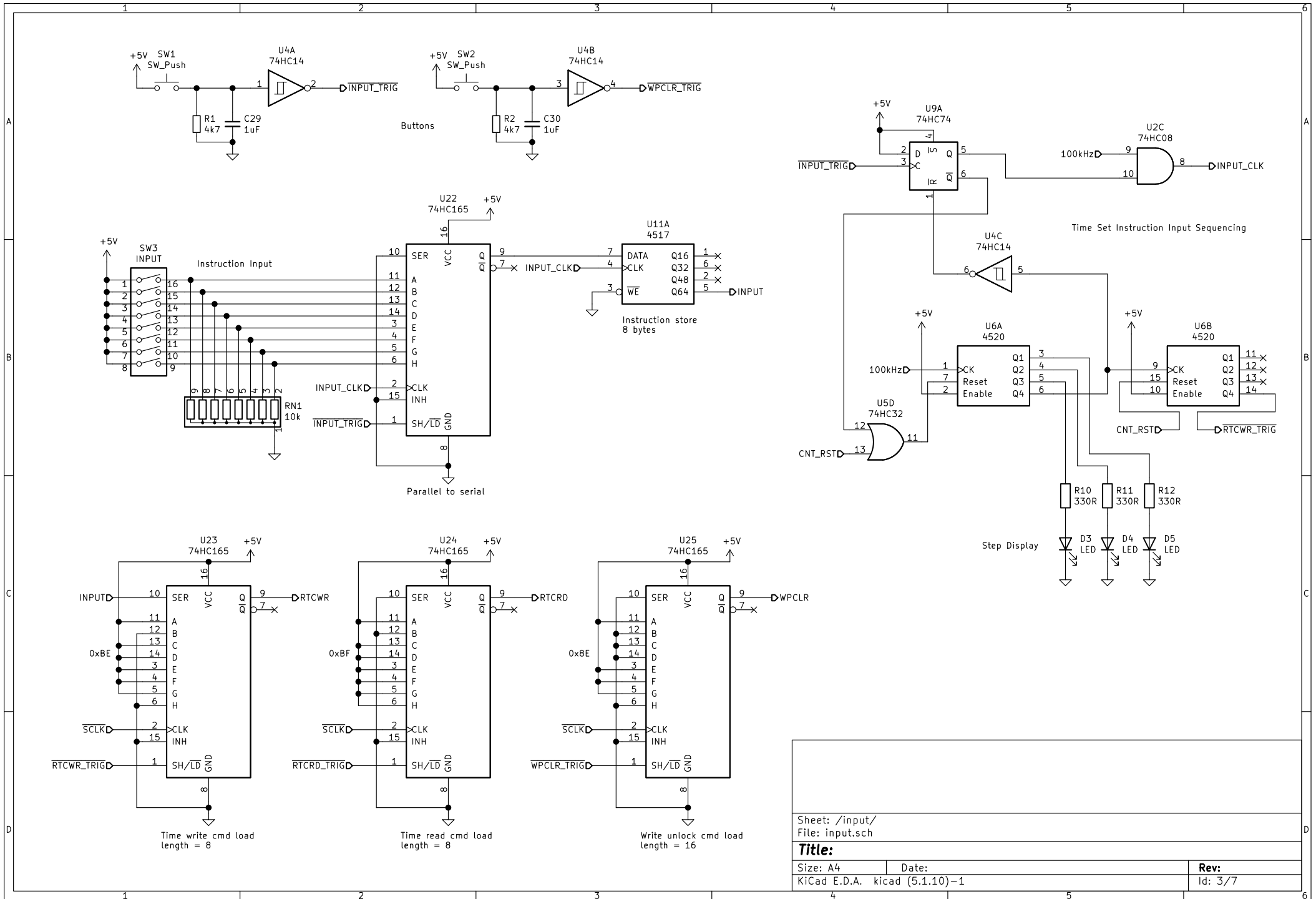


Sheet: /shiftreg/  
File: shiftreg.sch

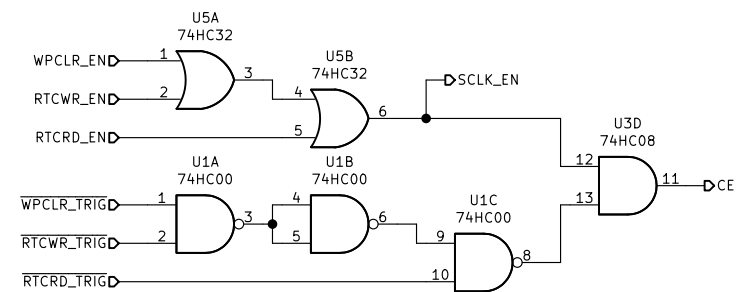
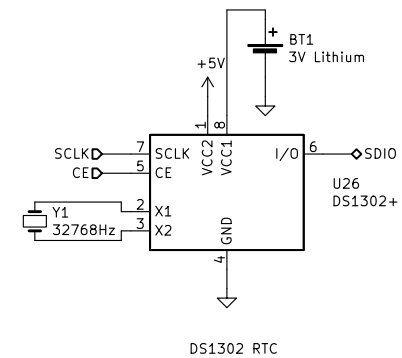
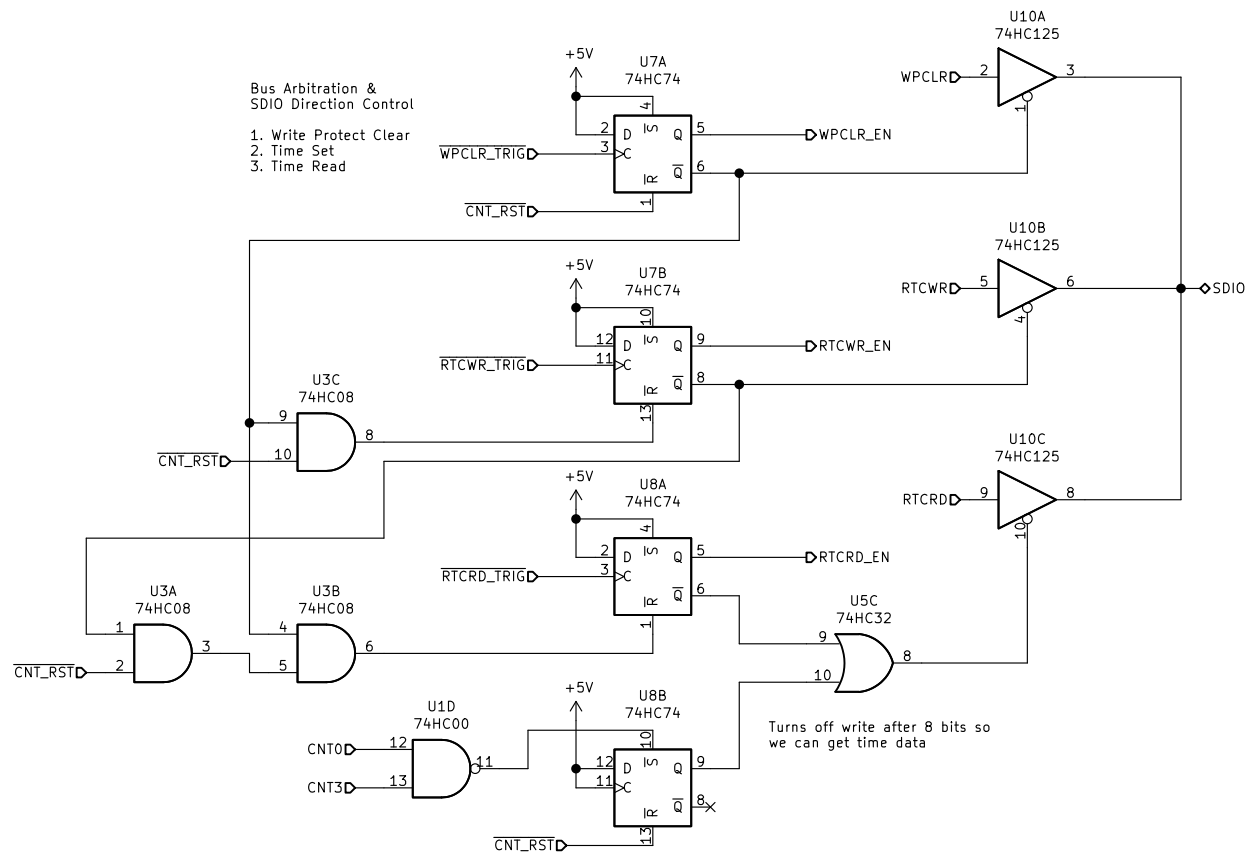
**Title:**

Size: A4 Date:  
KiCad E.D.A. kicad (5.1.10)-1

**Rev:**  
Id: 2/7



Sheet: /input/ File: input.sch	
<b>Title:</b>	
Size: A4	Date:
KiCad E.D.A. kicad (5.1.10)-1	Rev: Id: 3/7



**CE Signal Control**

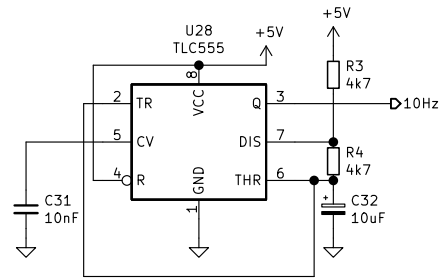
TRIG	EN	OUT	
0	0	0	Trigger in action
0	1	0	Bus arbitration
1	0	0	Idle
1	1	1	I/O operation

Sheet: /ds1302control/  
File: ds1302control.sch

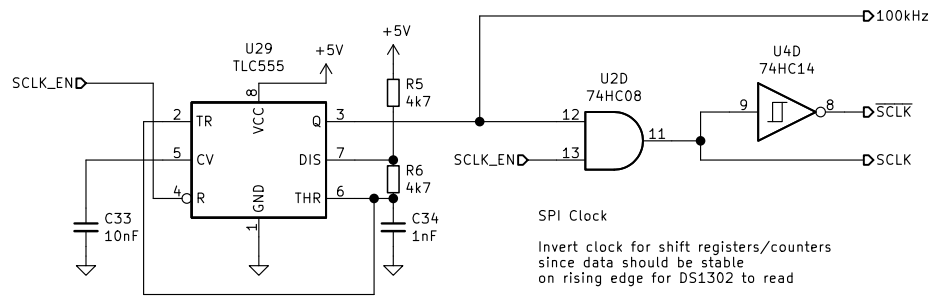
**Title:**

Size: A4 Date:  
KiCad E.D.A. kicad (5.1.10)-1

**Rev:**  
Id: 4/7



Time Read Signal Clock



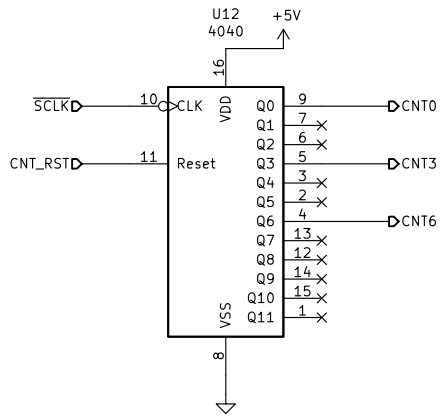
SPI Clock  
 Invert clock for shift registers/counters  
 since data should be stable  
 on rising edge for DS1302 to read

Sheet: /clock/  
 File: clock.sch

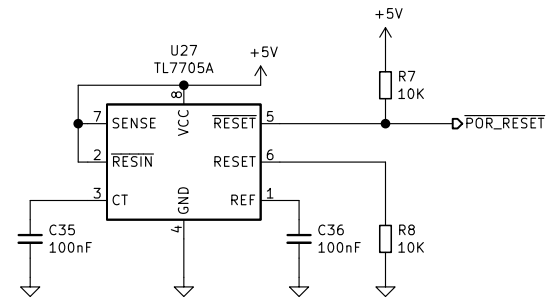
**Title:**

Size: A4 Date:  
 KiCad E.D.A. kicad (5.1.10)-1

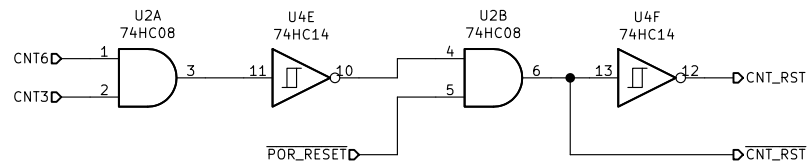
**Rev:**  
 Id: 5/7



I/O Bytes Counter

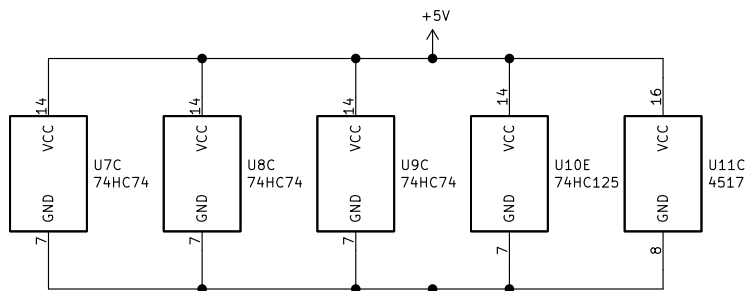
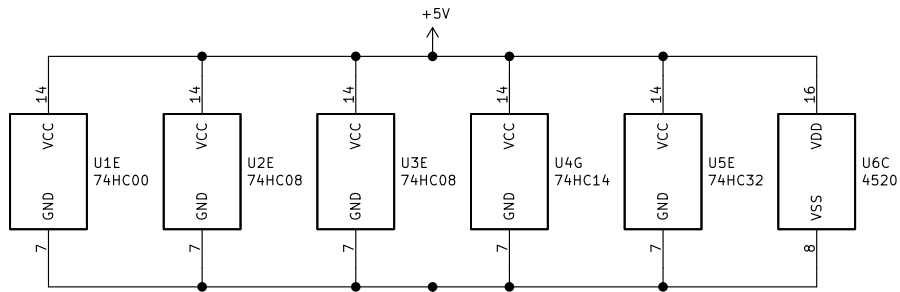


POR Reset 1.3ms

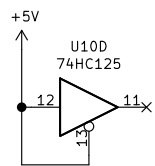
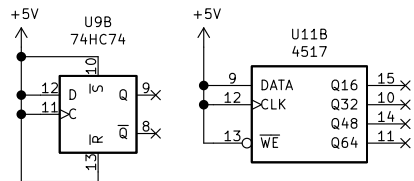


Reset Logic  
 - Reset on counter reaching 72  
 - Reset on POR

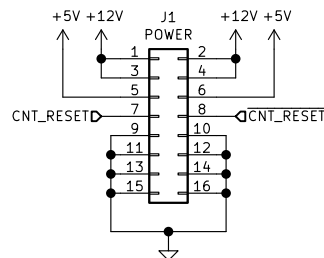
Sheet: /counter/		
File: counter.sch		
<b>Title:</b>		
Size: A4	Date:	Rev:
KiCad E.D.A. kicad (5.1.10)-1		Id: 6/7



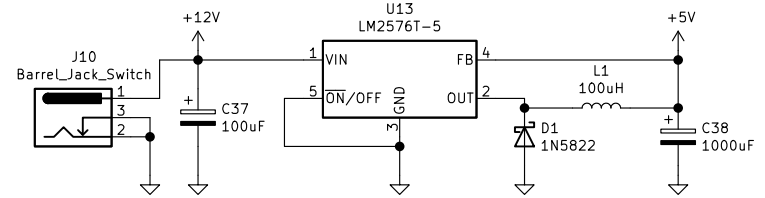
Power Units



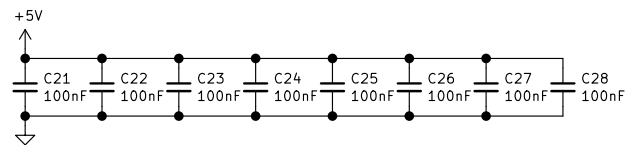
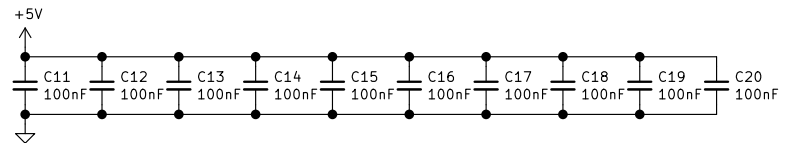
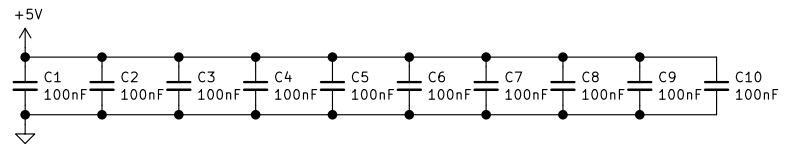
Unused Units



Output Board Connection Header



Buck Converter



Decoupling Capacitors

Sheet: /power/  
File: power.sch

Title:

Size: A4

Date:

KiCad E.D.A. kicad (5.1.10)-1

Rev:

Id: 7/7