# AIM104-COM8

**8 Channel RS232 PC/104 Board**

**Technical Manual**



# Arcom
**www.arcom.com**

a **spectris** company
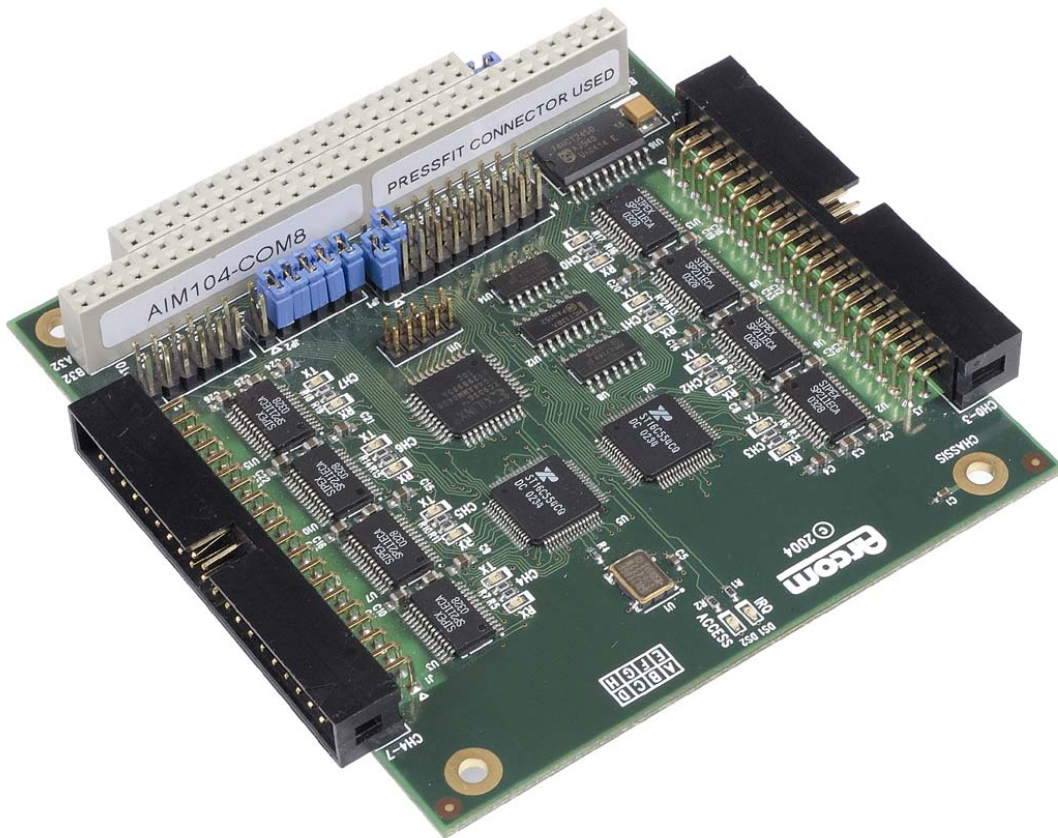
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**Revision History**

| Manual | PCB | Date | Comments |
|--------|-----|------|----------|
| Issue A | V1.1 | 29th September 2004 | First full release of manual. |

For contact details, see page .

Arcom operates a company-wide
quality management system
which has been certified by the
British Standards Institution (BSI)
as compliant with ISO9001:2000

# Contents

# Introduction

The AIM104-COM8 is an 8 or 16-bit PC/104 module that provides up to eight RS232 asynchronous communications channels.

## *Variants*

There is only one standard variant of the this board:

- AIM104-COM8: 8 Channel RS232 PC/104 board.

A four channel version of the board may also be available for volume orders. Please contact the Arcom sales team for information on this variant.

## *Features*

- 8 x 16C550 compatible UART channels.

- Transfer rates up to 115.2Kbaud supported.

- +5V only operation.

- All channels can appear as a block anywhere in I/O address range 000-3FFh.

- First four channels can be individually set as standard PC/AT COM1-4.

- Each QUART (Quad-UART) can drive one link-selectable IRQ in the range 3, 4, 5, 7, 9, 10, 11, 12, 14, 15.

- The two QUART interrupts can be combined to drive one IRQ.

- PC/104 16 bit interface (but can be used in 8-bit slot if IRQ10, 11 and 15 are not required).

- Zero wait state bus operation capability.

- Board access LED.

- Interrupt activity LED.

- TxD/RxD activity indicator LEDs on all channels.

- Power requirements:   220 mA (typical) at +5V DC

- Temperature range:    -20°C (-4°F) to +70°C (158°F) operating.
                        -40°C (-40°F) to +125°C (125°F) storage.

# Handling your board safely

### *Anti-static handling*

This board contains CMOS devices. These could be damaged in the event of static electricity being discharged through them. Observe anti-static precautions at all times when handling circuit boards. This includes storing boards in appropriate anti-static packaging and wearing a wrist strap when handling them.

### *Electromagnetic Compatibility (EMC)*

The AIM104-COM8 is classified as a 'component' with regard to the European Community EMC regulations and it is the user's responsibility to ensure that systems using the board are compliant with the appropriate EMC standards.

The AIM104-COM8 has been designed to minimize noise emissions generated by the high frequency host PC/104 system. It includes filter components on all serial I/O lines. It is possible to capacitively couple the board ground to the chassis using metal pillars and fastenings at the mounting hole marked 'CHASSIS'. This is shown in the following diagram:



### *Packaging*

Should a board need to be returned to Arcom, please ensure that it is adequately packed, preferably in the original packing material.

# About this manual

This manual describes the operation and use of the AIM104-COM8 PC/104 module.
It is both a reference and user manual and includes information about all aspects of the module.

## Conventions

### Symbols

The following symbols are used in this guide:

| Symbol | Explanation |
|---|---|
| | Note - information that requires your attention. |
| | Tip - a handy hint that may provide a useful alternative or save time. |
| | Caution – proceeding with a course of action may damage your equipment or result in loss of data. |

### Terminology

To prevent confusion with the standard PC AT nomenclature of COM1-4, this manual refers to the channels on the AIM104-COM8 as 0-7. Where this manual specifies COM1-4, this refers to the standard PC AT communications ports.

# What items are provided?

The AIM104-COM8 is supplied with the following items:

- The AIM104-COM8 board.

- This manual.

# Description

The AIM104-COM8 uses two 16C550 type Quad-UART chips to provide eight standard PC AT type serial channels which are supported by a wide range of third party software and standard operating systems.

All channels are buffered to RS232 levels, supporting all the signals found on a PC AT type 9-pin RS232 port.

The simplest I/O address mapping has the eight serial channels appearing as eight bytes each, next to each other, based at any 16-byte boundary in the I/O map from 000-3FFh.

Channels 0-3 can be individually relocated at standard PC AT communications channel addresses for COM1-4 respectively. See JP3 - Channel re-mapping to COM addresses, page 15, for further details about address mapping.

Each QUART has its own interrupt line that can be linked to any of the following PC/104 interrupts: IRQ3-5, 7, 9-12, 14-15.

The interrupt lines from the second QUART chips can be merged with the first to drive a single IRQ line.

The AIM104-COM8 has a 16 bit PC/104 connector but utilizes only interrupt lines IRQ10, 11 12, 14 and 15 on the J5 connector. This means that the board can also be used in an 8 bit PC/104 slot providing these interrupt lines are not required.
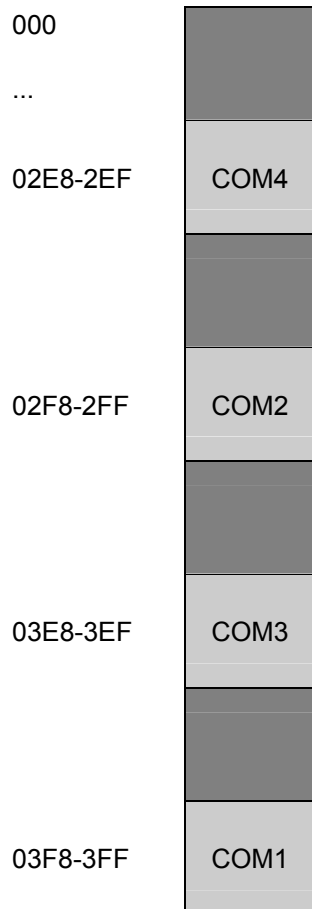
A further link on the AIM104-COM8 allows zero wait state operation of the PC/104 bus. (This is dependant on the PC/104 CPU board supporting this option.)
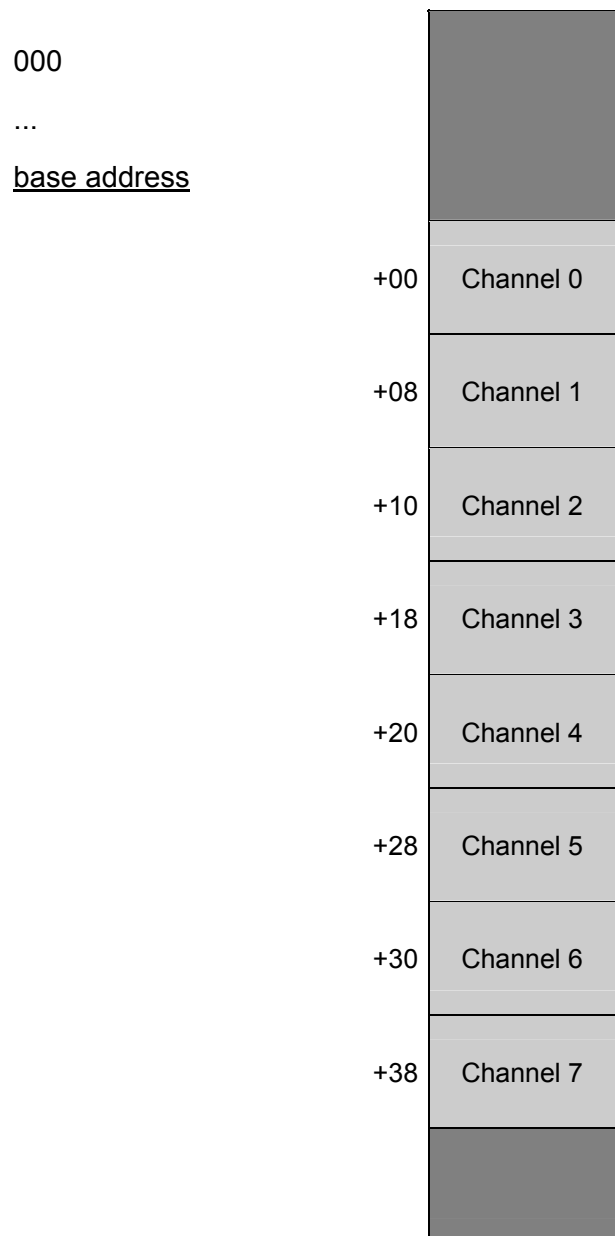
# I/O map

The I/O mapping allows a flexible configuration to be achieved. At its simplest, the UART's appear as an array of eight contiguous ports with eight bytes for each UART. The base address can be set at any 16-byte boundary.

Channels 0-3 can also be individually relocated at standard PC/AT communications channel addresses for COM1-4 respectively. As this is done, these channels 'disappear' from the group until only the last four remain. When that happens, the board logic knows that it has only 32 bytes in the group and so decodes those channels as a 32-byte block.

**PC COM port locations**                    **Group addressed map**

000

...

base address

|       |           |
|-------|-----------|
| +00   | Channel 0 |
| +08   | Channel 1 |
| +10   | Channel 2 |
| +18   | Channel 3 |
| +20   | Channel 4 |
| +28   | Channel 5 |
| +30   | Channel 6 |
| +38   | Channel 7 |

000

...

| 02E8-2EF | COM4 |
|----------|------|
| 02F8-2FF | COM2 |
| 03E8-3EF | COM3 |
| 03F8-3FF | COM1 |

## UART structure

Each channel occupies 8 bytes of I/O space with the following registers defined:

| Offset | Register | Read | Write | |
|---|---|---|---|---|
| +0 | RHR/THR | Receive Holding Register | Transmit Holding Register | |
| +1 | IER | Interrupt Enable Register | | |
| +2 | ISR/FCR | Interrupt Status Register | FIFO Control Register | General Register Set (DLAB [ICR:7] set) |
| +3 | LCR | Line Control Register | | |
| +4 | MCR | Modem Control Register | | |
| +5 | LSR | Line Status Register | | |
| +6 | MSR | Modem Status Register | | |
| +7 | SCR | Scratchpad Register | | |

| Offset | Register | Read | | |
|---|---|---|---|---|
| +0 | DLL | LSB of Divisor Latch | | Baud Rate Register (DLAB [ICR:7] clear) |
| +1 | DLM | MSB of Divisor Latch. | | |

If you are planning to write your own low level software for the AIM104-COM8, refer to the datasheet for the Exar ST16C554 device. This is available to download from www.exar.com/products/st16c554_v3.3_081004.pdf.

You can also download some example C source code from www.arcom.com/support/downloads/PCCOMS.zip.

# Interrupts

The first four channels drive one shared interrupt line and the last four channels drive another. These IRQ lines can be selected from IRQ3, 4, 5, 7, 9, 10, 11, 12, 14 or 15.

Please note that IRQs 10, 11, 12, 14 and 15 are only available when the AIM104-COM8 is used in a 16 bit PC/104 stack.

# Jumpers

There are four user-selectable jumpers on the AIM104-COM8. These are used to configure the I/O address and the interrupt line for each QUART.
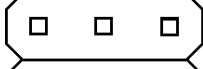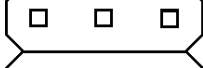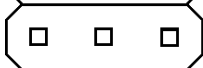
## Default settings
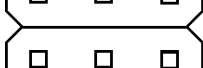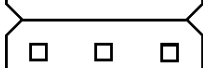
The default positions of the jumpers are as follows:
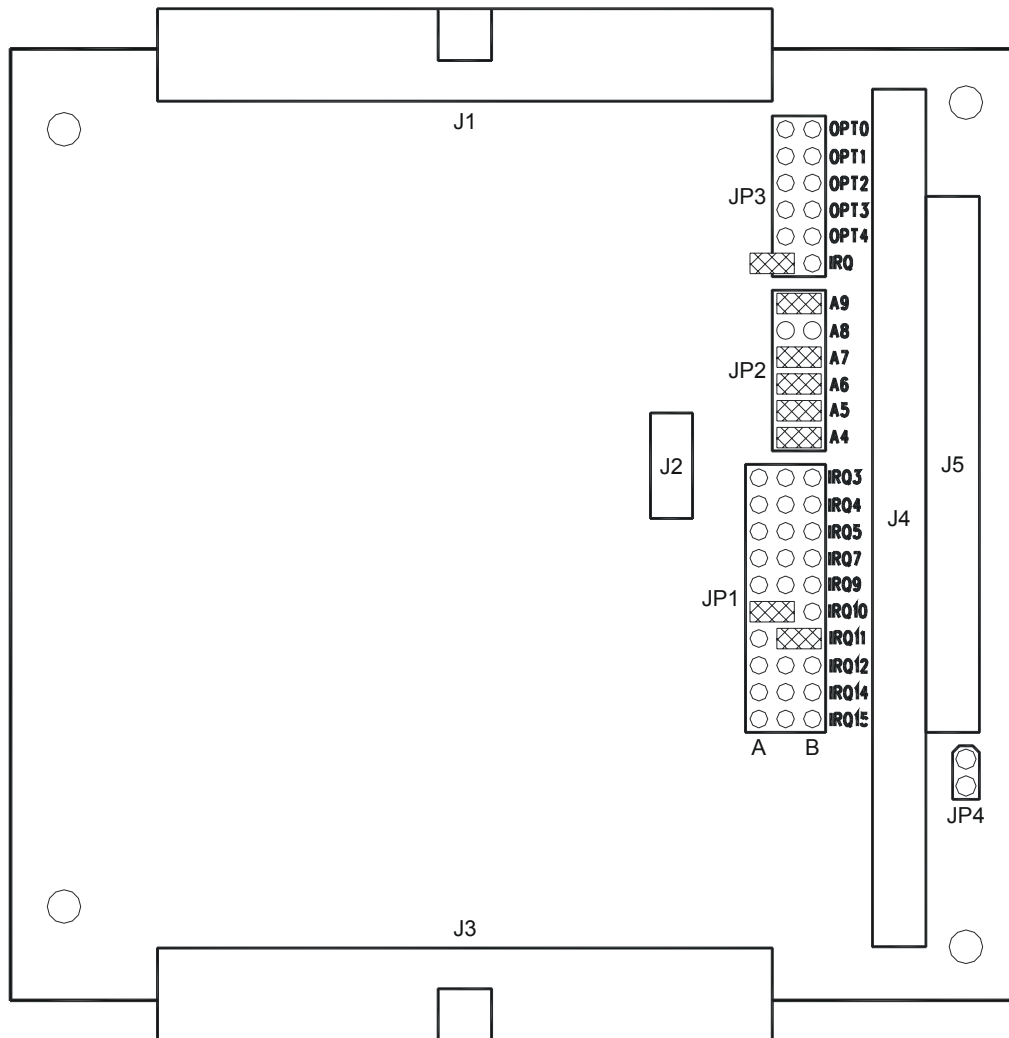


Refer to the documentation supplied with your CPU card to establish which spare I/O and interrupt channels to use.

# JP1 - Interrupt selection

The JP1 jumper is used to set the IRQ line for each group of four serial port channels. The A position is used for channels 0-3 and the B position for channels 4 – 7.

| JP1 | Line | Function when fitted |
|---|---|---|
| ☐ ☐ ☐ | IRQ3 | Routes IRQ line to IRQ3. |
| ☐ ☐ ☐ | IRQ4 | Routes IRQ line to IRQ4. |
| ☐ ☐ ☐ | IRQ5 | Routes IRQ line to IRQ5. |
| ☐ ☐ ☐ | IRQ7 | Routes IRQ line to IRQ7. |
| ☐ ☐ ☐ | IRQ9 | Routes IRQ line to IRQ9. |
| ☐ ☐ ☐ | IRQ10 | Routes IRQ line to IRQ10. |
| ☐ ☐ ☐ | IRQ11 | Routes IRQ line to IRQ11. |
| ☐ ☐ ☐ | IRQ12 | Routes IRQ line to IRQ12. |
| ☐ ☐ ☐ | IRQ14 | Routes IRQ line to IRQ14. |
| ☐ ☐ ☐ | IRQ15 | Routes IRQ line to IRQ15. |
| **A**      **B** | | |

When jumper JP3 (see page ) is set to 'IRQ', side A is for all channels and the signal on side B becomes tri-stated so that it does not interrupt on both sides. In this case, the link on side B should be removed.
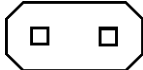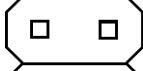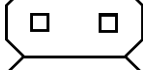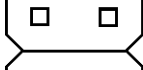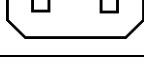
Channels 0-3 share the same interrupt line, while 4-7 share another. You cannot, for instance, set COM1/COM3 to use IRQ4 and COM2/COM4 to use IRQ3, which are the PC defaults.

# JP2 - Group base address selection

This jumper is used to set the I/O base address for the serial ports. The default jumper settings configure all of the serial ports at a 64-byte contiguous I/O space from this address location.

The base address is always decoded to a 16-byte boundary. Fitting the link sets the address line to zero for the decode. Leaving the link off means that the corresponding address line must be a logic '1' to select the board.

| JP2 | Line | Function when fitted |
|-----|------|----------------------|
| ☐ ☐ | A9 | Sets A9 in I/O address decode to 0. |
| ☐ ☐ | A8 | Sets A8 in I/O address decode to 0. |
| ☐ ☐ | A7 | Sets A7 in I/O address decode to 0. |
| ☐ ☐ | A6 | Sets A6 in I/O address decode to 0. |
| ☐ ☐ | A5 | Sets A5 in I/O address decode to 0. |
| ☐ ☐ | A4 | Sets A4 in I/O address decode to 0. |

The default base address is 0x100, to avoid conflicts with common PC I/O maps. In order to achieve this fit all links apart from A8. Check your system I/O map for conflicts before use.
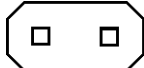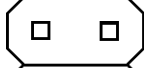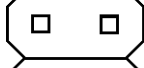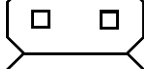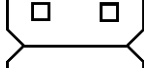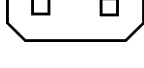
# JP3 - Channel re-mapping to COM addresses

You can individually re-map channels 0 to 3 at the standard COM port addresses. When these channels are mapped at COM ports they vanish from the group. This prevents the host seeing them in two places.

If all four are mapped in that way, the group size falls to 32 bytes and channels 4 to 7 begin at the base address.

You should avoid addressing conflicts due to the group decoding overlapping COM decoding. If there is a conflict, then the group decoding applies and any conflicting COM decoded channel.

The decoding logic above ensures the minimum use of scarce I/O locations.

| JP3 | Line | Function when fitted |
|-----|------|----------------------|
| □ □ | OPT0 | Channel 0 remapped to COM1. |
| □ □ | OPT1 | Channel 1 remapped to COM2. |
| □ □ | OPT2 | Channel 2 remapped to COM3. |
| □ □ | OPT3 | Channel 3 remapped to COM4. |
| □ □ | OPT4 | Disables I/O address decoding for channels 4 to 7. |
| □ □ | IRQ | Combines interrupts from both quad-UART chips into one (side A on links below). |

Interrupt merging: each quad-UART chip can assert an individual IRQ line, but in systems where IRQ lines are scarce they can be combined into one for both chips.

## JP4 - Wait state behavior selection

Computers normally wait for a fixed time for PC104 bus access. If the zero wait state (0WS) is selected this waiting is skipped and the signal is asserted as soon as the board decodes a valid address. This can shorten the amount of time spent accessing the board in some situations.

| JP4 | Description |
|-----|-------------|
| | Waits for bus access. |
| | Zero wait. |

Default setting:

# Cable Connections

The serial I/O connectors have been wired so that they can be easily split into 9-way male D-sub connectors with standard pin-outs for PC/AT RS232 serial ports.

The table below shows the corresponding channel and connector pinouts.

| 40 Way IDC ribbon header | Male 9 way IDC D-Sub | Channel | Pinout |
|---|---|---|---|
| Pins 1-9 | Pins 1-9 | 0 | |
| Pins 11-19 | Pins 1-9 | 1 | PC/AT RS232 port |
| Pins 21-29 | Pins 1-9 | 2 | |
| Pins 31-39 | Pins 1-9 | 3 | |

The same cabling applies to both of the 40-way boxed headers.

# Appendix A – Contacting Arcom

## Arcom sales

Arcom's sales team is always available to assist you in choosing the board that best meets your requirements. Contact your local sales office or hotline.

| | |
|---|---|
| ***Sales office US*** | ***Sales office Europe*** |
| Arcom<br>7500W 161$^{st}$ Street<br>Overland Park<br>Kansas<br>66085<br>USA | Arcom<br>Clifton Road<br>Cambridge<br>CB1 7EA<br>UK |
| | Tel:        01223 411 200<br>Fax:        01223 410 457<br>E-mail:    euro-sales@arcom.com |
| Tel:        913 549 1000<br>Fax:        913 549 1002<br>E-mail:    us-sales@arcom.com | |

Full information about all Arcom products is available on our Web site at www.arcom.com.

While Arcom's sales team can assist you in making your decision, the final choice of boards or systems is solely and wholly the responsibility of the buyer. Arcom's entire liability in respect of the boards or systems is as set out in Arcom's standard terms and conditions of sale. If you intend to write your own low level software, you can start with the source code on the disk supplied. This is example code only to illustrate use on Arcom's products. It has not been commercially tested. No warranty is made in respect of this code and Arcom shall incur no liability whatsoever or howsoever arising from any use made of the code.

## Technical support

Arcom has a team of technical support engineers who can provide assistance if you have any problems with your APC-INDUSTRIAL PC-P4 board.

| Technical support US | Technical support Europe |
|---|---|
| Tel:913 549 1010 | Tel:+44 (0)1223 412 428 |
| Fax:913 549 1001 | Fax:+44 (0)1223 403 409 |
| E-mail:us-support@arcom.com | E-mail:euro-support@arcom.com |

# Appendix B – Connector details

The serial port connections are routed to two 40-way headers on the AIM104-COM8. One of these connectors J3 has the channel 0 – 3 signals and the other J1 has the channel 4 – 7 signals. The pinout details for these connectors is shown below:

## J3 Channel 0 – 3

Connector: 40 way, 2.54mm (0.1") x 2.54mm (0.1") dual row right angle boxed header.

Mating Connector: Framatome 71600-040

| Pin | Signal Name | Pin | Signal Name |
|-----|-------------|-----|-------------|
| 1 | DCD0 | 2 | DSR0 |
| 3 | RXD0 | 4 | RTS0 |
| 5 | TXD0 | 6 | CTS0 |
| 7 | DTR0 | 8 | RI0 |
| 9 | GND | 10 | GND |
| 11 | DCD1 | 12 | DSR1 |
| 13 | RXD1 | 14 | RTS1 |
| 15 | TXD1 | 16 | CTS1 |
| 17 | DTR1 | 18 | RI1 |
| 19 | GND | 20 | GND |
| 21 | DCD2 | 22 | DSR2 |
| 23 | RXD2 | 24 | RTS2 |
| 25 | TXD2 | 26 | CTS2 |
| 27 | DTR2 | 28 | RI2 |
| 29 | GND | 30 | GND |
| 31 | DCD3 | 32 | DSR3 |
| 33 | RXD3 | 34 | RTS3 |
| 35 | TXD3 | 36 | CTS3 |
| 37 | DTR3 | 38 | RI3 |
| 39 | GND | 40 | GND |
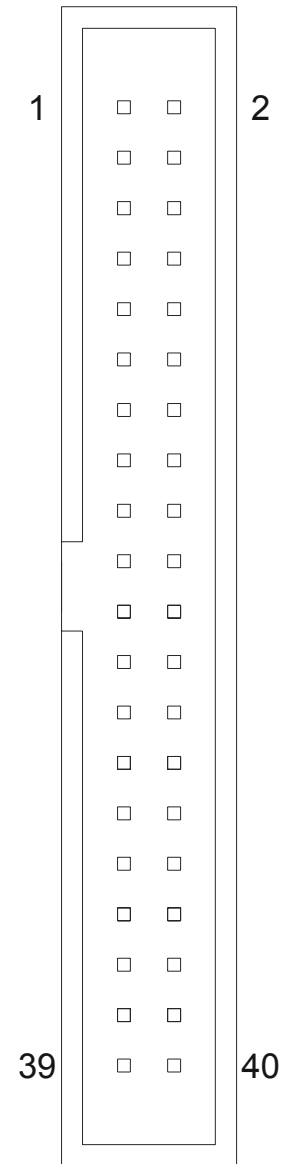
## J1 Channel 4 - 7

Connector: 40 way, 2.54mm (0.1") x 2.54mm (0.1") dual row right angle boxed header

Mating Connector: Framatome 71600-040

| Pin | Signal Name | Pin | Signal Name |
|-----|-------------|-----|-------------|
| 1 | DCD4 | 2 | DSR4 |
| 3 | RXD4 | 4 | RTS4 |
| 5 | TXD4 | 6 | CTS4 |
| 7 | DTR4 | 8 | RI4 |
| 9 | GND | 10 | GND |
| 11 | DCD5 | 12 | DSR5 |
| 13 | RXD5 | 14 | RTS5 |
| 15 | TXD5 | 16 | CTS5 |
| 17 | DTR5 | 18 | RI5 |
| 19 | GND | 20 | GND |
| 21 | DCD6 | 22 | DSR6 |
| 23 | RXD6 | 24 | RTS6 |
| 25 | TXD6 | 26 | CTS6 |
| 27 | DTR6 | 28 | RI6 |
| 29 | GND | 30 | GND |
| 31 | DCD7 | 32 | DSR7 |
| 33 | RXD7 | 34 | RTS7 |
| 35 | TXD7 | 36 | CTS7 |
| 37 | DTR7 | 38 | RI7 |
| 39 | GND | 40 | GND |
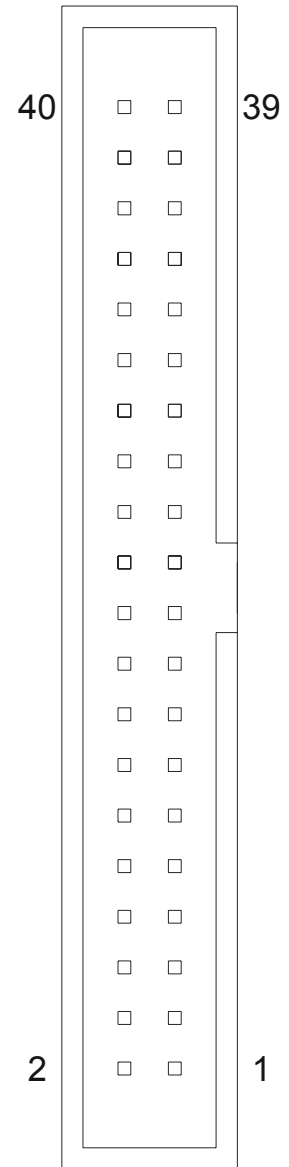
# Appendix C – Notes on using the 16C550 UART

## Enabling the interrupt outputs

If you intend to write your own low level UART handler, remember that in order for the UART channel on the AIM104-COM8 to generate interrupts to the host CPU, you must enable the IRQ output from the UART by setting bit 3 in the Modem Control Register (MCR).

Standard driver software does this as part of the port initialization, so no action is necessary if you are using Arcom's example software or that of a third party vendor.

## The receiver FIFO trigger point and timeout

The 16C550 has sixteen byte FIFO's for both its transmit buffer and receive buffer. This can enhance the performance of the serial ports and reduce the interrupt rate to the main processor. However, it is necessary to set up the receive trigger point optically for your application.
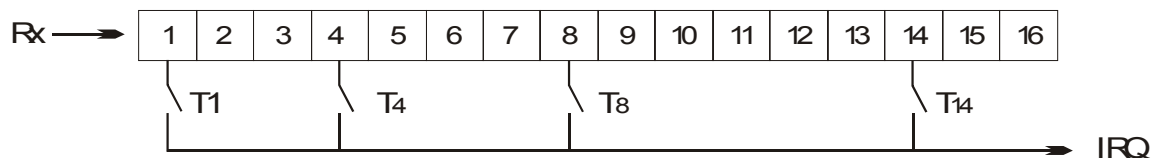


With the FIFO enabled, any character received is added to the 16 byte receive FIFO. This has four programmable trigger points as shown in the following diagram:

Once the FIFO has received sufficient characters to reach the FIFO trigger point, an interrupt is generated that is serviced in order to remove all the characters from the FIFO.

If the FIFO trigger point is set to a value other than 1, a situation may arise where the input data stream stops adding characters to the FIFO before the trigger point is reached. For example, the trigger may be set at eight when only six characters has been received. In this situation the UART generates an IRQ after a specific timeout period from the end of the last character received.

The timeout period, expressed in the number of characters, can be calculated using the following equation:

$$T = [\,(4 \times n_{Char}) + 12\,] / [\,n_{Parity} + n_{Char} + n_{Stop} + 1\,]$$

where:

$n_{Char}$ is the number of programmed bits per character (5, 6, 7 or 8).
$n_{Parity}$ is the number of programmed parity bits (1 unless no parity).
$n_{Stop}$ is the number of programmed stop bits (1, 1½ or 2).

The actual time for the timeout is simply defined as:

$$t = [ (4 \times n_{Char}) + 12 ] / F_{Baud}$$

where $F_{Baud}$ is the baud rate.

For example, communications at 9600 baud, 8 data bits, no parity and 1 stop bit would have the following timeout period:

$$T = [ (4 \times 8) + 12 ] / [ 0 + 8 + 1 + 1 ] = 44/10 = 4.4 chars$$

$$t = [ (4 \times 8) + 12 ] / 9600 = 4.58ms$$

This timeout can significantly impact on the performance of the serial communications within an application. If your serial communications is single character oriented, it is better to set the FIFO trigger point lower and handle more frequent receive interrupts. If your application transfers large blocks of data it is probably better to set the FIFO trigger point higher.

Remember that the FIFO trigger point does not define the size of the FIFO. Characters are still received after the trigger has been activated until all sixteen positions in the FIFO have been filled**.**

# Appendix D – Reference information

There are many other communications programming resources available on the Internet, including:

- www.simtel.net.
  Archive of shareware and public domain code for Windows 9x and DOS. There is a multitude of source code available, some of which is useful for communications programming

- www.acs.oakland.edu/oak.html.
  Archive of software, similar to the above with communications programming source code available.

The C Programmer's Guide to Serial Communications (author: Joe Campbell, publisher: Sams Paperback, ISBN: 0672302861) provides a comprehensive guide to designing and implementing serial communications software architectures. The guide is available through Amazon (www.amazon.com).

# Appendix E – Acronyms and abbreviations

| | |
|---|---|
| COM | Communication port |
| CMOS | Complementary Metal Oxide Semiconductor |
| CTS | Clear To Send |
| DC | Direct Current |
| DCD | Data Carrier Detect |
| DSR | Data Set Ready |
| DTR | Data Terminal Ready |
| EMC | Electromagnetic Compatibility |
| FIFO | First In First Out |
| LED | Light Emitting Diode |
| IO | Input/Output |
| QUART | Quad-UART |
| RI | Ring Indicator |
| RTS | Request to Send |
| RXD | Receive Data |
| TXD | Transmit Data |
| UART | Universal Asynchronous Receiver-Transmitter |

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