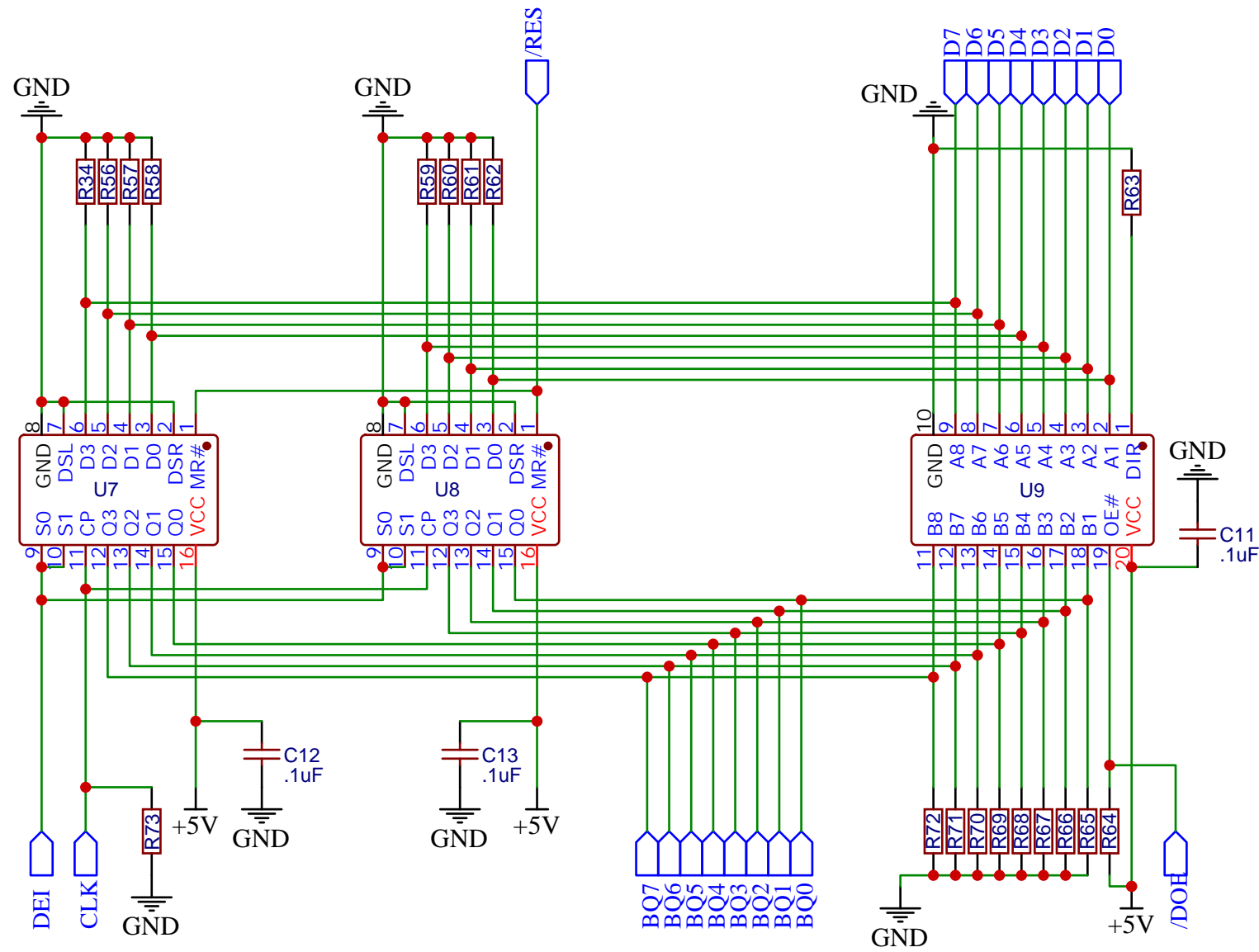


TITLE: Accumulator Register Module Register "A"		REV: 1.0
	Company: Z80_Dad	Sheet: 1/1
	Date: 2022-02-22	Drawn By: dave collins

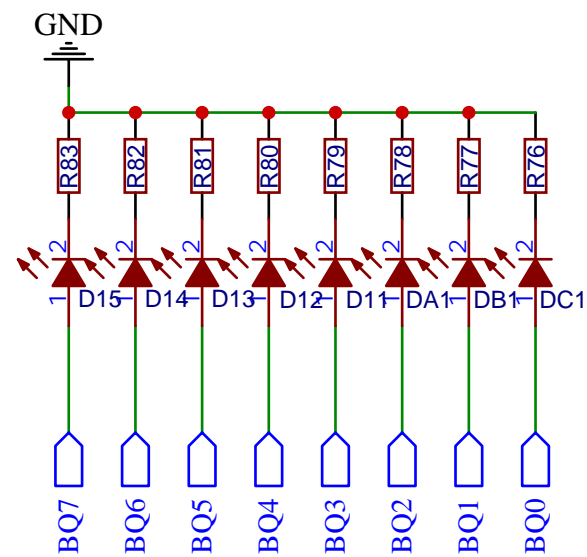
Latch pull downs support the main bus state



View 74HC194 datasheet for S0/S1 Vaules

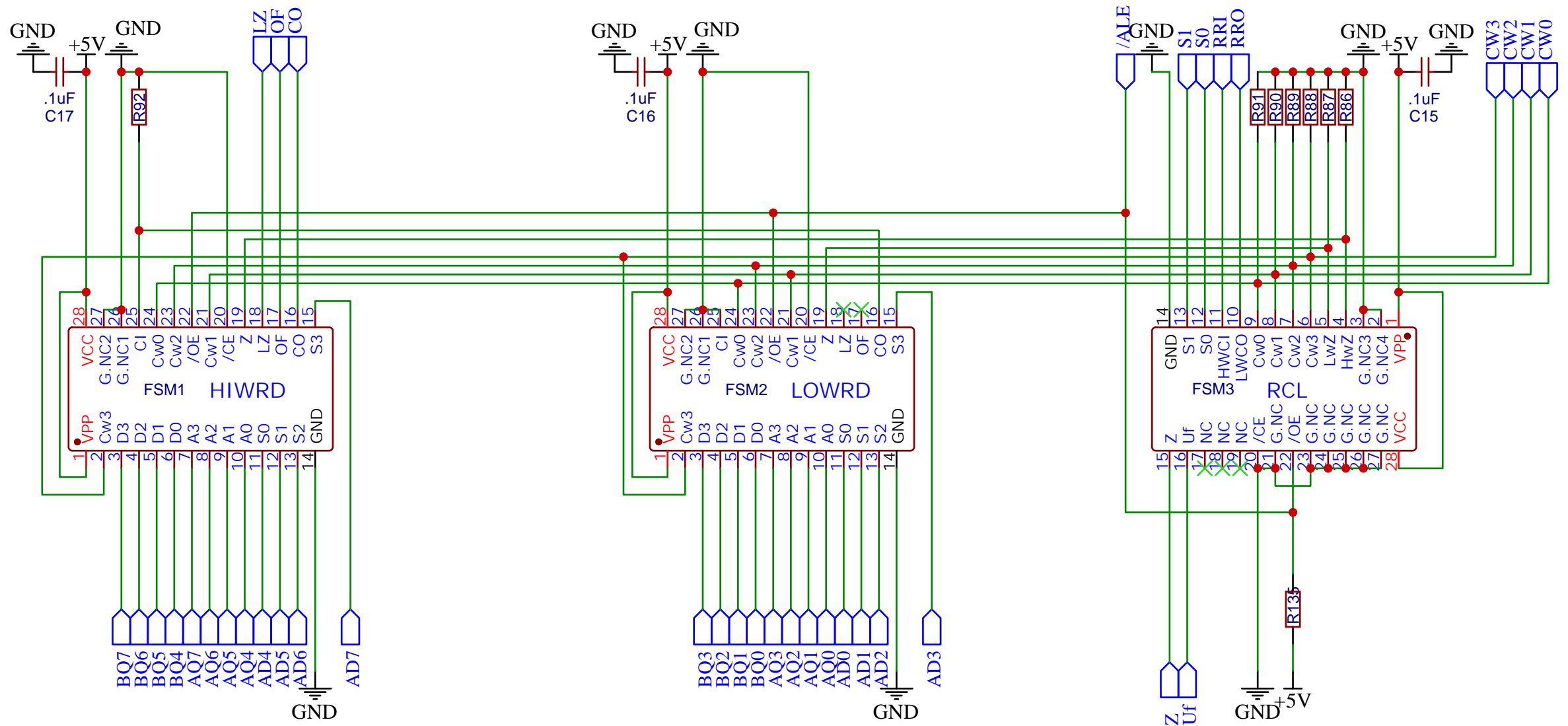
All Curent Limiting are 220 Ohm
All Pull Up/Down are 10K Ohm


CD74HC194E U7
CD74HC194E U8
CD74HC245E U9

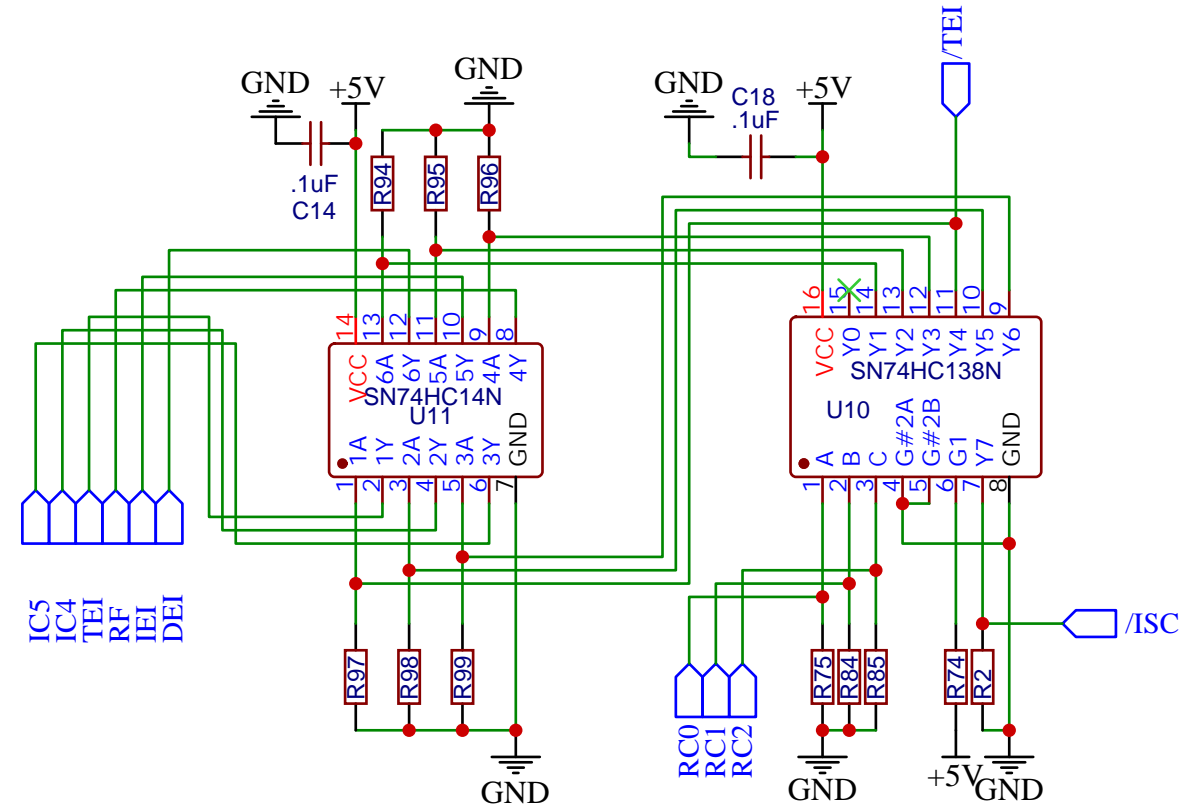
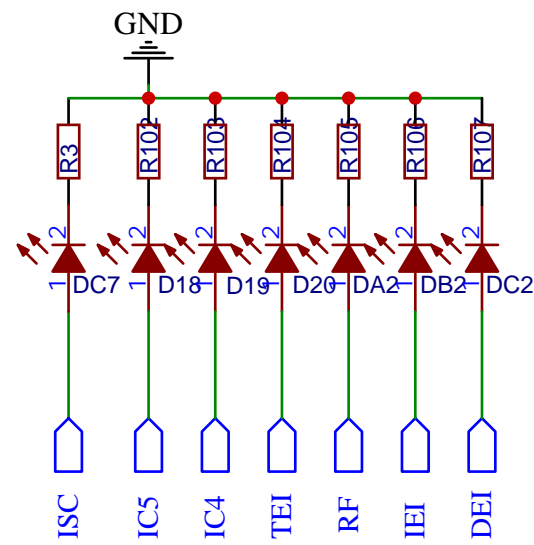


TITLE: Data Bus Storage Module Register "B"		REV: 2.0
EasyEDA	Company: Z80_Dad	Sheet: 1/1
	Date: 2022-04-18	Drawn By: dave collins

W27E258
FSM1
FSM2
FSM3

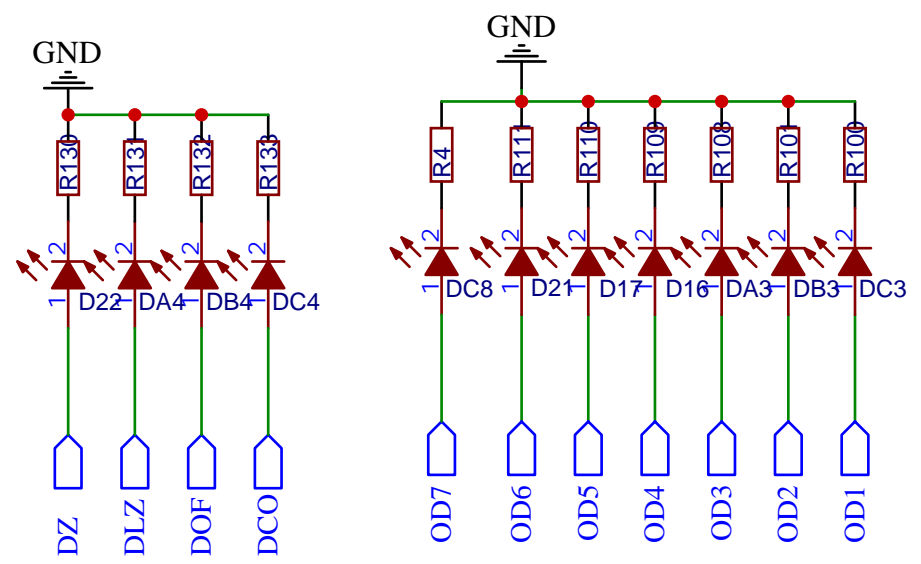
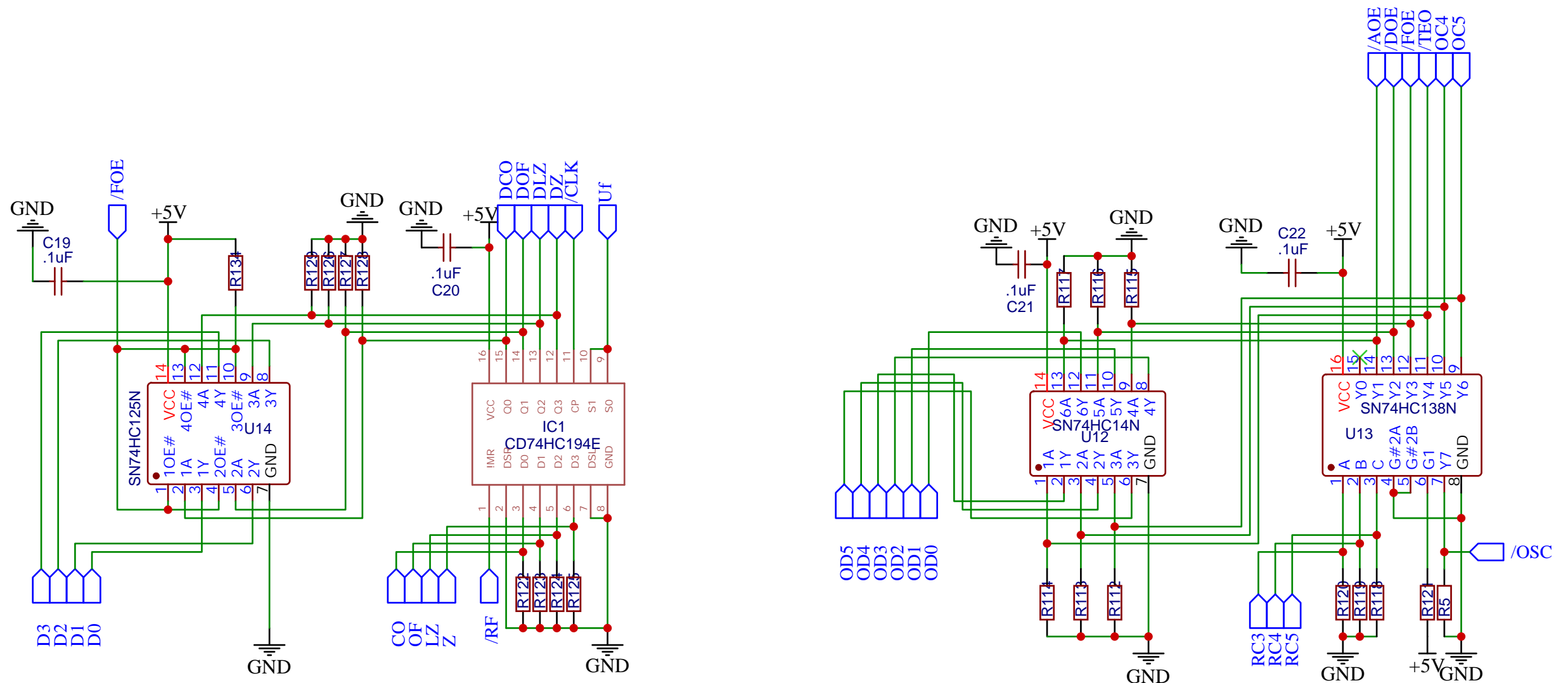


TITLE: 8 Bit Arithmetic Logic Unit - Module		REV: 1.0
	Company: Z80_DAD	Sheet: 1/1
	Date: 2022-04-19	Drawn By: dave collins



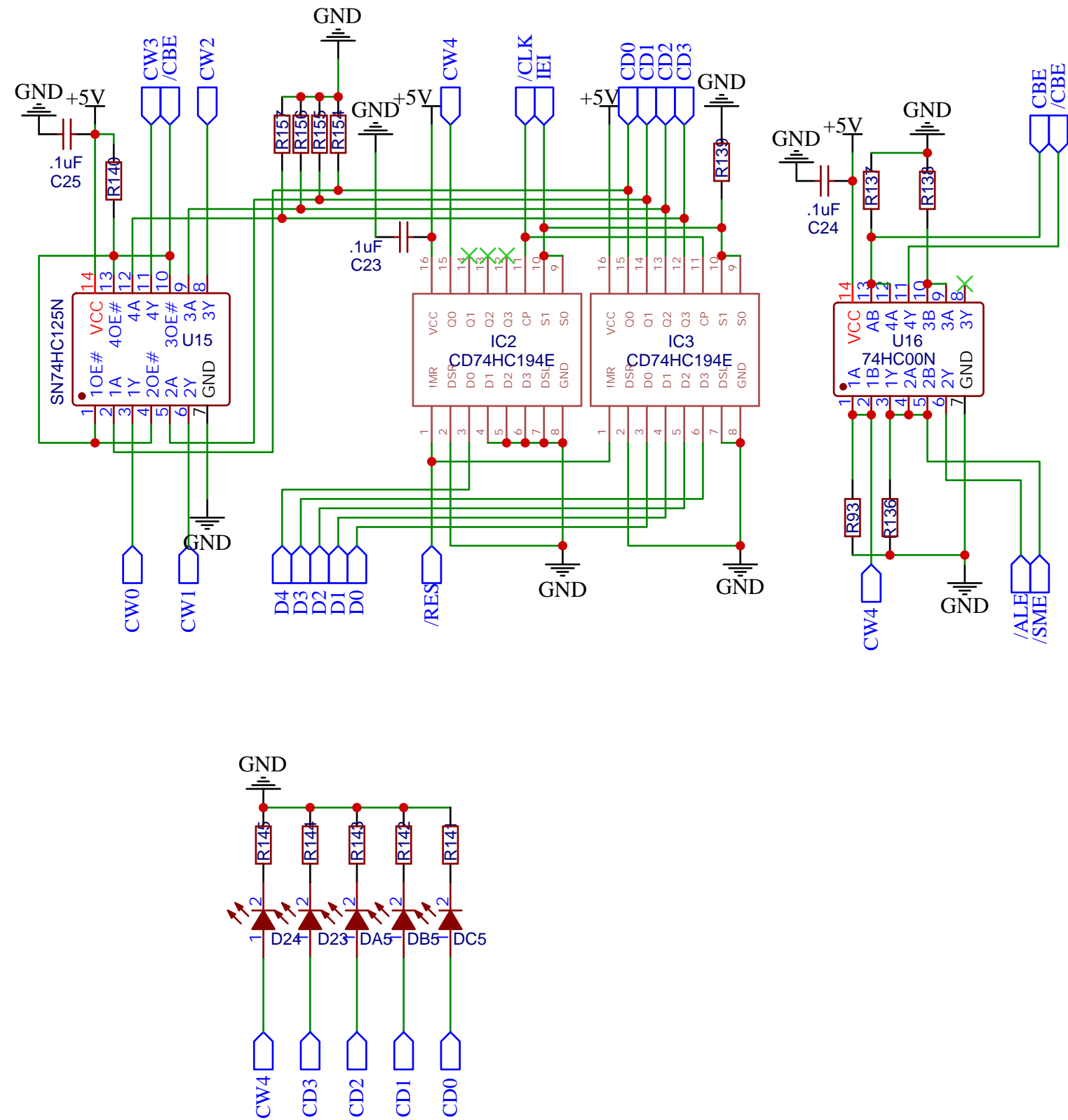
PULL UP / DOWN RES. ARE 10K
CURRENT LIMIT ARE 220R

TITLE: Input Decode logic		REV: 1.0
	Company: Z80Dad	Sheet: 1/1
	Date: 2022-05-30	Drawn By: dave collins



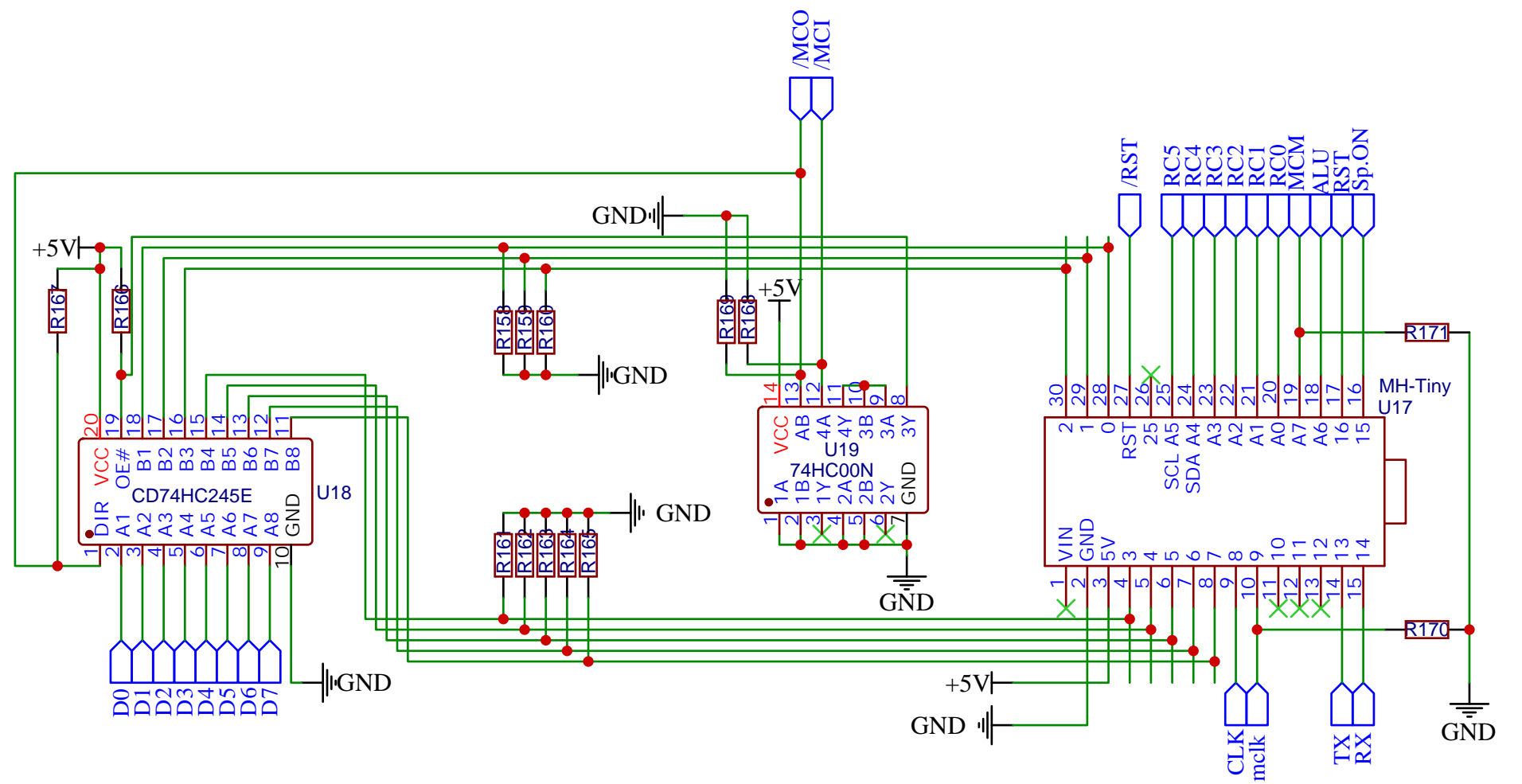
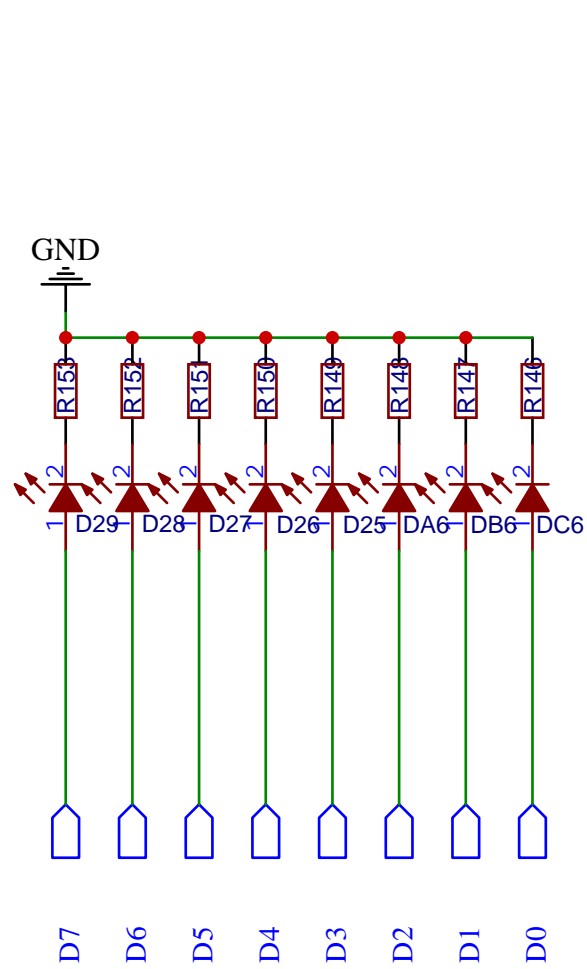
PULL UP / DOWN RES. ARE 10K
CURRENT LIMIT ARE 220R

TITLE: Output Decode / Flags Register		REV: 1.0
EasyEDA	Company: Your Company	Sheet: 1/1
	Date: 2022-05-30	Drawn By: dave collins



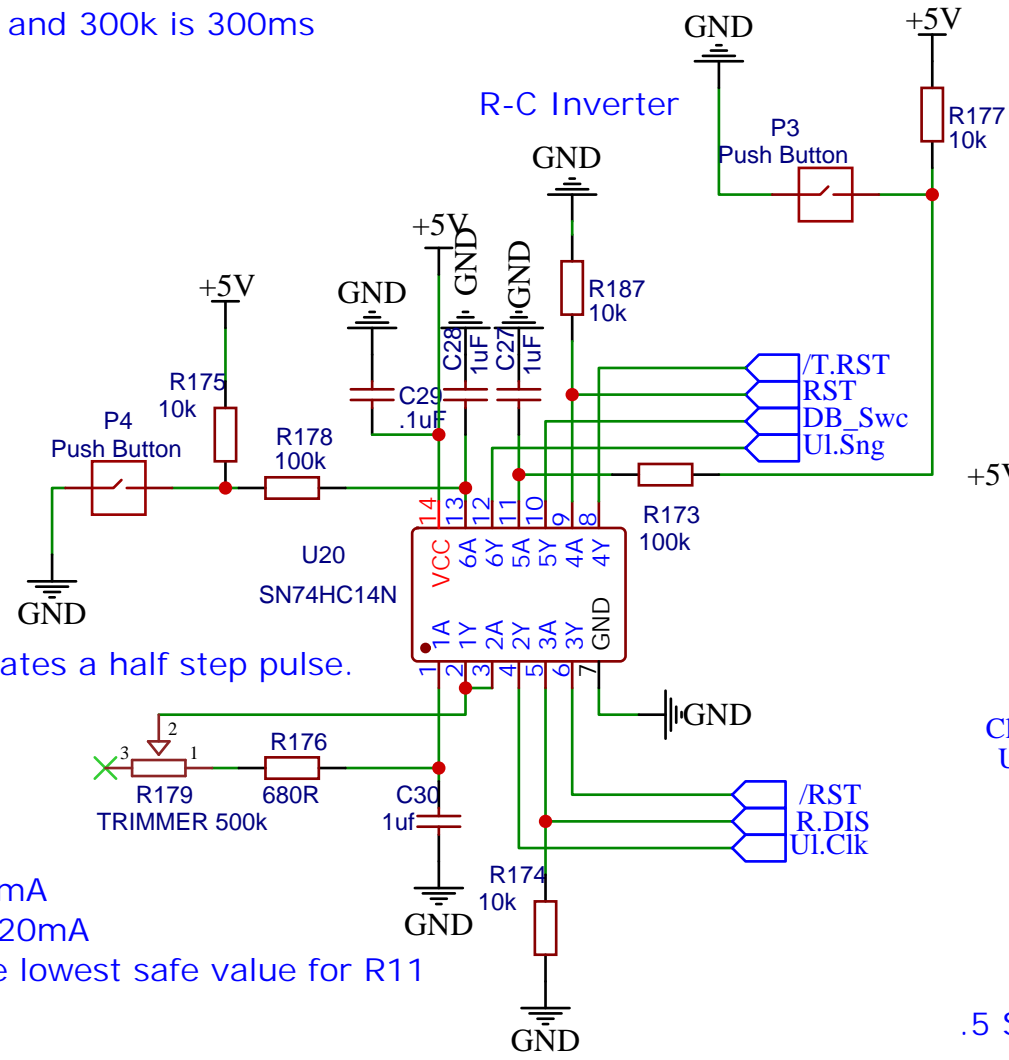
PULL UP / DOWN RES. ARE 10K
CURRENT LIMIT ARE 220R

TITLE: Instruction Register		REV: 1.0
	Company: Z80Dad	Sheet: 1/1
	Date: 2022-05-31	Drawn By: dave collins



TITLE: ATTINY88 CONTROL MODULE		REV: 1.0
	Company: Z80Dad	Sheet: 1/1
	Date: 2022-05-31	Drawn By: dave collins

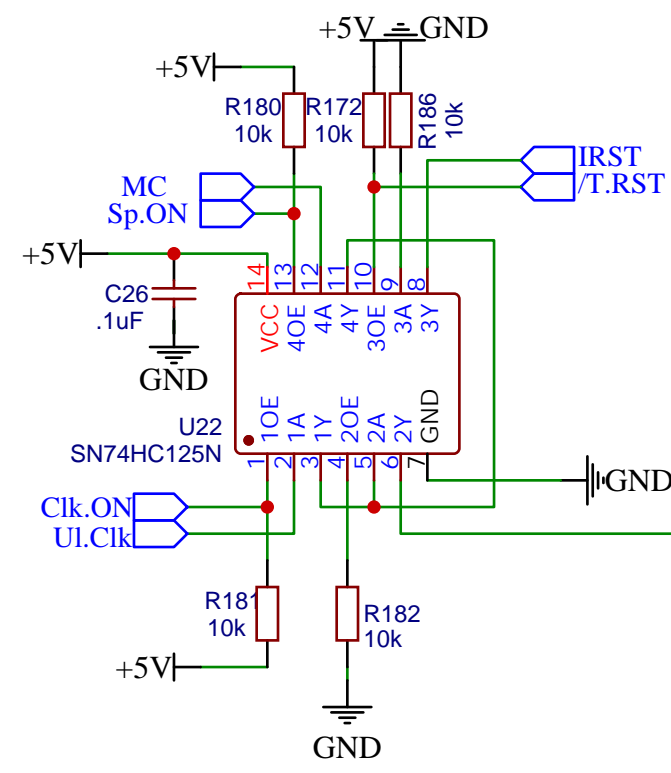
RC math for 1uF and 100k is 100ms
 RC math for 1uF and 300k is 300ms



P2 Generates a half step pulse.

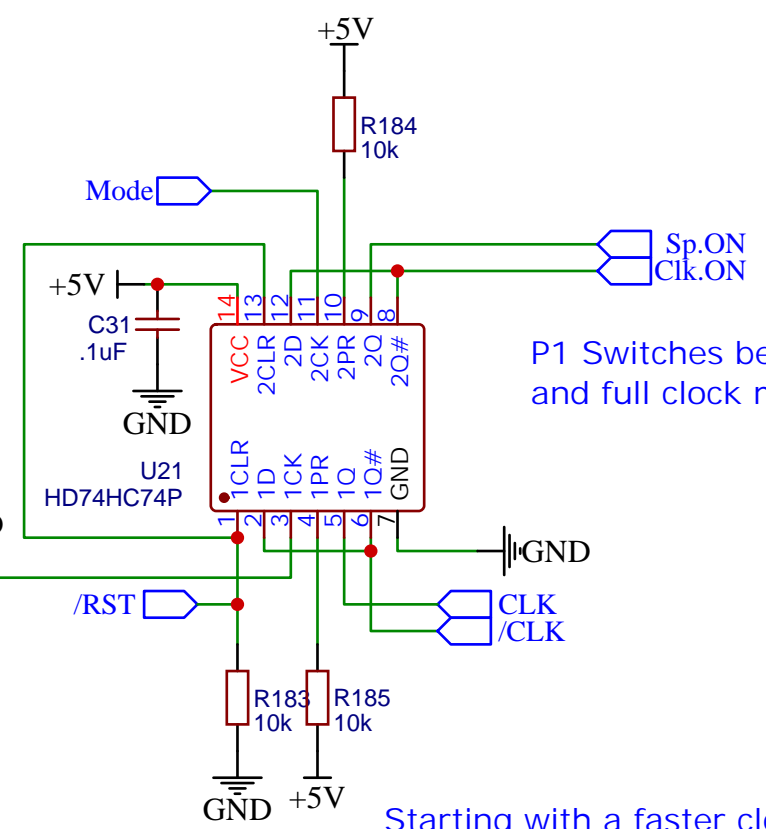
$I = 18\text{mA}$
 $\text{MAX } I = 20\text{mA}$
 270R is the lowest safe value for R11

Function Select Buffer



.5 Sec Reset Pulse

Clock and Control Latch

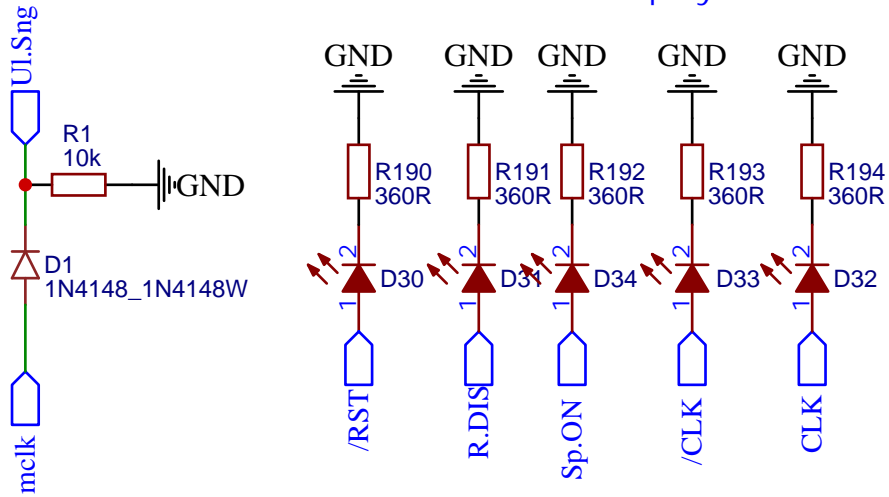


P1 Switches between half step and full clock mode.

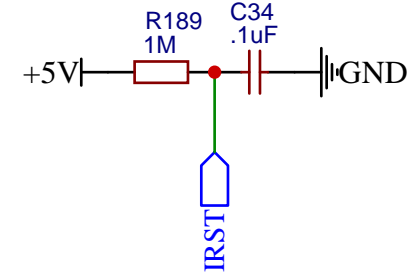
Starting with a faster clock than we need. We can achieve a latch clock that holds its state through functional transitions.

The Result is both a perfect 50% duty cycle between CLK & ~CLK, at the cost of 50% the frequency of UI.CLK and CLK.

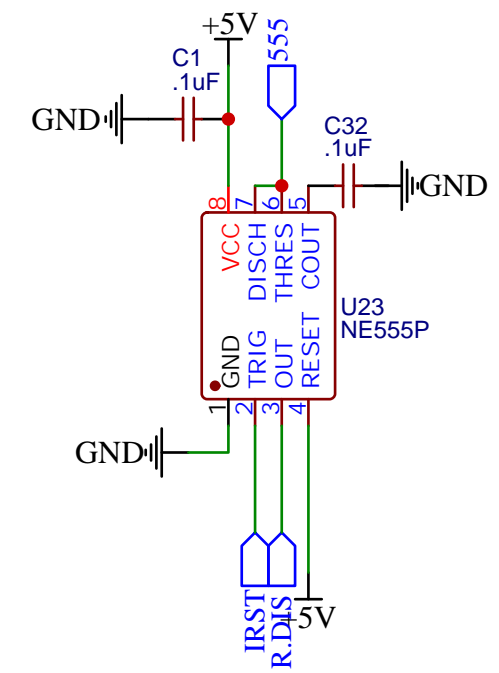
Display



Initial Reset RC

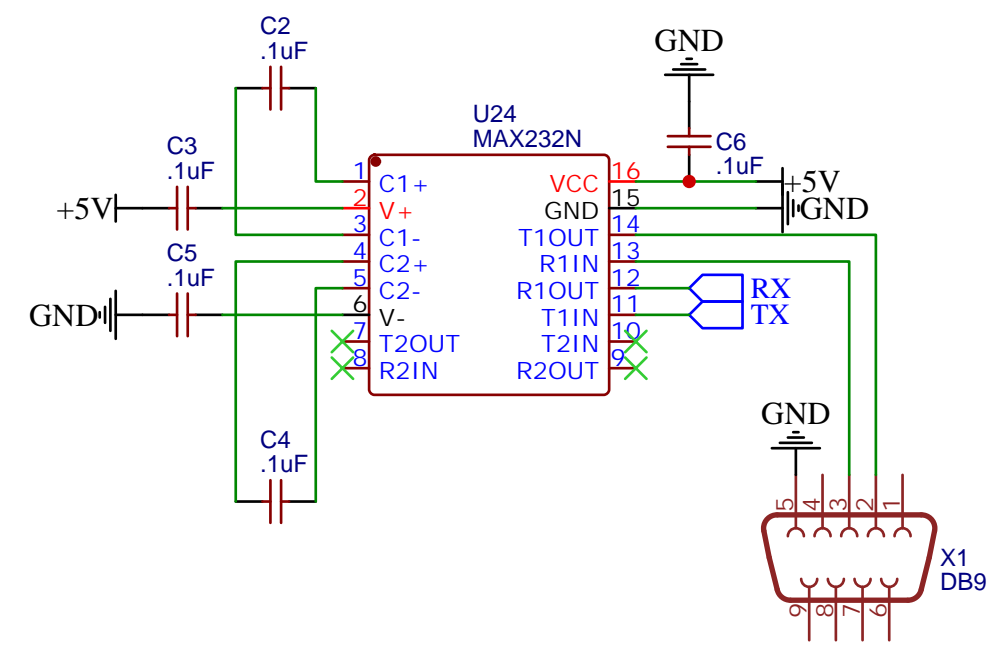
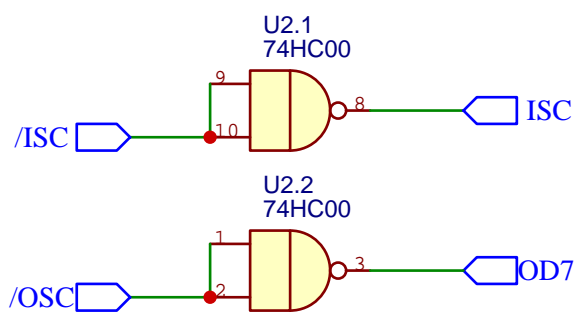
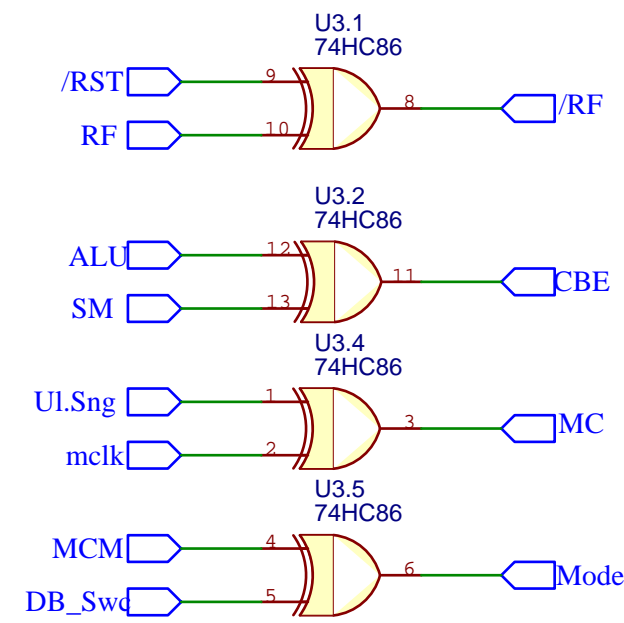
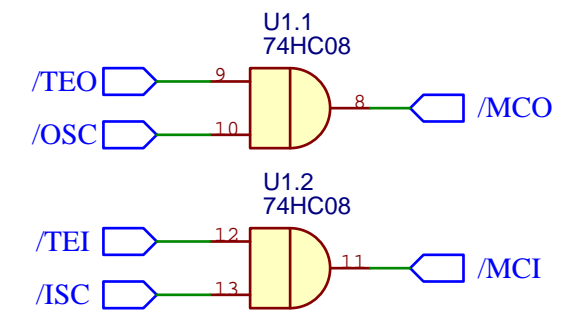


Reset timer Circuit



TITLE: Clock Module		REV: 2.0
EasyEDA	Company: Z80Dad	Sheet: 1/1
	Date: 2022-06-16	Drawn By: dave collins

These are scattered throughout the build



TITLE: Glue Logic		REV: 1.0
EasyEDA	Company: Your Company	Sheet: 1/1
	Date: 2022-07-04	Drawn By: dave collins