SCPC486

STEbus 486DX PC AT Compatible Board

Technical Manual

Product Information

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Useful Contact Information

Customer Support
Tel: +44 (0)1223 412 428
Fax: +44 (0)1223 403 400
E-mail: support@arcom.co.uk

Sales
Tel: +44 (0)1223 411 200
Fax: +44 (0)1223 410 457
E-mail sales@arcom.co.uk
or for the US
E-mail icpsales@arcomcontrols.com

United Kingdom
Arcom Control Systems Ltd
Clifton Road
Cambridge CB1 4WH, UK
Tel: 01223 411 200
Fax: 01223 410 457
FoD: 01223 240 600

United States
Arcom Control Systems Inc
13510 South Oak Street
Kansas City MO 64145 USA
Tel: 816 941 7025
Fax: 816 941 0343
FoD: 800 747 1097

France
Arcom Control Systems
Centre d'affaires SCALDY
23 rue Colbert
7885 SAINT QUENTIN
Cedex, FRANCE
Tel: 800 90 84 06
Fax: 800 90 84 12
FoD: 800 90 23 80

Germany
Kostenlose Infoline:
Tel: 0130 824 511
Fax: 0130 824 512
FoD: 0130 860 449

Italy
NumeroVerde:
FoD: 1678 73600

Belgium
Groen Nummer:
Tel: 0800 7 3192
Fax: 0800 7 3191

Netherlands
Gratis 06 Nummer:
Tel: 06022 11 36
Fax: 06022 11 48

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Contents

Preface

The Manual

This manual details the operation and use of the Arcom range of STEbus 486DX PC AT compatible processor boards which will be generically referred to as SCPC486. It has been designed to be used as both a reference and user manual and includes sections from getting started with the board through to using the more advanced features available.

If you require further assistance in using the SCPC486 you can contact our free technical support service on 01223 412428

Utility Disks

Supplied free with the SCPC486DX4 are three utility disks.

Disk 1 contains a full copy of the Arcom Flash Filing System, ROM-DOS 6.22 utilities and utilities for accessing the EEPROM and configuring the STEbus. Refer to section 4. Using the Board.

Disk 2 and 3 contain the video drivers for DOS and Microsoft Windows.

Anti-Static Handling

This board contains CMOS devices which could be damaged in the event of a static electricity being discharged through them. At all times, please observe anti-static precautions when handling the board and always unpack and install it in an anti-static working area.

Battery

The SCPC486 contains a cadmium free rechargeable battery which will be shipped with a link disconnecting it from the battery backup supply.

Prior to use, link LK5 should be moved to position **B** for correct operation of the battery backup. Refer to **Section 3. Links & Options.**

Packaging

Please ensure that should a board need to be returned to Arcom, it is adequately packed and that the battery is isolated.

Section 1. Introduction

The SCPC486 is a single height Eurocard PC AT based on the Intel 486DX4 processor. The bus interface complies with the ANSI/IEEE 1000-1987 standard for STEbus. It provides the following advanced features:

- Full PC AT compatible core.
  486DX4-100 Microprocessor.
  Memory options of 4, 8 or 16Mb.
  Local-bus VGA supporting CRT and flat panel displays.
  Standard RS232 COM1/2 using 16550 UARTS.
  Bi-directional centronics printer port LPT1.
  On-board floppy disk interface (up to 2 drives).
  On-board IDE hard disk interface (up to 2 drives).

- Flash memory of 2 or 4Mb.
  Arcom Flash Filing System (AFFS)
  Datalight ROM-DOS 6.22

  Note: AFFS and ROM-DOS are only installed on SCPC486 boards fitted with FlashFile memory.

- Hardware watchdog timer.

- ANSI/IEEE 1000-1987 (STEbus) bus interface
  Default or potential bus master.
  Programmable bus time-out monitor.
  Software configurable interrupt mapping.

Because the SCPC486 is fully PC AT compatible, standard software tools available for the PC AT platform can be used to develop your software. The SCPC486 is fully compatible with the following operating systems:

- Microsoft MS-DOS
- Microsoft Windows 3.10, 3.11
- Microsoft Windows 95
- Microsoft Windows NT
- SCO UNIX
- QNX

Section 2. Getting Started

The SCPC486 is shipped in a default configuration that will work in most single-master STEbus applications. Only one link change is required plus the appropriate breakout connections to the keyboard, display and disk drives.

Note: If you are using a flat panel interface module (FPIF), refer to the documentation accompanying that board for details on configuring the flat panel interface.

Anti-static Handling

This board contains CMOS devices which could be damaged in the event of a static electricity being discharged through them. At all times, please observe anti-static precautions when handling the board and always unpack and install it in an anti-static working area.

Before Powering up the Board

The SCPC486 is supplied in a default configuration that will operate correctly in the basic system that is supplied below. Only one link is required to be changed for a fully functioning industrial PC system to be fully operational.

Battery Link

The battery backup is disconnected on the SCPC486 during shipment. Move link LK5 to position B to enable the battery backup facility.

ROM-DOS and AFFS

All SCPC486 boards fitted with FlashFile memory are supplied with Arcom Flash Filing System (AFFS) and ROM-DOS 6.22 installed. AFFS turns the on-board FlashFile memory into a Flash Drive which can be used exactly as if it were a standard hard drive. ROM-DOS is a flexible, small and fast compatible DOS. More information on the differences between ROM-DOS and DOS standard can be found on the utilities Disk 1 under *a:\docs\romdos.doc.*

With AFFS and ROM-DOS installed the SCPC486 will boot directly from the FlashFile memory which appear as the C:\drive. If a hard drive is connected to the SCPC486 it must be configured in the BIOS setup as the C:\ drive. The AFFS will over-ride this setting and allocate the FlashFile memory a C:\ and the hard drive as D:\. The AFFS FlashFile drive can be disabled so that the hard drive appears as the C:\ drive by typing:

```
a:\affs\blowbios
```

To recover the AFFS FlashFile drive the SCPC486 should be booted from the utilities Disk 1 and the AFFS and ROM-DOS re-installed.

Additional Equipment Required

In order to construct a basic system the following items will be required:

- A VGA CRT Monitor.
- An IBM PC AT Compatible Keyboard.
- An Arcom PCIF2 and a 10 Way and 14 Way Ribbon Cable.
- A 1.44Mb Floppy Disk Drive and 34 Way Ribbon Cable.
- An STEbus rack with power cables for disk drives.
- A bootable floppy disk containing MS-DOS.

An IDE hard disk system will be described later in this chapter.

Floppy Disk cables and links

The SCPC486 floppy disk interface has been designed to operate with two drives attached to a non-twisted 34 way ribbon cable. This means that the floppy disk drives themselves must be configured as drive A or drive B. This is done with linked on the floppy disk drive. The floppy disk drive must be configured as drive 0 for drive A and drive 1 for drive B. Floppy disk manufacturers usually ship all their drives linked as drive 1 for use with a ribbon cable with a twist; therefore a link generally has to be changed on the floppy disk drive when installing drive A.

Installation

Note: Ensure that no power is applied to the STEbus rack before starting this installation.

1. Check (and change if necessary) the position of the battery link LK5.
2. Place the SCPC486 onto the sliders of a rack slot but do not push home into the bus connector. (STEbus does not require any particular slot to be used.)
3. Connect the ribbon cables between the SCPC486 and the PCIF2. Connect the VGA monitor and the keyboard to the PCIF2.
4. Configure the floppy disk drive as drive 0. (This will probably require a link change on the disk drive, refer to the documentation supplied with the drive.)
5. Connect the 34Way ribbon cable to the floppy disk drive and the SCPC486. Ensure that the ribbon cable is correctly oriented at the floppy disk drive. Connect the power to the floppy disk drive.
6. Push the SCPC486 home into the back plane connectors.

The basic system is now ready to be powered up.

Switching On

Insert the floppy disk into the disk drive and apply power to the rack.

As the battery link has been removed during transit, the CMOS RAM will be corrupt and the board will need to set up . Hold down the DEL key and CMOS set-up will be entered. Set the time, date and the floppy disk type from the Standard Set-up Icon and then press the ESC key. Save the changes and exit the set-up utility.

Because of the speed of the DX4 microprocessor, the SCPC486 processes the memory test extremely quickly and you may not press the DEL key fast enough. If this occurs you will probably get a message "Hit F1 to continue". Although this message is displayed, the F1 feature has been disabled to permit setup information being restored from the EEPROM. It will be necessary to re-boot with CTRL-ALT-DEL and use the DEL key to enter the setup screens.

The SCPC486 will now re-boot, the floppy disk drive will be accessed and MS-DOS will boot. If this process does not occur, please refer to the troubleshooting section.

Adding An IDE Hard Disk Drive

Additional Equipment Required

In order to add an IDE hard disk drive you will need the following:

- An IDE hard disk drive.
- A 40 Way ribbon cable.
- Operating system installation disks. (e.g.. MS-DOS or Windows 95)

Installation

Note: This installation assumes that you have already constructed the basic system described above.

Ensure that the system is powered off before attempting to attach the hard disk drive:

1. Slide the SCPC486 partially out of the STEbus rack in order to access the 40 Way connector on the board.
2. Note the disk parameters for your disk drive. You may need to know the number of tracks, the number of sectors per track and the number of heads that your particular drive uses. This is normally printed on a label on the disk drive, if it is not, consult the documentation supplied with the drive.
3. Attach the 40 Way ribbon cable between the hard disk drive and the SCPC486. Ensure correct cable polarity at the drive end.
4. Attach a power connector to the hard disk drive.
5. Slide the SCPC486 back into the STEbus rack and ensure that it is fully engaged into the backplane.

IDE Drives Greater Than 528Mb

Drives greater than 528Mb use what is termed as LBA (Logical Block Address) mode to access the full capacity of the drive. The SCPC486 supports LBA mode but it had to be enabled in the BIOS "Advanced" setup menu before the drive will operate to its full capacity.

To accomplish this, press the DEL key to enter the setup screen during power on, and in the Advanced options at the end of the menu, enable the LBA mode for "Primary Master" if the drive is C: or "Primary Slave" if the drive is the second in the system (D:). Now you can use the auto detect utility as described below.

Configuring the SCPC486 with a hard disk

All SCPC486 boards that have on-board FlashFile memory fitted will be supplied with AFFS and ROM-DOS fitted. This means that an additional hard drive connected to the system will appear as the D:\drive.

Note: Although the AFFS FlashFile drive appears as the C:\ drive if a hard drive is connected to the SCPC486 it should still be configured within the BIOS set-up as the C:\ drive. On boot up the AFFS will reallocate the hard drive to D:\ and install the FlashFile drive as C:\.

Insert the operating system installation disk into the floppy disk drive and power up the STEbus rack and enter the BIOS set-up utility by pressing the **DEL** key when instructed.

Using the **TAB** key, move to the utilities window. SElect the **Detect Master** icon and press **ENTER**. The SCPC486 will then interrogate your disk drive and return with the parameters against those noted down above and if correct, accept them.

In the unlikely event that the **Detect Master** fails to correctly find your disk, press **TAB** to the set-up window and select the **standard set-up icon**. Now select the **Master Drive** item and page down to **Type 47**. Press **ENTER** and manually enter the settings noted down.

Press **ESC** until prompted to save the BIOS settings. Select **Save Settings and Exit** and the SCPC will reboot.

The operating system will now be installed onto the hard disk drive. Consult the documentation supplied with the operating system for installation instructions.

When the installation is complete, remove any floppy disks from the disk drive and reboot the computer (this will probably be incorporated in the installation procedure for the operating system). The SCPC486 will then boot from the installed operating system on the hard disk.

Installing a flat panel display interface

You will require a flat panel interface module (FPIF) in order to connect the SCPC486 to a flat panel display. As each display generally requires its own unique FPIF, please contact Arcom sales department for more information on availability of FPIFs for the SCPC486.

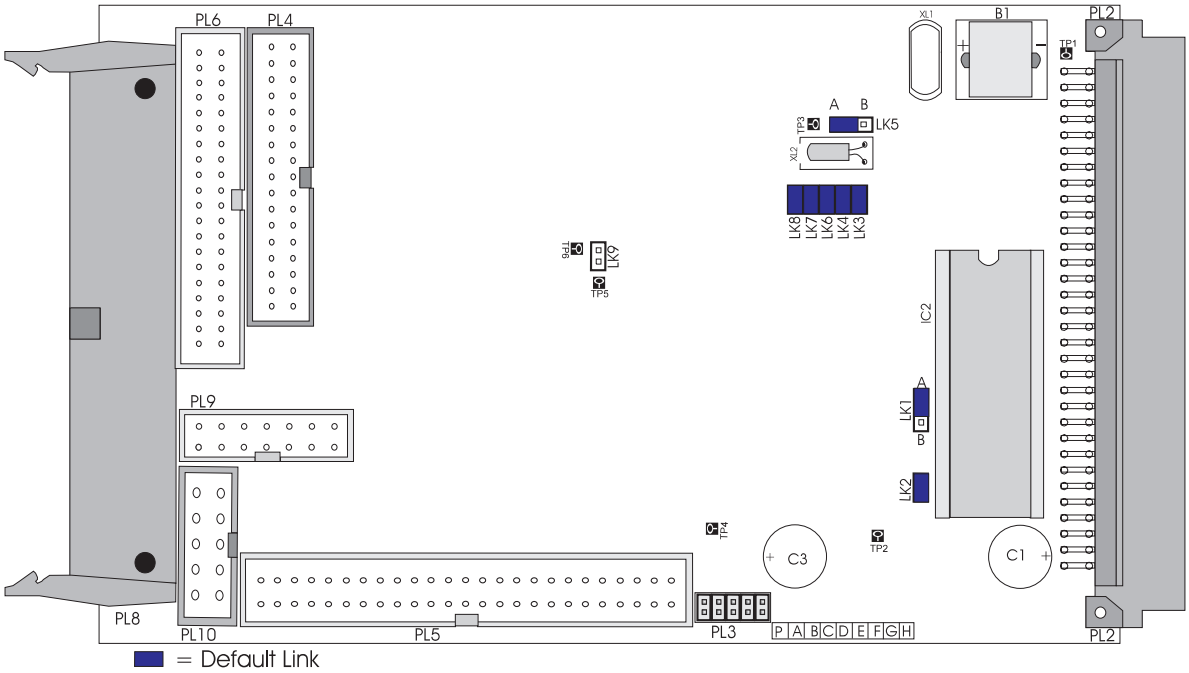
Configuring the Flat Panel Interface

Flat panels required the Video BIOS to be re-configured. Follow the instructions supplied with the FPIF from Arcom.

Section 3. Links & Options

There are nine user selectable links on the SCPC486. Most of these are used to configure the STEbus controller which operates independently of the CPU core.

Default Link Position Diagram



STEbus Reset and Clock Drive Links

LK1 - STEbus Reset Link

The SCPC486 can either generate the STEbus SYSRST* signal or use this signal to derive the on-board reset.

LK1	Description
A+	SCPC486 generates SYSRST* whenever CPU in reset.
B	SCPC486 is reset by SYSRST* asserted.

The SYSRST* generated by the SCPC486 conforms fully with the requirements of IEEE1000.

Normally the SCPC486 would generate the SYSRST* signal unless it is used in a multi-master system where another board is providing all the system controller functions.

LK2 - STEbus Clock Drive Link

The SCPC486 can be used to generate the STEbus SYSCLK signal.

LK2	Description
Fit +	SCPC486 generates SYSCLK.
Omit	SYSCLK generated by another board in system.

The SYSCLK generated by the SCPC486 conforms fully to the requirements of IEEE1000.

Normally SYSCLK would be generated by the SCPC486 unless it is used in a multi-master system where another board is providing all the system controller functions.

Note: Although the SCPC486 generates the SYSCLK signal, it does not itself require this clock line because the STEbus interface on the SCPC486 is entirely asynchronous.

STEbus Arbiter Configuration Links

The SCPC 486 can operate in an STEbus multi-master system as either a default of potential master. All system arbiter functions conform to the IEEE1000 standard.

LK3 - Arbiter Select Link

In a default master system the SCPC486 must provide the STEbus arbiter: in a potential master system an external arbiter is required.

LK3	Description
Fit +	SCPC486 provides system arbiter (Default Bus Master).
Omit	SCPC486 uses external arbiter (Potential Bus Master).

Definitions of default and potential master are found in the IEEE1000 specification document.

The SCPC486 would always be configured as the default bus master in a single master system. In a multi-master system the SCPC486 would normally be configured as the default master if it uses the STEbus more than other masters in the system, otherwise it would be configured as a potential master.

LK4 - Arbiter Level Select

If the SCPC486 is configured as a potential bus master (LK3 omitted), this link defines which of the bus request signals will be used by the SCPC486 when it arbitrates for control of the bus. This link has no effect if the SCPC486 is configured as a default bus master.

LK4	Description
Fit +	SCPC486 asserts BUSRQ0* during arbitration.
Omit	SCPC486 SCPC asserts BUSRQ1* during arbitration.

The IEEE1000 standard does not specify the method of arbitration to be used by a system controller, but nominally BUSRQ0* is assumed to have a higher priority than BUSRQ1*.

The SCPC486 applies this bus prioritisation when the on-board arbiter is used.

Battery Link

A battery link is fitted that is used to prevent drain on the battery during shipment. This link can also be used to clear the content of the CMOS set-up RAM.

LK5 - Battery Link

It is necessary to change this link from its default setting before battery backup of the SCPC486 will be enabled.

LK5	Description
A+	Battery back-up is disabled (CMOS RAM cleared).
B	Battery back-up enabled.

COM1 Redirect Link

There are instances where it is desirable for COM1 to be installed as a card on the STEbus such as when using an STEbus modem card.

LK6 - COM1 Redirect

LK6	Description
Fit +	COM1 on SCPC486 is used.
Omit	COM1 is used on the STEbus.

Normally COM1 on the SCPC486 would be used.

User Links

Two user links are provided on the board that are read at special function register I/O 025Ch.

LK7, 8 - User Links

The user links are intended entirely for customer use and no restriction on their use is made by Arcom.

LK7,8	Description
Fit +	Corresponding bit in special function register reads 0.
Omit	Corresponding bit in special function register reads 1.

Local Bus Video Disable Links

It is sometimes desirable to use a video display card on the STEbus rather than the on-board local bus video. LK9 is used to disable the local bus video display as follows:

LK9- VGA Redirect Links

LK9	Description
Omit +	On board local-bus VGA used.
Fit	OmitSTEbus VGA used.

Note: Local bus VGA graphics are in the region of 7 times faster than VGA using an STEbus board.

Note: *When Link LK9 is fitted, I/O address 3C3h is still directed to the local bus VGA and is not available on the STEbus.*

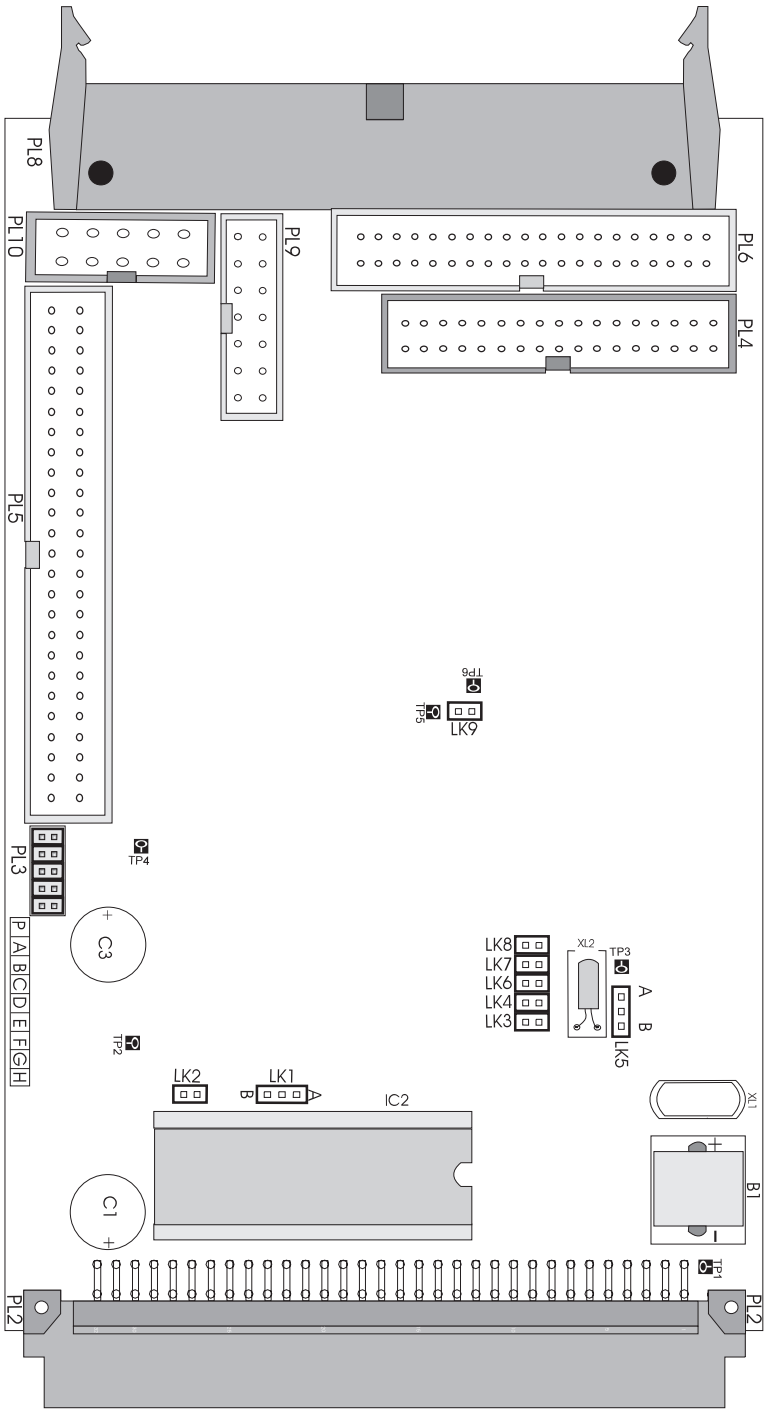
This means that only VGA boards that use address 46E8h as the enable register can function with the SCPC486. Both of Arcom's VGA boards, the SQVGA and the SPVGA are compatible for use with the SCPC486.

Note, however that V1 Ix versions of the SPVGA will not function with the SCPC486.

User Configuration Record Diagram

This page may be duplicated.

User Configuration Record Table	
Link	**Position**
LK1	
LK2	
LK3	
LK4	
LK5	
LK6	
LK7	
LK8	
LK9	



Section 4. Using the SCPC486

Getting Started

Please ensure that you have read the Getting Started Section of this manual as it contains important information that should be used in conjunction with this section.

Using the STEbus

STEbus is a high reliability 8 bit backplane system, ideal for industrial I/O applications with powerful facilities for multi-processing and exception handling.

Boards on the STEbus are classed as either **bus masters** or **slaves**. A bus master can initiate a bus transfer whereas a slave can only respond to one. Both bus masters and slaves can be placed in any slot of the STEbus backplane. Generally, bus masters are CPU boards which access I/O or peripheral slave boards, however some slave boards may also contain microprocessors.

The **SCPC486** is an IBM PC AT compatible STEbus bus master and can be used either as the only bus master in the system (which is most generally the situation) or can be used with up to two other bus masters.

When there is more than one bus master in a system, one must be a **Default** bus master and the others are **Potential** bus masters. The default bus master contains a bus-arbiter which controls which bus master has access to the bus through the bus arbitration request signals **BUSRQ0*** and **BUSRQ1*** (and their corresponding acknowledge signals BUSAK0* and BUSAK1*). The default bus master has control of the bus when neither of the potential bus masters need it. When a potential master requests the bus an arbitration sequence begins which gives control to one or other of the requesting boards. The arbiter on the SCPC486 gives highest priority to BUSRQ0* which is nominally specified in the STEbus specification.

Bus arbitration is entirely handled by hardware and is transparent to any software running on any of the bus masters. Once the appropriate links are configured on each of the masters in an STEbus system, its operation is invisible. If you are using the SCPC486 as the only CPU board in your system, you do not need to change any of the links on the board relating to the STEbus interface for the board to work optimally with the STEbus.

Accessing slaves on the STEbus is as easy as accessing peripheral cards in a standard desktop PC. The slaves should be configured at I/O and Memory addresses that correspond to STEbus locations in the following memory and I/O maps.

There-after, simply accessing these locations from the SCPC486 will access the slave boards.

There are eight exception signals on the STEbus (**ATNRQ0*** to **ATNRQ7***) which are mapped into the interrupt controllers on the SCPC486 (see the following sections). This facility allows slave boards to signal the SCPC486 for attention in the same way that a PCbus peripheral card would assert an interrupt.

Finally, all transfers on the STEbus are monitored by a bus controller that terminate any bus cycles that exceed a given time. This is necessary as STEbus transfers are normally terminated by a slave board; if there is an STEbus access to a location that no board responds to, the bus cycle will continue indefinitely. The SCPC486 has a programmable bus time-out for either 4, 8 or 16µS or can be disabled if an external bus controller is available.

Memory Map

Address	Block Size	Description
00100000h	15Mb	External Memory
000F0000h	64Kb	System BIOS ROM
000D0000h	128Kb	STE, Used by Peripheral
000CC000h	16Kb	Flash EPROM
000C8000h	16Kb	BIOS External Memory
000C0000h	64Kb	VGA VIdeo BIOS
000A0000h	128Kb	Video RAM real Mode Window
00000000h	640Kb	System RAM

STEbus Memory Space

Addresses between Dooo:oooo and Eooo:FFFF are mapped onto the STEbus and are therefore available for memory mapped slave boards. However, when an STEbus peripheral uses part or all of this memory, it is necessary to instruct any memory management software running on the SCPC486 (such as Microsoft EMM386 or the Windows 95 memory manager) not to make this available for loading programs into high memory. Refer to the documentation supplied with the memory manager that you are using.

Flash EPROM

Please refer to the section on AFFS and ROM-DOS which is installed to all SCPC486 boards with Flash memory.

If you have a board populated with Flash EPROM memory, you must also exclude the memory region from any Memory Management Software (Such as EMM386).

I/O Map

46E8h	1	VGA	STEbus	VGA enable register	(1)
400h-FFFh	3K	-	STEbus	Available for slave I/O boards	
3F8h-3FFh	8	COM1	SCPC486	Communications Controller for COM1	(2)
3F0h-3F7h	8	Disks	SCPC486	Floppy and Hard Disk Drives	
3E0h-3EFh	32	-	STEbus	Available for slave I/O boards	
3B0h-3DFh	48	VGA	SCPC486	VGA Control Registers	(3)
300h-3AFh	176	-	STEbus	Available for slave I/O boards	
2F8h-2FFh	8	COM2	SCPC486	Communications Controller for COM2	
280h-2F7h	120	-	STEbus	Available for slave I/O boards	
278h-27Fh	8	LPT1	SCPC486	Parallel Port LPT1	
60h-277h	24	-	STEbus	Available for slave I/O boards	
258h-25Fh	8	Specia	SCPC486	Special Function Registers	(4)
1F8h-257h	96	-	STEbus	Available for slave I/O boards	
1F0h-1F7h	8	Disks	SCPC486	IDE hard disk interface	
100h-1EFh	240	-	STEbus	Available for Slave I/O Boards	(5)
0F0h-0F1h	2	PC AT	SCPC486	Coprocessor Registers	(6,7)
0C0h-0DFh	32	PC AT	SCPC486	DMA Controller 2	(6,7)
0A0h-0A1h	2	PC AT	SCPC486	Interrupt Controller 2	(6,7)
092h	1	PC AT	SCPC486	PS/2 Fast Reset Register	(6,7)
081h-08Fh	15	PC AT	SCPC486	DMA and Refresh Page Registers	(6,7)
080h	1	PC AT	SCPC486	POST Diagnostics POD output (write Only)	
070h-071h	2	PC AT	SCPC486	Real Time Clock Registers	(6,7)
064h	1	PC AT	SCPC486	Keyboard Controller Register	(6,7)
061h	1	PC AT	SCPC486	Control/Status Register	(6,7)
060h	1	PC AT	SCPC486	Keyboard Controller Register	(6,7)
040h-043h	4	PC AT	SCPC486	imer Counter Register	(6,7)
022h-023h	2	SIS471	SCPC486	CHIPset Configuration Registers	
020h-021h	2	PC AT	SCPC486	Interrupt Controller 1	(6,7)
000h-00Fh	16	PC AT	SCPC486	DMA Controller 1	(6,7)

Notes:

(1) This I/O location actually outside STEbus range.
(2) Maps to STEbus if link LK6 removed.
(3) Maps to STEbus if link LK9 is fitted except for location 3C3h
(4) See later in this section for details.
(5) Avoid 102h as this is used by some VGA boards.
(6) See suitable PC AT reference manual for details.
(7) No address between oooh and oFFh is available on STEbus except writes to o80h

Special Function Registers

Special Function Register Descriptions

There are six special I/O registers locations specific to the SCPC486. These are presented in the following table:

I/O Address	Description
258h	Flash Memory Control Register1/Status
259h	Flash Memory Control Register 2
25Ch	User Register
25Dh	Watchdog/Status Register
25Eh	STEbus Configuration register
25Fh	Peripheral Register

The following registers are implemented:

Flash Memory (258h, 259h), (Only if fitted)

Bit 7	6	5	4	3	2	1	Bit 0
X	X	X	IE	FPA3	FPA2	FPA1	FPA0

Bit 7	6	5	4	3	2	1	Bit 0
X	X	X	FPA8	FPA7	FPA6	FPA5	FPA4

The registers are normally accessed by the Arcom Silicon Drive Software. This information is included for reference only.

Signal	Reset	Description
FPA0 - FPA8	0	Flash Memory Control Register1/Status
IE	0	Flash Memory Control Register 2

User Register (25Ch)

SCLK, SDTA are normally only accessed by the Arcom E PROM utility programmes. The Information included here is for reference only.

Bit 7	6	5	4	3	2	1	Bit 0
LED	X	LINK1	LINK0	X	X	SCLK	SDTA

Bit	State	Access	Description
SDTA	0	R/W	=0 Floats Line
SCLK	0	R/W	=0 Floats Line to (0V)
LINK0	-	Read	=0 Link Fitted
LINK1	-	Read	=0 Link Removed
LED	0	R/W	Lights LED when set to (1)

Watchdog/Status Register (25Dh)

Bit 7	6	5	4	3	2	1	Bit 0
VGA_STE	COM_STE	ARB_LVL	EXT_ARB	X	X	BTO_FLAG	WDOG_RUN

A read on this register clears the bus TIme-out flag.

Bit	Reset	Access Type	Description
WDOG_RUN	0	Read Only	=1 When Watchdog is enabled
BTO_FLAG	0	Read Only	=1 When bus Time-out occurred
EXT_ARB	✢	Read Only	=0 For default master STE =1 For potential master STE
ARB_LVL	✢	Read Only	Arbitration level for potential master
COM_STE	✢	Read Only	If COM1 re-mapped to STE
VGA_STE	✢	Read Only	If VGA re-mapped to STE
✢ = Dependant on Links Settings			

Writing to this register enables watchdog and flash BIOS reprogramming. The watchdog is disabled on power up and is enabled by writing consecutively the values of (33h) and (CCh) to this register location.

There-after a write sequence of (55h) and (AAh) must be applied to this register within the watchdog Time-out period (1 second) to prevent a full system reset.

System Reset State	Description
Enabled Operation	Write Sequence 33h, CCh
259h	Write Sequence 55h, AAh

This register is also used when the BIOS is re-programmed. A write sequence of 33h, 99h remaps the BIOS ROm so that it can be re-programmed. The remapping is as shown in the following table:

E000 : 0000 (64K)	Lower 64K EPROM
D000 : 0000 (64K)	Upper 64K EPROM

Certain disk operations (such as accessing the floppy disk) may take longer than the nominal 1 second time-out period and the Watchdog may cause a reset in this situation when the software is actually functioning normally. To prevent this occurring, it is possible to disengage the Watchdog by writing the sequence 55h;66h to the register. Once disengaged, the watchdog is re-engaged by writing the normal enable sequence to the register.

STEbus Configuration Register (25E)

Bit 7	6	5	4	3	2	1	Bit 0
BTO1	BTO0	BTO_M	IE_ATN7	IE_ATN5	IE_ATN1	IE_ATN1	IE_ATN0

Interrupt mapping for STEbus is achieved by using bits (0-4) in this register.

Bit	Reset	Access	Description
IE_ATN0	0	R/W	ATNRQ0* Maps to NMI when set
IE_ATN1	0	R/W	ATNRQ1* Maps to IRQ3 when set
IE_ATN2	0	R/W	ATNRQ2* IRQ4 when set
IE_ATN5	0	R/W	ATNRQ5* IRQ7 when set
IE_ATN7	0	R/W	ATNRQ7* IRQ12 when set

Note: IE_ATN1 has no effect when COM1 is mapped to STEbus
IE_ATN7 when set prevents the use of the PS/2 Mouse Port.

STEbus Bus Time-out is programmable using the following bits in this register.

Bit	Reset	Access	Description
BTO_M	0	R/W	Bus Time-out Compatibility
IE_ATN1	0	R/W	Bus Time-Out Period Select
IE_ATN2	0	R/W	Bus Time-out Period Select

BTO_M is used to set the compatibility with other boards on the STEbus. When clear, a bus Time-out will not assert TFRERR*. When set, TFRERR* will be asserted on bus Time-out to all boards on the STEbus.

Note: For multi master operation with the SCIMX and other Arcom CPU boards, leave BTO_M clear.

Time-out period is defined in the following table.

BTO1	BTO0	Description
0	0	(Reset State) Time-out Nominally> 16 us
0	1	(Reset State) Time-out Nominally> 8 us
1	0	(Reset State) Time-out Nominally> 4 us
1	1	Bus Time-out Disabled

Warning: Never set BTOo and BTO1 unless a dully compliant STEbus Arbiter is available extremely on STEbus. The SCPC486 will fail to operate otherwise.

Peripheral Configuration Register

Bit 7	6	5	4	3	2	1	Bit 0
NMI-COM2	X	X	X	X	IE_LPT1	IE_COM2	IE_CPM1

Bit	State	Access Type	Description
IE_COM1	1	R/W	Maps COM1 IRQ to IRQ4
IE_COM2	1	R/W	Maps COM2 IRQ to IRQ3
IE_LPT1	1	R/W	Maps LPT1 IRQ to IRQ7
NMI-COM2	0	R/W	Maps COM2 IRQ to NMI

Note: IE_COM1 will be clear if COM1 is mapped to STEbus.

Interrupts

IRQ Map

Interrupt	Links	Register Bits	Description
NMI		25E(0), 25F(7)	TFRERR/COM2/ATNRQ0
IRQ3		25E(1), 25F(1)	COMJ2/ATNRQ1
IRQ4	LK1	25E(2), 25F(0)	COM1/ATNRQ2
IRQ5			ATNRQ3
IRQ6			FLOPPY
IRQ7		25E(0), 25F(7)	LPT1/ATNRQ5
IRQ9			BUS TIME-OUT
IRQ10			ATNRQ4
IRQ11			ATNRQ6
IRQ12		25E(4)	MOUSE/ATNRQ7
IRQ14			IDE
IRQ15			FLASH MEMORY (IF FITTED)

Using interrupts on the SCPC486

The IRQ lines on the PC compatible interrupt controller are either connected directly to the interrupt sources or masked by special function registers 25Eh and 25Fh.

Where there is a direct connection between the IRQ line and the STEbus ATNRQ signal (such as ATNRQ3*, ATNRQ4* and ATNRQ6*) the interrupt only needs to be unmasked in the interrupt controller for it to be used. By default, the BIOS masks all unrecognised interrupts so that any ATNRQ line activity on the STEbus will be ignored until it is unmasked in the interrupt controller.

Where an IRQ line is shared between an on-board interrupt source and an STEbus ATNRQ signal, care must be undertaken to enable only the interrupts that are required in registers 25Eh and 25Fh and that software handlers are installed before writing to the registers. Interrupts still have to be unmasked in the interrupt controller as described above.

The STEbus ATNRQ signals are defined as active low signals. However, PC type architecture only generates an IRQ to the CPU on the first active edge. Therefore, if more than one card on the STEbus can assert an ATNRQ signal, the software handler must poll all possible interrupt sources on the STEbus before clearing sown the interrupt controller, otherwise interrupts may be lost.*

Using the Battery and Battery Link

The SCPC486 is fitted with a cadmium free rechargable battery for standby power to the real time clock and CMOS RAM stepup information.

When the board is supplied by Arcom, the battery will be partially charged but the battery link LK5 will have disconnected the battery from the circuitry on the board. Move the battery link LK5 to enable battery backup. (Consult section 3, Links and Options.)

The battery will be fully charged after 100 hours use of the board and the standby period at 25°C is in excess of 30 days Beyond this period the Arcom Lock CMOS utility can be used to store the CMOS configuration into the on-board EEPROM. (See later for details.)

Additional On-Board Features

The SCPC486 contains a number of features that make it ideal for industrial applications:

User Links

Links LK7 and LK8 are available on the board for user configuration information and are entirely uncommitted by Arcom. These links can be read at I/O location 25Ch and could be used for configuring software or identifying a system build status.

User LED

The red LED on the front edge of the SCPC486 is available for use with your application software. This can be useful for indicating when a fault has occurred that requires the intervention of an engineer or to give a heartbeat indication to show that the system is working properly.

Watchdog

The watchdog feature of the SCPC486 provides a deadman timer facility so that should a system lock-up occur, a full system reset is instigated.

The watchdog facility is disabled on power-up and is enabled by writing the sequence of bytes 033h and 0CCh to I/O location 25Dh.

Once enabled, a write sequence of byte value 055h followed by 0AAh must occur within the minimum time-out period (1 second) to prevent the SCPC486 from resetting. (The reset signal will generate an STEbus SYSRST* if link LK1 is positioned accordingly.)

Configuring the STEbus

This section describes the link settings to use for the STEbus in a variety of STEbus configurations:

SCPC486 Is Only CPU Board in System

In this situation, the SCPC486 is the Default Master and Bus Controller. the link positions that you would require are as follows:This is the most commonly used link setting.

Link	Description	Position	Action
LK1	SYSRST Link	A	SCPC486 Generates SYSRST* Signal
LK2	SYSRST Link	Fit	SCPC486 Generates SYSCLK* Signal
LK3	Arbiter Link	Fit	SCPC486 Arbiter used for STEbus
LK4	Arbiter Level Link	X	Don't Care

SCPC486 Used in System also containing Slave CPU boards

Use the same link positions as above as te slave CPU boards are not STEbus masters.

Multi-master System (SCPC486 Heaviest STEbus usage)

Configure the SCPC486 links as in the above table. The SCPC486 is the Default bus master. Configure the other bus masters as Potential bus masters, one using BUSRQ0* and the other using BUSRQ1*. Ensure that the other bus masters do not generate the SYSCLK signal and are configured to accept the SYSRST* signal as an input.

Multi-master System (SCPC486 Occasional STEbus usage)

Configure the SCPC486 as a potential bus master (using LK4 to select the arbitration level). The link settings are as follows:

Link	Description	Position	Action
LK1	SYSRST Link	B	SCPC486 uses SYSRST* signal as input
LK2	SYSRST Link	Omit	SCPC486 doesn't generate SYSCLK* Signal
LK3	Arbiter Link	Omit	SCPC486 uses an external STEbus arbiter
LK4	Arbiter Level Link	Fit/Omit	Fit for BUSRQ0*. Omit for BUSRQ1*

Using a VGA Card on the STEbus

It may be desirable to use an STEbus VGA controller to provide the graphics support for the SCPC486 (such as Arcom's quarter sized VGA controller card - SQVGA).

To do this, link LK9 should be fitted. This will direct all relevant VGA accesses to the STEbus except accesses to I/O location 3C3h. This means that VGA controller cards have to operate at the VGA adaptor enable location at I/O 46E8h.

Arcom's SQVGA and SPVGA (from production state V2I1 onwards) and a MOD404 mounted on an SSIP carrier card are fully compatible as alternative VGA devices for the SCPC486.

Using an STEbus Board for COM1

In some instances an STEbus board may be required to provide COM1 (for example a Modem Card). To accomplish this remove link LK6.

STEbus Specification

STEbus is an international standard and is ratified by the Institute of Electrical and Electronic Engineers under standard IEEE1000. This publication is available from them. See the bibliography (Appendix D) for details.

Utility Disks

Three utility disks are provided with the SCPC486: Disk 1 contains the EEPROM utility programs LOCKCMOS and STE_LOCK as well as a complete copy of AFFS and ROM-DOS 6.22 utilities, Disk 2 contains the Windows 3.1 drivers and utility programs for the VGA controller and Disk 3 contains the DOS drivers and utility programs for the VGA controller.

Disk 1 - AFFS, ROM-DOS and EEPROM Utilities

Disk 1 contains a complete installation of AFFS (Arcom Flash Filing System) and all the standard ROM-DOS 6.22 utilities supplied by Datalight. The file `a:\docs\rduser.exe` is a self extracting manual for all the ROM-DOS utilities supplied. The disk also boots to a menu that allows you to reformat the on-board FlashFile memory and re-install ROM-DOS. Simply boot the SCPC486 from this floppy and follow carefully the on-screen instructions. This option is only for use if the FlashFile memory has become corrupted in some way.

The disk also contains two utility programs called LOCKCMOS.EXE and STE_LOCK.EXE which allow you to use the EEPROM to save the configuration information stored in the battery backed CMOS and also to load the STEbus interrupt mapping registers automatically at boot-up time. Please refer to the text files on the disk for more information.

Disk 2 - Windows 3.1 Drivers for VGA

This Disk contains a Windows installation utility called INSTALL.EXE which must be run from Windows. Ensure that Windows is configured for standard 16 colour VGA mode before attempting to install this disk.

Note that Windows 95 will automatically detect and configure for the Cirrus Logic 6245 VGA controller and will not require this disk.

Disk 3 - DOS Drivers for VGA

To install the DOS drivers and utilities for the Cirrus Logic 6245 VGA controller you need to run the program INSTALL.EXE from the DOS prompt.

This is a menu driven installation utility and there is a file READ.ME which contains the latest installation information.

Section 5. Troubleshooting

Note that the VGA controller device (the Cirrus Logic 6245) configures the CRT interface on power up. If it detects that a monitor is not fitted, no VGA output is directed to the CRT connector. You can force it to generate the CRT signals by running the utility program CRT.EXE (from Disk 1) in your AUTOEXEC.BAT file, or alternatively ensure a VGA monitor is connected at power-up.

Note that the following suggestion table assumes a system contains a PCIF2-EMC breakout board fitted with a speaker to hear the error codes.

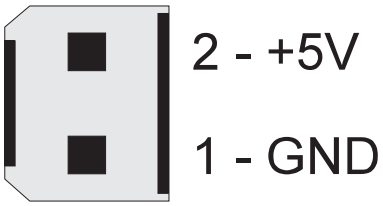
Problem	Suggestions
On power up, no display on screen and no beeps.	Check the power is is properly applied to the system. Check the links for the bus arbitration are appropriate for your installation. If problem persists contact Arcom's Customer Support.
System has no display but beeps once on power up.	This is likely to be CRT detect system on the VGA controller. Please see above.
System has no display and beeps more than once on power up.	Check CRT detect system (see above) and battery link. Check that link LK9 is omitted for local bus graphics, or, if fitted, the STEbus VGA controller is functioning correctly.
Can't access floppy disks.	Ensure that the drive links are configured correctly. The SCPC486 expects drive A: to be configured as drive 0 and B: as drive 1 when using a non-twisted ribbon cable. Note that 360Kb & 720Kb drives are not supported by the SCPC486.
Can't use hard disk capacity above 528Mb.	In the advanced section of the CMOS setup, enable 32 bit LBA access mode for the hard disk drive.
Can't access Flash Memory.	Check that Flash Memory is fitted to the board. Check that any memory managers in the system exclude region CC00h-CFFFh
Can't access STEbus memory mapped slaves.	Check that slaves are mapped into memory D000:0000h to E000:FFFFh. Check that any memory managers in the system exclude the memory regions that you are using.
Multi-master system just won't work!	Check the SYSCLK links on all masters to ensure that there is only one source for this signal.
Multi-master system with SCIMX; SCIMX reports parity error.	Ensure that the BTO_M bit in register I/O 25Eh is not set. This mode is not compatible with the SCIMX or other Arcom CPU boards.
CHECKIT Memory Tests.	The PC test program CHECKIT will cause a system reboot during its memory tests if EMM386.SYS is loaded. Note that this is a failure in CHECKIT and occurs on all PC's.
PS/2 Mouse Problems.	To use the PS/s mouse it must be installed in the PCIF2-EMC mouse connector at power up, and you cannot use the ATNRQ7* as an interrupt line for the SCPC486.

Appendix A. Specifications

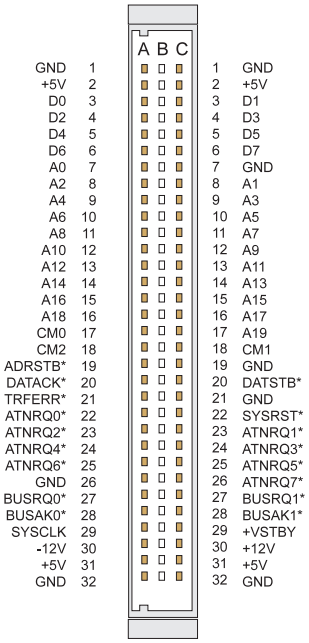
Microprocessor	Intel 80468DX4	
Speed	100MHz	
Memory	4, 8 or 16Mb DRAM 2 or 4Mb Flash EPROM 256byte serial EEPROM	
VGA Video	Cirrus Logic CL-GD6245 32bit Local Bus VGA Controller 512Kb Video DRAM Flat Panel Support for 640 by 480, dual-/single-scan colour/mono STN LCD's and colour/mono TFT LCD's	
Resolution	CRT Resolution	Colours
	640 x 480	256
	800 x 600	256
	1024 x 768	16
Peripherals	RS232:	COM1, COM2 (16550 UART compatible)
	Centronics:	LPT1 (supports PS/2 Bidirectional Mode)
	Keyboard:	PC AT Style (using PCIF2-EMC)
	Mouse:	PS/2 Style (using PCIF2-EMC)
	Floppy	2 off high density drives
	IDE:	Master & Slave support (including 32bit LBA mode)
Temperature	Operating: 0 to 55°C Storage: 0 to 70°C	
Humidity	10 to 80% RH (non-condensing)	
Power Requirements	+5V ± 5%	1.25A (typical), 2.0A (max)
Battery	NiMH:	30 day standby period (at 25 ºC) 100hrs charge time
Dimensions	160 x 100 mm	
Weight	153g	
MTBF	>75,000hrs Based on MIL-SPEC-217F using generic failure rates.	

Appendix B. Connections

PL1 - Fan Power

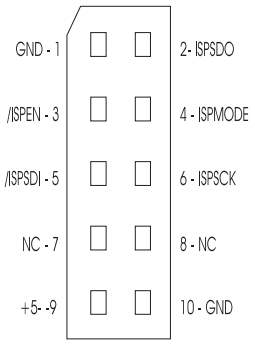


PL2 - STEbus



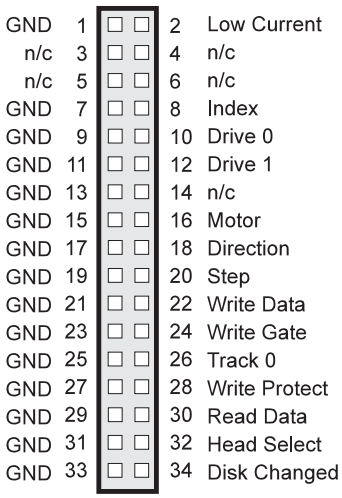
Note that Row B is not used.
A three-row DIN41612 type connector is utilised for VME/STEbus inter-compatibility.

PL3 - ISPLSI PAL Programming Header

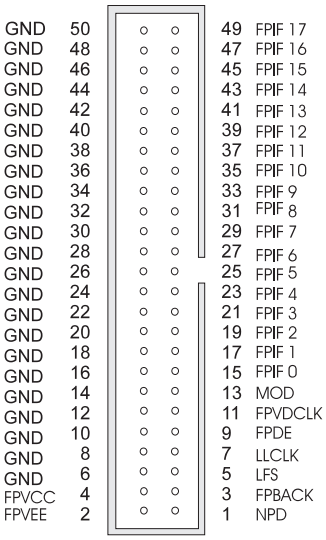


Note: This connector pinout is only included for reference. The Warranty in the SCPC486 will be invalidated if any user connections are made to this connector.

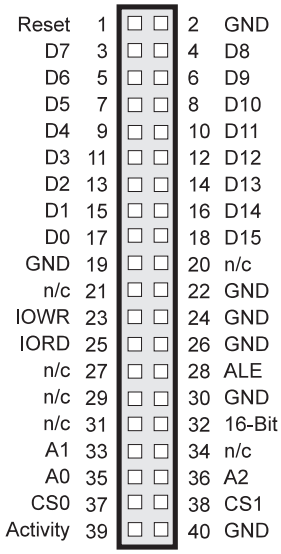
PL4 - Floppy Disk Connector



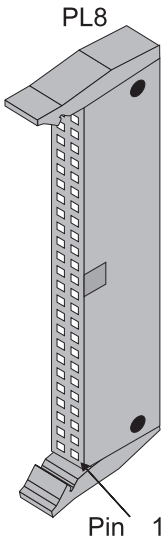
PL5 - Flat Panel Interface Connector



PL6 - IDE Interface



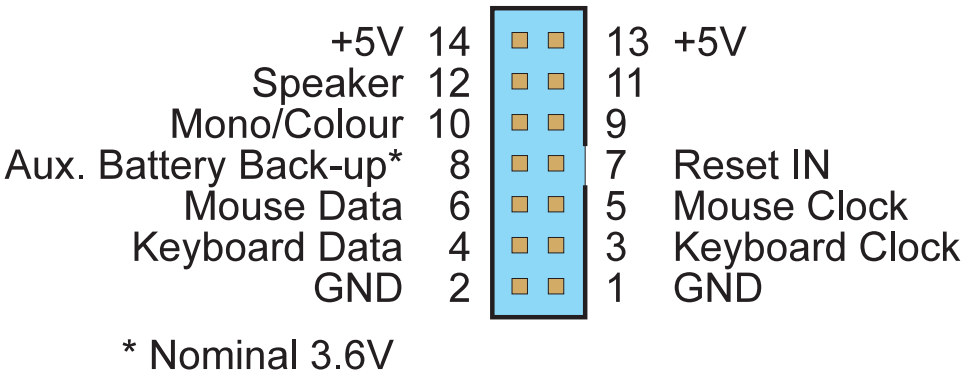
PL8 - COM1,COM2 & LPT1 Connector



Pin Assignment for PL8

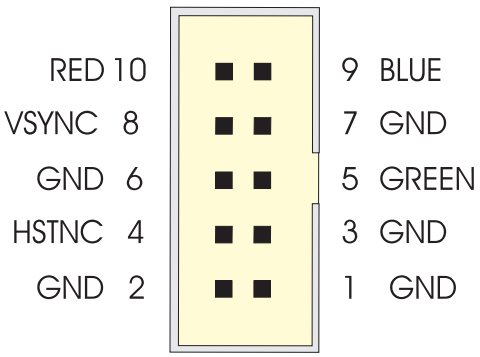
	Signal Title	50-way Pin		Signal Title	
5	**GND**	**50**	**49**	**RIA**	**9**
4	**DTRA**	**48**	**47**	**CTSA**	**8 9-way D type**
3	**TXDA**	**46**	**45**	**RTSA**	**7**
2	**RXDA**	**44**	**43**	**DSRA**	**6**
1	DCDA	42	41	GND	5
9	RIB	40	39	DTRB	4 9-way D type
8	CTSB	38	37	TXDB	3
7	RTSB	36	35	RXDB	2
6	DSRB	34	33	DCDB	1
	n/c	32	31	n/c	
	n/c	30	29	n/c	
	n/c	28	27	n/c	
	n/c	26	25	**Print Selected**	**13**
25	GND	24	23	**Paper End**	**12**
24	GND	22	21	**BUSY**	**11**
23	GND	20	19	**ACK**	**10**
22	GND	18	17	**D7**	**9**
21	GND	16	15	**D6**	**8 25-way**
20	GND	14	13	**D5**	**7 D type**
19	GND	12	11	**D4**	**6 LPT1**
18	GND	10	9	**D3**	**5**
17	Select In	8	7	**D2**	**4**
16	Initialise	6	5	**D1**	**3**
15	Error	4	3	**D0**	**2**
14	Autofeed	2	1	**Strobe**	**1**

PL9 - 14 way Utility Header



* Nominal 3.6V

PL10 - CRT Video Connector



Appendix C. Reference

This section details the BIOS Power ON Self Test (Post) codes that are written to I/O location o8oh during power-up, before the operating system is loaded.

Also included is a description of the audible error codes.

Uncompressed INIT code checkpoints	
C2	NMI is Disabled Power on delay starting.
C5	Power on delay complete. Going to disable Cache if any.
C6	Calculating ROM BIOS checksum.
C7	ROM BIOS checksum passed. CMOS shutdown register test to be done next.
C8	CMOS shutdown register test done. CMOS checksum calculation to be done next.
CA	CMOS checksum calculation is done, CMOS DIag byte written. CMOS status register about to init for Date and Time.
CB	CMOS status register init done. Any initialisation before keyboard BAT to be done next.
CD	BAT command to keyboard controller is to be issued.
CE	Keyboard controller BAT result verified. Any initialisation after KB controller BAT to be done next.
CF	Initialisation after KB controller BAT done. Keyboard command byte to be written next.
D1	Keyboard controller command byte is written. Going to check pressing of *key during power-on*
D2	Checking for pressing of *key during power-on done.* Going to disable DMA and Interrupt controllers.
D3	DMA controller #1, #2, interrupt controller #1, #2 disabled Chipset init/ auto memory detection about to begin.
D4	Chipset initialisation/ auto memory detection over. To uncompress the RUNTIME code.
D5	RUNTIME code is uncompressed.
DD	Transfer control to uncompressed code in shadow RAM at F000:FFF0

Runtime code is uncompressed in F000 shadow RAM	
03	NMI is Disabled. To check soft reset/power-on.
05	Soft reset/power-on determined. Going to disable Cache is any.
06	POST code to be uncompressed.
07	POST code is uncompressed . CPU init and CPU data area init to be done next.
08	CPU and CPU data area init done. CMOS checksum calculation to be done next.
09	CMOS checksum calculation is done, CMOS Diag byte written. CMOS init to begin (if "Init CMOS in every boot" is set).
0A	CMOS initialisation done (if any). CMOS status register about to init for Date and Time.
0B	CMOS status register init done. Any initialisation before keyboard BAT to be done next.
0C	KB controller I/B free. Going to issue the BAT command to keyboard controller.
0D	BAT command to keyboard controller is issued Going to verify the BAT command
0E	Keyboard controller BAT result verified. Any initialisation after KB controller BAT to be done next.
0F	Initialisation after KB controller BAT done. Keyboard command byte to be written next.
10	Keyboard controller command byte is written. Going to issue Pin-23,24 blocking/unblocking command.
1	Pin-23,24 of keyboard controller is blocked/unblocked. Going to check pressing of *key during power-on*.
12	Checking for pressing of *key during power-on done*. Going to disable DMA and Interrupt controllers.
13	DMA controller #1, #2, interrupt controller #1, #2 disabled. Video display is disabled and port-B is initialised. Chipset init about to begin.
15	Chipset initialisation over. 8254 timer test about to start.
19	8254 timer test over. About to start memory refresh test.
1A	Memory Refresh line is toggling. Going to check 15 micro second ON/OFF time.
20	Memory Refresh period 30 micro second test complete. Base 64K memory to be initialised.
23	Base 64K memory initialised. Going to set BIOS stack and to do any setup before Interrupt vector init.
24	Setup required before interrupt vector initialisation complete. Interrupt vector initialisation about to begin.
25	Interrupt vector initialisation done. Going to read Input port of 9042 for turbo switch (if any) and to clear password if post diag switch is on.
26	Interrupt port of 8042 is read. Going to initialise global data for turbo switch.
27	Global data initialisation for turbo switch is over. Any initialisation before setting video mode to be done next.
28	Initialisation before setting video mode is complete. Going for monochrome mode and colour mode setting.
2A	Different BUSes init (system, static, output devices) to start if present. (Please see Appendix for details of different BUSes).
2B	About to give control for any setup required before optional video ROM check.
2C	Processing before video ROM control is done. About to look for optional video ROM and give control.
2D	Optional video ROM control is done. About to give control to do any processing after video ROM returns control.

2E	Return form processing after the video ROM control. If EGA/VGA not found then do display memory R/W test.
2F	EGA/VGA not found. Display memory R/W test about to begin.
30	Display memory R/W test passed. About to look for the retrace checking.
31	Display memory R/W test or retrace checking failed. About to do alternate Display memory R/W test.
32	Alternate Display memory R/W test passed. About to look for the alternate display retrace checking.
34	Video display checking over. Display mode to be set next.
37	Display mode set. Going to display the power on message.
38	Different BUSes init (input, IPL, general devices) to start if present. (Please see Appendix for details of different BUSes).
39	Display different BUSes initialisation error messages. (Please see Appendix for details of different BUSes).
3A	New cursor position read and saved. Going to display the Hit 6 message.
3B	Hit 6 message displayed. Virtual mode memory test about to start.
40	Going to prepare the descriptor tables.
42	Descriptor tables prepared. Going to enter in virtual mode for memory test.
43	Entered in the virtual mode. Going to enable interrupts for diagnostics mode.
44	Interrupts enabled (if diagnostics switch is on). Going to initialise data to check memory wrap around at) 0:0.
45	Data initialised. Going to check for memory wrap around at 0:0 and finding the total system memory size.
46	Memory wrap around test done. Memory size calculation over. About to go for writing patterns to test memory.
47	Pattern to be tested written in extended memory. Going to write patterns in base 640K memory.
48	Patterns written in base memory. Going to find out amount of memory below 1M memory.
49	Amount of memory below 1M found and verified. Going to find out amount of memory above 1M memory.
4B	Amount of memory above 1M found and verified. Check for soft reset and going to clear memory below 1M for soft reset. (If power on, go to check point# 4Eh).
4C	Memory below 1M cleared, (SOFT RESET) Going to clear memory above 1M.
4D	Memory above 1M cleared, (SOFT RESET) Going to save the memory size. (Go to check point#52h).
4E	Memory test started, (NOT SOFT RESET) About to display the first 64k memory size.
4F	Memory size display started. This will be updated during memory test. Going for sequential and random memory test.
50	Memory testing/initialisation below 1 complete. Going to adjust displayed memory size for relocation/shadow.
51	Memory size display adjusted due to relocation/shadow. Memory test above 1M to follow.
52	Memory testing/initialisation above 1M complete. Going to save memory size information.
53	Memory size information is saved. CPU registers are saved. Going to enter in real mode.
54	Shutdown successful, CPU in real mode. Going to disable gate A20 line and disable parity/NMI.

57	A20 address line, parity/NMI disable successful. Going to adjust memory size depending on relocation/shadow.
58	Memory size adjusted for relocation/shadow. Going to clear Hit 6 message.
59	Hit 6 message cleared. Message displayed. About to start DMA and interrupt controller test.
60	DMA page register test passed. To do DMA#1 base register test.
62	DMA#1 base register test passed. To do DMA#2 base register test.
65	DMA#2 base register test passed. To program DMA unit 1 and 2.
66	DMA unit 1 and 2 programming over. To initialise 8259 interrupt controller.
67	8259 initialisation over.
7F	Extended NMI sources enabling is in progress.
80	Keyboard test started. Clearing output buffer, checking for stuck key, About to issue keyboard reset command.
81	Keyboard reset error/stuck key found. About to issue keyboard controller interface test command.
82	Keyboard controller interface test over. About to write command byte and init circular buffer.
83	Command byte written, Global data init done. About to check for lock-key.
84	Lock-key checking over. About to check for memory size mismatch with CMOS.
85	Memory size check done. About to display soft error and check for password or bypass setup
86	Password Checked. About to so programming before setup.
87	Programming before setup complete. Going to uncompress SETUP code and execute CMOS setup.
88	REturned from CMOS setup program and screen is cleared. About to do programming after setup
89	Programming after setup complete. Going to display power on screen message.
8B	First screen message displayed. Message displayed. About to do video BIOS shadow.
8C	Video BIOS shadow successful. Setup options programming after CMOS setup about to start.
8D	Setup options are programmed, mouse check and init to be done next.
8E	Mouse check and Initialisation complete. Going for hard disk controller reset.
8F	Hard disk controller reset done. Floppy setup to be done next.
91	Floppy setup complete. Hard disk setup to be done next.Z
94	Hard disk setup complete. To set base and extended memory size.
95	Memory size adjusted due to mouse support. Init of different BUSes optional ROMs from C800 to start.
96	Going to any init before C800 optional ROM control is over.
97	Any init before C800 optional ROM control is over. Optional ROM check and control will be done next.
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control.
99	Any initialisation required after optional ROM test is over. Going to setup timer data area and printer base address.
9A	Return after setting timer and printer base address. Going to set the RS-232 base address.
9B	Returned after RS-232 base address. Going to do any initialisation before Coprocessor test.
9C	Required initialisation before Coprocessor is over. Going to initialise the Coprocessor next.

9D	Coprocessor initialised. Going to do any initialisation after Coprocessor test.
9E	Initialisation after Coprocessor test is complete. Going to check extd keyboard, Keyboard ID and num-lock.
9F	Extd keyboard check is done, ID flag set, num-lock on/off. Keyboard ID command is to be issued.
A0	Keyboard ID command issued. Keyboard ID flag to be reset.
A1	Keyboard ID flag reset. Cache memory test to follow.
A2	Cache memory test over. Going to display any soft errors.
A3	Soft errors display complete. Going to set keyboard typematic rate.
A4	Keyboard typematic rate set. To program memory wait states.
A5	Memory wait states programming over. Going to clear the screen and enable parity/NMI.
A7	NMI and parity enabled. Going to do any initialisation required after E000 optional ROM control.
A8	Initialisation before E000 ROM control over. E000 ROM to get control next.
A9	Returned from E000 ROM control. Going to do any initialisation required after E000 optional ROM control.
AA	Initialisation after E000 optional ROM control is over. Going to display the system configuration.
B0	System configuration is displayed.
B1	Going to copy any code to specific area.
00	Copying of code to specific area done. Going to give control to INT-19 boot loader.

Beep Codes

Beeps	Description
1 Short	POST Passed
1 Long	Memory refresh failed
1 Long & 2 Short	VGA BIOS failed
1 Long & 3 Short	VGA Controller Failed Tests
3 Beeps	DRAM Base 64K Failed
4 Beeps	On-board timer failed
5 Beeps	CPU Error
6 Beeps	Gate A20 Failed, Can't switch to protected mode.
7 Beeps	CPU unexpected interrupt.
8 Beeps	Display Memory Error
9 Beeps	ROM Checksum Failed
10 Beeps	CMOS Shutdown Register Failed.

Appendix D. Bibliography

Processor

IntelDX4 Processor Data Book

Intel Corporation
2200 Mission College Boulevard
PO Box 58119
Santa Clara CA 95052-8119

MMD Rapid Ltd
3 Bennet Court
READING
Berks RG2 0QX

CHIPset

SIS 85C471 Green PC ISA-VESA Single Chip Reference Manual
SIS 85C407 Buffer Chip

Silicon Integrated Systems Corp
240 North Wolfe Road
Sunnyvale CA 94086

Silicon Concepts Ltd
PEC Lynchborough Road
Passfield
LIPHOOK
Hants GU30 7SB

Combo Device

FDC37C653 Super I/O Device Data Sheet
FDC37C665 Super I/O Device Data Sheet

Standard Microsystems Corp
80 Arkay Drive
ParkHauppauge NY 11788

Kudos Thame Ltd
55 Suttons
London Road
READING
Berks RG6 1AZ

VGA Controller

Cirrus Logic CL-GD6245 Data Sheet
Cirrus Logic CL-GD624X Application Book

Cirrus Logic Inc
3100 West Warren Ave
Fremont CA 94538

Sequoia Technology Ltd
Tekelec House
Back Lane
Spencers Wood
READING
Berks RG7 1PD

Flash Memory Devices

28F008A Data Sheet

Intel Corporation
Mission College Boulevard
58119
95052-8119

MMD Rapid Ltd 2200
3 Bennet CourtPO Box
READINGSanta Clara CA
Berks RG2 0QX

STEbus Specification

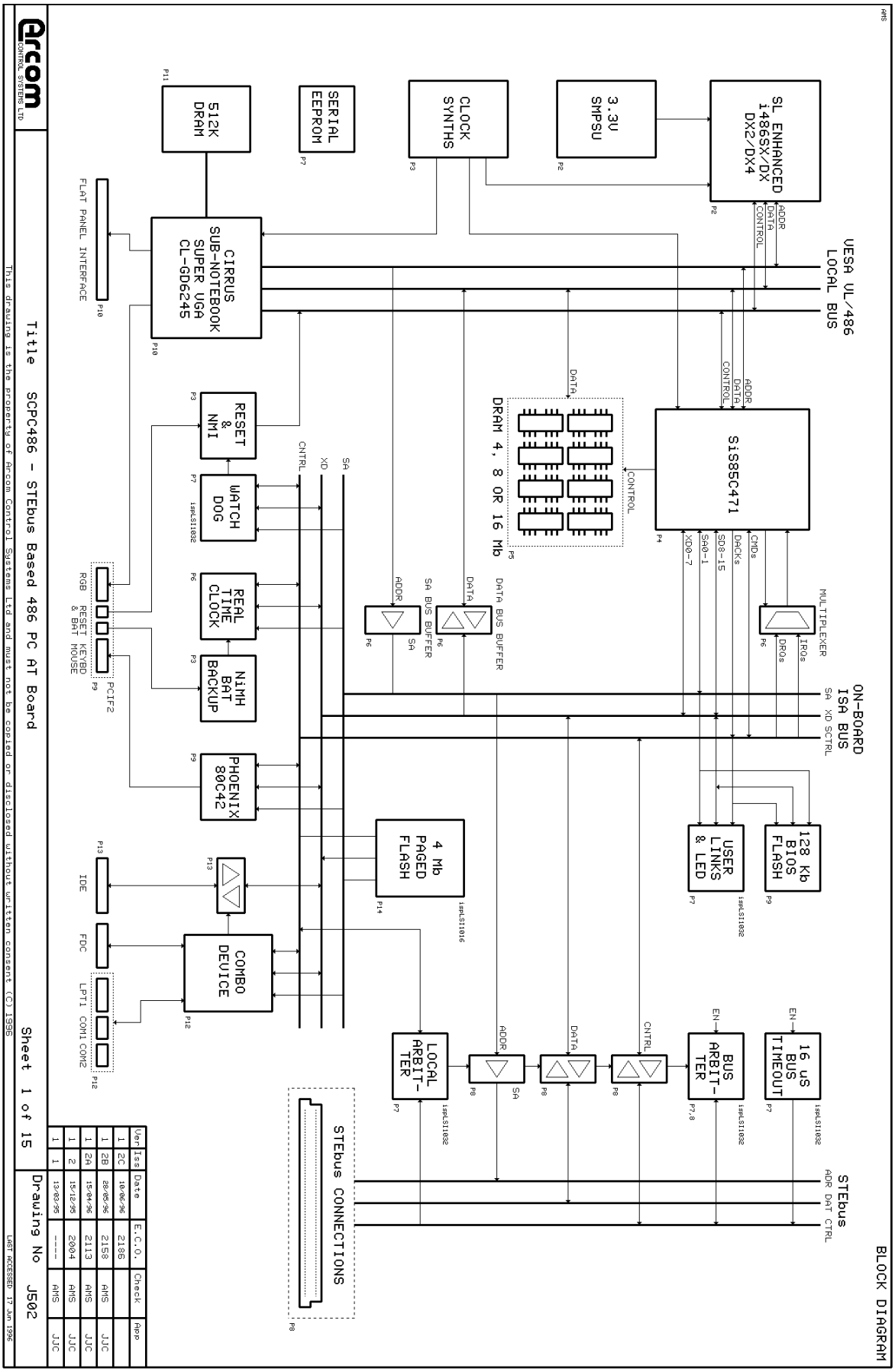
IEEE 1000-1987 STEbus Specification
The Institute of Electrical and Electronic Engineers Inc
345 East 47th Street New York NY 10017
ISBN 1-55937-002-5

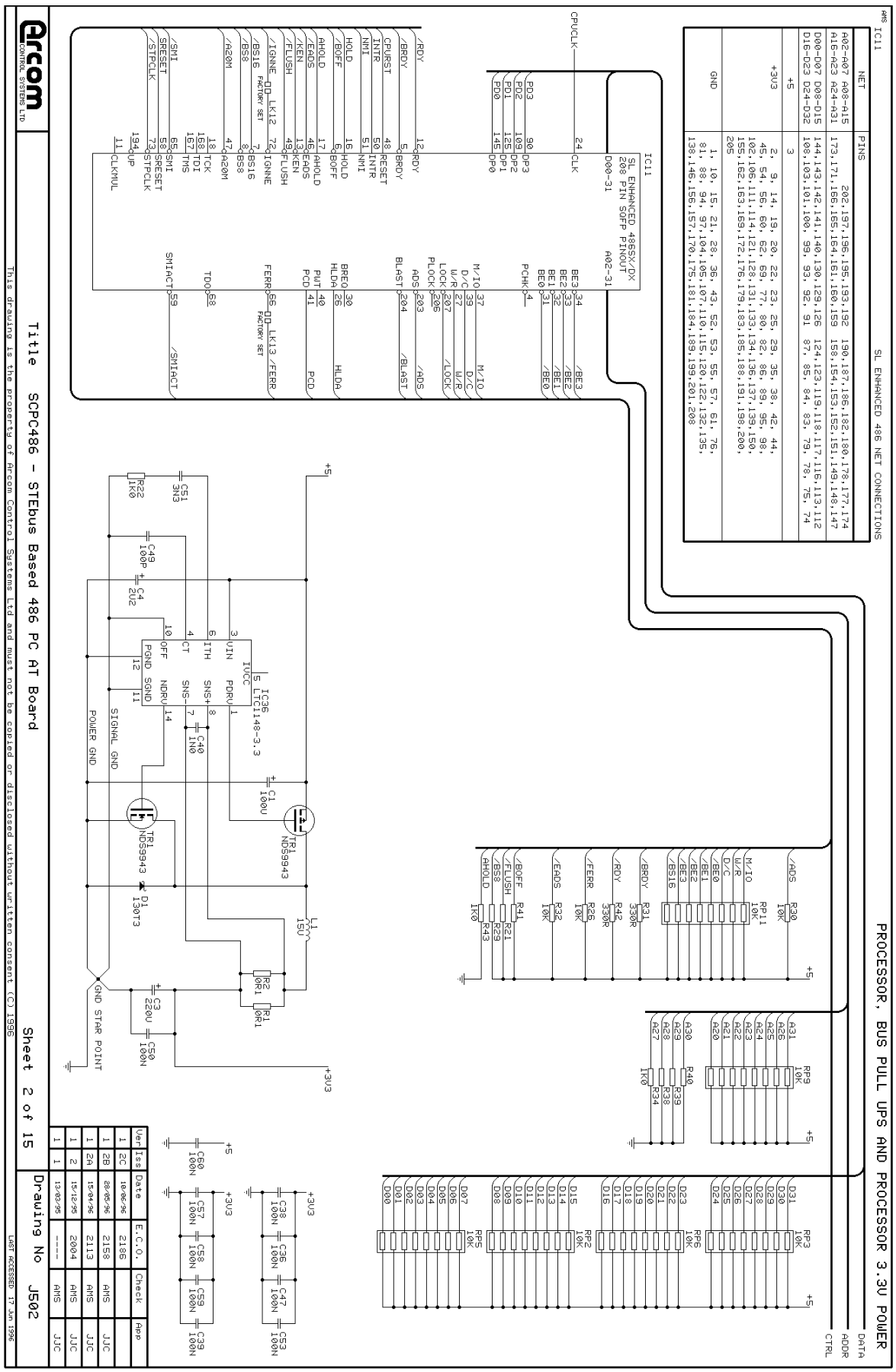
Appendix E. Product Issue Changes

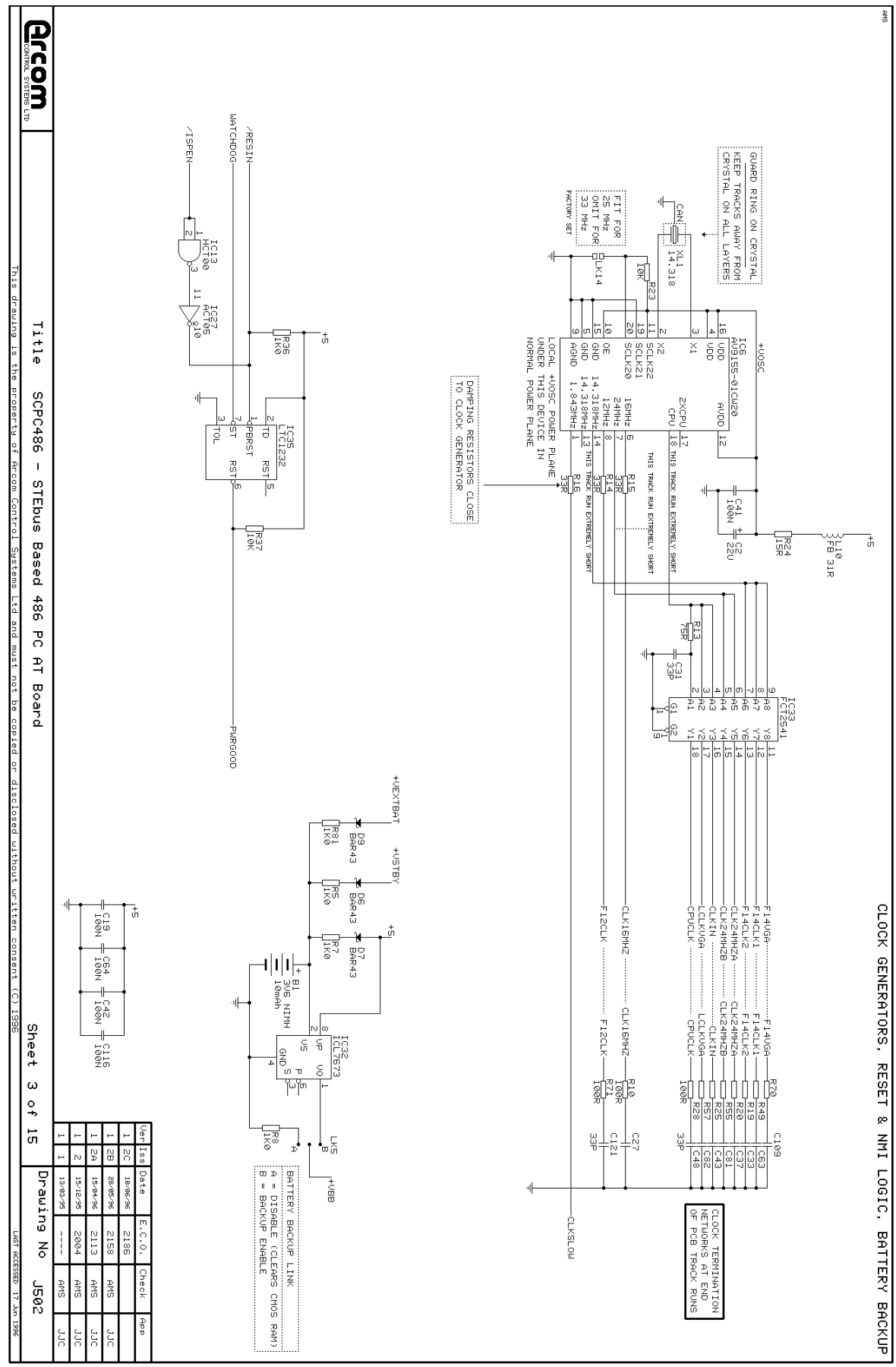
PCB Version/Issue	Comment
V1 Iss 1	Engineering Prototype - Not distributed customers
V1 Iss 2	Beta Production Release Product

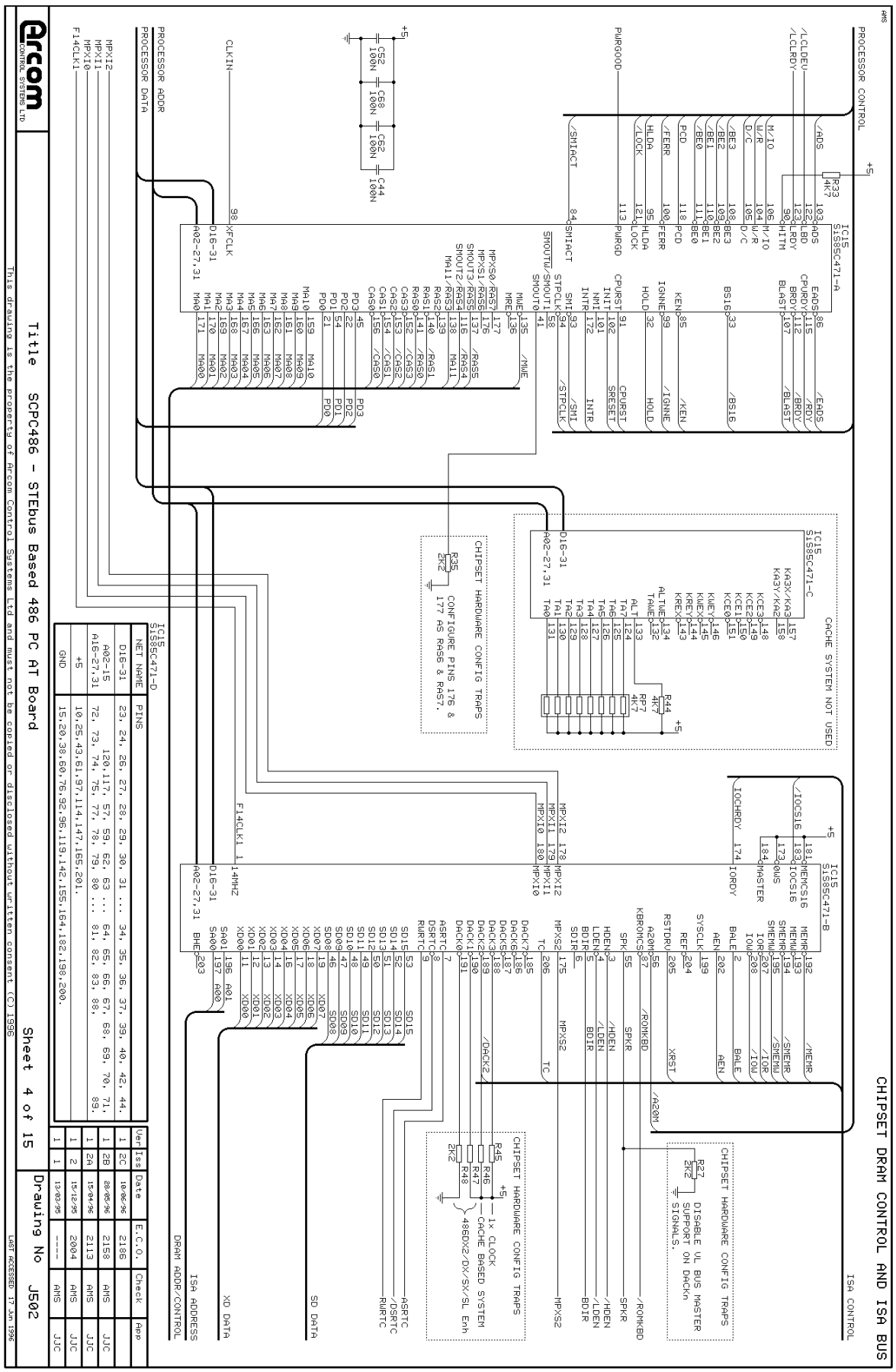
BIOS	Comment
V1.0	Beta Production Release Product
V1.1	Video BIOS Update; Add AFFS BIOS Extension

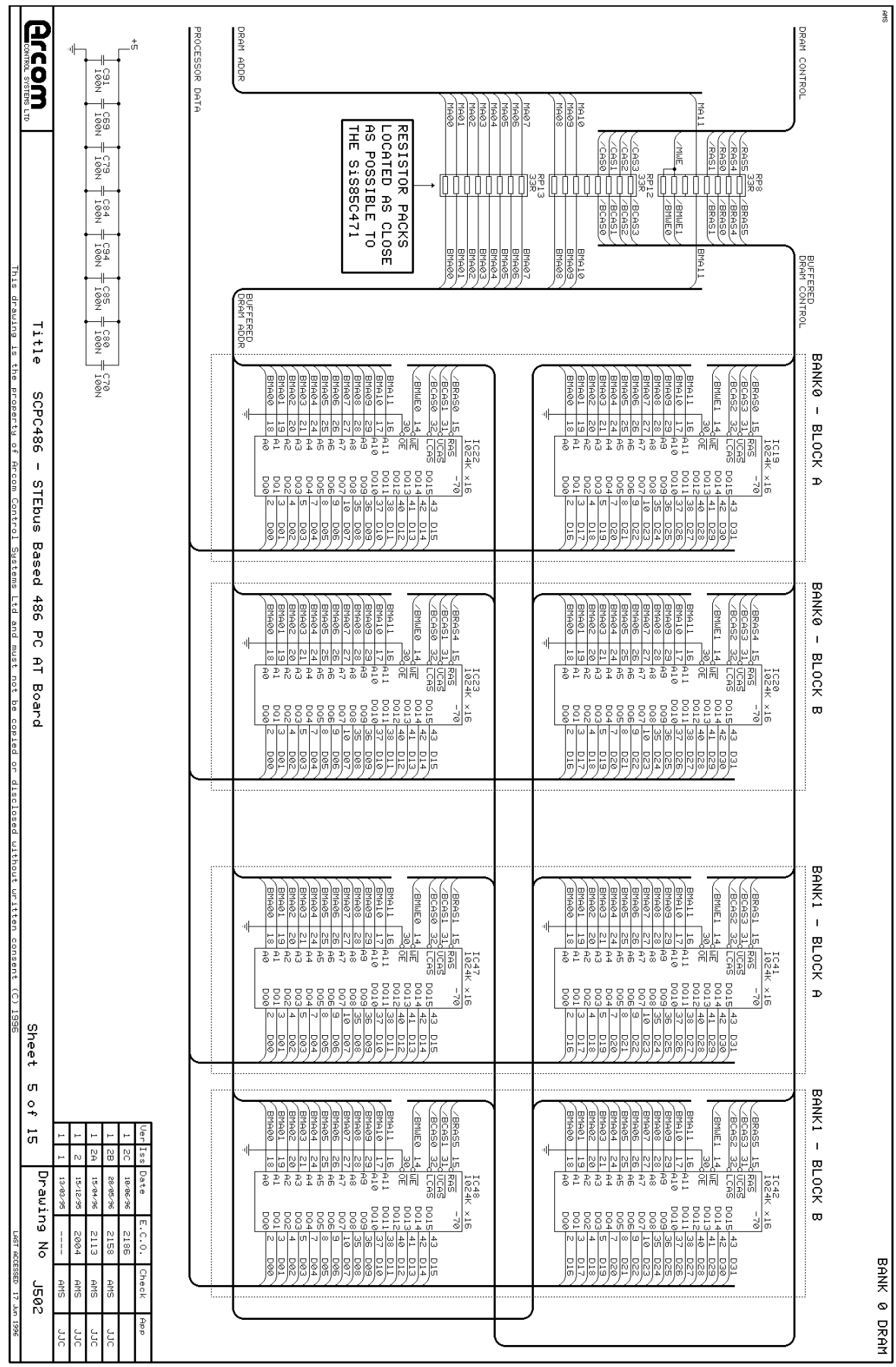
Appendix F. Circuit Diagrams

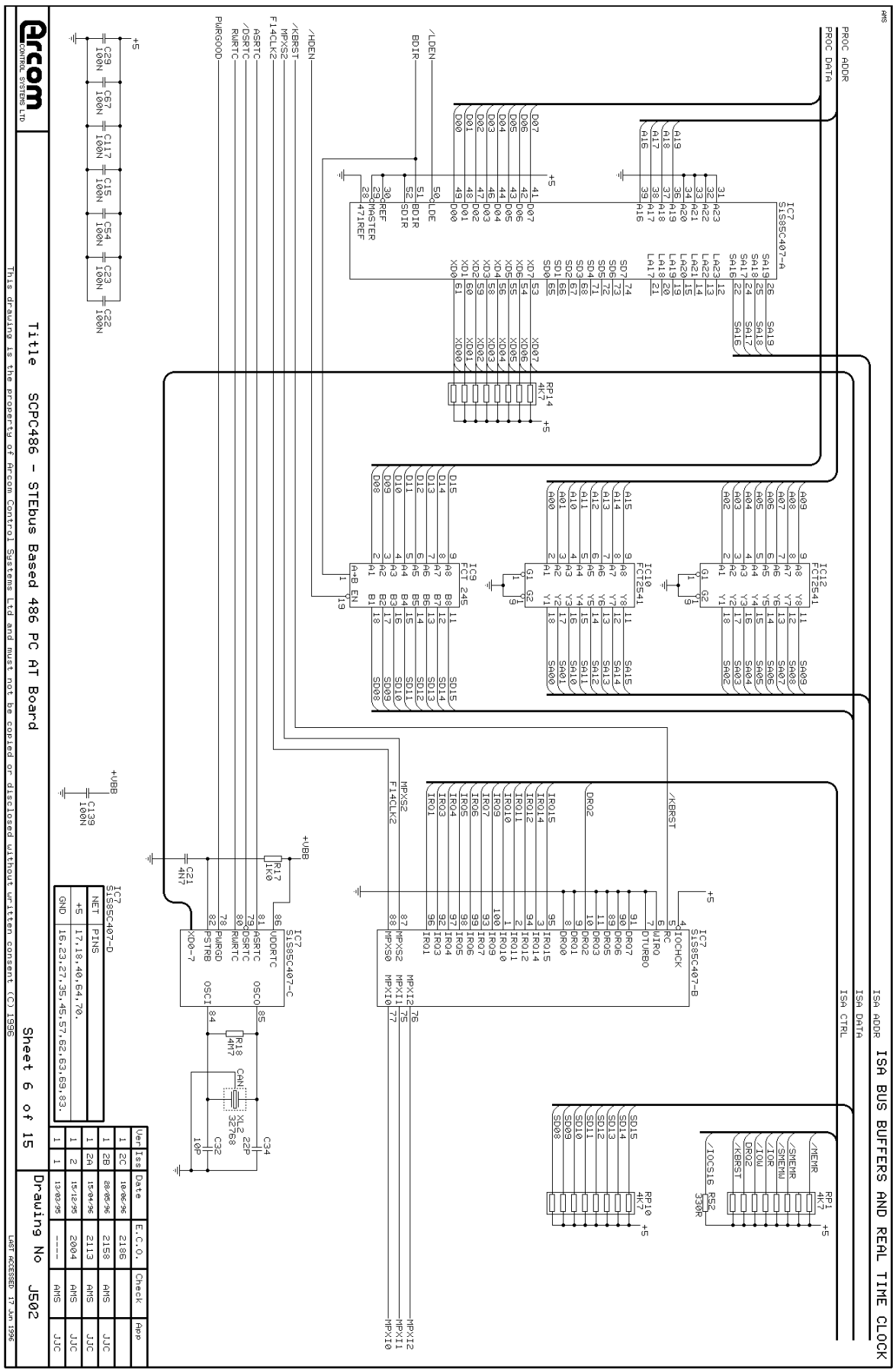


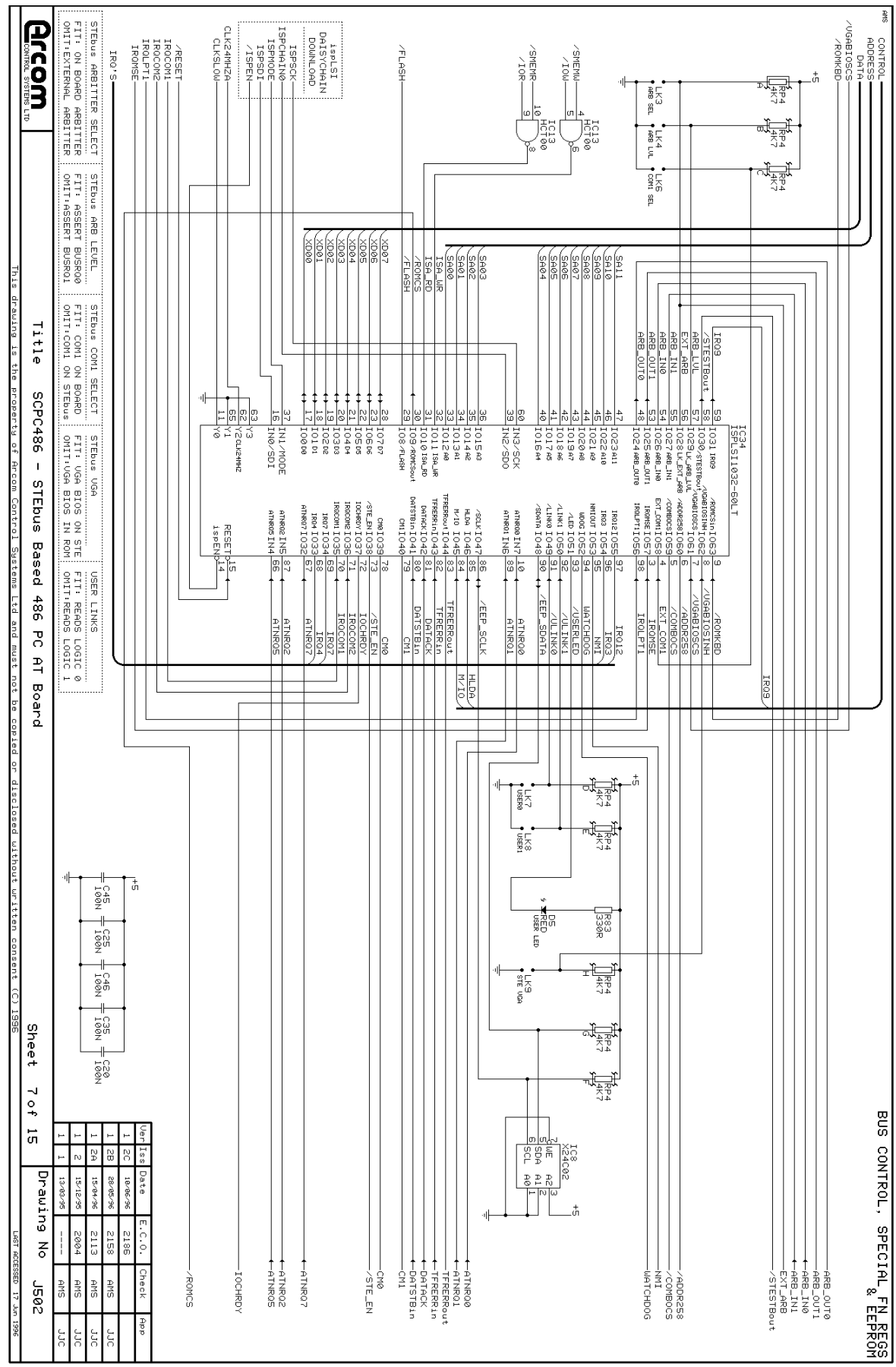

PROCESSOR, BUS PULL UPS AND PROCESSOR 3.3V POWER
SL ENHANCED 486 NET CONNECTIONS
IC11
SL ENHANCED 486SX/DX
208 PIN SQFP PINOUT
Title SCPC486 - STEbus Based 486 PC AT Board
Sheet 2 of 15
Drawing No J502
This drawing is the property of Arcom Control Systems Ltd and must not be copied or disclosed without written consent (C) 1996
LAST ACCESSED 17 Jun 1996

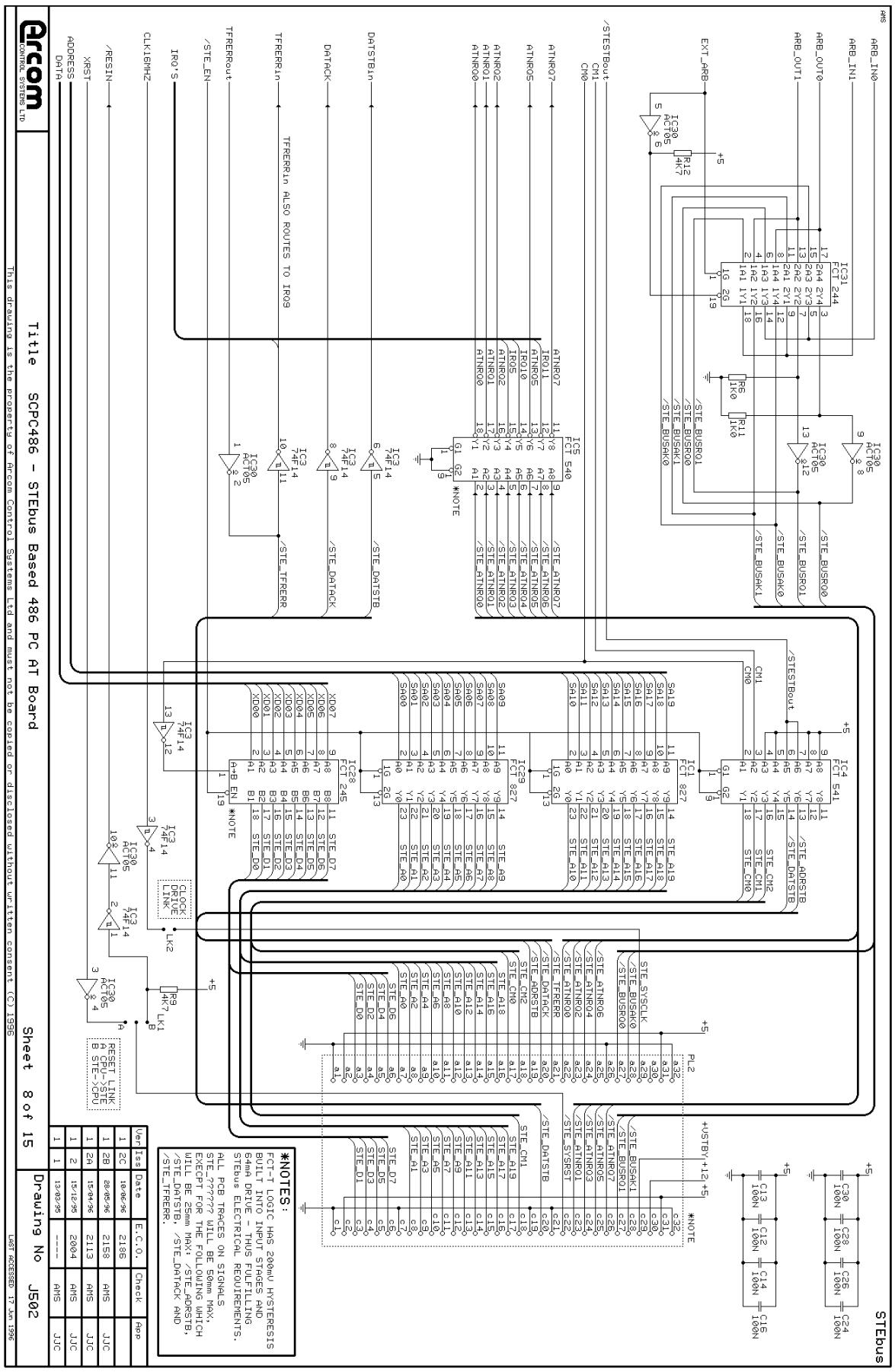

CLOCK GENERATORS, RESET & NMI LOGIC, BATTERY BACKUP
Arcom CONTROL SYSTEMS Ltd
Title SCPC486 - STEbus Based 486 PC AT Board
Sheet 3 of 15
Drawing No J502
This drawing is the property of Arcom Control Systems Ltd and must not be copied or disclosed without written consent (C) 1996
LAST ACCESSED 17 Jun 1996
Ver Iss Date E.C.O. Check App
1 2C 18/06/96 2186 JJC
1 2B 28/05/96 2158 AMS JJC
1 2A 15/04/96 2113 AMS JJC
1 2 15/12/95 2004 AMS JJC
1 1 13/03/95 ---- AMS JJC
GUARD RING ON CRYSTAL
KEEP TRACKS AWAY FROM CRYSTAL ON ALL LAYERS
FIT FOR 25 MHz OMIT FOR 33 MHz
FACTORY SET
LOCAL +VOSC POWER PLANE UNDER THIS DEVICE IN NORMAL POWER PLANE
DAMPING RESISTORS CLOSE TO CLOCK GENERATOR
THIS TRACK RUN EXTREMELY SHORT
CLOCK TERMINATION NETWORKS AT END OF PCB TRACK RUNS
BATTERY BACKUP LINK
A = DISABLE (CLEARS CMOS RAM)
B = BACKUP ENABLE
+VOSC
+VEXTBAT
+VSTBY
+VBB
+5
/RESIN
WATCHDOG
/ISPEN
PURGOOD
CLKSLOW
CLK16MHZ
F12CLK
F14VGA
F14CLK1
F14CLK2
CLK24MHZA
CLK24MHZB
CLKIN
LCLKVGA
CPUCLK
IC33 FCT2541
IC8 ADSISS-01CUM20
IC32 ICL7673
IC35 LTC1232
IC13 HCT00
IC27 AC05
XL1 14.318
LK14
LK5
BT1 3V6 NIMH 100mAh
C41 100N
C2 22U
C31 33P
C121 33P
C27 33P
C109 33P
C19 100N
C84 100N
C42 100N
C116 100N
L10 FB 31R
R24 15R
R13 75R
R16 33R
R15 33R
R14 33R
R23 10K
R36 1K0
R37 10K
R81 1K0
R5 1K0
R7 1K0
R8 1K0
R20 100R
R49 100R
R19 100R
R33 100R
R25 100R
R57 100R
R28 100R
R10 100R
R71 100R
D9 BAR43
D6 BAR43
D7 BAR43

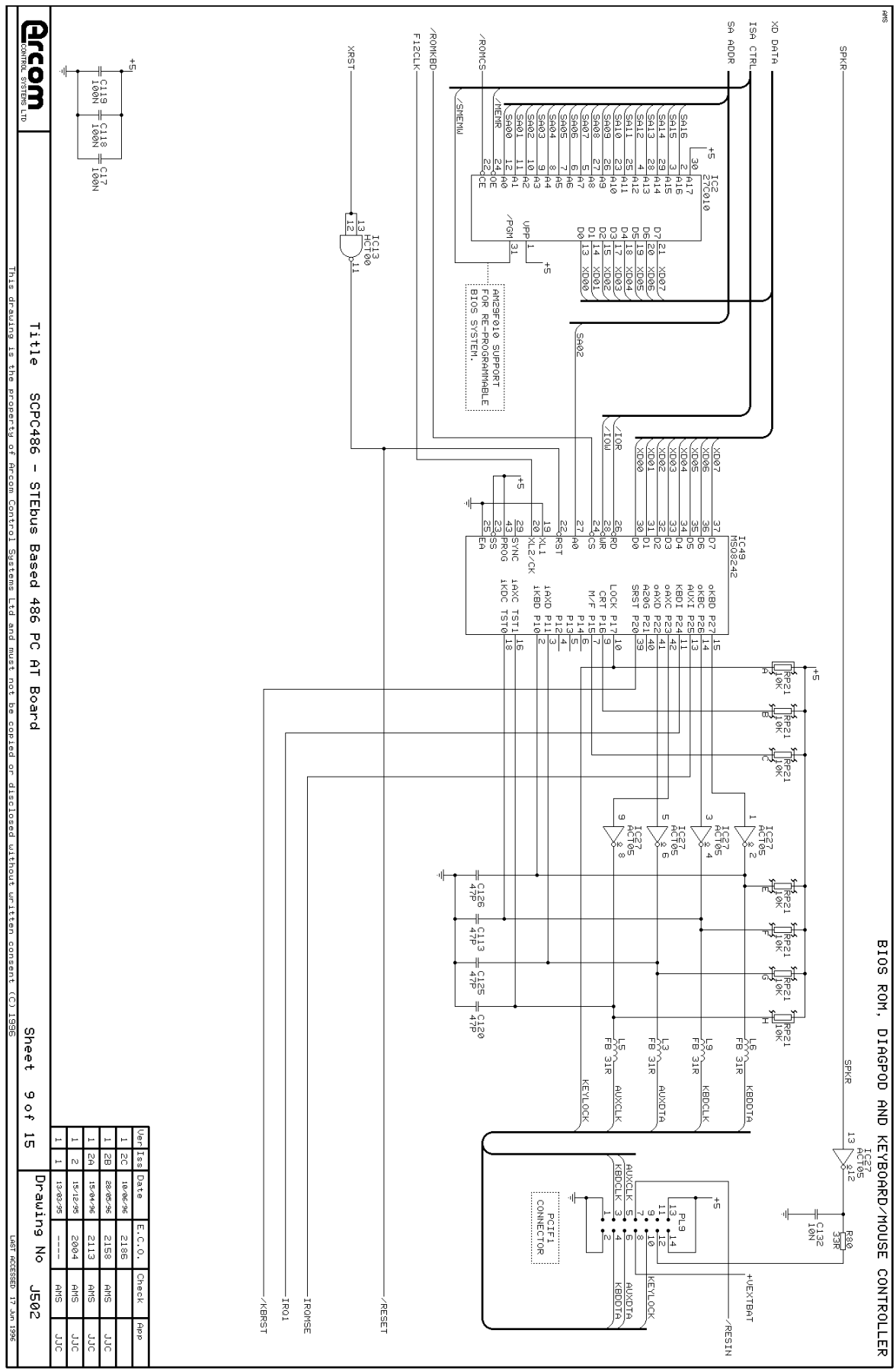

CHIPSET DRAM CONTROL AND ISA BUS
PROCESSOR CONTROL
PROCESSOR DATA
PROCESSOR ADDR
CLKIN
MPXI2
MPXI1
MPXI0
F14CLK1
ISA CONTROL
CACHE SYSTEM NOT USED
CHIPSET HARDWARE CONFIG TRAPS
CONFIGURE PINS 176 & 177 AS RAS6 & RAS7.
DISABLE VL BUS MASTER SUPPORT ON DACKn SIGNALS.
1x CLOCK — CACHE BASED SYSTEM 486DX2/DX/SX/SL Enh
ISA ADDRESS
DRAM ADDR/CONTROL
XD DATA
SD DATA
Title SCPC486 - STEbus Based 486 PC AT Board
Sheet 4 of 15
Drawing No J502
This drawing is the property of Arcom Control Systems Ltd and must not be copied or disclosed without written consent (C) 1996
LAST ACCESSED 17 Jun 1996

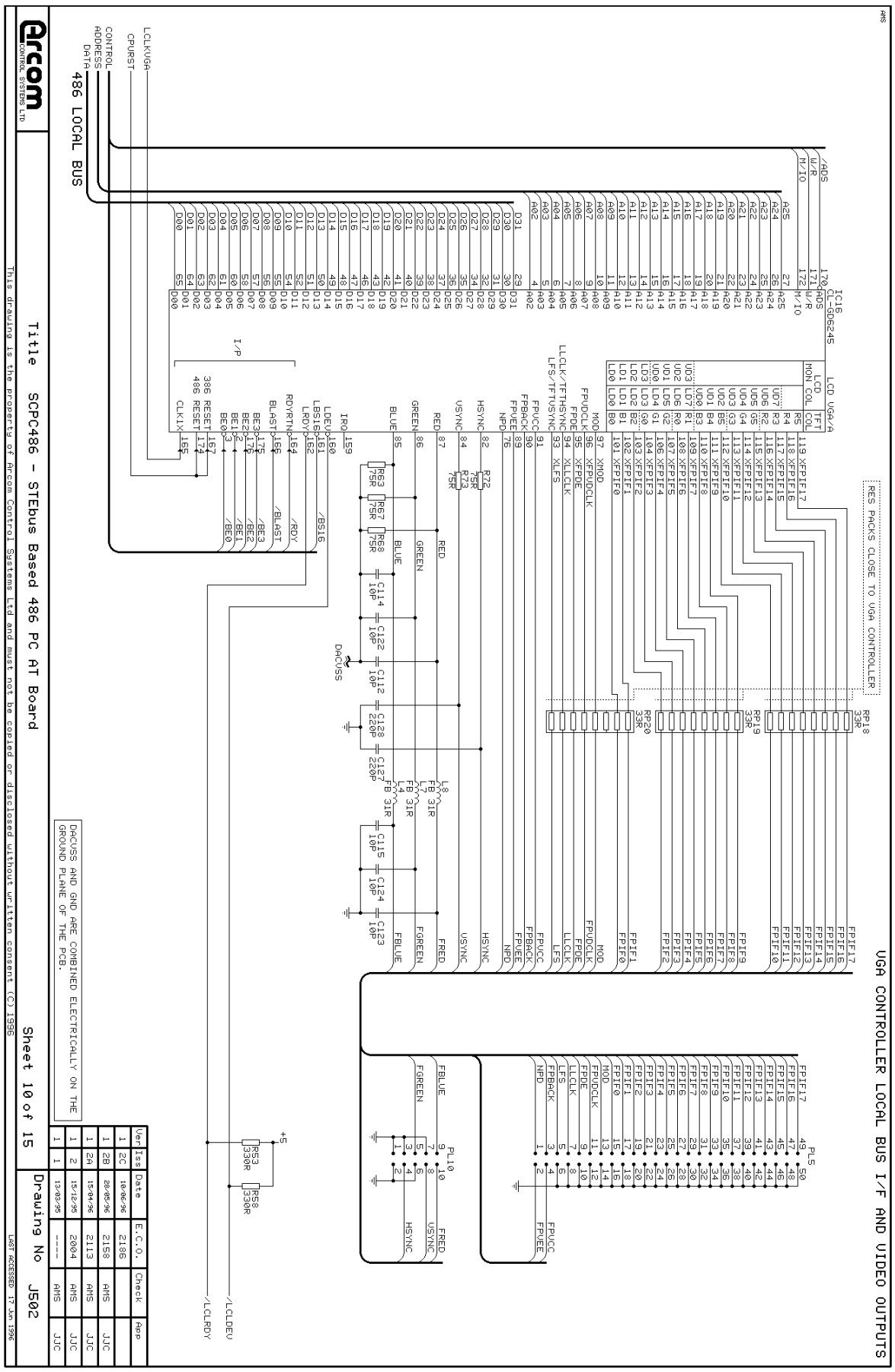

BANK 0 DRAM
BANK0 - BLOCK A
BANK0 - BLOCK B
BANK1 - BLOCK A
BANK1 - BLOCK B
DRAM CONTROL
BUFFERED DRAM CONTROL
DRAM ADDR
BUFFERED DRAM ADDR
PROCESSOR DATA
RESISTOR PACKS LOCATED AS CLOSE AS POSSIBLE TO THE SiS85C471
Title SCPC486 - STEbus Based 486 PC AT Board
Sheet 5 of 15
Drawing No J502
This drawing is the property of Arcom Control Systems Ltd and must not be copied or disclosed without written consent (C) 1996
LAST ACCESSED 17 Jun 1996

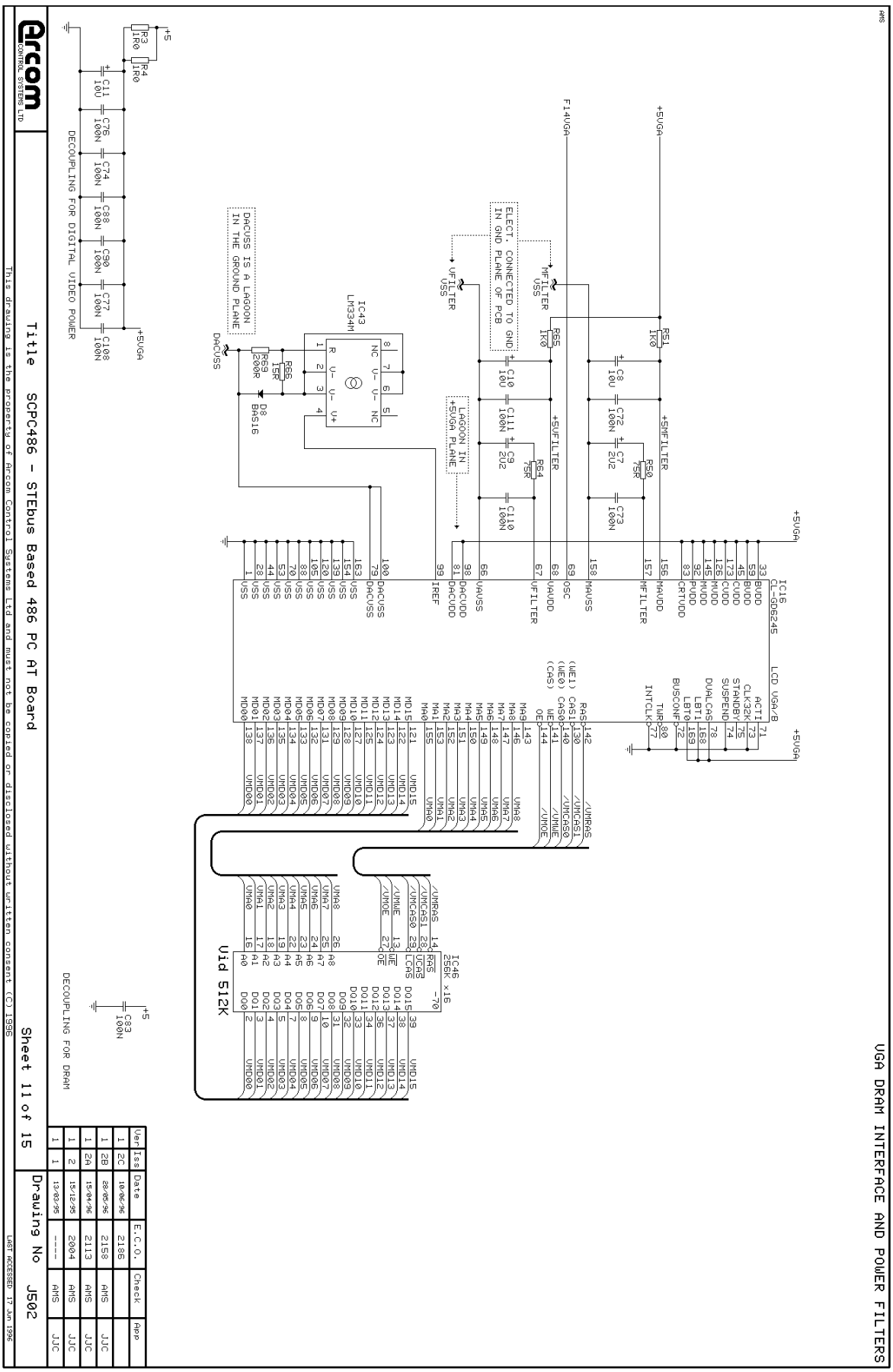

ISA BUS BUFFERS AND REAL TIME CLOCK
Title SCPC486 - STEbus Based 486 PC AT Board
Sheet 6 of 15
Drawing No J502
Arcom CONTROL SYSTEMS LTD
This drawing is the property of Arcom Control Systems Ltd and must not be copied or disclosed without written consent (C) 1996
LAST ACCESSED 17 Jun 1996
IC7 SIS95C407-A
IC7 SIS95C407-B
IC7 SIS95C407-C
IC7 SIS95C407-D
IC9 FCT 245
IC10 FCT2541
IC12 FCT2541
RP14 4K7
RP1 4K7
RP10 4K7
R52 330R
R17 1K0
R18 4M7
C21 4N7
C139 100N
C29 100N
C57 100N
C117 100N
C15 100N
C54 100N
C23 100N
C22 100N
C32 10P
C34 22P
XL2 32768
PROC ADDR
PROC DATA
ISA ADDR
ISA DATA
ISA CTRL
/LDEN
BDIR
/HDEN
/KBRST
MPXS2
F14CLK2
ASRTC
/DSRTC
RWRTC
PWRGOOD
+UBB
+5
Ver Iss Date E.C.O. Check App
1 2C 10/06/96 2186 JJC
1 2B 28/05/96 2158 AMS JJC
1 2A 15/04/96 2113 AMS JJC
1 2 15/12/95 2004 AMS JJC
1 1 13/03/95 ---- AMS JJC

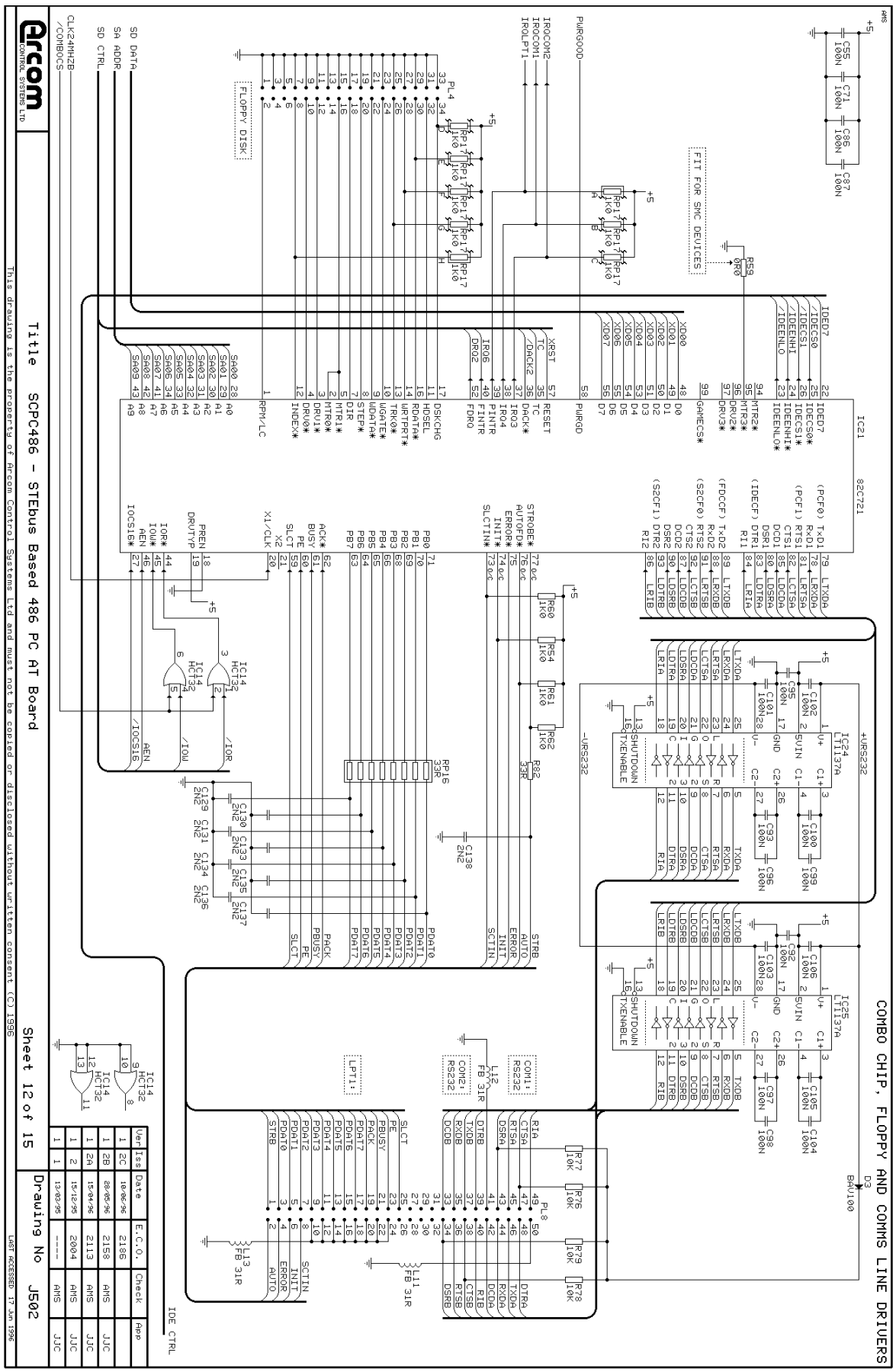

BUS CONTROL, SPECIAL FN REGS & EEPROM
Title SCPC486 - STEbus Based 486 PC AT Board
Drawing No J502
Sheet 7 of 15
Arcom CONTROL SYSTEMS Ltd
This drawing is the property of Arcom Control Systems Ltd and must not be copied or disclosed without written consent (C) 1996
LAST ACCESSED 17 Jun 1996
STEbus ARBITER SELECT
FIT: ON BOARD ARBITER
OMIT:EXTERNAL ARBITER
STEbus ARB LEVEL
FIT: ASSERT BUSR00
OMIT:ASSERT BUSR01
STEbus COM1 SELECT
FIT: COM1 ON BOARD
OMIT:COM1 ON STEbus
STEbus VGA
FIT: VGA BIOS ON STE
OMIT:VGA BIOS IN ROM
USER LINKS
FIT: READS LOGIC 0
OMIT:READS LOGIC 1
Ver Iss Date E.C.O. Check App
1 2C 18/06/96 2186 JJC
1 2B 28/05/96 2158 AMS JJC
1 2A 15/04/96 2113 AMS JJC
1 2 15/12/95 2004 AMS JJC
1 1 13/03/95 ---- AMS JJC
CONTROL
ADDRESS
DATA
/VGABIOSCS
/ROMKBD
/SMEMW
/IOW
/SMEMR
/IOR
IRQ'S
/RESET
IROCM1
IROCM2
IRQLPT1
IROMSE
ISPSCK
ISPCHAIN0
ISPMODE
ISPSDI
/ISPEN
CLK24MHZA
CLKSLOW
/FLASH
ispLSI DAISYCHAIN DOWNLOAD
/ROMCS
/ARB_OUT0
/ARB_OUT1
/ARB_IN0
/ARB_IN1
EXT_ARB
/STESTBout
/COMBOCS
NMI
WATCHDOG
/ADDR258
/ROMCS
/IOCHRDY
/STE_EN
CM0
DATSTBin
DATACK
TFRERRin
TFRERRout
ATNRQ0
ATNRQ1
ATNRQ2
ATNRQ5
ATNRQ7
IC34 ISPLSI1032-60LT
IC13 HCT00
IC8 X24C02
LK3 ARB SEL
LK4 ARB LVL
LK5 COMX SEL
LK7 USER0
LK8 USER1
LK9 STE VGA
RP4 4K7
R83 330R
D5 RED USER LED
C45 100N
C25 100N
C46 100N
C35 100N
C20 100N
+5

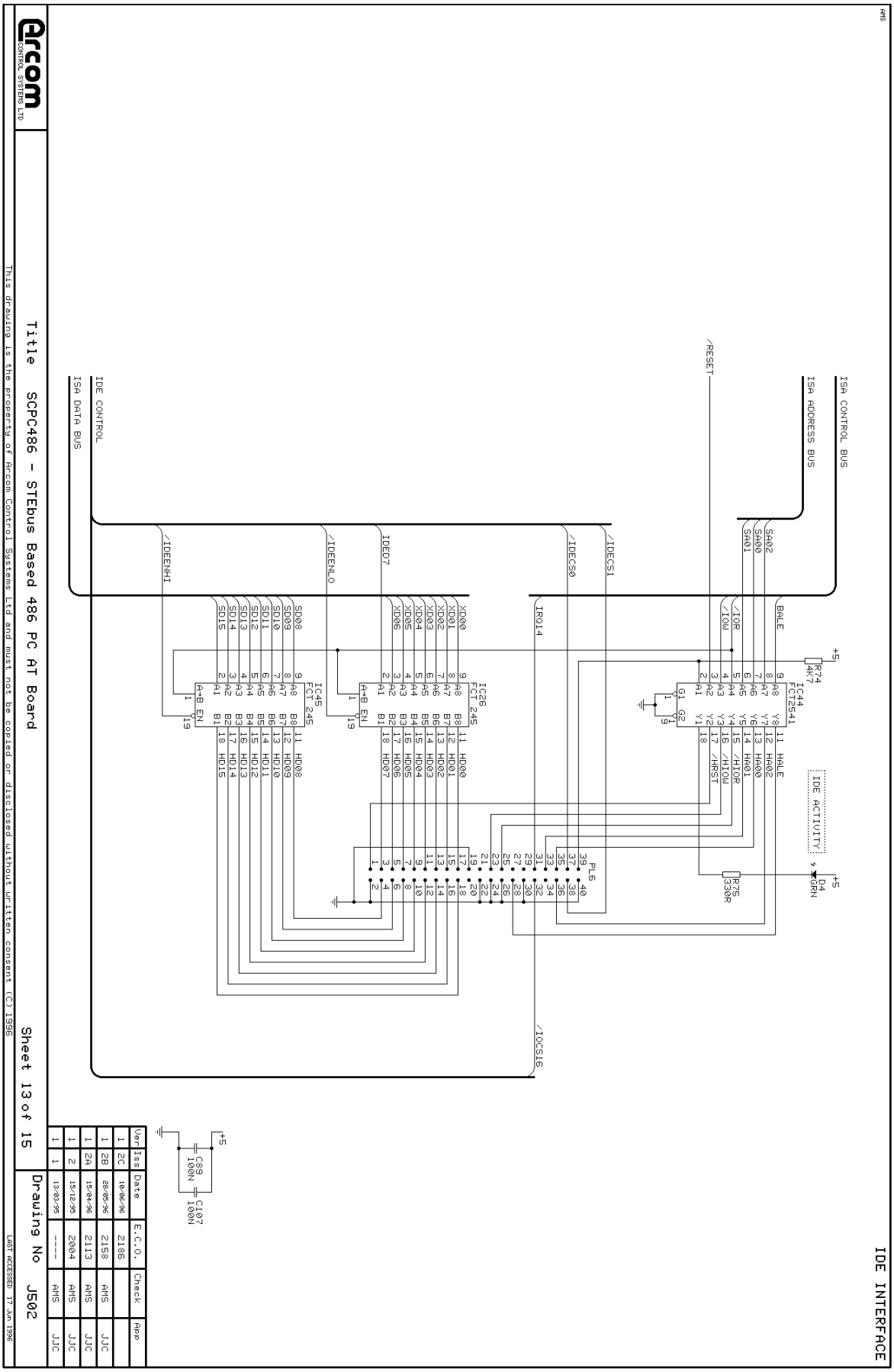

Arcom CONTROL SYSTEMS LTD
Title SCPC486 - STEbus Based 486 PC AT Board
Sheet 8 of 15
Drawing No J502
This drawing is the property of Arcom Control Systems Ltd and must not be copied or disclosed without written consent (C) 1996
LAST ACCESSED 17 Jun 1996
*NOTES:
FCT-T LOGIC HAS 200mV HYSTERESIS BUILT INTO INPUT STAGES AND 64mA DRIVE - THUS FULFILLING STEbus ELECTRICAL REQUIREMENTS.
ALL PCB TRACES ON SIGNALS STE_?????? WILL BE 50mm MAX, EXCEPT FOR THE FOLLOWING WHICH WILL BE 25mm MAX: /STE_ADRSTB, /STE_DATSTB, /STE_DATACK AND /STE_TFRERR.
ARB_IN0
ARB_IN1
ARB_OUT0
ARB_OUT1
EXT_ARB
/STESTBout
CM1
CM0
ATNR07
ATNR02
ATNR01
ATNR00
ATNR05
/RESIN
XRST
ADDRESS DATA
IRQ'S
CLK16MHZ
/STE_EN
TFRERRout
TFRERRin
TFRERRin ALSO ROUTES TO IRQ9
DATSTBin
DATACK
/STE_BUSRQ0
/STE_BUSRQ1
/STE_BUSAK0
/STE_BUSAK1
/STE_BUSRQ01
/STE_BUSRQ00
/STE_BUSHAK1
/STE_BUSHAK0
/STE_ATNR07
/STE_ATNR06
/STE_ATNR05
/STE_ATNR04
/STE_ATNR03
/STE_ATNR02
/STE_ATNR01
/STE_ATNR00
/STE_ADRSTB
/STE_DATACK
/STE_DATSTB
/STE_TFRERR
/STE_SYSRST
STE_SYSCLK
STE_CM0
STE_CM1
STE_CM2
STEbus
+5
+VSTBY
+12
-12
*NOTE
RESET LINK
A CPU->STE
B STE->CPU
Ver Iss Date E.C.O. Check App
1 2C 10-06-96 2186 AMS JJC
1 2B 28-05-96 2158 AMS JJC
1 2A 15-04-96 2113 AMS JJC
1 2 15-12-95 2004 AMS JJC
1 1 13-03-95 ---- AMS JJC

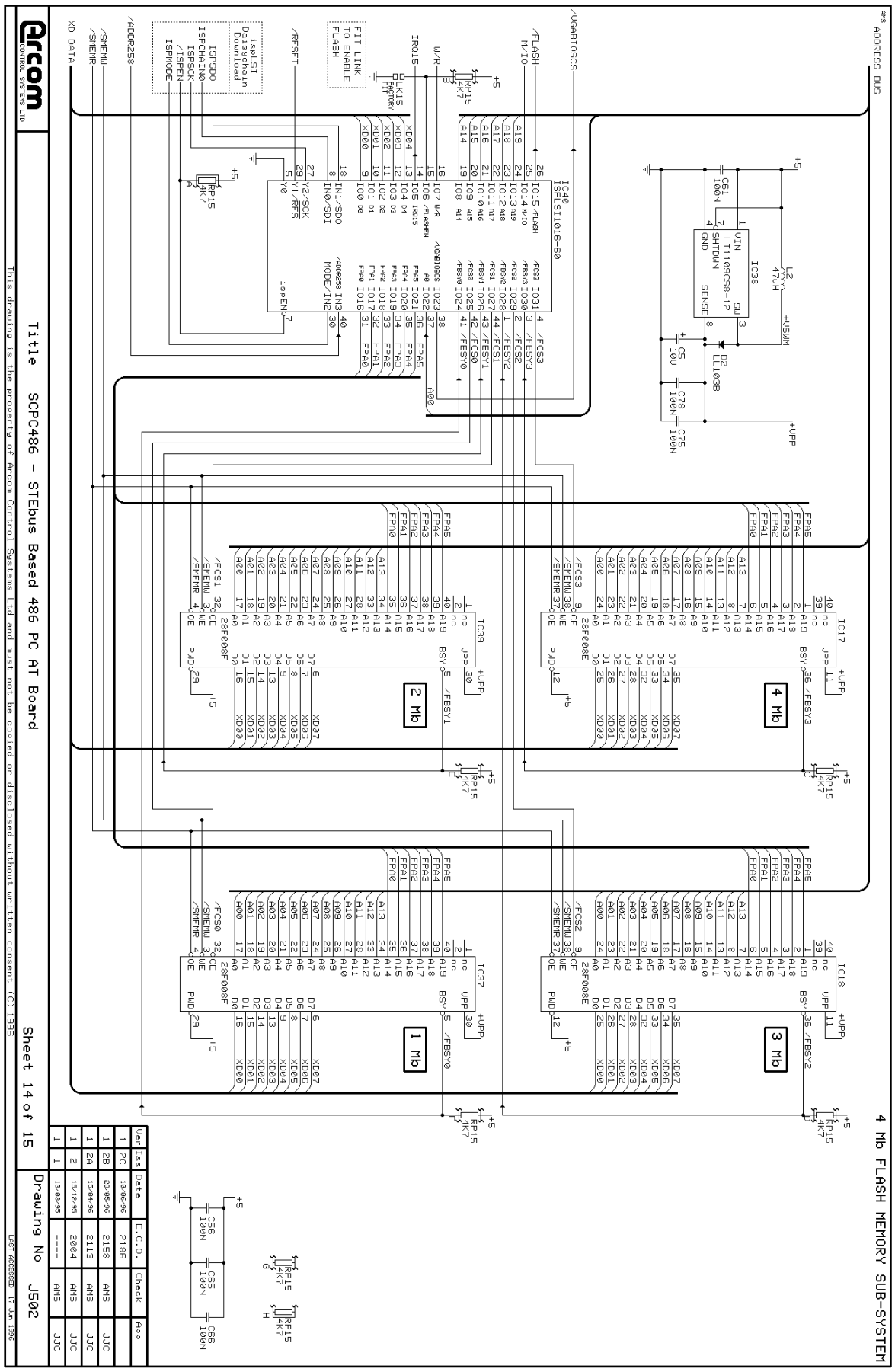

BIOS ROM, DIAGPOD AND KEYBOARD/MOUSE CONTROLLER
Arcom CONTROL SYSTEMS Ltd
Title SCPC486 - STEbus Based 486 PC AT Board
Sheet 9 of 15
Drawing No J502
This drawing is the property of Arcom Control Systems Ltd and must not be copied or disclosed without written consent (C) 1996
LAST ACCESSED 17 Jun 1996
Ver Iss Date E.C.O. Check App
1 2C 10/06/96 2186 JJC
1 2B 28/05/96 2158 AMS JJC
1 2A 15/04/96 2113 AMS JJC
1 2 15/12/95 2004 AMS JJC
1 1 13/03/95 ---- AMS JJC
AM29F010 SUPPORT FOR RE-PROGRAMMABLE BIOS SYSTEM.
PC/PI CONNECTOR
SPKR
XD DATA
ISA CTRL
SA ADDR
/ROMCS
/ROMKBD
F12CLK
XRST
/RESET
IRQ1
/KBRST
IRQMSE
+VEXTBAT
/RESIN
KEYLOCK
AUXCLK
AUXDTA
KBDCLK
KBDDTA


VGA CONTROLLER LOCAL BUS I/F AND VIDEO OUTPUTS
RES PACKS CLOSE TO VGA CONTROLLER
LCLKVGA
CPURST
CONTROL
ADDRESS
DATA
486 LOCAL BUS
IC15 CL-GD6245
LCD VGA/A
LCD TFT
MON COL
TFT COL
RP18 33R
RP19 33R
RP20 33R
FPIF17
FPIF16
FPIF15
FPIF14
FPIF13
FPIF12
FPIF11
FPIF10
FPIF9
FPIF8
FPIF7
FPIF6
FPIF5
FPIF4
FPIF3
FPIF2
FPIF1
FPIF0
PL5
PL10
I/P
CLK1X
386 RESET
486 RESET
R63 75R
R67 75R
R68 75R
R72 75R
R73 75R
R74 75R
C114 10P
C122 10P
C112 10P
C128 220P
C127 220P
C115 10P
C124 10P
C123 10P
L8 FB 31R
L7 FB 31R
L6 FB 31R
L4 FB 31R
DACVSS
RS3 330R
RS8 330R
+5
/LCLDEV
/LCLRDY
DACVSS AND GND ARE COMBINED ELECTRICALLY ON THE GROUND PLANE OF THE PCB.
Title SCPC486 - STEbus Based 486 PC AT Board
Sheet 10 of 15
Drawing No J502
Arcom CONTROL SYSTEMS LTD
This drawing is the property of Arcom Control Systems Ltd and must not be copied or disclosed without written consent (C) 1996
Last accessed 17 Jun 1996
Ver Iss Date E.C.O. Check App
1 2C 10-06-96 2186 JJC
1 2B 28-05-96 2158 AMS JJC
1 2A 15-04-96 2113 AMS JJC
1 2 15-12-95 2004 AMS JJC
1 1 13-03-95 ---- AMS JJC

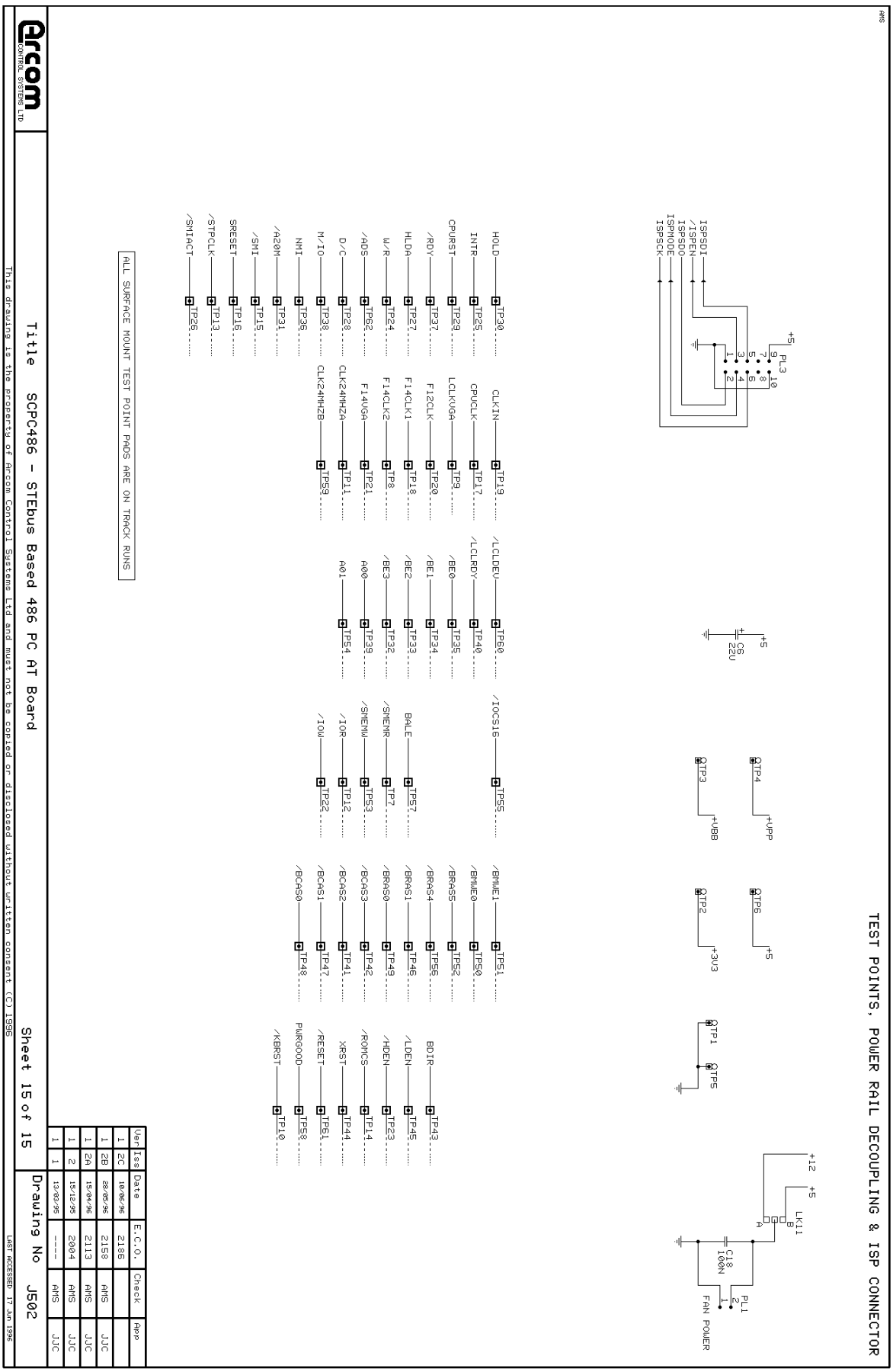

UGA DRAM INTERFACE AND POWER FILTERS
Title SCPC486 - STEbus Based 486 PC AT Board
Sheet 11 of 15
Drawing No J502
Arcom CONTROL SYSTEMS Ltd
This drawing is the property of Arcom Control Systems Ltd and must not be copied or disclosed without written consent (C) 1996
LAST ACCESSED 17 Jun 1996
DECOUPLING FOR DIGITAL VIDEO POWER
DECOUPLING FOR DRAM
DACVSS IS A LAGOON IN THE GROUND PLANE
ELECT. CONNECTED TO GND IN GND PLANE OF PCB
LAGOON IN +5VGA PLANE
IC16 CL-GD6245
LCD UGA/B
IC43 LM334M
IC46 256K x16 -70
Vid 512K
Ver Iss Date E.C.O. Check App
1 2C 18/06/96 2186 JJC
1 2B 28/05/96 2158 AMS JJC
1 2A 15/04/96 2113 AMS JJC
1 2 15/12/95 2004 AMS JJC
1 1 13/03/95 ---- AMS JJC


COMBO CHIP, FLOPPY AND COMMS LINE DRIVERS
Title SCPC486 - STEbus Based 486 PC AT Board
Sheet 12 of 15
Drawing No J502
This drawing is the property of Arcom Control Systems Ltd and must not be copied or disclosed without written consent (C) 1996
LAST ACCESSED 17 Jun 1996
FLOPPY DISK
FIT FOR SMC DEVICES
IDE CTRL
LPT1:
COM1: RS232
COM2: RS232
IC21 82C721
IC24 LTI137A
IC25 LTI137A
IC14 HCT32
SD DATA
SA ADDR
SD CTRL
/COMBOCS
CLK24MHZB


IDE INTERFACE
Arcom CONTROL SYSTEMS Ltd
Title SCPC486 - STEbus Based 486 PC AT Board
Sheet 13 of 15
Drawing No J502
This drawing is the property of Arcom Control Systems Ltd and must not be copied or disclosed without written consent (C) 1996
LAST ACCESSED 17 Jun 1996
ISA CONTROL BUS
ISA ADDRESS BUS
ISA DATA BUS
IDE CONTROL
/RESET
IDE ACTIVITY
IC44 FCT2541
IC26 FCT 245
IC45 FCT 245
R74 4K7
R75 330R
D4 GRN
C89 100N
C107 100N
PL6
/IOCS16
Ver Iss Date E.C.O. Check App
1 2C 18/06/96 2186 JJC
1 2B 28/05/96 2158 AMS JJC
1 2A 15/04/96 2113 AMS JJC
1 2 15/12/95 2004 AMS JJC
1 1 13/03/95 ---- AMS JJC



Ver	Iss	Date	E.C.O.	Check	App
1	2C	10-06-96	2136		
1	2B	28/05/96	2158	AMS	JJC
1	2A	15-04-96	2113	AMS	JJC
1	2	15/12/95	2004	AMS	JJC
1	1	13/03/95	----	AMS	JJC


TEST POINTS, POWER RAIL DECOUPLING & ISP CONNECTOR
Arcom CONTROL SYSTEMS Ltd
Title SCPC486 - STEbus Based 486 PC AT Board
Sheet 15 of 15
Drawing No J502
ALL SURFACE MOUNT TEST POINT PADS ARE ON TRACK RUNS
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LAST ACCESSED 17 Jun 1996
HOLD TP30 CLKIN TP19 /LCLDEV TP60 /IOCS16 TP55 /BMWE1 TP51
INTR TP25 CPUCLK TP17 /LCLRDY TP40 /BMWE0 TP50
CPURST TP29 LCLKVGA TP9 /BE0 TP35 /BRAS5 TP52
/RDY TP37 F12CLK TP20 /BE1 TP34 /BRAS4 TP56 BDIR TP43
HLDA TP27 F14CLK1 TP18 /BE2 TP33 BALE TP57 /BRAS1 TP46 /LDEN TP45
W/R TP24 F14CLK2 TP8 /BE3 TP32 /SMEMR TP7 /BRAS0 TP49 /HDEN TP23
/ADS TP62 F14VGA TP21 A00 TP39 /SMEMW TP53 /BCAS3 TP42 /ROMCS TP14
D/C TP28 CLK24MHZA TP11 A01 TP54 /IOR TP12 /BCAS2 TP41 XRST TP44
M/IO TP38 CLK24MHZB TP59 /IOW TP22 /BCAS1 TP47 /RESET TP61
NMI TP36 /BCAS0 TP48 PWRGOOD TP58
/A20M TP31 /KBRST TP10
/SMI TP15
SRESET TP16
/STPCLK TP13
/SMIACT TP26
ISPSDI
/ISPEN
ISPSDO
ISPMODE
ISPSCK
PL3
C6 22U
TP4 +VPP
TP3 +VBB
TP6 +5
TP2 +3V3
TP1
TP5
+12
LK11
C18 100N
PL1 FAN POWER
Ver Iss Date E.C.O. Check App
1 2C 18/06/96 2186 JJC
1 2B 28/05/96 2158 AMS JJC
1 2A 15/04/96 2113 AMS JJC
1 2 15/12/95 2004 AMS JJC
1 1 13/03/95 ---- AMS JJC