DIDACTIC DC/DC BUCK CONVERTER

with discrete PID controller

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Indice

1 | Introduction

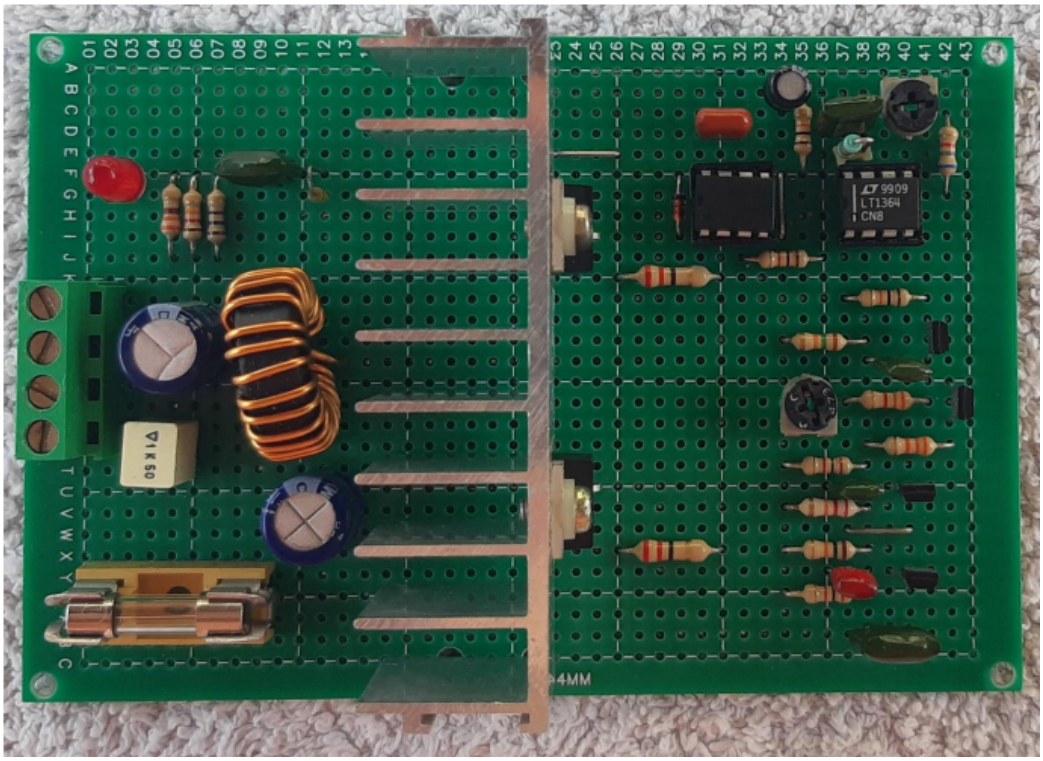

Figura 1.1 Final implementation of the Buck converter

This project aims to implement a didactic DC/DC step down converter from an input voltage of 12V to an output of 5V. Instead of using a single integrated circuit specifically designed for power converters, the circuit achieves the control function through ordinary op-amps to better understand how to practically implement a PID controller. The following initial parameters are evaluated:

- Output filter capacitor C2: 1000μF

- Output filter inductor L1: 280μH
- Modulation frequency: 40 kHz
- Carrier amplitude N_R: 5.0V

And the associated figures of merit at steady state:

- Conversion factor M: 0.417
- Bandwidth -3 dB: 2 kHz
- Phase margin: 70°

2 | Poles and Zeros location

The poles and zeros location can be easily carried out evaluating the small signal parameters of the buck circuit. Otherwise, the straightforward way is to check [1].

$$f_{resonance} = \frac{1}{2\pi}\frac{1}{\sqrt{LC}} = 300Hz \tag{2.1}$$

To guarantee some safety margin, the phase margin of the system is computed as 80° instead of 70° with a crossing frequency f_c of 2 kHz:

$$f_{zeroPD} = f_c\sqrt{\frac{1-sen(80°)}{(1+sen(80°))}} = 175Hz \tag{2.2}$$

$$f_{polePD} = f_c\sqrt{\frac{1+sen(80°)}{(1-sen(80°))}} = 22.9kHz \tag{2.3}$$

$$f_{zeroPI} = \frac{f_c}{10} = 200Hz \tag{2.4}$$

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$$K\frac{\sqrt{1+\left(\frac{f_c}{f_{zeroPD}}\right)^2}}{\sqrt{1+\left(\frac{f_c}{f_{polePD}}\right)^2}}\frac{V_{out}}{M}\frac{1}{N_R}\left(\frac{f_{resonance}}{f_c}\right)^2 = 1 \rightarrow K = 1.62V/V \tag{2.5}$$

3 | Schematic

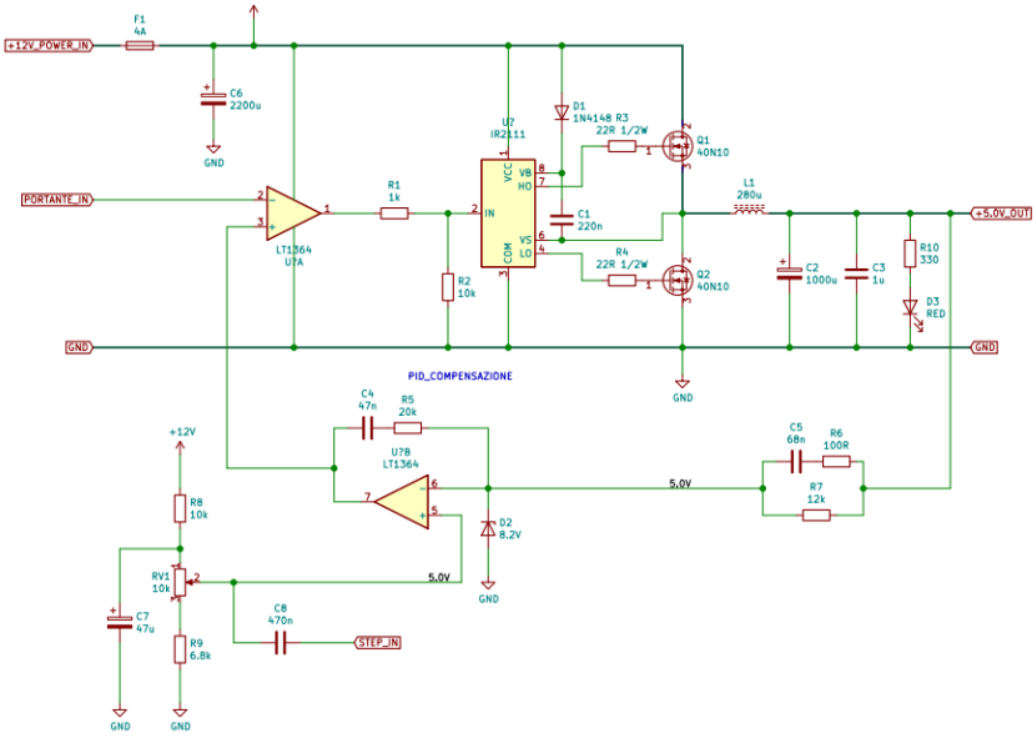

Figura 3.1 Schematic of the power section on the Buck converter

A degree of freedom is present and the values of the components are carried out starting from R7=12 kΩ as a reasonable value.

$$K = \frac{R_5}{R_7} \rightarrow R_5 = 19.44k\Omega \approx 20k\Omega \tag{3.1}$$

$$f_{zeroPD} = \frac{1}{2\pi C_4 R_5} \rightarrow C_4 = 46.8nF \approx 47nF \tag{3.2}$$

$$f_{zeroPI} = \frac{1}{2\pi C_5 \left(R_6 + R_7\right)} \rightarrow C_5 = 66.3nF \approx 68nF \left(if R_6 << R_7\right) \quad (3.3)$$

$$f_{polePD} = \frac{1}{2\pi C_5 R_6} \rightarrow R_6 = 102.3\Omega \approx 100\Omega \quad (3.4)$$

For a detailed discussion refer to [1]. An additional capacitor C7 is introduced on the schematic to guarantee a *soft start* when the buck is turned on.

4 | Carrier

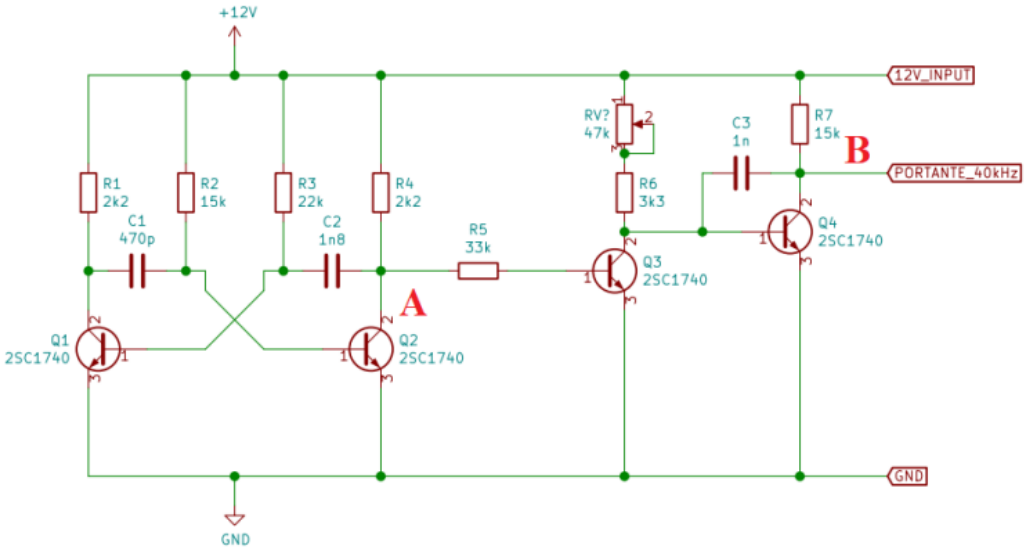

Figura 4.1 Final implementation of the Buck converter

The carrier is generated starting from an asymmetrical astabel mutlivibrator that feeds a pseudo-integrator implemented through a common emitter amplifier. The obtained square wave that is possible to observe at point A may be approximatelly described as:

- t_{ON}: 8.2μs

- t_{OFF}: 16.7μs

leading to an operatinig frequency of 40 KHz that is adequated to control the IR2111 gate driver. Frequencies above 100 KHz imply an overheating of the component.

The mosfets used in this circuit are IRLB4132, with a R_{DSON} of just 3.5 mΩ. The gate driver automatically introduces the required delay of dead

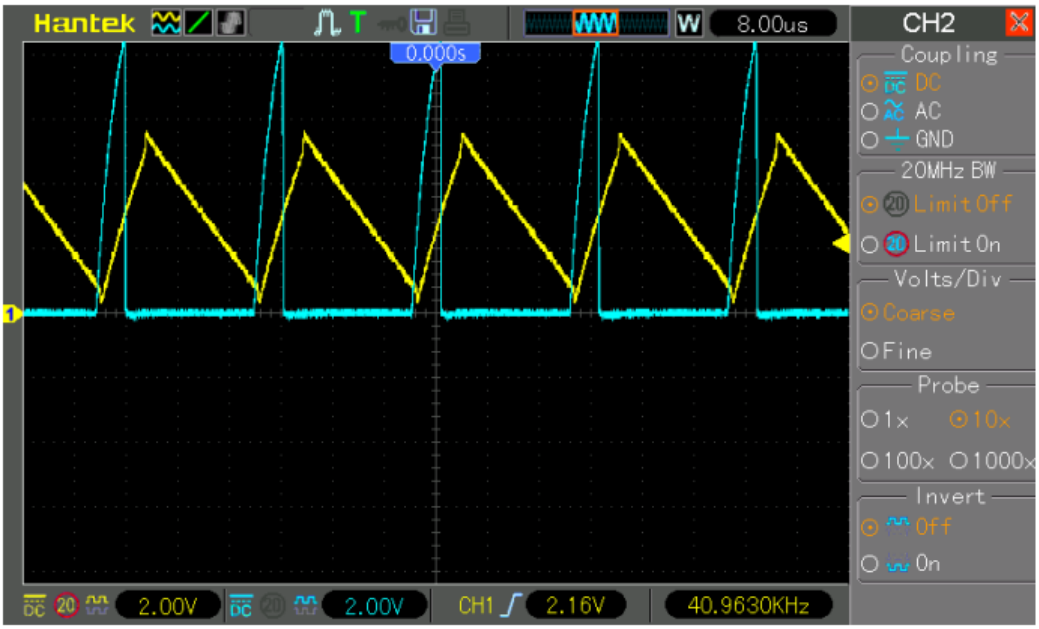

Figura 4.2 Waveforms at points A (blue) and B (yellow)

time and by looking at Fig. 4.3 and Fig. 5.2, it is possible to observe that the duty cycle is 0.416 as expected.

On the right side of Q2 it is defined the integrator circuit: during the ON time, Q3 is in saturation region with 0 V at its collector and Q4 off. Consequently, C3 is charged with an exponential growth that may be approximated as a linear growth since the ON time is very short, as reported in Fig. 4.2. During the OFF time, Q3 is off and the voltage at the collector of Q4 is the sum of the voltage between the terminals of C3 and V_{BE}.

Q4 is in the active region and the base current may be neglected. The current that flows into R6 is due to the capacitor C3 that is discharging.

During the OFF time the output waveform may be approximated as:

$$\frac{V_{CC} - V_{BE}}{R6 + RV} = C\frac{dV(t)}{dt} \tag{4.1}$$

$$V(t) = V(t_{ON}) - \frac{V_{CC} - V_{BE}}{R6 + RV} \times \frac{1}{C}\int_{t_{ON}}^{t_{ON}+t_{OFF}} dt = (5.0{+}0.65) - \frac{12 - 0.65}{3k3 + RV} \times \frac{1}{1n} \times T_{OFF}$$

Then, RV must be adjusted to 33kΩ to obtain: V(t_{ON}+t_{OFF})=0V.

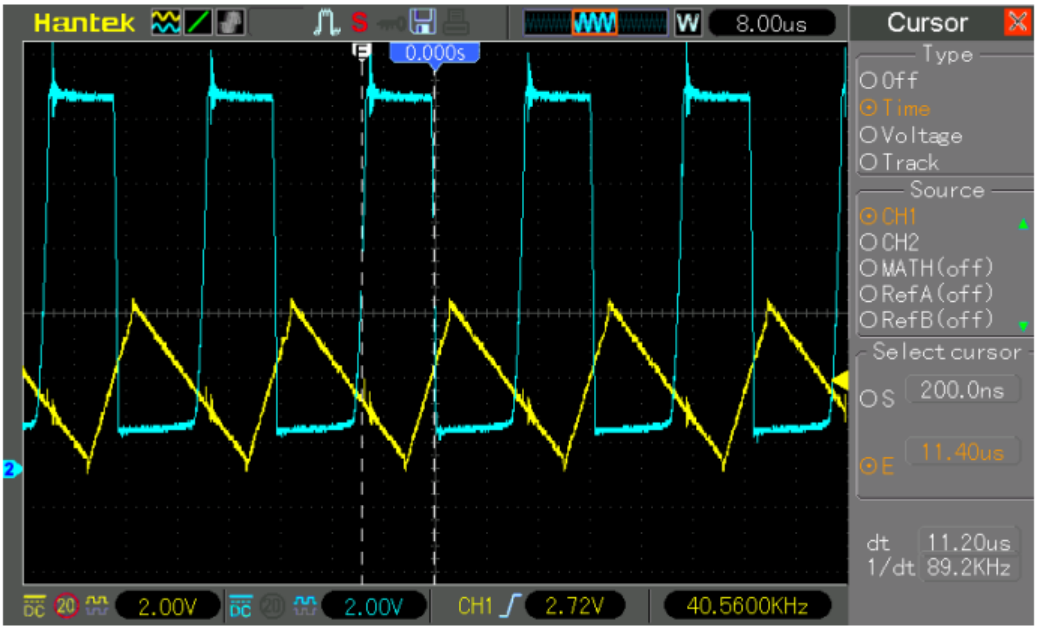

Figura 4.3 Carrier (yellow) and Output of the comparator (blue)

5 | Final results

The closed loop circuit behaves exactly as expected, as reported in the following figures.

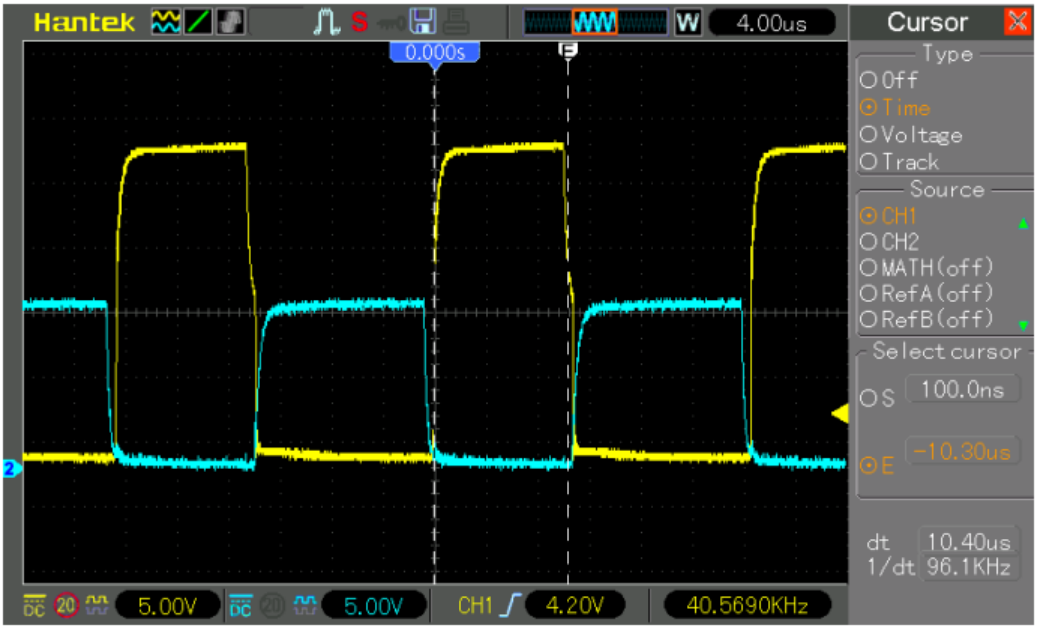

Figura 5.1 Voltage at the gate of Q1 (yellow) and Q2 (blue) at closed loop

It was possible to successfully test the performances of the converter with an output current of few Amperes. However, this circuit was just developed for didactic purposes only and it is not suggested to be used as a PSU because of its simplicity.

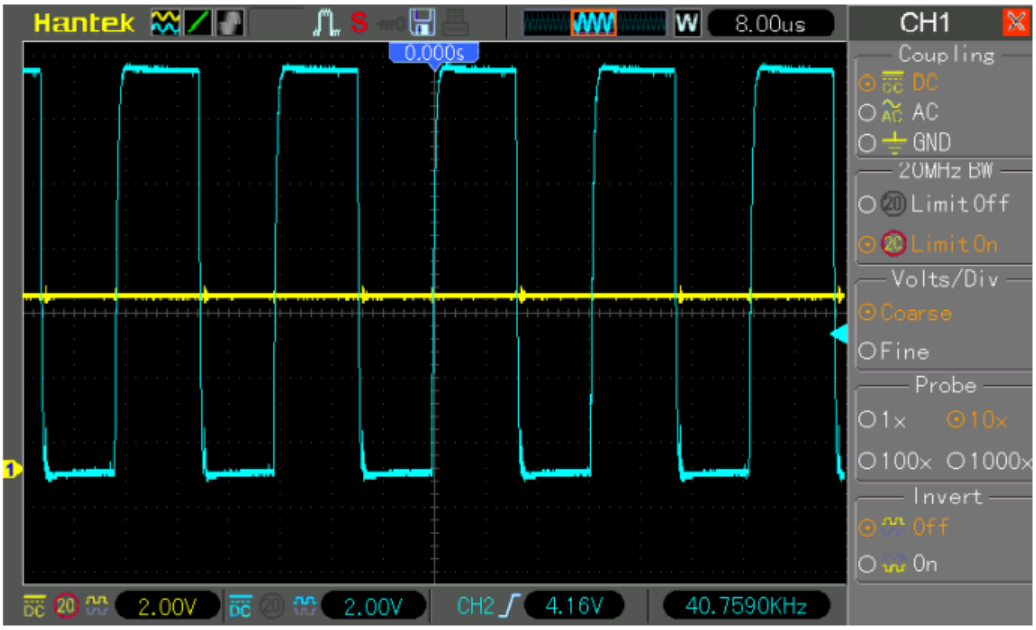

Figura 5.2 5.0V output voltage of the buck (yellow) and output of the comparator (blue) at closed loop

Bibliografia

[1] Voltage-mode control and compensation: Intricacies for buck regulators, https://www.edn.com/voltage-mode-control-and-compensation-intricacies-for-buck-regulators/