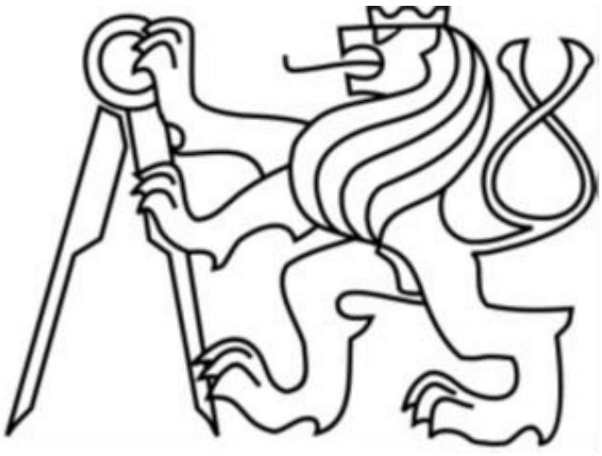
Czech Technical University in Prague

Faculty of Electrical Engineering

Department of Microelectronics



Bachelor thesis

Electronic load up to 40 A

Electronic Load up to 40 A

Author: Petr Polášek

Study program: Communication, multimedia, electronics (KME)
Field of study: Applied electronics

Supervisor: Ing. Lubor Jirásek, CSc.

Year of development: 2017

ČESKÉ VYSOKÉ UČENÍ TECHNICKÉ V PRAZE

ZADÁNÍ BAKALÁŘSKÉ PRÁCE

I. OSOBNÍ A STUDIJNÍ ÚDAJE

Příjmení: **Polášek** Jméno: **Petr** Osobní číslo: **435028**

Fakulta/ústav: **Fakulta elektrotechnická**

Zadávající katedra/ústav: **Katedra mikroelektroniky**

Studijní program: **Komunikace, multimédia a elektronika**

Studijní obor: **Aplikovaná elektronika**

II. ÚDAJE K BAKALÁŘSKÉ PRÁCI

Název bakalářské práce:

Elektronická zátěž do 40 A

Název bakalářské práce anglicky:

Electronic Load up to 40 A

Pokyny pro vypracování:

1. Prostudujte dostupnou literaturu týkající se zatěžování napájecích zdrojů.
2. Na základě 1) navrhněte a realizujte elektronickou zátěž schopnou zatěžovat zdroj s maximálním proudem do 40 A pro napětí do 100 V.
3. Proveďte ověřovací měření.
4. Zhodnoťte dosažené výsledky.
5. Navrhněte případné další změny zapojení.
6. Zařízení zůstane v majetku zadávajícího pracoviště.
7. Publikování výsledků dosažených v této práci je možné pouze se svolením zadavatele.

Seznam doporučené literatury:

[1] Krejčiřík, A.: Napájecí zdroje I. - III., BEN, Praha 2003 a další vydání.
[2] Aplikační poznámky fy IXYS, IRF, a dalších
[3] IT8500+ Electronic load datasheet [online]. B.m.: ITECH Electronics. Dostupné z: http://www.itech.sh/Upload/File/20150806110640.pdf, leden 2017.

Jméno a pracoviště vedoucí(ho) bakalářské práce:

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Jméno a pracoviště druhé(ho) vedoucí(ho) nebo konzultanta(ky) bakalářské práce:

Datum zadání bakalářské práce: **10.02.2017** Termín odevzdání bakalářské práce: _____

Platnost zadání bakalářské práce: **10.09.2018**

Podpis vedoucí(ho) práce	Podpis vedoucí(ho) ústavu/katedry	Podpis děkana(ky)

III. PŘEVZETÍ ZADÁNÍ

Student bere na vědomí, že je povinen vypracovat bakalářskou práci samostatně, bez cizí pomoci, s výjimkou poskytnutých konzultací. Seznam použité literatury, jiných pramenů a jmen konzultantů je třeba uvést v bakalářské práci.

. _____ Datum převzetí zadání

_____ Podpis studenta

Affidavit of the author of the work

I declare that I prepared the assigned work "Electronic load up to 40 A" independently and that I listed all the sources of information used in accordance with the methodological instruction on compliance with the principles of ethics in the preparation of university theses.

Author statement for undergraduate thesis

Hereby I declare that the presented work "Electronic load up to 40 A" was developed independently and that I have listed all sources of information used within it in accordance with methodical instructions for following the ethical principles during development of university thesis.

In Prague on May 25, 2017

. . . . . .

Petr Polasek

Thanks

I would like to thank my supervisor Ing. Lubor Jirásk, CSc. for helpfulness, valuable advice, willingness, and especially patience during consultations and during the preparation of the bachelor's thesis.

I would also like to thank the Silicon Hill club and especially the Bastlírna project for providing space, measuring equipment and the possibility to manufacture all the electronics here, including printed circuit boards and the mechanical construction of this work.

Annotation

This work describes the design and construction of an electronic load intended for testing power supplies up to a voltage of 100 V and a current of 40 A. This load operates in constant current mode, which is processor-controlled to behave as a constant power or constant current load . The details of the construction of this load and the technique to achieve the required properties are discussed in the work, especially the ability to (permanently) dissipate the large power loss arising from the load during the source testing.

Abstract

In this work, design and realization of an electronic load capable of testing power supplies handling voltages up to 100 V and currents up to 40 A, is described. This load is designed to operate in constant current mode which is driven by a microcontroller in such a manner to simulate constant power or constant current load. The work deals with details of construction of this load and techniques of achieving its demanded abilities, especially solutions of (permanently) dissipating heat generated on the load in the process of power supply testing.

Keywords

Load, current, power, testing, microcontroller

Index terms

Load, current, power, testing, microcontroller

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List of used symbols and quantities

BJT	Bipolar Junction Transistor, Czech bipolar transistor digital - analog
DAC	converter
DA converter	see DAC
EEPROM	electrically erasable and programmable memory of the ROM type (read only), in which it is possible to store e.g. calibration constants a type of rewritable memory
Flash	similar to EEPROM, which has however limited number of overrides
GPIO	input/output pins for any use
MOSFETs	Metal – Oxide – Semiconductor Field Effect Transistor, Czech metal-oxide-semiconductor field-controlled transistor
id	identifier
IGBT	Insulated Gate Bipolar Transistor, Czech bipolar transistor with an insulated gate
ICE	Light Emitting Diode, light-emitting diode
N-FET	field-controlled N-channel transistor
NPN	bipolar transistor composed of semiconductor layers about the NPN arrangement
P.I	see PID, but without the derivative component
SPAN	proportional – integration – derivative controller
PNP	bipolar transistor composed of semiconductor layers about the arrangement of the PNP
Sleep	Serial Peripheral Interface, serial interface for connection processor and peripherals
SWD	Single Wire Debug, programming and debugging interface STM32 processors

-	(AND)	electricity
AT	(IN)	voltage
P	(w)	performance
t	(°C)	temperature
R	(ÿ)	electric resistance
hFE	(-)	current amplification factor

1.1 Introduction

The goal of the work was to create a load capable of testing sources for voltage up to 100 V and current 40 A. Due to the fact that the load works with large currents and large power losses (up to units of kW), it was necessary to focus on the design of the device with these specifics in mind . PCBs and all wiring are resistant to the electromagnetic field caused by the large currents present and possibly their ripples. It was necessary to ensure that any wiring and control electronics were as small as possible and that they could not lead to failure or damage to the entire device. Furthermore, it was necessary to solve the problem of dissipation of power loss in the form of heat and to ensure protection in case of insufficient heat dissipation, so that failure or damage of the load due to exceeding the permissible temperature of the power elements could not occur.

1.2 Device concept

The load is constructed from functional blocks that have a precisely defined, delimited and overall function, so that it is possible in case of detection of deficiencies of one block or its failure easily replace it with another module. This is particularly advantageous in the design and testing phase designed parts of the device, because it is possible to make changes in the connection more easily (it is not the need to always remanufacture the entire device, only the changed module). There are also power blocks for example, can be easily used as teaching aids or as several separate loads, because require only power supply and communication with the control unit using a simple protocol. This approach is advantageous even within the device itself, as it can be scaled as needed so that when detected insufficient maximum current or power load, just add more modules, thereby increasing the capabilities of the entire device without the need for other modifications. When constructing the whole device as a whole, the resulting device could meet the set requirements exactly, but in the event of a change in requirements or the need to modify the device's function, could show that such a modification would be so difficult that it would be less demanding to redesign the entire facility to meet the new requirements.

2.1 Theoretical preparation of function principles

The division of the device into functional blocks was chosen for the design. The device is divided according to the following drawing:

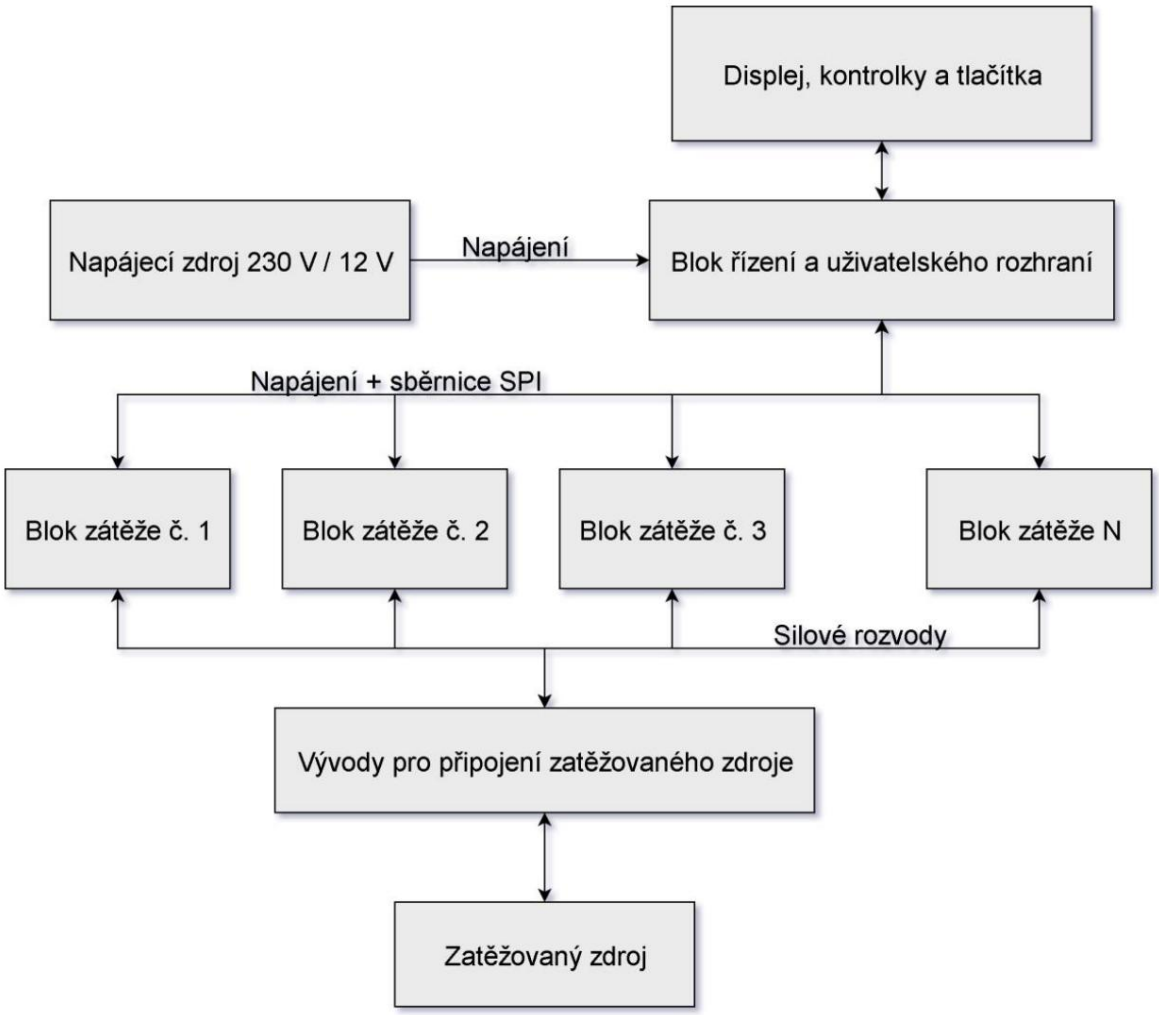


Figure 2.1: Principle arrangement of power load

By dividing it into modules, we gain an advantage – individual load blocks can be connected in parallel and easily increase the range of currents and powers with which the load can work. An important feature of the load blocks is that they behave as a so-called current sink, so if they are connected in parallel, the same current will flow through them all and the power will be distributed evenly between the individual modules (provided that only negligible voltage drops occur on the power distributions between individual blocks).

If the loads worked on the principle of constant voltage, it would be much more difficult to achieve an even distribution of power. For this, it would be necessary to measure the current through the individual modules and balance them against each other. In essence, this is a similar problem as when connecting ideal voltage sources. In the case of such a construction, it would easily happen

to the fact that all the current would flow through one module and none through the others, which it could have destructive effects. Any such load would have to be rectified so that the same would flow through it current like the others, which brings us back to the principle of current load. In addition to appearance to the fact that all load modules would have to communicate with each other very quickly (that is, each module with all others), the complexity of such a solution.

A possible solution would be to connect voltage loads in series. The disadvantage of this solution would but it was that the minimum voltage from which the load works would increase N times. This tension varies according to the technology on which the load is built around 1 V – 3 V [1], [2]. required for full load function. It can thus easily move in the order of tens of V when using a larger number of modules. This limitation is given by the physical principles of the semiconductor function (and the loss in the measuring resistance) and cannot be improved in any way. Another problem with this solution is that a fault on a single module would overload the other modules if the faulty piece were to short out. In the event that the flow of current would suddenly be interrupted due to a defective piece, the current would stop flowing through the loaded source immediately. In the first case, there would be a risk of damage to the load, in the second case, there could be an overshoot of the voltage on the loaded source, which could cause damage to the measuring circuits of the devices that measure the voltage on the loaded source.
For these reasons, the method of measuring voltage and loading with current tunnels was chosen.

Due to the intention of using this load for testing power supplies, the load supports 2 modes of operation - constant current mode and constant power mode. By modifying the software, it is possible to adjust the load for other function modes, e.g. constant voltage mode (the load maintains the set voltage at its terminals), constant resistance mode, or pulse mode. However, these modes usually do not provide relevant information when testing resources, so they are not implemented in the firmware. The reason is that in constant voltage mode, only the behavior of the source can be tested in the working area, where it is overloaded and its output voltage decreases under load. Hard sources cannot be tested this way at all. In addition, the constant resistance mode does not provide any information against the constant current mode, it only complicates the measurement of the source parameters, since it is necessary to write exactly 2 measured variables – current and voltage (in constant current mode, current is a parameter, so we have to write just one measured value), eventual one add up from the other. Impulse mode can only provide very rough information about stability loaded source [3]. A real stability test needs to be tested with a generator connected to the feedback of the source and the vector voltmeter. So only those are implemented the most useful two working modes. Other possible modes can be taken from [4].

3.1 Current load block

The basic principle on which the current load block is based is an analog regulation loop ensuring the maintenance of the set current. The principle block diagram is indicated in the drawing:

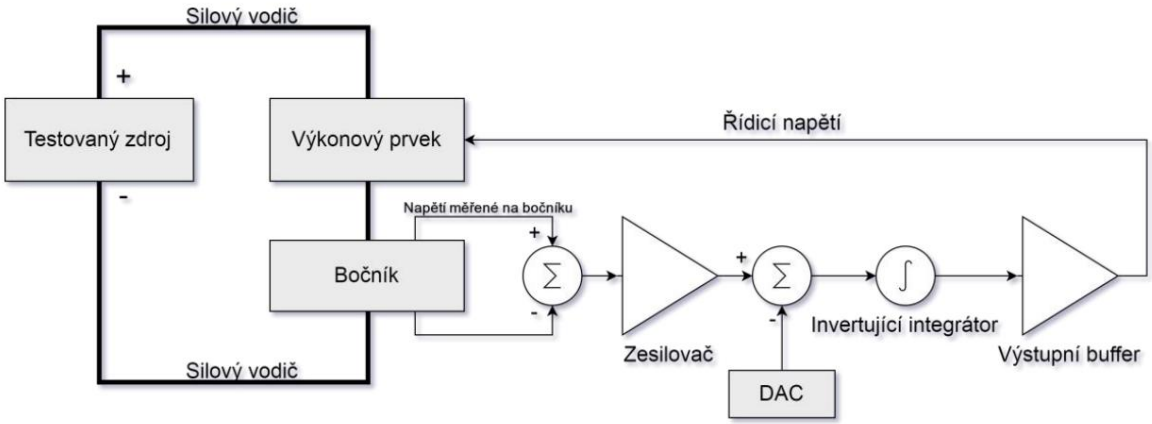


Figure 3.1: Principle diagram of the current load block

3.2 Explanation of the basic principle of the function On the shunt, the current is measured as a voltage drop [5]. This tension is amplified by the appropriate by a differential amplifier1 with a defined gain, then fed to a differential amplifier, where it is compared against the control voltage from the DA converter, the result is fed to the inverting integrator, and the resulting voltage is fed to the control electrode of the transistor. Behind the integrator there is a voltage monitor (buffer), the purpose of which is to separate the integrator from the power element. A MOSFET-type transistor is used as a power element in this design, which is controlled by voltage, but from the circuit point of view (simplified) it appears as a capacitor connected between the control electrodes [6]. Thus, the integrator could be current-stressed or overloaded during rapid changes in the voltage at the output, which could lead to unexpected and poorly simulated behavior of the control loop. The output buffer prevents this phenomenon.

It is therefore a simplified PI controller [7], which has a zero sum coefficient for the proportional and derivative components. Since we know the nature of the controlled system (for the working area of the load it is a MOSFET connected in common collector mode), there is no need to use these components. The derivative component is not necessary because the transistor cannot overshoot in this feedback circuit. The proportional component does not make sense to use, because the dependence of the current flowing through the MOSFET on the control voltage is

[1] The amplifier used should have as little voltage offset as possible. However, the demands are not so high that it is necessary to use *zero-drift* or *chopper-stabilized* amplifiers. Commonly available precision OZs, for example OP07, OP27 and the like, are suitable for this purpose. However, unipolar OZs are completely unsuitable for this use, as they normally have an input voltage offset of about 2 orders of magnitude larger. OP07 was used in the connection for suitable parameters, low price and good availability

quadratic. Only a linear system can be controlled by the proportional component, using it here would either it was not capable of independent regulation (the linearity error would have to be compensated by the integrator) or it could cause regulation instability in the form of overshoots, especially at high frequencies where the integrator would no longer be able to compensate for its behavior.

The reason for using the amplifier in the shunt is the fact that for the smallest possible power loss, it is necessary to choose resistance of small values (on the order of tens to hundreds of mÿ). On such a small one resistance then there is a small voltage drop (when using a 10 mÿ shunt there is a voltage drop 10 mV/A). Therefore, this voltage needs to be amplified to a greater level to be able to handle it more easily work. OP07 operational amplifiers with a small voltage input offset [8] are used instead of the input amplifier and the error amplifier, which minimizes the measurement error.
For these circuits, the size of the input voltage offset is typically 30 ÿV, maximum 75 ÿV [9].
This offset corresponds to a measurement error of 3 mA for this connection, or 7.5mA. Although operational amplifiers with a smaller offset are also produced, e.g. [10], [11], [12], [13], their price is currently several times higher than that of the OP07, moreover, it is usually only a selected variant of the given circuit from the best produced pieces, while retail chains mainly offer cheaper variants with a larger offset, which are 4x - 10x more expensive than OP07.

Special zero-drift or chopper-stabilized amplifiers are disadvantageous for large output noise and low frequency unity voltage gain [14], as a result of which the control loop would be very slow.

The shunt is connected so that it is connected between the source of the power MOSFET (N-type) and the loaded source. The power MOSFET is connected so that the source is connected to the local ground of the load block (each block is floating and isolated from the rest of the device). This connection simplifies current measurement - the measured differential voltage is not superimposed on any DC or AC source, thereby limiting the number of problems arising during measurement, especially the penetration of the positive component of the measured voltage into the output voltage. Given that the source voltage can be up to 100 V and the measured voltage is in the order of hundreds of mV, this is a significant limitation of measurement errors, especially errors caused by the tolerances of components in the connection of the differential amplifier. In addition, the current flowing through the control electrode at

when the control voltage changes, it closes through the local ground, so it has no effect on the measured value current.

3.3 Choice of power element

Applicable power elements include: BJT NPN, BJT PNP, N-Channel MOSFET, P-channel MOSFET, IGBT.

An N-channel MOSFET was chosen as the power element for the load. Other technologies were excluded based on worse parameters or higher price.

The reason for not using BJT PNP and P-channel MOSFET are worse parameters than for N elements, mainly because of the lower electron mobility of P semiconductors [15]. As a rule, with the same dimensions and price, they tend to have a smaller permitted emitter/source current and a smaller power loss.

The BJT NPN was not used for example due to the small current gain. Transistors for the required powers usually have a current gain of hfe<50 due to the Kirk effect at large collector-emitter currents, which requires a power amplifier for current injection into the base. This results in a large power loss in the driver. Due to the fact that the load modules are powered by an isolated DC/DC converter, their supply current is limited to tens of mA. In order to use a BJT, it would therefore be necessary to additionally develop a self-isolating DC/DC converter capable of supplying large currents.

A partial solution is the use of a Darlington pair, which, however, has a minimal working capacity voltage of approximately 1.5 V [16]. By using a modified Darlington pair with an N-MOSFET as with a BJT driver it is possible to reduce the minimum working voltage to approx. 0.8 V, however a large heat loss, up to tens of W, could occur on this drive MOSFET (if we consider a source voltage of 100 V and an excitation current of hundreds of mA). This is how the wiring would contain not one but two power elements, erasing the benefits of using a BJT. Current the collector is also highly dependent on the applied voltage collector - emitter due to Early phenomenon [17], which makes regulation difficult for sources that may oscillate under load. Even when overcoming these difficulties, however, we will finally encounter a problem with the availability of power NPN transistors. Of the types sold today, these transistors usually have parameters for use in audio technology (power loss max. 250 W, TO3 case, for which it is difficult to manufacture a cooler) and high price. This is because they have already been supplanted by unipolar in almost all branches of electronics transistors or IGBT transistors, with which smaller power applications are achieved losses. It was not so used for both technical and economic reasons.

The IGBT was not used mainly because it is not suitable for use in linear mode. Although as a rule, they have a large permitted operating voltage and large switching currents, but permitted power loss is usually small (TO220 case, power loss up to 60 W). Transistors in larger cases are usually available at high prices (they are produced mainly for means of transport, not for consumer electronics) in the form of intelligent modules that

they contain internal electronics that take care of switching these transistors. These performance types are thus not applicable for linear applications.

In contrast, MOSFET transistors offer suitable parameters. They can also be used in linear applications, they do not suffer from the Early effect, they are field controlled, so a current is needed to control them only
in case the voltage on their control electrode changes. Commonly available types are sold
e.g.
in a TO-247 case, which allows up to 300 W of heat to be transferred [18]. In the long run, it is possibly even higher reliability, bipolar transistors at high temperatures suffer from the problem of dopant migration [19 p. 19], which changes their parameters over time, while the initial problem can be a significant drop in hfe to a fraction of the original value . On the other hand, unipolar transistors contain only one type of semiconductor, and unwanted dopant migration should not have such a significant impact.

To realize the load, the IRFP260N transistor type in the TO-247 case was chosen, which is usable for currents up to 35 A - 50 A [18] depending on the temperature at which it is maintained.
The permitted working voltage is 200 V, which is sufficient for this load. With very good cooling, keeping the transistor at 25°C, it would be able to operate at a power loss of 280W, at 100°C (water cooling is a temperature the transistor should not be able to heat up to) 115W. Cooling it is therefore essential to achieve the highest possible power loss.

3.4 Choosing a suitable shunt

With an ideal shunt, phenomena such as temperature dependence of resistance on temperature do not appear. For metals, this dependence is positive, so the resistance of the shunt increases with its temperature. In practice, we cannot neglect this phenomenon [20]. With the currents with which the load works, it is already necessary to take this dependence into account [21]. Therefore, we try to achieve the smallest possible power loss on the shunt by using the smallest possible resistance value (see chapter 2.1), the best possible cooling
shunt
and using material with the lowest possible temperature coefficient.

Assuming a linear dependence of resistance on temperature (usually only valid for a limited temperature range or for some metals, otherwise courses according to [22]):

$$RR\ ttk\ \text{ÿ}\ \text{ÿ}1\ \text{ÿ}\qquad AR\ \text{ÿ}\ \text{ÿ} \tag{6.4.1}$$

where *R0* is the original resistance value, *t* is the current temperature, *tA* is the reference temperature and *kR* is the temperature coefficient

In addition, the following applies:

$$t\ t\text{ÿ}\ \text{ÿ}\ \text{ÿ}\ t \tag{6.4.2}$$

$$\text{ÿ}\ \text{ÿ}P\text{ÿ}\ tk_{TR} \tag{6.4.3}$$

where *kT* is the thermal resistance of the cooler (for ideal cooling equal to 0, otherwise > 0). Then:

$$P_{R}^{2} \tag{6.4.4}$$

$$\text{ÿ}\ \text{ÿ}\ \text{ÿ}\ tk_{T}^{2} \tag{6.4.5}$$

where I is the current through the resistor. It is necessary to realize that power loss it does not depend directly on the original resistance value, but on the instantaneous value

$$R\ \text{ÿ}\ \text{ÿ}\ kk\ I\ \text{R}_{TR}\quad \text{ÿ}\ 2 \tag{6.4.6}$$

$$R\ \text{ÿ}\ \frac{R_0}{1\quad R_0 kk_{TR}\ I^{2}} \tag{6.4.7}$$

We can therefore define the relative change in resistance as follows:

$$\frac{\text{ÿ}\ R}{R_0}\ \text{ÿ}\ \frac{1}{1\quad R_0 kk_{TR}\ I^{2}}\quad 1 \tag{6.4.8}$$

Since the shunt is to be used as a measuring element, it must be minimized
change in resistance depending on the current flowing. Since the size
the flowing current cannot be influenced, it is necessary to either use a resistor with a small value or
small temperature coefficient or improve cooling.

Although the formula only applies to the linear dependence of resistance on temperature, it serves well as outlining the problem that needed to be solved. The best solution is to minimize them all
parameters that affect this dependence.

3.4.1 Minimization of measurement error on the shunt at large currents

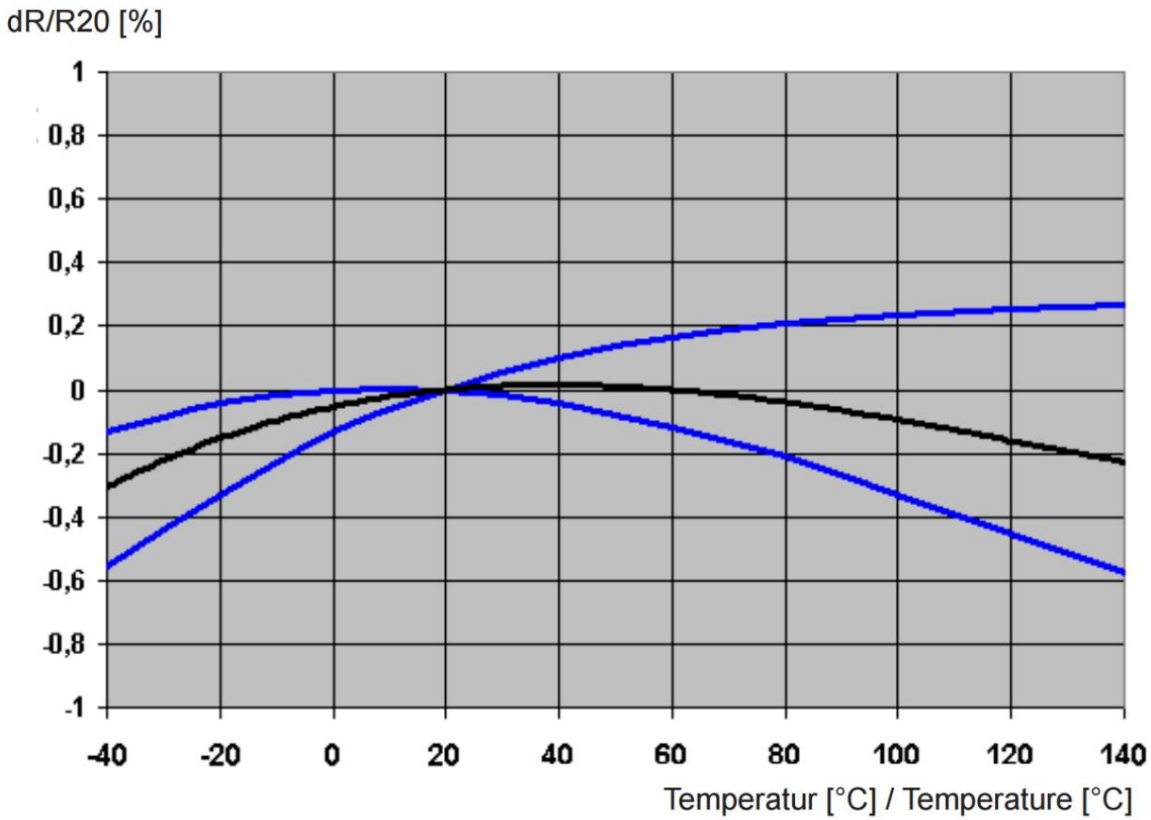
The logical step is to first eliminate the phenomenon itself by choosing the material
with minimal temperature dependence. Of the commonly available materials, manganin is usually used, which has a coefficient ÿ = 2.10-6 K^{-1} [23]. Only special materials have a lower temperature coefficient
significant gold content. However, such shunts are not available on the market, that's why they are
manganin shunt is the best option and is used in the connection of the load.

The second step is to reduce the base resistance value. For currents in the order of tens of A, resistance values greater than tens of mÿ are quite impractical. The power losses are so great that it would be necessary to solve not only the cooling of the load, but also the shunt itself in a complex way. However, shunts of such small values are not normally produced in standardized series, but in a few values, from which the value of 10 mÿ is the most suitable for the required use. At this resistance value, the heat loss of the shunt reaches units of W at most, which is already a realistic performance that can be easily cooled. Unfortunately, smaller values of shunts are not normally produced, at the same time a problem arises with measurement on such a shunt, because a current of 1 A corresponds to a drop in units of mV, which can cause difficulties during measurement. The measurement of such voltages is necessarily burdened by noise, interference from the environment and imperfections of amplifiers (especially voltage input asymmetry and its temperature and time drift).

When using manganin, for temperatures around 25 °C, an approximately linear dependence of 50 ppm / K is valid. In fact, it is a parabola, the resistance has the same value at 25 °C and at 60 °C.
In this area, it has a tolerance of up to 0.02% [24]. This range includes the entire range of 10 °C – 70 °C. At higher temperatures, the resistance of the manganin resistor decreases. Graph 1 (taken from [25]) shows the course of this temperature dependence.

The measurement error caused by the temperature dependence of the shunt could be compensated by measuring the temperature of the shunt and the inverse function calculated in the microcontroller. The disadvantage of such a solution is the increased computational complexity. Since the resistance tolerance is
in the range 10 °C - 70 °C 0.02%, which at 20 A corresponds to an error of about 4 mA, not necessary
compensation cannot be implemented in any way, because the larger measuring error is caused by the measuring devices themselves
operational amplifiers (it could be solved by using a more perfect type) and component tolerances

(more accurate than 0.1% is not normally produced). For this reason, it makes no sense to implement compensation. On the contrary, in the event that the theoretical course of resistance dependence on temperature did not correspond exactly to reality, the error could increase even more.



Graph 1: Temperature dependence of the manganin resistance of the PBH F1 series (taken from [25])

The PBH F1 resistor from Isabellenhütte Heusler was chosen as the shunt GmbH & Co. with a resistance of 10 mÿ. This shunt can be loaded up to 10 W when used with a cooler, which roughly corresponds to a current of 31.5 A. So at least two modules are needed for this work, because it is not possible to reach a current of 40 A with one module. It is possible with two modules already theoretically reach a current of 63 A.

3.5 Connection and principle of operation of the load block The
basic principle of the load block has already been outlined in section 12, figure 6.1 contains

principle diagram. Figure 3.2 contains the connection of the analog part of the load block.

3.5.1 Principle of operation of the analog regulator of the load block

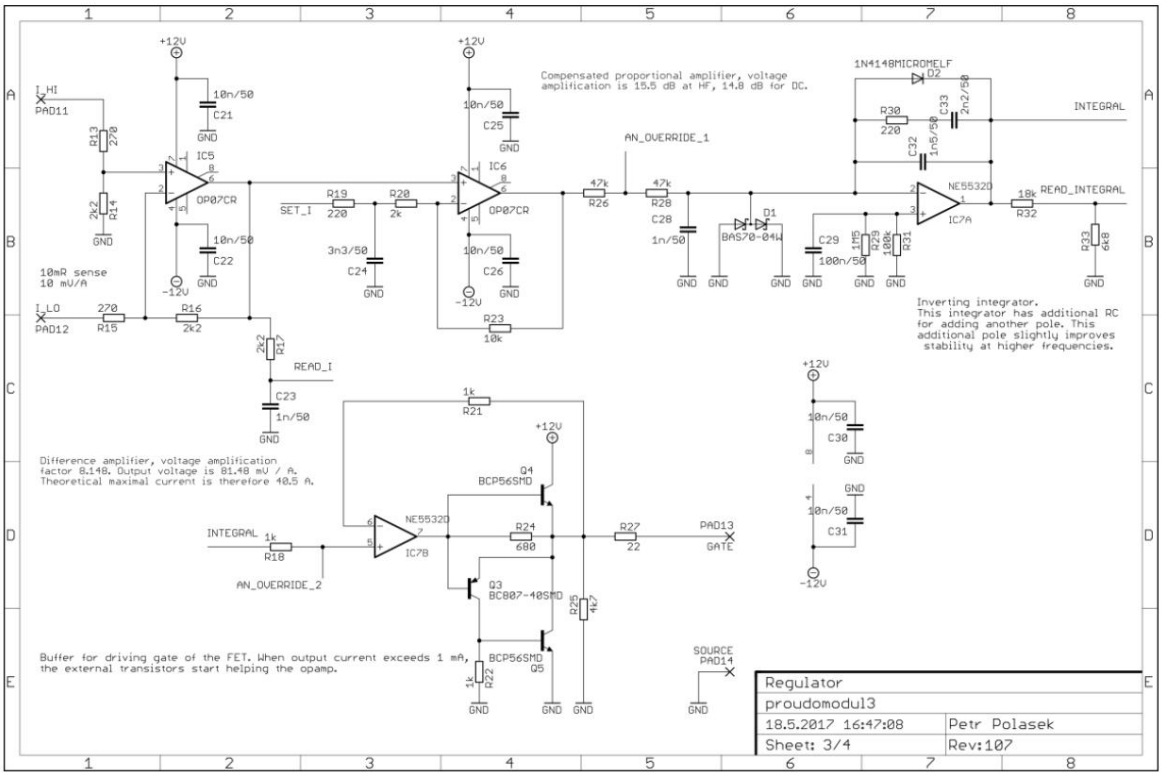


Figure 3.2: Schematic of the analog part of the load block

The schematic that Figure 6.2 shows is based on the wiring created for
projects A2B34IN1 and A2B34IN2, the continuation of which is this work. Contains bug fixes,
shortcomings

and functions that were missing in the prototypes created for the needs of these subjects.

The control loop is solved analogically, because it allows faster, more accurate
and more stable steering than with direct digital steering. It only controls the processor using the DAC
control voltage with which the control loop is set to the current value it should maintain (SET_I branch). This allows
computing power to be used for communication, load management and error condition detection.

The input amplifier, which measures the voltage drop on the shunt, and thus indirectly the current passing
through the load, is implemented differentially. In the prototypes there was a ground loop problem arising when
connecting a simple amplifier, which largely eliminates this solution.
To perfectly suppress this phenomenon, it would be necessary for the tolerance of the components to be zero,

unfortunately, commonly available components have the smallest tolerance of 0.1%, however, this solution seems to be sufficient.

The amplifier is followed by an error amplifier. Here the amplified measured is compared voltage with the voltage from the DAC. The resulting voltage indicates the difference between desired and actual measured current. If the load is working properly and the loaded source is capable to provide the desired current, the voltage at the output of the error amplifier is zero (referenced to ground).

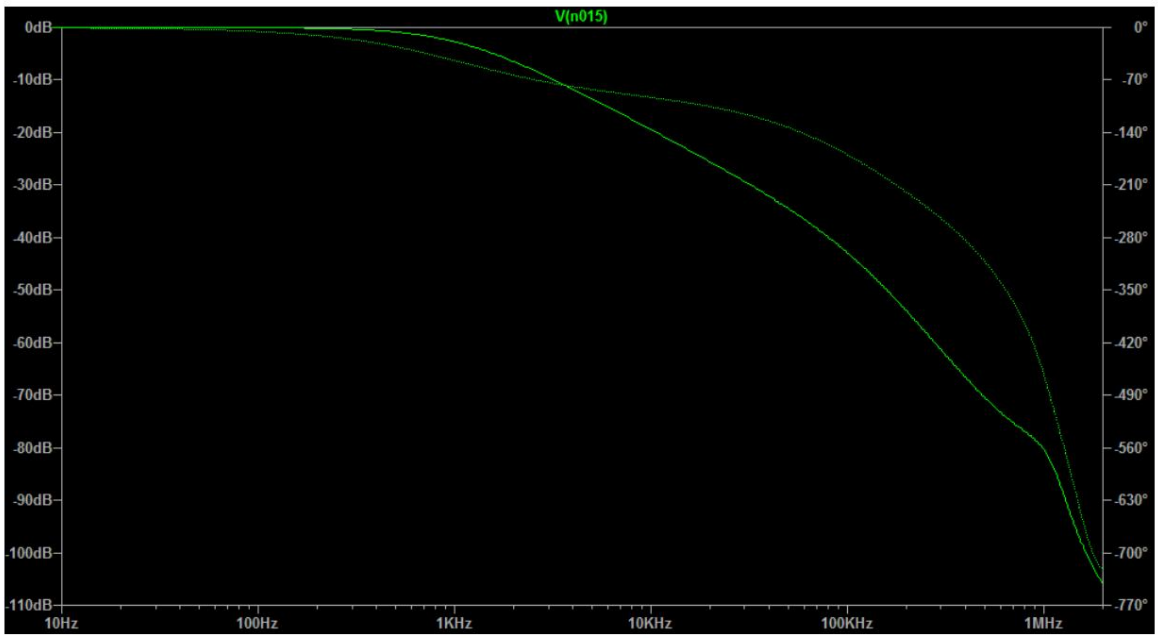
The input of the integrator is the voltage from the error amplifier. The integrator accumulates this error and introduces it as feedback, whereby the controller always converges to the correct value current.
A diode is connected in the integrator, which prevents the voltage at the output from being less than about -0.5 V, so the integrator cannot reach saturation in the area of negative output voltage. Switching on the load from the zeroing mode of the integrator or the zero set current takes a significantly shorter time. A double Schottky diode is connected at the input of the integrator, which prevents the generation of a large voltage at the input of the integrator in the event that the integrator reaches positive saturation. This again shortens the recovery time to normal work mode.

The output buffer is used because the operational amplifier used for the integrator is not capable of delivering large currents from its output. Therefore, a buffer is included behind it, which works as a voltage tracker. The transistors used in the buffer will open when the current flowing from the amplifier output exceeds about 1 mA. Operational amplifiers are thus not subjected to current stress, thereby limiting the possibility of their overheating, damage or oscillation.
At the same time, it is thus possible to control the gate of the power transistor more quickly.

3.5.2 Transmission characteristics of the analog controller and its stability

Transmission characteristics of the controller without a closed loop (Graph 2) and with a closed loop the loop (green) is on graph 2. According to the simulations in the LTSpice XVII program, the controller should be stable.

Graph 2: Transfer characteristic of the controller without a closed control loop



Graph 3: Transfer characteristic of the controller with a closed control loop

Since the controller has a phase shift of 180° up to a frequency of 118 kHz, where closed loop has a gain of -45 dB, it should not be possible for the controller to self-oscillate [26].

3.5.3 Principle of operation of power supply and filter circuits

Figure 3.3 contains a diagram of the power supplies of the load block. All analog even the digital part of the load block is floating. The power supply is realized by a DC/DC converter, on which input is 12 V, output voltage is ±12 V, output is galvanically isolated from input, permissible the voltage between input and output is 1.5 kV. The maximum current through one power branch is 42 mA. According to the manufacturer, the inverter can be overloaded so that the total supplied current is 84 mA [27], [28]. This property is not used in the connection, the current drawn by the electronics is approximately 36 mA from the positive branch and 15 mA from the negative branch. Depending on the operating frequency of the processor and the state of the surrounding electronics, the current in the positive branch may drop to 20 mA, but usually during operation it varies between 32 mA and 36 mA.

However, these DC/DC converters are not regulated or suppressed, so the output voltage is measured pieces (2 pieces of A1212S-1WR2 from the manufacturer Mornsun and 3 pieces of AM1D-0512DZ from the manufacturer Aimtec were tested) ranged from 12 V to 15 V. 15 V was reached by these converters only without load. With a defined minimum load of ±5 mA, the output voltage was around 13 V, with the highest allowed load 11.5 V – 12.5 V. The output noise reached tens of mV peak-to-peak, which could cause problems with the measurement of small voltages, therefore the supply voltage filters follow the source.

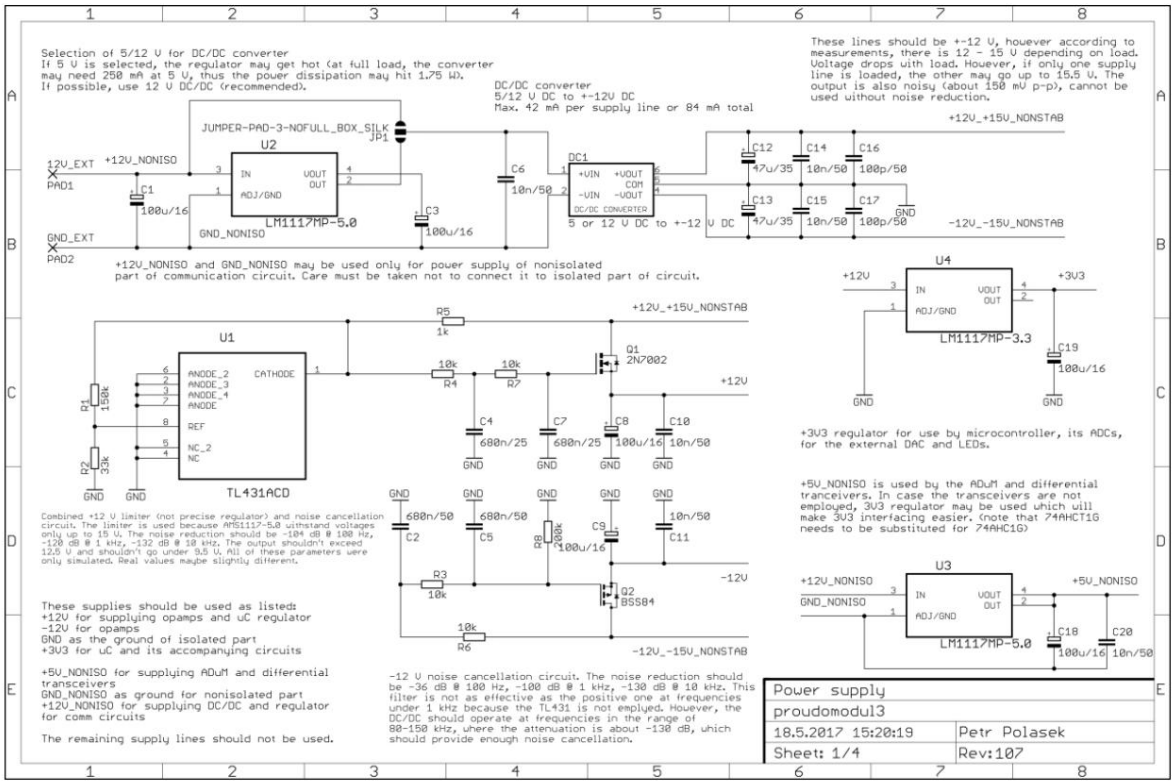


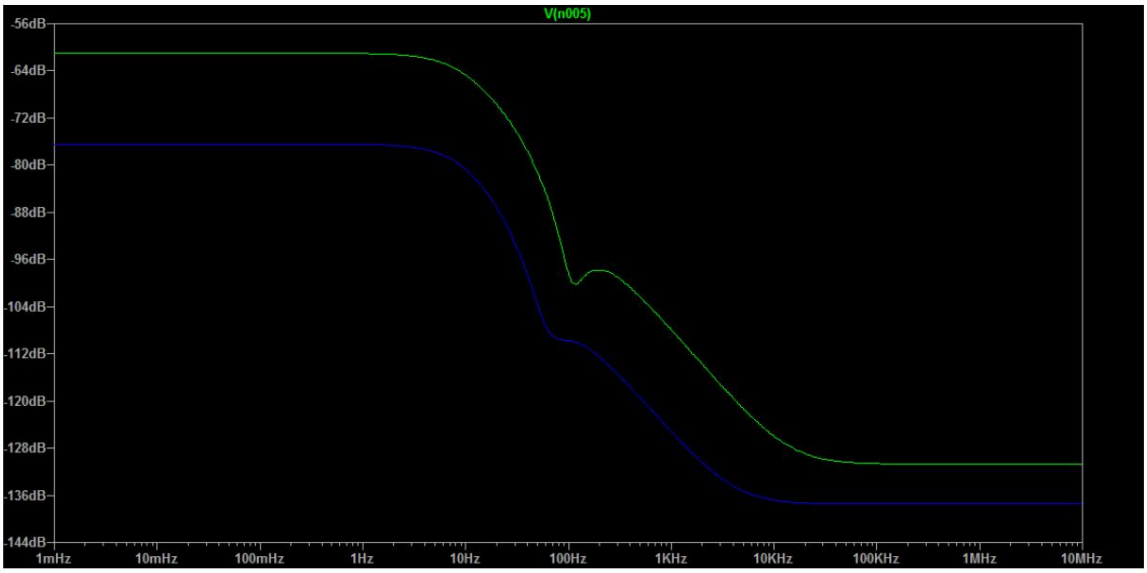
Figure 3.3: Schematic of load block power supplies

Supply voltage filters are implemented using voltage trackers that work based on the principle of filtering the power supply through 2 RC filters, which is then used as the control voltage of transistors Q1 and Q2. Since their gate voltage is filtered out, it is Noise has also been largely eliminated from the output voltage.

3.5.4 Transmission characteristics of power filters

Graph 4 contains the simulated transfer characteristic of this filter. Blue curve is the filter in the positive branch, green in the negative branch. At 100 Hz, it achieves an attenuation of 30 dB, at 1 kHz 87 dB, at 10 kHz 120 dB. The variant in the positive branch of the power supply achieves even greater attenuation at low frequencies, or 98 dB, 108 dB and 126 dB. So much attenuation ensures that any noise from the DC/DC converter will be attenuated to an unmeasurable level. Together with the PSRR of the operational amplifiers used, the penetration of noise from the source into the measured signals can be at most -130 dB. Considering to the measured noise level and its frequency distribution (the converter works at 80 kHz – 120 kHz) thus, the effect of such noise will be immeasurable, as it will be significantly smaller than the inherent noise of operational amplifiers. The filters thus fulfill their function as expected. The positive branch also contains a voltage limiter, which limits the output voltage to a maximum value of 12.2 V. The reason for not using conventional stabilizers is the fact that they do not sufficiently suppress noise, moreover, this suppression decreases with frequency, while it increases with the design used.

The analog part and the 3.3 V stabilizer for the microcontroller are powered from these ±12 V suppressed branches. The simulation was not confirmed by measurement because the technique required for this measurement (in the order of nV) is unavailable.



Graph 4: Transmission characteristics of power filters

3.5.5 Connecting the digital part of the load block

Figure 3.4 contains a diagram of the digital part of the load block. A microcontroller is used STM32F030F4P, which is responsible for communication with the controller and DAC. At the same time used to measure the voltage in the circuit and evaluate whether an error has occurred. In this part the scheme also includes circuits for zeroing the integrator and emergency shutdown of the load. Next here it has indicator LEDs that signal the state of the load and the switching on of the reset and emergency circuit. The last essential part is the connector with the programming and debugging interface SWD.

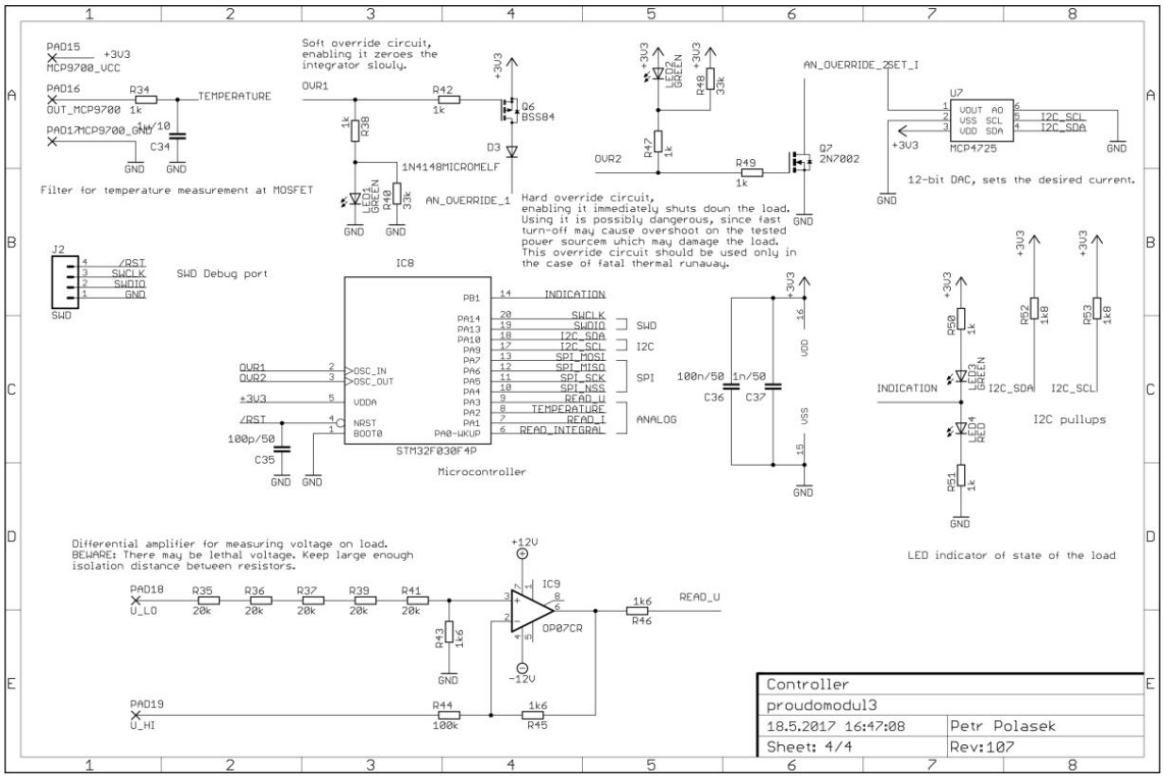


Figure 3.4: Circuit diagram of the digital part of the load block

3.5.6 Microcontroller and DAC used

The processor used is a thirty-two-bit ARM Cortex M0 microcontroller from ST Microelectronics with type designation STM32F030F4P6 [29], [30]. It is a microcontroller intended for undemanding and simple applications, where it replaces outdated eight-bit ones microcontrollers both for their low price and their computing power and equipment. Contains 8 MHz internal oscillator and PLL, so it can work up to 48 MHz, while the computing power reaches 44 DMIPS, GPIO pins can be switched with a frequency of up to 24 MHz, it contains one twelve-bit AD converter with a sampling rate of up to 1 MSa/ss multiplexer. Given that s

with the given capabilities, classic families of microcontrollers (8051, Atmel AVR, Microchip PIC etc.) to compete on price, this microcontroller was chosen.

As of May 2017, the price of this microcontroller is around 40c (CZK 9.60 according to of the current exchange rate as of 5/24/2017). Since only very outdated and underpowered processors (eg ATtiny and six-pin processors) were found in the same price range processors), for which there are also very limited and paid compilers, and the only drawback the chosen microcontroller has only 15 GPIOs, but these are enough to control the load block, there was no reason to use another microcontroller.

Since the microcontroller does not contain an integrated DA converter, a twelve-bit DA converter MCP4725 [31] was used. A multi-bit converter would allow finer control of the load, but sixteen-bit converters are significantly more expensive, and the control step with this converter comes out to 8.08 mA according to the measured values. Since the load block itself is rated for a maximum current of 30 A, and changing the temperature of the differential amplifier from 25 °C to another temperature in the range of 0 °C - 70 °C, the input voltage unbalance can increase by up to 55 ÿV, which corresponds to a measurement error of 5.5 mA (i.e. comparable to the control step), it makes no sense to increase the number of bits of this converter. The advantage of this type of converter is that it contains an EEPROM, which contains information about what mode and code word to enter after power-up and what voltage to set the output to. This allows the converter to be set so that when the entire device is switched on, it is set to the on state and the output is set to zero voltage, i.e. zero load current. Thus, an undefined load state should not occur when switched on.

3.5.7 Connection of communication circuits

Figure 3.5 contains the wiring of the ADuM2401 digital isolator and differential transceivers. ADuM2401 is a modern successor to optocouplers, it enables galvanic separation of fast digital signals. The BR variant used enables transfer rates of up to 10 Mb/s [32]. Allowed DC voltage between isolated parts is 846 V, AC voltage up to 565 Vrms. Compared to optocouplers, even at such high transfer rates, it does not consume much, only 2.1 mA per channel (it contains 4 channels, 3 in one direction, the last one in the opposite direction).

The 75176 [33] differential transceivers are used in case the load block is used separately on long cables, when transmission reliability using standard SPI could be an issue. Although transceivers limit the transmission speed to roughly 1 Mb/s, they ensure transmission reliability by being significantly more resistant to induced due to harmonic interference and due to the matched impedance at the ends of the cables, they do not occur reflections. In case the module is used as part of the device described in this work, it is not transceivers must be used because the cables inside the device are short. In that case,

the transceivers are not installed, the PSH connector is installed, which provides communication and power from the control block.

Since the SPI bus uses an inverted slave select signal, while the ADuM2401 and 75176 integrated circuits need a non-inverted one to turn on signal, i.e. logical H in case the data channel is to be switched on in the direction out of the block load, a 74AHCT1G14 single-gate inverter is used (74AHC1G14 can also be used), which provides the function. It is a small component in a 5-lead SOT23-5 package, which saves a significant amount of space compared to the standard 74*14 model, which has 14 leads.

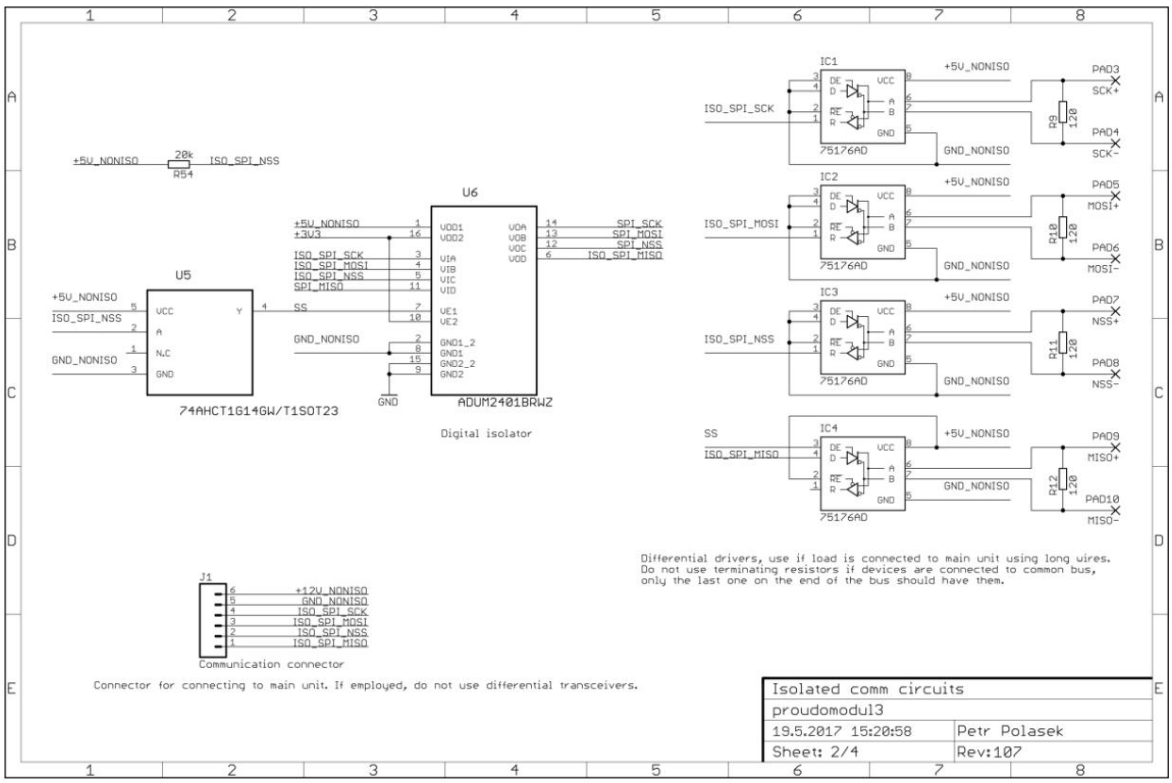


Figure 3.5: Circuit diagram of isolated digital communication

3.6 Construction of the load block printed circuit board The printed
circuit board was designed in Eagle software and fabricated by photolithography on

double-sided printed circuit board, a non-soldering mask was also created by photolithography.

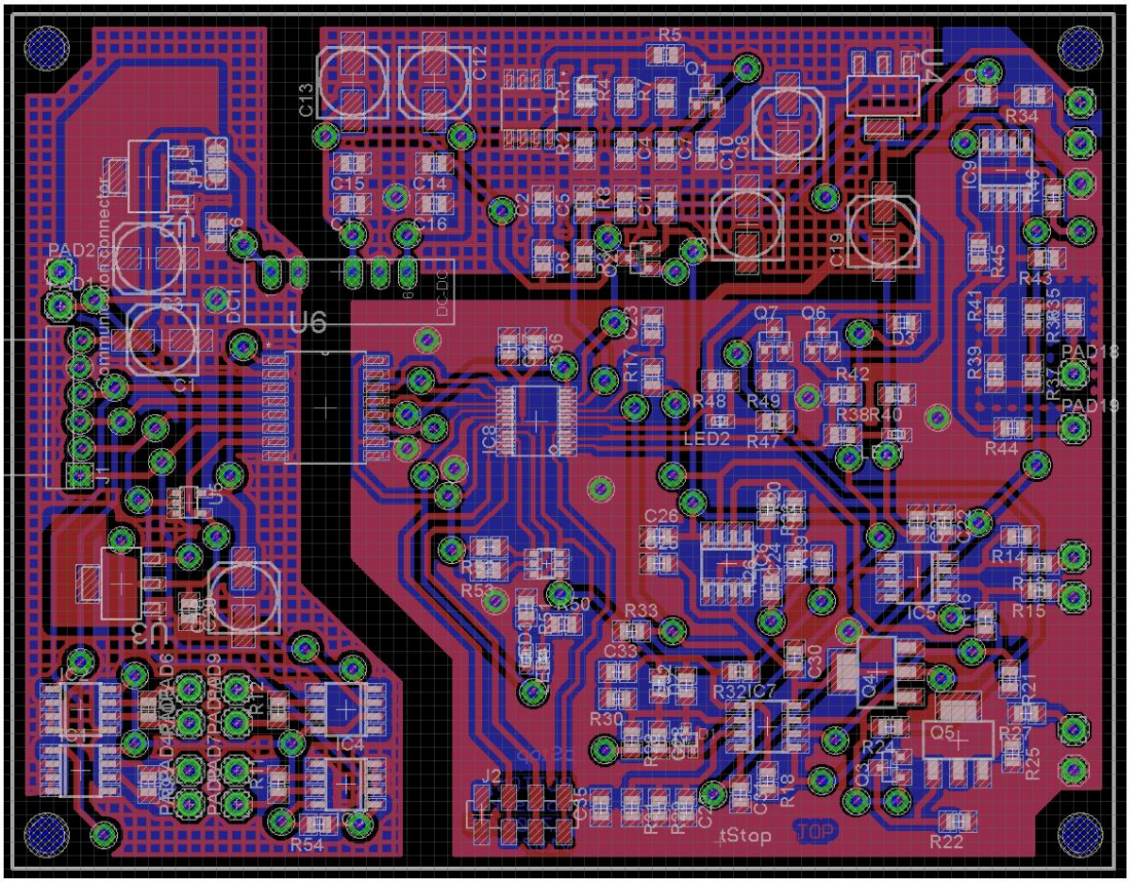


Figure 3.6: Motif of the designed PCB of the load block

The photolithographic process used in the production of printed circuit boards uses the so-called dry negative photoresist, which is a foil sensitive to UV radiation. In places where it is irradiated, it polymerizes. On a transparent film was attached to the cuprextite plate with blackened places where it should have remained copper foil. Subsequently, the unpolymerized parts were removed using a soda solution. IN the places where the photoresist did not polymerize was bare copper at this point, which was etched away in an etching bath (sodium persulfate solution was used). Subsequently, it was for chemical protection carried out surface electroless silvering in a chemical bath. After washing, the printed circuit board was painted with a prepolymer mass spread in a thin uniform layer under a transparent foil. The was developed again, unpolymerized residues were removed with alcohol. After further curing mask in UV radiation, the PCB was cut to the required size. Subsequently, they were drilled holes for metal fittings and component outlets with a carbide drill, rivets with an outer diameter of 1 mm (Figure 6.9) were inserted into the holes and tapped with a punch (Figure 6.9), which was then used for ensuring contact soldered to the PCB. Finally, the components were soldered (Fig 3.8).

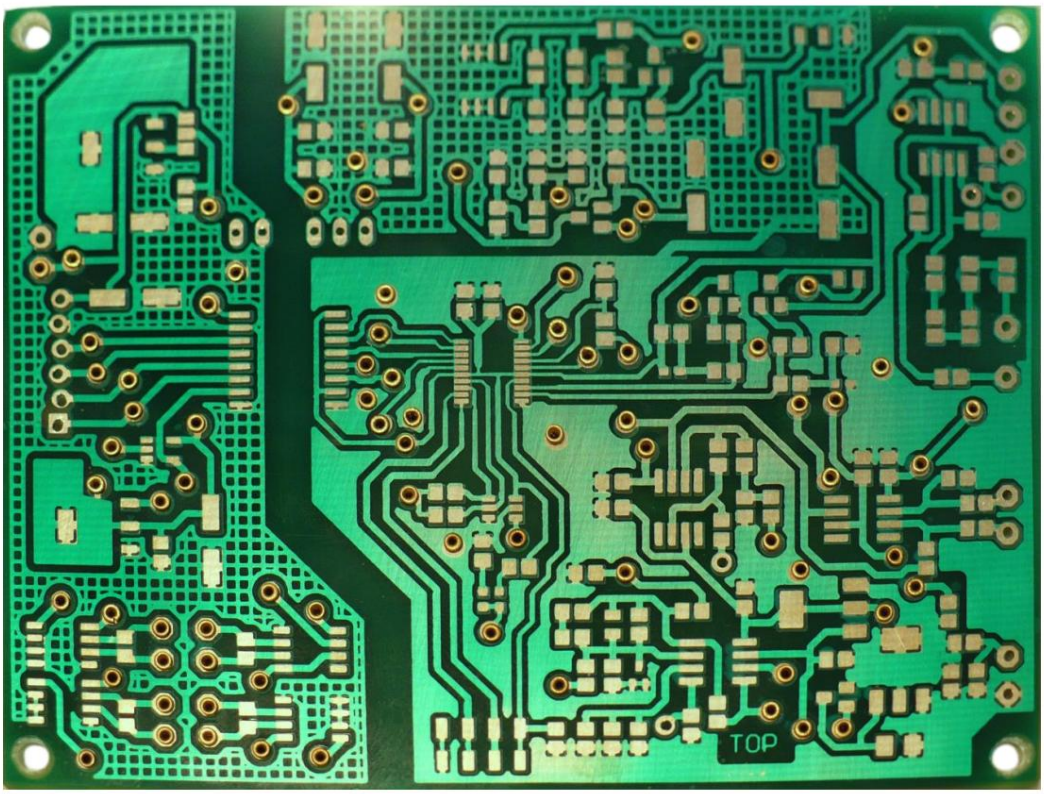


Figure 3.7: Fabricated PCB of the load block with unsoldered pins

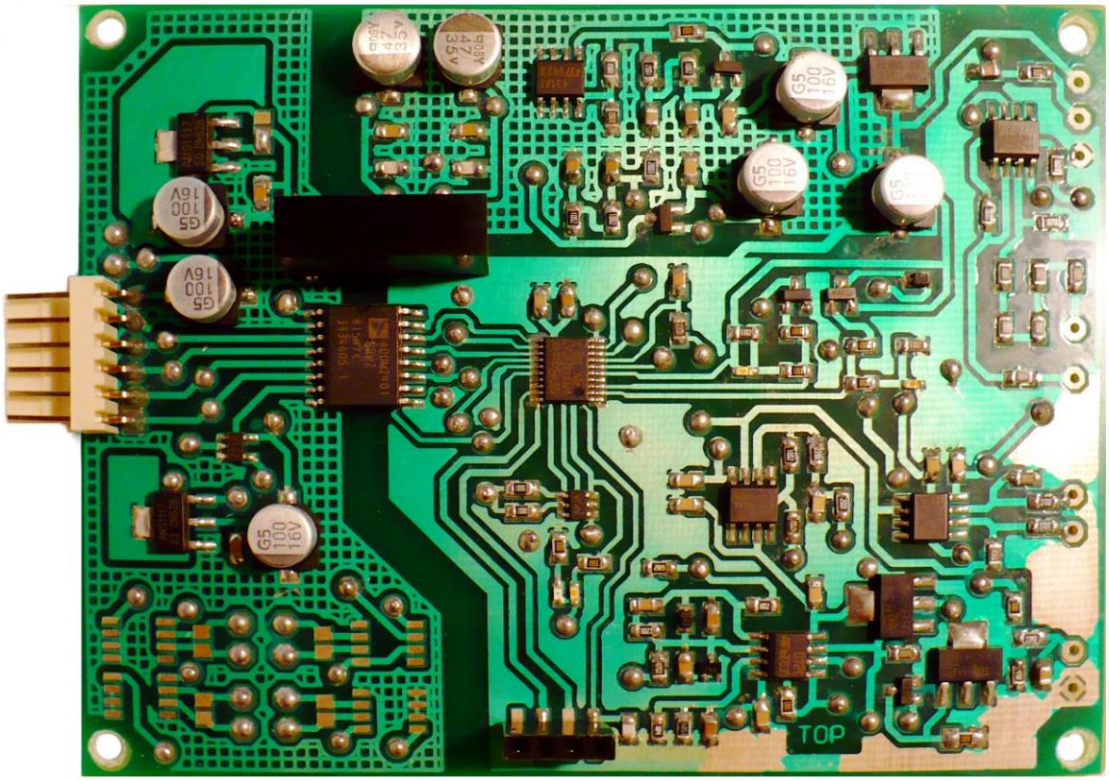


Figure 3.8: Manufactured and fitted load block piece

3.7 Treatment of error conditions

Several error states may occur during operation, which were necessary to treat, otherwise there could be damage to the load, damage to the tested source or inconvenience when connecting the tested source.

List of expected error states:

1) The power element is overloaded with power for a long time

2) The power element is impulsively overloaded

3) The load cannot reach the required current

The solution to these error conditions is as follows (the solution numbers correspond to the numbers error states):

1) Overheating of the power element can be prevented by measuring the temperature of the power element. The temperature is measured periodically, the maximum continuous power is set according to the Linear Derating Factor parameter, it decreases with temperature.

2) The load block itself measures the voltage on the power transistor, according to the applied voltage it limits the current flowing through the load so that the maximum power loss is not exceeded at the peak

3) If there is insufficient voltage on the load for its function (<2 V), the load temporarily switches off so that unwanted phenomena do not occur when the source is suddenly connected - impulse overload of the load or source or injury to the operator during connection power source.

These protections are built in at the firmware level, so they can continue to be modified even after device manufacturing. This approach also allows for a significant simplification of the analog part of the block load, which would otherwise have to be equipped with mechanisms for detecting these states and their distinction from the normal operating mode.

3.8 Method of programming, debugging, control and calibration

3.8.1 Programming and debugging

The load is programmed using the SWD interface, for which there is a dedicated connector with the same designation. This is communication using two wires, a reset signal
and a common ground that allows both programming and debugging and correct checking
program activities.

3.8.2 Load block control

Load control takes place digitally via the SPI interface. It runs through a digital isolator,
by which the user part of the device is galvanically separated from the power part. Optionally, differential communication can also be used for communication over longer distances (up to hundreds of meters depending on the unit's communication speed). In the case of using differential communication, the conductors of the UTP type supply cable are plugged directly into the circuit board. There are also flats on the printed circuit board for connecting a two-wire power cable. Otherwise, differential transceivers are not fitted and a PSH-type connector is fitted, which connects to the control unit with a short six-wire flat cable that provides both communication and power. The cable is terminated at both ends with a PFH type connector, which includes a lock, so it cannot be inserted incorrectly or disconnected accidentally.

Each module has its own /SS signal assigned, so it is possible to identify them, find out which modules are connected, configure them separately and read data from them. Due to the requirements placed on their configuration, a very simple communication protocol is implemented. The control unit can send only 2 types of command: current setting and power setting. Sending this command will automatically reconfigure the load block to the desired mode and value. Communication via a sixteen-bit SPI interface is used.

The highest bit tells the load block what mode to set it to. If MSB is 0, the load is set to constant current mode. If MSB is equal to 1, the load is set to constant power mode. The remaining 15 bits can contain a value of 0 - 32767. If a value of 0 is sent, it sets the load to zero current/power and uses the integrator reset circuit to force the load current to zero. This is due to the offset of the control loop, which can cause the DAC to still load when the DAC has zero voltage at its output.

a small current flows (on the order of tens of mA at the most, i.e. approx. 0.1% of the maximum value). If it is sent a different value, the load will be set to the desired value according to the calibration data.
The current is sent in mA units, so the maximum current through one load block is 32.767 A.
Power is sent in tens of mW, the largest possible adjustable power for one load block
it is therefore 327.67 W.

An almost identical format is used for feedback. The lower 15 bits contain
information about the currently measured value of current / input in the corresponding units.
However, the highest bit does not contain information about the current mode, but signals an error.
0 in the highest bit indicates an error condition or the absence of the module (pull-down is installed on the control board), 1 indicates correct function.

3.8.3 Load block calibration

Calibration is solved using calibration constants stored in the FLASH memory
microcontroller. The STM32 family of microcontrollers usually does not contain EEPROM memory
[29], FLASH memory is used instead, which can also be rewritten using a recorded program
in the microcontroller.

Calibration takes place using a linear approximation. Using the debug interface in the IDE
Keil ÿVision is set by the DAC code word. The code word is set from 0 to 1000 in steps of 50 (21 samples), i.e.
roughly 1/4 of the range, which should correspond to

8 A.

approximately From this number of samples, the coefficients a1 and a0 of the linear function can be precisely determined . According to the measured results, the dependence of the flowing current on the code word is truly linear. These constants can be obtained by linear regression using any spreadsheet or math software (Excel, LibreOffice Calc, Matlab, Maple, etc.). Thus, the calibration terms for
equation

$$I(x) \text{ and } y_0 y \text{ and } 1 \qquad (6.8.1)$$

where a1 is the conversion slope and a0 is the offset of the zero current. If a0 is positive, then it is theoretically not possible to directly achieve zero load current. For this case it is used
an integrator reset circuit to ensure that the power element is in the closed state.
Considering
to the fact that the term a0 should have a size of at most tens of mA, it should not be too large in practice defect. Thus, the DAC codeword is set using this relationship:

$$x \; {}^{y} \; \frac{And\ a_{0}}{and_{1}} \qquad (6.8.2)$$

3.8.4 Implementation of the code word calculation on the microcontroller

Since this calculation could be on a processor without math
coprocessor for division and floating-line operations is slow, a calculation adjustment is applied.

$$x \quad \frac{\text{And ad}}{131072} \qquad (6.8.3)$$

We define the newly formed terms a0' and a1' as follows:

$$\frac{131072}{} \qquad (6.8.4)$$

The purpose of this adjustment is to speed up the calculation. Although the STM32F030F4P microcontroller
it does not have a math coprocessor, but it can multiply two in one cycle
32-bit numbers. By using variables of type 32-bit integer, division can be simulated
by multiplying the rescaled inverse value. The constant 131072 is used because it corresponds to a bit
shift of 17 bits, so there is no need to use division at all, just a bit shift of the result by 17 bits to the right.
Given that the result of the calculation will be an integer in the range 0 - 4096, and that the last operation
in the calculation is a shift of 17 bits to the right, it had
the resulting value would be sufficiently accurate.

It would be possible to increase the precision of the calculation by using 64-bit type variables
integer, while larger scaling constants would be used in the formula for calculating the code word, but even
with the mentioned calculation for the measured piece of the load block, the error of such a calculation
comes
out to be -0.0016%. Refinement of the calculation would therefore have little or no effect on the load
function, as this error will only be reflected at the upper limit of the possible adjustable current, where at 32
A the error will be approximately 0.3 mA. Such an error is practically immeasurable and is significantly
smaller than the errors caused by the imperfection of the analog part of the load block.

4.1 Control and user control block

The purpose of the control and user control block is to set load parameters using the user interface, communication and control of individual load modules and indication of error states. The user interface consists of a four-digit, seven-segment display,
sixteen-key keyboard and indicator diodes.

There are 16 buttons on the keyboard, they are marked with numbers 0 - 9, *, #, A - D. Numbers 0-9 are intended for setting the current or input power. Entering a number is confirmed with an asterisk, entering a number is canceled with a cross. Button A selects constant current mode, button B selects constant power mode. The load is switched off with button C, the load is switched on with button D.
If the load is switched on, it is not possible to switch between constant current and constant power mode. If a numerical value is being entered, the load cannot be switched on
nor change its mode, only turn it off or deselect a value. This simplified description is better described in the following two diagrams.

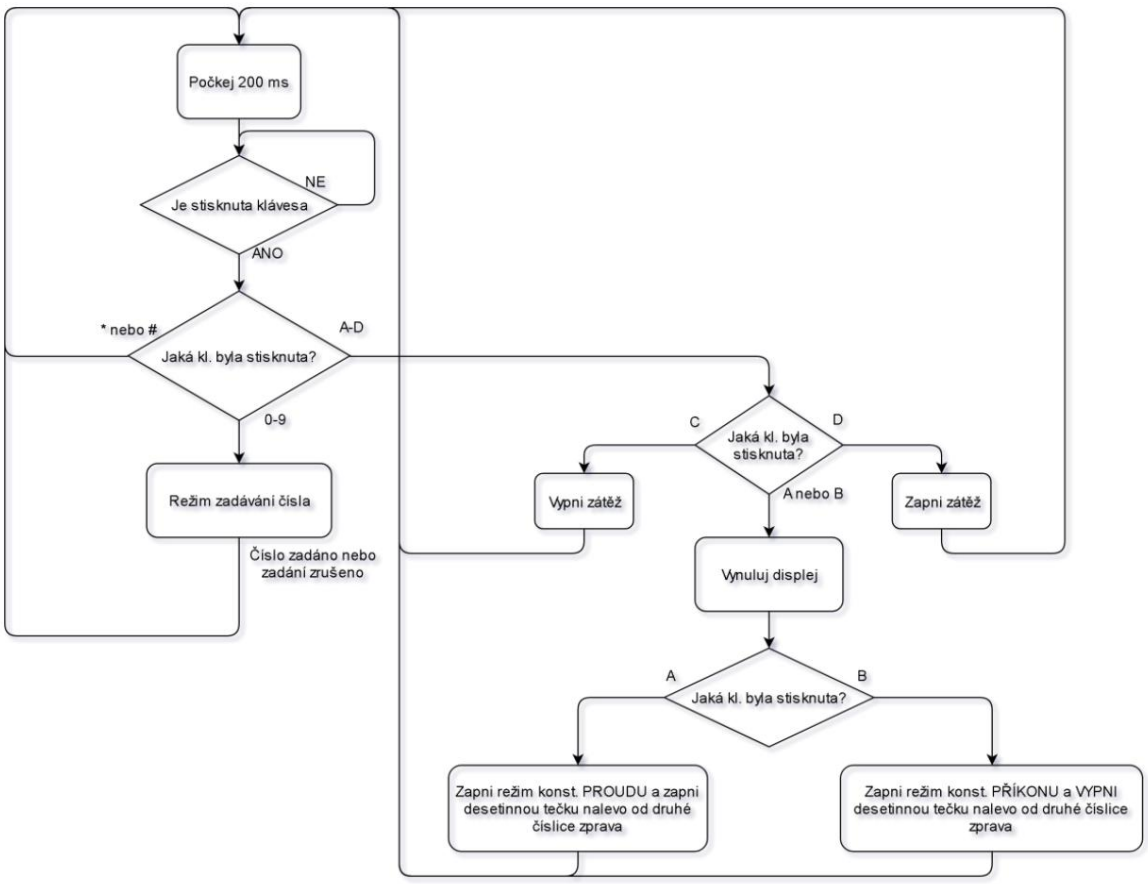


Figure 4.1: Command entry function diagram

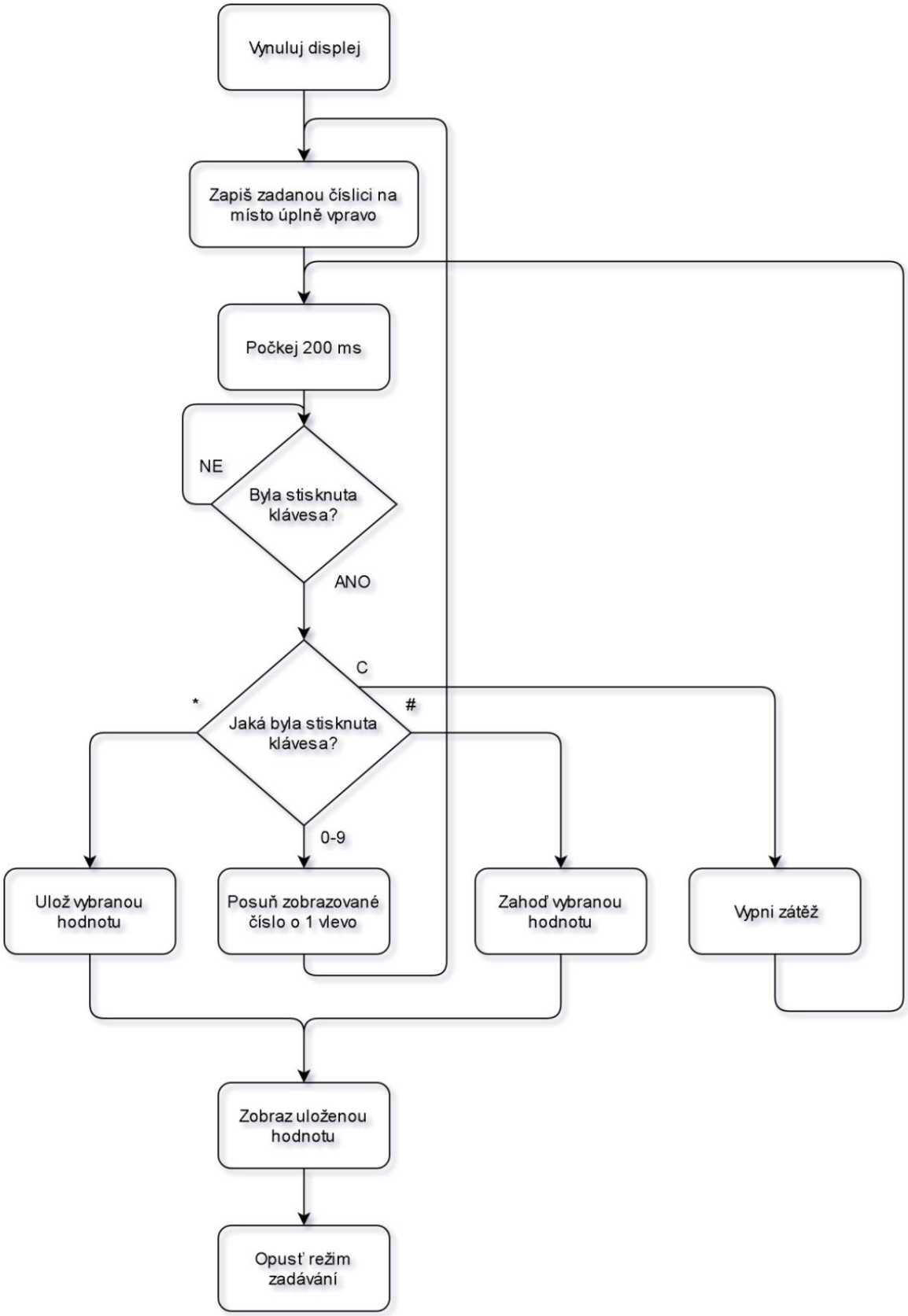


Figure 4.2: Value Entry Mode Diagram

4.2 Wiring and construction of the control block

The control block was again created in Eagle 7.2.0 software. Its wiring includes five seven-segment displays, their auxiliary electronics, a converter from 12 V to 3.4 V for processor and display power supply, STM32F10C8T processor and connectors for keyboard and indicator LED.

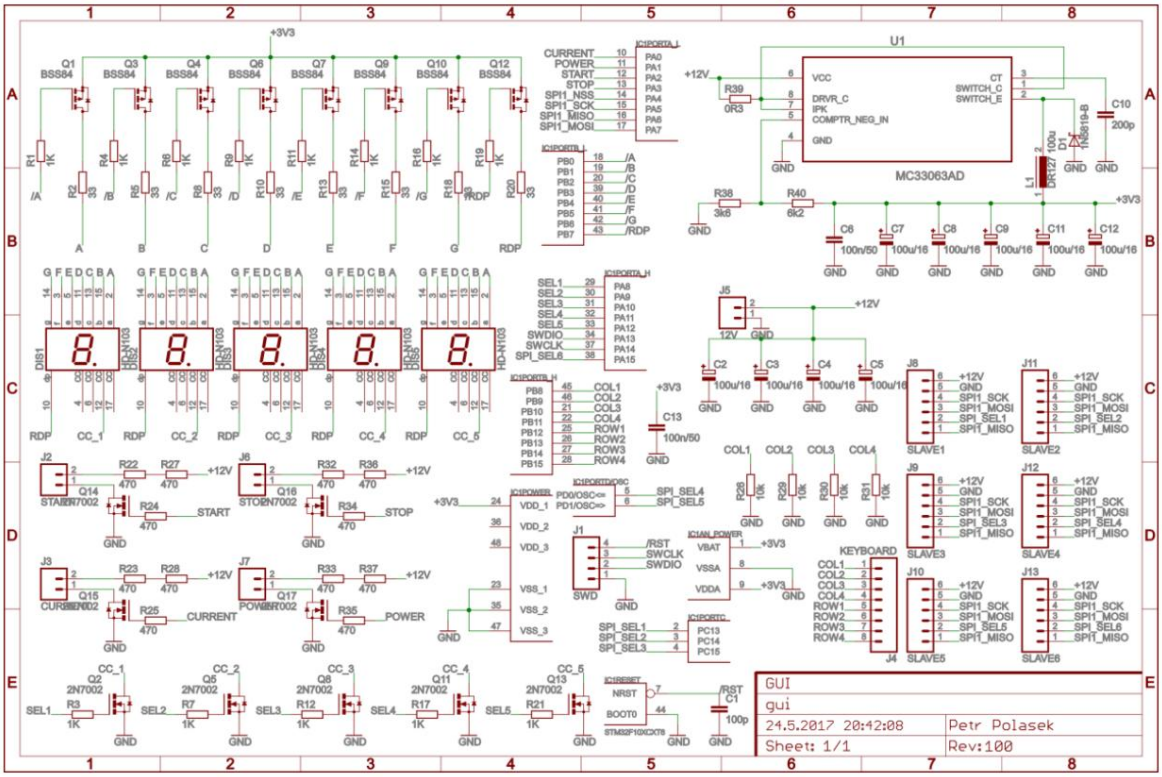


Figure 4.3: Connection of the control block

The processor used is again an STM32 series processor from ST Microelectronics. It was used to simplify the wiring, as it has 36 GPIOs, which made it unnecessary to use either shift registers or multiplexing to use multiple functions on one port. This processor is again a thirty-two-bit ARM, this time Cortex M3.

The keyboard used is of the 4x4 type, therefore it requires 8 wires, the display requires 8 wires to display the character and 5 wires to select the position. For the SPI interface, 3 wires are used for data and 6 for device block selection. 4 wires are used for the indicators, another 2 for the debugging and programming interface. So all 36 GPIOs were used.

The load blocks are powered and controlled from the control block. The control block is powered by the power source listed in 5.1. Since this block's PCB pattern design is made specifically for the box used in this device, it is not shown as an image. However, it is included as a project for Eagle.

5.1 Power supply

No great demands are placed on the power supply. A 12 V, max. 120 mA source is needed to power the load blocks. About 450 mA is needed for used fans. A maximum of 200 mA is required for the control and user control block. Therefore, the Meanwell RS-15-12 [34] source was chosen, which provides a maximum current of 2.1 A at 12 V. With the current configuration of the device, this source is sufficient.

The source is switched by a rocker switch on the front panel, which disconnects it from the mains voltage.

6.1 Mechanical construction of the load

Cell burden Yippee built in to tin boxes type U-KK12-30221 measuring 302mm x 124mm x 217mm. Control and indicator elements are fitted in the holes created in the box. The box is isolated from the mains voltage and from tested resource.

For cooling the load, forced air cooling is used using three pieces of 80 mm of fans attached to the CHL32A type cooler, for which the manufacturer defines the thermal resistance 1.3 K/W when cooling by unforced convection [35]. With forced cooling, this resistance should be several times smaller. However, the cooling is not ideal as the cooler is located inside the box machines. The box does have holes, but they don't seem quite enough for this one type of cooling.

The original intention was to use water cooling, which would be implemented using open circuit. Inside the device, the through vessel was to be made of 4 pieces of flat copper rod measuring 40 x 5 mm, which would be bolted together in the shape of a cuboid. The seams should have been soldered to make them perfectly tight. They should have been at the ends of this hollow block 2 smaller rectangles as the remaining walls of the block to seal it. They should have been drilled in them holes for screwing, to which two hoses were to be connected, one inlet, the other outlet. The circuit was to be implemented in such a way that cold water would flow from the water supply through one hose, and it would flow directly into the waste via the other hose, because the resulting heat would cause the water to burn on the first pass it heated up so much that it could not be cooled down to the required temperature quickly enough. Unfortunately it does however, it showed that such a construction would be very demanding. Copper rods can only be bought in larger quantities, usually a four-meter rod is the basic unit. A large purchase price is also related to this. The problem is also the soldering of such a massive structure and ensuring tightness.

Another problem is that transistors at such power losses are not possible galvanically isolate from the cooler, and thus also the water that circulates in it. So the device could be

dangerous for the user if he were to test a source not isolated from the mains voltage because could result in electric shock.

The load is fully functional, it can be operated at specified voltages and currents, of course continuous power is limited to roughly 150 W. For use at higher powers it would be necessary mentioned water cooling. It is practically impossible to cool a power greater than 1 kW with air, because such powers already require the use of massive coolers weighing close to 10 kilograms, even when forced cooling is used. Such coolers are not manufactured as standard, they are manufactured only at the customer's request. Considering that these are small production pieces about large dimensions, such coolers are very expensive.

So the conclusion is that if the load were to be able to load the sources with a current of 40 A to a voltage of 100 V, it would be necessary to get rid of 4 kW of waste heat, which can only be achieved by cooling with single-flow water.

A photo of the mechanical design of the entire device can be found in Figure 6.1.

Figure 6.1: Mechanical construction of the whole device

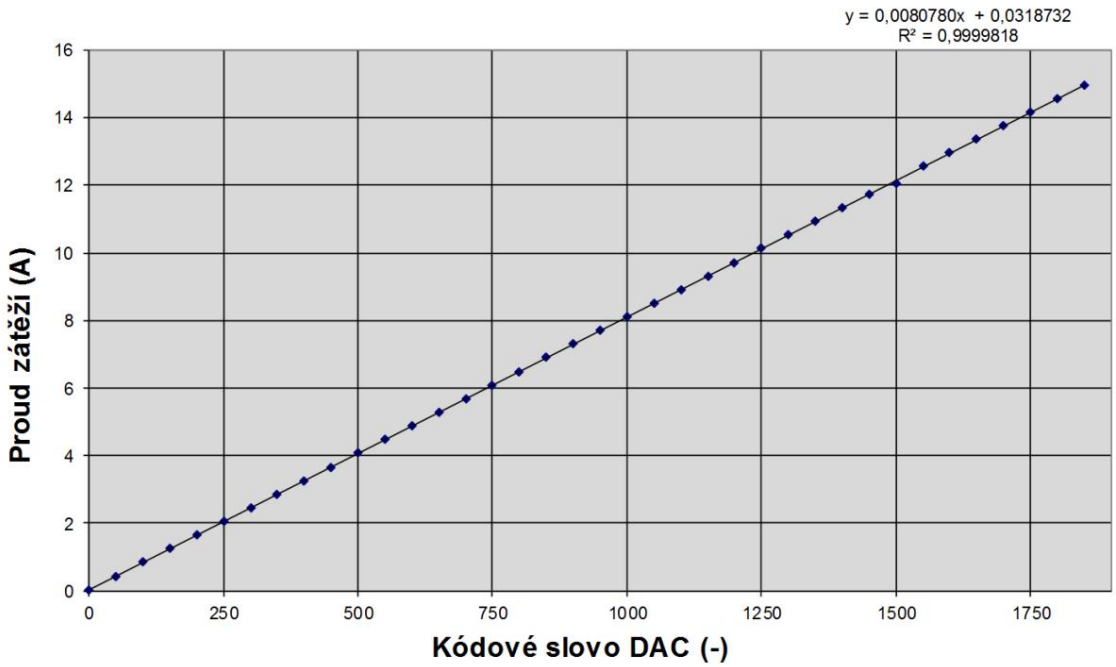
The entire device is installed in a tin box that is grounded for safety user. Due to the used isolated sources and digital isolators it is possible safely measure sources floating with respect to mains ground up to a voltage of 800 V.

7.1 Measured properties of the manufactured load block

The measured parameters of this load are located in this section. These are parameters describing the ability of the load to maintain the set current when the voltage of the loaded source changes, the linearity and offset of the conversion.

7.2 Measurement of load current dependence on DAC code word

The essential information about the quality of the connection is the measurement of the dependence of the load current on the DAC code word. Ideally, it should be a linear dependence without a constant member. In reality, however, this term will be non-zero due to the imperfection of analogs components.



Graph 5: Dependence of the load current on the DAC code word

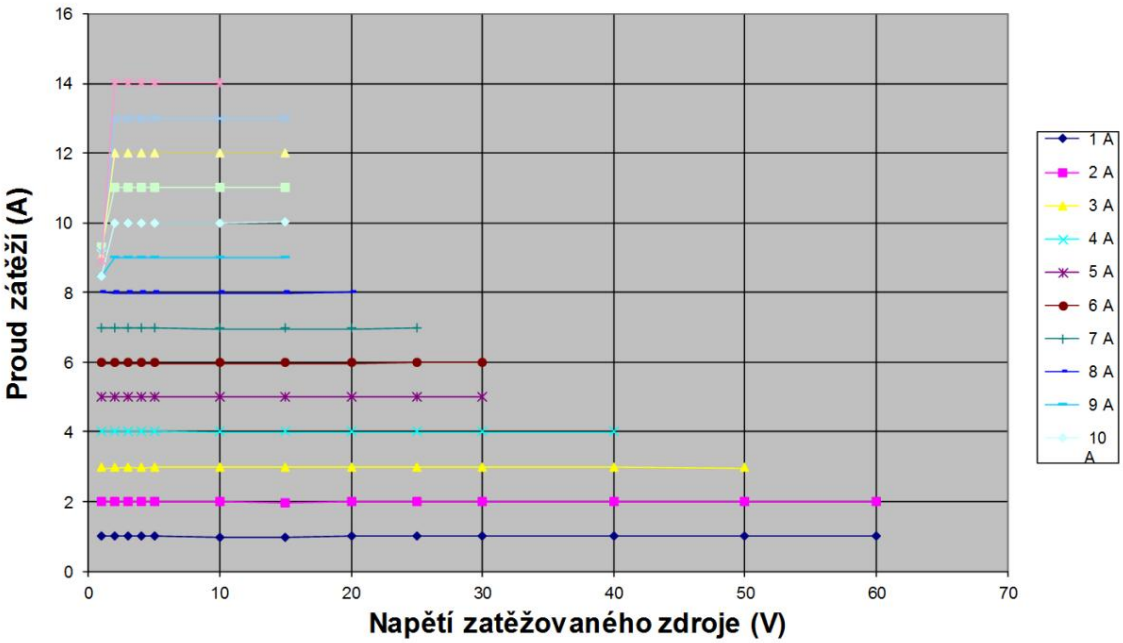
The following information can be found from the measured data: the slope of the transfer is 8.08 mA, the offset is 31.87mA. So if we increase the code word by 1, the current through the load block increases by 8.08 mA.
If we set the DAC codeword to 0, the current of 31.87 mA will still flow through the load.
However, this is not a serious problem - given that the smallest current step is
8.08 mA, it is only at the lower end of the current range that the three steps between 0 mA and 32.32 mA are missing. However, this small defect is completely negligible in practice, if we test sources with currents of tens of A, it does not matter that we cannot set exactly such a small current.

The essential knowledge from this measurement is that the linearity of the conversion is practically perfect (according to the parameter R2 , which compares the measured values with a linear regression). In addition, the load behaves correctly at least up to 15 A, but can be expected to behave this way even at tens of A, given the datasheets of the power MOSFET and the shunt.

The resistance wire shunt turned out to be unusable from currents exceeding 10 A. At such a current, it already heated up to hundreds of degrees, changing its resistance. On with large currents, the steepness of the transfer decreased, which greatly affected the linearity of the transfer. Considering for almost perfect linearity, there is no need to compensate the measurement with respect to temperature in any way shunt. Against resistance wire, which does not cool well, it seems to be an option manganin resistance with the right choice.

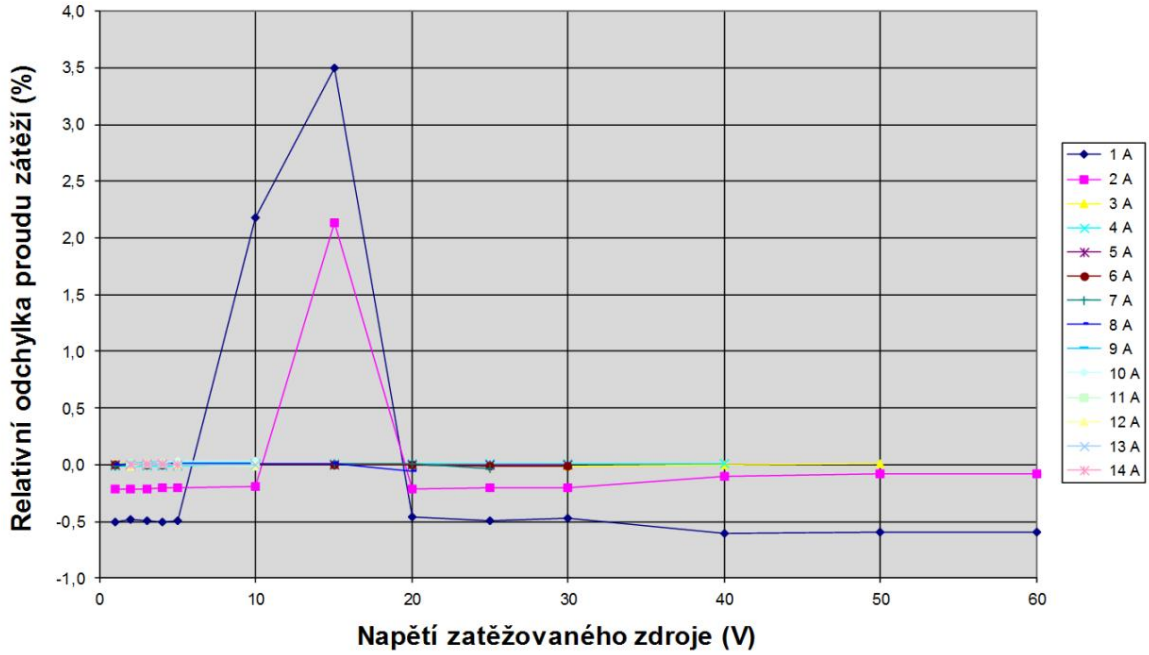
7.3 Measurement of load current dependence on load voltage resources

This measurement involved finding out how the load current changes when the voltage changes loaded resource. The measurement was made for currents of 1 A – 14 A. Depending on the use power source limited to 14 A and 188 W, the measurement could not be performed for the entire working period load range.



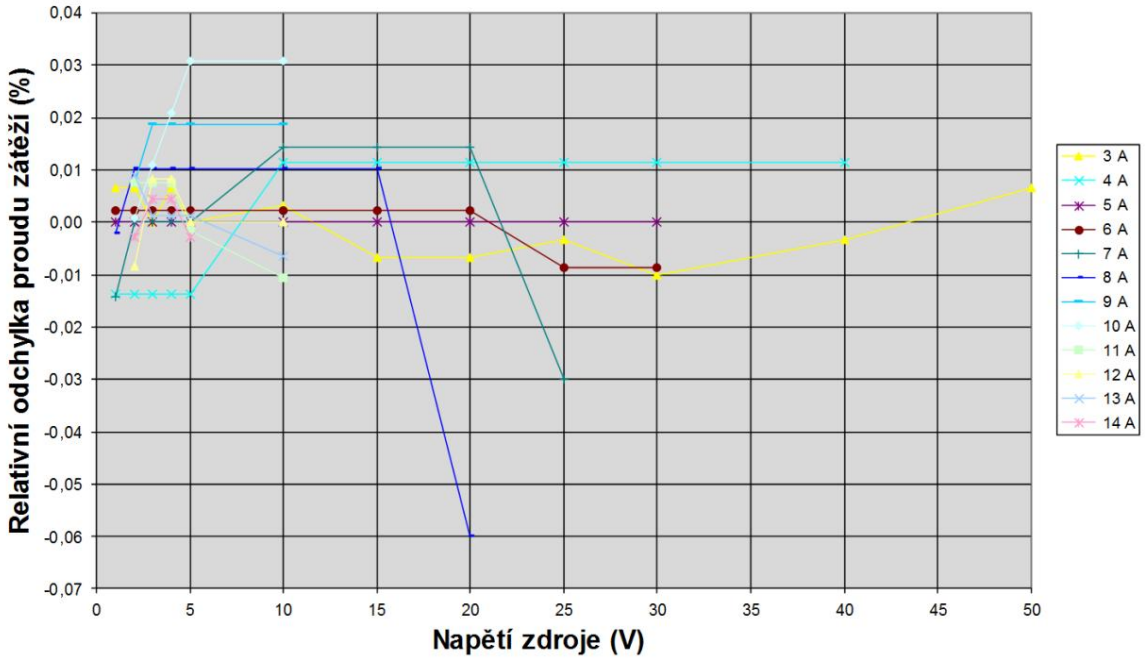
Graph 6: Dependence of the load current on the voltage of the loaded source

Considering the measured results, however, it can be assumed that the rest is also working load area, the load will behave similarly. The relative error is plotted on graph 7 current maintenance when the voltage of the loaded source changes.



Graph 7: Relative deviation of load current depending on source voltage

From graph 7, it is clear that the largest current maintenance error is for currents up to 3 A. The largest deviation occurs at a current of 1 A, where the deviation reaches 3.5%. By measurement with an oscilloscope, however, this deviation is apparently caused by noise at the output of the switching source, which increases significantly at this voltage and current. For currents from 3 A, this graph is plotted again with a different scale as graph 8. The highest deviation reaches -0.06%.

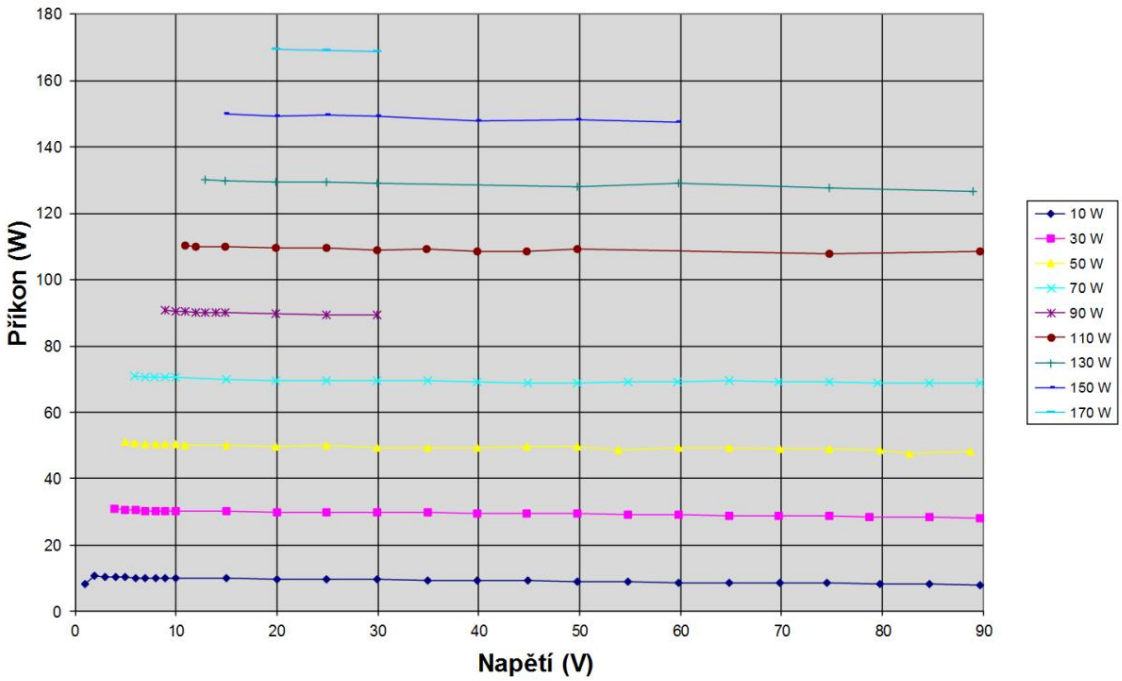


Graph 8: Relative deviation of the current depending on the voltage for currents from 3 A

It can be seen from the measured dependence that the minimum operating voltage of the load is up to a current of 8 A 1 V. For currents up to 14 A, the minimum working voltage is 2 V. For higher currents, it should be of the datasheet for the IRFP260 transistor including the loss on the minimum working shunt increase the voltage to no more than 3 V. This result should be sufficient for testing most sources. An exception can be made only by low-voltage sources with an output voltage less than 5 V.

7.4 Measuring the ability to maintain constant power

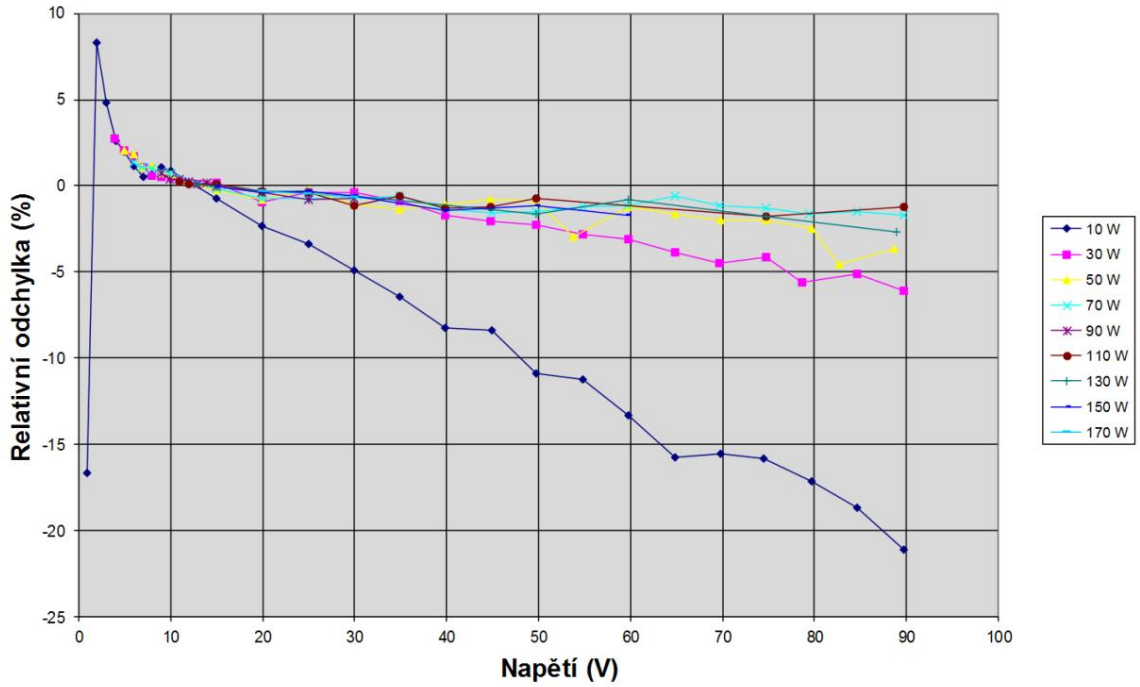
In this measurement, it was about finding out how the load can maintain the power input when the voltage changes loaded resource. One piece of load block was measured.



Graph 9: Dependence of the load input on the voltage of the loaded source

According to graph 9, the constant power mode is also functional, but with less accuracy than the constant power mode. For better visualization, this dependence is also plotted as a relative deviation from the required value (graph 10).

From graph 10, it follows that the relative deviation is dependent on the voltage of the source as well as on the required input power. For low voltages up to 10 V, the predominant factor of error is the inaccuracy of the voltage measurement. For the measured voltage, use the internal DAC of the processor, which is twelve-bit.



Graph 10: Dependence of the relative deviation of power maintenance on the source voltage

For damage resistance, the circuit is designed to measure voltages up to 200 V. The smallest measurable step is thus 48.8 mV, the real measurement results in 50.8 mV, which is determined by the tolerance of the components in the divider. For a voltage greater than 15 V, this component of the deviation ceases to be significant and an error caused by either the impossibility of setting the exact required current or rounding in the calculation (the calculation takes place in whole numbers) begins to manifest itself. The greater the required power, the less this error manifests itself, for an input of 90 W it reaches less than 1%. For a power consumption of 30 W, it reaches a maximum of 6%, for 10 W, 22%. If the load is to be used for small powers, it would be advisable to use a shunt with a higher resistance to limit this error.

7.5 Evaluation of measurement results

One piece of load block was measured. The measurement shows that the load meets the requirements requirements and has the expected properties. The smallest load step is 8.08 mA, the offset is 31.9 mA, or approximately 0.1% of range.

The accuracy of load current maintenance is better than for currents from 3 A in the measured range 0.06%, for smaller currents the highest deviation is 3.5%. Current holding accuracy is pro performances of the order of tens of W better than 1%, in the worst possible case 22%.

Therefore, according to the measured parameters, the load is functional and accurate enough for the purpose resource testing.

With the use of two load modules and a used cooler, it is possible to load sources with a power of up to 560 W peak and approximately 280 W continuously.

7.5.1 Working load area

According to the measured values, it is possible to create an assumed working area of this loads. There are two dependencies, one for short-term load and the other for permanent load. The operating range is limited by the MOSFET's minimum operating voltage for small voltages and power loss and higher voltages.

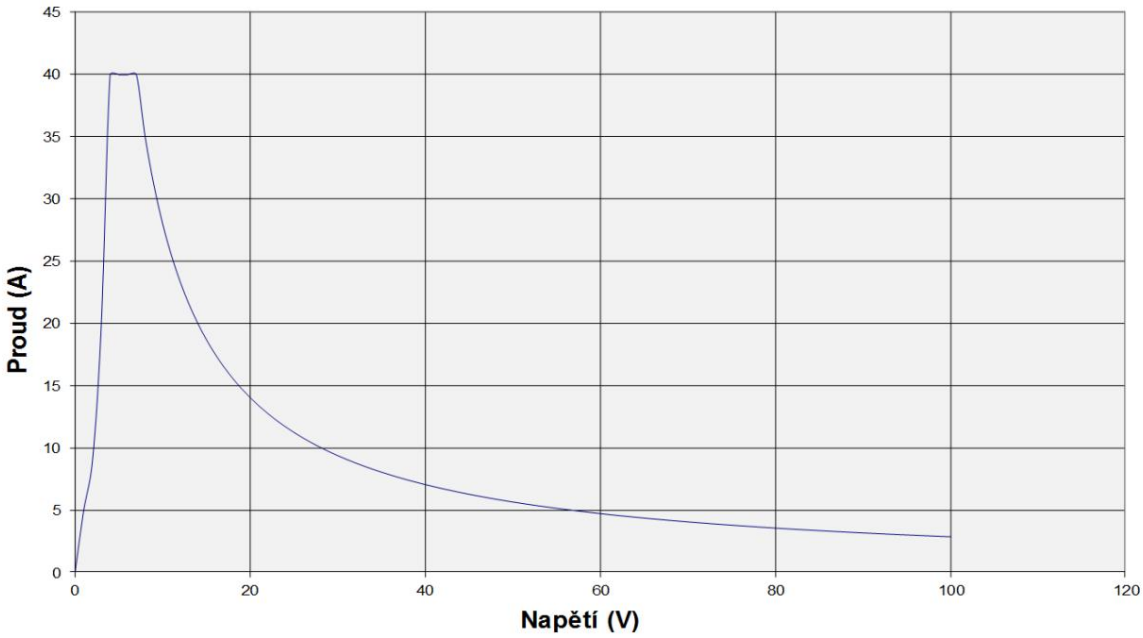


Chart 11: Working load area for continuous load

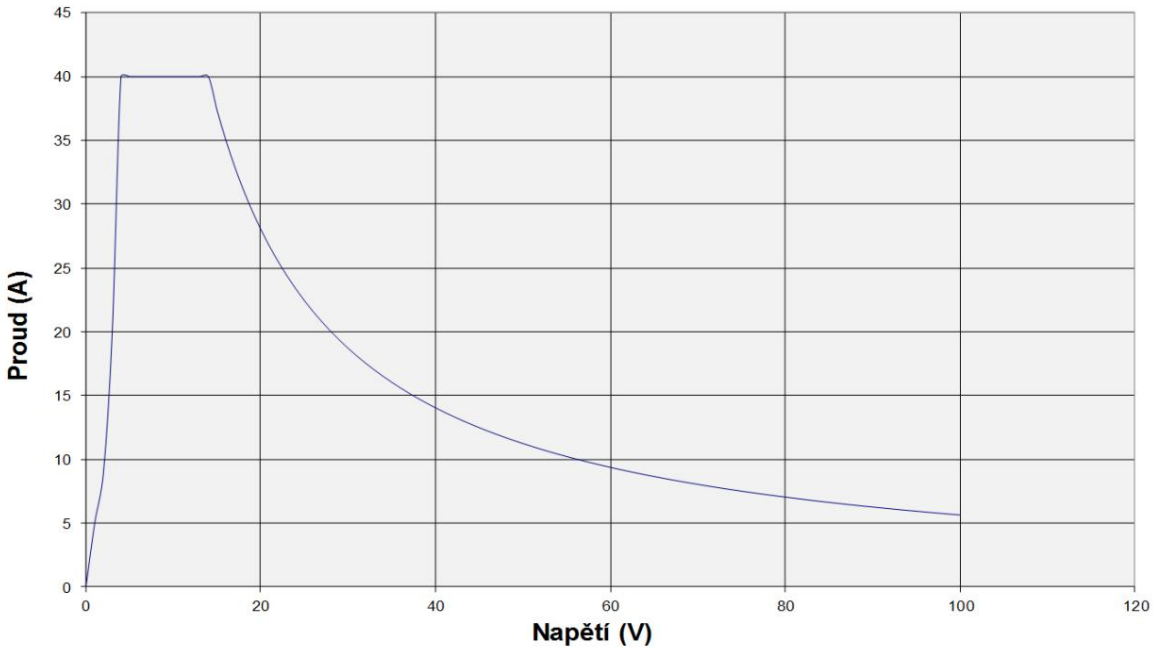


Chart 12: Working load area for peak load

8.1 Conclusion of work results

The designed and manufactured device achieves the required parameters - it is possible to load sources up to a voltage of 100 V and for currents up to 40 A. The permanent permitted power of the load is around 280 W, depending on the ambient temperature. The impulse power reaches approximately 560 W (permitted power loss of two pieces of IRFP260N at 25 °C).

The load can operate in constant current and power modes. In constant current mode, the required current holding accuracy is better than ±0.06% over most of the operating range. In constant power mode, the accuracy of maintaining the required power is better than 5% in most of the working range.

The load includes protections against current overload, peak power and continuous power. The default setting of these protections is suitable for the used IRFP260N power transistor and PBH F1 series shunt. For other power elements used, the device can be easily recalibrated, there is no need to intervene in the connection. Current limitations are 30 A without time limitation due to shunt parameters, 280 W peak power and 150 W continuous power per module due to power transistor cooling options. In the case of a requirement for a continuous power of 280 W per module, it would be necessary to solve the cooling, probably with a water circuit, because such power cannot be sufficiently cooled by forced convection

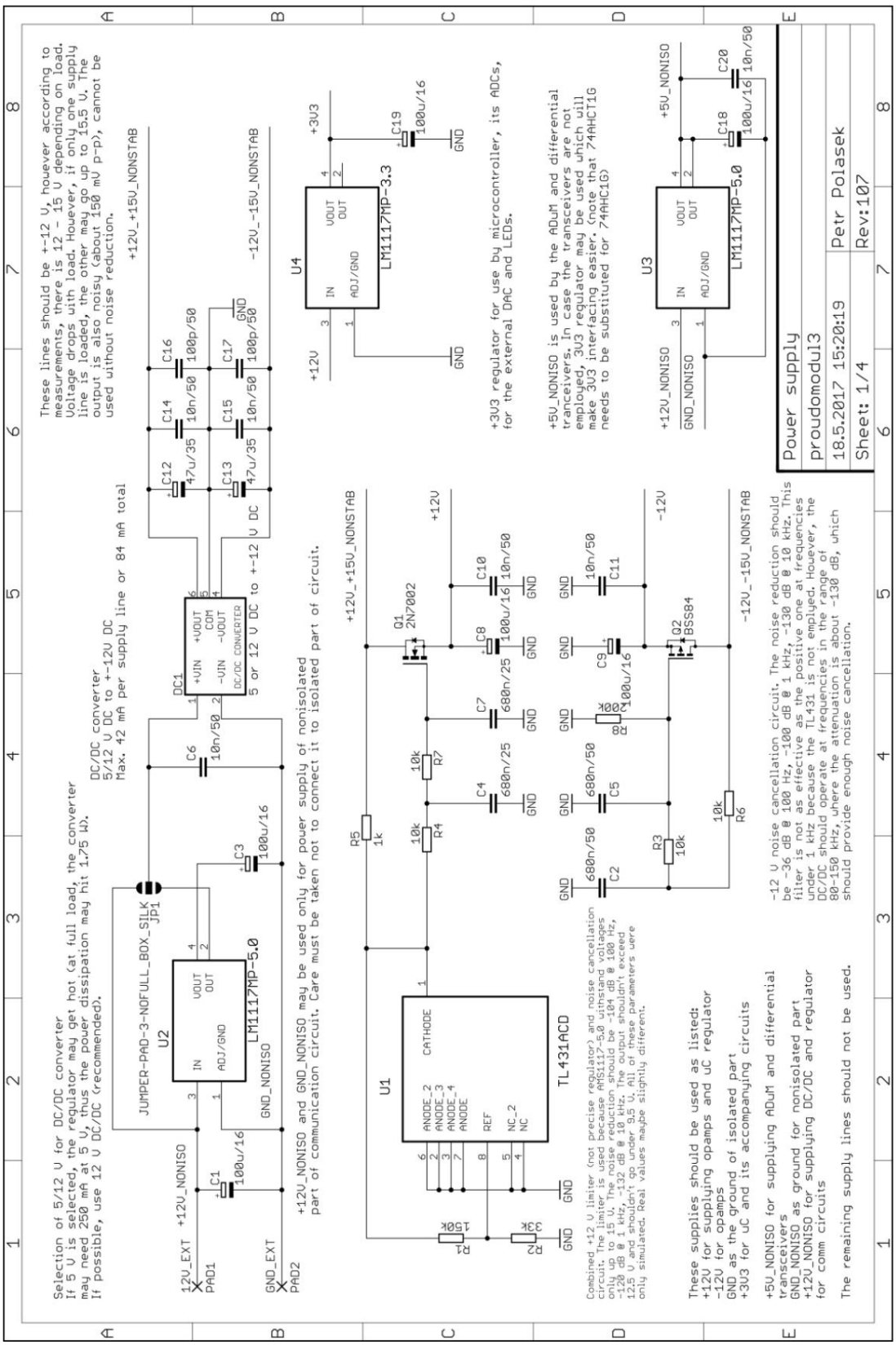
take away.

If a higher achievable current or power is required, the load can be simply expanded using other modules. There is no restriction on the part of the individual load modules of their number connected to the control block.

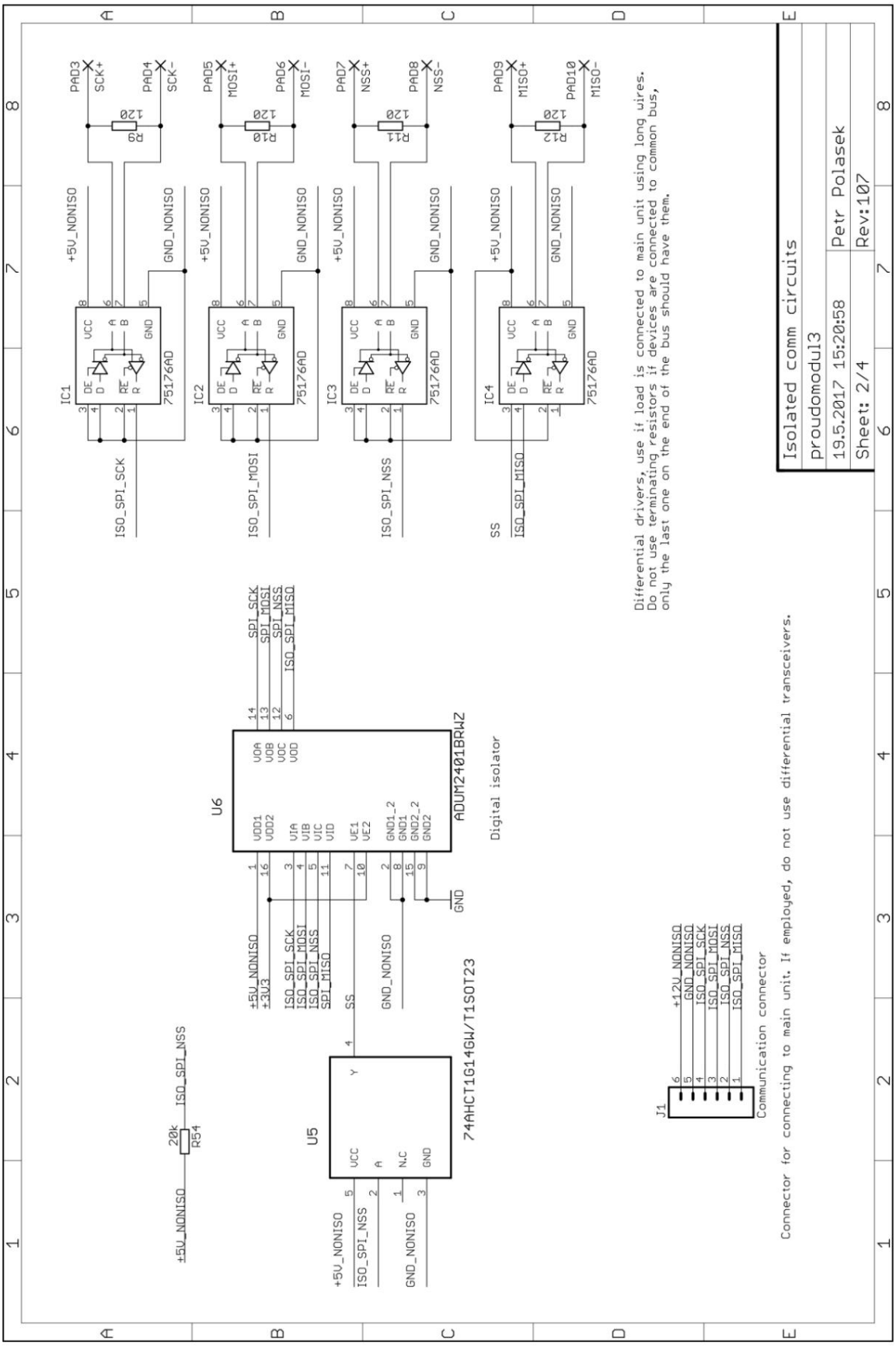
Individual load modules can also be used outside of this integrated device, they can be used for example, to place around a large test device. This allows use differential transmission, which is much more resistant to interference from the environment.

Unfortunately, it was not possible to get the load to be able to load the resources on 100 V and at the same time at 40 A (ie 4 kW). This is because to dissipate such amount of heat is quite difficult. Due to the fact that a load with such power is produced only a few models with a minimum price of CZK 113,000 (as of the date of writing this work) [36], while for smaller performances there is a choice between a several times larger number of models, it is possible to assume that this is indeed a problem that is also faced by companies that manufactures such devices commercially.

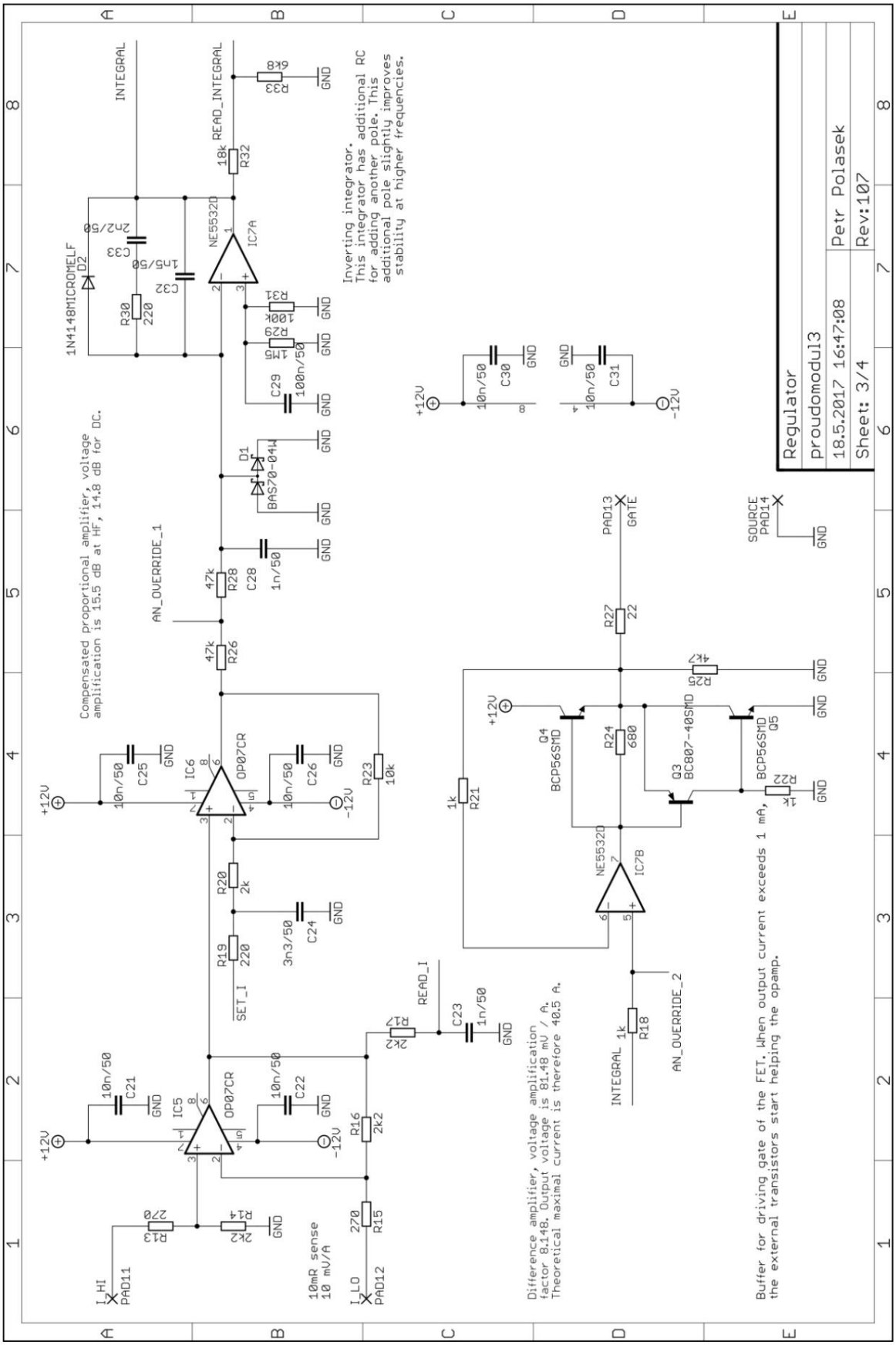
9.1 Attachments



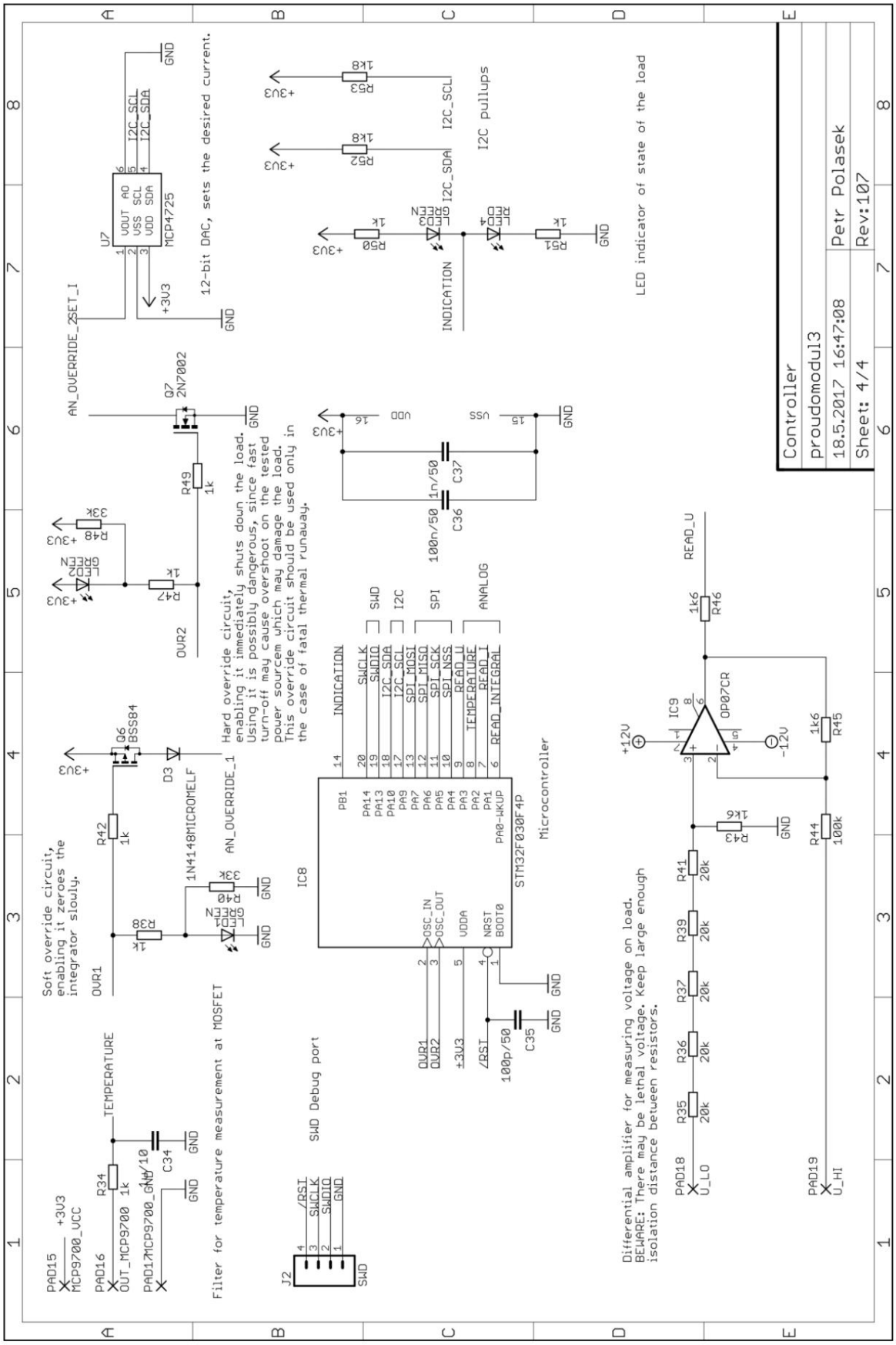
Appendix 1: Schematic of the load block power supply



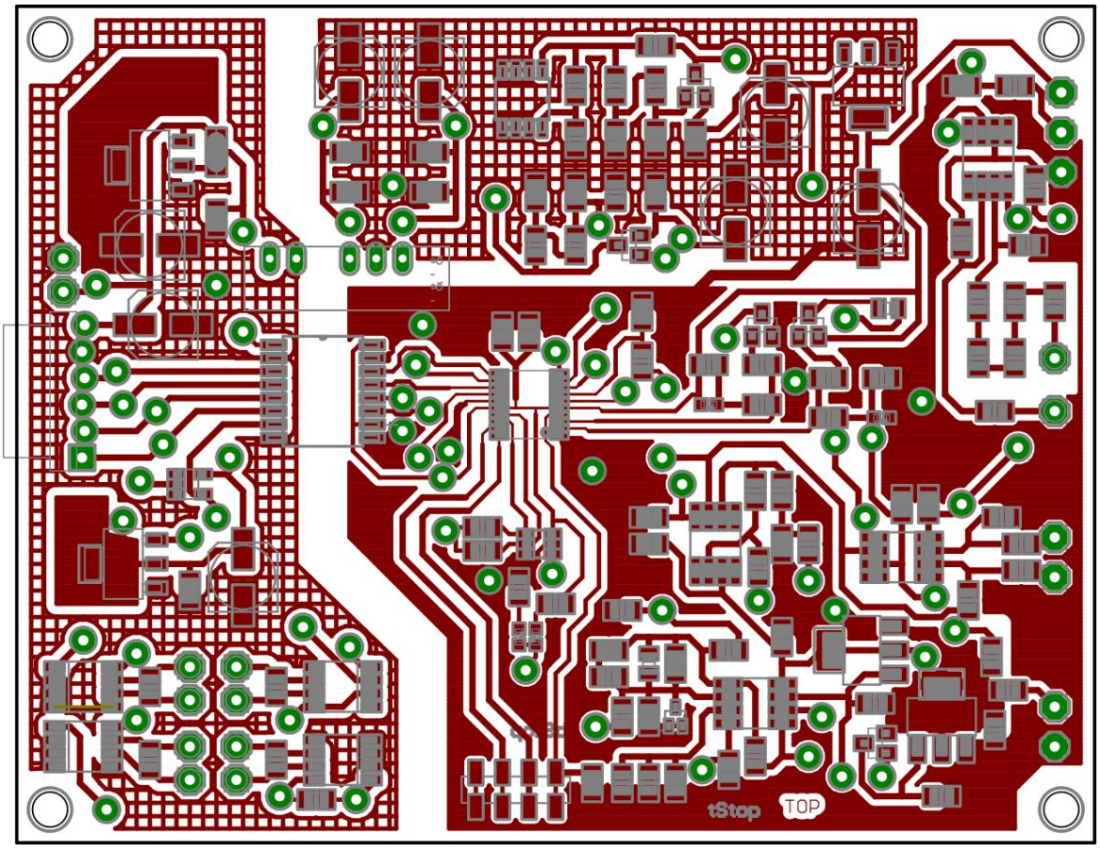
Appendix 2: Diagram of the communication part of the load block



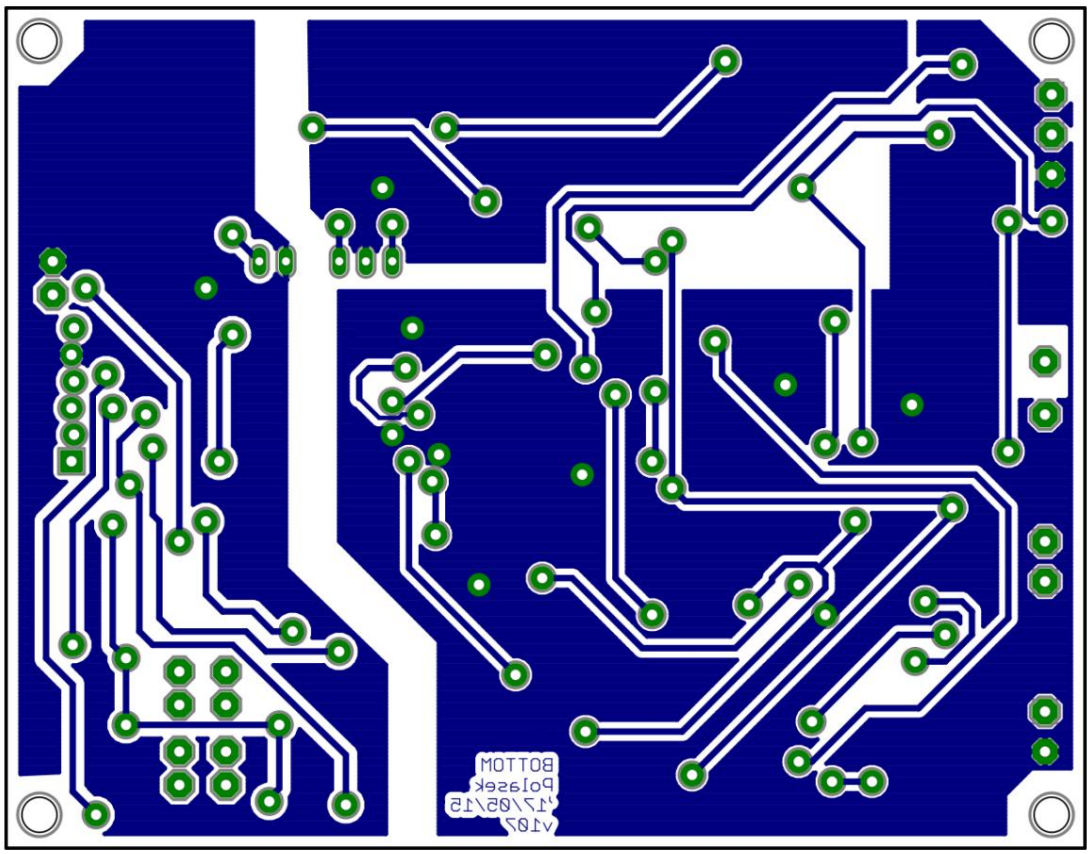
Appendix 3: Connection diagram of the control loop of the load block



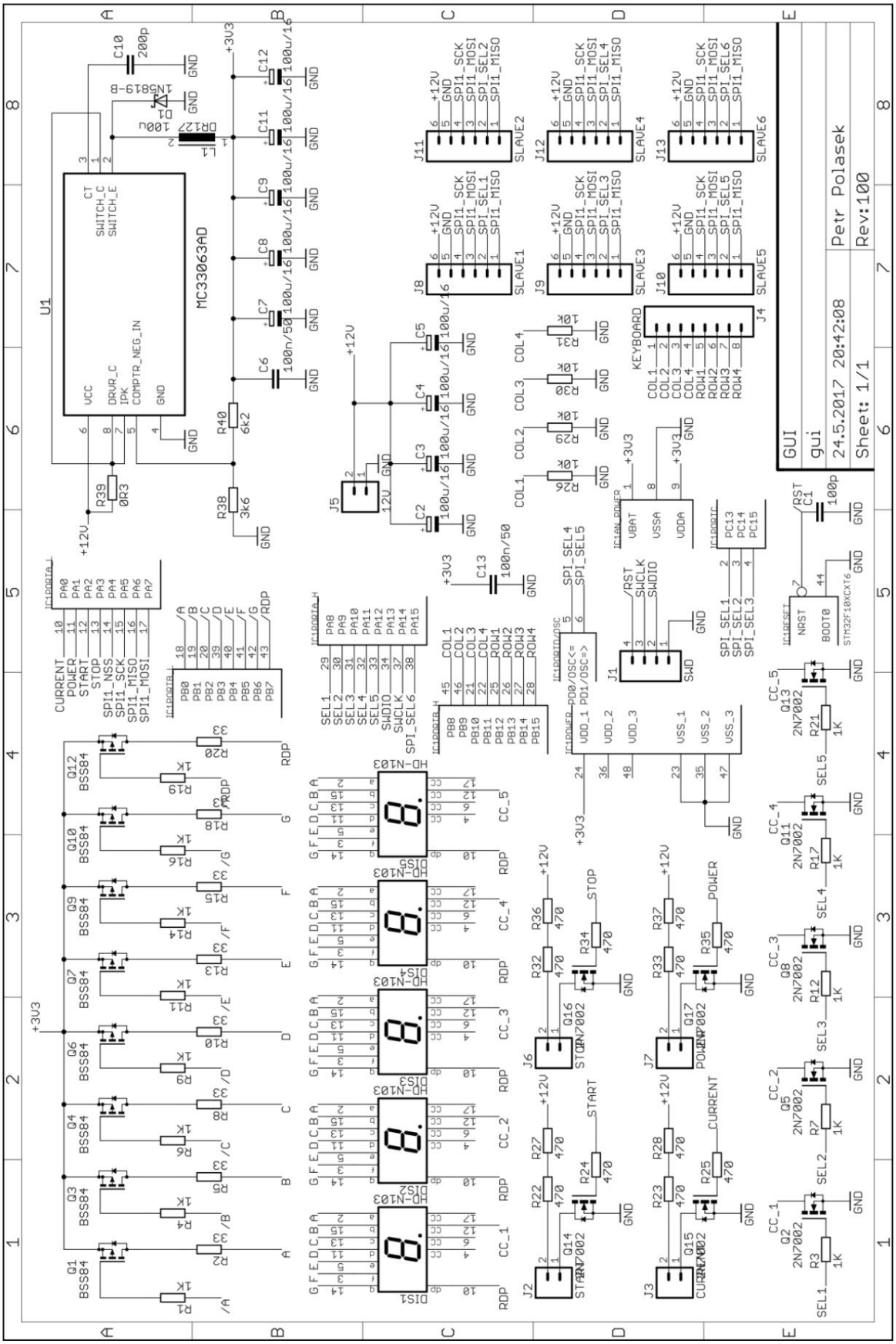
Appendix 4: Circuit diagram of the processor part of the load block



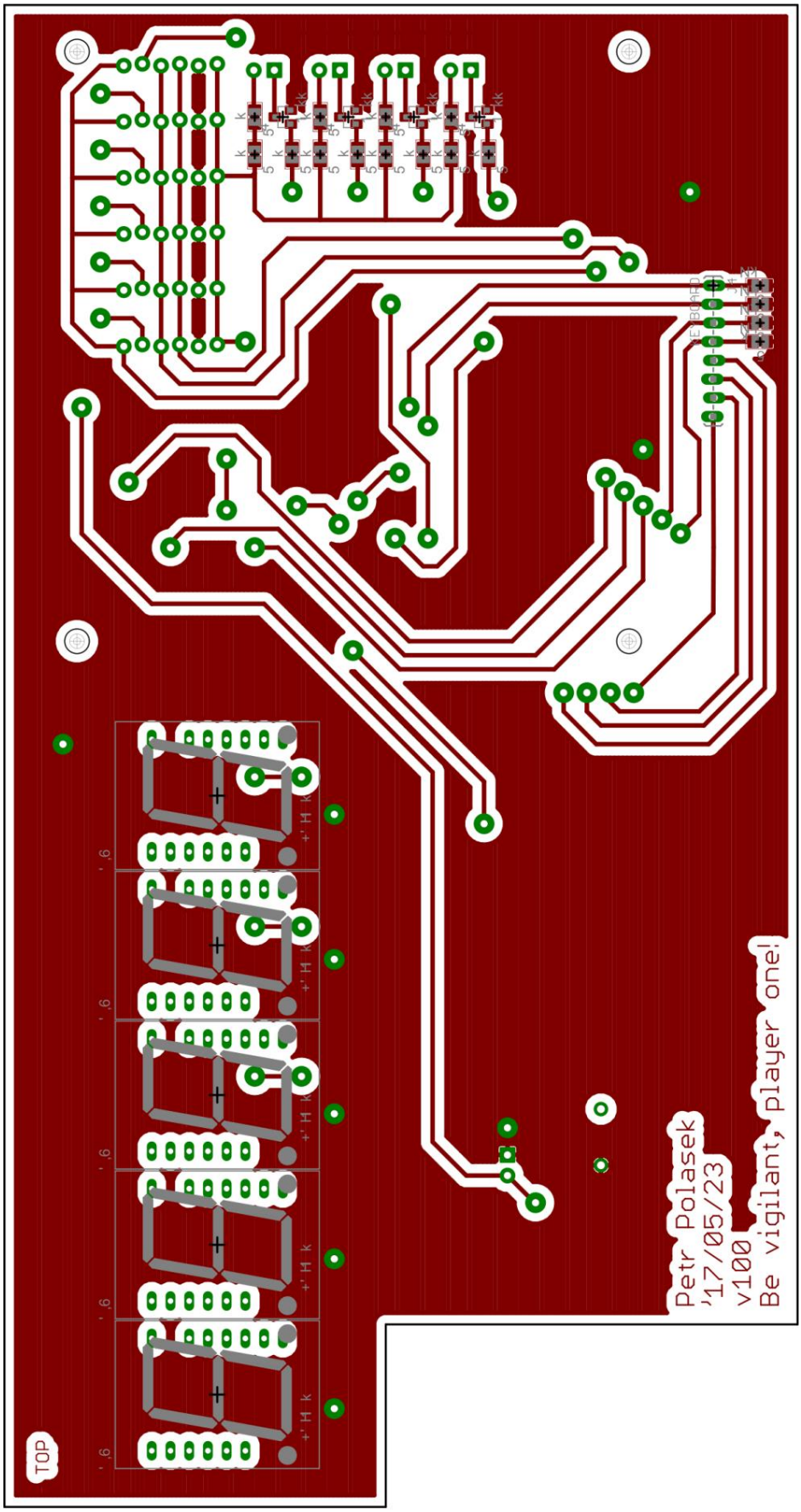
Appendix 5: Layout of the upper layer of the load block



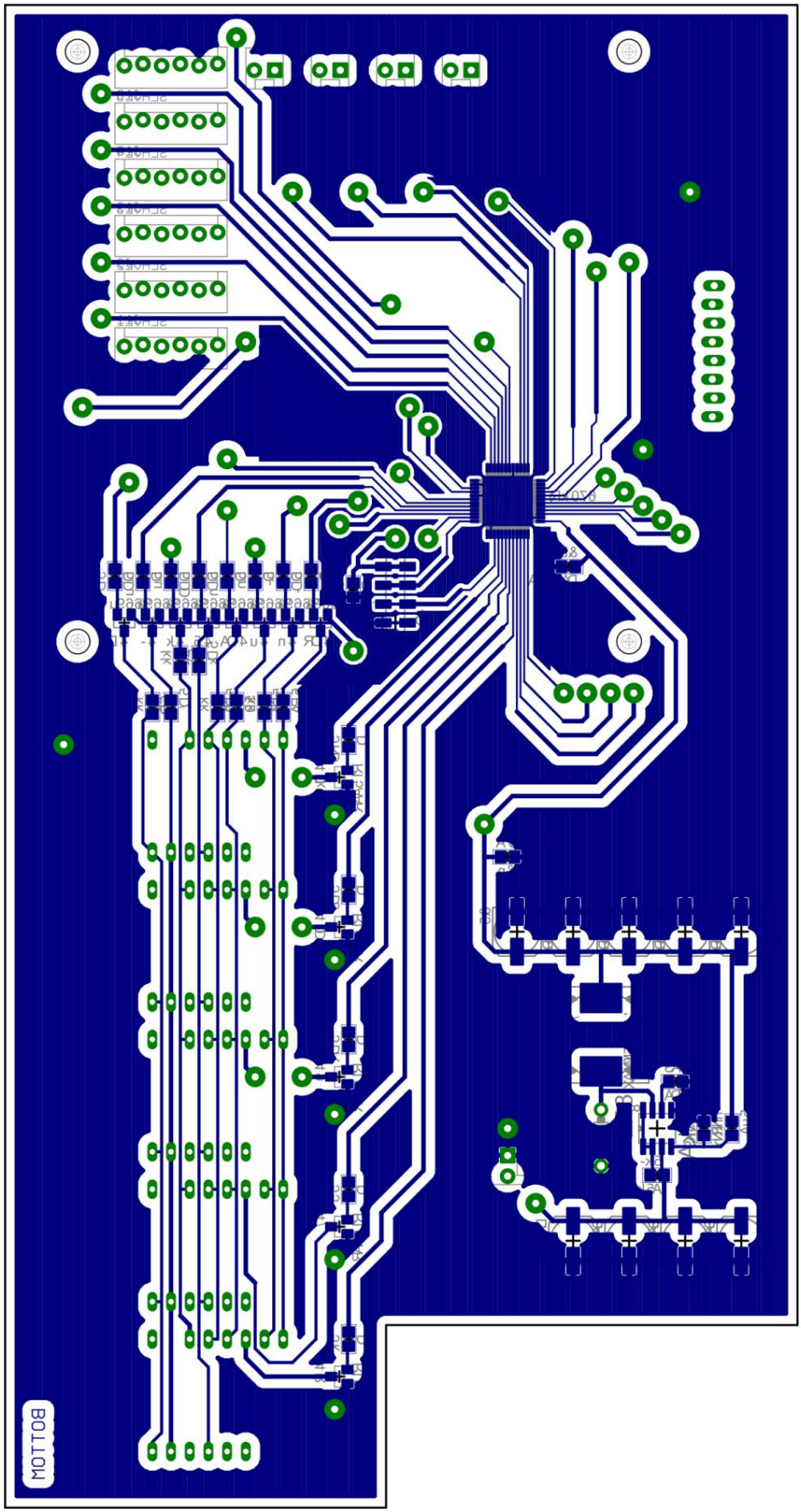
Appendix 6: Layout of the bottom layer of the load block



Appendix 7: Control block diagram



Appendix 8: Layout of the upper layer of the control block



Appendix 9: Layout of the bottom layer of the control block

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13.1 List of attachments on the CD

1) Eagle project load block	module_load_schema_layout.zip
2) Eagle project control block	management_schema_layout.zip
3) ÿVision load block project	modul_zatez_keil_projekt.zip
4) ÿVision control block project	rizeni_keil_projekt.zip
5) Measured current mode data	measured_data_current.xlsx
6) Measured power mode data	measured_data_prikon.xls

14.1 List of used literature

[1] ZEGHBROECK VAN, Bart. *Principles of semiconductor devices, Chapter 7: MOS Field effect transistors* [online]. 2011. Available from: https://ecee.colorado.edu/~bart/book/book/chapter7/ch7_3.htm

[2] WU, Prof. Ming. *EE lecture 5: Bipolar junction Transistor in Saturation* [online]. 2008. Available from: http://www-inst.eecs.berkeley.edu/~ee105/sp08/lectures/lecture5_2.pdf

[3] *Power (sub)systems* [online]. Lecture. February 12, 2015. Craft Wednesdays. Available from: https://www.youtube.com/watch?v=gGv5l_srs7k

[4] *IT8500+ Electronic load datasheet* [online]. Bm: ITECH Electronics. Available from: http://www.itech.sh/Upload/File/20150806110640.pdf

[5] *Current Shunt & Voltage Measurement Reference Design for EV/ HEV Automotive Battery Monitoring* [online]. Bm: Texas Instruments. October 2015. Available from: http://www.ti.com/lit/ug/tidua81/tidua81.pdf

[6] BARKHORDARIAN, Pub. *Power MOSFET Basics* [online]. Bm: International Rectifier. 25 October 2005. Available from: http://www.infineon.com/dgdl/mosfet.pdf?fileId=5546d462533600a4015357444e913f4f

[7] ÅSTRÖM, Karl Johan. *PID Control* [online]. 2002. Available from: https://www.cds.caltech.edu/~murray/courses/cds101/fa02/caltech/astrom-ch6.pdf

[8] *MT-037: Op Amp Input Offset Voltage* [online]. Bm: Analog Devices. October 2008. Available from: http://www.analog.com/media/en/training-seminars/tutorials/MT-037.pdf

[9] *OP07 Datasheet* [online]. Bm: Analog Devices. 11 Jan. 2016. Available from: http://www.analog.com/media/en/technical-documentation/data-sheets/OP07.pdf

[10] *AD708 Datasheet* [online]. Bm: Analog Devices. 2006. Available from: http://www.analog.com/media/en/technical-documentation/data-sheets/AD708.pdf

[11] *NCS333 Datasheet* [online]. Bm: ON Semiconductor. March 2017. Available from: http://www.onsemi.com/pub/Collateral/NCS333-D.PDF

[12] *LT1012 Datasheet* [online]. Bm: Linear Technology. 1991. Available from: http://cds.linear.com/docs/en/datasheet/1012afbs.pdf

[13] *OP27 datasheet* [online]. Bm: Analog Devices. 2016. Available from: http://www.analog.com/media/en/technical-documentation/data-sheets/OP27.pdf

[14] *LTC1050 Datasheet* [online]. Bm: Linear Technology. 23 September 2002. Available from: http://cds.linear.com/docs/en/datasheet/1050fb.pdf

[15] ZEGHBROECK VAN, Bart. *Principles of Semiconductor Devices, Chapter 2: Semiconductor Fundamentals* [online]. 2011. Available from: https://ecee.colorado.edu/~bart/book/book/chapter2/ch2_7.htm

[16] Darlington Transistors. *Darlington Transistors* [online]. 2015. Available from: http://www.electronics-tutorials.ws/transistor/darlington-transistor.html

[17] LAKER, Kenneth R. *Early Effect & BJT Biasing* [online]. Bm: University of Pennsylvania. 11 September 2008. Available from: http://www.seas.upenn.edu/~ese319/Lecture_Notes/Lec_4_BJTBias1_08.pdf

[18] *IRFP260N Datasheet* [online]. Bm: International Rectifier. October 8, 2004. Available from: http://www.infineon.com/dgdl/irfp260n.pdf?fileId=5546d462533600a4015356289dcf1fe 2

[19] PECHT, Michael. *The influence of temperature on microelectronic device failure mechanisms* [online]. Bm: Ramsearch Company. 4 September 1993. Available from: http://www.dtic.mil/dtic/tr/fulltext/u2/a275029.pdf

[20] *Sensing Elements for Current Measurements* [online]. Bm: Intersil. 2014. Available of:
http://www.intersil.com/content/dam/Intersil/whitepapers/amplifiers/current-sense measurements.pdf

[21] KLEVENS, Jay. *Calibrating DC Current Shunts: Techniques and Uncertainties* [online]. Bm: Ohm-Labs. 2011. Available from: http://ohm-lab.com/pdfs/Shunt%20Calibration.pdf

[22] VISHAY PRECISION GROUP. *TN-108: Non-Linearity of Resistance/ Temperature Characteristic: Its Influence on Performance of Precision Resistors* [online]. Bm: Vishay Precision Group. 2 July 2013. Available from: http:// www.vishaypg.com/docs/60108/VFR_TN108.pdf

[23] HYPERPHYSICS. *Resistivity and Temperature Coefficient at 20 C* [online]. Available of:
http://hyperphysics.phy-astr.gsu.edu/hbase/Tables/rstiv.html

[24] *Manganin Datasheet* [online]. Bm: Isabellenhütte Heusler GmbH & Co. KG. 29 March 2014. Available from:
http://www.isabellenhuette.de/uploads/media/MANGANIN_02.pdf

[25] *PBH F1 Manganin precision resistors* [online]. Bm: Isabellenhütte Heusler GmbH & What. KG. 6 April 2012. Available
from: http://www.isotekcorp.com/sites/default/files/sites/default/files/pdfs/PBH.pdf

[26] Rasmussen, Angela. *Introduction to Bode Plot* [online]. Bm: ECE Utah. 2005. Available from: http://www.ece.utah.edu/~ee3110/bodeplot.pdf

[27] *A1212S Datasheet* [online]. Bm: Mornsun Guangzhou Science & Technology Co., Ltd. March 3, 2014. Available from:
https://www.ecom.cz/open_sheet/sheet_name=D29296

[28] *AM1D-0512DZ Datasheet* [online]. Bm: aimtec. 1 Apr 2016. Available from: http://www.aimtec.com/site/Aimtec/files/Datasheet/HighResolution/AM1D-Z.pdf

[29] *STM32F030F4P6 Datasheet* [online]. Bm: ST Microelectronics. 2017. Available from: http://www.st.com/content/ccc/resource/technical/document/datasheet/a4/5d/0b/0e/87/ c4/4d/71/DM00088500.pdf/files/DM00088500.pdf/jcr: content/translations/en.DM00088 500.pdf

[30] *STM32F030F4P Reference Manual* [online]. Bm: ST Microelectronics. April 2017. Available
from: http://www.st.com/content/ccc/resource/technical/document/reference_manual/cf/ 10/a8/c4/29/fb/4c/42/DM00091010.pdf/files/DM00091010. pdf/jcr:content/translations/ en.D M00091010.pdf

[31] *MCP4725 Datasheet* [online]. Bm: Microchip. 2007. Available from: https://www.sparkfun.com/datasheets/BreakoutBoards/MCP4725.pdf

[32] *ADuM2401 Datasheet* [online]. Bm: Analog Devices. 2015. Available from: http://www.analog.com/media/en/technical-documentation/data sheets/ADuM2400_2401_2402.pdf

[33] *SN75176A Differential Bus Transceiver Datasheet* [online]. Bm: Texas Instruments. January 2015. Available from: http://www.ti.com/lit/ds/symlink/sn75176a.pdf

[34] *RS-15 Power Supply Series Datasheet* [online]. Bm: Meanwell. September 7, 2010. Available from: https://www.gme.cz/data/attachments/dsh.332-303.1.pdf

[35] *Semiconductor cooler data sheet* [online]. Bm: EZK. 2007. Available from: https:// www.gme.cz/data/attachments/dsh.072-400.1.pdf

[36] Catalog of power loads. *Farnell e-shop* [online]. 22 May 2017. Available from: http:// cz.farnell.com/c/testovani-mereni/stolni-napajeci-zdroje-zdroje-zateze/dc elektronice-zateze