STDP9320, STDP9310, STDP9210
STDP7320, STDP7310

Athena — Premium high resolution multimedia monitor controller with 3D video

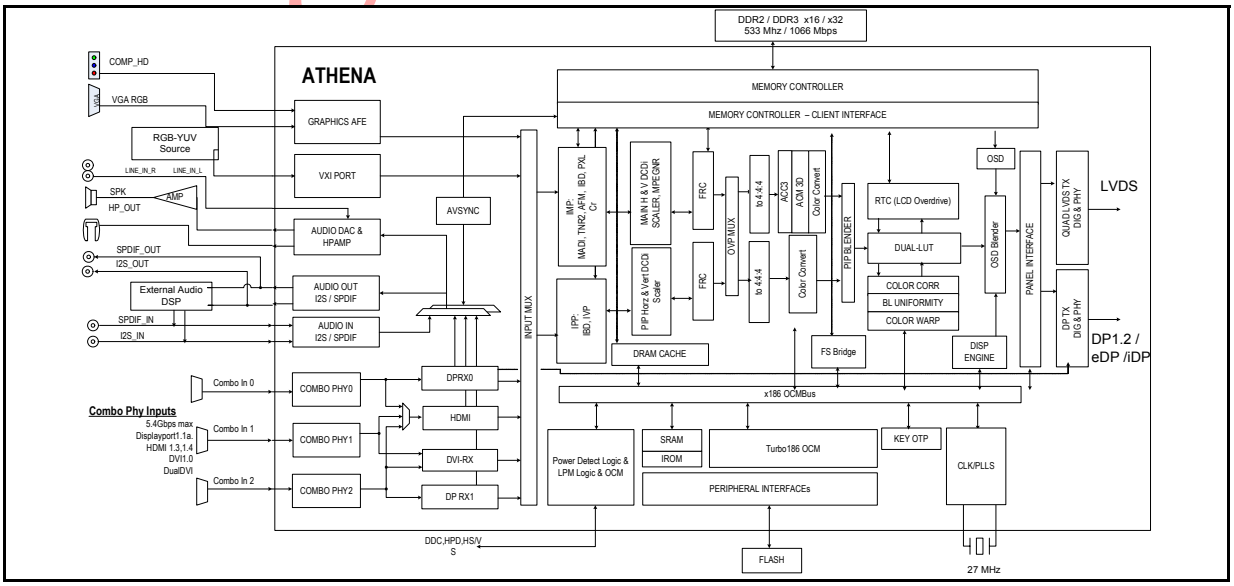
Preliminary data

Features

- Single-chip WQXGA (2560 x 1600) monitor scaler (STDP93x0)
- Single-chip 3D FHD (1920 x 1080 120 Hz) monitor scaler (STDP9210)
- Single-chip WUXGA (1920 x 1200) monitor scaler (STDP73x0)
- Integrated DisplayPort® (DP) 1.2 compliant Rx and Tx with support for eDP, multistream, and 3D video formats
- Video processing supports full or partial capture of 4096 x 2160 format scaled to 2560 x 2160 output format
- Integrated HDMI 1.4 receiver to support 3D video
- Integrated dual-DVI receiver to support 3D video
- 10-bit triple ADCs (sampling rate up to 205 MHz)
  - Integrated 2:1 MUX to receive VGA and component input
- High-speed dual LVDS Tx (STDP73x0) or quad LVDS Tx (STDP93x0/STDP9210)
- Advanced PIP/PBP for all input sources
- DDR2/DDR3 memory interface 32 bits wide (STDP93x0/STDP9210) or 16 bits wide (STDP73x0)
- Supports daisy chaining of monitors of up to four streams (STDP9320/STDP7320)
- Video window detection for multimedia content display
- Panel backlight RGB uniformity compensation
- Advanced Faroudja® video processing: MADi and DCDi
- 6-axis color control independent of ACC
- On-chip microprocessor
- Advanced bit-mapped OSD controller
- 3D Frame Rate Conversion (FRC) and advanced overdrive to support 3D video
- 4Kx2K screen resolution support

Applications

- Multifunctional monitors including 3D monitor, max input and output resolution up to WQXGA (STDP93x0), FHD (STDP9210), and WUXGA (STDP73x0)



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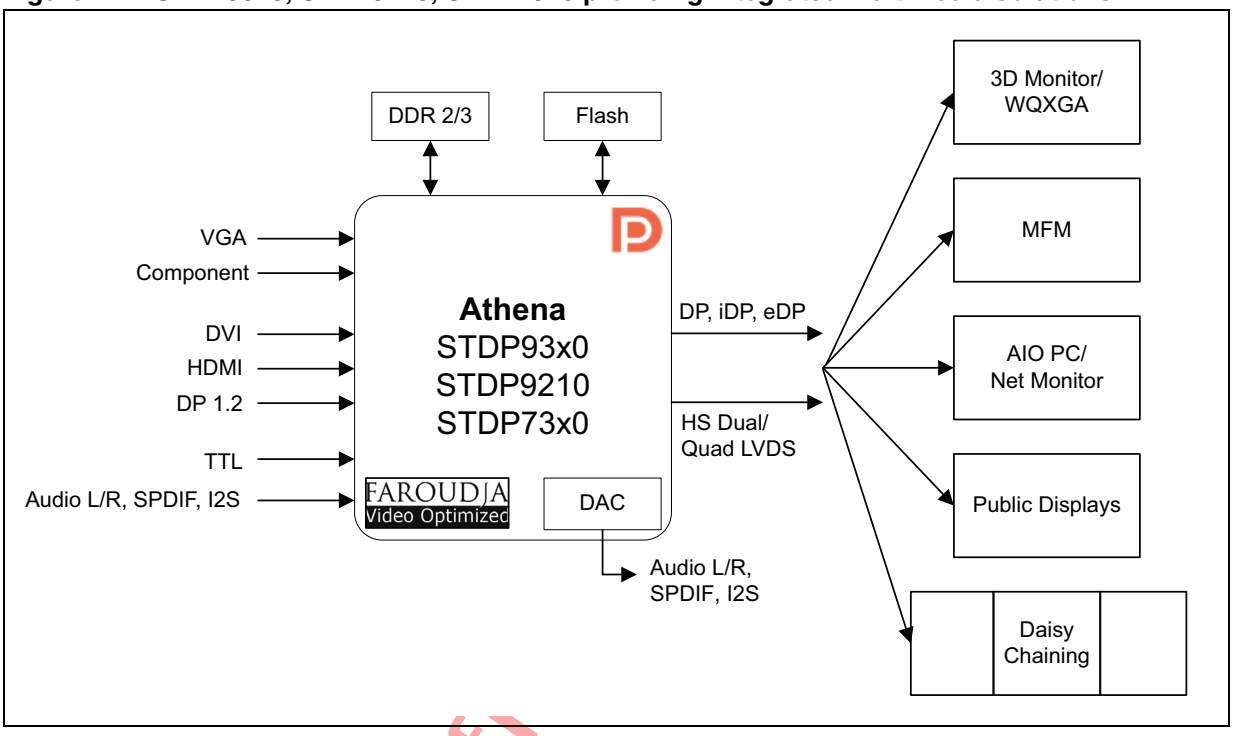


2 Description

The STDP93x0, STDP9210, and STDP73x0 (i.e. Athena) ICs are a series of innovative System-on-Chip (SoC) controllers designed for multifunctional monitors with a maximum resolution of up to 2560 x 1600 (STDP93x0), 1920 x 1200 (STDP73x0), and 120 Hz FHD (STDP9210).

The Athena chips are the first ICs to combine a DP 1.2 receiver/transmitter, HDMI 1.4 receiver, and dual DVI receiver to support 3D video source from graphics cards and Blu-rays for full HD 120 Hz display.

The Athena ICs can capture a maximum of 4096 pixels by 2160 lines. This can be either bypassed unchanged or scaled down to a maximum of 2560 x 1600 or 2048 x 2160 (STDP93x0) or 1920 x 1200 (STDP73x0) or 120 Hz FHD (STDP92x0). Two types of output ports (i.e. LVDS and DP) deliver unparalleled image quality and supports display resolutions of up to WQXGA, WUXGA, and FHD as well. Both outputs simultaneously output the scaled video, or bypass the captured input video. Alternately, the DisplayPort transmitters may be programmed to drive a multi-stream display.

The Athena SoCs allow for a flexible LCD/notebook panel interface by providing high-speed dual (STDP73x0) and quad (STDP93x0/STDP9210) LVDS transmitters as well as iDP/eDP1.2 transmitters. DP 1.2 enables multi-monitor displays (i.e. daisy chain support) in STDP9320 and STDP7320 by providing multiple streams through a signal cable connection.

These new SoCs greatly simplify the design for WQXGA monitors, 120 Hz FHD monitors, and WUXGA multifunctional monitors with their unique integration of video inputs/outputs, video processors, advanced video quality enhancement engines, DDR2 and DDR3 controllers, usability features such as PIP/PBP, video window detection, and cost-effective firmware update technology. In addition, the Athena ICs allow design of 4K x 2K monitors using multiple devices.

Their rich feature sets, high level of integration, improved scaling and video processing, and color management technologies (e.g. 6-axis color control and RGB uniformity compensation) make STDP93x0, STDP9210, and STDP73x0 the ideal answers for high-quality, integrated multimedia monitor solutions.

A new feature—Video Window detection— automatically detects video content on selected PC DVI, HDMI, or DP input and frames the content in a window to enable selective video processing such as Adaptive Contrast Control 3 (ACC3) and Active Color Management-3D (ACM-3D), TNR, enhancer, and sharpness. This enables viewers to enjoy watching Web based multimedia content with image enhancement applied inside the detected active video window.

The new technology, EZ-Display UP, provides the ability to upgrade to the latest firmware through the existing DisplayPort or HDMI interfaces on the monitor scaler. This new feature enables faster and easier firmware upgrades than the traditional method—without the need to open the monitor cabinet.

The Athena SoCs offer DisplayPort (DP) 1.2 interface for receiver and transmitter applications. The integrated receiver and transmitter support an open industry “DisplayPort Standard” AV interface introduced by VESA. This new interface standard offers high bandwidth AV signal transmission over fewer lines for interconnects within multimedia monitor applications. The DisplayPort standard includes an optional HDCP 1.3 content protection scheme for secured audio-visual data transmission between sources and sink devices.

Table 1. Athena selection table

Part number	Application	DDR I/F	TTL Input	Output	Package
STDP9320-BB	WQXGA with daisy chain	32-bit	Yes	Quad LVDS and DP 1.2	521-ball HSBGA
STDP9310-BB	WQXGA	32-bit	Yes	Quad LVDS or DP 1.2	521-ball LFBGA
STDP9210-BB	3D FHD 120 Hz	32-bit	Yes	Quad LVDS or DP 1.2	521-ball LFBGA
STDP7320-BB	WUXGA with daisy chain	16-bit	No	Dual LVDS and DP 1.2	361-ball LFBGA
STDP7310-BB	WUXGA	16-bit	No	Dual LVDS or DP 1.2	361-ball LFBGA

3 Main features

3.1 Resolutions

- WQXGA (2560 x 1600 / 1440) 60 Hz input and output
- 3D FHD (1920 x 1080) 120 Hz input and output
- 4Kx2K screen resolution support
- 4096 x 2160 input frame capture & bypass
- 2560 x 2160 video processing output

3.2 Dual integrated DisplayPort receivers

- Two 4-lane DisplayPort receivers, one DP1.2 & the other DP1.1a compliant
- Max DP link speed up to 5.4 GHz for DP1.2 and max 2.7 GHz speed on the DP1.1a receiver
- Support eDP1.2 input
- Max video resolution 2560x1600
- Support 3D stereo video format
- Max video stream pixel clock : 300 MHz
- Support GTC AVSync & HBR audio format
- Support repeater for multi-stream daisy-chain monitor
- HDCP 1.3 content protection with integrated key storage

3.3 Integrated HDMI 1.4 receiver

- Max HDMI speed up to 3 GHz
- Deep color and wide gamut support
- Max video resolution 2560x1600
- Support 3D stereo video format
- Max video stream pixel clock out: 300 MHz
- Support HBR audio format
- HDCP 1.4 content protection with integrated key storage

3.4 Dual integrated DVI receiver

- Support Dual DVI input for 3D Video up to 300 MHz
- Max DVI speed up to 165 MHz in single DVI Mode
- Max video resolution 2560x1600
- HDCP 1.2 content protection with integrated key storage

3.5 Analog video input port

- Integrated 10-bit triple ADCs
- 1x VGA(RGB) and 1x component input
- Max ADC sampling rate : 205 MHz
- Low power mode support and sync detection

3.6 TTL video input port

- 24-bit multi-format video input port

3.7 Dual input video capture ports

- Flexible PIP, PBP, and POP support capability (video, graphics) between any 2 input ports
- Input Format Detection & video processing

3.8 Audio input and output system

- 8-CH HBR audio source from DP or HDMI receivers
- SPDIF & I2S Rx ports: max input sampling rate 192 KHz
- Analog audio line In for HP, line-out bypass
- 24 b audio DAC with mute ramp @ 44.1 KHz, 48 KHz, stereo line out/headphone out
- SPDIF Tx port: output sampling rate 192 KHz, HD audio
- Quad stereo I2S Tx port: output sampling rate 192 KHz

3.9 3D monitor support

- Comprehensive 3D input format decode from HDMI1.4, DP1.2 or dual DVI sources up to 120 Hz inputs
- Enhanced overdrive with temperature compensation
- 3D Frame Rate Conversion and formatting for 120 Hz frame
- Sequential or line interleaved panels
- Shutter glass on-off timing control signal
- Scanning backlight PWM ccntrol to reduce crosstalk

3.10 Active video window detection and enhancement

- Robust detection works with complex background condition
- Applies enhancer, sharpness, ACC3, ACM3D inside detected window

3.11 Video image processing

- Dual path input video processing
- Dual path vertical and horizontal downscale or upscale
- High quality linear sharpness control via peaking filter
- Support non-linear scaling for aspect ratio conversion
- Support spatial de-interlacing through vertical filter
- Maximum input resolution: 4096 x 2160
- Maximum scaled output resolution: 2560 x 2160
- Maximum bypass resolution: 4096 x 2160

3.12 Faroudja technology for image quality

- DCDi
- Frame/field-based motion detection and pixel-based Motion Detection for Adaptive De-Interlacing (MADI)
- Film mode detection
- Non-linear video enhancer

3.13 Output video processing

- Main, PIP & OSD blender with multi-PIP support
- Independent 6-Axis color control engine
- Quick-Match2 enhanced dual gamma Look Up Table
- RGB uniformity compensation
- LCD overdrive with temperature compensation and 3D display enhancement
- Left-Right dual-drive panel format support
- Enhanced line interleaved and frame sequential 3D panel interface support

3.14 DDR memory controller

- Support DDR2 and DDR3 memory interface
- Supports 16/32-bit memory I/F 1x16, 2x16, 1x32
- DDR max frequency 533MHz for DDR2-1066

3.15 Output ports

- Quad/dual channel LVDS transmitter
- DisplayPort 1.2, 5.4 GHz transmitter with multi-stream capability for daisy-chaining monitors
- Support eDP1.2 for notebook monitor
- Simultaneous output on LVDS & DPTx
- Bypass mode to bypass video from capture source to output port

3.16 On-chip microprocessor and OSD controller

- Integrated 200 MHz x186-turbo microprocessor with rich function library
- Advanced bit-mapped OSD controller with 3D support
- Integrated JTAG debug bridge, UART, DDC2BI
- General Purpose Inputs/Outputs (GPIOs)

4 System-on-chip subsystem overview

This section gives a top-level overview of the device components and functional units.

4.1 Power domains

There are two power domains in the Athena SoCs: mission power domain, and LPM power domain. The bulk of the digital core logic, crystal oscillator, DDR interface, audio subsystem, panel interfaces are part of the mission power domain.

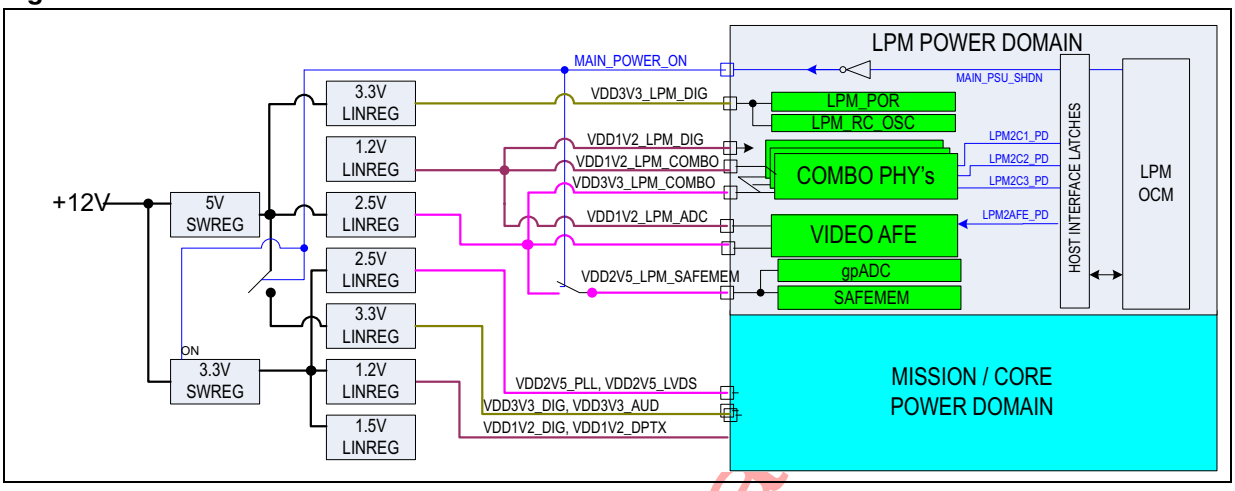
The Combo-Phy receivers, the analog video front-end are within an isolated power rail that form part of the LPM power domain. The LPM power domain also contains the cold power-on initialization control circuitry and a Low-Power On Chip Micro (LPM-OCM) and an RC-oscillator that clocks all digital logic inside the LPM domain.

Table 2. Power domains

Module	Power domain	Rails
MISSION CORE LOGIC	Mission	VDD1V2_DIG
MISSION I/O	Mission	VDD3V3_DIG
DDR INTERFACE	Mission	VDDQ_DDR
CLOCKS AND PLLs	Mission	VDD2V5_PLL
AUDIO AFE	Mission	VDD1V2_AUDIO, VDDA3V3_AUD, VDD3V3_HP_AUD
DISPLAYPORT TRANSMITTER	Mission	VDD1V2_DPTX, VDD2V5_DPTX
LVDS TRANSMITTER	Mission	VDD2V5_LVDS
LPM CORE LOGIC	LPM	VDD1V2_LPM_DIG
LPM I/O	LPM	VDD3V3_LPM_DIG
VIDEO AFE	LPM	VDD1V2_LPM_ADC, VDD2V5_LPM_ADC
COMBO ANALOG PHY'S	LPM	VDD1V2_LPM_COMBO, VDD3V3_LPM_COMBO
SAFEMEM	LPM	VDD2V5_LPM_SAFEMEM

Logic in the LPM section controls these power domains by controlling external switches on the power rails. The MISSION power rails are switched off in low power modes to save power.

Figure 2. Power domain



4.2 Clock generation

4.2.1 Mission side clock generation

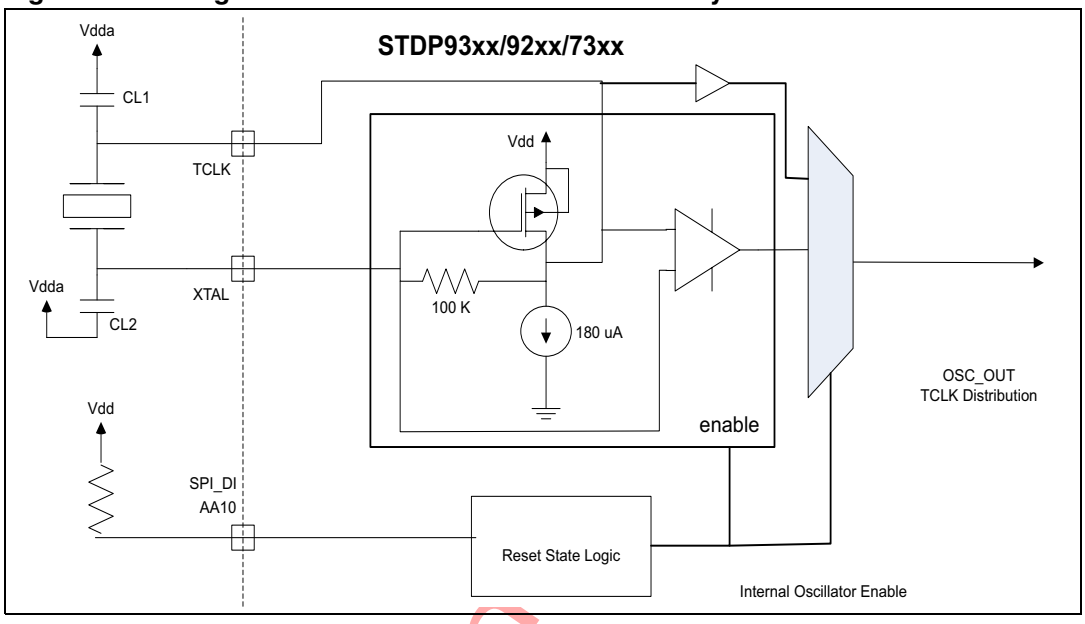
All clocks on the mission side required by the Athena ICs are either derived from the system 27 MHz TCLK crystal clock oscillator or are the respective input sampling clocks. The TCLK oscillator circuitry is a custom-designed circuit to support the use of a crystal resonator to generate a reference frequency source for the Athena devices.

4.2.2 Using the internal oscillator with an external crystal

The option for providing a clock reference is to use the internal oscillator with an external crystal. The oscillator circuit is designed to provide a very low jitter and very low harmonic clock to the internal circuitry of the Athena SoCs. An Automatic Gain Control (AGC) is used to ensure startup and operation over a wide range of conditions. The oscillator circuit also minimizes the overdrive of the crystal, which reduces its aging.

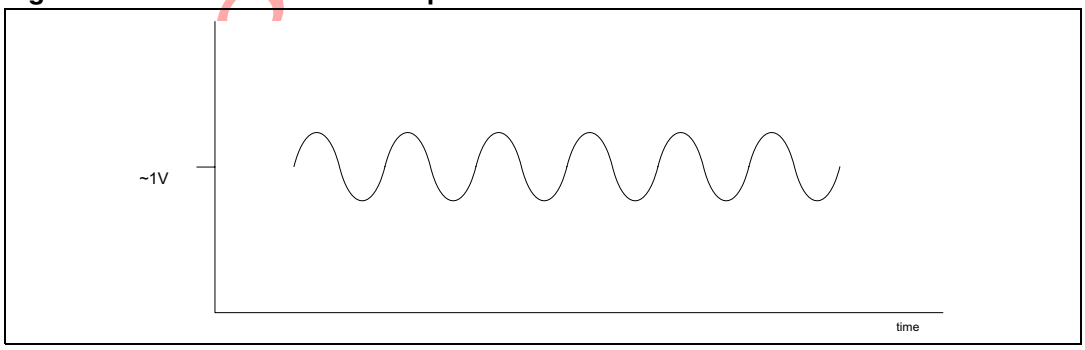
In this mode a 27 MHz crystal resonator is connected between TCLK and XTAL with the appropriate size loading capacitors CL1 and CL2. The size of CL1 and CL2 are determined from the crystal manufacturer's specification and by compensating for the parasitic capacitance of the Athena SoCs and the printed circuit board traces. The loading capacitors are terminated to the analog VDD12 power supply to increase the power supply rejection ratio when compared to terminating the loading capacitors to ground.

Figure 3. Using the internal oscillator with external crystal



The TCLK oscillator uses a pierce oscillator circuit. The output of the oscillator circuit, measured at the TCLK ball, is an approximate sine wave with a bias of about 1 V above ground (see *Figure 5: Sources of parasitic capacitance on page 17*). The peak-to-peak voltage of the output can range from 250 mV to 1000 mV depending on the specific characteristics of the crystal and variation in the oscillator characteristics. The output of the oscillator is connected to a comparator that converts the sine wave to a square wave. The comparator requires a minimum signal level of about 50 mV peak-to-peak to function correctly. The output of the comparator is buffered and then distributed to the Athena device circuits.

Figure 4. Internal oscillator output



The value of the loading capacitors used with the crystal as shown in *Figure 3: Using the internal oscillator with external crystal on page 16*, is an important design parameter. The loading capacitance (Cload) on the crystal is the combination of CL1 and CL2 and is calculated by:

Cload = ((CL1 * CL2)/(CL1 + CL2)) + Cshunt.

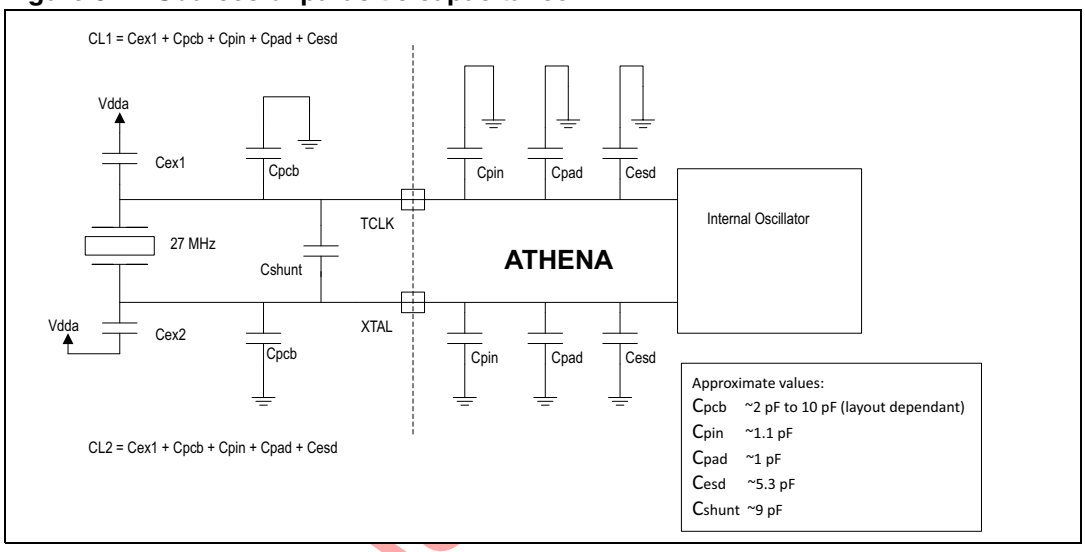
The shunt capacitance Cshunt is the effective capacitance between the XTAL and TCLK pins. For the Athena SoCs, the shunt capacitance is approximately 9 pF. CL1 and CL2 are a parallel combination of the external loading capacitors (Cex), the PCB board capacitance

(Cpcb), the ball capacitance (Cpin), the pad capacitance (Cpad), and the ESD protection capacitance (Cesd). The capacitances are symmetrical so that:

CL1 = CL2 = Cex + CPCB + Cpin + Cpad + CESD.

The correct value of Cex must be calculated based on the values of the load capacitances.

Figure 5. Sources of parasitic capacitance



When the oscillator circuit is used with a crystal resonator, the PCB traces should be as short as possible. Do not exceed the value of Cload specified by the manufacturer; this may cause potential start up problems with the oscillator. Additionally, the crystal should be a parallel resonate-cut and the value of the equivalent series resistance must be less than 90.

It is recommended to utilize a crystal of +/-25 ppm for all applications. This will ensure optimum performance.

Table 3. TCLK specifications

Frequency	Jitter tolerance	Rise time (10% to 90%)	Max duty cycle
27 MHz	+/- 25 ppm	10 ns (typical)	48% to 52%

4.2.3 LPM side clock generation

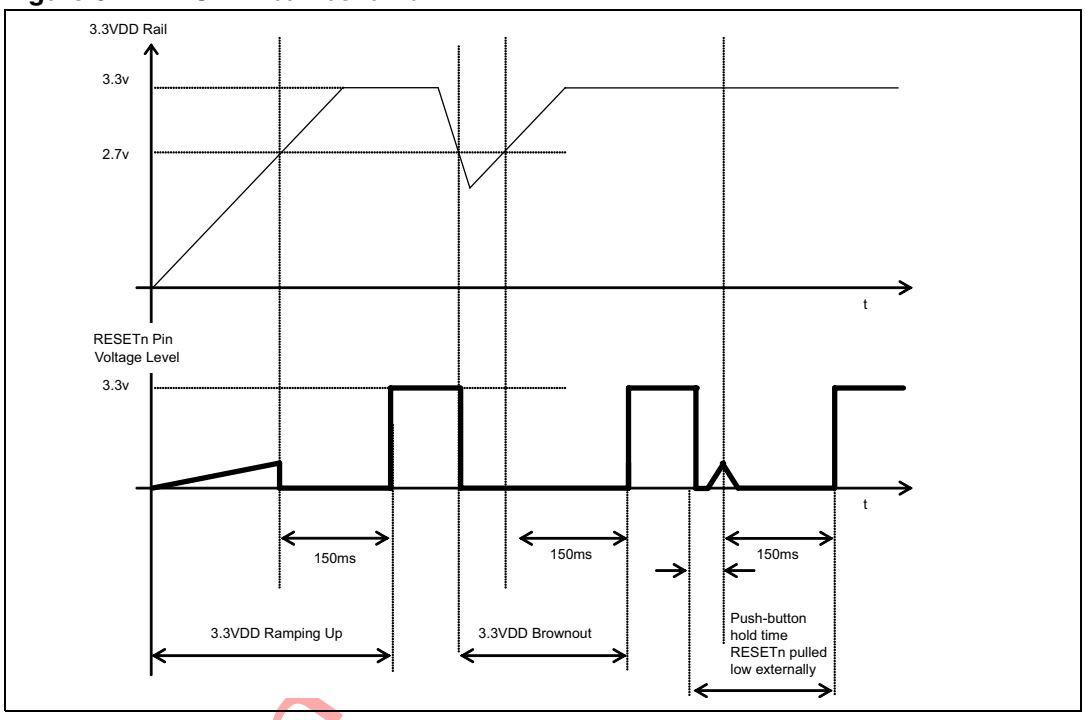
In standby and low-power modes, an LPM island digital logic maintains the chip in Low Power Mode. The clock source for this logic is from a 27 MHz RC-Oscillator . This oscillator needs to be trimmed before use. trimming is done as part of system initialization by the software. The oscillator is enabled after a power-on reset.

4.3 Hardware cold reset

The Athena SoCs integrate a voltage monitor as part of the hardware reset controller block. This block monitors the input level at the RESETn ball and the 3.3 V power supply. If the RESETn ball is pulled low, the Athena SoCs are held in reset. If the 3.3 V power supply is below 2.7 V, the Athena SoCs are held in reset and the RESETn ball is actively driven low.

When the 3.3 V supply exceeds 2.7 V or RESETn is released (no longer pulled low), an internal timer keeps the Athena SoCs in reset for 150 ms. During this 150 ms reset hold time, the RESETn ball is actively held low. The RESETn ball can therefore be connected to the active low reset input of other integrated circuits on the PCB. The figure below shows the behavior of the RESETn ball.

Figure 6. RESETn ball behavior



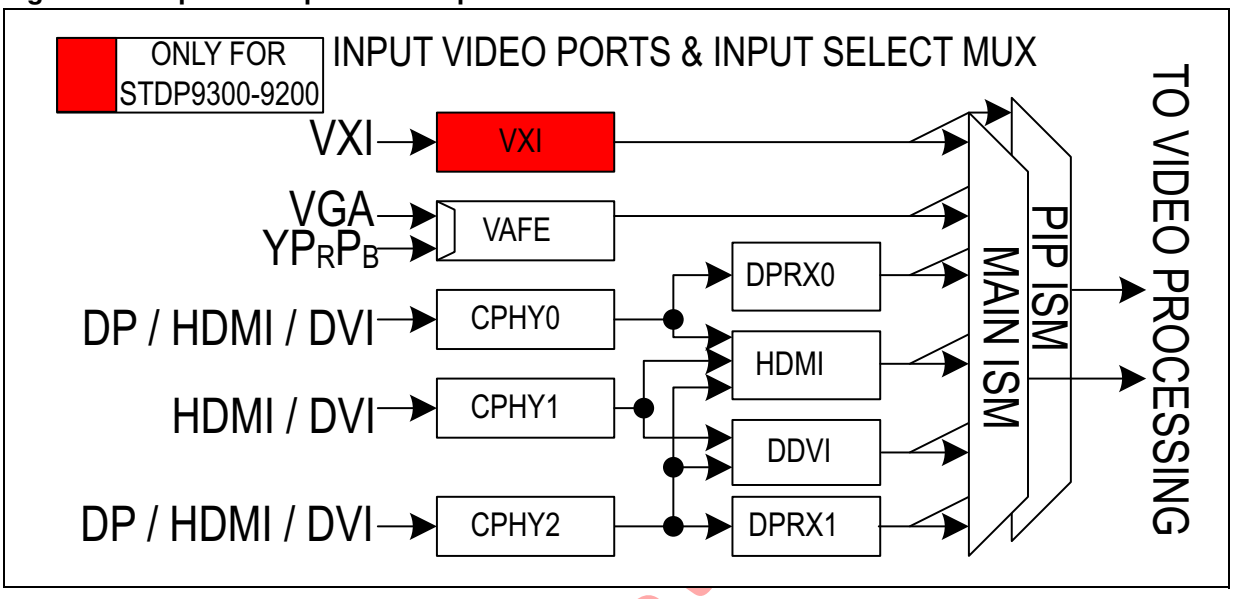
A TCLK input (see Clock Options above) must be applied during and after the reset.

Note: The reset time may vary from 125 ms to 175 ms.

4.4 Input video ports

Athena ICs feature three combo high speed digital receivers that may be configured for DisplayPort, HDMI or DVI operation, a 3-channel video analog front-end with a 2:1 MUX for VGA or component video digitization and a 24-bit TTL video input interface.

Figure 7. Input video ports and input select MUX



4.4.1 Front-end for input selection

The Athena SoCs' video processing unit can receive any two streams of the five basic ports described above processing one of these streams on the main path and the second on the PIP path.

Athena ICs have flexible ISM (Input Selection Multiplexer) to be used for capturing signals for main and PIP channel. All Analog and Digital Video Input Ports connect to the input select MUX. This MUX supplies the Video IP block with two channels, main and PIP.

The maximum capture pixel rate is 300 MHz through the main or PIP ISM modules. The two channels are processed through the video IP block. The following selections are possible through the main and PIP ISM blocks.

Figure 8. STDP93xx/92xx video input matrix

MAIN / PIP	ComboPhy0	ComboPhy1	ComboPhy2	ComboPhy1+2 (DUAL-DVI)	VGA	COMPONENT VIDEO	TTL VXI
ComboPhy0	×	✓	✓	✓ (93XX-92XX ONLY)	✓	✓	✓ (93XX-92XX ONLY)
ComboPhy1	✓	×	✓	×	✓	✓	✓ (93XX-92XX ONLY)
ComboPhy2	✓	✓	×	×	✓	✓	✓ (93XX-92XX ONLY)
ComboPhy1+2 (DUAL-DVI)	✓ (93XX-92XX ONLY)	×	×	×	✓	✓	✓ (93XX-92XX ONLY)
VGA	✓	✓	✓	✓	×	×	✓ (93XX-92XX ONLY)
COMPONENT VIDEO	✓	✓	✓	✓	×	×	✓ (93XX-92XX ONLY)
TTL VXI	✓ (93XX-92XX ONLY)	✓ (93XX-92XX ONLY)	✓ (93XX-92XX ONLY)	✓ (93XX-92XX ONLY)	✓ (93XX-92XX ONLY)	✓ (93XX-92XX ONLY)	×

Figure 9. STDP73xx video input matrix

MAIN / PIP	ComboPhy0	ComboPhy1	ComboPhy2	ComboPhy1+2 (DUAL-DVI)	VGA	COMPONENT VIDEO	TTL VXI
ComboPhy0	×	✓	✓	×	✓	✓	×
ComboPhy1	✓	×	✓	×	✓	✓	×
ComboPhy2	✓	✓	×	×	✓	✓	×
ComboPhy1+2 (DUAL-DVI)	×	×	×	×	✓	✓	×
VGA	✓	✓	✓	✓	×	×	×
COMPONENT VIDEO	✓	✓	✓	✓	×	×	×
TTL VXI	×	×	×	×	×	×	×

Note: 1 Comp TV implies analog component SD/ ED/HD.

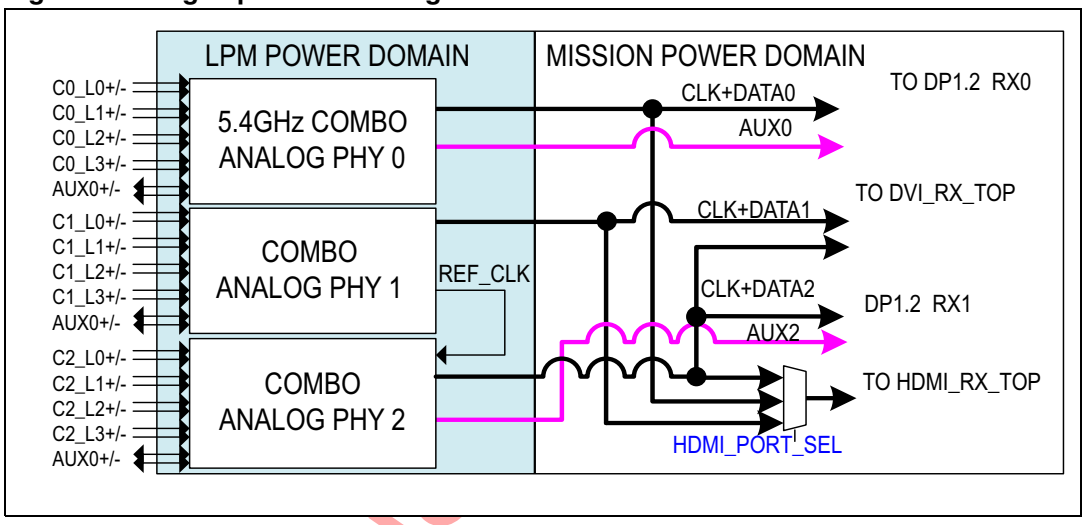
2 Combo ports can be DP1.1a/HDMI/DVI/dual-DVI.

3 Dual-DVI uses two combo ports.

4.4.2 High speed digital receivers

Athena SoCs have three high speed combo digital receivers (Combo_Phy0, Combo_Phy1, Combo_Phy2) that can be configured for DisplayPort, HDMI or DVI operation. Combo_PHY0 can support up to 5.4 Gbps link speed. Combo_Phy1 and 2 can go up to 3 Gbps.

Figure 10. High speed combo digital receivers



Each Combo-Phy features four high speed differential input channels and a differential AUX Channel. The FastAUX feature is not supported. The Phy is configurable for either DisplayPort mode or for HDMI/ DVI mode. The receivers feature internal differential termination of 100 ohms (50 ohms on each line to AVDD33). This can either be calibrated to 1/5th the external resistor value or manually programmable using registers bits.

Inputs can be AC-coupled in DisplayPort mode and DC-Coupled in HDMI / DVI modes. Either receiver differential pair takes in high speed serial differential data and converts it into 20-bit parallel data using equalization and CDR. The equalizer gain and peak frequency settings are common for all the lanes.

The Combo-Phy0 receiver characteristics will meet HBR2 operation (in accordance with DisplayPort-1.2 specification). The Phy is also configurable for HDMI-1.4 operations up to 3.0 Gbps. The Combo-Phy1 and Combo-Phy2 receiver characteristics are both designed to support up to 3 GHz. Special clock multiplexing circuitry allows combining Combo-Phy1 and Combo-Phy2 so they share a common clock receiver for Dual-DVI operation. Each lane receiver of the Phy can be set up for either clock or for data receiving. The lane ordering is programmable to optimize connectivity on the board for each of the interface standards. Note that the HDMI1.4 LAN and the audio back channel features are not supported.

The Combo-Phy is part of an isolated power domain and can continue to be powered up, operating in a special low power mode when the core power rails are off. In this mode, the Phy can be set up for activity monitoring and is under control of the LPM interface. The core interface is disabled. The Phy can be set up either for DisplayPort AUX channel communication or for HDMI / DVI mode clock channel monitoring when in low power mode. Note that the LPM handles all interface communication support features such as HDP, DDC, CEC, cable detect and others.

Combo Phy pin usage mapping

The following pin usage mappings are defined.

Figure 11. DisplayPort Combo_PHY pin map

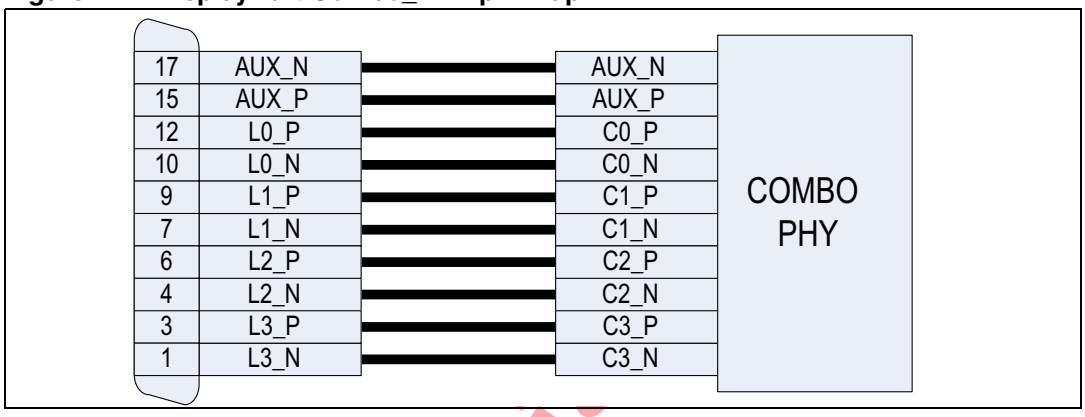


Figure 12. DVI Combo_PHY pin map

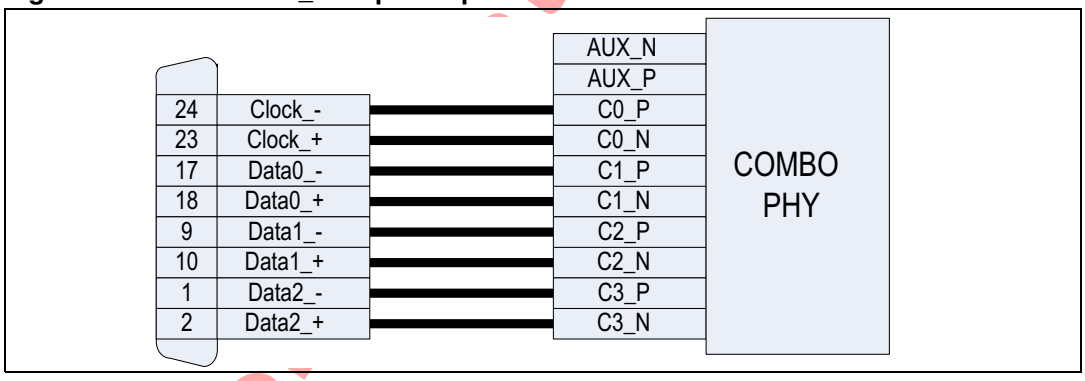


Figure 13. HDMI Combo_PHY pin map

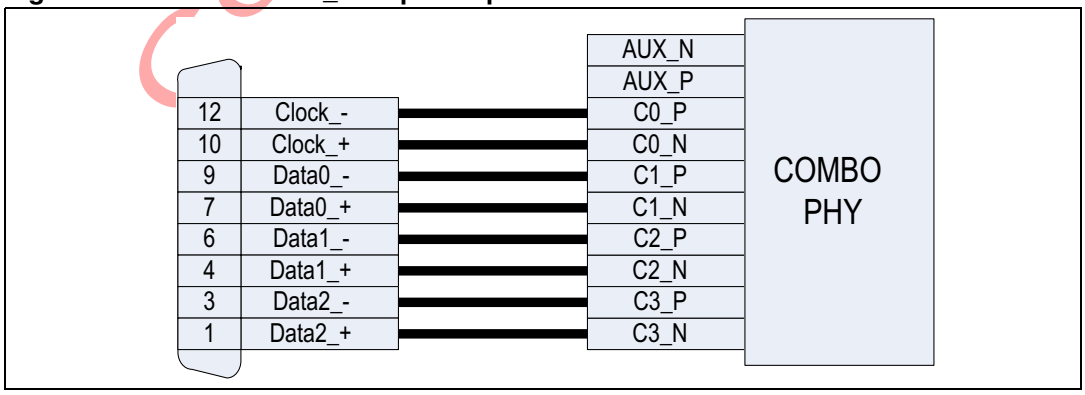
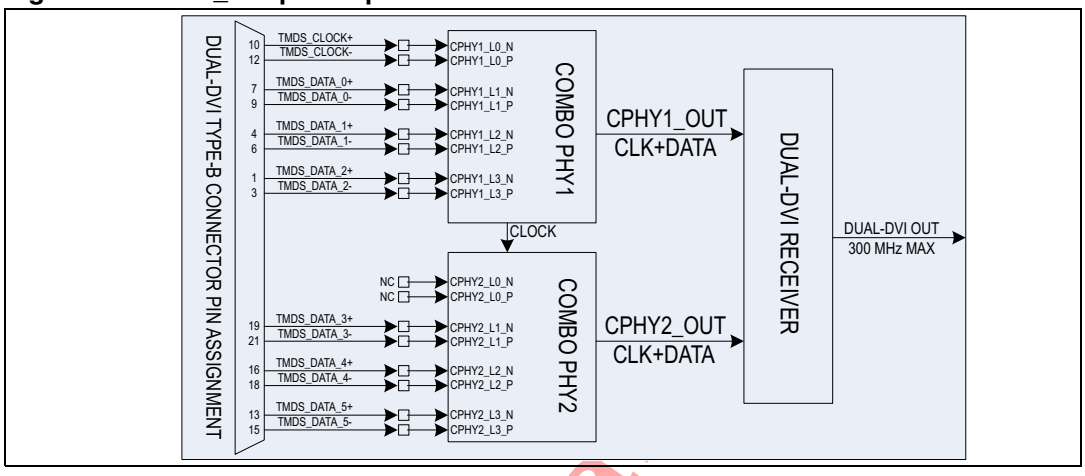


Figure 14. Dual_DVI pin map



In Dual-DVI mode, Combo-Phy1 receives RX channel 0 to 2 data pairs, along with the clock pair. Combo-Phy2 receives RX channel pairs 3,4 & 5. Combo Phy2 uses the clock received from Combo-Phy1 to recover clock and data samples. Lane0 receive pins of Combo-Phy2 are not used.

Digital receivers system usage

There are four digital receivers that can received sample data and clocks from the three Combo Phys. These are:

- DP12RX0: DisplayPort 1.2 C_BY compliant receiver with MST and GTS support
- DP12RX1: DisplayPort 1.1a compliant receiver
- HDMIRx: HDMI 1.4 compliant receivern (no support for LAN or audio back channel)
- DDVIRX: Dual DVI receivers capable of operating in a single mode (only 1 receiver can output data at a time) or in a concatenated dual-DVI mode in accordance with HDMI 1.4 specifications

The Combo Phy usage is based on the internal connectivity between the combo receivers and the digital receivers.

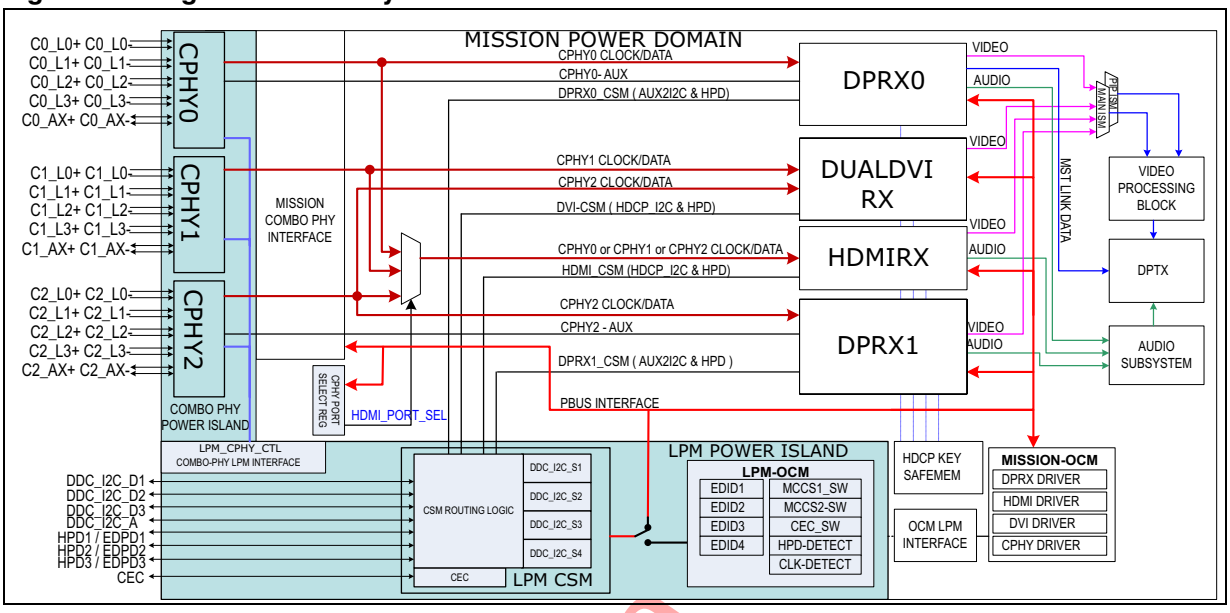
Figure 15. Internal connectivity between combo and digital receivers

COMBO PHY OUTPUT			DIGITAL RECEIVER	COMMENTS
CHPY0	CHPY1	CPHY2		
✓	×	×	DP12RX0	USE THIS FOR DP1.2 MULTISTREAM (MST)
×	×	✓	DPRX1	USE THIS FOR 2ND DP1.1a
✓	✓	✓	HDMI	HDMI CAN COME FROM ANY CPHY
×	✓	×	DVI-A	DVI-A AS SINGLE DVI RX
×	×	✓	DVI-B	DVI-B AS SINGLE DVI RX
×	✓	✓	DUAL-DVI	ONLY IN 93XX-92XX PARTS. USES DVI-A + DVI-B.

Digital receivers system overview

The System overview of the digital receivers is shown below.

Figure 16. Digital receivers system



The Combo Phy inputs support Low Power Mode operation. The Combo Phys arelocated within an isolated power rail (shown as the shaded area). During Low Power Mode operation, the receiver is put in a reduced power state. In this mode, the analog circuitry limits power consumption. One of the channels is set up for activity monitoring. AUX channel activity (in the DisplayPort mode) and clock channel (in the DVI or HDMI mode) are monitored. In Low Power Mode, the mission power domain is off. All monitoring activities are controlled by the LPM interface when in the Low Power Mode. Power optimization allows these activities to be carried out within very low power consumption levels. Special Auto_Wake logic within the LPM interface, allows automatic monitoring and Wake_Up event generation. Subsequent event processing by the LPM-OCM during the process of System_Wakeup can cause power rail restoration and warm reset of the mission side.

Under active power mode operation, the Combo-Phys are controlled through PBus interface by the mission-OCM which also provides all system drivers. The connectivity between the Combo Phy outputs and digital receivers is as defined in the table shown in the previous section, *Figure 15: Internal connectivity between combo and digital receivers*. The LPM power domain provides other communication support features such as cable detect, host power detect and HPD_out capabilities, DDC slave devices and CEC device and port interface. In addition, the LPM-OCM provides drivers for MCCS and EDID support services. A communication interface exists between the mission and LPM-OCMs to ensure a smooth exchange of control, status, and data information.

The outputs of the four digital receivers are routed to the video and audio processing blocks. At any instance, all three of the Combo-Phys and any two of the receivers may be simultaneously active.

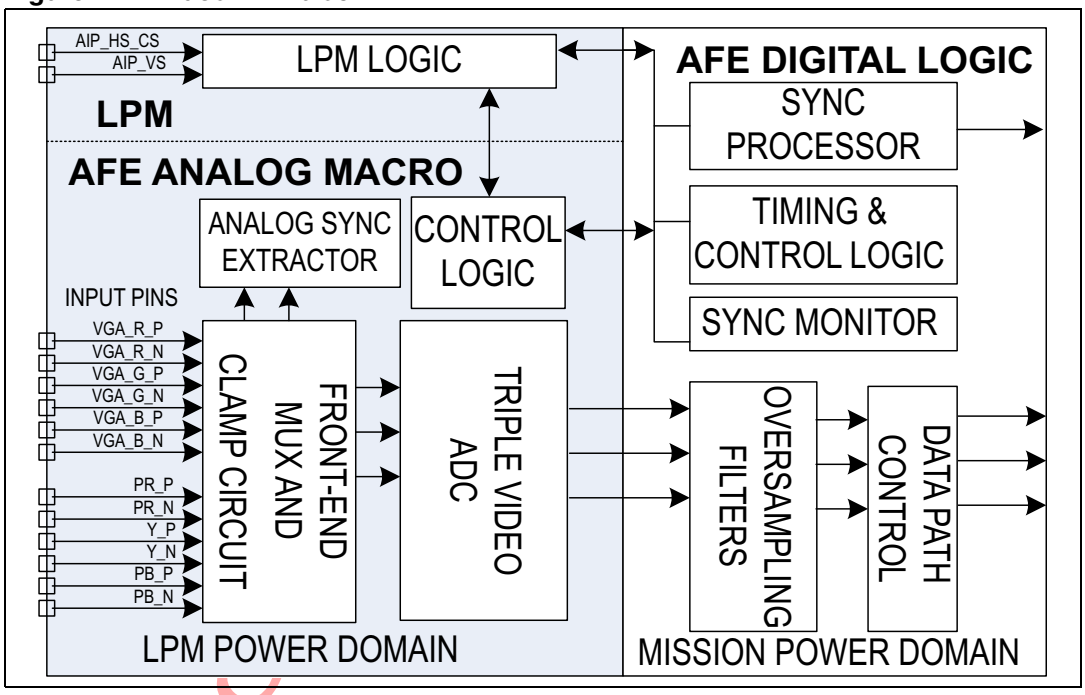
The DP12RX0 receiver accepts both SST and MST data streams and can output one of the streams on the MST packet to the DP digital receiver backend block for recovery of video and audio data from one of the streams. A payload of up to four streams can be handled. Advanced effort symbol detection and correction for MST streams is supported. The MST link data can also be routed to the DP transmitter link layer. The DP receiver handles HDCP 1.3 encrypted streams. Multiple video formats as defined in DP1.2 specs including xvYCC and AdobeRGB formats are supported. The receiver also supports GTC protocol to perform audio-video stream synchronization. High bit rate audio formats of up to 768 kbps can be

received. Other DP1.2 features that are additionally supported include, SDP nesting and handling of 3D formats. The AUX channel can handle streams of 1.5 Mbps. It supports I2C_over_Aux as well as side-band messaging and GTC messaging as defined in DP1.2 specifications.

4.4.3 Video analog front-end

The video analog front-end in the Athena ICs provides the capability to digitize one of two analog video ports: VGA-RGB or component video. The video AFE block is shown below:

Figure 17. Video AFE block



There are two modules on this interface, the AFE analog macro and the AIP-AFE digital logic. The AFE analog macro is isolated from the core logic and is part of the LPM power domain. This allows Low Power Mode, port activity monitoring to take place under control of the LPM interface when the mission power domain is off. To ensure Low Power Mode port activity detection is possible, the AIP HSYNC and VSYNC pins are processed by LPM logic in the LPM power domain.

AFE macro

The Athena SoCs' front end supports three internal 205 MHz, 10-bit ADCs for analog video input processing. A 2:1 input multiplexer selects one of the two input video ports for digitization. It is not possible to support PIP between the two inputs ports (RGB & YPrPb). The AFE macro contains clamp circuitry to support hard clamping or video loop clamping of the selected video ports. There are two analog sync separator circuits, one for VGA Sync-On-Green and one for component luma (Y) inputs. So simultaneous monitoring of one port and digitization on the other port is possible. The AFE analog macro incorporates Instant_AutoAdjust circuitry for rapid, ADC sampling phase optimization and digitization subsequent to a port switch or mode change. The table below summarizes the ADC characteristics.

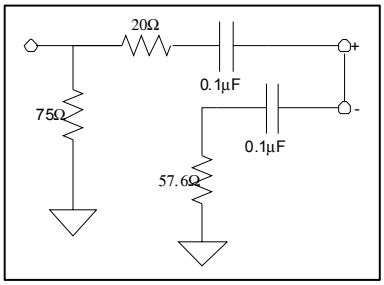
Table 4. ADC characteristics

ADC features	Min	Typ	Max	Units
Input signal dynamic range			1.0	V
Input signal digitization range		0.7		V
Zero scale adjust sensitivity		3		LSB
Sampling Frequency (Fs)		0-205		MHz
Differential Non-Linearity (DNL)		+/-0.5		LSB
Integral Non-Linearity (INL)		4.5		LSB

AFE video signal connection

The necessary external hardware is integrated into the AFE of the Athena SoCs to support direct connection to the physical analog signal connector on the PCB. Only an AC coupling capacitor and a termination resistor are needed between the physical connector and the Athena SoCs. The ADCs in Athena SoCs require a differential routing across the input positive terminal and the return line.

Figure 18. Sample connection for analog input signal



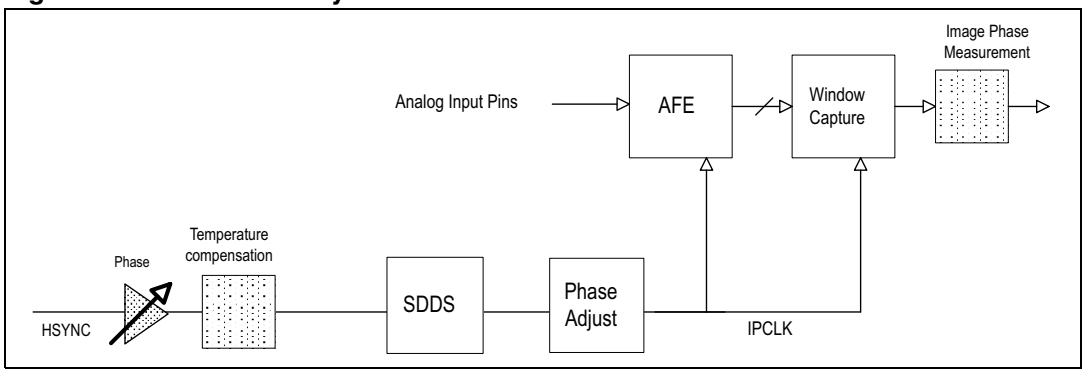
Note: Follow the recommend layout guidelines for the circuit.

ADC sampling clock recovery circuit

The Source Direct Digital Synthesis (SDDS) clock recovery circuit generates the clock used to sample analog video signals. The SDDS is used to generate closed loop Sampling Clock (SCLK). The maximum closed loop sample rate is 205 MHz. In the closed loop mode of operation, the circuit is locked to the HSync of the incoming video signal. HSync is either from TTL HSYNC inputs or recovered from the sync extracted by the ASE circuits.

Patented digital clock synthesis technology makes the Athena SoCs' clock circuits resistant to temperature/voltage drift. Using Direct Digital Synthesis (DDS) technology, the clock recovery circuit can generate any IP_CLK clock frequency within the range of 10-205 MHz.

Figure 19. Clock recovery



ADC sampling phase adjustment for RGB graphics inputs

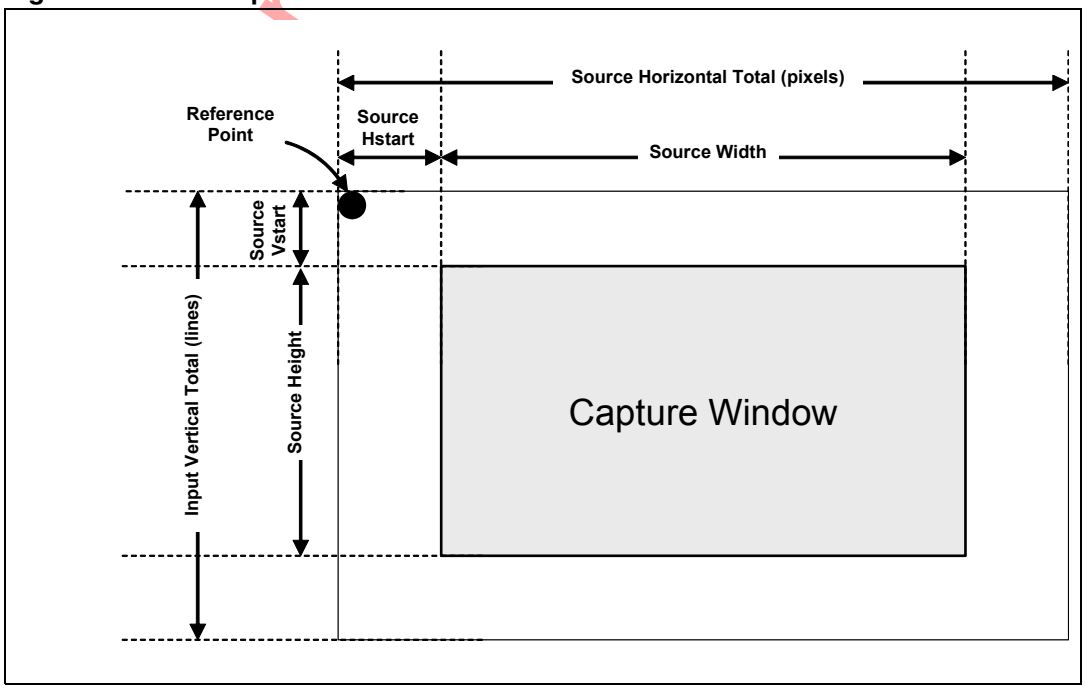
The programmable ADC sampling phase is adjusted by delaying the SDDS clock with respect to the HSync input. The accuracy of the sampling phase is checked and the result is read from a register. This feature enables accurate auto-adjustment of the ADC sampling phase.

ADC capture window

The figure below illustrates the capture window used for input. In the horizontal direction, the capture window is defined in IP_CLKs (equivalent to a pixel count). In the vertical direction, it is defined in lines. All the parameters beginning with “Source” are programmed Athena register values.

Note: The Input Vertical Total is determined solely by the input and is not a programmable parameter.

Figure 20. ADC capture window



The reference point marks the leading edge of the first internal HSync following the leading edge of an internal VSync. Both the internal HSync and VSync are derived from external HSync and VSync inputs.

Horizontal parameters are defined in terms of single-pixel increments relative to the internal horizontal sync. Vertical parameters are defined in terms of single-line increments relative to the internal vertical sync.

For interlaced inputs, the Athena SoCs may be programmed to automatically determine the field type (even or odd) from the VSync/HSync relative timing.

4.4.4 Digital input port

The STDP93xx and STDP92xx devices, (STDP73xx has no Digital Input Port) support a 24-bit digital input port with digital sync inputs, field indicator, data enable, and two clock inputs. The 24-bit input can be flexibly configured to support a wide range of digital sources. Inputs to the digital input port are TTL-compatible with a maximum clock speed of 150 MHz. Sync and clock polarities are programmable.

Supported digital input formats

The following digital video formats are supported by the Athena SoCs' digital video graphic port:

- ITU-BT-656
- 8-bit 4:2:2 YCbCr or YPbPr
- 16-bit 4:2:2 YCbCr or YPbPr
- 20-bit 4:2:2 YCbCr or YPbPr
- 24-bit 4:4:4 YCbCr or YPbPr
- 24-bit RGB

The following figures illustrate the timing of the video formats:

Figure 21. ITU-R BT656 input

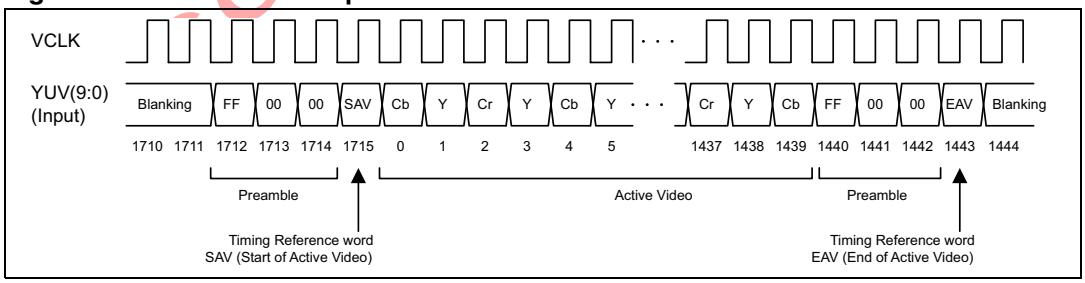


Figure 22. 8-bit 4:2:2 YCbCr/YPbPr

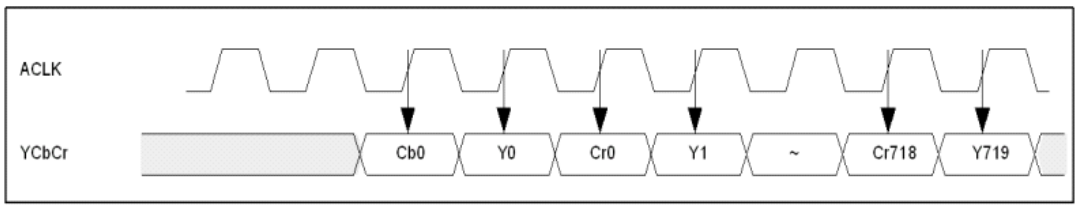


Figure 23. 16/20-bit 4:2:2 YCbCr/YPbPr

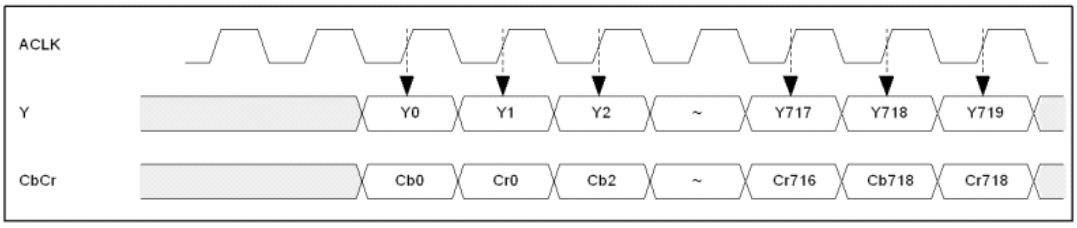


Figure 24. 24-bit 4:4:4 YCbCr/YPbPr

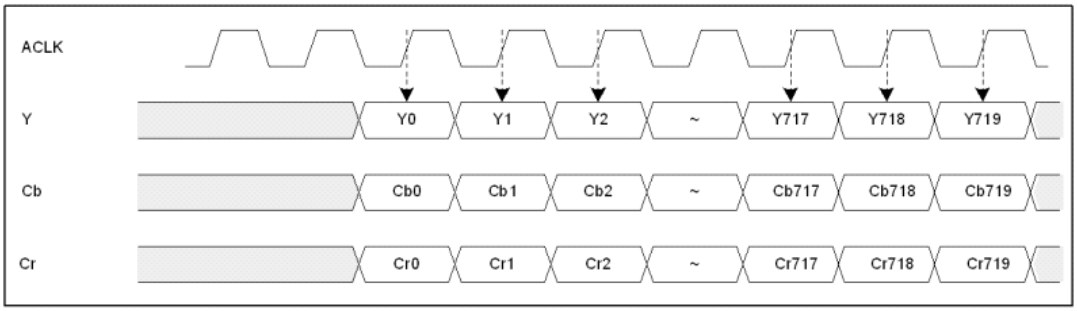
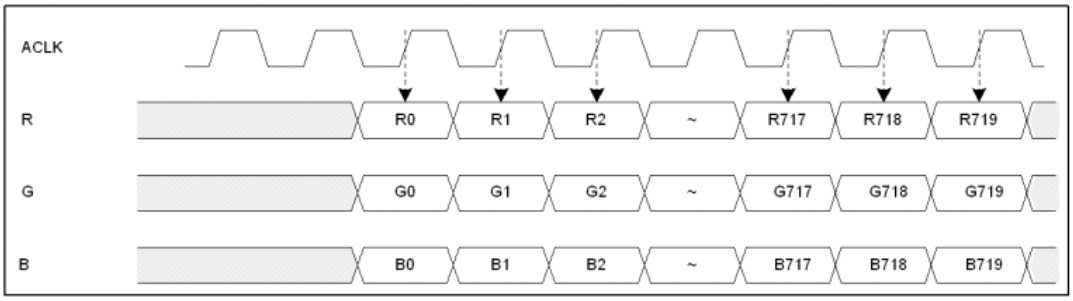


Figure 25. 24-bit RGB



4.4.5 656 decoder

The ITU-BT-656 video format consists of pixel clock and 8 bits/10 bits of data depending on the input. No separate HSync, VSync, and odd signals are present. Timing data is embedded in the data stream. The internal 656 decoder will extract the HSync, VSync, and odd signals from the embedded timing data.

Digital input port configuration

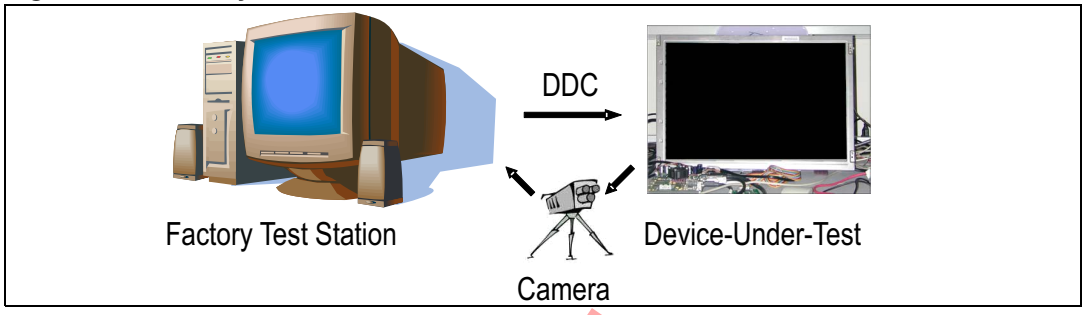
The digital input port offers flexible mapping of the 24-bit input bus and allows individual bit configuration. The purpose of this flexible mapping is to ease the circuit board design when interfacing to other devices.

4.5 Factory and display calibration

The DDC2Bi port can be used for factory testing. This is illustrated in the figure below. The factory test station connects to Athena SoCs through the DDC channel of the DSUB15

connectors. The PC makes Athena SoCs' display test patterns. A camera can be used to automate the calibration of the LCD panel.

Figure 26. Factory calibration and test environment



STMicroelectronics provides tools to create user settings for ACC/ACM, gamma compensation, and LCD overdrive functions. These tools allow the user to optimize the settings of the Athena SoCs for the display in question as well as their preference for video performance.

4.6 Input Format Measurement (IFM)

The Athena SoCs support multiple Input Format Measurement (IFM) blocks. These blocks can be independantly used for measuring the horizontal and vertical timings of main and PIP inputs as well as measure the timing format directly at the port receiver output. This flexiblity allows background monitoring as well as allows easier port driver control. A third IFM on the capture path can be used for detecting the change in either the main or PIP input to configure the system accordingly.

The IFM features a programmable reset, separate from the regular Athena SoCs soft reset. This reset disables the IFM, reducing power consumption. The IFM is capable of operating while the chips are running standby mode (mission rails are still powered). All port monitoring activities are handled by LPM logic when in sleep mode.

Horizontal measurements are assessed in terms of the selected IFM_CLK—either TCLK (normal operation) or OCM_CLK/2—while vertical measurements are assessed in terms of HSync pulses.

4.6.1 Horizontal and vertical measurement

The IFM is able to measure the horizontal period and active high pulse width of the HSync signal, in terms of the selected clock period (either TCLK or OCM_CLK/2). Horizontal measurements are performed only on a single line per frame (or field). The line used is programmable. It measures the vertical period and VSync pulse width in terms of rising edges of HSync.

Once enabled, measurement begins on the rising VSync and is completed on the following rising VSync. Measurements are made on every field/frame until disabled.

4.6.2 Format change detection

The IFM is able to detect changes in the input format relative to the last measurement and then alerts both the system and the on-chip microcontroller. The microcontroller sets a measurement difference threshold separately for horizontal and vertical timing. If the current

field/frame timing is different from the previously captured measurement by an amount exceeding this threshold, a status bit is set. An interrupt can also be programmed to occur.

4.6.3 Watchdog

The watchdog monitors input VSync/HSync. When any HSync/VSync period exceeds the programmed timing threshold, status bits are set. An interrupt can also be programmed to occur.

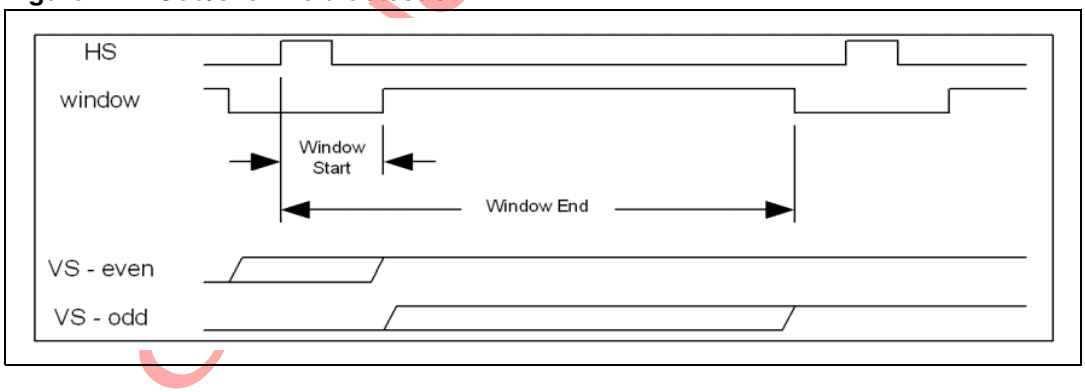
4.6.4 Internal odd/even field detection

The IFM has the ability to perform field decoding of interlaced inputs to the ADC via two methods.

The first method consists of internal hardware counting the number of lines between Vsync pulses for the current field. If the count is found to be an odd number, then the next field is marked even. This first method is recommended to be used.

The second method consists of the user specifying start and end values to outline a window relative to HSync. If the VSync leading edge occurs within this window, the IFM signals the start of an odd field. If the VSync leading edge occurs outside this window, an even field is indicated (the interpretation of odd and even can be reversed). The window start and end points are selected from a predefined set of values.

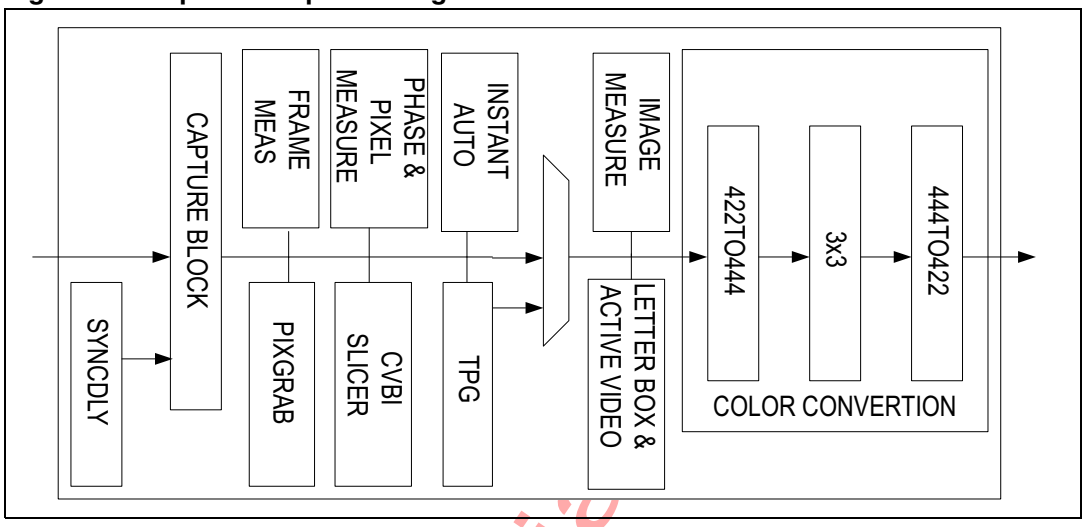
Figure 27. Odd/even field detection



4.7 Input video processing

Input video processing involves video capture, measurement, data extraction and formatting of two streams of video from the selected input video source. Each channel first goes through an input video processor which is used for image analysis and pre-conditioning. This block is used to collect information about the video content and also to prepare the video into the proper format to be processed downstream. For example, 4:4:4 YUV video is converted to 4:2:2 YUV video in the input video processor since the downstream blocks require YUV in 4:2:2 format.

Figure 28. Input video processing



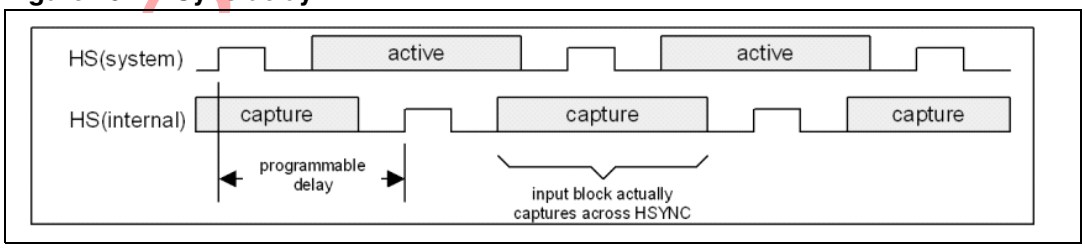
4.7.1 HSync/VSync delay

The active input region captured by the Athena SoCs is specified with respect to internal HSync and VSync. By default, internal syncs are equivalent to the HSync and VSync at the input pins and thus force the captured region to be bounded by external HSync and VSync timing. However, the Athena SoCs provide an internal HSync and VSync delay feature that removes this limitation. By delaying the sync internally, the Athena SoCs can capture data that spans across the sync pulse.

It is possible to use HSync and VSync delay for image positioning. (Alternatively, Source_HSTART and Source_VSTART in *Figure 20: ADC capture window on page 27* are used for image positioning of analog input). The intentional movement of images across apparent HSync and VSync boundaries creates a horizontal and/or vertical wrap effect.

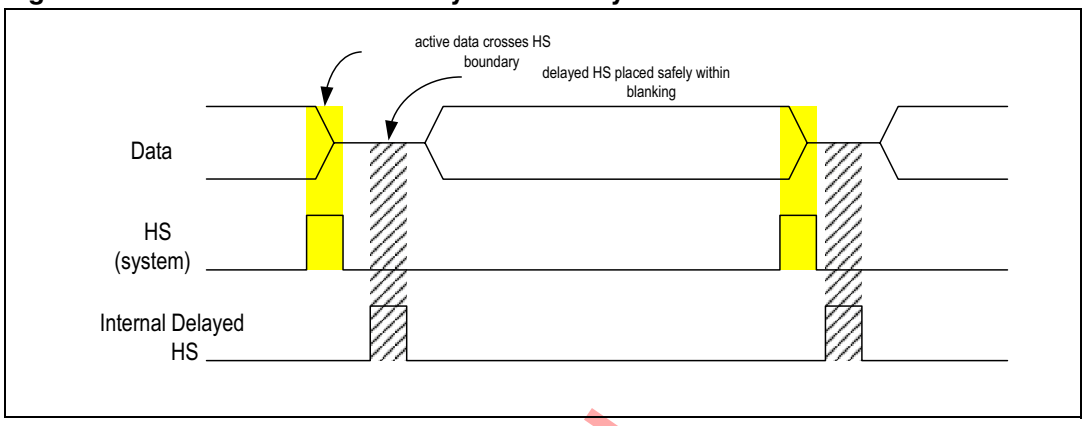
HSync is delayed by a programmed number of selected input clocks.

Figure 29. HSync delay



Delayed horizontal sync may be used to solve a problem with VSync jitter with respect to HSync. VSync and HSync are generally driven active with different paths to the Athena SoCs (HSync is often regenerated from a PLL). As a result, VSync may be seen earlier or later. Because VSync is used to reset the line counter and HSync is used to increment it, any difference in the relative position of HSync and VSync is seen on-screen as vertical jitter. By delaying the HSync a small amount, it can be ensured that VSync always resets the line counter prior to it being incremented by the “first” HSync.

Figure 30. Active data crosses HSync boundary



4.7.2 Capture block

The capture block involves framing of two selected (main & PIP) input videos for capture including the ADC capture vindow as explained in an earlier section. It is also responsible for driving the frame memory input capture clients.

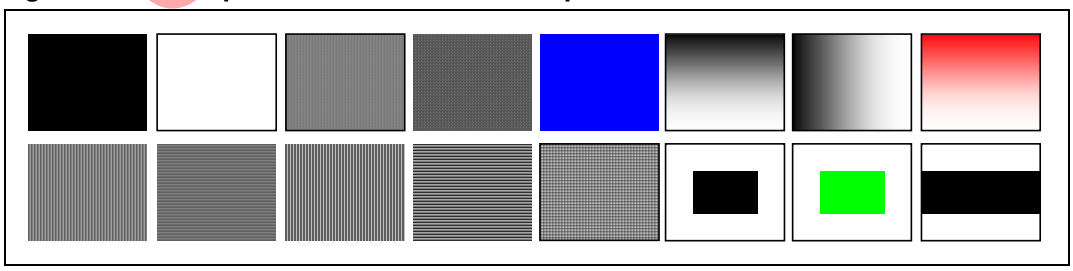
4.7.3 Image boundary detection

The Athena SoCs perform measurements to determine the image boundary. This information is used to program the active window and center the image.

4.7.4 Test Pattern Generator (TPG)

The Athena chips contain hundreds of test patterns, some of which are shown below. Once programmed, the test pattern generator can replace a video source (e.g. a PC) during factory calibration and test. This simplifies the test procedure and eliminates the possibility of image noise being injected into the system from the source. The foreground and background colors are programmable. In addition, the chip OSD controller can be used to produce other patterns.

Figure 31. Examples of Athena built-in test patterns



4.7.5 Input pixel & phase measurement

The Athena SoCs provide a number of pixel measurement functions intended to assist in configuring system parameters such as pixel clock, SDDS sample clocks per line and phase setting, centering the image, or adjusting the contrast and brightness.

The image phase measurement function measures the sampling phase quality over a selected active window region. This feature may be used when programming the source DDS to select the proper phase setting.

4.7.6 Instant Auto™

Instant Auto is used to perform consistant, accurate, rapid, image content independent, automatic adjustment of Htotal (clock) and phase for an incoming RGB signal. There are two algorithms: Htotal and Phase. Each of the algorithms is implemented partly in hardware and partly in firmware.

4.7.7 Letterbox detection

Letterbox detection uses a firmware algorithm with hardware logic to determine whether or not an input is letterbox format. This information is used to set up the image scaling hardware to maximize display viewing area for various inputs videos, while preserving the aspect ratio.

4.7.8 Active video window detection

Active video window detection uses a firmware algorithm with hardware logic to detect an active video content on a digital input from a PC source. The detected video window frame is used to create highlight window, inside or outside which, various image enhancement techniques including noise filter, sharpness enhancement, contrast enhancement, color enhancement and gamma control can be applied.

4.7.9 Noise reduction and signal conditioning

This block performs temporal and MPEG noise reduction and color conversion for capture.

3D/TNR noise reduction

3D noise reduction is implemented by applying temporal (inter-field) and spatial (intra-field) noise reduction filters to the video data.Temporal Noise Reduction (TNR) coefficients are a function of both luma and chroma channel motion values. In addition, the Athena SoCs have LUTs so that NR coefficients may be chosen based on the raw Luma value as well. The temporal NR block for the Athena chips also supports Noise Reduction of the Fleshtone regions. Due to Chroma motion detection in the NR block, color smearing can be avoided during NR.

A motion-adaptive frame-based recursive noise reduction is performed on both the chroma and luma data. An innovative noise meter measures the amount of noise in the backporch region without any serrations. The recursive filter values are selected based on the degree of noise present and motion sensitivity defined. The degree of sensitivity to motion is programmable.

Facial features may be adversely affected if the noise reduction done on such areas uses the recursive filter levels optimized for the overall picture. To prevent this and to provide a more natural picture, flesh tones are identified and when they are present, the noise reduction algorithm is modified. Furthermore, the TNR block helps to remove the noise without introducing image tearing artifacts.

Media noise reduction

The media noise reduction block removes unwanted ringing and block noise from images that have undergone MPEG or JPEG compression and decompression. This feature is only available on the main video path, The two types of media noise that Athena SoCs can reduce are:

- Block Noise: MPEG encoders, in the presence of an almost flat area, can create a squared structure due to the discrete 8x8 squares that are used in the MPEG compression process. This creates a noticeable squared structure in the image. The Athena SoCs smoothen these square boundaries so they are not visible. The amount of smoothening is programmable between neighboring pixel values that will be smoothened. The amount of smoothening starts to decrease linearly from the maximum (defined by T0) to 0 (defined by 2 x T0) to avoid the hard switch effect of the smoothening applied.
- Mosquito Noise: The Athena SoCs smoothen checker box and discrete noise artifacts referred to as “mosquito noise” around large edge transitions caused by MPEG encoders. The smoothening level is programmable.

Removal of Chroma up-sampling error

The Athena SoCs have the ability to remove the Chroma Up-Sampling Error (CUE) or “chroma bug” found in many DVD players on the market today. This feature fixes the errors on many DVD players by up-sampling the 4:2:0 MPEG stream to a 4:2:2 sequence required for display video processing.

Input color conversion

The color conversion block allows video capture in RGB or YUV color spaces including wide gamut formats such as xvYCC or Adobe-RGB.

4.8 3D format capture and processing

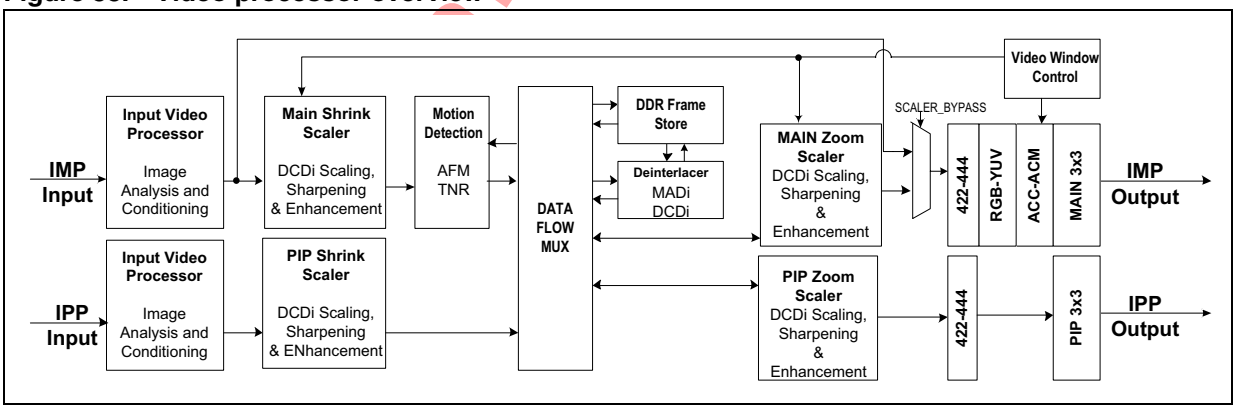
The Athena SoCs support capture and frame rate conversion various 3D formats from DisplayPort, HDMI and dual-DVI inputs.

Figure 32. 3D format capture and processing

	3D FORMAT	Input Timing	Frame Interleaved - 1080P Panel		Line Interleaved
			VS_{OUT}= 95.92 Hz / 96Hz	VS_{OUT} =120Hz / 100Hz	VS_{OUT} = VS_{IN} OR VS_{OUT} = 2x VS_{IN}
HDMI1.4	Frame Packing: 3D_STRUCTURE=0x0, VIC= 31	1920x1080p @ 50Hz	×	√ 2x VS_{OUT} = VS_{IN}	√
	Frame Packing: 3D_STRUCTURE=0x0, VIC= 16	1920x1080p @ 60Hz	×	√ 2x VS_{OUT} = VS_{IN}	√
	Frame Packing: 3D_STRUCTURE=0x0, VIC= 32	1920 x 1080p @23.98/24Hz	√ 2x VS_{OUT} = VS_{IN}	√ 10x VS_{OUT} = 4x VS_{IN}	√
	Frame Packing: 3D_STRUCTURE=0x0, VIC= 4	1280 x 720p @59.94/ 60Hz	×	√ 2x VS_{OUT} = VS_{IN}	√
	Frame Packing: 3D_STRUCTURE=0x0, VIC= 19	1280 x 720p @50Hz	×	√ 2x VS_{OUT} = VS_{IN}	√
	Line Alternative: 3D_STRUCTURE=0x2, VIC= 16	1920x1080p @ 50Hz	×	√ 2x VS_{OUT} = VS_{IN}	√
	Line Alternative: 3D_STRUCTURE=0x2, VIC= 31	1920x1080p @ 60Hz	×	√ 2x VS_{OUT} = VS_{IN}	√
	Side by Side (Half): 3D_STRUCTURE=0x8, VIC= 5	1920 x 1080i @59.94/60Hz	×	√ 2x VS_{OUT} = VS_{IN}	√
	Side by Side (Half) : 3D_STRUCTURE=0x8, VIC= 20	1920 x 1080i @50Hz	×	√ 2x VS_{OUT} = VS_{IN}	√
	Top and Bottom: 3D_STRUCTURE=0x6, VIC= 32	1920 x 1080p @23.98/24Hz	√ 4x VS_{OUT} = VS_{IN}	√ 20x VS_{OUT} = 4xVS_{IN}	√
	Top and Bottom: 3D_STRUCTURE=0x6, VIC= 4	1280 x 720p @59.94 / 60Hz	×	√ 2x VS_{OUT} = VS_{IN}	√
	Top and Bottom: 3D_STRUCTURE=0x6, VIC= 19	1920 x 1080p @60Hz	×	√ VS_{OUT}=VS_{IN} x 2	√
DP1.2	Stacked Top Bottom: VSC=0x02	1920 x 1080p @23.98/24Hz	√ 2x VS_{OUT} = VS_{IN}	√ 5xVS_{OUT}= 4x VS_{IN}	√
	Stacked Top Bottom: VSC=0x02	1280 x 720p @59.94 / 60Hz	×	√ 2x VS_{OUT} = VS_{IN}	√
	Stacked Top Bottom: VSC=0x02	1280 x 720p @50Hz	×	√ 2x VS_{OUT} = VS_{IN}	√
	Side by Side (Half): VSC=0x04 or 0x14,	1920 x 1080i @59.94/60Hz	×	√ 2x VS_{OUT} = VS_{IN}	√
	Side by Side (Half): VSC=0x04 or 0x14	1920 x 1080i @50Hz	×	√ 2x VS_{OUT} = VS_{IN}	√
	Frame SEQ: VSC=0x01 or 0x11 or 0x21	1920 x 1080p @120Hz	×	√ VS_{OUT} = VS_{IN}	√VS_{OUT}=VS_{IN}
	Line Interleaved: VSC= 0x03 or 0x13	1920 x 1080p @60Hz	×	×	√
Dual DVI	Frame Sequential NVidia 3D	1920 x 1080p 120Hz 3D	×	√ VS_{OUT} = VS_{IN}	√VS_{OUT}=VS_{IN}
	Frame Sequential NVidia 3D	1680 x 1050p 120Hz 3D	×	√ VS_{OUT} = VS_{IN}	√VS_{OUT}=VS_{IN}
	Frame Sequential Increased back-Porch 3D	1680 x 1050p 120Hz 3D	×	√ VS_{OUT} = VS_{IN}	√VS_{OUT}=VS_{IN}

4.9 DCDi® by Faroudja® video processing

Figure 33. Video processor overview



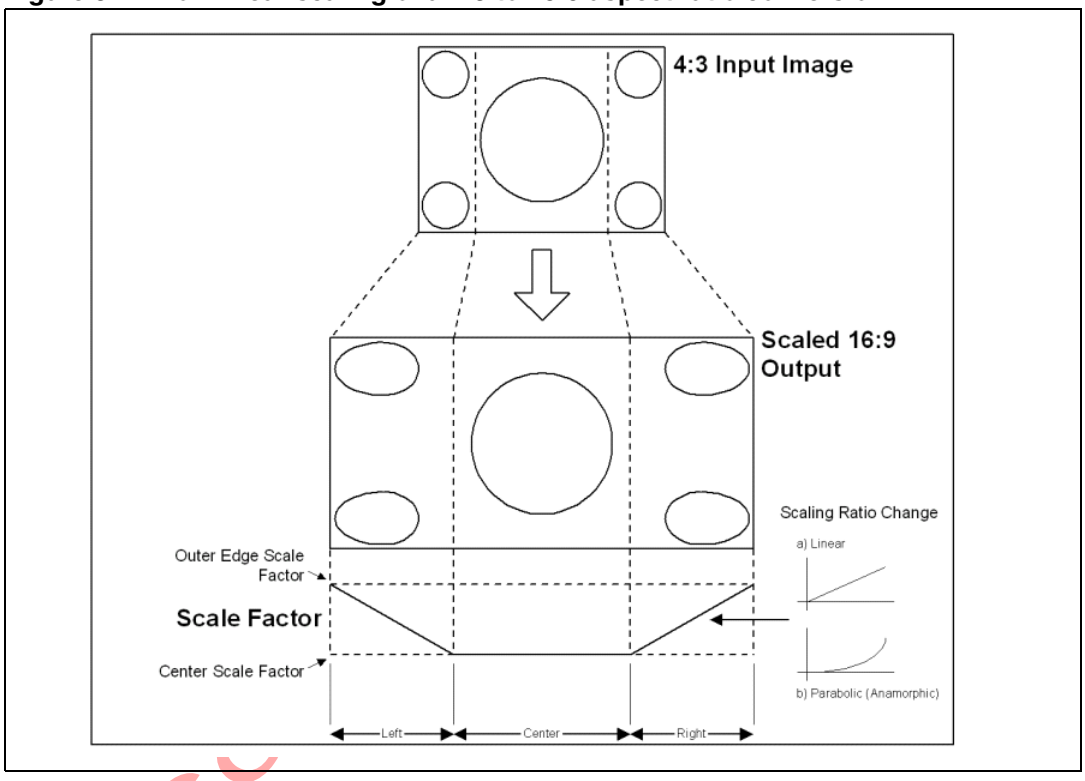
4.9.1 Format and aspect ratio conversion—scaling

The Athena SoCs' dual zoom/shrink scalers (main channel & PIP channel) use an advanced polyphase scaling technique. They provide simultaneous high quality scaling of real-time video images and graphics on both channels. An input field/frame is scalable arbitrarily in both the vertical and horizontal dimensions. The scaler can support a maximum horizontal active of 2560 pixels. The scaler's input pixel depth is 10-bit/color. Its output pixel depth is 12 bits.

Aspect ratio conversion and non-linear scaling

The input image is separated into three zones horizontally: left, center, and right. The center zone is scaled at a programmable fixed ratio. The left and right zones have a programmable changing scale factor that changes from left to right (see figure below). The scale ratio change can either be linear or parabolic. Both main and PIP scalers support aspect ratio conversion.

Figure 34. Non-linear scaling of a 4:3 to 16:9 aspect ratio conversion



Note: A conversion for 16:9 to 4:3 aspect ratio would use the same method with an inverse parabolic ratio for the scale factor of the left and right zones.

4.9.2 Dynamic scaling and animation

The Athena SoCs have an advanced scaling engine that can support dynamic scaling of video without producing any judder or dropper of frames during the video sequence. Advanced synchronization hardware aligns the video to produce smooth resizing of the image.

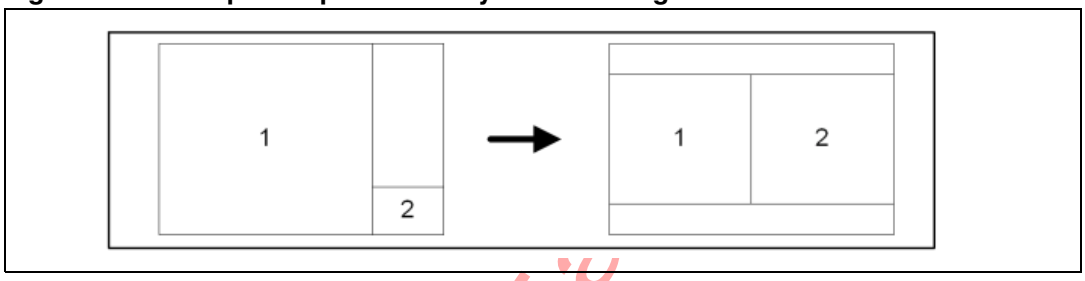
With split screen dynamic scaling, two windows are shown on the display (as with Picture by Picture [PBP]) with the ability to change the size of the selected window through +/- keys on the remote control.

The Athena SoCs allow for very flexible PIP display configurations whereby either the graphics or the video channel may act as the PIP source to overlay over the other channel. Single PIP allows the PIP display to be placed arbitrarily in the display window. It can be placed within the main display, partially overlapped with main display, or fully detached from Main display. The size of the PIP display is fully programmable. Also, single PIP display

allows 16 levels of alpha blending within the PIP window either with a specified background color or the main channel. A special case of single PIP display is side-by-side configuration.

Using external memory, the second channel image data can be frame-rate converted so that it matches the refresh rate of the main image and can subsequently be merged in various picture arrangements. The frame rate conversion of the second channel ensures no frame tear is present in the PIP channel video.

Figure 35. Example of split-screen dynamic scaling



4.9.3 Inverse 3:2/2:2 pull-down de-interlacing

Video graphics with 3:2/2:2 field sequences are processed with the built-in adaptive film mode controller. The field sequence is first detected by examining the field motion values and once a field sequence is identified, the corresponding film mode processing is applied. This feature is available only on the main scaling path.

4.9.4 Adaptive media display (3:3 and 2:2 film modes)

The Athena SoCs have the ability to take 3:2 film sequences of 24 Hz original film content and convert this to an output of 48 Hz or 72 Hz vertical refresh rate. This feature reduces the noticeable uneven judder seen on a 3:2 film sequence that is converted to 60 Hz vertical refresh rate. This feature is only available on the main scaling path.

4.9.5 Motion Adaptive De-Interlacing (MADi)

Motion adaptive de-interlacing in the Athena SoCs is a pixel-based two-phase process. Phase 1 involves the detection of motion and the generation of a motion value for each pixel. These pixel motion values are used as a measure of the current “degree of motion”. In Phase 2, the pixel motion values are used to select the appropriate de-interlacing technique. As a result, areas of an image that are not moving will be fully static (flicker free) and moving objects will have smooth edges. This feature is only available on the main scaling path.

4.9.6 DCDi® by Faroudja low-angle diagonal interpolation

In addition to the advanced de-interlacing capabilities mentioned in the previous sections, further image enhancement is achieved by applying special processing to a moving low-angle diagonal pattern in a video image.

For motion video, the intra-field interpolation is done using the patented and highly acclaimed DCDi® (Directional Correlational De-interlacing) algorithm by Faroudja®. DCDi® by Faroudja computes and tracks the angles of edges and uses this information to optimally fill in the missing pixels, removing jagged edge artifacts. The PIP channel supports a reduced version of DCDI.

4.9.7 Video enhancement

Main channel sharpening filters

The Athena SoCs provide a sharpness control system for both the luminance and the chrominance based on filtering. It includes a programmable noise coring function which is used to control noise amplification as well as a non-linear shaper to control the sharpness level in different amplitude ranges. The amount of sharpness is controlled by the independent programmable horizontal and vertical gains.The sharpness system for Athena SoCs support advanced peaking filters which help to improve sharpness without increasing noise.The main channel sharpness filters can be applied within the active video window.

PIP channel sharpening filters

The sharpening filters are duplicated on the PIP channel which allows the user to independently enhance the second channel video to a level different from the Main channel. The PIP channel also contains a programmable noise coring function.

Faroudja® TrueLife™ non-linear enhancement

The Faroudja® TrueLife™ non-linear enhancer provides a non-linear edge enhancement of both chrominance and luminance to give video images a more realistic and life-like appearance. The system provides independent controls for “small” and “large” horizontal and vertical luminance edge enhancement as well as “small” and “large” horizontal and vertical chrominance edge enhancement. The system includes a noise coring function that is controlled by means of a “noise threshold”.

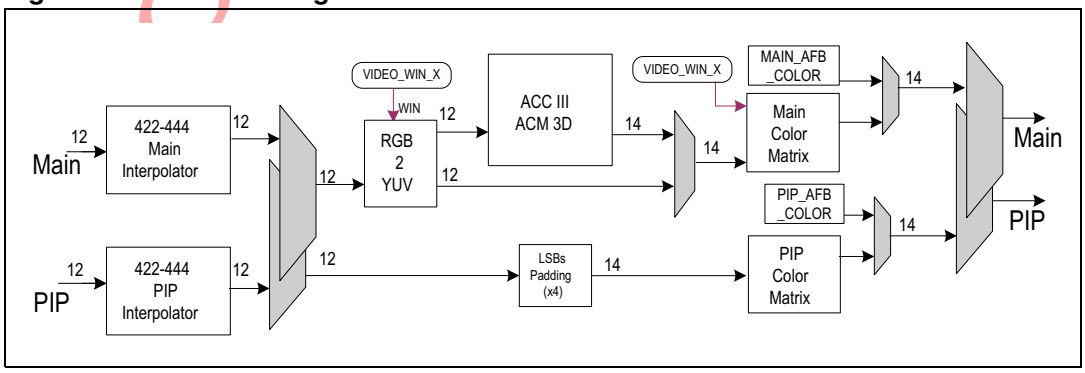
The edge enhancement engine can be combined with the sharpness filters engine to increase flexibility in the customization of the sharpness system.

The edge enhancement can be applied within the active video window.

Advanced digital color controls

The advanced digital color controls consist of the block in the following diagram.

Figure 36. Advanced digital color control block



ACC3-ACM3D

ACC3-ACM3D is the next generation Faroudja RealColor® enhancer. It features the following:

- Increased precision 14-bit datapath
- Programmable full frame and local zone histogram optimization
- 64 bin histogram sampling: more accurate control without contouring or flicker
- Luma to chroma tracking: insures proper color levels as contrast ratio is improved
- ACM-3D driven chroma to luma tracking: allows for skin tone compensation
- Scene change detection: accurate ACC tracking even with fast edits

The Enhancement can be applied over the full display area or over a Highlight Window. The Highlight Window can be driven by the Active_Video_Window_Detection.

4.9.8 Active Color Management–3D™ (ACM-3D)

Active Color Management-3D provides accurate control of global color parameters like hue, saturation, contrast, and local color changes such as skin tone adjustment or green enhance.

ACM-3D can be applied within a highlight window or over the full display area. The ACM-3D feature for the Athena SoCs provides three dimensional color controls for Y, U, and V signals for a particular color component.

The enhancement can be applied over the full display area or over a highlight window. The highlight window can be driven by the active video window detection.

Flesh tone correction

A function of the ACM-3D block, the dedicated flesh tone correction feature has been added to ensure flesh tones are reproduced accurately. Without flesh tone compensation, some video processing techniques may manipulate flesh tone shades incorrectly.

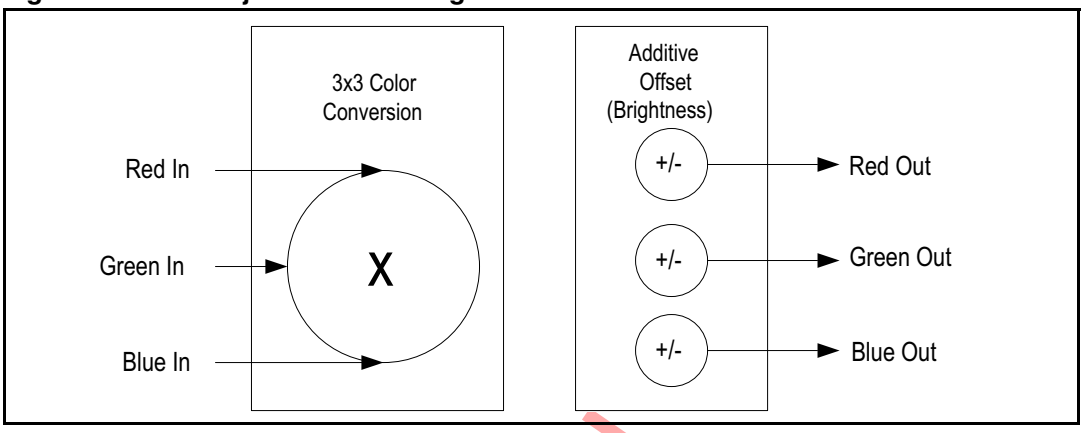
Blue stretch

Another function of the ACM-3D block is the blue stretch system. The blue stretch system analyzes and manipulates the white point of the incoming signal in order to shift the color temperature towards blue. A bluer white point is considered beneficial by some viewers. The amount of blue stretch is programmable.

Faroudja RealColor® control

The Athena SoCs provide high-quality digital color controls that can be applied independently to the video and RGB data streams. These consist of a full 3x3 RGB matrix multiplication stage, followed by a signed offset stage as shown below in the following figure.

Figure 37. Faroudja RealColor® digital color controls



This structure can accommodate all RGB color controls such as contrast (multiplicative stage) and brightness (signed additive offset). In addition, it supports all YUV color controls including brightness (additive factor applied to Y), contrast (multiplicative factor applied to Y), hue (rotation of U and V through an angle), and saturation (multiplicative factor applied to both Y and V). To provide the highest color purity, all mathematical functions use 14 bits of accuracy.

Six-axis color control

The Athena ICs implement hardware based six-axis color control through the color-warping engine (which is part of the dual-gamma block). This engine allows independent control of each of the color six component vertices (RGBCYM) and white-point.

Each color corner maps to a dedicated color filter. The color warping engine transforms 3D linear RGB color space into six adjacent 3D vector subspaces. Based on the slider bar control settings provided to the user for vertex adjustment, each vertex may be shifted in color space. In response, the color coefficients of the 3x3 matrix in the dual-gamma block will be dynamically modified.

Display uniformity control

The Athena SoCs support non-linearity of display uniformity (flatness) compensation by applying a region based gain correction of RGB data over the entire screen. The corrections are done in the light-linear space after de-gamma. The screen can be broken up into multiple regions with RGB coefficients available for each of these regions. Measurements are made on the screen using an off-line calibration tool. After analysis for flatness, the tool generates compensation data for each region. These coefficients are downloaded into system flash memory for use by the display uniformity compensation hardware, during run time. This calibration is performed in factory, on a per-unit basis.

4.10 Frame store interface

The external frame buffer provides the storage required for the frame rate conversion process, image enhancement processing, and the integrated OSD.

The integrated memory controller arbitrates and controls the writing/reading of video data to/from the external memory. Input video data is written into the frame buffer for processing and display data is read back from the frame buffer. Frame buffer addresses are fully

programmable so as to provide flexibility for memory allocation of main and PIP display. This flexibility also allows the implementation of various multiple PIP display configurations.

The Athena SoCs can store 8 bpp or 10 bpp in memory for RGB or YUV 4:2:2.

4.10.1 Supported DDR devices

The Athena SoCs operate seamlessly with most commercially available DDR2 and DDR3 devices. The frame store interface is 16 or 32 bits wide and can support 1x16, 2x16, 1x32 devices. The interface speed will support DDR2-1066 and DDR3-1066 devices.

The maximum amount of memory space that is addressable by the Athena SoCs is 256 MByte. This corresponds to two 64 M x 16 devices.

Note: Adherence to STMicroelectronics design guidelines for the PCB is recommended, especially with regards to DDR-related parts.

4.10.2 DDR estimates

The DDR estimates for various Athena devices and panel sizes are as given below.

Table 5. STDP73xx DDR speed estimates

Device	DDR width	Panel size	PIP	Max input freq	Max Main BPC	Max PIP H-size	Max PIP V-size	Max PIP BPC	Required DDR devices
STDP73XX	x16	1600_1200/60Hz	NO	210 MHz	8	0	0	-	DDR2/3-667
STDP73XX	x16	1600_1200/60Hz	NO	210 MHz	10	0	0	-	DDR2/3-800
STDP73XX	x16	1600_1200/60Hz	YES	210 MHz	10	924	520	10	DDR2/3-1066
STDP73XX	x16	1680_1050/60Hz	NO	210 MHz	10	0	0	-	DDR2/3-667
STDP73XX	x16	1680_1050/60Hz	YES	210 MHz	10	1188	742	10	DDR2/3-1066
STDP73XX	x16	1920*1080 /60Hz	NO	210 MHz	10	0	0	-	DDR2/3-667
STDP73XX	x16	1920*1080 /60Hz	YES	210 MHz	10	1358	764	10	DDR2/3-1066
STDP73XX	x16	1920*1200/60Hz	NO	210 MHz	10	0	0	-	DDR2/3-800
STDP73XX	x16	1920*1200/60Hz	YES	210 MHz	10	960	600	8	DDR2/3-1066
STDP73XX	x16	1920*1200/60Hz	YES	210 MHz	8	1358	849	8	DDR2/3-1066

Table 6. STDP93xx/STDP92xx DDR speed estimates

Device	DDR width	Panel size	PIP	Max input freq	Max Main BPC	Max PIP H-size	Max PIP V-size	Max PIP BPC	Required DDR devices
STDP9XXX	x16	2048*1156/60Hz	No	210 MHz	8	0	0	-	DDR2/3-800
STDP9XXX	x16	2048*1536/60Hz	No	210 MHz	8	0	0	-	DDR2/3-1066
STDP9XXX	x16	2560*1440/60Hz	No	270 MHz	8	0	0	-	DDR2/3-1066
STDP9XXX	x16	2560*1600/60Hz	No	270 MHz	8	0	0	-	DDR2/3-1066
STDP9XXX	X32	1920*1080/120Hz, 300MHz	No	300 MHz	10	-	-	-	DDR2/3-800
STDP9XXX	X32	1920*1080/120Hz, 400MHz	No	300 MHz	10	-	-	-	DDR2/3-1066
STDP9XXX	X32	2048*1536/60Hz	Yes	300 MHz	10	1182	887	10	DDR2/3-800
STDP9XXX	X32	2560*1440/60Hz	Yes	300 MHz	10	1280	831	10	DDR2/3-1066
STDP9XXX	X32	2560*1600/60Hz	Yes	300 MHz	10	1478	924	8	DDR2/3-1066

DDR memory size estimates

The table below summarizes approximate DDR buffer sizes for various applications. The actual sizes may vary depending on the application requirement.

Figure 38. DDR buffer sizes

	MAIN SIZE					PIP SIZE					OVERDR	OSD SIZE					OCM	AUDIO	TOTAL	32Mx 16
PANEL	H	V	BPP	Qty	Total	H	V	BPP	Qty	Total	SIZE	H	V	BPP	Qty	Total	SIZE	SIZE	SIZE	DDR's Qty.
QHD 16:10	2560	1600	30	3	44 MB	1920	1080	30	4	30 MB	9 MB	1920	1080	8	2	4 MB	4 MB	4 MB	**94 MB**	**2**
QHD 16:9	2560	1440	30	3	40 MB	1920	1080	30	4	30 MB	8 MB	1920	1080	8	2	4 MB	4 MB	4 MB	**89 MB**	**2**
QXGA	2048	1536	30	3	34 MB	2048	1536	30	4	45 MB	7 MB	1920	1080	8	2	4 MB	4 MB	4 MB	**97 MB**	**2**
WUXGA	1920	1200	30	3	25 MB	1920	1080	30	4	30 MB	5 MB	1920	1200	8	2	4 MB	4 MB	4 MB	**72 MB**	**2**
FHD 3D	1920	1080	30	6	44 MB	1920	1080	30	4	30 MB	9 MB	1920	1080	8	2	4 MB	4 MB	4 MB	**95 MB**	**2**
FHD	1920	1080	30	3	22 MB	1920	1080	24	4	24 MB	4 MB	1920	1080	8	2	4 MB	4 MB	4 MB	**62 MB**	**1**
UXGA	1600	1200	30	3	21 MB	1600	1200	30	4	27 MB	4 MB	1600	1200	8	2	4 MB	4 MB	4 MB	**64 MB**	**1**
SXGA+	1680	1050	30	3	19 MB	1680	1050	30	4	25 MB	4 MB	1680	1050	8	2	3 MB	4 MB	4 MB	**59 MB**	**1**

4.10.3 Adjustable frame store interface parameters

The Athena SoCs provide a full set of registers to optimize the timing parameters for a particular memory interface. Most will not require adjustment as the chips automate the process of initialization.

4.10.4 DDR memory power-on and initialization sequence

DDR devices have power-on and initialization sequences that must be performed before they can be reliably accessed. The Athena SoCs automatically perform these sequences.

4.10.5 DDR memory power down

DDR devices typically have a low power, non-operational mode. The Athena SoCs support this feature by providing a power down sequence.

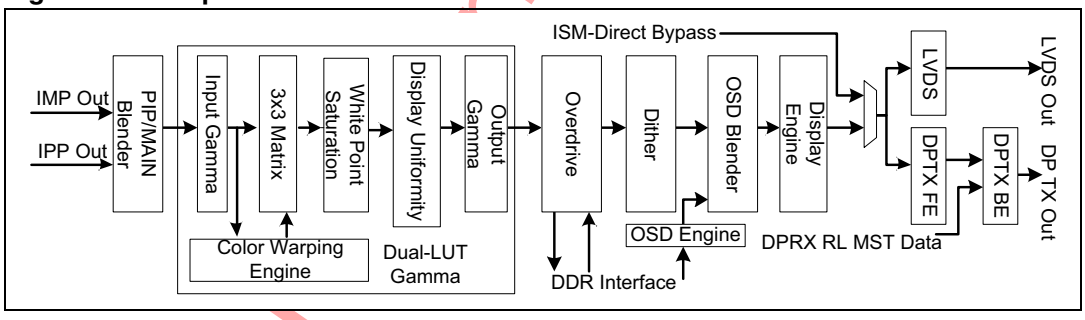
4.10.6 Freeze frame

Freeze frame capability is made available by disabling the input capture during the vertical blanking interval. This does not disrupt the flow of data from the frame store. During freeze frame, adjustments made to the contrast and brightness controls will still have an effect on the displayed image.

4.11 Output data processing

The output data processing is responsible for PIP overlay blending, color correction, gamma, panel calibration instrumentation, backlight uniformity correction LCD response time enhancement, OSD overlay blending and panel interface. The dataflow is as shown below.

Figure 39. Output data flow



4.11.1 PIP blender

The Athena SoCs allow for very flexible PIP display configurations whereby either the graphics or the video channel may act as the PIP source to overlay over the other channel. Single PIP allows the PIP display to be placed arbitrarily in the display window. It can be placed within the main display, partially overlapped with main display, or fully detached from main display. The size of the PIP display is fully programmable. Also, single PIP display allows 16 levels of alpha blending within the PIP window either with a specified background color or the main channel. A special case of single PIP display is side-by-side configuration. Using external memory, the second channel image data can be frame-rate converted so that it matches the refresh rate of the main image and can subsequently be merged in various picture arrangements. The frame rate conversion of the second channel ensures no frame tear is present in the PIP channel video. The PIP channel contains advanced video processing including DCDi low angle processing and sharpening filters to provide a high quality image, even on the second channel.

4.11.2 Athena PIP matrix

The Athena SoCs support simultaneous capture (and PIP/PBP etc) between all independent input ports. The video analog front end which has 2:1 Mux on its two input

ports is an exception. Simultaneous capture between these two ports is not possible. The table below summarizes the PIP matrix.

Figure 40. PIP matrix

MAIN / PIP	COMBO_PHY0	COMBO_PHY1	COMBO_PHY2	COMBO1+ COMBO2 (DUAL-DVI)	ANALOG VGA PORT	COMPONENT VIDEO	TTL VXI PORT
COMBO_PHY0	×	✓	✓	✓ (93XX-92XX ONLY)	✓	✓	✓ (93XX-92XX ONLY)
COMBO_PHY1	✓	×	✓	×	✓	✓	✓ (93XX-92XX ONLY)
COMBO2 PHY	✓	✓	×	×	✓	✓	✓ (93XX-92XX ONLY)
COMBO1 + COMBO2 (DUAL-DVI)	✓ (93XX-92XX ONLY)	×	×	×	✓	✓	✓ (93XX-92XX ONLY)
VGA PORT	✓	✓	✓	✓	×	×	✓ (93XX-92XX ONLY)
COMPONENT VIDEO	✓	✓	✓	✓	×	×	✓ (93XX-92XX ONLY)
TTL VXI PORT	✓ (93XX-92XX ONLY)	✓ (93XX-92XX ONLY)	✓ (93XX-92XX ONLY)	✓ (93XX-92XX ONLY)	✓ (93XX-92XX ONLY)	✓ (93XX-92XX ONLY)	×

4.11.3 Multi-PIP

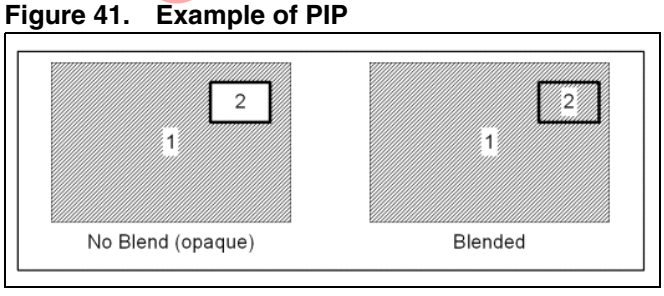
Multiple PIP displays allow a number of PIP windows to be displayed at the same time depending on display pixel resolution. The main and one PIP window will be running in real time. PIP size in multi-PIP mode is adjustable.

There are up to 16 PIP windows available simultaneously, however only one might be active. All windows should be aligned to the 4x4 grid. Default software application uses multiple PIP windows to display different channels. Windows are aligned as shown in the diagram below.

4.11.4 PIP border and blending

The PIP display mode consists of two windows with one smaller window sitting on top of the other. This smaller window is called the PIP window. Its size and position are fully programmable up to the entire display size. The transparency (blend) level of the PIP window is adjustable up to 16 levels.

Figure 41. Example of PIP



The Athena SoCs have hardware support for the PIP border. In single and multi-PIP modes, the PIP border size, color, and on/off status is programmable for each PIP window. An independent highlight window can also be programmed to be used primarily for highlighting the active PIP window in a multi-PIP system.

4.11.5 Dual LUT gamma

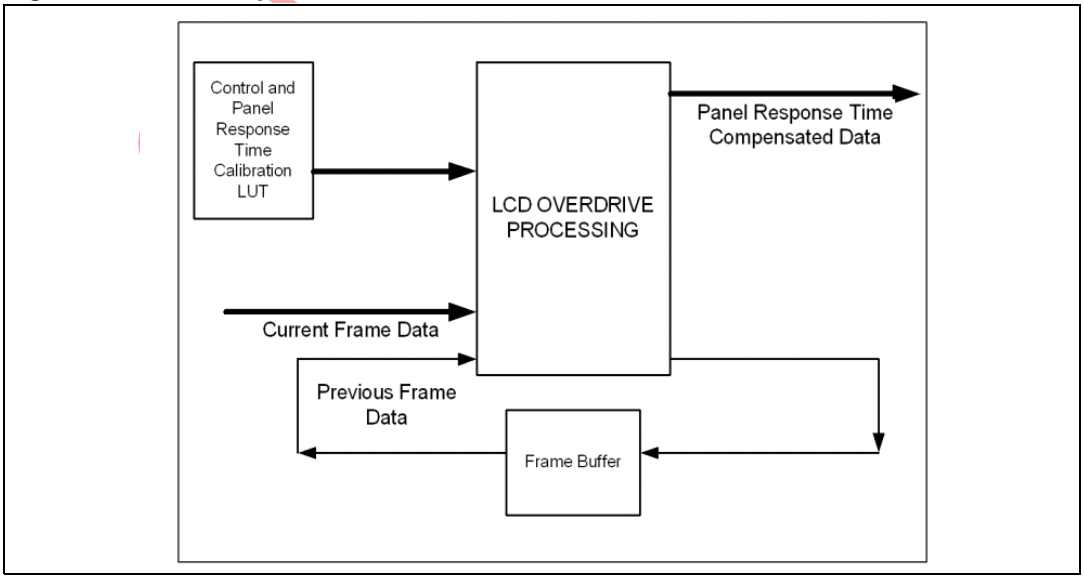
The Athena SoCs provide dual 14-bit Look-Up Tables (LUT) for each input color channel intended for gamut remapping and gamma correction. A 14-bit data path results in an improved color depth control. The 3x3 matrix allows color-space conversion for panel gamut remapping. The matrix coefficients and the input and output gamma entries are created using an off-line tool. This process can be used for unit-by-unit panel calibration using QuickMatch2® algorithm. In addition, the color coefficients can be dynamically modified through the color warping engine explained in an earlier section). This logic allows dynamic, user interactive 6-axis color correction. The gamma LUT's and the color matrix can be applied over the entire screen on a highlight window, the coordinates for which are generated by the active video window detection feature. The dual-LUT module can also compensate for any color non-linearity of display uniformity (flatness) by applying a region based gain correction of RGB data over the entire screen. The calibration is done using an off-line tool on a per-unit basis.

4.11.6 LCD response time enhancement

The Athena SoCs provide an LCD panel response time enhancement system. The LCD overdrive recursive engine is constituted by a programmable LUT which is generated after measuring the response of the panel to be used. The LUT is used by the overdrive engine to manipulate the pixels at the output in such a way that the panel response is improved, therefore, reducing the image smearing due to poor panel response. The response time enhancement can be temperature compensated and can also be optimized for 3D interfaces.

Note: The LCD panel response time enhancement system utilizes considerable bandwidth. Bandwidth consideration must be taken before utilizing LCD overdrive processing as other chip features may need to be disabled.

Figure 42. LCD response time enhancement



4.11.7 ODP dither engine

The dither engine on the output data path provides up to 4-bit dither on the panel data. The dither can be programmed to specific patterns on a spatial and temporal basis to optimize its performance to suit specific panel characteristics.

4.12 Display output interface

The display output port provides data and control signals that permit the chips to connect to a variety of display devices using a DisplayPort or LVDS interfaces. The output interface is configurable for LVDS in 18, 24, or 30-bit RGB pixel format in single or double or quad-wide formats. DisplayPort output can be eDP/iDP or standard DisplayPort in compliance with DP1.2 Specification. Fast-Aux feature is not supported.

On the LVDS interface, all display data and timing signals are synchronous with the DCLK output clock. The integrated LVDS transmitter is programmable to allow the data and control signals to be re-mapped to support all common LVDS receiver formats.

DisplayPort and LVDS can be turned on simultaneously . The maximum DCLK speed is 400MHz. The table below summarizes the display output interface support.

Figure 43. Display output interface support

PART NUMBER	COMMENT	OUTPUTS			
		DUAL LVDS	QUAD LVDS	eDP / iDP	DP1.2 / MST
STDP9320	WQXGA, DP1.2 MST , Quad LVDS, 32b DDR	✓	✓	✓	✓
STDP9310	WQXGA Quad LVDS Out, 32b DDR	✓	✓	✓	✗
STDP9210	FHD 120Hz 3D, Quad LVDS, 32b DDR	✓	✓	✓	✗
STDP7320	WUXGA, DP1.2 MST, Dual LVDS, 16b DDR	✓	✗	✓	✓
STDP7310	WUXGA, eDP / iDP Out, Dual LVDS, 16b DDR	✓	✗	✓	✗

4.12.1 Frame rate conversion and display synchronization

The display synchronization modes are:

- Frame sync mode: The display frame rate is synchronized to the input frame or field rate. This mode is used for standard operation. Frame rate conversion is optionally performed. The display frame can be locked to the Main or the PIP channel.
- Free run mode: (no synchronization) This mode is used when there is no valid input timing (i.e. to display OSD messages or a splash screen) or for testing purposes. In free-run mode, the display timing is determined only by the values programmed into the display window and timing registers.
- DFL mode: (Dynamic Frame Lock) The goal of this mode is to slowly lock the display to the input whenever the difference between the input and output timing is smaller than the maximum threshold [DFL_MAX_ERR_CORR], otherwise the synchronizer just free runs. In order to achieve this goal, the block will perform two types of measurement. First, it measures the difference between input and output period. Second the input-output phase difference. After taking the measurements, compare between the period

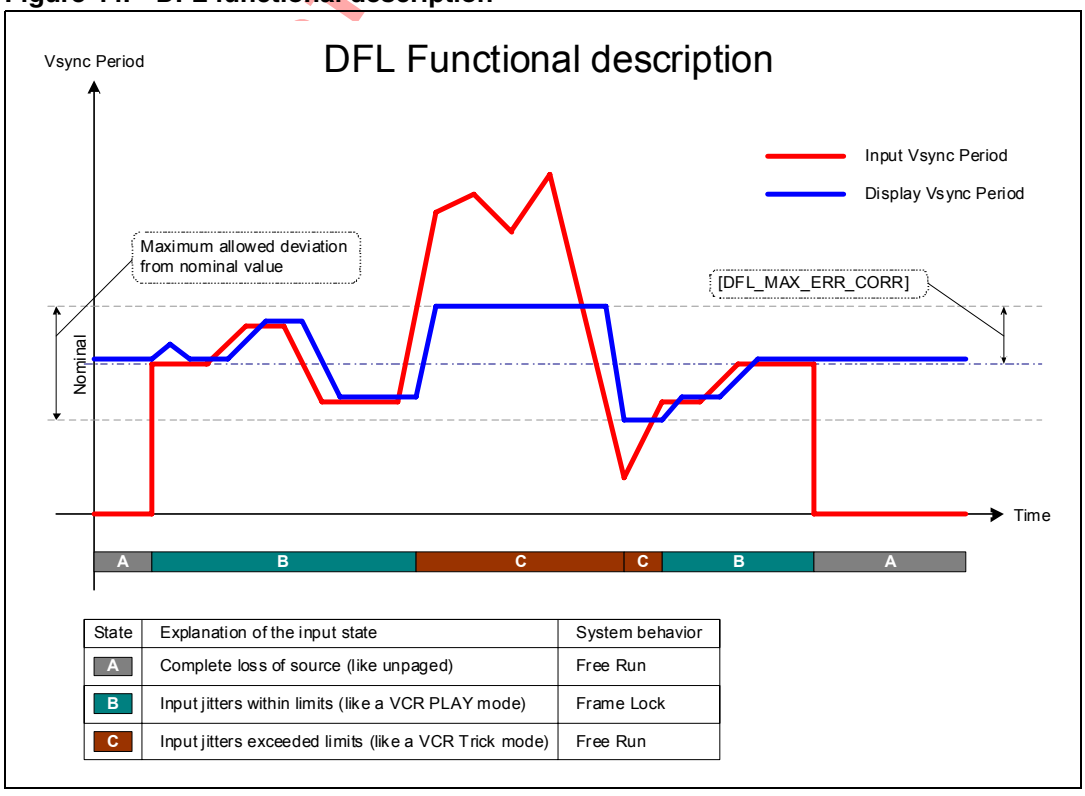
error and the maximum allowed correction (in pixels) [DFL_MAX_ERR_CORR]. Based on this comparison do one of the following:

– When the period error is smaller than the maximum error correction, which means that the input-output timing difference is small (achievable), the display synchronizer will start adding/dropping pixels and/or lines in a predefined locations using the measured phase error (adding/dropping pixels can be done per line in the vertical front porch or in every line). The total horizontal and vertical correction should not exceed the maximum allowed correction ([DFL_H_CORR_TOL], [DFL_V_CORR_TOL]) resulting in a successful locking. It may take some time before it reaches the desired phase.

– When the period error is greater than the maximum error correction, which means that the input-output timing difference is large enough. This cannot be corrected using the current tolerance limitation (it will output unusable timing). The display synchronizer will ignore the measured phase error and add (or drop) the maximum allowed correction per frame ([DFL_MAX_ERR_CORR]) which will get translated to a multiple [DFL_H_CORR_TOL] and one [DFL_V_CORR_TOL] every frame during the predefined locations (internally calculated). The system remains in this state until the input change and the error becomes small enough for the synchronizer to switch back to state A. It is also possible that the system will stay in this state because the input-output difference is large and not changing, which means that the display will never catch up with the input. During this mode, the display is not locked to the input and the display is in a free run mode. The new DTG total #pixel/frame = Host DTG total # pixel/frame +/- DFL_MAX_ERR_CORR.

DFL mode is mandatory for all cases where Display Clock (DCLK) exceeds 360 MHz.

Figure 44. DFL functional description



State	Explanation of the input state	System behavior
A	Complete loss of source (like unpaged)	Free Run
B	Input jitters within limits (like a VCR PLAY mode)	Frame Lock
C	Input jitters exceeded limits (like a VCR Trick mode)	Free Run

4.12.2 Stereo 3D frame rate conversion

The Athena SoCs support frame rate conversion of stereo 3D format inputs from HDMI1.4, DisplayPort1.2 or dual-DVI stereo formatted inputs and frame rate converts these to be suitable for display on either frame sequential or line interleaved type stereo LCD panels. The Athena SoCs also feature temporal dithering support for line interleaved panels.

Sync insertion, frame marking and buffer control logic allow conversion of multiple 3D formats to frame sequential or line interleaved formats. Interlaced 3D Inputs will not supported. 24 Hz 3D formats can either be frame doubled to 96 Hz or frame rate converted to 120 Hz.

4.12.3 Display timing programming

Display timing signals provide timing information so the display output interface can be connected to an external display device via a TTL or LVDS interface. Based on values programmed in registers, the display timing generator produces the horizontal sync (DHS), vertical sync (DVS), and data enable (DEN) control signals. The figure below provides the registers that define the output display timing.

Horizontal values are in single-pixel increments. When the display is in double wide mode, horizontal settings should use even numbers. Vertical values are programmed in line increments relative to the leading edge of the vertical sync signal.

Figure 45. Display windows and timing

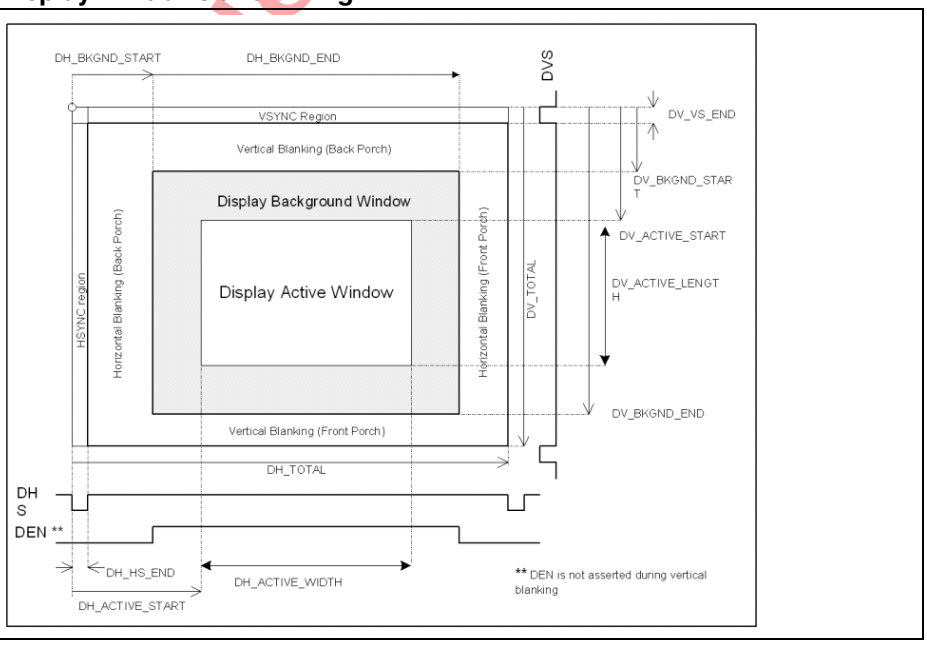
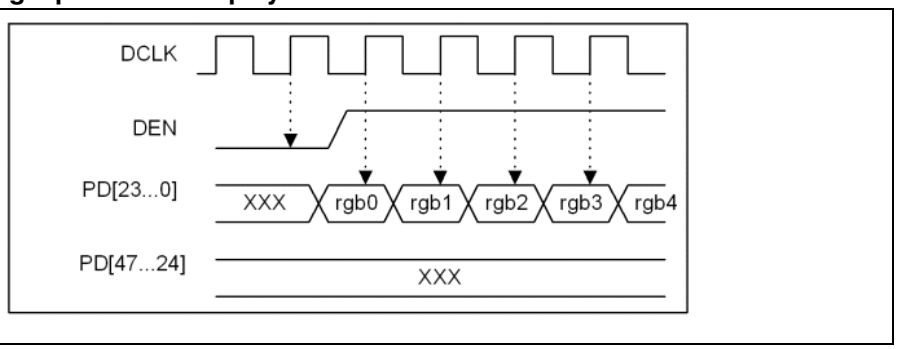


Figure 46. Single pixel wide display data



To improve routing on the system PCB, the Athena SoCs support swapping of display pixel data.

4.12.4 Output image flip

The Athena SoCs output data path support image flip (H-flip and V-flip).

4.12.5 Split LVDS drive

The Athena SoCs LVDS output can support left/right split LVDS output whereby the left half of the image is outputted on the LVDS A-B interface and simultaneously, the right half of the image is outputted on LVDS-C-D interface.

4.12.6 LVDS transmitter

Four LVDS links (A through D) are available on the output of the Athena ICs to transmit data and timing information to the display device (only A & B interfaces on the STDP72xx parts)

The Athena SoCs directly drive the standard LVDS interface panels, supporting all standard data formats with 18-bit, 24-bit, or 30-bit data output. The following diagrams illustrate the RGB, HSync, VSync, and data enable signal mapping in a single bus output configuration. The same formats holds for multi-link outputs.

Figure 47. Data mapping for LVDS output in 8-bit config.

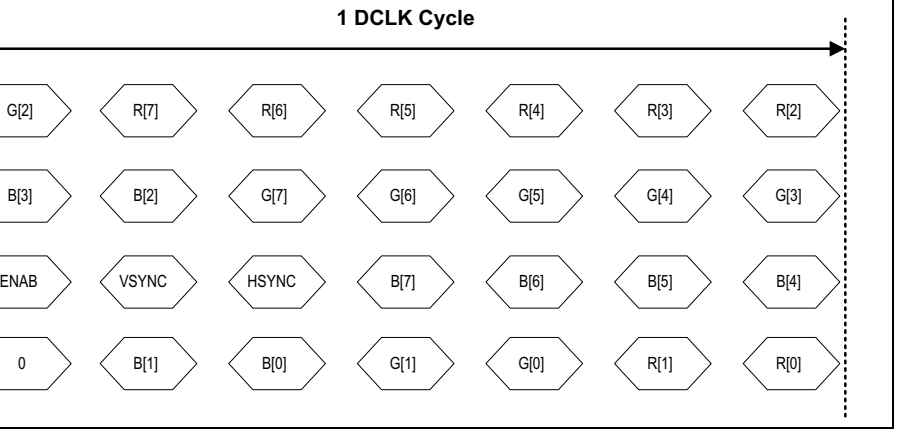


Figure 48. Data mapping for LVDS output in 8-bit config.

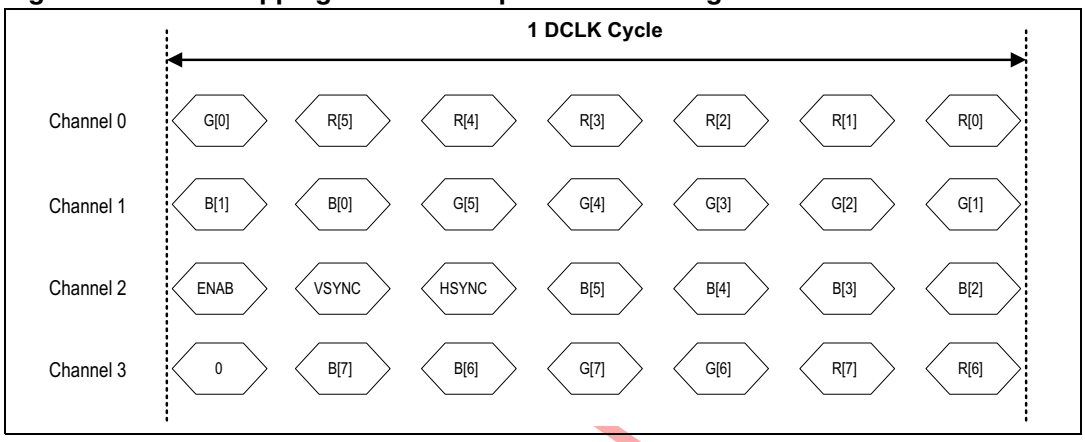
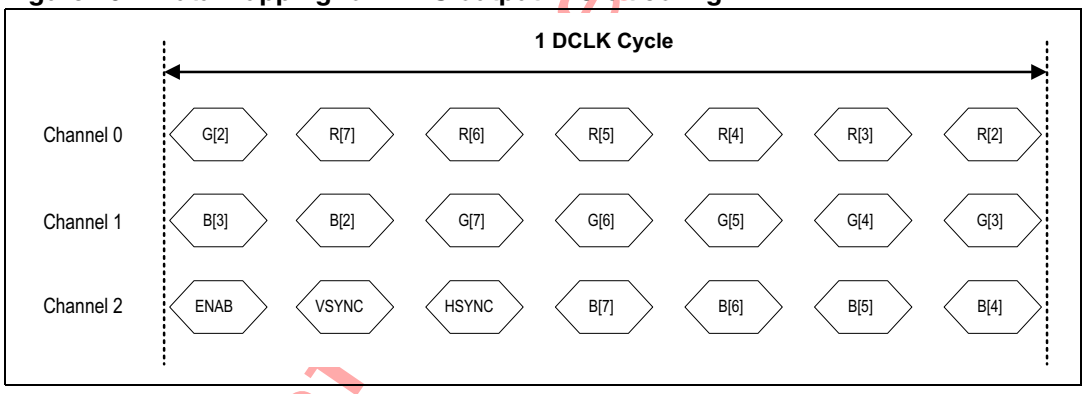


Figure 49. Data mapping for LVDS output in 6-bit config.



For system board layout flexibility there are several data swapping options. These data swapping options are independent of the data bit formatting options. One example is shown below:

Figure 50. Data mapping for LVDS output in 8-bit config.

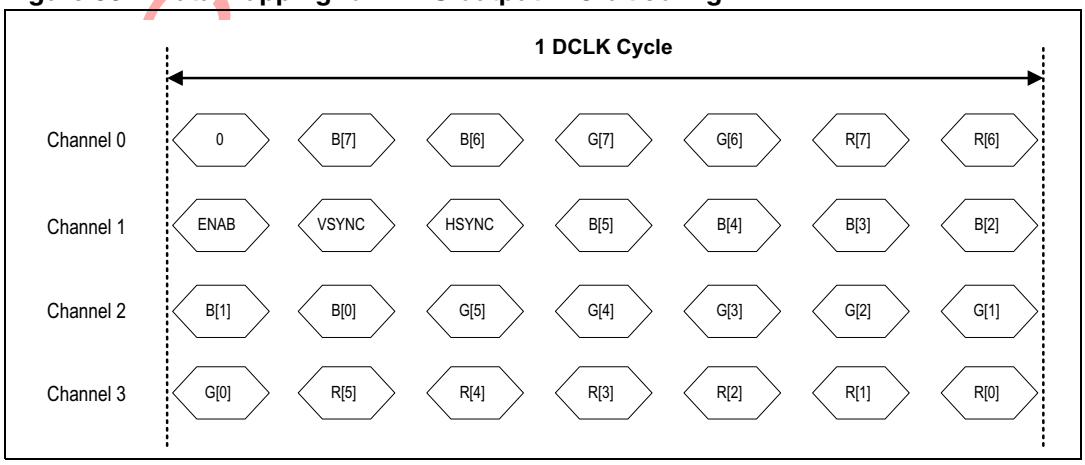
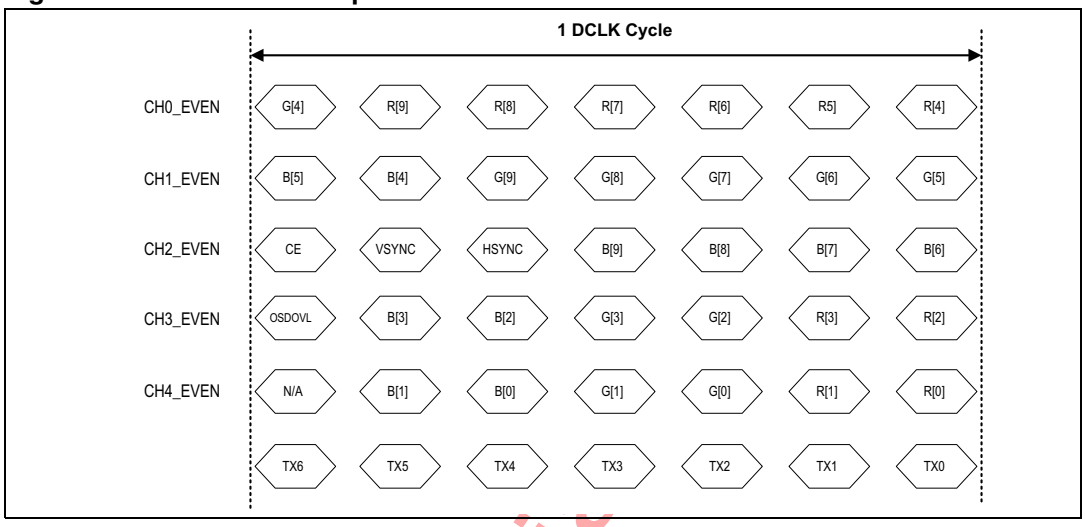


Figure 51. 30-bit LVDS output stream



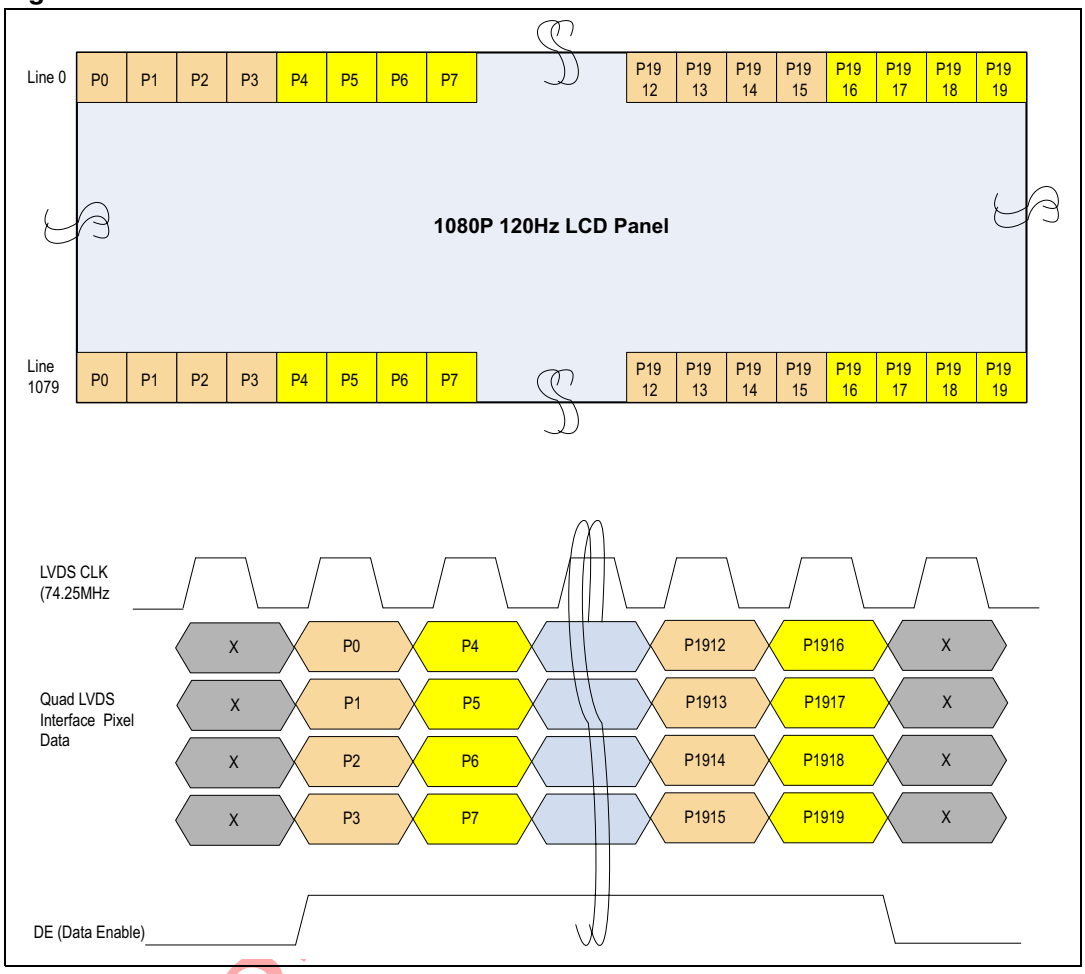
Custom LVDS mapping

LVDS mapping is customizable through a bit-by-bit mapping option for those panels that do not support any of the above mappings.

Stereo 3D LVDS interface

The LVDS interface is configurable for driving a stereo 3D LVDS panel at up to 120 Hz. Both frame sequential and line interleaved outputs can be supported.

Figure 52. 3D LVDS interface



LVDS output data L-R split

The Athena SoCs support the vertical split of LVDS output into independent left drive (on LVDS A,B links) and a right drive (on LVDS C,D Links), Driving each half of the screen independently. This feature is only available in the STDP 93xx/ STDP92xx parts.

4.12.7 DisplayPort transmitter

The DisplayPort output features a 5.4GHz DP1.2 compliant, 4-lane transmitter with AUX channel. The transmitter can also be configured or iDP/eDP operation. The transmitter will support multi-stream connectivity to allow daisy-chaining of multiple monitors over a DisplayPort1.2 link. The DisplayPort transmitter can receive data either from the Output Display Path (ODP) or from the DisplayPort1.2 compliant receiver wich features a MST source. The DisplayPort transmitter can output stereo data to drive a 3D panel interface. Both frame sequential and line interleaved outputs can be supported. The Athena SoCs can function as a HDCP repeater with DPTX output.

4.12.8 Pulse Width Modulation (PWM) back light control

The Athena SoCs have 16 pins that can function as PWM outputs (identifiable by suffix _PWM[0:15]). There are two types of PWMs on the Athena SoCs. One of these is intended

for use general purpose PWMs to implement voltage sources for audio volume or backlight brightness control. The second type of PWM is intended for use as a scanning backlight controller.

General purpose PWM controller

The general purpose PWM controller function is available on pins with the suffix PWM[0:3]. The duty cycle of these signals is programmable. They may be connected to an external RC integrator to generate a variable DC voltage for a LCD back light inverter or they may control the inverter directly using pulse width modulation. Panel HSync is used as the clock for a counter generating this output signal. PWMs can be synchronized to Vsync. Note that the scanning backlight PWM function can also be enabled on the same pins.

Scanning backlight PWM control

16 PWM outputs can be programmed to implement a scanning LED backlight interface. There is one PWM generator driving up to 16 PWM outputs, but each PWM output can be configured to output aPWM signal at different times.

All signals are timed with respect to DCLK. DCLK is divided down to create PWM clocks, which are further divided down to PWM periods. The resolution of the PWM generator output signal is controlled by changing the number of PWM clocks in a PWM period that the PWM output on. The controller can be used to generate PWM signals up to four sequential frames. The number of PWM periods that the PWM outputs stay active is programmable.

A typical use case would involve drive controls for side mounted LED backlight modules. Here the screen is divided into multiple PWM regions from the top to bottom of the screen. Each of the LED drives is controlled by a scanning PWM output. Depending on the duty cycle, the drives are sequentially driven in synchronism with the LCD raster.

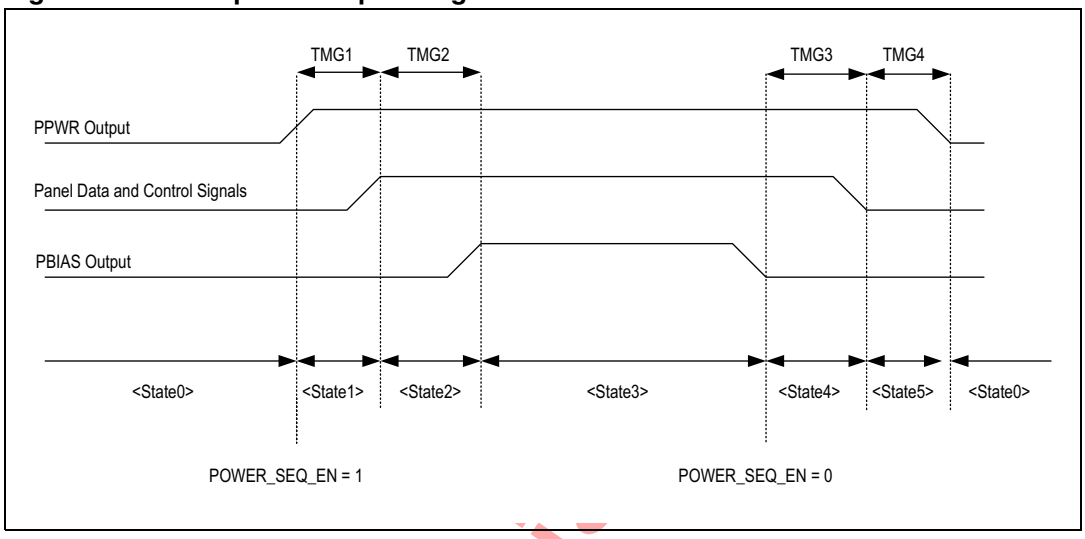
4.12.9 Stereo timing signal interface

A flexible stereo timing signal generation logic allows the encoding of the stereo left-right signal suitable for driving an IR LED. The signal can be received by active shutter glasses to enable 3D visualization.

4.12.10 Panel power sequencing (PPWR, PBIAS)

There are two dedicated outputs—PPWR and PBIAS—to control LCD power sequencing once data and control signals are stable. The timing of these signals is fully programmable.

Figure 53. Panel power sequencing



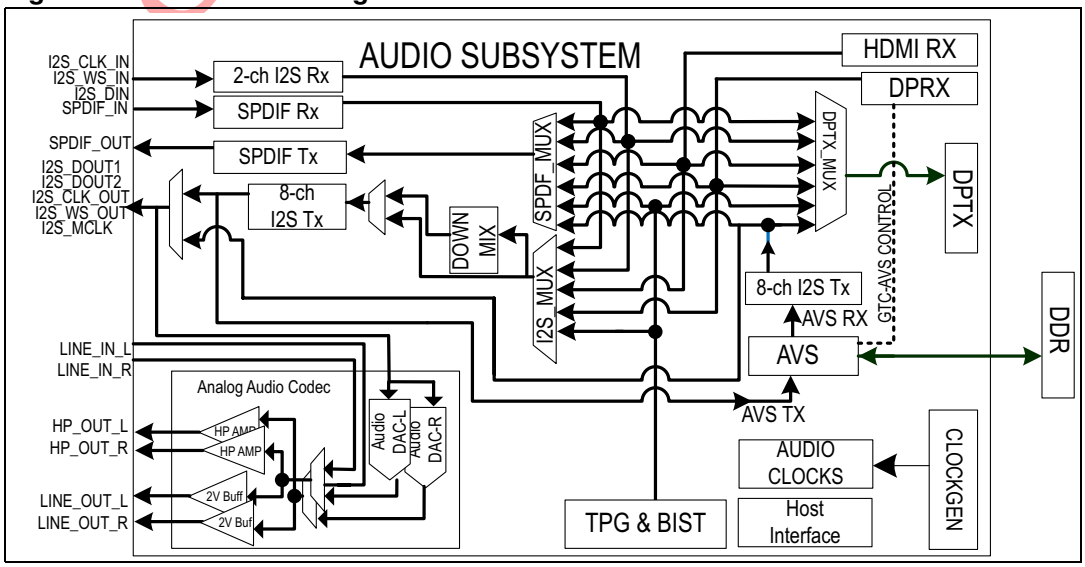
4.13 Energy Spectrum Management™ (ESM)

The Athena SoCs have features that can be used to reduce EMI. These include support of low EMI output interfaces (LVDS & DPTX), single crystal clock source and ESM support on PLLs.

4.14 Audio subsystem

The audio subsystem receives audio data from HDMI or DisplayPort , I2S and SPDIF receivers and routes these to DPTX, I2S or SPDIF transmitters. It also has an on-chip 20-bit audio DAC which it drives using 44.1 or 48 KHz PCM audio samples. Down-mixing is supported on this interface. The DAC Interface can drive standard line-out or headphone audio in stereo. It also supports line-in bypass.

Figure 54. Audio block diagram



The audio subsystem performs audio-video synchronization that may also be driven by GTC control from a DPRX 1.2 compliant audio source. Bufferred audio data is stored in an off-chip DDR buffer. The audio subsystem does not perform any baseband audio processing or sample rate conversion. The audio subsystem will not decode compressed audio. Compressed audio inputs can be received from DisplayPort, HDMI, SPDIF or I2S receivers and can be output to DisplayPort, I2S, or SPDIF transmitters unprocessed. The audio subsystem can receive formatted in HDMI1.4 or DP1.2 complant high bitrate audio streams. The audio subsystem cannot handle DSD streams.

4.14.1 Analog audio front-end

Athena audio front-end has the following features:

- A 24 bit, 32 kHz to 48 kHz Stereo DAC
- A volume control
- A headphone stereo amplifier with 2x 40 mW drive into 16 Kohm.
- A stereo input line buffer with volume control
- A 2 Vpp @ 10 Kohm, output stereo output line buffer
- A multiplexer with softmute
- An anti-pop engine

The line stereo inputs receive the audio signals which can be sent to line outputs and/or headphone outputs. A volume control component is dedicated to the line path allows to adjust the volume within a 46.5 dB range.

The DAC receives the input signal in I2S format. After conversion, the signal can be sent to line outputs and/or headphone outputs. The DAC internal volume control allows to adjust the signal amplitude within 60dB range. A mute control ramps the DAC output to ensure a soft mute.

The stereo inputs LIN_L and LIN_R receive the audio line signals and are directly connected to the line volume control component. The inputs are DC biased internally so the signal must be provided through a 150 nF coupling capacitor. The maximum input voltage is 1 Vpp. With a DC biasing at 1.45 V the input swing is 0.95 V / 1.95 V. A 5 bit volume control allows control from -40.5 dB to +6 dB at 1.5 dB per step.

The output buffers can deliver a 2 Vpp audio signal into 5 kO load. The output coupling must be done using a 1 uF capacitor. The DC biasing is linked with a bandgap reference with a typical value of 1.45 V in operating mode. Each buffer can by turned in stand-by mode independently.

The output buffers can deliver 40 mWrms audio signal into 16 O load. The output coupling must be done using a capacitor. The DC biasing is linked with a bandgap reference with a typical value of 1.45 V in operating mode. Headphone output is short circuit protected with a 160 mA current limit.

All reference voltages must be decoupled with 10 uF and 100 nF capacitors. All analog supply pins must be decoupled with 10 uF and 100 nF capacitors. All digital supply pins must be decoupled with 100 nF capacitors.

Table 7. Analog audio input and output signal specifications

Parameter	Conditions	Min	Typ	Max	Unit
Line-in resistance	Gain: 0 dB, Input: 1 kHz		50		Kohm
Line input DC level			1.45		V
Clipping line input level	THD +N > 0.1%	1			Vpp
THD	Vin = 1Vpp at 1 KHz		0.02		%
SNR	Vin = 1Vpp, 20 Hz to 20 KHz, Unweighted BW	85			dB
Bandwidth flatness	20 Hz to 20 KHz	-0.5	0	0.5	dB
Left / right crosstalk	VinL = 1 Vpp at 1 kHz, VinR = Gnd		90		dB
3.3V PSRR	All inputs GND, VDD33 = 3.3 V + 0.1 VRMS @ 2 KHz		TBD		dB
Line-out resistance			40		ohm
Line-out DC level			TBD		
Max output voltage	Rload >= 5 Kohm		2		Vpp

4.14.2 Digital audio interface

The digital audio interface enables the connection of external capture devices, such as ADCs, and digital output from other audio sources. It also enables connections to other STMicroelectronics devices or external audio systems (for example, DSPs or power amplifier systems). The Athena SoCs perform I2S and SPDIF output functions and an updated number of pairs and different configurations are possible.

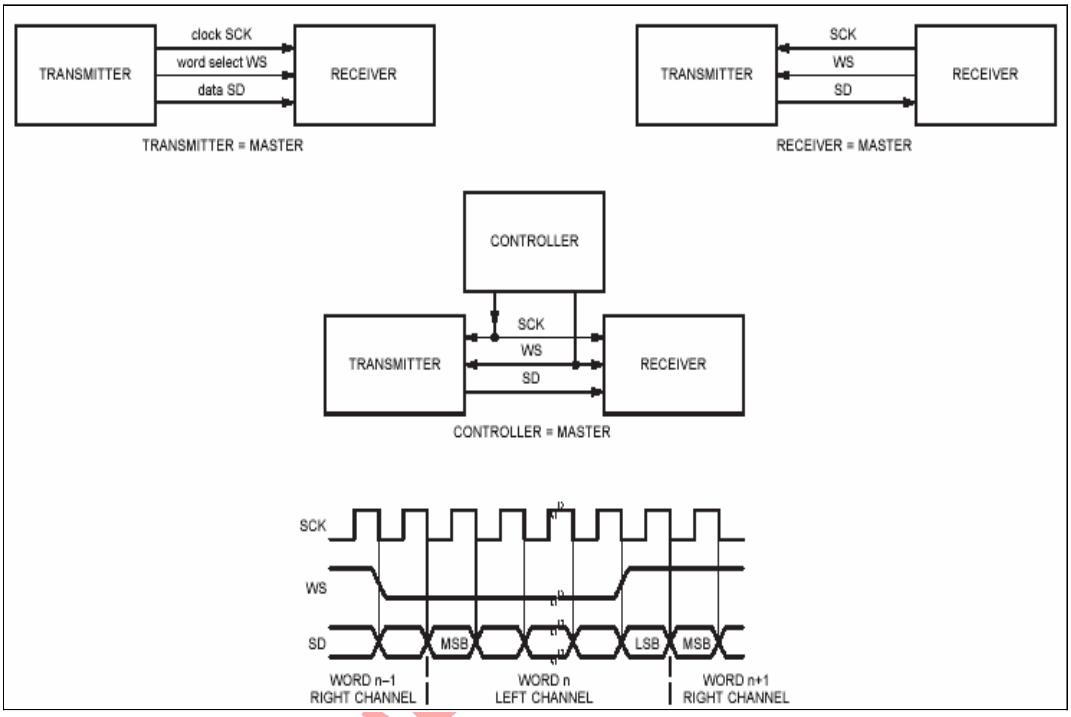
The Athena SoCs support one stereo Inter-IC Sound (I2S) input device and a four-channel stereo I2S output device.

The I2S bus input line is capable of receiving a two channel I2S signal. The interface consists of the following ports:

- I2S_DATA_IN: I2S serial data input
- I2S_CLK: I2S serial clock
- I2S_WS: I2S word strobe signal, defines left and right sample

The simple system configurations and basic interface timing are shown below. Please refer to the I2S specifications for more detailed information.

Figure 55. I2S transmitter and receiver blocks



SPDIF input supports all IEC60958 (SPDIF) formats. For detailed specifications, please refer to the proper IEC958 (IEC60958, SPDIF) specifications documents.

Table 8. Digital input/output configuration

Items		Specifications	Comments
Input	Format	I2S/SPDIF	
	Number of inputs	1 I2S, 1 SPDIF	
	Audio data length	16, 20, and 24 bits	For I2S
	Sample rate	32, 44.1, 48, 88.2, 96, 176.4,192 kHz	
Output	Format	I2S/SPDIF	
	Number of outputs	4 I2S, 1 SPDIF	Can carry 8-channel audio
	Audio data length	16, 20, and 24 bits	For I2S
	Audio master clock	3.072, 6.144, 12.288 MHz	Accepts external audio clock or generates internal clock

4.15 High-Bandwidth Digital Content Protection (HDCP)

The DisplayPort and HDMI digital interfaces support content encryption technology to enable content to be encrypted. Both intefaces use High-Bandwidth Digital Content

Protection (HDCP), a content protection standard defined and maintained by HDCP LLC as the means of protecting the content over the interface links.

The Athena SoCs contain embedded HDCP keys to simplify and help customers with their manufacturing process and to avoid handling HDCP keys on their production floor. As the HDCP keys are shared between the DisplayPort and HDMI receiver, only one set of HDCP receiver keys is required.

The Athena SoCs can function as a repeater (DP to DP or HDMi to DP or DVI to DP). In the repeater mode, the chips will need an additional HDCP key for the transmitter (DisplayPort output). For enhanced security, STMicroelectronics provides solutions for storing and accessing receiver keys in an encrypted format using an external HDCP key device or on-chip memory. Please contact an STMicroelectronics representative for further details.

4.16 On Screen Display (OSD)

The Athena SoCs have a fully programmable, true color bit-mapped OSD controller capable of displaying up to 16 tiles or bitmap windows on the display. The individual tiles are programmable for location, size, and bits per pixel, and have a precedence determining which tiles appear when overlapping occurs on the display. Tile data is stored in the external frame store memory by the OCM in either 1-, 2-, 4-, or 8-bit per pixel format. On-chip table registers point to the start of tiles in external memory. A programmable on-chip 256 x 24-bit color lookup table is provided to map the OSD pixels onto a true 24-bit color space.

Some general features of the OSD controller include:

- OSD position: The OSD menu is composed of tiles that can be positioned anywhere on the display region. The OSD can be flipped either horizontally or vertically.
- OSD zoom: The OSD image can be stretched horizontally and vertically by a factor of two (this is not an independent zoom: either zoom both horizontal and vertical, or neither). Pixel and line replication is used to stretch the image.
- OSD blending: Blending can be enabled on a tile-by-tile basis. OSD blending is performed between an OSD tile and the video stream below the tile. Up to eight simultaneous blending levels are supported at one time, with blend percentage specified at a resolution of 6.25%. OSD color LUT value FF is reserved for transparency and is unaffected by the blend attribute. A programmable blinking rate is also supported.
- Highlight window: Four independent highlight windows 1, 2, 3, and 4 are available for each tile. A highlight window is specified with a start and end position in pixels/lines and a 4-bit palette index register. A highlight window is used to highlight a selected section of a tile. This is achieved by modifying the color indices of pixels within the highlight window. The highlight window hardware allows a menu item to be highlighted by modifying a small number of SRAM-based registers as opposed to having to re-render the required pixels in DDR.

4.16.1 Color Look-Up Tables (LUT)

The color of every pixel in an OSD resolves to an 8-bit color code. This selected color code is then transformed to a 24-bit value using a 256 x 24-bit LUT. This LUT is stored in an on-chip RAM. The color index value 0xFF is reserved for transparent OSD pixels.

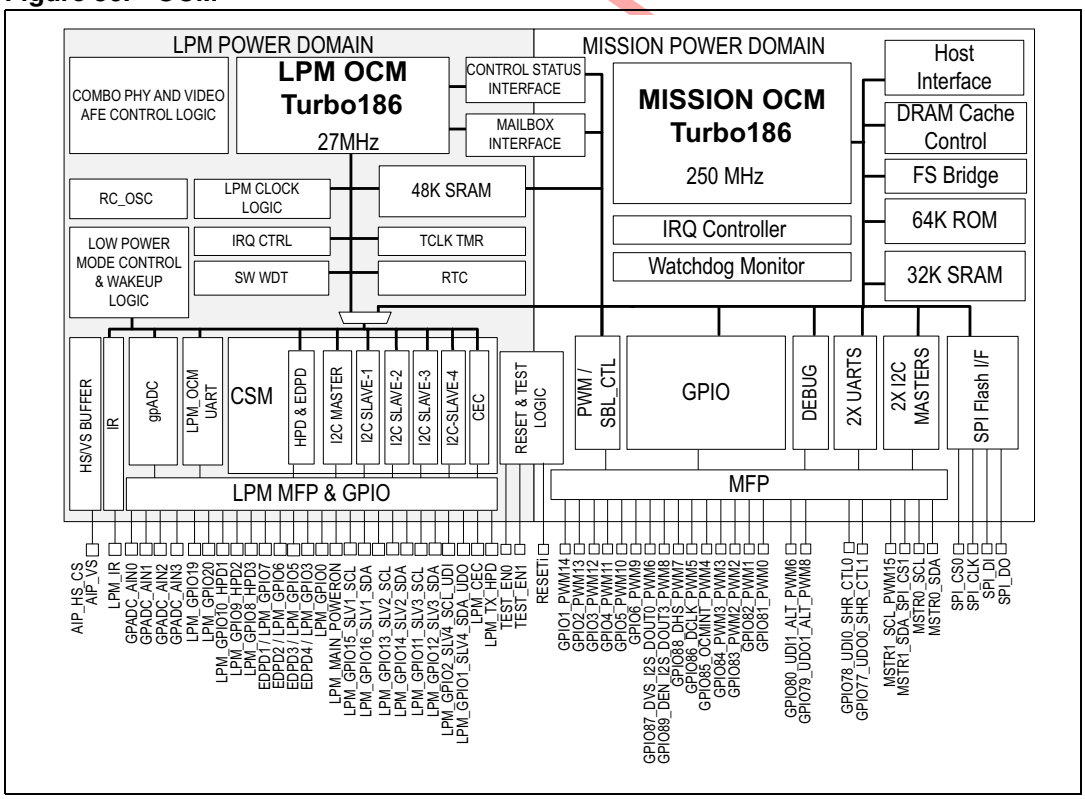
4.16.2 OSD for 3D panels

The devices support the OSD depth control for frame sequential or line interleaved panels.

4.17 On-Chip Microcontroller (OCM)

There are two OCMs on the Athena devices. Mission OCM runs the main monitor application. LPM OCM performs power management, provides key interface and manages DDC & CEC interfaces. Mission OCM is in the mission power domain along with the bulk of the Athena SoCs' logic and I/O. Power to the mission power domain will be turned off by LPM OCM in sleep mode. Switching of power supply rails is controlled by LPM OCM. These switch control outputs will default to the "on" state during cold boot process.

Figure 56. OCM



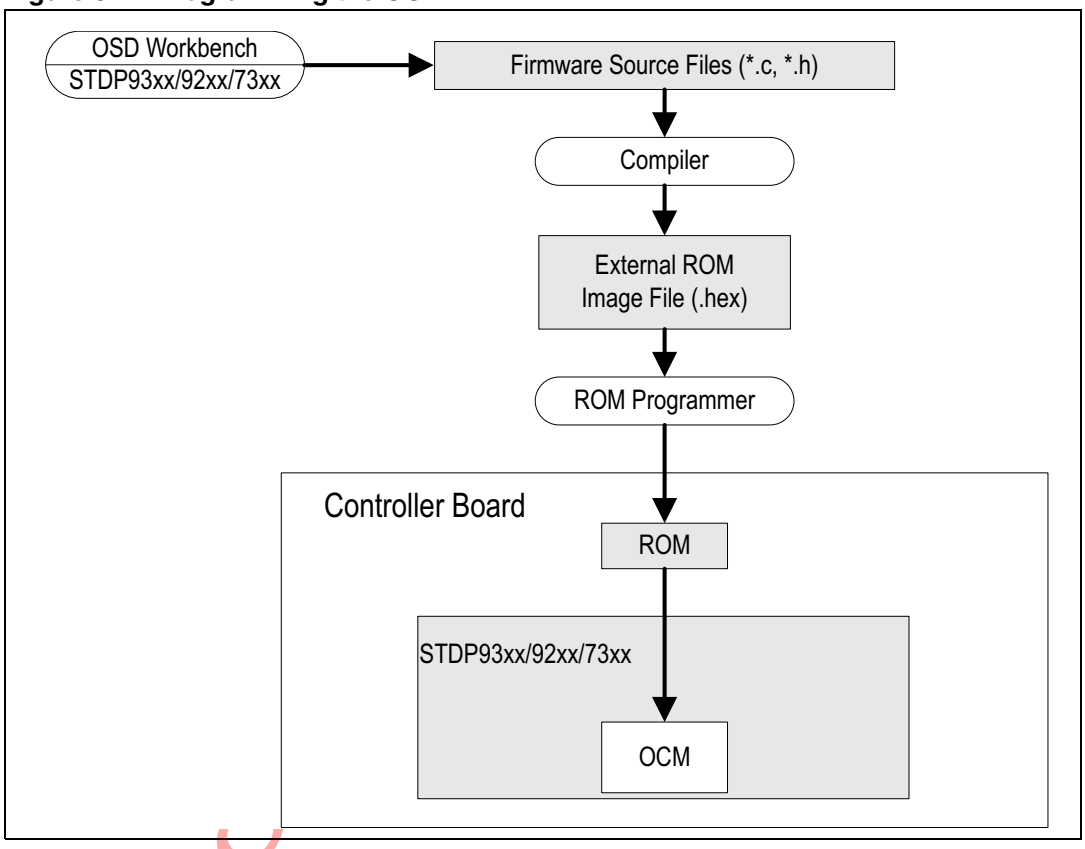
4.17.1 Mission OCM

Cold boot occurs on mission OCM from internal ROM. After system initialization, full boot up takes place from SPI flash memory.During the process of bootup, the mission OCM will also boot up LPM OCM. The OCM operates as illustrated in the figure above.

The OCM executes a firmware program running from external SPI ROM, as well as driver-level (or Application Programming Interface – API) functions residing in internal ROM. A serial programming interface is provided to support this request. This port connects directly to standard, commercially available SPI programmable Flash ROM. External Flash-ROM memory requirements range from 2 MB to 4 MB depending on the application.

Both firmware and OSD content must be compiled into a HEX file and then loaded onto the external ROM. The OSD content is generated using ST Workbench. ST Workbench is a GUI-based tool for defining OSD menus, navigation, and functionality. See the figure below for more options.

Figure 57. Programming the OCM



The Paradigm compiler (http://www.devtools.com) should be used to compile the firmware source code into a hex file. This hex file is then downloaded into the external ROM using commercially available ROM programmers.

Serial Peripheral Interface (SPI) for SPI Flash ROM

Hardware support is provided for SPI serial Flash ROM up to 4 M at a minimum speed of 33, 40, 50, 67, 100 MHz. The SPI interface is configured as follows:

- SPI_CSn <-> CE# of SPI ROM
- SPI_CLK <-> SCK of SPI ROM
- SPI_DO <-> SI of SPI ROM
- SPI_DI <-> SO of SPI ROM

Pins WP# and HOLD# of SPI ROM are options for the control of SPI ROM. Refer to the SPI ROM specifications for details. The Athena SoCs support dual SPI Flash devices as well as dual code banks. These mechanisms are used to provide failsafe bootup in case of inadvertent or incomplete ISP SPI programming.

In-System Programming (ISP) of Flash ROM devices

The Athena SoCs contain hardware to program SPI Flash devices while mounted to the system PCB. ISP can be done through serially through UART or DDC ports or alternately through a high speed receiver port over HDMI or DisplayPort using EZ_Display UP.

Interrupts

Theare are three external interrupt pins that can be used to interrupt the internal processor. The interrupts may be programmed for either active polarity.

JTAG OCM interface

A JTAG interface is provided to allow in-circuit debugging of the internal OCM. The JTAG interface can operate through a two-wire serial interface.

UART interface

The OCM has two integrated Universal Asynchronous Remote Terminal (UART) ports that can be used as a factory debug port. In particular, the UART can be used to:

- Read/write chip registers
- Read/write to NVRAM
- Read/write to flash ROM. Registers within the internal X186 controller determine the baud rate for serial communication.

I2C master ports

Featured are I2C ports on mission side labeled withprefix MSTR1_ and MSTR0_. These can be configured for I2C master operation through I2C master devices located on mission side. They can alternately be used for debug or GPIO functions.

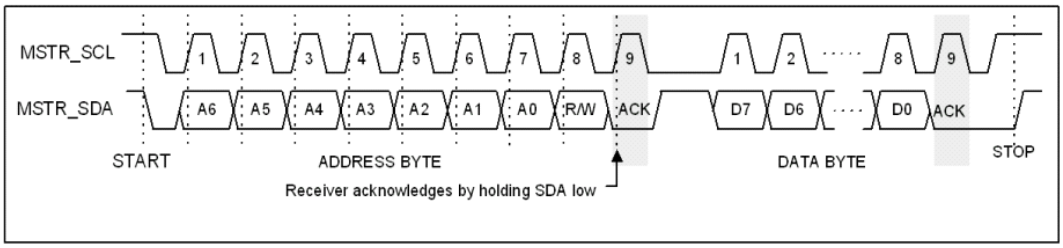
Two-wire master serial protocol

The two-wire protocol consists of a serial clock MSTR_SCL and bi-directional serial data line MSTR_SDA. The Athena SoCs act as bus master and drives MSTR_SCL. The master or slave can drive the MSTR_SDA line (open drain) depending on whether a read or write operation is being performed.

There are two isolated master serial busses, all driven by a common master serial controller. These busses can be independently taken “off-line” or pulled up to different voltages without affecting the other busses. The two master serial busses may be driven by a single serial master or optionally driven by independent serial masters.

The two-wire protocol requires each slave device to be addressable by a 7-bit identification number. A two-wire data transfer consists of a stream of serially transmitted bytes formatted as shown in the figure below. A transfer is initiated (START) by a high-to-low transition on MSTR_SDA while MSTR_SCL is held high. A transfer is terminated by a stop (a low-to-high transition on MSTR_SDA while MSTR_SCL is held high) or by a start (to begin another transfer).

Figure 58. Two-wire protocol data transfer



Each transaction on the MSTR_SDA is in integer multiples of 8 bits (i.e. bytes). The number of bytes that can be transmitted per transfer is unrestricted. Each byte is transmitted with the most significant bit (MSB) first. After the 8 data bits, the master releases the MSTR_SDA line and the receiver asserts the MSTR_SDA line low to acknowledge receipt of the data. The master device generates the MSTR_SCL pulse during the Acknowledge Cycle. The addressed receiver acknowledges each received byte.

Low Power Mode (LPM) OCM

The LPM-OCM is responsible for power management and has an output pin (MAIN_POWER_ON), which is used to control power to the mission power domain through external switching circuitry. It also controls user keys, IR, CEC, DDC for four ports, cable activity detect and HPD signaling.

LPM power control function

On a cold power-on the LPM-OCM stays in reset state and the MAIN_POWER_ON output defaults to the “on” state. On the mission side, the Power-On-RESET (POR) circuit generates the COLD RESET.

The MISSION-OCM comes out of reset and performs system initialization. As part of the initialization, it checks the LPM SRAM status (LP_SRAM_LOADED).

If the LPM-OCM SRAM is uninitialized (LP_SRAM_LOADED=0), it loads the LPM-OCM SRAM with boot code and sets a GO_LOW_POWER signal. This causes LPM_OCM to come out of reset state and boot up. After boot-up the LPM-OCM sets the LP_SRAM_LOADED to 1. Once the LPM-OCM has booted, the power-supply control output (MAIN_POWER_ON) can be controlled LPM-OCM software by which the external power-supply unit powering the mission power rails, can be turned-off during low power modes in order to reduce standby power to a minimum. The LPM-OCM software will turn-off MAIN_POWER_ON under command received from MISSION-OCM.

When system power is restored to active mode (MAIN_POWER_ON=1), the LPM-OCM software will issue a warm reset after powering up the mission power rails by making MAIN_POWER_ON=1. The WARM_RESET signal is controled by LPM-OCM Software write to the WARM_RESET register. If the LP_SRAM_LOADED=1 is detected once MISSION-OCM boots, it implies the MISSION-OCM has received a warm reset through LPM-OCM software action.

DDC ports

The Athena SoCs feature complete hardware support for four independent DDC2Bi channels communication implemented on the LPM-OCM. These are available on LPM_SLV1:4 I2C PORTS. The SLV1 port can also be configured as an I2C master to control an external DDC EDID device. In addition, SLV1 and SLV3 ports can also be used as

AUX2I2C master from the two internal DPRX receivers to control external DDC slave EEPROMs.

Multiplexing logic can also allow two additional I2C slave devices available on the mission side to map to SLV1 and SLV2 ports. This can be used as a temporary configuration for debugging or ISP access. The recommended port usage for the four I2C ports on LPM is SLV1-> COMBO1, SLV2-> COMBO2, SLV3-> COMBO3 and SLV4-> VGA.

For DDC2Bi communication over the analog VGA connector pins VGA_SCL and VGA_SDA should be connected to the DDC clock and data pins of the analog DSUB15 VGA connector. For DDC2Bi communication over the DVI or HDMI, connector pins HDMI_SDA and HDMI_SCL should be connected to the DDC clock and data pins of the DVI connector. Drivers for four I2C slave and one I2C saster will run on LPM OCM. In addition, LPM OCM. These ports form Part of the CSM or Communications Service Module function.

Infrared receiver

An infrared receiver is integrated to allow for the reception of infrared signals from remote control units. Standard protocols such as RECS 80 and RC5 are supported. The ability also exists to analyze raw signal streams for custom protocols. Optional Carrier filtering is available. Flow control is managed through host bit polling or an IRQ.

Low bandwidth ADC

The Athena SoCs support four low bandwidth ADC INPUTs (gpADC). The ADC inputs are available in the LPM section (GPADC_AIN[0:3]) and are under the control of the LPM OCM. Note that these pins are multi-functional and can be configured for use as digital inputs or outputs or as a 2 V input for GPADC on an individual basis.

When configured as an ADC input, these pins can be used to input and convert low speed analog signals (0-2 V range) to digital. The LBADCs are integrated to allow for functions such as keypad scanning or the monitoring of system temperature or voltage sensors. The ADCs have 10 bits of resolution and can perform a conversion in 14 clock periods. An analog multiplexer selects one of four analog input pins as the input to the ADC. Most systems will require just one input to be configured for use as a key analog input. In this mode, an external resistive ladder network may be used to encode multiple keys. Other GPADC_AIN pins can be configured for digital general purpose interface functions. The table below lists the ADC specification.

Table 9. Low bandwidth ADC specification

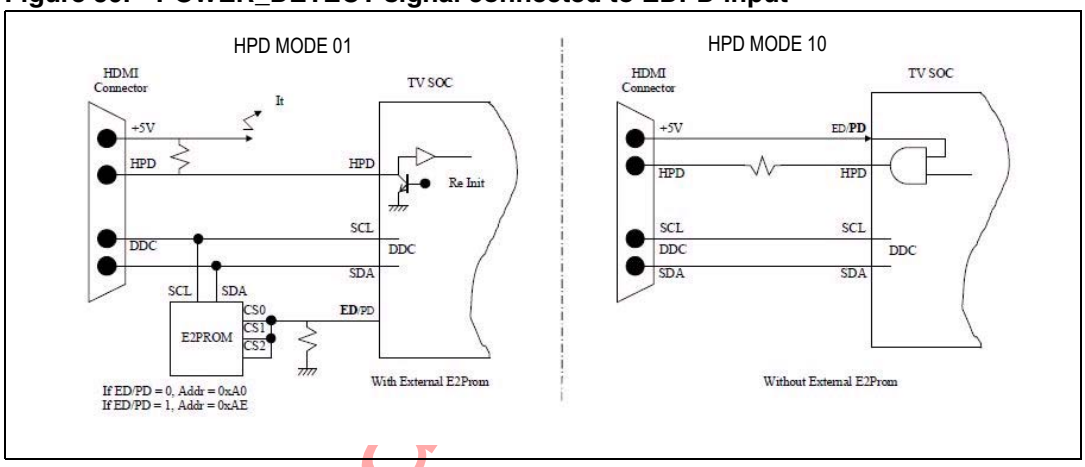
	Parameter	Min	Typ	Max
Power supply	Analog	2.25 V	2.5 V	2.8 V
Internal reference	REFINT	1.95 V	2.0 V	2.05 V
Resolution			10 bits	
Clock requirement	Frequency	2.5 MHz	14 MHz	20 MHz

HPD and cable detect logic

The LPM section of Athena SoCs also contain four HPD signaling and cable detect ports (which are also part of the CSM function). These are labeled with the suffixes HPD1:3 and TX_HPD. The recommended usage is HPD1->Combo1, HPD2-> Combo2, HPD3-> Combo3 and TX-HPD to DPTX HPD signal.

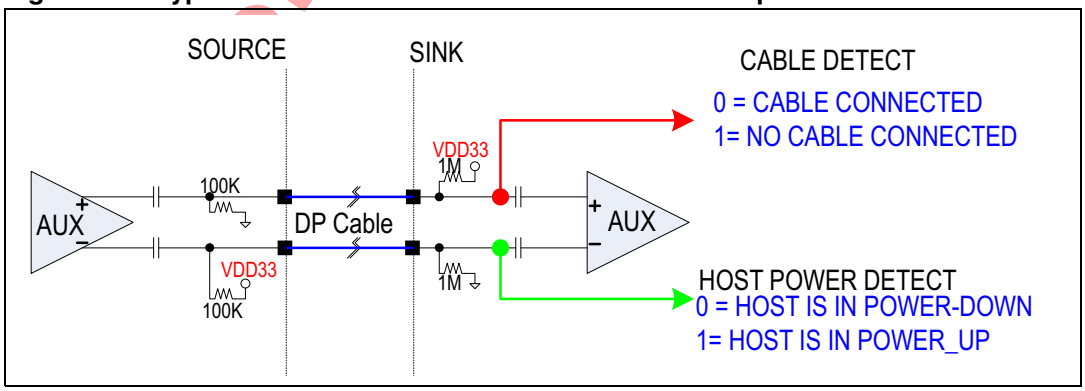
Note that the HPD may be configured as an Open_Drain or as an output gated by the VDD POWER_DETECT signal from HOST. In this case, the POWER_DETECT signal is to be connected to an EDPD input as shown below.

Figure 59. POWER_DETECT signal connected to EDPD input



The LPM also features four signals labeled with the prefixes EDPD1:4 for use as cable detection inputs or host power detection inputs or as EPROM disable controls. These pins have interrupt capability. Drivers for these capabilities will execute on LPM OCM.

Figure 60. Typical use case for DPRX cable detect or host power detect



CEC port

The CEC Port is part of the HDMI interface. This port is in the LPM power domain under control of the LPM OCM. Port monitoring capabilities can be enabled during sleep modes, to ensure a rapid system recovery. This follows the standard HDMI CEC Electrical Specification to implement the Consumer Electronics Control interface. The CEC channel is optionally used for higher-level user functions such as automatic setup tasks or tasks typically associated with infrared remote control usage. The CEC drivers will run on the LPM OCM.

4.18 General Purpose Inputs and Outputs (GPIOs)

Theare are an extensive number of GPIO pins. All of these may not be available depending on shared functionality of particular pins. The table below summarizes the recommended usage for these GPIOs.

Table 10. Mission GPIO signals

Signals	GPIO numbers	Function 1	Function 2	Function 3	RD board usage
DIN_CK1	GPIO0	DIN_CK1			VXI PORTCK1
DIN_VS	GPIO1	DIN_VS			VXI PORTVS
DIN_HS_CS	GPIO2	DIN_HS_CS			VXI PORTHS_CS
DIN_ODD	GPIO3	DIN_ODD			VXI PORTODD
DIN_HREF_DE	GPIO4	DIN_HREF_DE			VXI PORTHREF_DE
DIN_0	GPIO32	DIN_0			VXI PORT DATA0
DIN_1	GPIO31	DIN_1			VXI PORT DATA1
DIN_2	GPIO30	DIN_2			VXI PORT DATA2
DIN_3	GPIO29	DIN_3			VXI PORT DATA3
DIN_4	GPIO28	DIN_4			VXI PORT DATA4
DIN_5	GPIO27	DIN_5			VXI PORT DATA5
DIN_6	GPIO26	DIN_6			VXI PORT DATA6
DIN_7	GPIO25	DIN_7			VXI PORT DATA7
DIN_8	GPIO22	DIN_8			VXI PORT DATA8
DIN_9	GPIO21	DIN_9			VXI PORT DATA9
DIN_10	GPIO20	DIN_10			VXI PORT DATA10
DIN_11	GPIO19	DIN_11			VXI PORT DATA11
DIN_12	GPIO18	DIN_12			VXI PORT DATA12
DIN_13	GPIO17	DIN_13			VXI PORT DATA13
DIN_14	GPIO16	DIN_14			VXI PORT DATA14
DIN_15	GPIO15	DIN_15			VXI PORT DATA15
DIN_16	GPIO12	DIN_16			VXI PORT DATA16
DIN_17	GPIO11	DIN_17			VXI PORT DATA17
DIN_18	GPIO10	DIN_18			VXI PORT DATA18
DIN_19	GPIO9	DIN_19			VXI PORT DATA19
DIN_20	GPIO8	DIN_20			VXI PORT DATA20
DIN_21	GPIO7	DIN_21			VXI PORT DATA21
DIN_22	GPIO6	DIN_22			VXI PORT DATA22
DIN_23	GPIO5	DIN_23			VXI PORT DATA23
I2S_DIN	GPIO59	I2S DATA IN			I2S_DIN

Table 10. Mission GPIO signals

Signals	GPIO numbers	Function 1	Function 2	Function 3	RD board usage
I2S_WS_IN	GPIO60	I2S WORD SYNC IN			I2S_WS_IN
I2S_CLK_IN	GPIO61	I2S CLOCK IN			I2S_CLK_IN
I2S_DOUT2	GPIO62	I2S DATA2 OUT			I2S_DOUT2
I2S_DOUT1	GPIO63	I2S DATA1 OUT			I2S_DOUT1
I2S_WS_OUT	GPIO64	I2S WORD SYNC OUT			I2S_WS_OUT
I2S_CLK_OUT	GPIO65	I2S CLOCK OUT			I2S_CLK_OUT
I2S_MCLK_OUT_IN	GPIO66	I2S MASTER CLOCK			I2S_MCLK_OUT_IN
SPDIF_OUT	GPIO67	SPDIF OUTPUT			SPDIF_OUT
SPDIF_IN	GPIO68	SPDIF INPUT			SPDIF_IN
MSTR0_SDA	GPIO69	I2C MASTER0 SDA			MSTR0_SDA
MSTR0_SCL	GPIO70	I2C MASTER0 SCL			MSTR0_SCL
MSTR1_SDA_SPI_CS1	GPIO71	I2C MASTER1 SDA	SPI_CS1		MSTR1_SDA
MSTR1_SCL_PWM15	GPIO72	I2C MASTER1 SCL	PWM15		MSTR1_SCL
GPIO78_UDI0_SHTR_CTL1	GPIO78	UART0 RX	SHUTTER CTRL1		OCM_UDI0 GPROBE-A
GPIO77_UDO0_SHTR_CTL0	GPIO77	UART0 TX	SHUTTER CTRL0		OCM_UDO0 GPROBE-A
GPIO79_UDO1_ALT_PWM8	GPIO79	UART1 TX	PWM8		LED_GREEN
GPIO80_UDI1_ALT_PWM6	GPIO80	UART1 RX	ALT PWM6		DIN Connect Detect
GPIO81_PWM0	GPIO81	PWM0			MAIN_MUTE
GPIO82_PWM1	GPIO82	PWM1			AUD_GAIN0
GPIO83_PWM2	GPIO83	PWM2			AUD_GAIN1
GPIO84_PWM3	GPIO84	PWM3			PANEL PWM Control
GPIO85_OCMINT_PWM4	GPIO85	OCMINT	PWM4		DIP_INT_IN
GPIO86_DCLK_PWM5	GPIO86	DISPLAY CLOCK	PWM5	OCM_INT2	AUD_SDBY
DVS_GPIO87_PWM6_I2S_DOUT0	GPIO87	DISPLAY VSYNC OUT	I2S DOUT0	PWM6	I2S_DOUT0

Table 10. Mission GPIO signals

Signals	GPIO numbers	Function 1	Function 2	Function 3	RD board usage
GPIO88_DHS_PWM7	GPIO88	DISPLAY HS	PWM7		AUD_DAC_RESET
DEN_GPIO89_PWM8_I2S_DOUT3	GPIO89	I2S DOUT3	PWM8		I2S_DOUT3
GPIO6_PWM9	GPIO90	PWM9			NVRAM_WP
GPIO5_PWM10	GPIO91	PWM10			EDID_WP
GPIO4_PWM11	GPIO92	PWM11			DUAL_SPI_HOLD1
GPIO3_PWM12	GPIO93	PWM12			SPI_WP
GPIO2_PWM13	GPIO94	SHUTTER CTRL0	PWM13		SHTR_CTL0
GPIO1_PWM14	GPIO95	SHUTTER CTRL1	PWM14		SHTR_CTRL

Table 11. LPM GPIO signals

Signals	GPIO numbers	Function 1	Function 2	Function 3	RD board usage
GPADC_AIN0	ADC_GPIO0	GPADC ANA IN0			GPADC_AIN0 KEYBOARD
GPADC_AIN1	ADC_GPIO1	GPADC ANA IN1			GPADC_AIN1 KEYBOARD
GPADC_AIN2	ADC_GPIO2	GPADC ANA IN2			VGA/DVI Cable Detect
GPADC_AIN3	ADC_GPIO3	GPADC ANA IN3			TMDS_EN TMDS SW VDD Control
LPM_GPIO0	LPM GPIO0	INTERRUPT INPUT			LPM_OCM_INT
LPM_UDO_GPIO1_SLV4_SDA	LPM_GPIO1	I2C SLAVE4 SDA	LPM OCM UART TX		VGA_SDA_UDO
LPM_UDI_GPIO2_SLV4_SCL	LPM_GPIO2	I2C SLAVE4 SCL	LPM OCM UART RX		VGA_SCL_UDI
LPM_GPIO3_EDPD4	LPM_GPIO3	POWER DETECT 4	EPROM DISABLE 4		POWERMODULE_SDBY
LPM_CEC	LPM_GPIO4	CEC			CEC_LPM
LPM_GPIO5_EDPD3	LPM_GPIO5	POWER DETECT 3	EPROM DISABLE 3		HDMI_CABLE Detect
LPM_GPIO6_EDPD2	LPM_GPIO6	POWER DETECT 2	EPROM DISABLE 2		CP0 AUX_N Host Power Detect
LPM_GPIO7_EDPD1	LPM_GPIO7	POWER DETECT 1	EPROM DISABLE 1		CP0 AUX_P Cable Detect
LPM_GPIO8_HPD3	LPM_GPIO8	HPD OUT 3			LPM_HDMI_HPD
LPM_GPIO9_HPD2	LPM_GPIO9	HPD OUT 2			LPM_DVI_HPD

Table 11. LPM GPIO signals

Signals	GPIO numbers	Function 1	Function 2	Function 3	RD board usage
LPM_GPIO10_HPD1	LPM_GPIO10	HPD OUT 1			LPM_DPRX_HPD
LPM_GPIO11_SLV3_SCL	LPM_GPIO11	I2C SLAVE3 SCL			LPM_HDMI_SCL
LPM_GPIO12_SLV3_SDA	LPM_GPIO12	I2C SLAVE3 SDA			LPM_HDMI_SDA
LPM_GPIO13_SLV2_SCL	LPM_GPIO13	I2C SLAVE2 SCL			LPM_DVI_SCL
LPM_GPIO14_SLV2_SDA	LPM_GPIO14	I2C SLAVE2 SDA			LPM_DVI_SDA
LPM_GPIO15_SLV1_SCL	LPM_GPIO15	I2C SLAVE 1 SCL			LPM_MSTR_SCL for EEPROM & Touch Pad control
LPM_GPIO16_SLV1_SDA	LPM_GPIO16	I2C SLAVE 1 SDA			LPM_MSTR_SDA for EEPROM & Touch Pad control
LPM_TX_HPD	LPM_GPIO17	TX HPD IN			DPTX_HPD
LPM_MAIN_POWER_ON	LPM_GPIO18	MAIN_POWER_ON			MAIN_POWER_ON
LPM_GPIO_19	LPM_GPIO19				TMDS_SEL External TMDS SW control
LPM_GPIO_20	LPM_GPIO20				LED_AMBER

4.19 Host register interface

The Athena SoCs contain many internal registers that control its operation. These registers are mapped directly into the OCM's memory space. A complete list is part of the register specification document to be published.

5 BGA footprint and ball lists

5.1 Ball grid array

The ball grid array (BGA) diagrams give the allocation of pins to the package, shown from the top looking down using the PCB footprint.

Signal names are prefixed by NOT if they are active low; otherwise they are active high. Some signal names in BGA diagrams have been abbreviated. Refer to *Section 5.3: Ball lists on page 80* for the full signal names.

Figure 61. Key to BGA diagrams

Function	Type	Key
Digital Input Port	SIG	
Analog Front End		
Analog Audio		
Low Power Monitor		
COMBO PHY		
DIGITAL Audio I/O		
Multifunction		
DPTX Output		
LVDS Transmitter		
Reset		
Frame Store DDR Interface		
VDD1.2V Analog LPM /Combo PHY / DisplayPort Analog	PWR	
VDD1.2V Audio		
VDD1.2V Digital / Core		
VDD1.2V Digital LPM		
VDD2.5V LVDS / DPTX / PLL / Analog LPM		
VDD2.5V LPM SAFEMEM		
VDDQ_DDR / VDD3.3 ANALOG / REG_OUT_VDDR		
VDD3.3V Digital LPM/ VDD3.3V LPM Combo PHY		
VDD3.3V Digital		
Ground	GND	
No connect/Do not connect	NC/DNC	
No ball		

5.2 STDP93xx / 92xx / 73xx ball out

The STDP93xx and STDP92xx are available in a 521-ball BGA package. The STDP73xx is available in a 361-ball BGA package. The figures on the following pages provide ball locations for all signals (viewed from the top of the package).

Figure 62. STDP93xx and STDP92xx ball out diagram: Top-left quadrant

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	A1 GND	A2 LPM_GPIO6_EDPD2	A3 LPM_GPIO13_SLV2_SCL	A4 LPM_GPIO8_HPD3	A5 LPM_GPIO12_SLV3_SDA	A6 AO_HP_OUT_L	A7 AO_LOUT_L	A8 AO_LINE_L	A9 GND	A10 VGA_B_P	A11 VGA_G_P	A12 VGA_R_P	A13 PB_P
B	B1 LPM_GPIO5_EDPD3	B2 LPM_GPIO3_EDPD4	B3 LPM_GPIO14_SLV2_SDA	B4 LPM_GPIO9_HPD2	B5 LPM_GPIO11_SLV3_SCL	B6 AO_HP_OUT_R	B7 AO_LOUT_R	B8 AO_LINE_R	B9 GND	B10 VGA_B_N	B11 VGA_G_N	B12 VGA_R_N	B13 PB_N
C	C1 LPM_MAIN_POWER_ON	C2 LPM_GPIO_19	C3 LPM_GPIO10_HPD1	C4 LPM_GPIO15_SLV1_SCL	C5 LPM_UDO_GPIO1_SLV4_SDA	C6 AIP_HS_CS	C7 AUD_VBG	C8 AO_VREF_L	C9 GND	C10 GND	C11 GND	C12 GND	C13 GND
D	D1 LPM_GPIO_20	D2 LPM_IR	D3 LPM_GPIO7_EDPD1	D4 LPM_GPIO16_SLV1_SDA	D5 LPM_UDI_GPIO2_SLV4_SCL	D6 AIP_VS	D7 AO_VREF_H	D8 VDDA3V3_AUD	D9 GND	D10 GND	D11 GND	D12 GND	D13 GND
E	E1 LPM_GPIO0	E2 LPM_DPTX_HPD	E3 GPADC_AIN0	E4 TEST_EN0	E5 VDD1V2_LPM_DIG	E6 VDD3V3_HP_AUD	E7 VDD3V3_HP_AUD	E8 VDD1V2_AUDIO	E9 GND	E10 VDD1V2_LPM_ADC	E11 VDD1V2_LPM_ADC	E12 VDD2V5_LPM_ADC	E13 VDD2V5_LPM_ADC
F	F1 GPADC_AIN1	F2 GPADC_AIN2	F3 GPADC_AIN3	F4 TEST_EN1	F5 VDD1V2_LPM_DIG								
G	G1 CP0_AUXN	G2 CP0_AUXP	G3 CP0_REXT	G4 LPM_CEC	G5 VDD3V3_LPM_DIG								
H	H1 CP0_0P	H2 CP0_0N	H3 GND	H4 GND	H5 VDD2V5_LPM_SAFEMEM								
I	J1 CP0_1P	J2 CP0_1N	J3 GND	J4 GND	J5 GND								
J	K1 CP0_2P	K2 CP0_2N	K3 GND	K4 GND	K5 VDD3V3_LPM_COMBO					K10 VDD1V2_DIG	K11 VDD1V2_DIG	K12 GND	K13 GND
K	L1 CP0_3P	L2 CP0_3N	L3 GND	L4 GND	L5 VDD3V3_LPM_COMBO					L10 VDD1V2_DIG	L11 GND	L12 GND	L13 GND
L	M1 CP1_AUXN	M2 CP1_AUXP	M3 CP1_REXT	M4 GND	M5 VDD3V3_LPM_COMBO					M10 VDD1V2_DIG	M11 GND	M12 GND	M13 GND
M	N1 CP1_0P	N2 CP1_0N	N3 GND	N4 GND	N5 VDD3V3_LPM_COMBO					N10 VDD1V2_DIG	N11 GND	N12 GND	N13 GND
P	P1 CP1_1P	P2 CP1_1N	P3 GND	P4 GND	P5 VDD3V3_LPM_COMBO					P10 VDD1V2_DIG	P11 GND	P12 GND	P13 GND

Figure 63. STDP93xx and STDP92xx ball out diagram: Top-right quadrant

14	15	16	17	18	19	20	21	22	23	24	25	26	27	
A14 Y_P	A15 PR_P	A16 DIN_22	A17 DIN_19	A18 DIN_15	A19 DIN_11	A20 DIN_7	A21 DIN_3	A22 DIN_HREF_DE	A23 DIN_VS	A24 DIN_CK0	A25 GPIO80_UDI1_ALT_PWM6	A26 GPIO78_UDI0_SHTR_CTL1	A27 GND	A
B14 Y_N	B15 PR_N	B16 DIN_23	B17 DIN_20	B18 DIN_16	B19 DIN_12	B20 DIN_8	B21 DIN_4	B22 DIN_0	B23 DIN_HS_CS	B24 DIN_CK1	B25 GPIO79_UDO1_ALT_PWM8	B26 GPIO77_UDO0_SHTR_CTL0	B27 GPIO85_OCMINT_PWM4	B
C14 GND	C15 GND	C16 GND	C17 DIN_21	C18 DIN_17	C19 DIN_13	C20 DIN_9	C21 DIN_5	C22 DIN_1	C23 GPIO88_DHS_PWM7	C24 DIN_ODD	C25 GPIO6_PWM9	C26 GPIO5_PWM10	C27 GPIO4_PWM11	C
D14 GND	D15 GND	D16 GND	D17 RESETN	D18 DIN_18	D19 DIN_14	D20 DIN_10	D21 DIN_6	D22 DIN_2	D23 GPIO86_DCLK_PWM5	D24 GPIO81_PWM0	D25 GPIO82_PWM1	D26 DDR_D[21]	D27 DDR_D[23]	D
E14 VDD2V5_LPM_ADC	E15 VDD2V5_LPM_ADC	E16 GND	E17 GND	E18 GND	E19 GND	E20 GND	E21 VDD3V3_DIG	E22 VDD3V3_DIG	E23 GND	E24 GPIO83_PWM2	E25 GPIO84_PWM3	E26 DDR_D[19]	E27 DDR_D[17]	E
									F23 GND	F24 GPIO3_PWM12	F25 GPIO2_PWM13	F26 DDR_D[24]	F27 DDR_D[26]	F
									G23 VDD2V5_PLL	G24 GPIO1_PWM14	G25 DDR_VREF2	G26 DDR_D[30]	G27 DDR_D[28]	G
									H23 GND	H24 DDR_ODT	H25 DDR_RASN	H26 DDR_DQSN[3]	H27 DDR_DQSP[3]	H
									J23 VDDQ_DDR	J24 DDR_CASN	J25 DDR_CSN	J26 DDR_DQSN[2]	J27 DDR_DQSP[2]	I
K14 GND	K15 GND	K16 GND	K17 VDD1V2_DIG	K18 VDD1V2_DIG					K23 VDDQ_DDR	K24 DDR_ZQ	K25 DDR_A[0]	K26 DDR_DQM[2]	K27 DDR_DQM[3]	J
L14 GND	L15 GND	L16 GND	L17 GND	L18 VDD1V2_DIG					L23 VDDQ_DDR	L24 DDR_A[2]	L25 DDR_A[4]	L26 DDR_D[25]	L27 DDR_D[31]	K
M14 GND	M15 GND	M16 GND	M17 GND	M18 VDD1V2_DIG					M23 VDDQ_DDR	M24 DDR_A[6]	M25 DDR_A[8]	M26 DDR_D[29]	M27 DDR_D[27]	L
N14 GND	N15 GND	N16 GND	N17 GND	N18 VDD1V2_DIG					N23 VDDQ_DDR	N24 DDR_A[13]	N25 DDR_A[11]	N26 DDR_D[16]	N27 DDR_D[18]	M
P14 GND	P15 GND	P16 GND	P17 GND	P18 VDD1V2_DIG					P23 VDDQ_DDR	P24 DDR_A[12]	P25 DDR_A[9]	P26 DDR_D[22]	P27 DDR_D[20]	P

Figure 64. STDP93xx and STDP92xx ball out diagram: Bottom-left quadrant

	1	2	3	4	5	6	7	8	9	10	11	12	13
R	R1 CP1_2P	R2 CP1_2N	R3 GND	R4 GND	R5 GND					R10 VDD1V2_DIG	R11 GND	R12 GND	R13 GND
T	T1 CP1_3P	T2 CP1_3N	T3 GND	T4 GND	T5 VDD1V2_LPM_COMBO					T10 VDD1V2_DIG	T11 GND	T12 GND	T13 GND
U	U1 CP2_AUXN	U2 CP2_AUXP	U3 CP2_REXT	U4 GND	U5 VDD1V2_LPM_COMBO					U10 VDD1V2_DIG	U11 GND	U12 GND	U13 GND
V	V1 CP2_0P	V2 CP2_0N	V3 GND	V4 GND	V5 VDD1V2_LPM_COMBO					V10 VDD1V2_DIG	V11 VDD1V2_DIG	V12 GND	V13 GND
W	W1 CP2_1P	W2 CP2_1N	W3 GND	W4 GND	W5 VDD1V2_LPM_COMBO								
Y	Y1 CP2_2P	Y2 CP2_2N	Y3 GND	Y4 GND	Y5 VDD1V2_LPM_COMBO								
AA	AA1 CP2_3P	AA2 CP2_3N	AA3 GND	AA4 GND	AA5 VDD1V2_LPM_COMBO								
AB	AB1 I2S_DIN	AB2 I2S_WS_IN	AB3 I2S_CLK_IN	AB4 SPDIF_IN	AB5 GND								
AC	AC1 I2S_DOUT1	AC2 I2S_DOUT2	AC3 I2S_WS_OUT	AC4 I2S_CLK_OUT	AC5 GND	AC6 GND	AC7 GND	AC8 GND	AC9 VDD1V2_DPTX	AC10 VDD1V2_DPTX	AC11 VDD1V2_DPTX	AC12 GND	AC13 VDD2V5_DPTX
AD	AD1 I2S_MCLK_OUT_IN	AD2 SPDIF_OUT	AD3 SPI_CLK	AD4 SPI_DO	AD5 GND	AD6 GND	AD7 GND	AD8 GND	AD9 GND	AD10 GND	AD11 GND	AD12 GND	AD13 GND
AE	AE1 SPI_DI	AE2 SPI_CSN	AE3 GND	AE4 GND	AE5 GND	AE6 GND	AE7 GND	AE8 GND	AE9 GND	AE10 DP_TX_REXT	AE11 GND	AE12 GND	AE13 GND
AF	AF1 DVS_GPIO87_PWM6_I2S_DOUT0	AF2 DEN_GPIO89_PWM8_I2S_DOUT3	AF3 MSTR0_SCL	AF4 PPWR	AF5 GND	AF6 GND	AF7 GND	AF8 GND	AF9 GND	AF10 DP_AUXTXN	AF11 DP_TX3N	AF12 DP_TX2N	AF13 DP_TX1N
AG	AG1 GND	AG2 MSTR1_SDA_SPI_CS1	AG3 MSTR1_SCL_PWM15	AG4 MSTR0_SDA	AG5 PBIAS	AG6 GND	AG7 VDD3V3_DIG	AG8 VDD3V3_DIG	AG9 VDD3V3_DIG	AG10 DP_AUXTXP	AG11 DP_TX3P	AG12 DP_TX2P	AG13 DP_TX1P

Figure 65. STDP93xx and STDP92xx ball out diagram: Bottom-right quadrant

R14 GND	R15 GND	R16 GND	R17 GND	R18 VDD1V2_DIG					R23 VDDQ_DDR	R24 DDR_RESETN	R25 DDR_A[7]	R26 DDR_CLKN	R27 DDR_CLKP	R
T14 GND	T15 GND	T16 GND	T17 GND	T18 VDD1V2_DIG					T23 VDDQ_DDR	T24 DDR_A[5]	T25 DDR_A[3]	T26 DDR_D[5]	T27 DDR_D[7]	T
U14 GND	U15 GND	U16 GND	U17 GND	U18 VDD1V2_DIG					U23 VDDQ_DDR	U24 DDR_A[1]	U25 DDR_A[10]	U26 DDR_D[3]	U27 DDR_D[1]	U
V14 GND	V15 GND	V16 GND	V17 VDD1V2_DIG	V18 VDD1V2_DIG					V23 VDDQ_DDR	V24 DDR_BA[2]	V25 DDR_BA[1]	V26 DDR_D[8]	V27 DDR_D[10]	V
									W23 VDDQ_DDR	W24 DDR_BA[0]	W25 DDR_WEN	W26 DDR_D[14]	W27 DDR_D[12]	W
									Y23 VDDQ_DDR	Y24 DDR_CKE	Y25 DDR_VREF1	Y26 DDR_DQSN[1]	Y27 DDR_DQSP[1]	Y
									AA23 VDDQ_DDR	AA24 GND	AA25 REG_OUT_VDDR	AA26 DDR_DQSN[0]	AA27 DDR_DQSP[0]	AA
									AB23 GND	AB24 LVTX_A_CH0N	AB25 LVTX_A_CH0P	AB26 DDR_DQM[0]	AB27 DDR_DQM[1]	AB
AC14 VDD2V5_PLL	AC15 VDD2V5_PLL	AC16 GND	AC17 VDD2V5_LVDS	AC18 VDD2V5_LVDS	AC19 VDD2V5_LVDS	AC20 VDD2V5_LVDS	AC21 GND	AC22 GND	AC23 GND	AC24 LVTX_A_CH1N	AC25 LVTX_A_CH1P	AC26 DDR_D[9]	AC27 DDR_D[15]	AC
AD14 XTAL	AD15 LVTX_D_CH4N	AD16 LVTX_D_CLKN	AD17 LVTX_D_CH1N	AD18 LVTX_C_CH4N	AD19 LVTX_C_CLKN	AD20 LVTX_C_CH1N	AD21 LVTX_B_CH4N	AD22 LVTX_B_CLKN	AD23 LVTX_B_CH1N	AD24 LVTX_A_CH4N	AD25 LVTX_A_CLKN	AD26 DDR_D[13]	AD27 DDR_D[11]	AD
AE14 TCLK	AE15 LVTX_D_CH4P	AE16 LVTX_D_CLKP	AE17 LVTX_D_CH1P	AE18 LVTX_C_CH4P	AE19 LVTX_C_CLKP	AE20 LVTX_C_CH1P	AE21 LVTX_B_CH4P	AE22 LVTX_B_CLKP	AE23 LVTX_B_CH1P	AE24 LVTX_A_CH4P	AE25 LVTX_A_CLKP	AE26 DDR_D[0]	AE27 DDR_D[2]	AE
AF14 DP_TX0N	AF15 LVTX_D_CH3N	AF16 LVTX_D_CH2N	AF17 LVTX_D_CH0N	AF18 LVTX_C_CH3N	AF19 LVTX_C_CH2N	AF20 LVTX_C_CH0N	AF21 LVTX_B_CH3N	AF22 LVTX_B_CH2N	AF23 LVTX_B_CH0N	AF24 LVTX_A_CH3N	AF25 LVTX_A_CH2N	AF26 DDR_D[6]	AF27 DDR_D[4]	AF
AG14 DP_TX0P	AG15 LVTX_D_CH3P	AG16 LVTX_D_CH2P	AG17 LVTX_D_CH0P	AG18 LVTX_C_CH3P	AG19 LVTX_C_CH2P	AG20 LVTX_C_CH0P	AG21 LVTX_B_CH3P	AG22 LVTX_B_CH2P	AG23 LVTX_B_CH0P	AG24 LVTX_A_CH3P	AG25 LVTX_A_CH2P	AG26 CORE_VDD12_FB	AG27 GND	AG
14	15	16	17	18	19	20	21	22	23	24	25	26	27	

Figure 66. STDP73xx ball out diagram: Top-left quadrant

	1	2	3	4	5	6	7	8	9	10
A	A1 GND	A2 LPM_IR	A3 LPM_GPIO15_SLV1_SCL	A4 LPM_GPIO16_SLV1_SDA	A5 LPM_UDO_GPIO1_SLV4_SDA	A6 LPM_GPIO12_SLV3_SDA	A7 AO_LOUT_L	A8 AO_LINE_L	A9 VGA_B_P	A10 VGA_G_P
B	B1 GPADC_AIN0	B2 LPM_GPIO0	B3 LPM_GPIO5_EDPD3	B4 LPM_GPIO10_HPD1	B5 LPM_UDI_GPIO2_SLV4_SCL	B6 LPM_GPIO11_SLV3_SCL	B7 AO_LOUT_R	B8 AO_LINE_R	B9 VGA_B_N	B10 VGA_G_N
C	C1 GPADC_AIN1	C2 LPM_DPTX_HPD	C3 LPM_GPIO3_EDPD4	C4 LPM_GPIO13_SLV2_SCL	C5 LPM_GPIO8_HPD3	C6 AIP_HS_CS	C7 AO_HP_OUT_L	C8 AO_VREF_L	C9 GND	C10 VDD2V5_LPM_ADC
D	D1 CP0_AUXN	D2 CP0_AUXP	D3 TEST_EN0	D4 LPM_GPIO14_SLV2_SDA	D5 LPM_GPIO9_HPD2	D6 AIP_VS	D7 AO_HP_OUT_R	D8 AO_VREF_H	D9 AUD_VBG	D10 VDD2V5_LPM_ADC
E	E1 CP0_0P	E2 CP0_0N	E3 CP0_REXT	E4 TEST_EN1	E5 VDD1V2_LPM_DIG	E6 VDD1V2_LPM_DIG	E7 VDDA3V3_AUD	E8 VDD3V3_HP_AUD	E9 VDD3V3_HP_AUD	E10 VDD1V2_AUDIO
F	F1 CP0_1P	F2 CP0_1N	F3 LPM_MAIN_POWER_ON	F4 LPM_GPIO7_EDPD1	F5 VDD3V3_LPM_DIG	F6 GND	F7 GND	F8 GND	F9 GND	F10 GND
G	G1 CP0_2P	G2 CP0_2N	G3 LPM_GPIO_19	G4 LPM_GPIO6_EDPD2	G5 VDD2V5_LPM_SAFEMEM	G6 GND	G7 GND	G8 GND	G9 GND	G10 GND
H	H1 CP0_3P	H2 CP0_3N	H3 LPM_GPIO_20	H4 GPADC_AIN2	H5 VDD3V3_LPM_COMBO	H6 GND	H7 GND	H8 VDD1V2_DIG	H9 VDD1V2_DIG	H10 VDD1V2_DIG
J	J1 CP1_AUXN	J2 CP1_AUXP	J3 LPM_CEC	J4 GPADC_AIN3	J5 VDD3V3_LPM_COMBO	J6 GND	J7 GND	J8 VDD1V2_DIG	J9 GND	J10 GND
K	K1 CP1_0P	K2 CP1_0N	K3 GND	K4 GND	K5 VDD3V3_LPM_COMBO	K6 GND	K7 GND	K8 GND	K9 GND	K10 GND

Figure 67. STDP73xx ball out diagram: Top-right quadrant

11	12	13	14	15	16	17	18	19	
A11 VGA_R_P	A12 PB_P	A13 Y_P	A14 PR_P	A15 GPIO79_UDO1_ALT_PWM8	A16 GPIO80_UDI1_ALT_PWM6	A17 GPIO77_UDO0_SHTR_CTL0	A18 GPIO78_UDI0_SHTR_CTL1	A19 GND	A
B11 VGA_R_N	B12 PB_N	B13 Y_N	B14 PR_N	B15 GPIO88_DHS_PWM7	B16 GPIO85_OCMINT_PWM4	B17 GPIO6_PWM9	B18 GPIO5_PWM10	B19 GPIO4_PWM11	B
C11 VDD2V5_LPM_ADC	C12 RESETN	C13 DIN_CK1	C14 DIN_CK0	C15 GPIO86_DCLK_PWM5	C16 GPIO81_PWM0	C17 GPIO82_PWM1	C18 GPIO83_PWM2	C19 GPIO84_PWM3	C
D11 VDD2V5_LPM_ADC	D12 GND	D13 GND	D14 GND	D15 GND	D16 DDR_RASN	D17 GPIO3_PWM12	D18 GPIO2_PWM13	D19 GPIO1_PWM14	D
E11 VDD1V2_LPM_ADC	E12 VDD1V2_LPM_ADC	E13 VDD3V3_DIG	E14 VDD3V3_DIG	E15 VDD3V3_DIG	E16 DDR_CASN	E17 DDR_CSN	E18 DDR_ODT	E19 DDR_CLKP	E
F11 GND	F12 GND	F13 GND	F14 GND	F15 VDD2V5_PLL	F16 DDR_A[0]	F17 DDR_ZQ	F18 DDR_CLKN	F19 DDR_VREF2	F
G11 GND	G12 GND	G13 GND	G14 GND	G15 VDD2V5_PLL	G16 DDR_A[4]	G17 DDR_A[2]	G18 DDR_D[7]	G19 DDR_D[5]	G
H11 VDD1V2_DIG	H12 VDD1V2_DIG	H13 GND	H14 GND	H15 VDDQ_DDR	H16 DDR_A[8]	H17 DDR_A[6]	H18 DDR_D[1]	H19 DDR_D[3]	H
J11 GND	J12 GND	J13 GND	J14 GND	J15 VDDQ_DDR	J16 DDR_A[11]	J17 DDR_A[13]	J18 DDR_D[10]	J19 DDR_D[8]	J
K11 GND	K12 GND	K13 GND	K14 GND	K15 VDDQ_DDR	K16 DDR_A[9]	K17 DDR_A[12]	K18 DDR_D[12]	K19 DDR_D[14]	K

Figure 68. STDP73xx ball out diagram: Bottom-left quadrant

	1	2	3	4	5	6	7	8	9	10
L	L1 CP1_1P	L2 CP1_1N	L3 CP1_REXT	L4 GND	L5 VDD3V3_LPM_COMBO	L6 GND	L7 GND	L8 GND	L9 GND	L10 GND
M	M1 CP1_2P	M2 CP1_2N	M3 DEN_GPIO89_PWM8_I2S_DOUT3	M4 DVS_GPIO87_PWM6_I2S_DOUT0	M5 VDD1V2_LPM_COMBO	M6 GND	M7 GND	M8 GND	M9 GND	M10 GND
N	N1 CP1_3P	N2 CP1_3N	N3 SPI_CSN	N4 SPI_DI	N5 VDD1V2_LPM_COMBO	N6 GND	N7 GND	N8 VDD1V2_DIG	N9 VDD1V2_DIG	N10 VDD1V2_DIG
P	P1 CP2_AUXN	P2 CP2_AUXP	P3 SPI_DO	P4 SPI_CLK	P5 VDD1V2_LPM_COMBO	P6 GND	P7 GND	P8 GND	P9 GND	P10 GND
R	R1 CP2_0P	R2 CP2_0N	R3 SPDIF_OUT	R4 I2S_MCLK_OUT_IN	R5 VDD1V2_LPM_COMBO	R6 VDD1V2_LPM_COMBO	R7 VDD1V2_LPM_COMBO	R8 VDD1V2_DPTX	R9 VDD1V2_DPTX	R10 VDD1V2_DPTX
T	T1 CP2_1P	T2 CP2_1N	T3 CP2_REXT	T4 I2S_CLK_OUT	T5 MSTR0_SDA	T6 VDD3V3_DIG	T7 VDD3V3_DIG	T8 DP_TX_REXT	T9 GND	T10 GND
U	U1 CP2_2P	U2 CP2_2N	U3 I2S_WS_OUT	U4 I2S_DOUT2	U5 MSTR0_SCL	U6 GND	U7 GND	U8 PD_AUXTXN	U9 PD_AUXTXP	U10 VDD2V5_DPTX
V	V1 CP2_3P	V2 CP2_3N	V3 I2S_DOUT1	V4 SPDIF_IN	V5 MSTR1_SCL_PWM15	V6 PBIAS	V7 DP_TX3N	V8 DP_TX2N	V9 DP_TX1N	V10 DP_TX0N
W	W1 GND	W2 I2S_CLK_IN	W3 I2S_WS_IN	W4 I2S_DIN	W5 MSTR1_SDA_SPI_CS1	W6 PPWR	W7 DP_TX3P	W8 DP_TX2P	W9 DP_TX1P	W10 DP_TX0P

Figure 69. STDP73xx ball out diagram: Bottom-right quadrant

	11	12	13	14	15	16	17	18	19	
L	L11 GND	L12 GND	L13 GND	L14 GND	L15 VDDQ_DDR	L16 **DDR_A[7]**	L17 **DDR_A[1]**	L18 **DDR_DQSN[1]**	L19 **DDR_DQSP[1]**	L
M	M11 GND	M12 VDD1V2_DIG	M13 GND	M14 GND	M15 VDDQ_DDR	M16 **DDR_BA[2]**	M17 **DDR_BA[0]**	M18 **DDR_DQSN[0]**	M19 **DDR_DQSP[0]**	M
N	N11 VDD1V2_DIG	N12 VDD1V2_DIG	N13 GND	N14 GND	N15 VDDQ_DDR	N16 **DDR_A[10]**	N17 DDR_BA[1]	N18 **DDR_DQM[0]**	N19 **DDR_DQM[1]**	N
P	P11 GND	P12 GND	P13 GND	P14 GND	P15 VDDQ_DDR	P16 **DDR_A[3]**	P17 **DDR_A[5]**	P18 **DDR_D[9]**	P19 **DDR_D[15]**	P
R	R11 GND	R12 VDD2V5_LVDS	R13 VDD2V5_LVDS	R14 VDD2V5_LVDS	R15 VDD2V5_LVDS	R16 DDR_WEN	R17 **DDR_RESETN**	R18 **DDR_D[13]**	R19 **DDR_D[11]**	R
T	T11 GND	T12 **LVTX_B_CH4P**	T13 **LVTX_B_CLKP**	T14 **LVTX_B_CH1P**	T15 **LVTX_A_CH4P**	T16 **DDR_CKE**	T17 **DDR_VREF1**	T18 **DDR_D[0]**	T19 **DDR_D[2]**	T
U	U11 VDD2V5_PLL	U12 **LVTX_B_CH4N**	U13 **LVTX_B_CLKN**	U14 **LVTX_B_CH1N**	U15 **LVTX_A_CH4N**	U16 **LVTX_A_CLKP**	U17 **LVTX_A_CLKN**	U18 **DDR_D[6]**	U19 **DDR_D[4]**	U
V	V11 **XTAL**	V12 **LVTX_B_CH3P**	V13 **LVTX_B_CH2P**	V14 **LVTX_B_CH0P**	V15 **LVTX_A_CH3P**	V16 **LVTX_A_CH2P**	V17 **LVTX_A_CH1P**	V18 **LVTX_A_CH0P**	V19 REG_OUT_VDDR	V
W	W11 **TCLK**	W12 **LVTX_B_CH3N**	W13 **LVTX_B_CH2N**	W14 **LVTX_B_CH0N**	W15 **LVTX_A_CH3N**	W16 **LVTX_A_CH2N**	W17 **LVTX_A_CH1N**	W18 **LVTX_A_CH0N**	W19 GND	W

5.3 Ball lists

Table 12. DDR interface

Signal	STDP9320/ STDP9310/ STDP9210	STDP7320/ STDP7310	Pullup/ pulldown	Dir	Reset state	Description	Comments
DDR_D[0]	AE26	T18		BIDIR	TRISTATE	DDR DATA[0]	
DDR_D[1]	U27	H18		BIDIR	TRISTATE	DDR DATA[1]	
DDR_D[2]	AE27	T19		BIDIR	TRISTATE	DDR DATA[2]	
DDR_D[3]	U26	H19		BIDIR	TRISTATE	DDR DATA[3]	
DDR_D[4]	AF27	U19		BIDIR	TRISTATE	DDR DATA[4]	
DDR_D[5]	T26	G19		BIDIR	TRISTATE	DDR DATA[5]	
DDR_D[6]	AF26	U18		BIDIR	TRISTATE	DDR DATA[6]	
DDR_D[7]	T27	G18		BIDIR	TRISTATE	DDR DATA[7]	
DDR_D[8]	V26	J19		BIDIR	TRISTATE	DDR DATA[8]	
DDR_D[9]	AC26	P18		BIDIR	TRISTATE	DDR DATA[9]	
DDR_D[10]	V27	J18		BIDIR	TRISTATE	DDR DATA[10]	
DDR_D[11]	AD27	R19		BIDIR	TRISTATE	DDR DATA[11]	
DDR_D[12]	W27	K18		BIDIR	TRISTATE	DDR DATA[12]	
DDR_D[13]	AD26	R18		BIDIR	TRISTATE	DDR DATA[13]	
DDR_D[14]	W26	K19		BIDIR	TRISTATE	DDR DATA[14]	
DDR_D[15]	AC27	P19		BIDIR	TRISTATE	DDR DATA[15]	
DDR_D[16]	N26	-		BIDIR	TRISTATE	DDR DATA[16]	
DDR_D[17]	E27	-		BIDIR	TRISTATE	DDR DATA[17]	
DDR_D[18]	N27	-		BIDIR	TRISTATE	DDR DATA[18]	
DDR_D[19]	E26	-		BIDIR	TRISTATE	DDR DATA[19]	
DDR_D[20]	P27	-		BIDIR	TRISTATE	DDR DATA[20]	
DDR_D[21]	D26	-		BIDIR	TRISTATE	DDR DATA[21]	
DDR_D[22]	P26	-		BIDIR	TRISTATE	DDR DATA[22]	
DDR_D[23]	D27	-		BIDIR	TRISTATE	DDR DATA[23]	
DDR_D[24]	F26	-		BIDIR	TRISTATE	DDR DATA[24]	
DDR_D[25]	L26	-		BIDIR	TRISTATE	DDR DATA[25]	
DDR_D[26]	F27	-		BIDIR	TRISTATE	DDR DATA[26]	
DDR_D[27]	M27	-		BIDIR	TRISTATE	DDR DATA[27]	
DDR_D[28]	G27	-		BIDIR	TRISTATE	DDR DATA[28]	
DDR_D[29]	M26	-		BIDIR	TRISTATE	DDR DATA[29]	
DDR_D[30]	G26	-		BIDIR	TRISTATE	DDR DATA[30]	
DDR_D[31]	L27	-		BIDIR	TRISTATE	DDR DATA[31]	

Table 12. DDR interface

Signal	STDP9320/ STDP9310/ STDP9210	STDP7320/ STDP7310	Pullup/ pulldown	Dir	Reset state	Description	Comments
DDR_DQM[0]	AB26	N18		OUT	TRISTATE	DDR DATA MASK 0	
DDR_DQM[1]	AB27	N19		OUT	TRISTATE	DDR DATA MASK 1	
DDR_DQM[2]	K26	-		OUT	TRISTATE	DDR DATA MASK 2	
DDR_DQM[3]	K27	-		OUT	TRISTATE	DDR DATA MASK 3	
DDR_DQSP[0]	AA27	M19		OUT	TRISTATE	DDR DATA STROBE 0 - DIFFERENTIAL POSITIVE	
DDR_DQSN[0]	AA26	M18		OUT	TRISTATE	DDR DATA STROBE 0 - DIFFERENTIAL NEGATIVE	
DDR_DQSP[1]	Y27	L19		OUT	TRISTATE	DDR DATA STROBE 1 - DIFFERENTIAL POSITIVE	
DDR_DQSN[1]	Y26	L18		OUT	TRISTATE	DDR DATA STROBE 1 - DIFFERENTIAL NEGATIVE	
DDR_DQSP[2]	J27	-		OUT	TRISTATE	DDR DATA STROBE 2 DIFFERENTIAL POSITIVE	
DDR_DQSN[2]	J26	-		OUT	TRISTATE	DDR DATA STROBE 2 DIFFERENTIAL NEGATIVE	
DDR_DQSP[3]	H27	-		OUT	TRISTATE	DDR DATA STROBE 3 DIFFERENTIAL POSITIVE	
DDR_DQSN[3]	H26	-		OUT	TRISTATE	DDR DATA STROBE 3 DIFFERENTIAL NEGATIVE	
DDR_A[0]	K25	F16		OUT	TRISTATE	DDR ADDRESS [0]	
DDR_A[1]	U24	L17		OUT	TRISTATE	DDR ADDRESS [1]	
DDR_A[2]	L24	G17		OUT	TRISTATE	DDR ADDRESS [2]	
DDR_A[3]	T25	P16		OUT	TRISTATE	DDR ADDRESS [3]	
DDR_A[4]	L25	G16		OUT	TRISTATE	DDR ADDRESS [4]	
DDR_A[5]	T24	P17		OUT	TRISTATE	DDR ADDRESS [5]	

Table 12. DDR interface

Signal	STDP9320/ STDP9310/ STDP9210	STDP7320/ STDP7310	Pullup/ pulldown	Dir	Reset state	Description	Comments
DDR_A[6]	M24	H17		OUT	TRISTATE	DDR ADDRESS [6]	
DDR_A[7]	R25	L16		OUT	TRISTATE	DDR ADDRESS [7]	
DDR_A[8]	M25	H16		OUT	TRISTATE	DDR ADDRESS [8]	
DDR_A[9]	P25	K16		OUT	TRISTATE	DDR ADDRESS [9]	
DDR_A[10]	U25	N16		OUT	TRISTATE	DDR ADDRESS [10]	
DDR_A[11]	N25	J16		OUT	TRISTATE	DDR ADDRESS [11]	
DDR_A[12]	P24	K17		OUT	TRISTATE	DDR ADDRESS [12]	
DDR_A[13]	N24	J17		OUT	TRISTATE	DDR ADDRESS [13]	
DDR_BA[0]	W24	M17		OUT	TRISTATE	DDR BANK ADDRESS 0	
DDR_BA[1]	V25	N17		OUT	TRISTATE	DDR BANK ADDRESS 1	
DDR_BA[2]	V24	M16		OUT	TRISTATE	DDR BANK ADDRESS 2	
DDR_CLKP	R27	E19		OUT	TRISTATE	DDR CLOCK OUTPUT DIFFERENTIAL POSITIVE	
DDR_CLKN	R26	F18		OUT	TRISTATE	DDR CLOCK OUTPUT DIFFERENTIAL NEGATIVE	
DDR_CASN	J24	E16		OUT	TRISTATE	DDR COLUMN ADDRESS STROBE	
DDR_RASN	H25	D16		OUT	TRISTATE	DDR ROW ADDRESS STROBE	
DDR_CSN	J25	E17		OUT	TRISTATE	DDR CHIP SELECT	
DDR_CKE	Y24	T16		OUT	TRISTATE	DDR CLOCK ENABLE	
DDR_WEN	W25	R16		OUT	TRISTATE	DDR WRITE ENABLE	
DDR_RESETN	R24	R17		OUT	TRISTATE	DDR3 ACTIVE LOW RESET SIGNAL TO DDR	

Table 12. DDR interface

Signal	STDP9320/ STDP9310/ STDP9210	STDP7320/ STDP7310	Pullup/ pulldown	Dir	Reset state	Description	Comments
DDR_ODT	H24	E18		OUT	TRISTATE	DDR ON DIE TERMINATION OUTPUT	
DDR_ZQ	K24	F17		IN		REFERENCE PIN FOR DDR3 ZQ CALIBRATION	Connected to GND through 240ohm 1% resistor.
DDR_VREF1	Y25	T17		IN		DDR REFERENCE VOLTAGE	Generate from VDDQ using 20K+20K Res Divider. Decouple with Caps to DVDDQ & GND
DDR_VREF2	G25	F19		IN		DDR REFERENCE VOLTAGE	Generate from VDDQ using 20K+20K Res Divider. Decouple with Caps to DVDDQ & GND
REG_OUT_ VDDR	AA25	V19		OUT	OUT	VREF FEEDBACK PIN	Feedback to VDDQ Linear Regulator

Table 13. TTL video input port

Signal	STDP9320/ STDP9310/ STDP9210	STDP7320/ STDP7310	Pullup/ pulldown	Dir	Reset state	Description	Comments
DIN_CK0	A24	C14	PD	IN	IN	3.3V TTL VIDEO INPUT PORT CLOCK0	
DIN_CK1	B24	C13	PD	BIDIR	IN	3.3V TTL VIDEO INPUT PORT CLOCK1 IN	
DIN_ODD	C24	-	PD	BIDIR	IN	3.3V TTL VIDEO INPUT PORT ODD FIELD IN	
DIN_VS	A23	-	PD	BIDIR	IN	3.3V TTL VIDEO INPUT PORT 'VSYNC IN	

Table 13. TTL video input port

Signal	STDP9320/ STDP9310/ STDP9210	STDP7320/ STDP7310	Pullup/ pulldown	Dir	Reset state	Description	Comments
DIN_HS_CS	B23	-	PD	BIDIR	IN	3.3V TTL VIDEO INPUT PORT HSYNC / CSYNC IN	
DIN_HREF_DE	A22	-	PD	BIDIR	IN	3.3V TTL VIDEO INPUT PORT HREF / DE IN	
DIN_0	B22	-	PD	BIDIR	IN	3.3V TTL VIDEO INPUT PORT DATA IN 0	
DIN_1	C22	-	PD	BIDIR	IN	3.3V TTL VIDEO INPUT PORT DATA IN 1	
DIN_2	D22	-	PD	BIDIR	IN	3.3V TTL VIDEO INPUT PORT DATA IN 2	
DIN_3	A21	-	PD	BIDIR	IN	3.3V TTL VIDEO INPUT PORT DATA IN 3	
DIN_4	B21	-	PD	BIDIR	IN	3.3V TTL VIDEO INPUT PORT DATA IN 4	
DIN_5	C21	-	PD	BIDIR	IN	3.3V TTL VIDEO INPUT PORT DATA IN 5	
DIN_6	D21	-	PD	BIDIR	IN	3.3V TTL VIDEO INPUT PORT DATA IN 6	
DIN_7	A20	-	PD	BIDIR	IN	3.3V TTL VIDEO INPUT PORT DATA IN 7	
DIN_8	B20	-	PD	BIDIR	IN	3.3V TTL VIDEO INPUT PORT DATA IN 8	
DIN_9	C20	-	PD	BIDIR	IN	3.3V TTL VIDEO INPUT PORT DATA IN 9	
DIN_10	D20	-	PD	BIDIR	IN	3.3V TTL VIDEO INPUT PORT DATA IN 10	
DIN_11	A19	-	PD	BIDIR	IN	3.3V TTL VIDEO INPUT PORT DATA IN 11	
DIN_12	B19	-	PD	BIDIR	IN	3.3V TTL VIDEO INPUT PORT DATA IN 12	
DIN_13	C19	-	PD	BIDIR	IN	3.3V TTL VIDEO INPUT PORT DATA IN 13	
DIN_14	D19	-	PD	BIDIR	IN	3.3V TTL VIDEO INPUT PORT DATA IN 14	
DIN_15	A18	-	PD	BIDIR	IN	3.3V TTL VIDEO INPUT PORT DATA IN 15	
DIN_16	B18	-	PD	BIDIR	IN	3.3V TTL VIDEO INPUT PORT DATA IN 16	
DIN_17	C18	-	PD	BIDIR	IN	3.3V TTL VIDEO INPUT PORT DATA IN 17	

Table 13. TTL video input port

Signal	STDP9320/ STDP9310/ STDP9210	STDP7320/ STDP7310	Pullup/ pulldown	Dir	Reset state	Description	Comments
DIN_18	D18	-	PD	BIDIR	IN	3.3V TTL VIDEO INPUT PORT DATA IN 18	
DIN_19	A17	-	PD	BIDIR	IN	3.3V TTL VIDEO INPUT PORT DATA IN 19	
DIN_20	B17	-	PD	BIDIR	IN	3.3V TTL VIDEO INPUT PORT DATA IN 20	
DIN_21	C17	-	PD	BIDIR	IN	3.3V TTL VIDEO INPUT PORT DATA IN 21	
DIN_22	A16	-	PD	BIDIR	IN	3.3V TTL VIDEO INPUT PORT DATA IN 22	
DIN_23	B16	-	PD	BIDIR		3.3V TTL VIDEO INPUT PORT DATA IN 23	

Table 14. Analog video input port

Signal	STDP9320/ STDP9310/ STDP9210	STDP7320/ STDP7310	Pullup/ pulldown	Dir	Reset state	Description	Comments
PR_P	A15	A14		IN	IN	ANALOG COMPONENT VIDEO IN CHROMA RED POSITIVE	
PR_N	B15	B14		IN	IN	ANALOG COMPONENT VIDEO IN CHROMA RED NEGATIVE	
Y_P	A14	A13		IN	IN	ANALOG VIDEO IN GREEN / LUMA POSITIVE	
Y_N	B14	B13		IN	IN	ANALOG VIDEO IN GREEN / LUMA NEGATIVE	
PB_P	A13	A12		IN	IN	ANALOG COMPONENT VIDEO IN CHROMA BLUE POSITIVE	
PB_N	B13	B12		IN	IN	ANALOG COMPONENT VIDEO IN CHROMA BLUE NEGATIVE	
VGA_R_P	A12	A11		IN	IN	ANALOG VGA VIDEO IN RED POSITIVE	

Table 14. Analog video input port

Signal	STDP9320/ STDP9310/ STDP9210	STDP7320/ STDP7310	Pullup/ pulldown	Dir	Reset state	Description	Comments
VGA_R_N	B12	B11		IN	IN	ANALOG VGA VIDEO IN RED NEGATIVE	
VGA_G_P	A11	A10		IN	IN	ANALOG VGA VIDEO IN GREEN POSITIVE	
VGA_G_N	B11	B10		IN	IN	ANALOG VGA VIDEO IN GREEN NEGATIVE	
VGA_B_P	A10	A9		IN	IN	ANALOG VGA VIDEO IN BLUE POSITIVE	
VGA_B_N	B10	B9		IN	IN	ANALOG VGA VIDEO IN BLUE NEGATIVE	
AIP_HS_CS	C6	C6		IN	IN	5V Tolerant TTL VGA HSYNC / CSYNC INPUT	5V Tolerant INPUT
AIP_VS	D6	D6		IN	IN	5V Tolerant TTL VGA VSYNC INPUT	5V Tolerant INPUT

Table 15. Analog audio input port

Signal	STDP9320/ STDP9310/ STDP9210	STDP7320/ STDP7310	Dir	Description	Comments
AO_LINE_L	A8	A8	IN	ANALOG AUDIO LINE IN LEFT	1Vpp Input with 1.45V DC Bias. AC Couple using .15uF Cap.
AO_LINE_R	B8	B8	IN	ANALOG AUDIO LINE IN RIGHT	1Vpp Input with 1.45V DC Bias. AC Couple using .15uF Cap.
AUD_VBG	C7	D9	IN	AUDIO 1.26V VREF DECOUPLING	Filter using 10uF Electrolytic Cap & a .1uF Ceramic Cap
AO_VREF_L	C8	C8	OUT	AUDIO 1.47V VREF DECOUPLING	Filter using 10uF Electrolytic Cap & a .1uF Ceramic Cap
AO_VREF_H	D7	D8	OUT	AUDIO 1.62V VREF DECOUPLING	Filter using 10uF Electrolytic Cap & a .1uF Ceramic Cap
AO_LOUT_L	A7	A7	OUT	ANALOG AUDIO LINE OUT LEFT	2Vpp Signal Swing with 5kom load. AC Couple with 1uF cap.
AO_LOUT_R	B7	B7	OUT	ANALOG AUDIO LINE OUT RIGHT	2Vpp Signal Swing with 5kom load. AC Couple with 1uF cap.

Table 15. Analog audio input port

Signal	STDP9320/ STDP9310/ STDP9210	STDP7320/ STDP7310	Dir	Description	Comments
AO_HP_OUT_R	B6	D7	OUT	AUDIO HEADPHONE OUT RIGHT	40mW rms into 16ohm load. AC Couple with 470uF Cap
AO_HP_OUT_L	A6	C7	OUT	AUDIO HEADPHONE OUT LEFT	40mW rms into 16ohm load. AC Couple WITH 470uF Cap

Table 16. LPM general purpose ADC

Signal	STDP9320/ STDP9310/ STDP9210	STDP7320/ STDP7310	Dir	Reset state	Description	Comments
GPADC_AIN0	E3	B1	BIDIR	IN	3V3 FS OD DIG BIDIR - ANA_IN	3.3V I/O FAILSAFE OPENDRAIN
GPADC_AIN1	F1	C1	BIDIR	IN	3V3 FS OD DIG BIDIR - ANA_IN	3.3V I/O FAILSAFE OPENDRAIN
GPADC_AIN2	F2	H4	BIDIR	IN	3V3 FS OD DIG BIDIR - ANA_IN	3.3V I/O FAILSAFE OPENDRAIN
GPADC_AIN3	F3	J4	BIDIR	IN	3V3 FS OD DIG BIDIR - ANA_IN	3.3V I/O FAILSAFE OPENDRAIN

Table 17. LPM digital inputs and outputs

Signal	STDP9320/ STDP9310/ STDP9210	STDP7320/ STDP7310	Pullup/ pullldown	Dir	Reset state	Description	Comments	Recommended functional mode usage of GPIO MFP pin
LPM_GPIO12_SLV3_SDA	A5	A6		BIDIR	IN	LPM_GPIO 12 or I2C SLAVE3 SDA	3.3V Tolerant FAILSAFE DIGITAL I/O	COMBO PORT 3 DDC I2C SLAVE SDA (DP/ HDMI/DVI)
LPM_GPIO11_SLV3_SCL	B5	B6		BIDIR	IN	LPM_GPIO 11 or I2C SLAVE3 SCL	3.3V Tolerant FAILSAFE DIGITAL I/O	COMBO PORT 3 DDC I2C SLAVE SCL (DP/HDMI/DVI)
LPM_UDO_GPIO1_SLV4_SDA	C5	A5		BIDIR	IN	LPM_GPIO 1 / LPM OCM UART TX / I2C SLAVE4 SDA	3.3V Tolerant FAILSAFE DIGITAL I/O	VGA PORT DDC I2C SLAVE SDA

Table 17. LPM digital inputs and outputs

Signal	STDP9320/ STDP9310/ STDP9210	STDP7320/ STDP7310	Pullup/ pullldown	Dir	Reset state	Description	Comments	Recommended functional mode usage of GPIO MFP pin
LPM_UDI _GPIO2_ SLV4_SC L	D5	B5		BIDIR	IN	LPM_GPIO 2 / LPM OCM UART RX / I2C SLAVE4 SCL	3.3V Tolerant FAILSAFE DIGITAL I/O	VGA PORT DDC I2C SLAVE SCL
LPM_GPI O8_HPD3	A4	C5		BIDIR	IN	LPM_GPIO 8 / HPD OUT 3	3.3V DIGITAL I/O	COMBO PORT3 HPD OUT
LPM_GPI O9_HPD2	B4	D5		BIDIR	IN	LPM_GPIO 9 / HPD OUT 2	3.3V DIGITAL I/O	COMBO PORT2 HPD OUT
LPM_GPI O15_SLV 1_SCL	C4	A3		BIDIR	IN	LPM_GPIO 15 / I2C SLAVE 1 SCL	3.3V Tolerant FAILSAFE DIGITAL I/O	COMBO PORT1 DDC I2C SLAVE SCL (DP/ HDMI/DVI)
LPM_GPI O16_SLV 1_SDA	D4	A4		BIDIR	IN	LPM_GPIO 16 / I2C SLAVE 1 SDA	3.3V Tolerant FAILSAFE DIGITAL I/O	COMBO PORT1 DDC I2C SLAVE SDA (DP/ HDMI/DVI)
LPM_GPI O13_SLV 2_SCL	A3	C4		BIDIR	IN	LPM_GPIO 13 / I2C SLAVE2 SCL	3.3V Tolerant FAILSAFE DIGITAL I/O	COMBO PORT2 DDC I2C SLAVE SCL (DP/ HDMI/DVI)
LPM_GPI O14_SLV 2_SDA	B3	D4		BIDIR	IN	LPM_GPIO 14 / I2C SLAVE2 SDA	3.3V Tolerant FAILSAFE DIGITAL I/O	COMBO PORT2 DDC I2C SLAVE SDA (DP/ HDMI/DVI)
LPM_GPI O10_HPD 1	C3	B4		BIDIR	IN	LPM_GPIO 10 / HPD OUT 1	3.3V DIGITAL I/O	COMBO PORT1 HPD OUT
LPM_GPI O7_EDPD 1	D3	F4		BIDIR	IN	LPM_GPIO 7 / EPROM DISABLE 1 / POWER DETECT 1 PIN	3.3V DIGITAL I/O	CABLE DETECT INPUT1

Table 17. LPM digital inputs and outputs

Signal	STDP9320/ STDP9310/ STDP9210	STDP7320/ STDP7310	Pullup/ pullldown	Dir	Reset state	Description	Comments	Recommended functional mode usage of GPIO MFP pin
LPM_GPIO6_EDPD2	A2	G4		BIDIR	IN	LPM_GPIO 6 / EPROM DISABLE 2 / POWER DETECT 2 PIN	3.3V DIGITAL I/O	CABLE DETECT INPUT2
LPM_GPIO5_EDPD3	B1	B3		BIDIR	IN	LPM_GPIO 5 / EPROM DISABLE 3 / POWER DETECT 3 PIN	3.3V DIGITAL I/O	CABLE DETECT INPUT3
LPM_GPIO3_EDPD4	B2	C3		BIDIR	IN	LPM_GPIO 3 / EPROM DISABLE 4 / POWER DETECT 4 PIN	3.3V DIGITAL I/O	CABLE DETECT INPUT4
LPM_MAIN_POWER_ON	C1	F3	PU	BIDIR	OUT	LPM_GPIO 18 / MISSION POWER ON CONTROL OUT PIN	3.3V DIGITAL I/O	MISSION POWER-ON CONTROL OUTPUT
LPM_GPIO_19	C2	G3	PD	BIDIR	IN	LPM_GPIO 19 PIN	3.3V DIGITAL I/O	LED1 DRIVE OUTPUT
LPM_GPIO_20	D1	H3	PD	BIDIR	IN	LPM_GPIO 20 PIN	3.3V DIGITAL I/O	LED2 DRIVE OUTPUT
LPM_IR	D2	A2	PD	IN	IN	IR INPUT PORT PIN	3.3V DIGITAL I/O	IR INPUT PORT
LPM_GPIO0	E1	B2	PD	BIDIR	IN	LPM GPIO10	3.3V DIGITAL I/O	SPARE GPIO
LPM_DPTX_HPD	E2	C2		BIDIR	IN	TX_HPD DETECT INPUT	3.3V DIGITAL I/O	DPTX HPD DETECT INPUT
LPM_CEC	G4	J3		BIDIR	IN	LPM CEC INTERFACE PIN	3.3V Tolerant FAILSAFE DIGITAL I/O	CEC INTERFACE I/O

Table 18. DP/HDMI/DVI combo analog receivers

Signal	STDP9320/ STDP9310/ STDP9210	STDP7320/ STDP7310	Dir	Reset state	Description	Comments
CP0_AUXP	G2	D2	IN	IN	COMBO PHY0 AUX POSITIVE INPUT	3.3V Tolerant ANALOG INPUT
CP0_AUXN	G1	D1	IN	IN	COMBO PHY0 AUX NEGATIVE INPUT	3.3V Tolerant ANALOG INPUT
CP0_REXT	G3	E3	IN	IN	Combo PHY0 External resistor for the termination calibration circuit	REXT 249 ohm Resistor to VDD33.
CP0_0P	H1	E1	IN	IN	COMBO PHY0 LANE_0 POSITIVE INPUT	3.3V Tolerant ANALOG INPUT
CP0_0N	H2	E2	IN	IN	COMBO PHY0 LANE_0 NEGATIVE INPUT	3.3V Tolerant ANALOG INPUT
CP0_1P	J1	F1	IN	IN	COMBO PHY0 LANE_1 POSITIVE INPUT	3.3V Tolerant ANALOG INPUT
CP0_1N	J2	F2	IN	IN	COMBO PHY0 LANE_1 NEGATIVE INPUT	3.3V Tolerant ANALOG INPUT
CP0_2P	K1	G1	IN	IN	COMBO PHY0 LANE_2 POSITIVE INPUT	3.3V Tolerant ANALOG INPUT
CP0_2N	K2	G2	IN	IN	COMBO PHY0 LANE_2 NEGATIVE INPUT	3.3V Tolerant ANALOG INPUT
CP0_3P	L1	H1	IN	IN	COMBO PHY0 LANE_3 POSITIVE INPUT	3.3V Tolerant ANALOG INPUT
CP0_3N	L2	H2	IN	IN	COMBO PHY0 LANE_3 NEGATIVE INPUT	3.3V Tolerant ANALOG INPUT
CP1_AUXP	M2	J2	IN	IN	COMBO PHY1 AUX POSITIVE INPUT	3.3V Tolerant ANALOG INPUT
CP1_AUXN	M1	J1	IN	IN	COMBO PHY1 AUX NEGATIVE INPUT	3.3V Tolerant ANALOG INPUT
CP1_REXT	M3	L3	IN	IN	Combo PHY1 External resistor for the termination calibration circuit	REXT 249 ohm Resistor to VDD33.
CP1_0P	N1	K1	IN	IN	COMBO PHY1 LANE_0 POSITIVE INPUT	3.3V Tolerant ANALOG INPUT
CP1_0N	N2	K2	IN	IN	COMBO PHY1 LANE_0 NEGATIVE INPUT	3.3V Tolerant ANALOG INPUT
CP1_1P	P1	L1	IN	IN	COMBO PHY1 LANE_1 POSITIVE INPUT	3.3V Tolerant ANALOG INPUT
CP1_1N	P2	L2	IN	IN	COMBO PHY1 LANE_1 NEGATIVE INPUT	3.3V Tolerant ANALOG INPUT
CP1_2P	R1	M1	IN	IN	COMBO PHY1 LANE_2 POSITIVE INPUT	3.3V Tolerant ANALOG INPUT

Table 18. DP/HDMI/DVI combo analog receivers

Signal	STDP9320/ STDP9310/ STDP9210	STDP7320/ STDP7310	Dir	Reset state	Description	Comments
CP1_2N	R2	M2	IN	IN	COMBO PHY1 LANE_2 NEGATIVE INPUT	3.3V Tolerant ANALOG INPUT
CP1_3P	T1	N1	IN	IN	COMBO PHY1 LANE_3 POSITIVE INPUT	3.3V Tolerant ANALOG INPUT
CP1_3N	T2	N2	IN	IN	COMBO PHY1 LANE_3 NEGATIVE INPUT	3.3V Tolerant ANALOG INPUT
CP2_AUXP	U2	P2	IN	IN	COMBO PHY2 AUX POSITIVE INPUT	3.3V Tolerant ANALOG INPUT
CP2_AUXN	U1	P1	IN	IN	COMBO PHY2 AUX NEGATIVE INPUT	3.3V Tolerant ANALOG INPUT
CP2_REXT	U3	T3	IN	IN	Combo PHY2 External resistor for the termination calibration circuit	REXT 249 ohm Resistor to VDD33.
CP2_0P	V1	R1	IN	IN	COMBO PHY2 LANE_0 POSITIVE INPUT	3.3V Tolerant ANALOG INPUT
CP2_0N	V2	R2	IN	IN	COMBO PHY2 LANE_0 NEGATIVE INPUT	3.3V Tolerant ANALOG INPUT
CP2_1P	W1	T1	IN	IN	COMBO PHY2 LANE_1 POSITIVE INPUT	3.3V Tolerant ANALOG INPUT
CP2_1N	W2	T2	IN	IN	COMBO PHY2 LANE_1 NEGATIVE INPUT	3.3V Tolerant ANALOG INPUT
CP2_2P	Y1	U1	IN	IN	COMBO PHY2 LANE_2 POSITIVE INPUT	3.3V Tolerant ANALOG INPUT
CP2_2N	Y2	U2	IN	IN	COMBO PHY2 LANE_2 NEGATIVE INPUT	3.3V Tolerant ANALOG INPUT
CP2_3P	AA1	V1	IN	IN	COMBO PHY2 LANE_3 POSITIVE INPUT	3.3V Tolerant ANALOG INPUT
CP2_3N	AA2	V2	IN	IN	COMBO PHY2 LANE_3 NEGATIVE INPUT	3.3V Tolerant ANALOG INPUT

Table 19. Mission multi-function digital

Signal	STDP9320/ STDP9310/ STDP9210	STDP7320/ STDP7310	Pullup/ pullldown	Dir	Reset state	Description	Recommended functional mode usage of GPIO MFP pin
GPIO1_PWM14	G24	D19	PD	BIDIR	IN	GPIO1 / PWM14 / SHUTTER CTRL1	3D SHUTTER CONTROL SHTR_CTL1
GPIO2_PWM13	F25	D18	PD	BIDIR	IN	GPIO2 / PWM13 / SHUTTER CTRL0	3D SHUTTER CONTROL SHTR_CTL0

Table 19. Mission multi-function digital

Signal	STDP9320/ STDP9310/ STDP9210	STDP7320/ STDP7310	Pullup/ pullldown	Dir	Reset state	Description	Recommended functional mode usage of GPIO MFP pin
GPIO3_PWM12	F24	D17	PD	BIDIR	IN	GPIO3 / PWM12	SCANNING BACKLIGHT PWM12
GPIO84_PWM3	E25	C19	PD	BIDIR	IN	GPIO84 / PWM3	SCANNING BACKLIGHT OR GENERAL PWM3
GPIO83_PWM2	E24	C18	PD	BIDIR	IN	GPIO83 / PWM2	SCANNING BACKLIGHT OR GENERAL PWM2
GPIO82_PWM1	D25	C17	PD	BIDIR	IN	GPIO82 / PWM1	SCANNING BACKLIGHT OR GENERAL PWM1
GPIO81_PWM0	D24	C16	PD	BIDIR	IN	GPIO81 / PWM0	SCANNING BACKLIGHT OR GENERAL PWM0
GPIO4_PWM11	C27	B19	PD	BIDIR	IN	GPIO4 / PWM11	AUDIO MUTE
GPIO5_PWM10	C26	B18	PD	BIDIR	IN	GPIO5 / PWM10	SCANNING BACKLIGHT PWM10
GPIO6_PWM9	C25	B17	PD	BIDIR	IN	GPIO6 / PWM9	SCANNING BACKLIGHT PWM9
GPIO85_OCMINT_PWM4	B27	B16	PD	BIDIR	IN	GPIO85 / OCMINT / PWM4	SCANNING BACKLIGHT OR GENERAL PWM4
GPIO78_UDI0_SHTR_CTL1	A26	A18	PD	BIDIR	IN	GPIO78 / UART0 RX / SHUTTER CTRL1	GPROBE RX
GPIO77_UDO0_SHTR_CTL0	B26	A17	PD	BIDIR	IN	GPIO77 / UART0 TX / SHUTTER CTRL0	GPROBE TX
GPIO80_UDI1_ALT_PWM6	A25	A16	PD	BIDIR	IN	GPIO80 / UART1 RX / ALT PWM6	SCANNING BACKLIGHT PWM6
GPIO79_UDO1_ALT_PWM8	B25	A15	PD	BIDIR	IN	GPIO79 / UART1 TX / PWM8	SCANNING BACKLIGHT PWM8

Table 19. Mission multi-function digital

Signal	STDP9320/ STDP9310/ STDP9210	STDP7320/ STDP7310	Pullup/ pullldown	Dir	Reset state	Description	Recommended functional mode usage of GPIO MFP pin
GPIO88_DHS_ PWM7	C23	B15	PD	BIDIR	IN	GPIO88 / DISPLAY HS / PWM7	SCANNING BACKLIGHT PWM7
GPIO86_DCLK _PWM5	D23	C15	PD	BIDIR	IN	GPIO86 / DISPLAY CLOCK / PWM5	SCANNING BACKLIGHT PWM5
I2S_DIN	AB1	W4	PD	IN	IN	AUDIO I2S INTERFACE DATA IN	INPUT I2S AUDIO DATA
I2S_WS_IN	AB2	W3	PD	IN	IN	AUDIO I2S INTERFACE WORD SYNC IN	INPUT I2S AUDIO WORD SYNC
I2S_CLK_IN	AB3	W2	PD	IN	IN	AUDIO I2S INTERFACE CLOCK IN	INPUT I2S AUDIO CLOCK
SPDIF_IN	AB4	V4	PD	IN	IN	AUDIO SPDIF INTERFACE INPUT	INPUT SPDIF INTERFACE
I2S_DOUT1	AC1	V3	PD	OUT	IN	AUDIO I2S INTERFACE DATA1 OUT	OUTPUT I2S DATA1
I2S_DOUT2	AC2	U4	PD	OUT	IN	AUDIO I2S INTERFACE DATA2 OUT	OUTPUT I2S DATA2
I2S_WS_OUT	AC3	U3	PD	OUT	IN	AUDIO I2S INTERFACE WORD SYNC OUT	OUTPUT I2S WORD SYNC
I2S_CLK_OUT	AC4	T4	PD	OUT	IN	AUDIO I2S INTERFACE CLOCK OUT	OUTPUT I2S CLOCK
I2S_MCLK_OU T_IN	AD1	R4	PD	BIDIR	IN	AUDIO I2S INTERFACE MASTER CLOCK	OUTPUT I2S MCLK I/O
SPDIF_OUT	AD2	R3	PD	OUT	IN	AUDIO SPDIF INTERFACE OUTPUT	OUTPUT SPDIF INTERFACE
DVS_GPIO87_ PWM6_I2S_DO UT0	AF1	M4	PD	BIDIR	IN	GPIO87 / DISPLAY VSYNC OUT / PWM6 / I2S DOUT0	OUTPUT I2S DATA0

Table 19. Mission multi-function digital

Signal	STDP9320/ STDP9310/ STDP9210	STDP7320/ STDP7310	Pullup/ pullldown	Dir	Reset state	Description	Recommended functional mode usage of GPIO MFP pin
DEN_GPIO89_ PWM8_I2S_DO UT3	AF2	M3	PD	BIDIR	IN	GPIO89 / PWM8 / I2S DOUT3	OUTPUT I2S DATA3
MSTR1_SDA_S PI_CS1	AG2	W5	PD	BIDIR	IN	GPIO71 / I2C MASTER1 SDA / SPI_CS1	SPI INTERFACE CS1 OUT
MSTR1_SCL_P WM15	AG3	V5	PD	BIDIR	IN	GPIO72 / I2C MASTER1 SCL / PWM15	SCANNING BACKLIGHT PWM15
MSTR0_SCL	AF3	U5	PD	BIDIR	IN	GPIO70 / I2C MASTER0 SCL	I2C MASTER SCL
MSTR0_SDA	AG4	T5	PD	BIDIR	IN	GPIO69 / I2C MASTER0 SDA	I2C MASTER SDA

Note: MSTR1_SDA, MSTR1_SCL, MSTR0_SDA, and MSTR0_SCL are 3.3V tolerant, failsafe pads.

Table 20. System control

Signal	STDP9320/ STDP9310/ STDP9210	STDP7320/ STDP7310	Pullup/ pulldown	Dir	Reset state	Description	Comments
RESETN	D17	C12		BIDIR		ACTIVE LOW RESET I/O	Drive Low with Open_Drain Logic or Push Button to GND
TEST_EN0	E4	D3	PD	IN		TEST ENABLE0 INPUT	3.3V DIGITAL INPUT
TEST_EN1	F4	E4	PD	IN		TEST ENABLE1 INPUT	3.3V DIGITAL INPUT
PBIAS	AG5	V6	PD	OUT	IN	PANEL BACKLIGHT BIAS CONTROL OUTPUT PIN	3.3V DIGITAL OUTPUT
PPWR	AF4	W6	PD	OUT	IN	PANEL POWER CONTROL OUTPUT PIN	3.3V DIGITAL OUTPUT
SPI_CLK	AD3	P4	PD	OUT	IN	SPI INTERFACE CLOCK OUT PIN	3.3V DIGITAL OUTPUT
SPI_DO	AD4	P3	PU	OUT	IN	SPI INTERFACE DATA OUT PIN	3.3V DIGITAL OUTPUT
SPI_DI	AE1	N4	PU	IN	IN	SPI INTERFACE DATA IN PIN	3.3V DIGITAL INPUT

Table 20. System control

Signal	STDP9320/ STDP9310/ STDP9210	STDP7320/ STDP7310	Pullup/ pulldown	Dir	Reset state	Description	Comments
SPI_CSN	AE2	N3	PU	OUT	IN	SPI INTERFACE CHIP SELECT OUT PIN	3.3V DIGITAL OUTPUT
TCLK	AE14	W11		IN	IN	TCLK INPUT	1.2V TOLERANT ANALOG INPUT
XTAL	AD14	V11		IN	IN	CRYSTAL OSCILLATOR INPUT	1.2V TOLERANT ANALOG INPUT

Table 21. DisplayPort analog transmitter

Signal	STDP9320/ STDP9310/ STDP9210	STDP7320/ STDP7310	Dir	Reset State	Description	Comments
DP_TX_REXT	AE10	T8	IN		DISPLAYPORT TRANSMITTER EXTERNAL TERMINATION CALIBRATION RESISTOR PIN	Connect to VDD1V2_DPTX using a 1% 249 ohm resistor.
DP_AUXTXP	AG10	U9	BIDIR	TRISTATE	DISPLAYPORT TRANSMITTER AUX POSITIVE PIN	1.2V TOLERANT ANALOG I/O
DP_AUXTXN	AF10	U8	BIDIR	TRISTATE	DISPLAYPORT TRANSMITTER AUX NEGATIVE PIN	1.2V TOLERANT ANALOG I/O
DP_TX3N	AF11	V7	OUT	TRISTATE	DISPLAYPORT TRANSMITTER LANE3 NEGATIVE	1.2V TOLERANT ANALOG OUTPUT
DP_TX3P	AG11	W7	OUT	TRISTATE	DISPLAYPORT TRANSMITTER LANE3 POSITIVE	1.2V TOLERANT ANALOG OUTPUT
DP_TX2N	AF12	V8	OUT	TRISTATE	DISPLAYPORT TRANSMITTER LANE2 NEGATIVE	1.2V TOLERANT ANALOG OUTPUT
DP_TX2P	AG12	W8	OUT	TRISTATE	DISPLAYPORT TRANSMITTER LANE2 POSITIVE	1.2V TOLERANT ANALOG OUTPUT
DP_TX1N	AF13	V9	OUT	TRISTATE	DISPLAYPORT TRANSMITTER LANE1 NEGATIVE	1.2V TOLERANT ANALOG OUTPUT
DP_TX1P	AG13	W9	OUT	TRISTATE	DISPLAYPORT TRANSMITTER LANE1 POSITIVE	1.2V TOLERANT ANALOG OUTPUT

Table 21. DisplayPort analog transmitter

Signal	STDP9320/ STDP9310/ STDP9210	STDP7320/ STDP7310	Dir	Reset State	Description	Comments
DP_TX0N	AF14	V10	OUT	TRISTATE	DISPLAYPORT TRANSMITTER LANE0 NEGATIVE	1.2V TOLERANT ANALOG OUTPUT
DP_TX0P	AG14	W10	OUT	TRISTATE	DISPLAYPORT TRANSMITTER LANE0 POSITIVE	1.2V TOLERANT ANALOG OUTPUT

Table 22. LVDS analog transmitter

Signal	STDP9320/ STDP9310/ STDP9210	STDP7320/ STDP7310	Dir	Reset State	Description	Comments
LVTX_D_CH4P	AE15	-	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK D, CH 4+	Not Available on STDP73xx
LVTX_D_CH4N	AD15	-	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK D, CH 4 -	Not Available on STDP73xx
LVTX_D_CH3P	AG15	-	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK D, CH 3+	Not Available on STDP73xx
LVTX_D_CH3N	AF15	-	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK D, CH 3 -	Not Available on STDP73xx
LVTX_D_CLKP	AE16	-	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK D, CLK+	Not Available on STDP73xx
LVTX_D_CLKN	AD16	-	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK D, CLK -	Not Available on STDP73xx
LVTX_D_CH2P	AG16	-	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK D, CH 2+	Not Available on STDP73xx
LVTX_D_CH2N	AF16	-	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK D, CH 2 -	Not Available on STDP73xx
LVTX_D_CH1P	AE17	-	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK D, CH 1+	Not Available on STDP73xx
LVTX_D_CH1N	AD17	-	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK D, CH 1 -	Not Available on STDP73xx

Table 22. LVDS analog transmitter

Signal	STDP9320/ STDP9310/ STDP9210	STDP7320/ STDP7310	Dir	Reset State	Description	Comments
LVTX_D_CH0P	AG17	-	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK D, CH 0+	Not Available on STDP73xx
LVTX_D_CH0N	AF17	-	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK D, CH 0 -	Not Available on STDP73xx
LVTX_C_CH4P	AE18	-	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK C, CH 4+	Not Available on STDP73xx
LVTX_C_CH4N	AD18	-	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK C, CH 4 -	Not Available on STDP73xx
LVTX_C_CH3P	AG18	-	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK C, CH 3+	Not Available on STDP73xx
LVTX_C_CH3N	AF18	-	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK C, CH 3 -	Not Available on STDP73xx
LVTX_C_CLKP	AE19	-	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK C, CLK+	Not Available on STDP73xx
LVTX_C_CLKN	AD19	-	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK C, CLK -	Not Available on STDP73xx
LVTX_C_CH2P	AG19	-	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK C, CH 2+	Not Available on STDP73xx
LVTX_C_CH2N	AF19	-	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK C, CH 2 -	Not Available on STDP73xx
LVTX_C_CH1P	AE20	-	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK C, CH 1+	Not Available on STDP73xx
LVTX_C_CH1N	AD20	-	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK C, CH 1 -	Not Available on STDP73xx
LVTX_C_CH0P	AG20	-	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK C, CH 0+	Not Available on STDP73xx
LVTX_C_CH0N	AF20	-	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK C, CH 0 -	Not Available on STDP73xx

Table 22. LVDS analog transmitter

Signal	STDP9320/ STDP9310/ STDP9210	STDP7320/ STDP7310	Dir	Reset State	Description	Comments
LVTX_B_CH4P	AE21	T12	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK B, CH 4+	
LVTX_B_CH4N	AD21	U12	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK B, CH 4 -	
LVTX_B_CH3P	AG21	V12	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK B, CH 3+	
LVTX_B_CH3N	AF21	W12	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK B, CH 3 -	
LVTX_B_CLKP	AE22	T13	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK B, CLK+	
LVTX_B_CLKN	AD22	U13	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK B, CLK -	
LVTX_B_CH2P	AG22	V13	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK B, CH 2+	
LVTX_B_CH2N	AF22	W13	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK B, CH 2 -	
LVTX_B_CH1P	AE23	T14	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK B, CH 1+	
LVTX_B_CH1N	AD23	U14	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK B, CH 1 -	
LVTX_B_CH0P	AG23	V14	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK B, CH 0+	
LVTX_B_CH0N	AF23	W14	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK B, CH 0 -	
LVTX_A_CH4P	AE24	T15	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK A, CH 4+	
LVTX_A_CH4N	AD24	U15	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK A, CH 4 -	

Table 22. LVDS analog transmitter

Signal	STDP9320/ STDP9310/ STDP9210	STDP7320/ STDP7310	Dir	Reset State	Description	Comments
LVTX_A_CH3P	AG24	V15	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK A, CH 3+	
LVTX_A_CH3N	AF24	W15	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK A, CH 3 -	
LVTX_A_CLKP	AE25	U16	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK A, CLK+	
LVTX_A_CLKN	AD25	U17	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK A, CLK -	
LVTX_A_CH2P	AG25	V16	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK A, CH 2+	
LVTX_A_CH2N	AF25	W16	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK A, CH 2 -	
LVTX_A_CH1P	AC25	V17	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK A, CH 1+	
LVTX_A_CH1N	AC24	W17	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK A, CH 1 -	
LVTX_A_CH0P	AB25	V18	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK A, CH 0+	
LVTX_A_CH0N	AB24	W18	OUT	TRISTATE	2.5V LVDS TX DIFFERENTIAL OUTPUT LINK A, CH 0 -	

Table 23. Power supplies

Signal	STDP9320/STDP9310/ STDP9210	STDP7320/STDP7310	Description	Comments
GND	M17, N16, N17, T17, U17, P16, P17, R17, R16, M16, H23, F23, E23, E16, E17, E18, E19, D11, A27, E20, C16, D14, D16, E9, D15, D13, D12, C11, C10, D10, D9, C9, B9, A9, AD5, AD6, AE5, AE6, AF6, AG6, J5, J4, H4, H3, J3, L3, L4, M4, N3, P3, R3, T3, N4, U4, V3, W3, Y3, AA3, AE4, AC6, AF9, AD10, AE9, AD11, AD9, AE12, AE11, AE13, AD13, AC12, AD12, AC16, AC21, AC22, AA24, AB23, AC23, K3, K4, K12, K13, K14, K15, K16, L11, L12, L13, L14, L15, L16, L17, M11, M12, M13, M14, M15, N11, N12, N13, N14, N15, P11, P12, P13, P14, P15, R11, R12, R13, R14, R15, T11, T12, T13, T14, T15, T16, U11, U12, U13, U14, U15, U16, V12, V13, V14, V15, V16, P4, R4, R5, T4, V4, W4, Y4, AA4, AC7, AC8, AD7, AD8, AE7, AE8, AF7, AF8 ,A1, AG1, AE3, AF5, AC5, AB5, C12, C13, C14, C15, AG27	A1,W1,A19,W19,C9, D12,D13,D14,D15,F6, F7,F8,F9,F10,F11,F12, F13,F14,G6,G7,G8, G9,G10,G11,G12,G13, G14,H6,H7,H13,H14, J6,J7,J9,J10,J11,J12, J13,J14,K3,K4, K6,K7, K8,K9,K10,K11,K12, K13,K14,L4,L6,L7,L8, L9,L10,L11, L12,L13, L14,M6,M7, M8,M9, M10,M11,M13,M14,N6 N7,N13, N14,P6,P7, P8,P9,P10,P11,P12, P13,P14,R11,T9,T10, T11,U6, U7	COMMON GND	
VDD1V2_DIG	M18, R18, N18, P18, T18, R10, L18, K17, K18, K11, K10, V17, V11, U18, V18, L10, M10, N10, P10, T10, U10, V10	H8, H9, H10, H11, H12, J8, N8, N9, N10, N11, N12, M12	1.2V MISSION CORE VDD SUPPLY	Decouple with .1uF Ceramic Cap.
VDDQ_DDR	J23, K23, L23, M23, N23, P23, R23, W23, V23, Y23, U23, T23, AA23	H15, J15, K15, L15, M15, N15, P15	VDDQ DDR IO VDD.	1.8V for DDR2. 1.5V for DDR3. Decouple with .1uF Ceramic Cap.
VDD2V5_PLL	G23, AC14, AC15	F15, G15, U11	PLL 2.5V ANALOG SUPPLY	Decouple with .1uF Ceramic Cap.

Table 23. Power supplies

Signal	STDP9320/STDP9310/ STDP9210	STDP7320/STDP7310	Description	Comments
VDD3V3_DIG	E22, E21, AG7, AG8, AG9	T6,T7, E13,E14, E15	3.3V DIGITAL IO VDD SUPPLY	Decouple with .1uF Ceramic Cap.
VDD1V2_LPM_ADC	E11, E10	E11, E12	ADC 1.2V ANALOG SUPPLY In LPM Power Domain	Decouple with .1uF Ceramic Cap.
VDD2V5_LPM_ADC	E12, E13, E14, E15	C10, C11, D10, D11	ADC 2.5V ANALOG SUPPLY IN LPM Power Domain	Filter using Ferrite Bead & decoupling Caps
VDD1V2_AUDIO	E8	E10	AUDIO 1.2V LOGIC SUPPLY	Filter using 10uF Electrolytic Cap with a .1uF Ceramic Cap in parallel.
VDDA3V3_AUD	D8	E7	AUDIO 3.3V ANALOG SUPPLY	Filter using 10uF Electrolytic Cap with a .1uF Ceramic Cap in parallel.
VDD3V3_HP_AUD	E6, E7	E8, E9	AUDIO 3.3V HEADPHONE ANALOG SUPPLY	Decouple The rail using 10uF Electrolytic. Add .1 uF Ceramic for each pin.
VDD1V2_LPM_DIG	E5, F5	E5, E6	1.2V LPM CORE VDD SUPPLY	1.2V LPM CORE LOGIC POWER RAIL is ISOLATED FROM MISSION POWER RAIL.
VDD3V3_LPM_DIG	G5	F5	3.3V DIGITAL IO SUPPLY in LPM Power Domain	Decouple with .1uF Ceramic Cap.
VDD2V5_LPM_SAFEMEM	H5	G5	2.5V POWER SUPPLY TO INTERNAL SAFEMEM OTP MEMORY.	Needs to be sequenced to turn on 10us after VDD12_LPM_DIG. Decouple with 10uF & .1uF
VDD1V2_LPM_COMBO	T5, U5, V5, W5, Y5,AA5	M5, N5, P5, R5, R6, R7	1.2V COMBO PHY ANALOG SUPPLY IN LPM POWER DOMAIN	Decouple with .1uF Ceramic Cap.
VDD3V3_LPM_COMBO	L5, K5, M5, N5, P5	H5, J5, K5, L5	3.3V LPM COMBO PHY ANALOG SUPPLY	Decouple with .1uF Ceramic Cap.
VDD1V2_DPTX	AC9, AC10,AC11	R8, R9, R10	DISPLAYPORT ANALOG 1.2V SUPPLY PIN	Decouple with .1uF Ceramic Cap.

Table 23. Power supplies

Signal	STDP9320/STDP9310/ STDP9210	STDP7320/STDP7310	Description	Comments
VDD2V5_LVDS	AC17, AC18, AC19, AC20	R12, R13, R14, R15	2.5V LVDS PHY ANALOG SUPPLY PIN	Decouple with .1uF Ceramic Cap.
CORE_VDD12_FB	AG26	-	CORE VDD1.2V FEEDBACK	Decouple with .1uF Ceramic Cap.
VDD2V5_DPTX	AC13	U10		

6 Bootstrap configuration

During hardware reset, the balls in the table below are configured as inputs. On the negating edge of RESETn, the value on these balls is latched and stored. This value is readable by the on-chip microcontroller to provide system configuration information. This process is called “bootstrapping”. External 1K pull-down/pull-up resistors need to be connected to the bootstrap balls to establish the bootstrap logic level.

Table 24. Bootstrap signals

Signal name	I/O	Ball name	Internal resistor	Description
OSC_SEL	I	SPI_DI Bootstrap ‘7’	50K PULLUP	0 = Select External OSC Operation ; Add External Pulldown to select. 1 = Select Internal OSC operation ; Default if NC
ICD_ENABLE_x186	I	I2S_CLK_OUT Bootstrap ‘6’	50K PULLDOWN	Enables the x186 In Circuit Debugger 0 = I2C to JTAG Bridge is disabled. ; Default if NC 1 = ICD_SDA on VGA_SDA, ICD_SCL on VGA_SCL. ; Add External Pullup to select
FORCE_DEBUG	I	I2S_DOUT2 Bootstrap ‘5’	50K PULLDOWN	IROM bootstrap 0 = Normal operating mode. ; Default if NC 1 = FORCE DEBUG mode. Code does not exit IROM and does not check DDC2Bi channel. (IROM Software Decoded); Add External Pullup to select
SPARE1	I	SPDIF_OUT Bootstrap’4’	50K PULLDOWN	SPARE1; NC reads LOW ; Add External Pullup to select 1
DUAL_FLASH_EN	I	SPI_DO Bootstrap ‘3’	50K PULLUP	0 – No Dual Flash ; Pull down to Disable. ; Add External Pulldown to select 1 – DUAL_FLASH Enabled; Default if NC
OCM_BOOT_XROM RESERVED	I	SPI_CLK Bootstrap ‘2’	50K PULLDOWN	Selects the initial state of internal OCM ROM 0 = Normal operation; Default if NC 0 = Internal ROM on, and mapped to top 32K of OCM address range. OCM boot will be from internal ROM code. 1 = Internal ROM off. This is a debug mode with the external ROM mapped to include the address range normally reserved for the internal ROM. OCM boot will be from external ROM code. ; Add External Pullup to select

Table 24. Bootstrap signals

Signal name	I/O	Ball name	Internal resistor	Description
WDT_MODE	I	I2S_WS_OUT Bootstrap '1'	50K PULLDOWN	Selects the recovery level of a watch dog timer error internal x186 micro-controller only. ; Default if NC 1 = WDT resets all digital logic in the IC. ; Add External Pullup to select
ATE_VECTOR_MODE	I	I2S_DOUT1 Bootstrap '0'	50K PULLDOWN	Enable ATE vector load mode (external nibble bus mode) 0 = Normal operating mode. ; Default if NC 1 = Nibble mode enabled for loading ATE vectors. ; Add External Pullup to select

7 Packages

STDP9320 package type: HSBGA 521 balls. Body: 23 x 23 mm

Figure 70. STPD9320 package top view

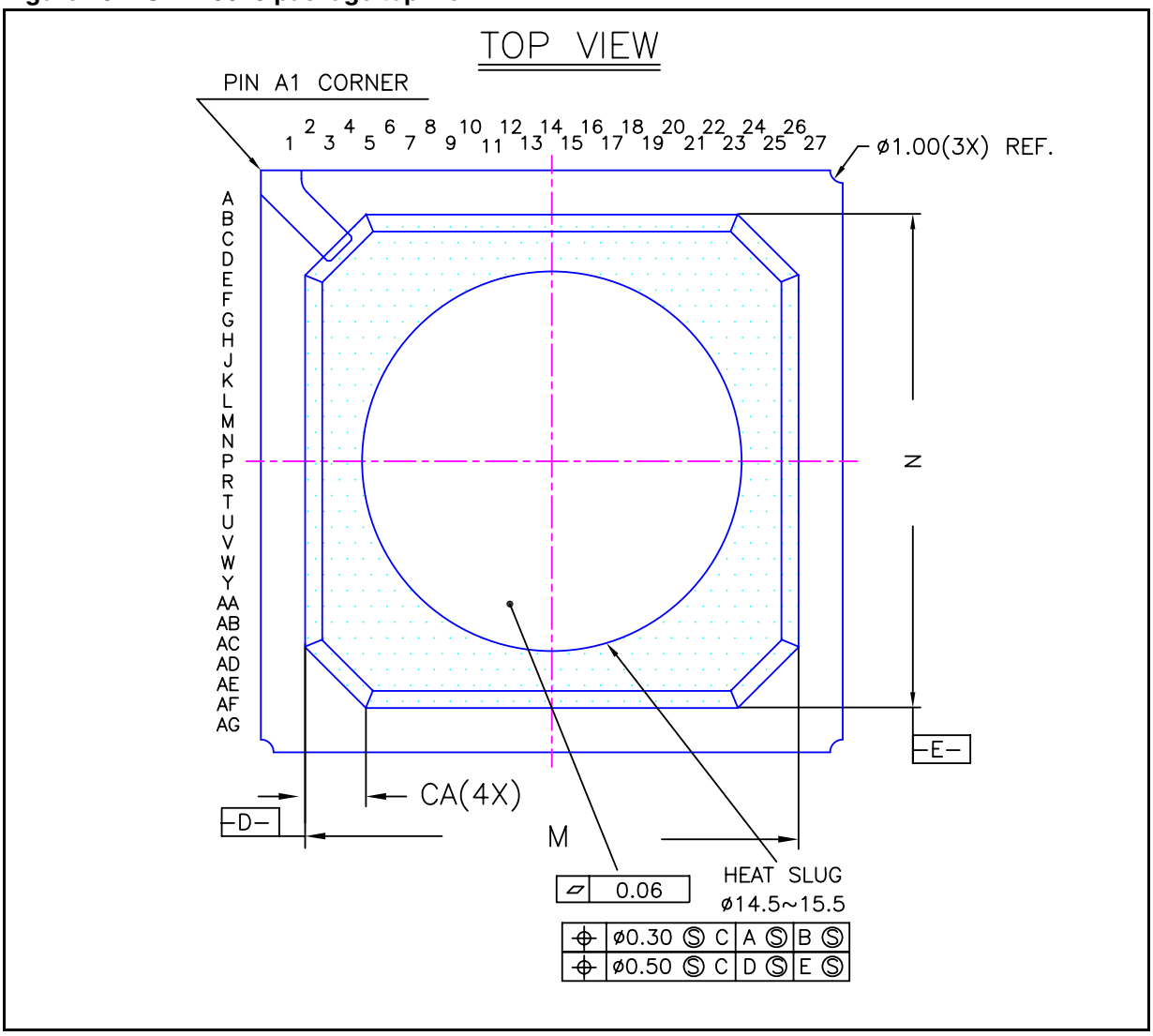


Figure 71. STDP9320 package bottom view

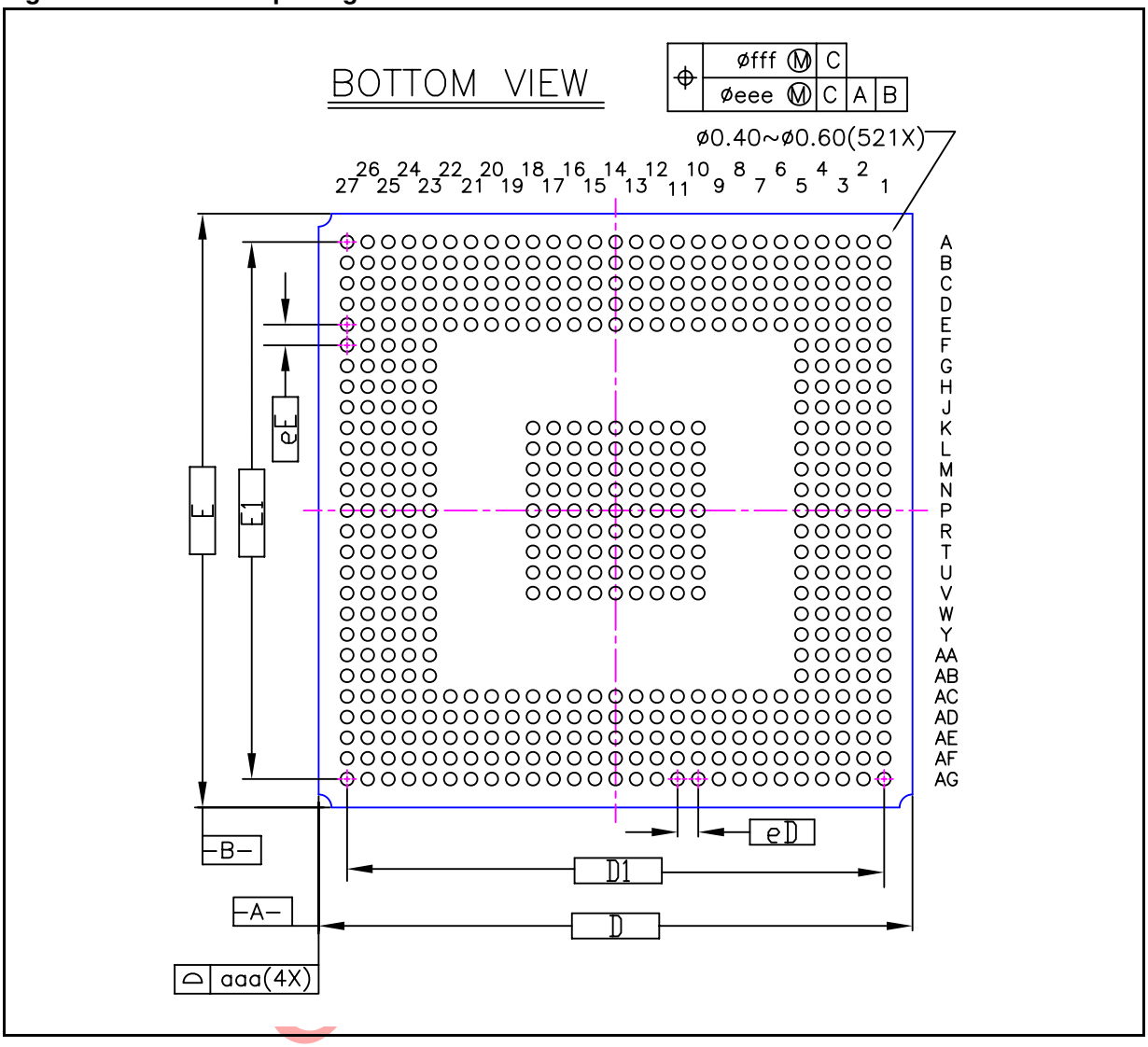


Figure 72. STDP9320 package side view

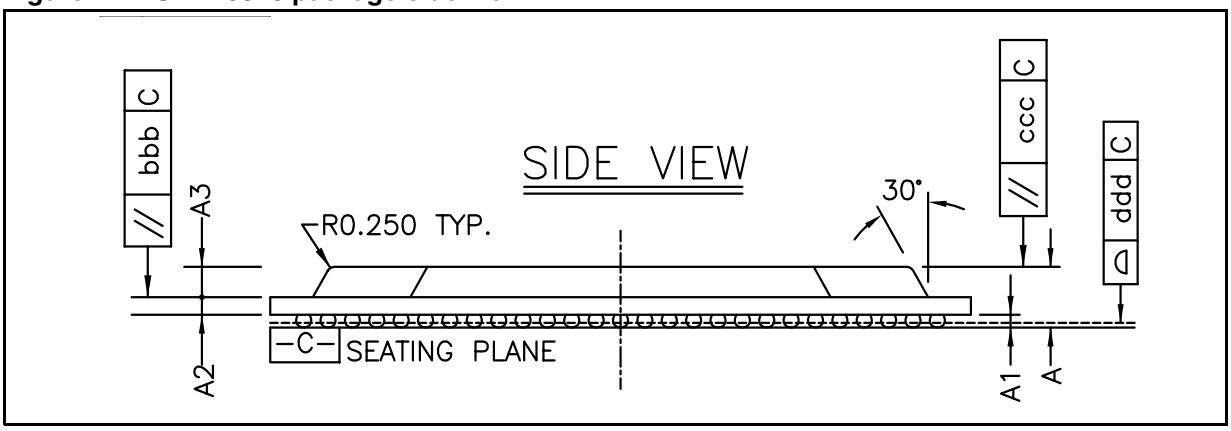


Table 25. STDP9320 JEDEC standard package dimensions

Dimension	Databook (mm)			Drawing (mm)			Notes
	Min	Typ	Max	Min	Typ	Max	
A			2.03			2.03	(1)
A1	0.36	0.41	0.46	0.36	0.41	0.46	
A2		0.56			0.56		
A3		0.97			0.97		
b	0.44	0.54	0.64	0.44	0.54	0.64	(2)
D. E	22.90	23.00	23.10	22.90	23.00	23.10	
D1. E1		20.80			20.80		
M, N		20			20		
Heat Slug	14.5	15.0	15.5	14.5	15.0	15.5	
CA		2.4			2.4		
aaa			0.20			0.20	
bbb			0.25			0.25	
ccc			0.35			0.35	
ddd			0.15			0.15	
eee			0.25			0.25	(3)
fff			0.10			0.10	(4)

1. HSFBGA stands for Heat Slug Ball Grid Array.

   The total profile height (Dim A) is measured from the seating plane to the top of the component. The maximum total package height is calculated by the following methodology: A Max = A1 Typ + A2 Typ + A3 + v ($A1^2 + A2^2 + A3^2$ tolerance values)

2. The typical ball diameter before mounting is 0.5 mm.

3. The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.

4. The tolerance of position that controls the location of the balls within the matrix with respect to each other.For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones.

   The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug.

   A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

STDP9310, STDP9210 package type: FPBGA 521 balls. Body: 23 x 23 mm

Figure 73. STDP9310, STDP9210 package top view

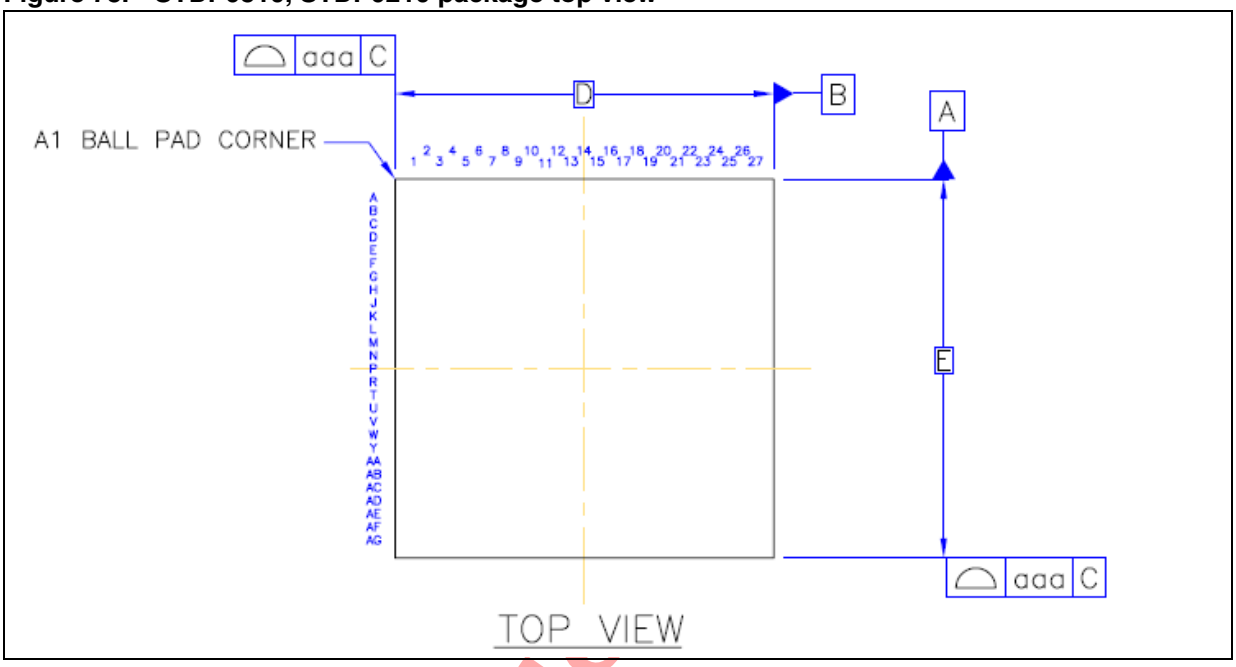


Figure 74. STDP9310, STDP9210 package bottom view

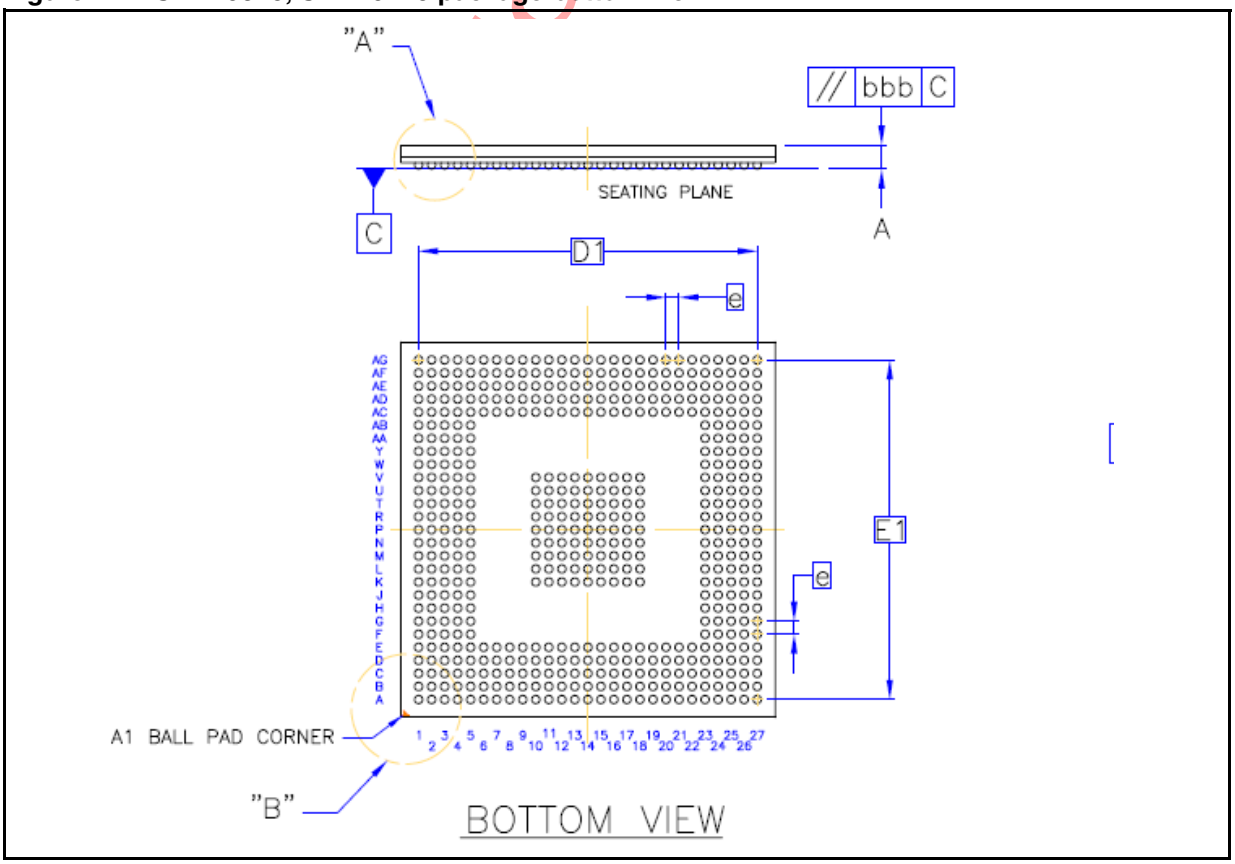


Figure 75. STDP9310, STDP9210 package detailed view

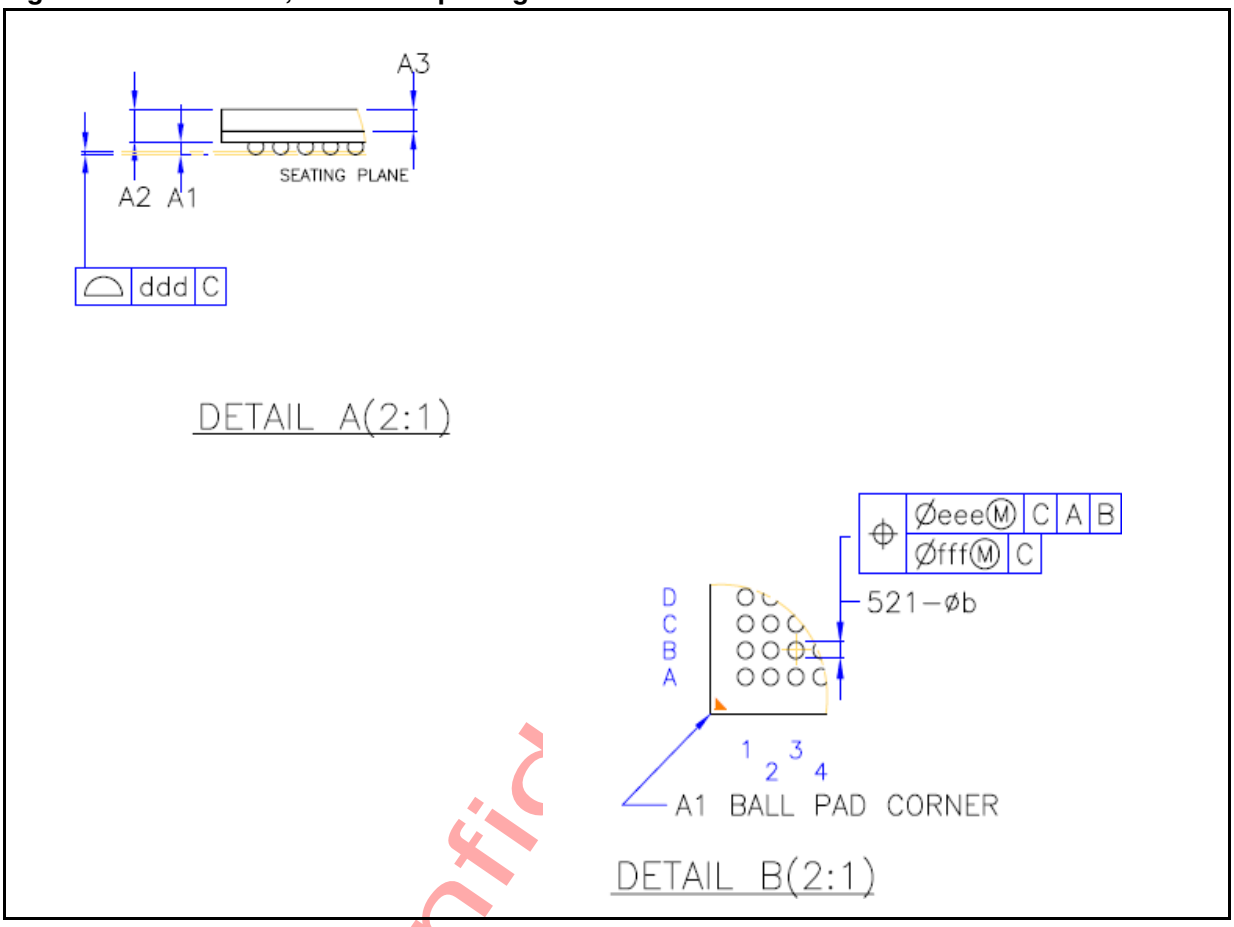


Table 26. STDP9310, STDP9210 JEDEC standard package dimensions

Dimension	Databook (mm)			Drawing (mm)			Notes
	Min	Typ	Max	Min	Typ	Max	
A			1.8			1.78	(1)
A1	0.35	0.40	0.45	0.35	0.40	0.45	(2)
A2		0.53		0.49	0.53	0.57	
A4		0.80		0.77	0.785	0.80	
D	22.85	23.00	23.15	22.90	23.00	23.10	
D1		20.80			20.80		
E	22.85	23.00	23.15	22.90	23.00	23.10	
E1		20.80			20.80		
e		0.80			0.80		
b	0.45	0.50	0.55	0.45	0.50	0.55	
Z		1.10			1.10		
aaa			0.15			0.10	
bbb			0.10			0.10	
ddd			0.20			0.20	
eee			0.15			0.15	(3)
fff			0.08			0.08	(4)

1. FPBGA stands for Fine Pitch Ball Grid Array.

   Fine pitch: e < 1.00mm pitch. The total profile height (Dim A) is measured from the seating plane to the top of the component. The maximum total package height is calculated by the following methodology: A Max = A1 Typ + A2 Typ +A4 Typ + v(A1² + A2² A4² tolerance values).

2. The typical ball diameter before mounting is 0.5 mm.

3. The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.

4. The tolerance of position that controls the location of the balls within the matrix with respect to each other.For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones.

   The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug. A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

STDP7320, STDP7310 package type: LFBGA 361 balls. Body: 16 x 16 mm

Figure 76. STDP7320, STDP7310 package bottom view

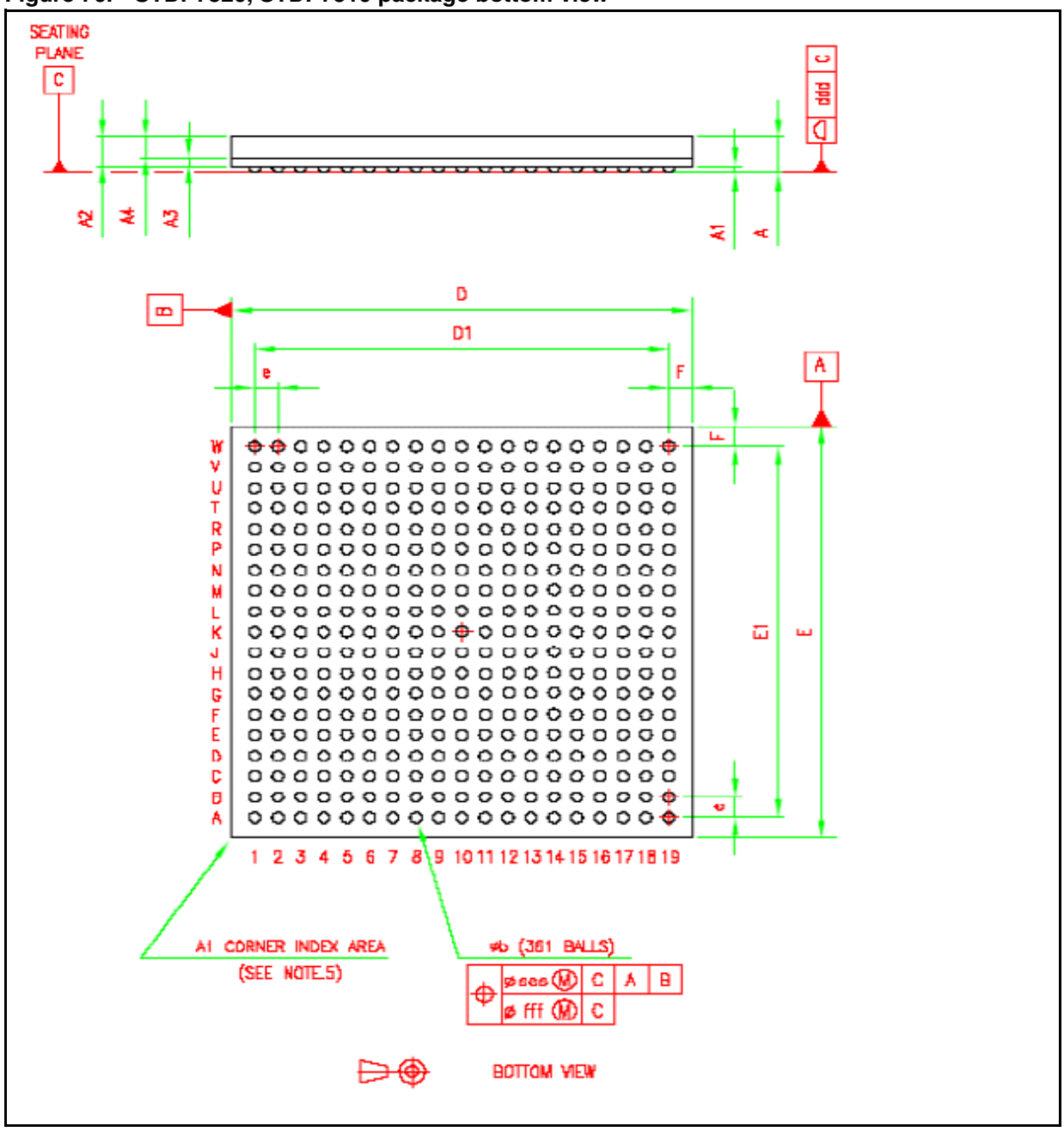


Table 27. STDP7320, STDP7310 JEDEC standard package dimensions

Dimension	Databook (mm)			Drawing (mm)			Notes
	Min	Typ	Max	Min	Typ	Max	
A			1.70			1.43	(1)
A1	0.21			0.25	0.30	0.35	
A2		1.065		1.03	1.065	1.14	
A3			0.40	0.24	0.28	0.32	
A4			0.80	0.77	0.785	0.80	
b	0.35	0.40	0.48	0.35	0.40	0.45	(2)
D	15.85	16.00	16.15	15.90	16.00	16.10	
D1		14.40			14.40		
E	15.85	16.00	16.15	15.90	16.00	16.10	
E1		14.40			14.40		
e		0.80			0.80		
F		0.80			0.80		
ddd			0.10			0.10	
eee			0.15			0.15	(3)
fff			0.08			0.08	(4)

1. LFBGA stands for Low Profile Fine Pitch Ball Grid Array.

   Low profile: The total profile height (Dim A) is measured from the seating plane to the top of the component. The maximum total package height is calculated by the following methodology: A2 Typ+A1 Typ +v ($A1^2+A3^2+A4^2$ tolerance values)

   Low profile: 1.20mm < A ≤1.70mm / Fine pitch: e < 1.00mm pitch.

2. The typical ball diameter before mounting is 0.40mm.

3. The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.

4. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones.

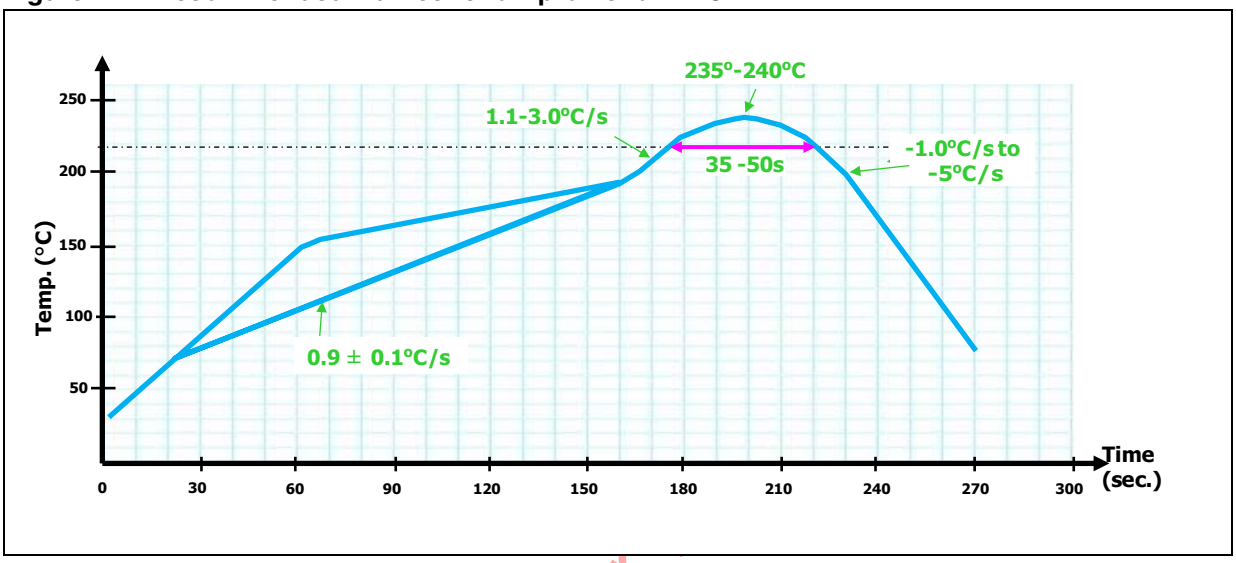
   The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug.

   A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 Solder reflow profile

Figure 77. Recommended Pb-free reflow profile for PBGA



Profile	Ramp-to-Spike (linear ramping)	
Temperature gradient in preheat	T = 125 to 180 °C	0.9 +/- 0.1 °C/s
Temperature gradient	T = 200 to 225 °C	1.1 - 3.0 °C/s
Peak temperature in reflow	235 °C - 240 °C	
Time above 217 °C	35-50 sec	
Temperature gradient in cooling	T = 217 to 150 °C	-1 to -5 °C/s
Time from 50 to 220 °C	150 to 220 sec	

Note: 1 Ramp-to-Spike profile is recommended for Pb-free assembly with better wetting and less thermal exposure than traditional Ramp-Soak-Spike profile..

2 Avoid temperature plateau around melting temperature for better accuracy.

3 Thermocouples are attached through bottom side of the board, underneath the center, and the corner of component BGA.

4 Perform optimization for actual board/panel and refer to solder paste supplier's recommendation.

7.2 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

8 Electrical specifications

8.1 Preliminary DC characteristics: absolute maximum ratings

Applied conditions greater than those listed under “Absolute maximum ratings” may cause permanent damage to the device. The device should never exceed absolute maximum conditions since it may affect device reliability.

Table 28. Absolute maximum ratings

Parameter	Symbol	Min	Typ	Max	Units
3.3 V supply voltages(1) (2)		-0.3	3.3	3.47	V
2.5 V supply voltages(1) (2)		-0.3	2.5	2.63	V
1.8 V supply voltages(1) (2)		-0.3	1.8	1.89	V
1.5 V supply voltages(1) (2)		-0.3	1.5	1.58	V
1.2 V supply voltages(1) (2)		-0.3	1.2	1.26	V
Input voltage (5 V tolerant inputs)(1) (2)	$V_{IN5Vtol}$	-0.3		5.5	V
Input voltage (3.3 V tolerant inputs)(1) (2)	$V_{IN3V3tol}$	-0.3		3.47	V
Input voltage (2.5 V tolerant inputs)(1) (2)	$V_{IN2V5tol}$	-0.3		2.63	V
Input voltage (1.8 V tolerant inputs)(1) (2)	$V_{IN1V8tol}$	-0.3		1.89	V
Input voltage (1.5 V tolerant inputs)(1) (2)	$V_{IN1V5tol}$	-0.3		1.58	V
Input voltage (1.2 V tolerant inputs(1) (2))	$V_{IN1V2tol}$	-0.3		1.26	V
ESD - Human Body Model (HBM)	V_{ESD}	+/-2			kV
ESD - Charged Device Model (CDM)	V_{ESD}	+/-500			V
Latch-up	I_{LA}	+/-200			mA
Ambient operating temperature	T_A	0		70	°C
Storage temperature	T_{STG}	-40		125	°C
Operating junction temperature	T_J	0	70	125	°C
Thermal resistance (Junction to Ambient) 521 HSBGA Package	θ_{JA}		13.6		°C/W
Thermal resistance (Junction to Ambient) 521 LFBGA Package	θ_{JA}		16.1		°C/W
Thermal resistance (Junction to Ambient) 361 LFBGA Package	θ_{JA}		19.0		°C/W
PSI (J-T) (Junction-to-Top-Center) 521 HSBGA Package	Ψ_{JT}		3.39		°C/W
PSI (J-T) (Junction-to-Top-Center) 521 LFBGA Package	Ψ_{JT}		0.15		°C/W
PSI (J-T) (Junction-to-Top-Center) 361 LFBGA Package	Ψ_{JT}		0.20		°C/W

Table 28. Absolute maximum ratings

Soldering temperature (30 sec.)	T_{SOL}			210	°C
LF Soldering Temperature (30 sec.)	T_{SOL}			250	°C

1. All voltages are measured with respect to GND
2. Absolute maximum voltage ranges are for transient voltage excursions.

Note: 1 Good thermal design practices should be followed to allow efficient heat removal from the system. Follow the steps in the ATHENA System Layout Guidelines (Cxxxx-SLG-01) to keep the system thermally efficient.

2 Customers are required to check TC (case top temperature) at the extremes of their system design operating conditions to ensure they have adequate heat removal and that TJ (junction temperature) is not exceeding 125 °C. TJ can be calculated with the PSI (J-T) parameters provided above.

Table 29. DC characteristics

Parameter	Symbol	Min	Typ	Max	Units
Power					
3.3 V supply voltages (AVDD and VDD)	$V_{VDD\_3.3}$	3.14	3.3	3.46	V
2.5 V supply voltages		2.38	2.5	2.63	V
1.8 V supply voltages		1.71	1.8	1.89	V
1.8 V supply voltages (VDD)	$V_{VDD\_1.8}$	1.71	1.8	1.89	V
1.5 V supply voltages		1.43	1.5	1.58	V
1.2 V supply voltages (AVDD and VDD)	$V_{VDD\_1.2}$	1.14	1.2	1.26	V
1.2 V supply voltages (CVDD)	$V_{VDD\_1.2}$	1.17	1.2	1.26	V

Table 29. DC characteristics

Parameter	Symbol	Min	Typ	Max	Units
Supply current					
1.2 V Audio analog supply	VDD1V2_AUDIO			0.5	mA
1.2 V core digital supply	VDD1V2_DIG			1320	
1.2 V DPTx analog supply	VDD1V2_DPTX			142	
1.2 V LPM ADC analog supply	VDD1V2_LPM_ADC		0.8	14(1)	
1.2 V LPM COMBO analog supply	VDD1V2_LPM_COMBO			277	
1.2 V LPM digital Power	VDD1V2_LPM_DIG			6.2	
2.5 V DPTx analog supply	VDD2V5_DPTX			23	
2.5 V LPM ADC analog supply	VDD2V5_LPM_ADC		8.1	103(1)	
2.5 V LPM SafeMem analog supply	VDD2V5_LPM_SAFEMEM			0.7	
2.5 V LVDS analog supply	VDD2V5_LVDS			119	
2.5 V PLL analog supply	VDD2V5_PLL			53	
3.3 V digital supply	VDD3V3_DIG			13.8	
3.3 V AUD HP analog supply	VDD3V3_HP_AUD			3.8	
3.3 V LPM COMBO analog supply	VDD3V3_LPM_COMBO			207	
3.3 V LPM digital Power	VDD3V3_LPM_DIG			3	
3.3 V AUD analog supply	VDDA3V3_AUD			17	
1.5 V DDR analog supply (DDR3)	VDDQ_DDR			243	
1.8 V DDR analog supply (DDR2)	VDDQ_DDR			370(2)	

1. VDD1V2_LPM_ADC and VDD2V5_LPM_ADC measured by enabled ADC with WUXGA 60 Hz input.
2. VDDQ_DDR for DDR2 measured separately with same input resolution and display size.

The values in the Max column represent absolute maximum current consumption under high voltage (+5%) and nominal temperature. These values are measured in an environment that includes some discreet components.

Measure condition include:

- Main input: Dual-DVI WQXGA 60 by external pattern generator; pattern: CHECKER 11
- PIP input: DP WQXGA 60 by external graphic card; pattern: CHECKER 11
- Reference Clock: 374 MHz (RCLK)
- Main display size: 2560 x 1600 60 Hz
- PIP display Size: 960 x 540
- OSD: No
- Display: WQXGA 60 Hz Qual-LVDS panel
- DPTx: MST HBR

Note: 1 Power measurement values are to be used for regulator sizing only, and not directly for package thermal calculations.

2 IC performance is only guaranteed when operating within the DC characteristics parameters.

Table 30. Standby low power operating mode

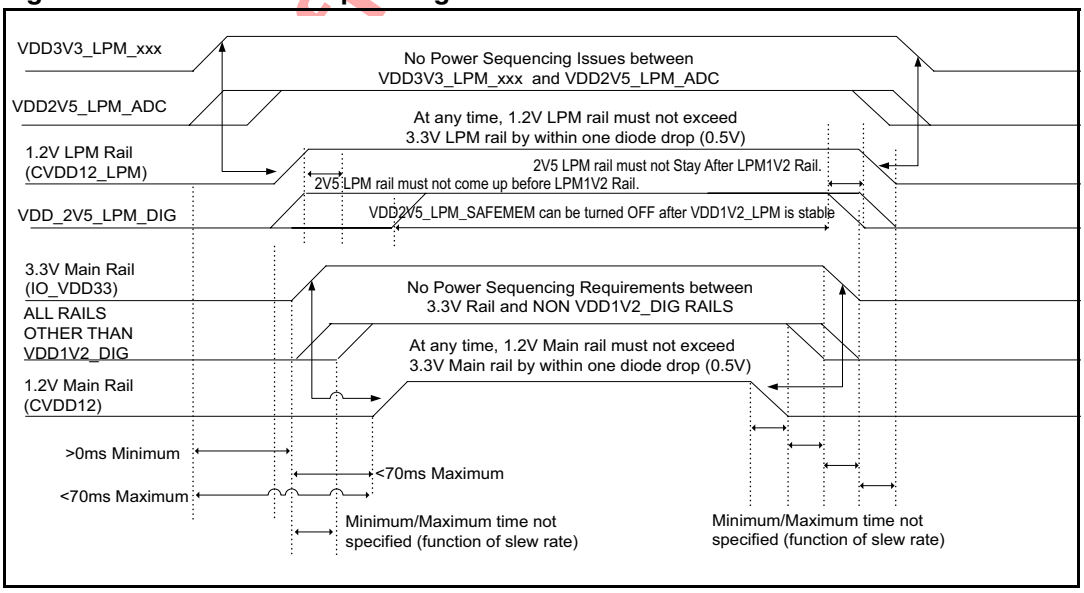
Power	Symbol	Min	Typ	Max	Units
Supply current(1)					
1.2 V LPM analog supply	VDD1V2_LPM_ADC+VDD1V2_LPM_COMBO		4.5	10	mA
1.2 V LPM digial supply	VDD1V2_LPM_DIG		0.8	10	
2.5 V LPM supply	VDD2V5_LPM_ADC+VDD2V5_LPM_SAFEMEM		1.8	4	
3.3 V LPM COMBO analog supply	VDD3V3_LPM_COMBO		0.5	10	
3.3 V LPM digital supply	VDD3V3_LPM_DIG		1.8	4	

1. Low power currents are measured at nominal voltages.

8.1.1 Power rails sequencing

The following diagram illustrates the procedure used to implement power rails sequencing for the Athena products.

Figure 78. Power rails sequencing



The diagram above details the following power rails sequencing principles:

- The 3.3 V LPM rail must be energized at the same time or earlier than the 3.3 V main rail. There is no maximum limit to this sequence.
- The 1.2 V LPM rail must be energized within a maximum of 70 ms of the 3.3 V LPM rail coming up. This ensures that the LPM digital core is powered when the LPM reset cell is still asserting reset. The only minimum limit on the 1.2 V LPM rail is that it must not

be powered up before the 3.3 V LPM rail (i.e. the 1.2 V LPM rail must not exceed the 3.3 V LPM rail by within one diode drop).

- VDD2V5_LPM_SAFEMEM must not be powered before VDD1V2_LPM_DIG. This is a SAFEMEM power sequencing requirement.
- The 1.2 V main rail must be energized within a maximum of 70 ms of the 3.3 V main rail coming up. This ensures the mission digital core is powered when the mission reset cell is still asserting reset. The only minimum limit on the 1.2 V main rail is that it must not be powered up before the 3.3V main rail (i.e. the 1.2 V main rail must not exceed the 3.3V main rail by within one diode drop).
- There is no power sequencing requirement between VDD3V3_DIG and mission rails other than VDD1V2_DIG.

8.1.2 Power regulator location

Since the 1.2 V rail can draw in excess of 1.0 A under extreme conditions, it is advisable to use efficient and low inductance power traces and planes to make sure that there is negligible IR drop along the trace/plane to the chip. This can be accomplished by using thick traces and multiple vias from the regulator to the 1.2 V plane under the chip. An adjustable regulator can also be used to slightly boost the rail to +2% to 3% accounting for any IR drop in the power distribution path from the regulator to the chip. In addition, it is recommended that the 1.2 V core regulator has a current rating of 2 A or greater.

8.2 Preliminary AC characteristics

Table 31. Maximum speed of operation

Clock domain	Max speed of operation
Reference Input Clock (TCLK)	27 MHz
Reference Internal Clock (RCLK)	432 MHz
Digital Video Input Clocks (IPCLK0, IPCLK1)	150 MHz
Input capture Clock (IMPCLK/IPPCLK)	300 MHz (STDP93x0/STDP9210) 205 MHz (STDP73x0)
Analog Video or Graphics Clock (SCLK)	205 MHz
On-Chip Microcontroller Clock (OCLK)	200 MHz
DDR Memory Clock (FCLK) for DDR2/3 x32	266 MHz
DDR Memory Clock (FCLK) for DDR2/3 x16	266 MHz
Display Clock (DCLK)	300 MHz (STDP93x0) 400 MHz (STDP9210) 165 MHz (STDP73x0)
I2S Input Clock (I2S_CLK_IN)	25 MHz
I2S Output Clock (I2Sx_CLK_OUT)	25 MHz
2-Wire Serial Slave (SLAVE_SCL)	2 MHz
2-Wire DDC2bi Slave (VGAx_SCL)	2 MHz
2-Wire Serial Master (MSTRx_SCL)	2 MHz

Figure 79. Digital input ports—DIP timing

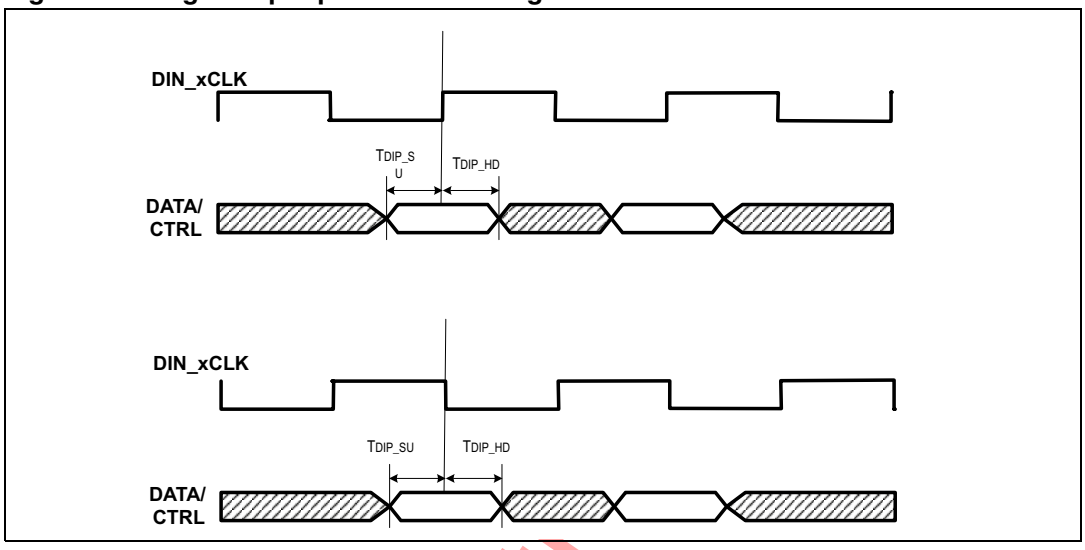


Table 32. Digital input ports—DIP timing

Power	Symbol	Min	Typ	Max	Units
Data/Control Hold from CLK (DIN_0CLK, DIN_1CLK) edge (DIN_HS, DIN_HREF_DE, DIN_VS, DIN_ODD, DIN_DATA)	T_{DIP_SU}	1.25			ns
Data/Control Hold from CLK (DIN_0CLK, DIN_1CLK) edge (DIN_HS, DIN_HREF_DE, DIN_VS, DIN_ODD, DIN_DATA)	T_{DIP_HD}	1.00			ns

Note: DIN_xCLK edge is programmable to be a rising or falling edge.

Figure 80. I2S input port timing

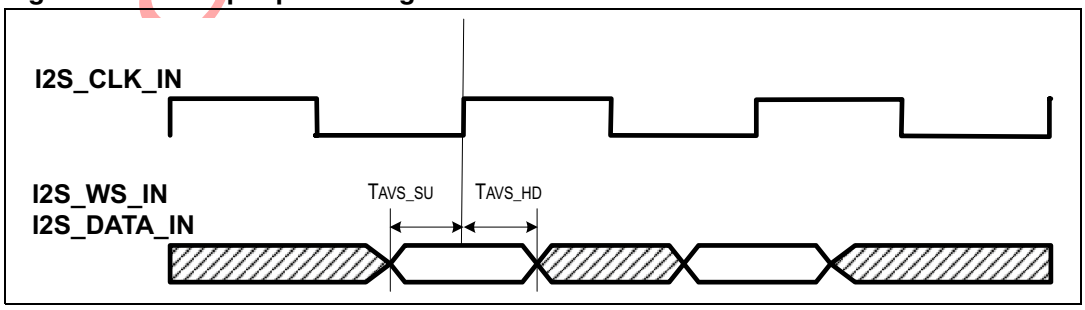


Table 33. I2S input port timing

Power	Symbol	Min	Typ	Max	Units
I2S_WS_IN and I2S_DATA_IN Setup to I2S_CLK_IN	T_{AVS_SU}	3.00			ns
I2S_WS_IN and I2S_DATA_IN Hold from I2S_CLK_IN)	T_{AVS_HD}	2.00			ns

Note: I2S_CLK_IN edge is programmable to be a rising or falling edge.

Figure 81. I2S output port timing

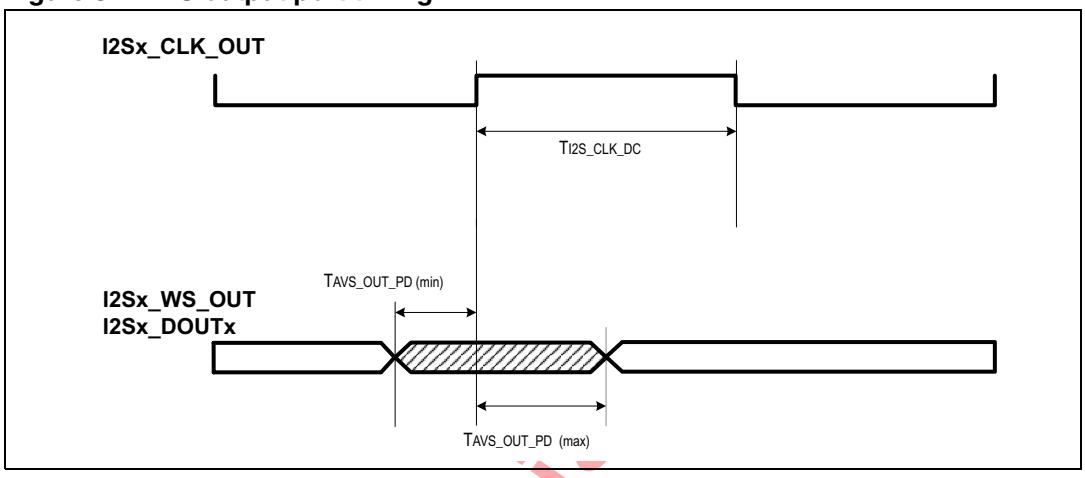


Table 34. I2S output port timing

Power	Symbol	Min	Typ	Max	Units
Propagation Delay from I2Sx_CLK_OUT to I2Sx_DOUTx and I2Sx_WS_OUT	$T_{AVS\_OUT\_PD}$	-7.00		5	ns
I2Sx_CLK_OUT Duty Cycle	$T_{I2S\_CLK\_DC}$	45		55	%

Note: I2Sx_CLK_OUT edge is programmable to be rising or falling edge.
DCLK edge is programmable to be a rising or a falling edge.

Figure 82. LVDS transmitter switching characteristics

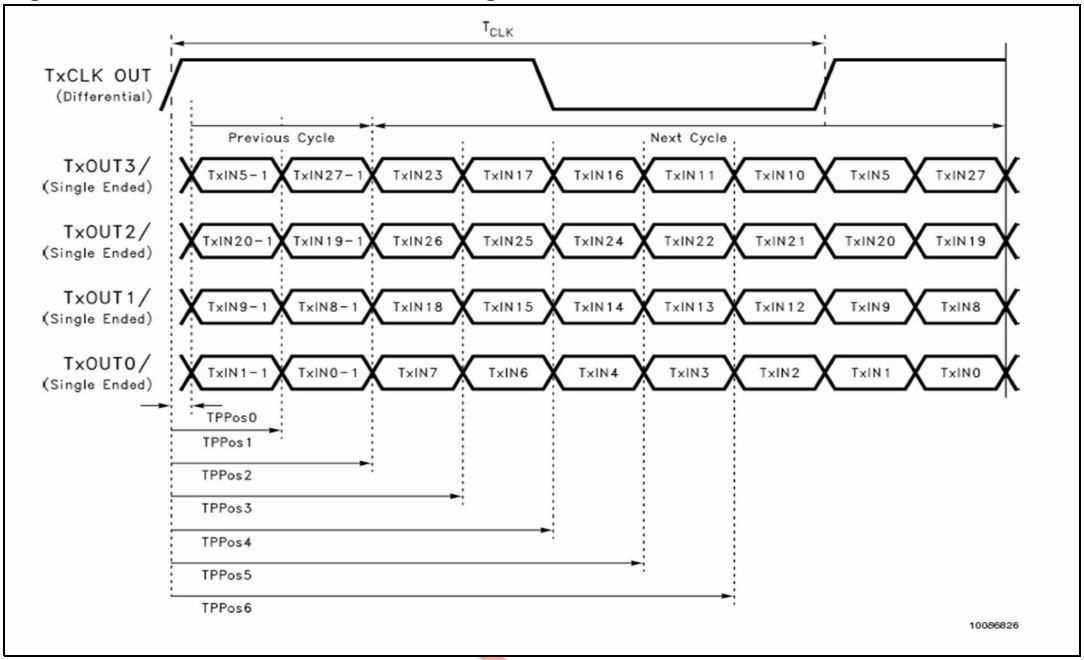


Table 35. LVDS AC charateristics (even and odd channels)

Symbol	Parameters	E_CH0 ~ E_CH3 O-CH0 ~ O_CH3	Typical	Units
TPPos0	T/X output pulse position for bit 0	F= 85 MHz	0	ns
TPPos1	T/X output pulse position for bit 1		1.681	
TPPos2	T/X output pulse position for bit 2		3.361	
TPPos3	T/X output pulse position for bit 3		5.042	
TPPos4	T/X output pulse position for bit 4		6.723	
TPPos5	T/X output pulse position for bit 5		8.403	
TPPos6	T/X output pulse position for bit 6		10.084	
TPPos7	T/X output pulse position for bit 7		11.765	

Note: There is a +/- ps variation for the measurements for even and odd channels.

Table 36. LVDS DC characteristics

Parameter	Min	Typical	Max	Units
Swing		1.74		V
Voltage Differential Output (VOD)	300	500	700	mV
Voltage Commmon Mode (VCM)		1.25		V
Tristate		10		uA

Figure 83. SPI output port timing

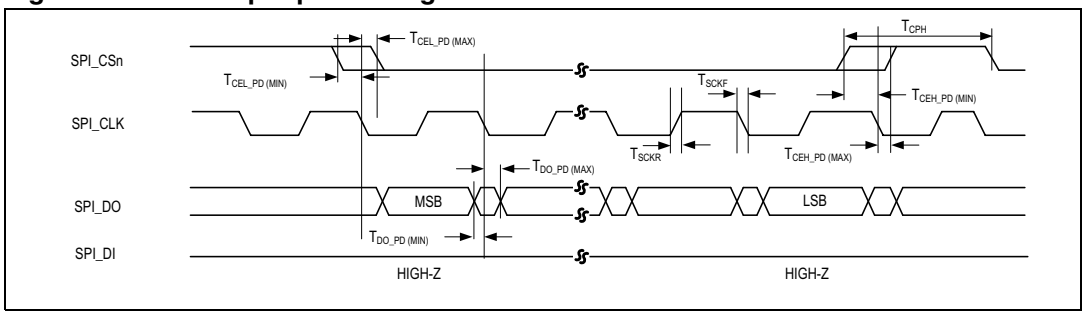


Figure 84. SPI input port timing

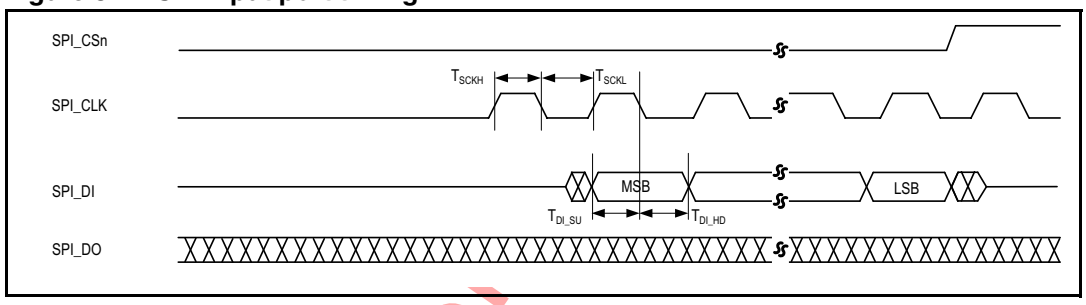


Table 37. SPI port timing

Parameter	Symbol	Min	Typ	Max	Units
SPI_CLK Frequency	FCLK		33.33	100	MHz
SPI_CLK High Time	T_{SCKH}	6			ns
SPI_CLK Low Time	T_{SCKL}	6			
SPI_CLK Rise Time	T_{SCKR}			5	
SPI_CLK Fall Time	T_{SCKF}			4	
SPI_CSn Prop Delay to Active	T_{CEL_PD}	-3		0	
SPI_CSn Prop Delay to Inactive	T_{CEL_PD}	-1		0	
SPI_DO Prop Delay	T_{DO_PD}	-3		0	
SPI_DI Setup Time	T_{DI_SU}	8.5			
SPI_DI Hold Time	T_{DI_HD}	0			
CE# High Time	T_{CPH}		(N+1)OCLKs(1)		

1. N = 5-bit programmable value

Note: Negative values indicate a signal transition leading the clock. SPI_CLK frequency options are OCM_CLK/2, OCM_CLK/3, OCM_CLK/4, OCM_CLK/5, and OCM_CLK/6.

Figure 85. Frame store write timing

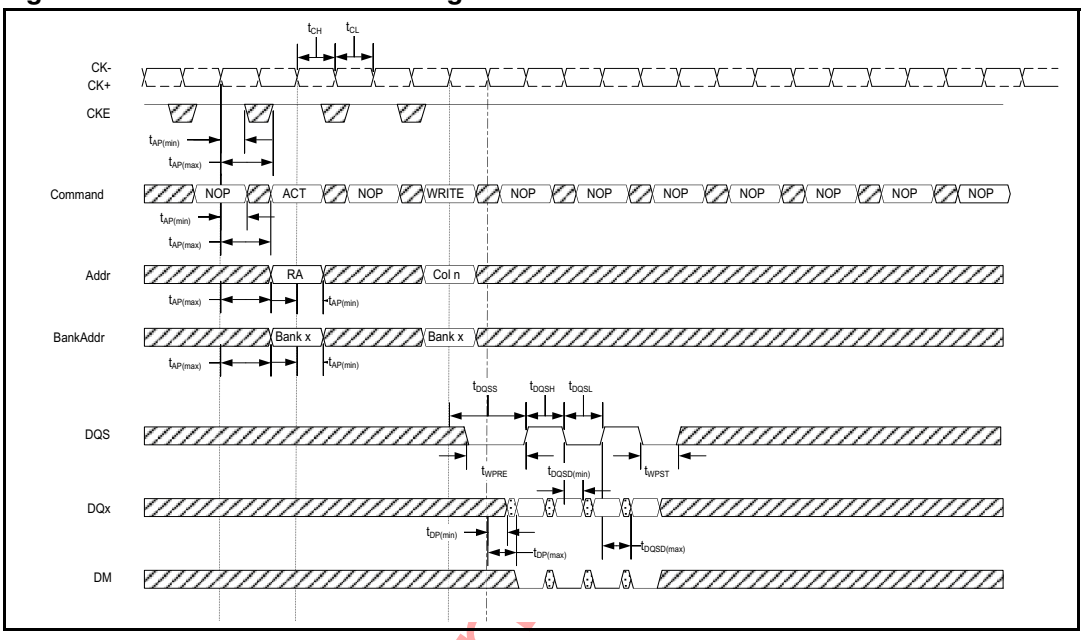


Table 38. DDR interface write timing

Parameter	Symbol	Min	Typical	Max	Units
Clock period	t_{CK}	1.875		4.0	ns
Clock high width	t_{CH}	48%		52%	t_{CK}
Clock low width	t_{CL}	48%		52%	t_{CK}
Address/command propagation	t_{AP}	1.25		1.5(1)	ns
Write command to first DQS latching transition	t_{DQSS}	-0.25		0.25	t_{CK}
DQS high pulse width	t_{DQSH}	45%		55%	t_{CK}
DQS low pulse width	t_{DQSL}	45%		55%	t_{CK}
DQS write preamble	t_{WPRE}	0.3			t_{CK}
DQS write postamble	t_{WPST}	0.3		0.65	t_{CK}
DQS-data/DM propagation	t_{DQSD}	0.25		0.35(2)	ns

1. At tCK = 2.5ns. Address/Command propagates from falling clock edge internally so increasing the clock period will increase the max propagation delay of this parameter accordingly.
2. At tCK = 2.5ns. Max data propagation will increase when clock period increases.

Note: For all DDR pins the CLOAD = 8 pF.

Figure 86. Frame store read timing

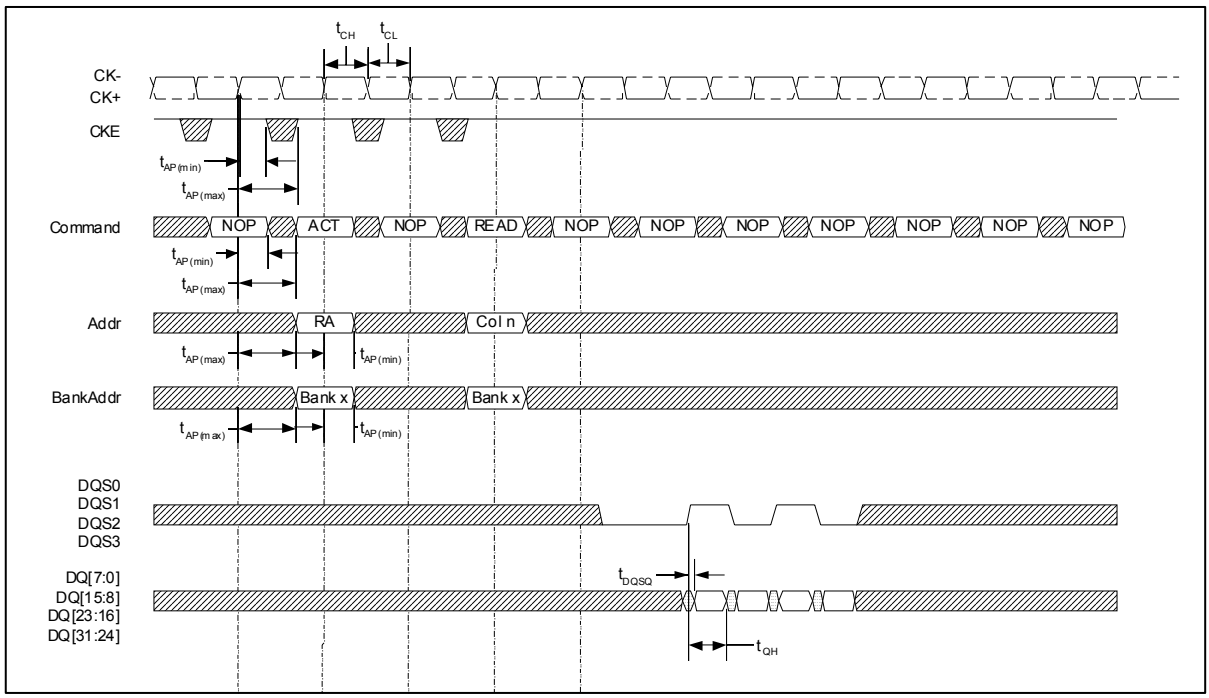


Table 39. DDR interface read timing

Parameter	Symbol	Min	Typ	Max	Units
Clock high width	t_{CH}	48%		52%	t_{CK}
Clock low width	t_{CL}	48%		52%	t_{CK}
Address/command propagation	t_{AP}	1.25		1.5(1)	ns
DQS-to-DQ Max Skew (Note: Each data byte has a unique DQS)	t_{DQSQ}	-0.3		0.3	ns
DQ-to-DQS Min Hold (Note: Each data byte has a unique DQS)	t_{QH}	0.38			t_{CK}

1. At tCK = 2.5ns. Address/Command propagates from falling clock edge internally so increasing the clock period will increase the max propagation delay of this parameter accordingly.

Note: 1 For all DDR pins the CLOAD=8 pF.

2 Board skew on DQ lines must be less than 50 ps.

Table 40. DisplayPort input timing

Parameter	Symbol	Min	Typ	Max	Units	Comments
HBR2 Unit Interval (5.4Gbps)	UI_HBR2		185		ps	DisplayPort link RX does not require local crystal for link clock generation
Turbo Unit Interval (3.2Gbps)	UI_TURBO		312		ps	
HBR Unit Interval (2.7Gbps)	UI_HBR		370		ps	
RBR Unit Interval (1.62Gbps)	UI_RBR		617		ps	
Link clock down spreading	Down Spread Amplitude	0.5			%	Modulation frequency range 0f 30kHz to 33kHz
Differential Peak-to-peak Input Voltage at package pins	$V_{RX-DIFFp-pa}$	120			mV	
Rx Horizontal Eye Specification for High Bit Rate						
Minimum Receiver Eye Width at Rx-side connector pins	T_{RX-EYE_CONN}	0.51			UI	
Minimum Receiver Eye Width at Rx package pins	T_{RX-EYE_CHIP}	0.47				
Maximum time between the jitter median and maximum deviation from the median at Rx package pins	$T_{RX-EYE-MEDIAN-to-MAX-ITTER\_CHIP}$			0.265		$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specifies the total allowable DJ
Rx Horizontal Eye Specification for Reduced Bit Rate						
Minimum Receiver Eye Width at Rx-side connector pins	T_{RX-EYE_CONN}	0.46			UI	
Minimum Receiver Eye Width at Rx package pins	T_{RX-EYE_CHIP}	0.42			UI	$(_{1-TRX-EYE\_CONN})$ specifies the allowable TJ
Maximum time between the jitter median and maximum deviation from the median at Rx package pins	$T_{RX-EYE-MEDIAN-to-MAX-ITTER\_CHIP}$			0.29	UI	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specifies the total allowable DJ
RX DC Common Mode Voltage	$V_{RX-DC-CM}$	0		VDD	V	Common mode voltage is equal to Vbias_Rx voltage. VDD is the receiver input power supply voltage and 3.6 V maximum.
RX Short Circuit Current Limit	$I_{RX-SHORT}$			90	mA	Total drive current of the transmitter when it is shorted to its ground.
Differential return loss at 0.675GHz	$R_{LRX-DIFF}$			12	dB	Straight loss line between 0.675 GHz and 1.35 GHz
Differential loss at 1.35GHz				9	dB	
Powered Down DC Input resistance	$R_{RX-HGIH-IMP-DC}$	200K			Ω	

Table 40. DisplayPort input timing

Parameter	Symbol	Min	Typ	Max	Units	Comments
Lane-to-Lane Skew at RX package pins	$L_{RX\text{-}SKEW\text{-}INTER\_CHIP}$			5200	ps	Maximum skew limit between different RX lanes of a DisplayPort link.
Intra-pair Skew Specification for High Bit Rate						
Lane Intra-pair Skew at RX package pins	$L_{RX\text{-}SKEW\text{-}INTRA\_CHIP\_High\text{-}Bit\text{-}Rate}$			100	ps	Maximum skew limit between D+ and D- of the same lane.
Intra-pair Skew Specification for Reduced Bit Rate						
Lane Intra-pair Skew at RX package pins	$L_{RX\text{-}SKEW\text{-}INTRA\_CHIP\_Reduced\text{-}Bit\text{-}Rate}$			300	ps	Maximum skew limit between D+ and D- of the same lane.
Jitter Tracking Bandwidth	$F_{RX\text{-}TRACKING\text{-}BW}$	-20			MHz	Minimum CDR tracking bandwidth at the receiver.

Figure 87. HDMI and DVI receiver AC characteristics

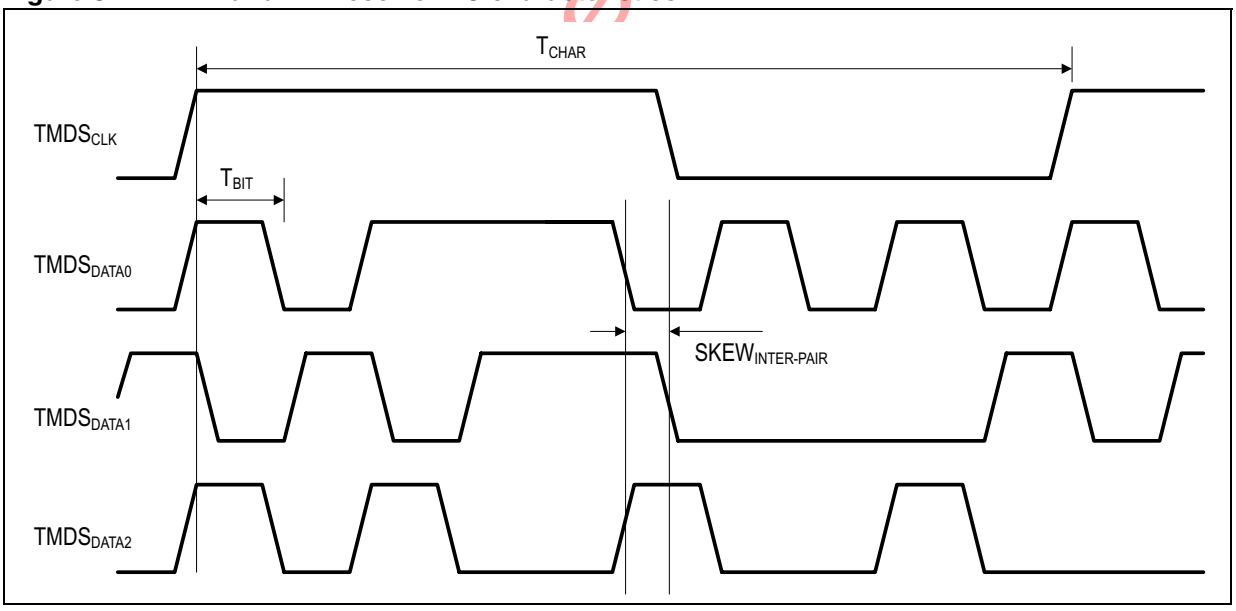


Table 41. HDMI receiver AC characteristics

AC characteristics	Min	Typical	Max	Units	Notes
Input clock frequency	25		300 (TBD)	MHz	
Differential input (peak-to-peak)	150		1560	mV	
Intra-pair skew tolerance			0.4	Tbit	(1)

Table 41. HDMI receiver AC characteristics

AC characteristics	Min	Typical	Max	Units	Notes
Inter-pair skew tolerance			0.2Tchar + 1.78nS	nS	
Input clock jitter tolerance			0.3	Tbit	(2)

1. Tbit (UI) is defined as 1/10 of TMDS clock period (Tchar).
2. With equalizer at TMDS clock frequency of 222.75 MHz.

9 Terminology

Table 42. Terminology

Term	Definition
A/V	Audio and Video
AC3	Adaptive Transform Coder 3 (relates to the bitstream format of Dolby Digital)
ACK	Acknowledge
ACR	Address Check Reply
ACC	Automatic Chroma Control
ADC	Analog-to-Digital Converter
ADSC	Audio Data-Stream Controller
AGP	Accelerated Graphics Port
API	Application Programming Interface
ARGB	Alpha Red Green Blue (Color coding technique)
ARIB	Association of Radio Industries and Businesses (Standardization organization in Japan)
ASC	Asynchronous Serial Controller (Also referred to as a UART)
ATSC	Advanced Television Systems Committee (Standardization committee in the USA)
AVI	Audio Video Interchange
CA	Conditional Access
CableCARD	The technology created by the United States cable television industry in response to government mandates by the FCC to separate the internal functions of integrated set-top boxes and allow third-party manufacturers to sell devices with built-in digital cable tuners directly to consumers
CCIR 601-656	The name of a standard published by the CCIR (now ITU-R) for encoding interlaced analog video signals in digital form
CC	Closed Caption
CD	Compressed Data
CEC	Consumer Electronics Control
CGMS	Copy Generation Management System
CI	Common Interface
CLUT	Color Look-Up Table
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
CRT	Cathode Ray Tube
CSDi™	Contour Sensitive Deinterlacer™
CTI	Color Transient Improvement
CVBS	Composite Video Broadcasting System
D1/HD	High definition digital TV format

Table 42. Terminology (continued)

Term	Definition
DAC	Digital to Analog Convertor
DCP	Digital Content Protection
DCR	Dot-Crawl Reducer
DDC	Display Data Channel
DDR2	Double-data-rate two synchronous dynamic random access memory
DEI	Deinterlacer
DES	Data Encryption Standard
DLP	Digital Light Processing (A technology used in projectors and video projectors)
DMA	Direct Memory Access
DMD	Dot Matrix Display
DSD	Direct Stream Digital
DSP	Digital Signal Processor
DTS	Digital Theater System
DTV	Digital TV
DVB	Digital Video Broadcasting
DVB-CI	A common interface for accessing scrambled content.
DVD	Digital Versatile Disk
ECM	Entitlement Control Message
E-DDC	Enhanced DDC
E-EDID	Enhanced Extended Display Identification Data
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMI	Electromagnetic Interference
EMI	External Memory Interface
EMM	Entitlement Management Message
EOM	End Of Message
EPG	Electronic Program Guide
ES	Elementary Stream
ESD	Electrostatic discharge
ETSI	European Telecommunications Standards Institute
FB	Fast Blanking
FCS	Frame Check Sequence
FE	Front End
FIFO	First In First Out
FMD	Film Mode Detection
FPD	Flat Panel Display

Table 42. Terminology (continued)

Term	Definition
FPU	Floating Point Unit
GDP	Graphics Display Plug
HBDCP	High-Bandwidth Digital Content Protection
HD	High Definition (TV)
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
HDMIRX	HDMI Receiver
HDTV	High Definition TV
HPD	Hot Plug Detect
HSRC	Horizontal Sample Rate Convertor
HW	Hardware
I/O	Input Output
I²S	Inter-IC Sound (Serial bus interface standard used for connecting digital audio devices together.)
ICD	In-Circuit Debugging
iDTV	Integrated Digital TV
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
IIF	Input interface
IP	Internet Protocol
IQI	Image Quality Improvement
IR	Infra-red
IRP	Infra-red Receiver Preprocessor
ITU	International Telecommunication Union
JPEG	Joint Photographic Experts Group (A commonly used standard method of compression for photographic images.)
JTAG	Joint Test Action Group (Technique used for testing printed circuit boards)
LCD	Liquid Crystal Display
LFE	Low-Frequency Effects
LMI	Local Memory Interface
LMM	Long Match Mode
LTI	Luma Transient Improvement
LVDS	Low Voltage Differential Signaling, a transmission method for sending digital information, used for LCD panel interface.
MB	Macro Block
MCHI	Multi-card Host Interface (MCARD SPI interface)

Table 42. Terminology (continued)

Term	Definition
MCU	Microcontroller Unit
MEMC	Motion Estimation Motion Compensation
MHEG-5	Multimedia and Hypermedia information coding Expert Group-5. A specification devised for the middleware of digital teletext services in the United Kingdom.
MHP	Multimedia Home Platform
MIPS	Million Instructions Per Second
MMM	MAC Match Mode
MMU	Memory Management Unit
MP@HL	Main Profile/High Level
MP@ML	Main Profile/Main Level
MP3	MPEG-1 Audio Layer 3 (Audio compression technique)
MPEG	Moving Pictures Experts Group (Audio and video compression technique)
MPEG-1	A group of audio and video coding and compression standards. MPEG-1 video is used by the video CD format.
MPEG-2	A group of coding and compression standards for audio and video, published as the ISO/IEC 13818 international standard. MPEG-2 is used for the TS.
MPTS	Multi-program Transport Stream
Multi2	A block cipher used for encryption of high-definition television broadcasts in Japan.
NTSC	National Television Systems Committee (Analog TV standard for the USA)
OOB	Out Of Band
OSD	On Screen Display
PAG	Picture And Graphic
PAL	Phase Alternating Line (Analog TV standard for most of Europe)
PAP	Picture And Picture
PAT	Picture And Text
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PCR	Program Counter Reference/Program Clock Reference
PDP	Plasma Display Panel
PER	PERipheral interface
PES	Packetized Elementary Stream
PID	Packet ID (identifier)
PIO	Programmed Input Output
PLL	Phase Locked Loop
POD	Point of Deployment
PRS	Pipeline Reset

Table 42. Terminology (continued)

Term	Definition
PSD	Power Spectral Density
PSI	Program Specific Information
PTI	Programmable Transport Interface
PTS	Presentation Time Stamp
PVR	Personal Video Recorder
PWM	Pulse Width Modulation
RAM	Random Access Memory (volatile memory)
RGB	Red Green Blue
RISC	Reduced Instruction Set Computer
RPTV	Rear Projection TV
RTC	Real Time Clock
S/PDIF	Sony/Philips Digital Interface Format
SACD	Super Audio Compact Disc
SCART	From “Syndicat des Constructeurs d'Appareils Radiorécepteurs et Téléviseurs”. A French-originated standard and associated 21-pin connector for connecting audio-visual equipment together.
SCD	Start Code Detector Unit
SCH	Start Code Hit
SCIF	Serial Communication Interface
SCL	Serial Clock (I²C bus clock line)
SD	Standard Definition (TV)
SDA	Serial Data (I²C bus data line)
SECAM	From “Séquentiel couleur à mémoire” (French for “sequential color with memory”). An analog color television system first used in France.
SF	Section Filtering
SI	Service Information
SIF	Sound Intermediate Frequency
SMM	Short Match Mode
SMPTE	Society of Motion Picture and Television Engineers.
SOG	Sync on Green A technology used in monitors.
SPTS	Single Program Transport Stream
SRAM	Static RAM
SRC	Sample Rate Converter
SRS	Software Reset
SSCG	Spread Spectrum Clock Generator
STB	Set Top Box

Table 42. Terminology (continued)

Term	Definition
STC	System Time Clock
SVGA	Super Video Graphics Array. An analog computer display standard. The term SVGA is often used to refer to a resolution of 800 × 600 pixels.
SVHS	Super VHS
SXGA	Super Extended Graphics Array. Standard monitor resolution of 1280 × 1024 pixels.
TC	Transport Controller
TLB	Translation Look-aside Buffer
TMDS	Transition Minimized Differential Signaling
TS	Transport Stream
TSGDMA	Transport Stream Generator DMA
TSSM	Transport Stream Switching Matrix
UART	Universal Asynchronous Receiver Transmitter
UDEC	Uncompress DECoder
UDI	User Debug Interface
UDS	Uncompress Data System
USB	Universal Serial Bus
UXGA	Ultra eXtended Graphics Array. A standard monitor resolution of 1600 × 1200 pixels.
VBI	Vertical Blanking Interval
VBV delay	Video Buffering Verifier
VCR	Video Cassette Recorder
VDP	Video Display Processor
VGA	Video Graphics Array. An analog computer display standard. The term VGA is often used to refer to a resolution of 640 × 480 pixels.
VHS	Video Home System. A recording and playing standard for analog video cassette recorders.
VHSRC	Vertical and Horizontal Sample Rate Converter
VLD	Variable Length Decode
VMx	Versatile Matrix
VPS	Video Program System
VSRC	Vertical Sample Rate Converter
VTG	Video Timing Generator
WDT	Watchdog Timer
WSS	Wide Screen Signaling
WST	World System Teletext
XGA	eXtended Graphics Array. An analog computer display standard. The term XGA is often used to refer to a resolution of 1024 × 768 pixels.

Table 42. Terminology (continued)

Term	Definition
Y/C	Y/C (also known as S-Video) An analog video signal that carries the video data as two separate signals (brightness Y and color C).
YCrCb	A family of color spaces used in video systems. Y is the luma component and Cb and Cr the blue and red chroma components.
YPrPb	A color space used for analog video monitors. – Y carries luminance information. – Pb carries the difference between blue and luminance (B - Y). – Pr carries the difference between red and luminance (R - Y).
YUV	A color space used for analog video monitors.

10 Revision history

Table 43. Document revision history

Date	Revision	Changes
13-Apr-2011	Rev A	Preliminary release.
08-Jul-2011	Rev B	Updated the following: Table 3, Power domains, DISPLAYPORT TRANSMITTER Section 5.12.2 Stereo 3D frame rate conversion Table 11, Mission GPIO signals, GPIO85_OCMINT_PWM4 Table 12, LPM GPIO signals, GPADC_AIN2, LPM_GPIO15_SLV1_SCL, LPM_GPIO16_SLV1_SDA Figures 60-63, STDP93xx and STDP92xx ball out diagram Figures 64-67, STDP73xx ball out diagram Ball lists: Table 14, Table 16, Table 18, Table 20, Table 21, Table 22, Table 23, Table 25 Table 31, Maximum speed, Digital Video Input Clocks
03-Nov-2011	Rev C	Added features to Features, Descriptions, and Main features sections. Updated the following: Figures 8-9, Video input matrix Figure 32, 3D format capture and processing Figure 33, Video processor overview Figure 39, Output data flow Section 5.12. 5, Split LVDS drive Chapter 6, BGA footprint and ball lists Chapter 8, Packages Table 2, Athena selection table Table 6, STDP73xx DDR speed estimates: Required DDR devices column Table 7, DDR speed estimates Table 29, Absolute max ratings Table 31, Supply currents Table 32, Maximum speed of operation Table 39, DDR interface writing time Table 40, DDR interface read timing
20-Mar-2012	Rev D	Updated for silicon rev. BB: Athena Block diagram Table 2, Athena selection table part numbers Figure 9, STDP73xx video input matrix Figures 47-51, Data mapping for LVDS figures' titles have changed Table 29, Data changes for HBM, CDM, and Latch-up. MM has been removed

Table 43. Document revision history

Date	Revision	Changes
26-Apr-2012	Rev E	Table 30 and 31: all data updated.
08-May-2012	Rev F	Chapter 7: Packages updated.

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