QCA7000 HomePlug® Green PHY Single Chip Solution

Data Sheet

MKG-15723 Ver. 11.0

October 8, 2012

Confidential and Proprietary - Qualcomm Atheros, Inc.

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Revision History

Revision	Date	Description
Ver. 1.0	May 2011	Preliminary QCA7000 Release
Ver. 2.0	August 2011	Revised some pinout and signal names
Ver. 3.0	October 2011	Revised Figure 2-1. QCA7000 8x8 mm 68-Pin QFN and Figure 2-3. QCA7000 Internal Block Diagram. Updated cpu_on, wrbuf_error and rd_buf_error descriptions throughout the document. Updated Package Dimensions content.
Ver. 4.0	November 2011	Revised Table 2-5 pin assignments.
Ver. 5.0	December 6, 2011	Revised Table 6-1 and Figure 6.1
Ver. 6.0	December 16, 2011	Revised Table 2-1 and Table 2-2
Ver. 7.0	February 2012	Revised Table 2-5; formatted Table 4-1 to stay on same page. Revised QCA7000 Power Supply Requirements.
Ver. 8.0	March 2012	Revised SPI Config register (SPI_CONFIG) Table
Ver. 9.0	June 2012	Revised Recommended Operating Conditions and Power Supply Requirements. Revised RESET_L leading edge point in timing diagram.
Ver. 10.0	September 2012	Revised Section 1.2 added Industrial temperature required Firmware version. Revised Table 2-5; added Table 2-6. Revised Section 4.2.1; revised Table 4-1; revised Section 4.3.2.
Ver. 11.0	October 2012	Revised Table 5-2 added Industrial Temperature Tcase values

Contents

1 General Information

1.1 Description

The QCA7000 is the latest addition to the Powerline Communications (PLC) portfolio of communication ICs from Atheros. It is fully compliant with the HomePlug Green PHY (HPGP) specification. HomePlug's Green PHY specification was developed specifically to meet the needs of the home, utility and Smart Grid applications. The QCA7000 uses a robust OFDM (ROBO) mode of communication that provides extended coverage and reliable communication over Powerline networks. However, the QCA7000 has been designed to meet specific industry requirements for HomePlug AV compatibility. The QCA7000 is interoperable up to the HPGP maximum data rate of 10 Mbps and offers lower power consumption, lower product complexity and reduced BOM costs.

The QCA7000 is fully interoperable with HomePlug AV and IEEE 1901 compliant products. The QCA7000 supports HomePlug Green PHY Distributed Bandwidth Control to ensure effective coexistence with HPAV equipment operating in close proximity on the same Powerline infrastructure. The IC also supports HPGP Power Save Mode, which enables the IC to enter and exit a low power state on a scheduled basis to maintain network synchronization.

An integrated switching power supply provides the 1.2 V core voltage. No external active components are required. Inductors and capacitors are required for the bypass circuit.

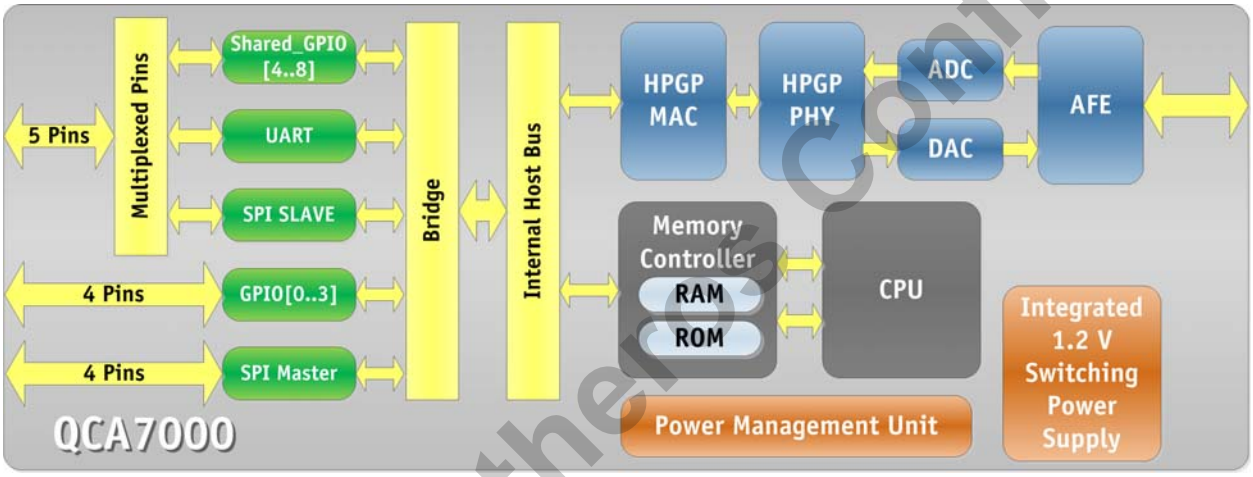
1.2 Features

- Compliant with HomePlug Green PHY specification
- Interoperable with HomePlug AV specification and IEEE 1901 Standard up to the maximum HPGP data rate
- Operates on 240 VAC, 120 VAC, 24 VAC, and DC lines
- Single chip solution with integrated analog front end and line driver
- Lower cost and power consumption than existing HPAV solutions for lower data rates - ideal for Smart Grid applications
- Industrial temperature range for extended temperature and smart meter applications
  - Requires QCA7000 HomePlug Green PHY Firmware v1.0.0-07 and higher
- Host interfaces: SPI (Slave) and UART
- Boot from host or external FLASH memory
- Dedicated FLASH memory port (SPI master)
- Supports Robust OFDM (ROBO) mode modulation: 4 Mbps to 10 Mbps PHY rates
- Powered from single 3.3 VDC rail with integrated Power Management Unit
- RoHS Compliant: 8 x 8 mm 68 pin QFN

1.3 Applications

- Smart Meters
- Energy Management Systems
- Programmable Controlled Thermostats
- Remote Metering Devices
- Solar Panels
- Industrial Applications

1.4 QCA7000 Functional Block Diagram



1.5 Conventions Used in this Data Sheet

Unit or Abbreviation	Definition	Comment
k	Kilo-	1,000
M	Meg(a)-	1,000,000
b	bit(s)	
B	Byte(s)	
0x	Hexadecimal	
0b	Binary	
sps	Samples per second	
ps	Pico-second	
ns	Nano-second	
μs	Micro-second	
ms	Milli-second	
bps	Bits per second	
Mbps	Megabits per second	
μin	Micro-inches	
mil	Thousandth of an inch	0.001”
mm	Milli-meter	
Ω	Ohm	
mΩ	Milli-Ohm	
A	Ampere	
mA	Milli-Ampere	
V	Volts	
mV	Milli-Volts	0.001

2 Pin Descriptions

This section contains both a package pinout (see Figure 2-1, Table 2-1 and Table 2-2) and tabular listings of the signal descriptions.

The following nomenclature is used for signal names:

DNC	No connection should be made to this pin
_L	Low true signal
_P	At the end of the signal name, indicates the positive side of a differential signal
_N	At the end of the signal name indicates the negative side of a differential signal
RSVD	Reserved

The following nomenclature is used for signal types:

GND	A ground signal
I	Digital input signal
I/O	A digital bidirectional signal
IA	Analog input signal
IH	Input signals with weak internal pull-up, to prevent signals from floating when left open
IL	Input signals with weak internal pull-down, to prevent signals from floating when left open
O	A digital output signal
OA	An analog output signal
P	A power signal

2.1 QCA7000 Signals

2.1.1 QCA7000 Pin Assignments

The QCA7000 package is a Pb-free, 8x8 mm 68-pin QFN

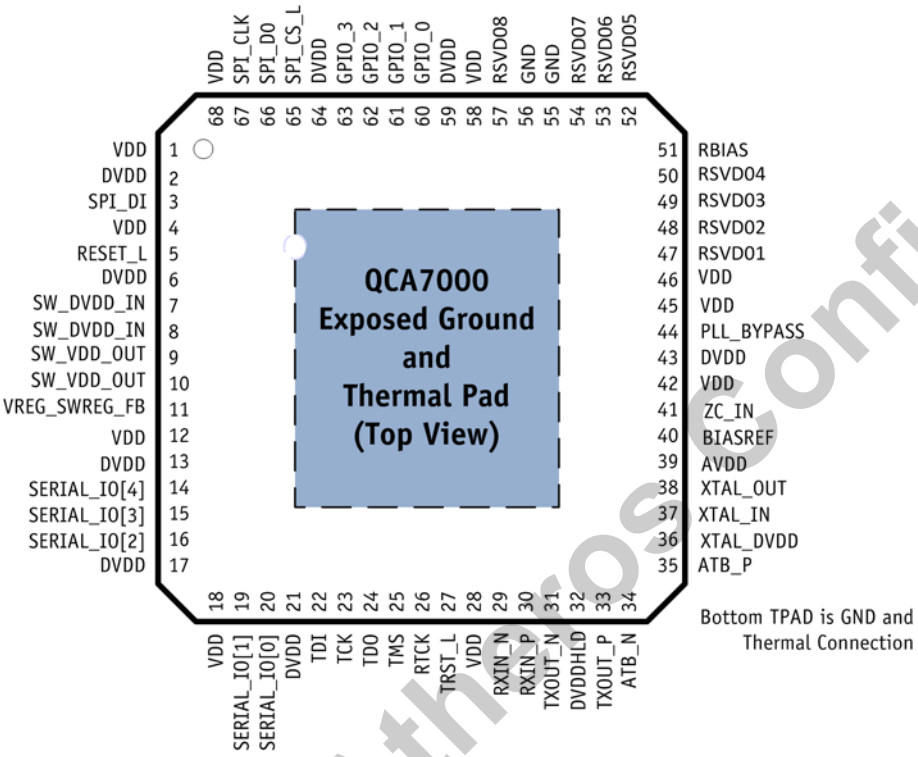


Figure 2-1 QCA7000 8x8 mm 68-Pin QFN

NOTE: The Thermal Pad (TPAD) is on the bottom of the IC.

Table 2-1 Signal-to-Pin Relationships and Descriptions

Pin	Symbol	Type	Interface	Description
1	VDD	P		1.2 V core voltage
2	DVDD	P		3.3 V
3	SPI_DI	I	SPI Master Bus DI	SPI Data In. The QCA7000 Master SPI_DI is used to transfer FW into the QCA7000. SPI_DI is latched on the rising edge of SPI_CLK. SPI Mode 3
4	VDD	P		1.2 V core voltage
5	RESET_L	I	Reset Input	Power on Reset. Active-low Power-on-Reset input.
6	DVDD	P		3.3 V
7	SW_DVDD_IN	P	Switching Regulator	3.3 V input of internal Switching Regulator
8	SW_DVDD_IN	P	Switching Regulator	3.3 V input of internal Switching Regulator
9	SW_VDD_OUT	P	Switching Regulator	1.2 V output of internal Switching Regulator
10	SW_VDD_OUT	P	Switching Regulator	1.2 V output of internal Switching Regulator
11	VREG_SWREG_FB	P	Switching Regulator	Switching Regulator Feedback Pin. Connected to the regulated 1.2 V supply bus.
12	VDD	P		1.2 V core voltage
13	DVDD	P		3.3 V
14	SERIAL_IO[4]	I/O	SERIAL_IO/GPIO	SERIAL I/O 4 - UART, SPI Slave or Shared_GPIO_8
15	SERIAL_IO[3]	I/O	SERIAL_IO/GPIO	SERIAL I/O 3 - UART, SPI Slave or Shared_GPIO_7
16	SERIAL_IO[2]	I/O	SERIAL_IO/GPIO	SERIAL I/O 2 - UART, SPI Slave or Shared_GPIO_6
17	DVDD	P		3.3 V
18	VDD	P		1.2 V core voltage
19	SERIAL_IO[1]	I/O	SERIAL_IO/GPIO	SERIAL I/O 1 - UART, SPI Slave or Shared_GPIO_5
20	SERIAL_IO[0]	I/O	SERIAL_IO/GPIO	SERIAL I/O 0 - UART, SPI Slave or Shared_GPIO_4
21	DVDD	P		3.3 V
22	TDI	I	JTAG	10K to GND for normal operation.
23	TCK	O	JTAG	10K to GND for normal operation.
24	TDO	I/O	JTAG	3.3 K to GND for normal operation.
25	TMS	I	JTAG	10 K to GND for normal operation.
26	RTCK	O	JTAG	Leave unconnected for normal operation.
27	TRST_L	I	JTAG	10 K to GND for normal operation.
28	VDD	P		1.2 V core voltage
29	RXIN_N	IA	ADC/DAC	Differential In. Negative differential input
30	RXIN_P	IA	ADC/DAC	Differential In. Positive differential input
31	TXOUT_N	OA	ADC/DAC	Differential Out. Negative differential output of the TX PGA
32	DVDDHLD	P		3.3 V Power for Analog Front End
33	TXOUT_P	OA	ADC/DAC	Differential Out. Positive differential output of the TX PGA
34	ATB_N	IA	Reserved	Make NO Connection. Analog Test pin. Reserved

Table 2-1 Signal-to-Pin Relationships and Descriptions (cont.)

Pin	Symbol	Type	Interface	Description
35	ATB_P	IA	Reserved	Make NO Connection. Analog Test pin. Reserved
36	XTAL_DVDD	P	ADC/DAC	3.3 V Analog
37	XTAL_IN	I	Crystal	Crystal Oscillator Inverter Input
38	XTAL_OUT	I/O	XTAL	External Oscillator Input/Crystal Oscillator Output
39	AVDD	P	ADC/DAC	1.2 V Analog
40	BIASREF	P	Analog	External Bias Resistor
41	ZC_IN[1]	IA	Analog	Zero Cross Input. Minimum: 100 mVpp, AC coupled and maximum: 3.3 Vpp, AC coupled
42	VDD	P		1.2 V core voltage
43	DVDD	P		3.3 V
44	PLL_BYPASS	I	Phase Lock Loop	Phase Lock Loop Bypass normally 10 KΩ to ground
45	VDD	P		1.2 V core voltage
46	VDD	P		1.2 V core voltage
47	RSVD01[2]		Reserved	Connect to 3.3 V
48	RSVD02		Reserved	Connect to Ground through a 0.1 μF capacitor
49	RSVD03		Reserved	Connect to Ground through a 0.1 μF capacitor
50	RSVD04		Reserved	Connect to 1.2 V and bypass to Ground using a 0.1 μF capacitor
51	RBIAS		Reserved	BIAS current set by resistor to ground
52	RSVD05		Reserved	Connect to Pin 48
53	RSVD06		Reserved	Do Not Connect
54	RSVD07		Reserved	Do Not Connect
55	GND	P		Connect to Ground through a 0 Ω resistor
56	GND	P		Connect to Ground through a 0 Ω resistor
57	RSVD08		Reserved	Connect to Pin 50
58	VDD	P		1.2 V core voltage
59	DVDD	P		3.3 V
60	GPIO_0	I/O	GPIO	GPIO 0 Sets mode at power on, then becomes I/O
61	GPIO_1	I/O	GPIO	GPIO 1 Sets mode at power on, then becomes I/O
62	GPIO_2	I/O	GPIO	GPIO 2 Sets mode at power on, then becomes I/O
63	GPIO_3	I/O	GPIO	GPIO 3 Sets mode at power on, then becomes I/O
64	DVDD	P		3.3 V
65	SPI_CS_L	O	SPI Master Bus	SPI Chip Select. SPI_CS_N is the chip select used to enable the serial boot flash. This signal is tri-stated and held high with a weak internal pull-up while RESET_L is asserted.

Table 2-1 Signal-to-Pin Relationships and Descriptions (cont.)

Pin	Symbol	Type	Interface	Description
66	SPI_D0	O	SPI Master Bus	SPI Data Out. SPI_DO is used to transfer serial data out of the QCA7000. SPI_DO is shifted out on the falling edge of SPI_CLK. This signal is tri-stated and held low with a weak internal pull-down while RESET_L is asserted.
67	SPI_CLK	O	SPI Master Bus	SPI Clock. SPI_CLK provides the SPI interface timing. Instructions, addresses, or data present at SPI_DI are latched on the rising edge of SPI_CLK. Data on SPI_DO changes after the falling edge of SPI_CLK. This signal is tri-stated and held low with a weak internal pull-down while RESET_L is asserted.
68	VDD	P		1.2 V core voltage
TPAD	GND	P	Power and Thermal	Power Ground and Thermal connection to PCB

1. If ZC_IN input is not used, connect ZC_IN to ground.
2. See 60005311 schematic for circuit details.

2.1.2 Signal-to-Pin Relationships and Descriptions

Table 2-2 Signal-to-Pin Relationships and Descriptions

Pin	Symbol	Type	Interface	Description
System Interface Signals				
5	RESET_L	I	Reset Input	Power on Reset. Active-low Power-on-Reset input.
44	PLL_BYPASS	I	Phase Lock Loop	Phase Lock Loop Bypass normally 10 KΩ to ground
Serial I/O See Table 3-2 and Table 3-3				
14	SERIAL_IO[4]	I/O	SERIAL_IO/GPIO	SERIAL I/O 4 - UART, SPI Slave or Shared_GPIO_8
15	SERIAL_IO[3]	I/O	SERIAL_IO/GPIO	SERIAL I/O 3 - UART, SPI Slave or Shared_GPIO_7
16	SERIAL_IO[2]	I/O	SERIAL_IO/GPIO	SERIAL I/O 2 - UART, SPI Slave or Shared_GPIO_6
19	SERIAL_IO[1]	I/O	SERIAL_IO/GPIO	SERIAL I/O 1 - UART, SPI Slave or Shared_GPIO_5
20	SERIAL_IO[0]	I/O	SERIAL_IO/GPIO	SERIAL I/O 0 - UART, SPI Slave or Shared_GPIO_4
JTAG Port				
22	TDI	I	JTAG	10K to GND for normal operation.
23	TCK	O	JTAG	10K to GND for normal operation.
24	TDO	I/O	JTAG	3.3 K to GND for normal operation.
25	TMS	I	JTAG	10K to GND for normal operation.
26	RTCK	O	JTAG	Leave unconnected for normal operation.
27	TRST_L	I	JTAG	10 K to GND for normal operation.
Crystal Interface				
37	XTAL_IN	I	Crystal	Crystal Oscillator Inverter Input
38	XTAL_OUT	I/O	XTAL	External Oscillator Input/Crystal Oscillator Output

Table 2-2 Signal-to-Pin Relationships and Descriptions (cont.)

Pin	Symbol	Type	Interface	Description
GPIO Bus Interfaces				
60	GPIO_0	I/O	GPIO	GPIO 0 Sets mode at power on, then becomes I/O
61	GPIO_1	I/O	GPIO	GPIO 1 Sets mode at power on, then becomes I/O
62	GPIO_2	I/O	GPIO	GPIO 2 Sets mode at power on, then becomes I/O
63	GPIO_3	I/O	GPIO	GPIO 3 Sets mode at power on, then becomes I/O
SPI Master Port for NVM Flash				
3	SPI_DI	I	SPI Master Bus	SPI Data In. The QCA7000 Master SPI_DI is used to transfer FW into the QCA7000. SPI_DI is latched on the rising edge of SPI_CLK. SPI Mode 3
65	SPI_CS_L	O	SPI Master Bus	SPI Chip Select. SPI_CS_N is the chip select used to enable the serial boot flash. This signal is tri-stated and held high with a weak internal pull-up while RESET_L is asserted.
66	SPI_D0	O	SPI Master Bus	SPI Data Out. SPI_DO is used to transfer serial data out of the QCA7000. SPI_DO is shifted out on the falling edge of SPI_CLK. This signal is tri-stated and held low with a weak internal pull-down while RESET_L is asserted.
67	SPI_CLK	O	SPI Master Bus	SPI Clock. SPI_CLK provides the SPI interface timing. Instructions, addresses, or data present at SPI_DI are latched on the rising edge of SPI_CLK. Data on SPI_DO changes after the falling edge of SPI_CLK. This signal is tri-stated and held low with a weak internal pull-down while RESET_L is asserted.
Power Supply				
1	VDD	P		1.2 V core voltage
2	DVDD	P		3.3 V
4	VDD	P		1.2 V core voltage
6	DVDD	P		3.3 V
7	SW_DVDD_IN	P	Switching Regulator	3.3 V input of internal Switching Regulator
8	SW_DVDD_IN	P	Switching Regulator	3.3 V input of internal Switching Regulator
9	SW_VDD_OUT	P	Switching Regulator	1.2 V output of internal Switching Regulator
10	SW_VDD_OUT	P	Switching Regulator	1.2 V output of internal Switching Regulator
11	VREG_SWREG_FB	P	Switching Regulator	Switching Regulator Feedback Pin. Connected to the regulated 1.2 V supply bus.
12	VDD	P		1.2 V core voltage
13	DVDD	P		3.3 V
17	DVDD	P		3.3 V
18	VDD	P		1.2 V core voltage
21	DVDD	P		3.3 V
28	VDD	P		1.2 V core voltage
32	DVDDHLD	P		3.3 V Power for Analog Front End

Table 2-2 Signal-to-Pin Relationships and Descriptions (cont.)

Pin	Symbol	Type	Interface	Description
36	XTAL_DVDD	P	ADC/DAC	3.3 V Analog
39	AVDD	P	ADC/DAC	1.2 V Analog filter voltage
42	VDD	P		1.2 V core voltage
43	DVDD	P		3.3 V
45	VDD	P		1.2 V core voltage
46	VDD	P		1.2 V core voltage
51	RBIAS	P	Reserved	BIAS current set by resistor to ground
55	GND	P		Connect to Ground through a 0 Ω resistor
56	GND	P		Connect to Ground through a 0 Ω resistor
58	VDD	P		1.2 V core voltage
59	DVDD	P		3.3 V
64	DVDD	P		3.3 V
68	VDD	P		1.2 V core voltage
TPAD	GND	P	Power and Thermal	Power Ground and Thermal connection to PCB
Analog Signals				
29	RXIN_N	IA	ADC/DAC	Differential In. Negative differential input
30	RXIN_P	IA	ADC/DAC	Differential In. Positive differential input
31	TXOUT_N	OA	ADC/DAC	Differential Out. Negative differential output of the TX PGA
33	TXOUT_P	OA	ADC/DAC	Differential Out. Positive differential output of the TX PGA
34	ATB_N	IA	Reserved	Make NO Connection. Analog Test pin. Reserved
35	ATB_P	IA	Reserved	Make NO Connection. Analog Test pin. Reserved
41	ZC_IN[1]	IA	Analog	Zero Cross Input. Minimum: 100 mVpp, AC coupled and maximum: 3.3 Vpp, AC coupled
40	BIASREF	O	Analog	External Bias Current from resistor
44	PLL_BYPASS	I	Phase Lock Loop	Phase Lock Loop Bypass normally 10 KΩ to ground
47	RSVD01[2]		Reserved	Connect to 3.3 V
48	RSVD02		Reserved	Connect to Ground through a 0.1 μF capacitor
49	RSVD03		Reserved	Connect to Ground through a 0.1 μF capacitor
50	RSVD04		Reserved	Connect to 1.2 V and bypass to Ground using a 0.1 μF capacitor
52	RSVD05		Reserved	Connect to Pin 48
53	RSVD06		Reserved	Do Not Connect
54	RSVD07		Reserved	Do Not Connect
57	RSVD08		Reserved	Connect to Pin 50

1. If ZC_IN input is not used, connect ZC_IN to ground.
2. See 60005311 schematic for circuit details.

2.2 System Introduction

The QCA7000 is designed to support HomePlug GreenPHY (GP or HPGP) applications. QCA7000 applications also include Smart Grid products. This document describes the details of the Atheros QCA7000 System on Chip (SoC) Integrated Circuit (IC).

2.2.1 System Overview

The QCA7000 is a complete system on a chip providing baseband Powerline Communication (PLC) processor/transceiver with serial and parallel data Input and Output (I/O). The key objectives are:

- Highly integrated IC for HPGP and SmartGrid Applications
- Small, low-cost 68-QFN Package
- Compatible with full HomePlug (HP) 2 MHz to 30 MHz PLC channel
- Coexists with HomePlugAV and supports data rate up to the maximum HPGP specification
- General Purpose single bit I/O - GPIO
- SPI Master Mode serial I/O interface to load and program NVM based Firm Ware (FW)
- Serial data I/O supported by UART
- UART or SPI Slave Host Port software interface including drivers
- Integrated ARM CPU & integrated memory for low pin count
- Integrated 1.2 V switching regulator for single 3.3 V supply operation
- Integrated Analog Front End for short distance communications
- HPGP compliant
- IEEE1901 and HPAV interoperable
- 10 Mbps Powerline PHY Rate (Max)

2.2.2 Integrated Functions

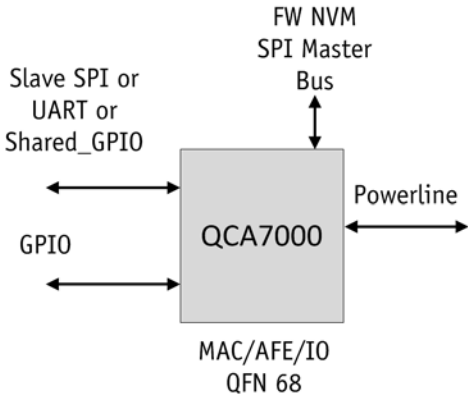


Figure 2-2 Basic Block Diagram

Configuration straps are read at power on and determine the function of various input and output pin options.

The following QCA7000 diagram Figure 2-2 shows some details of the internal functional blocks. The QCA7000 Analog Front End (AFE) includes the A/D and D/A converters, the analog receive amplifier, analog transmit amplifier, and analog line driver that supports the HomePlug-GP standard. An integrated analog zero crossing detector is included.

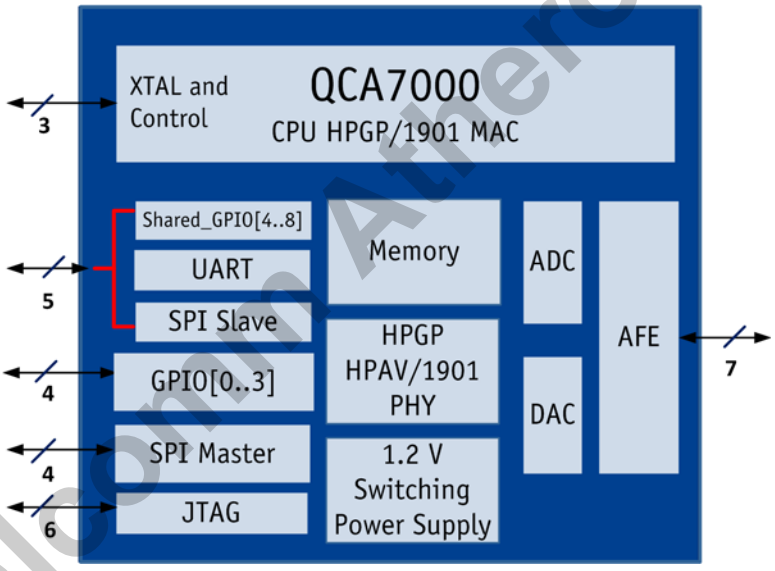


Figure 2-3 QCA7000 Internal Block Diagram

An external Powerline coupler passes HomePlug- Green PHY OFDM signals to and from the Powerline while providing isolation from hazardous Powerline voltages. The QCA7000 PHY is compliant with the IEEE 1901 Draft Standard with full support for the Inter System Protocol (ISP) including both in-home and access requirements up to the QCA7000 maximum data rate.

The Control Program Firmware (FW) is automatically read from an external Non Volatile Memory (NVM) flash IC after power on. This FW contains the application code and control parameters for all system elements.

2.2.2.1 Core Voltage Power Supply

The QCA7000 includes an integrated on-board core voltage 1.2 V Power Supply requiring no external active components. Inductors and capacitors are required for the Pi network bypass circuit. See the QCA7000 Reference Design for component values and placement on the PCB. Multiple vias (four or more) are required on all through board connections delivering core voltage.

2.2.2.2 Additional Internal Functions

Within the QCA7000, the HomePlug-GP MAC functions are executed in firmware running on the embedded ARM926 CPU, supported by DMA hardware, and on-chip SRAM for run-time code and data-store. The HomePlug-GP MAC firmware running on the CPU oversees operation of the integrated HomePlug-GP PHY via an interface that carries control/status information as well as transmits and receives data packets.

General-purpose I/O pins (GPIO) are available for application I/O and to drive LEDs directly to indicate PLC link status, as well as to indicate user reset or network-attach events. A dedicated QCA7000 IC sub-system is responsible for power-management functions.

An on-board PLL and on-chip crystal oscillator are used to generate the required system clocks. Various loop-back modes support manufacturing test.

2.3 Zero Cross

The QCA7000 has an analog amplifier circuit that detects when the 50 Hz or 60 Hz AC powerline voltage crosses through zero volts. This input pin is self biased so it is AC coupled by a capacitor. This input only requires a small AC waveform of about 100mVpp. This small analog voltage requirement simplifies the external Zero Cross circuit and greatly reduces power dissipation lowers resulting heat and cost.

This temporal information synchronizes the channel adaptation of the QCA7000 IC to any line cycle periodic noise that maybe present on the powerline. This synchronization information is used by software algorithms to optimize HP Powerline Communications in high noise conditions.

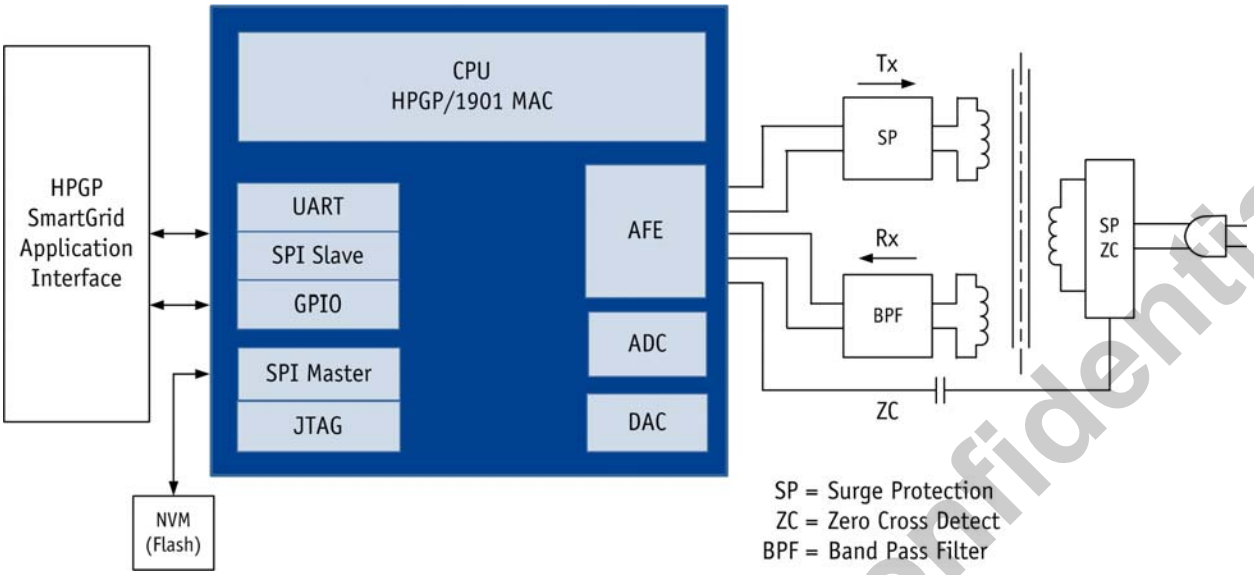


Figure 2-4 HPGP System Block Diagram

2.4 QCA7000 Power On Configuration Strap Values and Defaults

The following table shows GPIO pins that are read at power on to configure the operation of the QCA7000. The default, internal pull-up and pull-down resistor is shown in the right hand column. It is good design practice to set strap pins high or low by placing a 3 K to 10 K resistor tied to ground or to the 3.3 V power supply. This makes testing and changing modes for test easy.

After the Reset signal goes high several GIPIO pins are used by default by the FW program or can be used by the designer for general purpose I/O functions

Table 2-3 Configurative Strap Functions and Internal Defaults

Strap Function	Pin	QCA7000 Pin Name	Function Description	Internal Pull-Up/Down
Boot from NVM	60	GPIO_0	High (1) indicates boot code loads from NVM flash device on the Master SPI bus port.	PU (1)
Boot from SPI Slave Bus	61	GPIO_1	Must be Pulled LOW (0) for all QCA7000 applications.	PU (1)
SPI Slave Mode	62	GPIO_2	Low (0) = Legacy command/data. 1 = Burst command/data	PD (0)
User I/O	63	GPIO_3	Not defined during Boot Up	PD (0)

While the QCA7000 has low current internal pull up and pull down resistors it is recommended that all Configuration Straps have external resistors for easy connections and changing during troubleshooting and test.

- GPIO[0] Boot from external NVM (flash) device using the SPI Master bus
- GPIO[1] must be held low (0) at reset for all applications.

- The following two figures show the circuit arrangement for GPIO pull-up and pull-down.

  NOTE These are the connections if a LED is desired on one of these pins.

- Do not connect any GPIO directly to ground or to the 3.3 V bus. After the RESET_L signal goes high FW may drive any GPIO pin to an output. Any pin may be driven high or low by FW to indicate system status using the LED outputs.

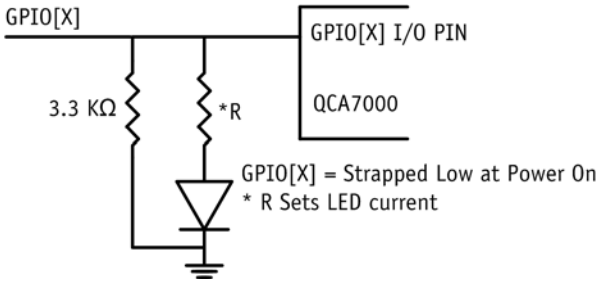


Figure 2-5 QCA7000 Pull-Down LED Strapping

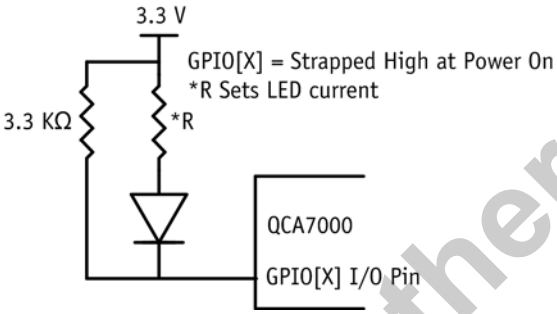


Figure 2-6 QCA7000 Pull-Up LED Strapping

The following additional straps are also available in any mode of operation:

Table 2-4 Special Straps for Test

Symbol	Pin	Strap=1	Strap=0
PLL-Bypass	44	Used for test. 1 = disable the PLL	Normal mode. PD (0) internally

Special test conditions are enabled by the pin straps listed in Table 2-4.

Table 2-5 Other Internal Pull-Up Pull-Down Signal List

Symbol	Pin	Description	Internal Pull-Up/Down
TCK	23	JTAG Test Clock Out	PU (1)
TDI	22	JTAG Test Data In	PU (1)
TMS	25	JTAG Test Mode Select	PU (1)
TRST_L	27	JTAG Test Reset	PD (0)
SERIAL_IO[0]	20	SERIAL I/O 0 - UART, SPI Slave or Shared_GPIO_4	PD (0)

Table 2-5 Other Internal Pull-Up Pull-Down Signal List (cont.)

Symbol	Pin	Description	Internal Pull-Up/Down
SERIAL_IO[1]	19	SERIAL I/O 1 - UART, SPI Slave or Shared_GPIO_5	PD (0)
SERIAL_IO[2]	16	SERIAL I/O 2 - UART, SPI Slave or Shared_GPIO_6	PD (0)
SERIAL_IO[3]	15	SERIAL I/O 3 - UART, SPI Slave or Shared_GPIO_7	PD (0)
SERIAL_IO[4]	14	SERIAL I/O 4 - UART, SPI Slave or Shared_GPIO_8	PD (0)

The Mode of the SERIAL_IO[X] pins is set by in internal register by FW. The Internal Pull-Up/Pull down for these pins applies only when the pin is an input as in Shared_GPIO[X] mode or some SPI Slave bus or UART input function.

The main chip reset is the active low RESET_L input. This reset input is first passed through a Schmidt trigger input, and then goes through a simple digital filter before it actually becomes the on-chip reset. This pin is the only filtered input pin.

While this power-on-reset signal is asserted, all clocks on all flops in the chip are active, and all on-chip registers are reset to a default state. To reduce the peak power used during this period of time, the frequency of all clocks is 8 times lower than normal.

Once RESET_L is de-asserted (goes high), the on-chip reset is further extended by a ~4000 clocks to allow the on-chip PLL to lock. At the end of this delay, the internal clocks are brought up to their normal operating frequency, and then the majority of them are gated off. Once the ARM processor is brought out of reset, the processor jumps to address 0xFFFF0000 and the Boot ROM software takes over.

In addition to these hardware initiated resets, there are also numerous sources of software controlled reset within the QCA7000. A MME command on the PLC bus can reset the entire chip as well as the ARM processor. This option is again selected through a software configuration register.

Internal to the QCA7000, there are also numerous sources of reset. The processor can write to internal registers to take individual modules in or out of reset, as well as initiate an entire chip reset. Furthermore, to recover from system problems, a watchdog reset circuit is available that initiates a reset if the software or system have crashed.

The Shared_GPIO[X] pins are not the same as the GPIO pins described earlier. These signal are only available when enabled on the Serial _IO pins.

The strength of these internal pull-ups/pull-downs is specified in Table 2-6.

Table 2-6 Internal Pull-Up/Down Strengths

	Min (µA)	Typ (µA)	Max (µA)
IPU	17.09	28.11	43.87
IPD	14.9	24.02	38.51

3 System Architecture

3.1 Architecture Block Diagram

The QCA7000 SoC and MAC baseline architecture is represented in Figure 3-1.

3.2 Host Interfaces

3.2.1 QCA7000 SPI Master Interfaces

The QCA7000 includes a SPI Master interface for interfacing to an external Non Volatile Memory (NVM -Flash) memory. The SPI Master Bus has dedicated pins and is always available to load the QCA7000 application Firmware (FW). The SPI Master interface signals are outlined in Table 3-1 and shown in Figure 3-2. The SPI Master port has dedicated un-multiplexed data, clock and chip-select pins, can be used to load FW. The NVM write and read cycle timing is fixed by the QCA7000 hardware.

Table 3-1 SPI Master Signal List

Signal Name	Description
SPI_CLK	SPI Master Clock Output
SPI_DO	SPI Master Data Output
SPI_DI	SPI Master Data Input
SPI_CS_L	SPI Master Chip Select Low

3.2.2 QCA7000 Serial Host Interfaces

Two host serial interfaces, UART or SPI Slave, are available for GreenPHY applications. The UART supports frequencies up to 115,200 baud, and has four signal pins: TX Data, RX Data, RTS and CTS. The use of RTS and CTS is completely optional. The SPI Slave and Master ports support the Motorola Mode 3 SPI protocol. The SPI Slave port has dedicated data, clock and chip-select pins. Due to pin limitations, only one of the serial interfaces, the UART or the Slave SPI bus may be used across the 5 pins allocated. These options are outlined in Table 3-2 and are shown in Figure 3-1.

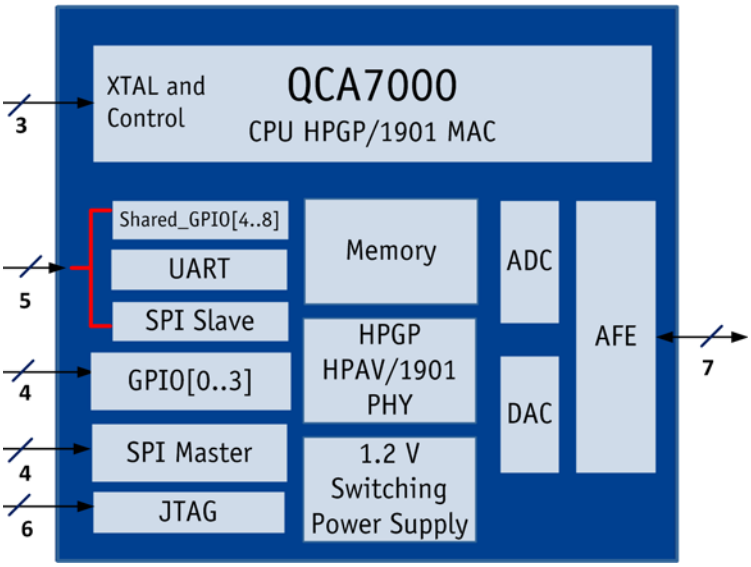


Figure 3-1 QCA7000 SoC and MAC Architecture Block Diagram

Table 3-2 Host Serial Interface Signal List

I/O Pad	GPIO Mode	SPI Slave Mode	UART Mode	UART with RTS/CTS Mode
SERIAL_IO[0]	SHARED_GPIO[4]	SPI Slave Interrupt	SHARED_GPIO[4]	SHARED_GPIO[4]
SERIAL_IO[1]	SHARED_GPIO[5]	SPI Clock	SHARED_GPIO[5]	RTS
SERIAL_IO[2]	SHARED_GPIO[6]	SPI Chip Select	SHARED_GPIO[6]	CTS
SERIAL_IO[3]	SHARED_GPIO[7]	Serial Out (MISO)	Serial Out	Serial Out
SERIAL_IO[4]	SHARED_GPIO[8]	Serial In (MOSI)	Serial In	Serial In

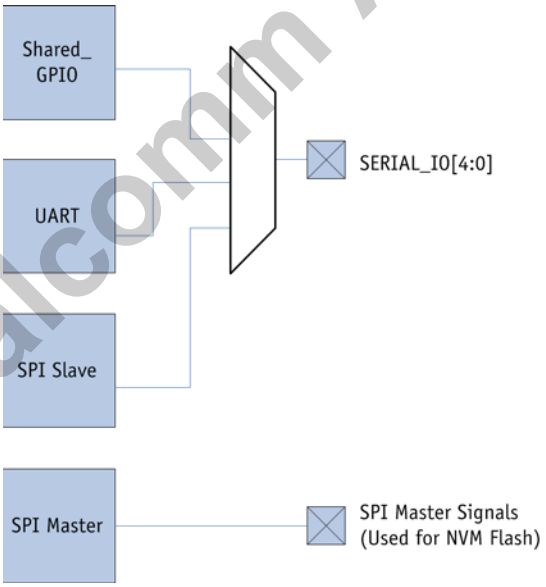


Figure 3-2 Serial I/O Options

3.2.3 QCA7000 SPI Slave Interface Command-Data Protocol

The QCA7000 SPI slave uses the standard 4-wire Motorola-SPI protocol plus an interrupt pin. Refer to Figure 3-3 below.

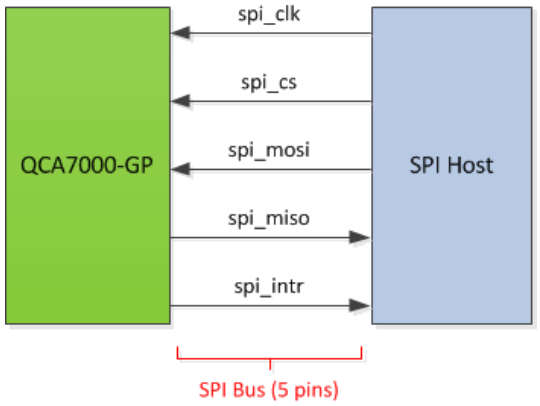


Figure 3-3 SPI Bus Diagram

Table 3-3 SPI Slave Signal Descriptions

Signal	Description
spi_clk	SPI slave input clock signal driven by the host during a bus transaction.
spi_cs	Bus qualifier to select the QCA7000 device in case the device is in a shared bus-arrangement with other peripherals. The SPI slave tri-states spi_miso when CS is de-asserted as well as ignore any data issued on spi_mosi (will not interpret spi frames).
spi_mosi	The master-out-slave-in signal. This is driven by the master to indicate a bus command and or data (write data).
spi_miso	The master-in-slave-out signal. This is return path of read data requested by the master.
spi_intr	QCA7000 pending interrupt signal.

The SPI host bus controller should support the following features:

- Minimum of 8-bit data framing (16-bit is recommended)
- Clock Phase and Polarity control (Requires SPI-Mode-3 clock Phase and Polarity)
- Level triggered interrupt for spi_intr line. This signal must be mask-able by software.

For optimal performance, the following features should be considered:

- 16 and 32-bit data framing (reduces inter-frame gaps for CS assertion)
- SPI-controller DMA support for large SPI data frame sequences

3.2.3.1 SPI Slave Bus Protocol

The SPI protocol uses a proprietary framing protocol and bus command set. The minimum bus data unit is 1 byte (8-bits) and framing is processed on byte boundaries. A bus transaction consists of a command phase followed by a data phase. The command phase operates in the direction of master-to-slave (bytes appear on spi_mosi line). The data phase occurs on either the spi_mosi line

(for writes, Master Out Slave In) or spi_miso line (for reads, Master In Slave Out) depending on the command.

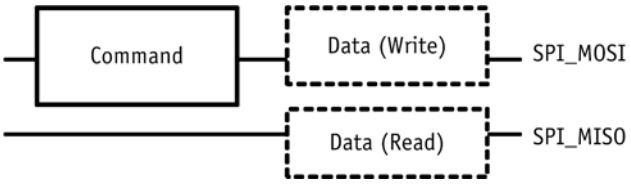


Figure 3-4 SPI Slave Framing Protocol

The bus command consists of 2 bytes followed by one or more bytes for the data phase of the transfer. Any sequence of bytes on the SPI bus can be optimized to the host controller's SPI data width capability (i.e. 8, 16 or 32-bits). Minimally, all SPI controllers support 8-bits, however controllers can get better bus utilization if they can support larger data frames. For example, the 2-byte command phase can be issued as either two 8-bit SPI data frames or a single 16-bit data frame. A 4-byte data sequence can be issued as 4 individual 8-bit SPI data frames or a single 32-bit data frame. The latter is more optimal on the bus as inter-frame gaps can be eliminated. The Atheros host reference software attempts to use SPI data frames optimal to the host controller's data framing capabilities. When 16- or 32-bit data frames are used, byte swapping may be necessary when the SPI host controller uses an external DMA controller (common on many designs). The QCA7000 SPI controller has internal byte swapping to accommodate such SPI host controller designs and can eliminate the overhead of software byte swapping.

SPI Slave Bus Access Types

The SPI protocol provides two bus access methods:

- SPI Register read/write
- SPI Buffer read/write

SPI Slave Register Read/Write

This method provides access to internal SPI registers. These registers typically are accessed 2 bytes at a time. The host software is responsible for insuring that no more than 1 external register access may be in progress.

SPI Slave Buffer Read/Write

The host communicates to the QCA7000 CPU through a FIFO in the SPI slave interface.

3.2.3.2 SPI Slave Commands

The SPI interface is a slave implementation and responds only to host-initiated bus commands. All SPI commands are 16-bits wide. A command includes a read/write bit, an external/internal address bit, follow by 14-bit of address. The most significant bit of a command is transmitted first on the spi_mosi pin.

Table 3-4 SPI Slave Commands Fields

Command Fields	Bit Position	Description
Read/Write Operation	15	0: Write Operation 1: Read Operation
Internal/External Addressing Mode	14	0: Buffer Mode 1: Register Address Mode
Internal or External Address	13:0	14 bit of register address

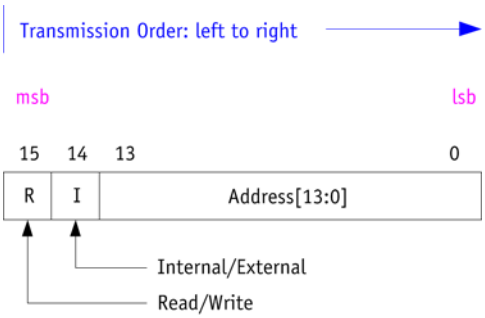


Figure 3-5 Command Diagram

Command Types

There are a total of four types of SPI operations. All of them are distinguished by the 16-bit SPI command.

SPI External accesses to core-logic registers are handled through a series of internal register operations (see paragraph 0). The SPI host accesses the buffers directly.

Transfer Format

It is important for the SPI host to choose the SPI clock polarity and phase format that matches the SPI slave. The SPI slave samples the incoming data (spi_mosi) on the rising edge and shifts out the outgoing data (spi_miso) on the falling edge of spi_clk pin.

The format that QCA7000 devices SPI is supporting corresponds to Mode 3 of the Motorola-SPI standard, in which the polarity and phase are both 'one'.

SPI Slave Internal Register Access

All SPI internal registers are 16-bits wide and they can only be accessed in 16-bit mode. The read or write data after the SPI command needs to be clock within a single spi_cs assertion window.

The SPI internal access comprises of a 16-bit command (command phase), followed by 16 clocks of data. For internal write, host will shift out 16-bit of data on spi_mosi signal, following the command phase. For internal read, SPI slave will shift out 16-bit of data on spi_miso signal, following the command phase.

During the data phase for INTERNAL read, the signal 'mosi' is a 'don't care' and is ignored by the slave controller.

3.2.3.3 SPI Slave Buffer Access

SPI buffer accesses are the primary mechanism to transfer packet data between the host and the target. In the transmit direction, a host may post as much data (packet writes) as there is SPI buffering available. In the receive direction, a host pulls as many data packets as indicated by the SPI receive buffer.

Table 3-5 SPI Slave Commands Types

Command Types		Read/ Write	Internal/ External	Address
1	SPI (Internal) Register Read	1	1	Any Range within the internal address space.
2	SPI (Internal) Register Write	0	1	Any Range within the internal address space.
3	SPI Buffer Read	1	0	Any Range. Address is ignored, since the read pops data from the buffer.
4	SPI Buffer Write	0	0	Any Range. Address is ignored, since the write pushes data to the buffer.

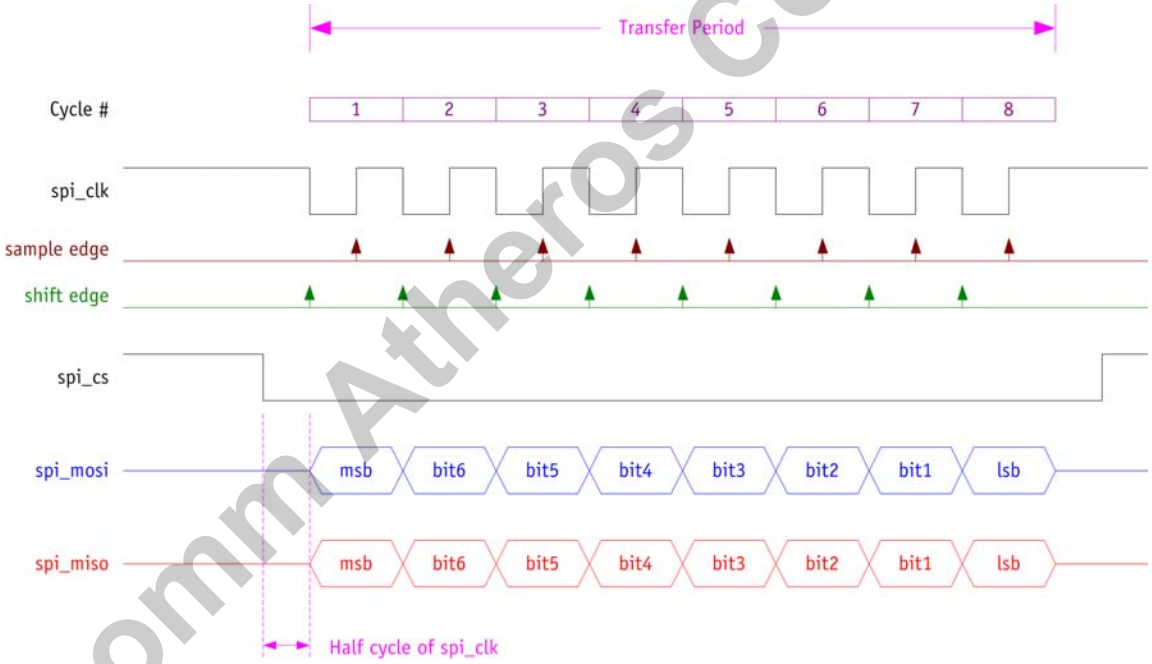


Figure 3-6 Transfer Format Diagram in 8-bit Mode

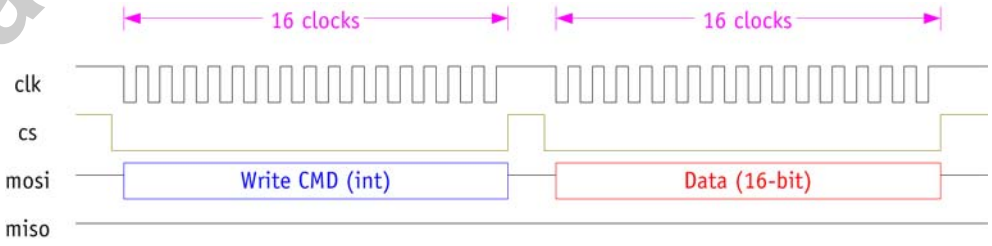


Figure 3-7 SPI INTERNAL Write

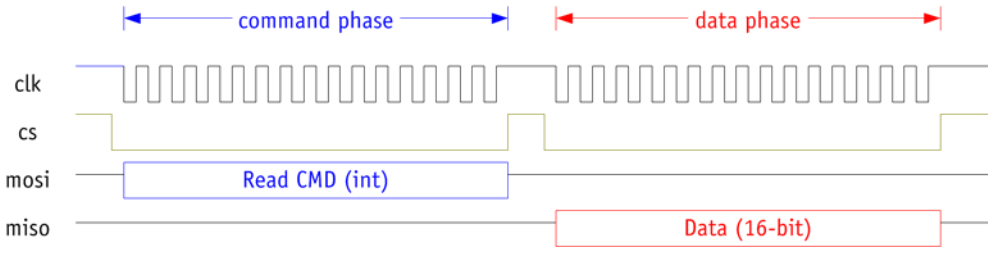


Figure 3-8 SPI INTERNAL Read

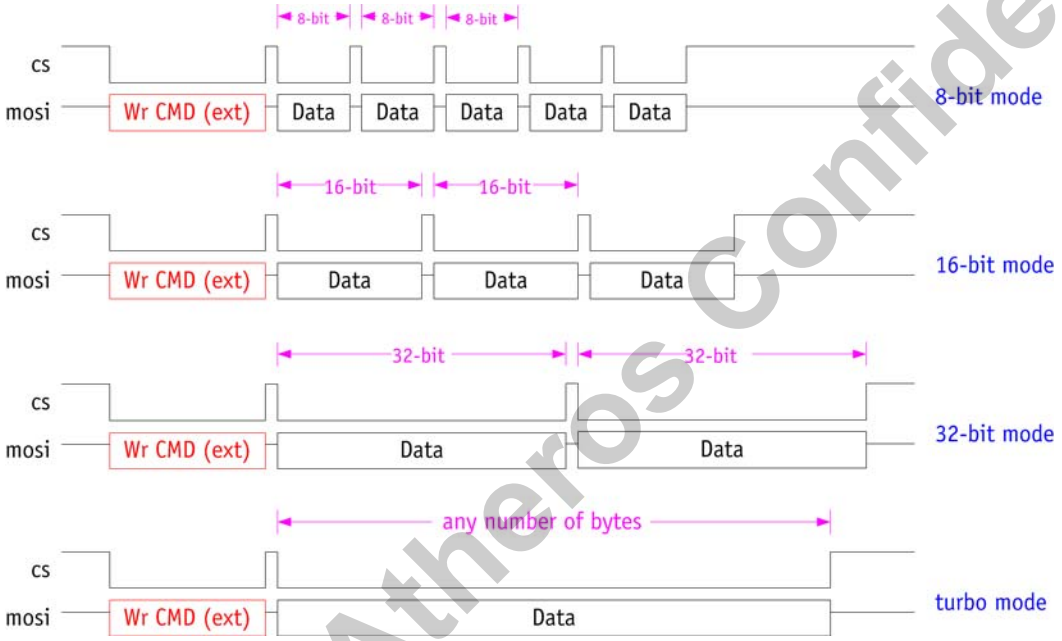


Figure 3-9 Transfer Mode Diagram

SPI Slave Transfer Modes

SPI supports 8-bit, 16-bit, 32-bit data frames for the data phase portion of the transfer. A special turbo mode is provided to ignore chip select toggles between frames. The entire data phase can be a continuous stream of data bits without chip-select gaps (if the host controller supports this mode).

SPI Slave Buffer Write

Packet data from the host is written to write buffer (FIFO). The write buffer has (typically) 3200 bytes of storage capacity allowing for rapid back-to-back writes of two-full network frames.

NOTE The host can read the WRBUF_SPC_AVA register on power up to determine the size of this buffer. It is recommended for the host to issue an internal access for the **WRBUF_SPC_AVA** register before issuing the buffer write command. If there is enough room for the next packet, the host should program the **BFR_SIZE** register with the upcoming packet size. The SPI host can then issue the buffer write command follow by the packet data.

Buffer Write Steps:

1. Internal read from **WRBUF_SPC_AVA** register.
2. Internal write to **BFR_SIZE** register.
3. Start buffer write command follow by the data phases.
4. If the host has another packet to send to QCA7000 devices, go back to step 1.

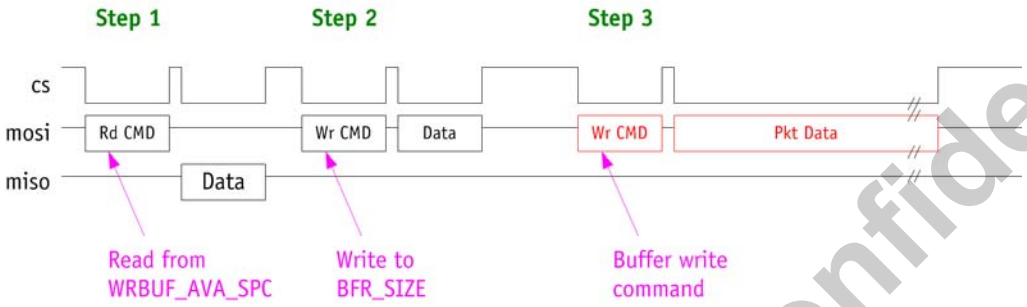


Figure 3-10 Buffer Write Steps Diagram

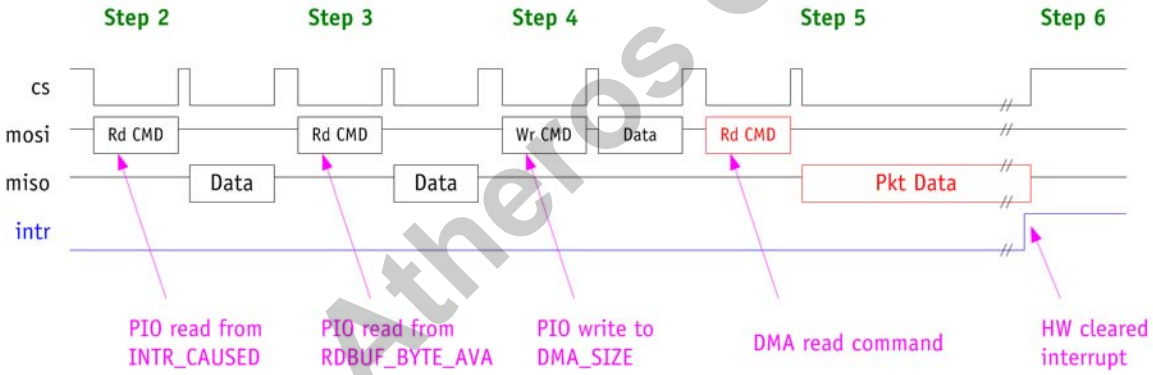


Figure 3-11 Buffer Read Steps Diagram

Write Buffer Error Interrupt

If the incoming write data overflows the buffer (**BFR_SIZE > WRBUF_SPC_AVA**), the SPI slave will drop the incoming data entirely. A "write buffer error" interrupt will be issued to the host. Host must insure that write data never overflows the buffer.

SPI Slave Buffer Read

The SPI controller pre-fetches data to the single 3200 byte read FIFO.

Once a full packet has been pre-fetched to the buffer, or the total number of bytes within the read buffer has exceeded **RDBUF_WATERMARK** register, a "packet available" interrupt will be issued to the SPI host.

Once the host has received the interrupt, it can issue an INTERNAL read from **INTR_CAUSE** register. If the interrupt is caused by the "packet available" interrupt, another INTERNAL read can be issued to **RDBUF_BYTE_AVA** register to determine the total number of data bytes held in the

read buffer. The final step to fetch the packet is to set the **BFR_SIZE** register with the intended read length. The host can then issue the buffer read command.

Buffer Read Steps:

1. Interrupt going from QCA7000 devices to SPI host.
2. INTERNAL read from **INTR_CAUSE** register.
3. INTERNAL read from **RDBUF_BYTE_AVA** register.
4. INTERNAL write to **BFR_SIZE** register.
5. Start buffer read command and start reading the data by de-asserting chip select pin.
6. The "packet available" will be cleared by HW at the end of the buffer read.

Packet Available Interrupt

The "packet available" interrupt can be processed in 2 ways. It is configured by the setting the “pkt_ava_intr_mode” of the ACT_CTRL register.

- When the “pkt_ava_intr_mode” bit is set to '0', the "packet available" interrupt is self cleared in the end of every data transfer. In this case, it is assumed that the host always issues register access between data transfers.
- When the “pkt_ava_intr_mode” bit is set to '1', the "packet available" interrupt needs to be manually cleared. The interrupt handling sequence is:
  - Host receives "packet available" interrupt
  - Host disable "packet available" interrupt
  - Host performs the buffer read operation
  - Host clears the "packet available interrupt
  - Host enables the "packet available" interrupt

Read Buffer Error Interrupt

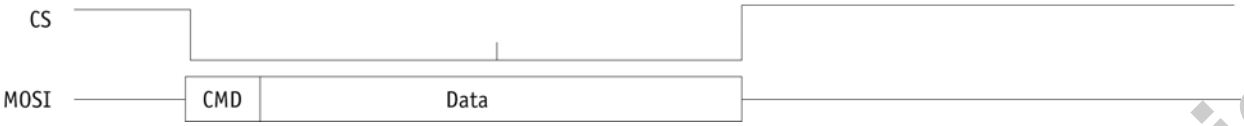
If the read operation is larger than the total available bytes within the read buffer (**BFR_SIZE > RDBUF_BYTE_AVA**), the read command will be ignored and spi slave will send out garbage onto spi_miso pin. At the same time, a "read buffer error" interrupt will be issued to the host.

3.2.3.4 Optional Mode of Operation

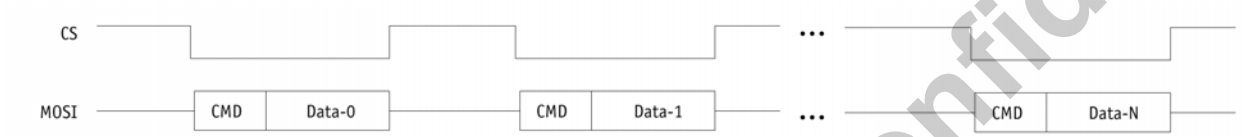
To give more flexibility in the SPI interface, a new interfaces mode is provided. The only difference in the Burst Mode is to enforce a rule that every falling edge of the spi_cs interface signal is a start of new command cycle. The selection of the operation mode is done by using the SPI-Salve Mode strapping pin described in “QCA7000 Power On Configuration Strap Values and Defaults” section of this document.

There are 2 sub mode of operations that is selected by the "multi_cs_enable" bit of ACT_CTRL register.

- When this bit is set to '0', the SPI host must complete a transaction within a signal sp_cs pulse.An example of buffer write show in the diagram below.The only difference for buffer read is that the Data is carried on the MISO instead of MOSI.



- When this bit is set to '1', the SPI host can optionally break a single transaction to multiple transfers carried by individual spi_cs pluses. An example buffer write diagram is shown below. The only difference for buffer read is that the Data-x is carried on the MISO instead of MOSI.



3.2.3.5 Byte Swapping

Some SPI bus controllers may swap bytes when 16-bit or 32-bit data frames are DMA'ed from host memory. This only affects data frames that are DMA'd from host memory to/from the QCA7000. SPI external core-logic register accesses do not require swapping as they typically do not use host DMA for such small transfers. QCA7000 data however can be full network frames of 1500+ bytes and may use the host's SPI DMA controller to optimize the transfer.

To avoid host software from having to correct the byte swapping, the AR6K SPI controller has a byte swapping mode feature programmed using **SPI_CONFIG**.*swap* bit. The SPI controller must also be programmed for the size of the byte swap either 2 bytes (16-bit) or 4 bytes (32-bit). This is controlled by a single **SPI_CONFIG**.*16bit_mode*. When 0, the swap is a 4-byte swap when 1, the swap occurs on 2 byte pairs. The host must only issue data frames whose transfer length align to the swap size of 2 or 4 bytes.

The following diagrams illustrate which bytes get received or sent first in the case of byte swapping. The diagrams only show the DMA write transfer, in which the incoming data byes are swapped before going into the write buffer. For DMA read transfer (not being shown in diagram), outgoing data bytes are swapped similarly coming out from the read buffer.

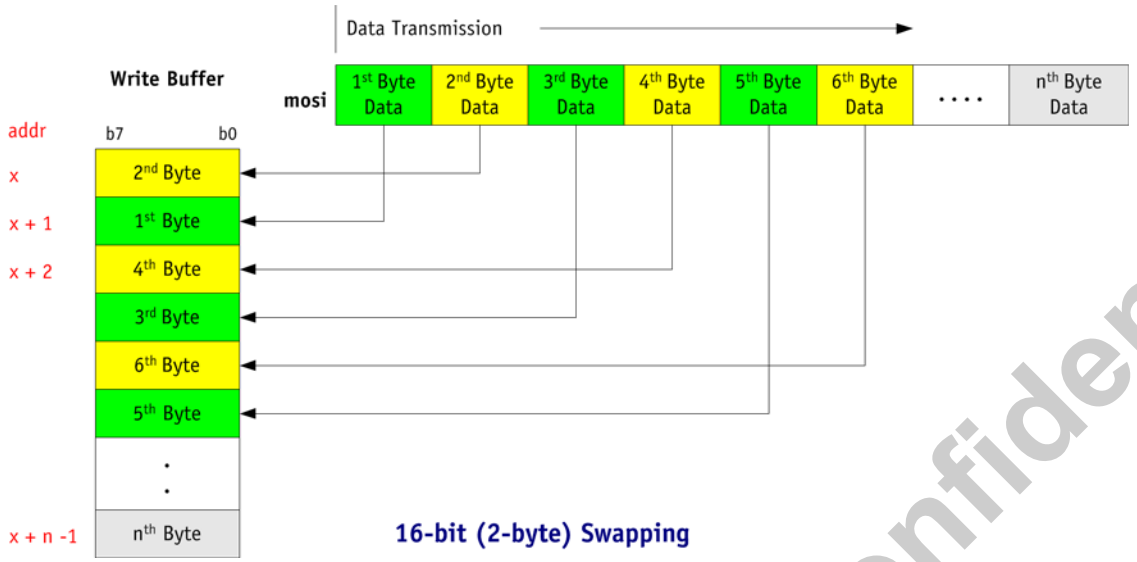


Figure 3-12 SPI Slave16-bit Byte Swapping

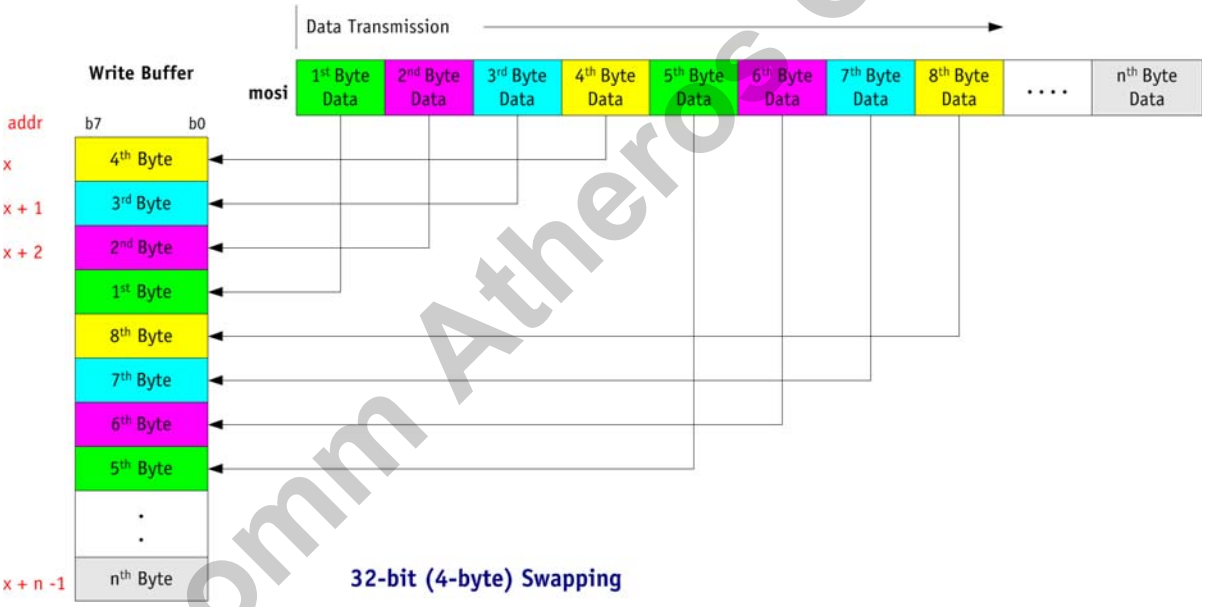


Figure 3-13 SPI Slave 32-bit Byte Swapping

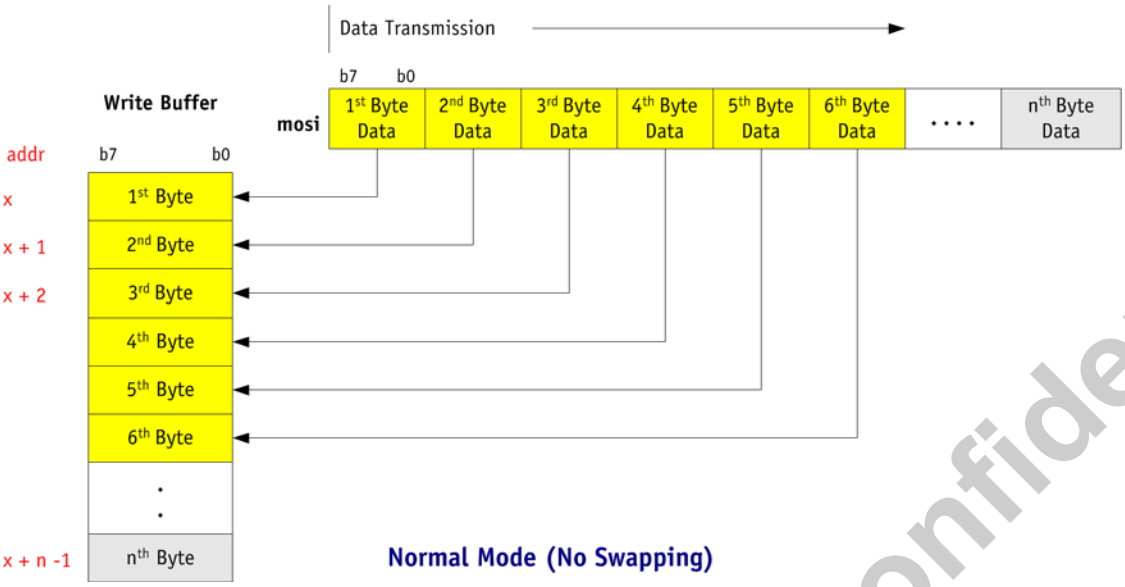


Figure 3-14 SPI Slave Normal Mode (No Swapping)

3.2.3.6 Out of Sync Recovery

This section describes the recovery mechanism for the unlikely event that the SPI host and QCA7000 gets out-of-sync, When the SPI interface is out-of-sync, QCA7000 will be unable to decode the host command correctly and data could be corrupted. The functions related to the recovery mechanism is

Possible Causes of Out-of-Sync

- The value returned from reading the SIGNATURE register is not 0xAA55: The SIGNATURE register can be read by the SPI host to detect out-of-sync condition. The SIGNATURE register contains a fixed value of 0xAA55. If, the SPI interface is out-of-sync.
- QCA7000 resets itself: When this happens the QCA7000 will assert "'cpu_on" interrupt.
- Host resets itself.

Host Resets QCA7000

When an out-of-sync condition happens, the SPI host needs to reset QCA7000 in order to sync up and to go back to the normal operation.

- Legacy Mode: When out-of-sync happens in this mode, the QCA7000 may not be able to decode the command correctly. In order to reset QCA7000, the SPI Host needs use a GPIO pin to control the POR pin of QCA7000. Thus, some board level design is needed to support this operation.
- Burst Mode: In this mode, every falling edge of spi_cs signal is the start of a new command cycle. Thus, the QCA7000 can always process the command from the host correctly. To reset QCA7000, the SPI host can issue register write to the bit[6] of SPI-CONFIG register.SPI Slave Registers

The following registers can be accessed by the SPI host at any point in time.

Table 3-6 SPI Slave Registers

Register Name	Address [13:0]
BFR_SIZE	0x0100
WRBUF_SPC_AVA	0x0200
RDBUF_BYTE_AVA	0x0300
SPI_CONFIG	0x0400
SPI_STATUS	0x0500
INTR_CAUSE	0x0C00
INTR_ENABLE	0x0D00
RDBUF_WATERMARK	0x1200
WRBUF_WATERMARK	0x1300
SIGNATURE	0x1A00
ACT_CTRL	0x1B00

Buffer Size register (BFR_SIZE)

Address: 0x0100

This register holds the buffer transfer size in terms of bytes.

Field Name	Bits	Access	Reset Value	Description
	15:12		0x0	Reserved
bfr_size	11:0	RW	0x1	Indicates buffer transfer size (in bytes). Programming of zero is not allowed.

Write Buffer Space Available register (WRBUF_SPC_AVA)

Address: 0x0200

This register holds the total number of empty space within the write buffer in terms of bytes.

Field Name	Bits	Access	Reset Value	Description
	15:12		0x0	Reserved
space_ava	11:0	RO	0x0	Indicates write buffer empty space (in bytes).

Read Buffer Byte Available register (RDBUF_BYTE_AVA)

Address: 0x0300

This register holds the total number of data bytes within the read buffer. Each write to the SPI slave consumes an additional 4 bytes of write buffer space. For example, if space_ava is 100 bytes, writing 70 bytes will actually consume 74 bytes leaving 26 bytes available.

Field Name	Bits	Access	Reset Value	Description
	15:12		0x0	Reserved
byte_ava	11:0	RO	0x0	Indicates the total number of data bytes within read buffer.

SPI Config register (SPI_CONFIG)

Address: 0x0400

This register is used to configure the SPI core.

Field Name	Bits	Access	Reset Value	Description
	15:11		0x0	Reserved
	10:9		0x0	Reserved
	8		0x0	Reserved
spi_io_enable	7	RW	0x0	This bit should be reset to 0 after power on reset. The SPI host can program this bit to always enable the QCA7000 to drive the spi_miso pin. When this bit is 0, the mido pin is enabled only when spi_cs is low. When spi_miso pin is not enabled, it is tristated.
soc_core_reset	6	RW	0x0	Write 1 to this bit will reset the whole QCA7000 chip.
	5:3		0x0	Reserved
swap	2	RW	0x0	0: No swapping 1: Byte swap
16bit_mode	1	RW	0x0	If swap bit is zero, this bit has no effect. If swap bit is asserted, and: 16bit_mode = 1: swap every 2 bytes 16bit_mode = 0: swap every 4 bytes
	0		0x0	Reserved

SPI Status register (SPI_STATUS)

Address: 0x0500

This register indicates the current status of the SPI core.

Field Name	Bits	Access	Reset Value	Description
	15:5		0x0	Reserved
wrbuf_error	4	RW, W1C	0x0	Indicates an error has occurred while accessing the write buffer. Write one will clear this bit. This is mainly used for debug. Note: edge triggered source.
rdbuf_error	3	RW, W1C	0x0	Indicates an error has occurred while accessing the read buffer. Write one will clear this bit. This is mainly used for debug. Note: edge triggered source.
	2:1		0x0	Reserved

Interrupt Cause register (INTR_CAUSE)

Address: 0x0C00

This register holds all the pending SPI interrupts. All interrupt bits can be cleared by programming a value of one to the corresponding interrupt bit.

1: interrupt is pending
0: no interrupt

Field Name	Bits	Access	Reset Value	Description
	15:11		0x0	Reserved
wrbuf_below_watermark	10	RW, W1C	0x0	Indicates the number of data bytes within the write buffer is below the water mark level. Note: level triggered source.
	9:7		0x0	Reserved
cpu_on	6	RW, W1C	0x0	Cpu has just been awakened. Write one will clear the interrupt. Write zero has no effect. Note: edge triggered source.
	5:3		0x0	Reserved
wrbuf_error	2	RW, W1C	0x0	Indicates an error has occurred while accessing the write buffer. It basically means that the host is trying to send a write which is larger than the available room within the write buffer. Write one will clear the interrupt. Write zero has no effect. Note: edge triggered source.
rdbuf_error	1	RW, W1C	0x0	Indicates an error has occurred while accessing the read buffer. It means that the host is sending a read in which the size is larger the total available bytes within the read buffer. Write one will clear the interrupt. Write zero has no effect. Note: edge triggered source.
packet_available	0	RW, W1C	0x0	Read buffer has at least one packet or the total number of available bytes has reached or exceeded the read buffer watermark. At the end of a read, this interrupt will be cleared by HW. Write one will clear the interrupt. Write zero has no effect. Note: level triggered source.

Interrupt Enable register (INTR_ENABLE)

Address: 0x0D00

This register is used to mask/enable interrupts going to the SPI host.

1: interrupt is enabled
0: interrupt is disabled

Field Name	Bits	Access	Reset Value	Description
	15:11		0x0	Reserved
wrbuf_below_watermark	10	RW	0x0	Enable the write buffer below watermark interrupt. Note: level triggered source.
	9-7		0x0	Reserved
cpu_on	6	RW	0x1	Enable the cpu on interrupt. Note: edge triggered source.
	5		0x0	Reserved
	4		0x0	Reserved
	3		0x0	Reserved
wrbuf_error	2	RW	0x0	Enable the write buffer error interrupt. Note: edge triggered source.
rdbuf_error	1	RW	0x0	Enable the read buffer error interrupt. Note: edge triggered source.
packet_available	0	RW	0x0	Enable the packet available interrupt. Note: level triggered source.

Read Buffer Water Mark register (RDBUF_WATERMARK)

Address: 0x1200

This register is holds the water mark value for the read buffer.

Field Name	Bits	Access	Reset Value	Description
	15:12		0x0	Reserved
watermark	11:0	RW	0x1	Read buffer watermark. Zero is not allowed.

Write Buffer Water Mark register (WRBUF_WATERMARK)

Address: 0x1300

This register is holds the water mark value for the write buffer.

Field Name	Bits	Access	Reset Value	Description
	15:11		0x0	Reserved
watermark	10:0	RW	0x40	Write buffer watermark. Zero is not allowed.

Signature register (SIGNATURE)

Address: 0x1A00

This register is holds a fixed signature value that is used for Host to read to confirm the SPI interface between the host and the QCA7000 are in sync and the QCA7000 can process Host's requests/commands correctly.

Field Name	Bits	Access	Reset Value	Description
signature	15:0	R	0xAA55	A fixed signature pattern.

Action Control register (ACT_CTRL)

Address: 0x1B00

This register is used to set the QCA7000 into different operation modes.

Field Name	Bits	Access	Reset Value	Description
	15:2		0x0	Reserved
multi_cs_enable	1	RW	0x1	** only used when the SPI Slave interface is operating in the Burst Mode (ie. SPI Slave Strap is tied to '1') 0: the host must complete a command/data transaction within a signal sp_cs pulse. 1: the host can complete a command/data transaction with multiple sp_cs pulse.
pkt_ava_intr_mode	0	RW	0x1	0: packet available interrupt is self cleared (This is assume that host issues at least 1 register r/w between DMA/data transaction). 1: packet available interrupt needs to be manually cleared.

3.2.4 GPIO

The QCA7000 supports a maximum of 4 General Purpose I/O signals. Each of these can be individually programmed as an input or output; outputs can be further programmed for different drive-strength for different applications. Up to 2 of these GPIO signals (depending upon configuration) can be used to trigger interrupts to the main ARM processor. Interrupts can be any of active high or low, or positive/negative edge triggered.

In addition to the normal functions associated with the GPIO pins, there are also additional debug functions associated with the GPIO I/O pads. These functions are shown within Table 3-7; the details on how to enter into the various debug modes goes beyond the details found in this document.

Table 3-7 GPIO Debug MUX Options

Pin	Normal Function	Clock Observability #1	Clock Observability #2
GPIO0	GPIO[0]	25 MHz Oscillator: Positive	25 MHz Oscillator: Positive
GPIO1	GPIO[1]	25 MHz Oscillator: Negative	25 MHz Oscillator: Negative
GPIO2	GPIO[2]	75 MHz PLL: Positive	62.5 MHz PLL: Positive
GPIO3	GPIO[3]	75 MHz PLL: Negative	62.5 MHz PLL: Negative

4 Functional Description

4.1 Overview

The QCA7000 HomePlug Green PHY integrated circuit is a PLC MAC/PHY Transceiver with serial data I/O. The device is designed to bridge lower data rate multi-stream PLC based Ethernet content from a HomePlug, HomePlug AV Powerline network or Smart Grid network to products in the home or office environment.

The Powerline communications (PLC) specific MAC manages network admission and service flows to maximize the quality of service (QoS) over the HomePlug network.

The single QCA7000 HPGP 10 Mbps IC contains many of the functions previously found in higher data rate Atheros two chip PLC system solutions. The QCA7000 does not support an Ethernet I/O port.

4.2 QCA7000 Maximum Throughput Data Rate

Maximum data rate is approximately 5.4 Mbps UDP in SPI Slave mode.

4.2.1 UART Baud Rates Set Serial Interface Data Rate

QCA7000 Firmware Release v1.0.0.719-05-20120601-FINAL (RC38) and later versions provide the baud rates shown in Table 4-1. Firmware prior to this release should not be used.

Table 4-1 UART Mode Baud Rate Selection

Nominal RS232 Rates	Default Divisor	Actual Baud Rates	Baud Rate Error(%)
110	14204	110.0042	0.0038
300	5208	300.0192	0.0064
600	2604	600.0384	0.0064
1200	1302	1200.0770	0.0064
2400	651	2400.1540	0.0064
4800	326	4792.945	0.1470
9600	163	9585.89	0.1470
14400	108	14467.5900	0.4694
19200	81	19290.1200	0.4694
38400	41	38109.76	0.7558
57600	27	57870.3700	0.4694
115200	14	111607.1429	3.1188

Please refer to the *Qualcomm Atheros QCA7000 AVitar User's Guide* for adjusting the baud rates

4.3 Power Management

4.3.1 Power Domains

To address the requirement that devices consume less power especially when they are not actively being used, the QCA7000 hardware and firmware supports power management functions. Power usage will be controlled using a combination of power gating and clock gating. The system contains two power islands, the Always Powered Island, and the Power Gated Island.

- Always Powered: 25 MHz Osc to PMUAlways On
- Always Powered, Low Power Mode: All Clocks Stopped in Sleep Mode
- Power Gated, Clock Gated: All Clocks stopped in Sleep Mode

4.3.2 Power Management Unit

Through a combination of hardware and software, four states of power consumption are supported shown in Table 4-2.

Table 4-2 Supported Power States

Power Mode	Functionality	Wake-up to Active
Deep Sleep (Optimized for Power Saving)	■ Lowest power consumption □ Utilizes internal power gating ■ Not capable of processing Powerline activity ■ Not capable of receiving host wake commands on SPI or UART ■ Not capable of monitoring link status ■ Not capable of supporting 802.3.az low power idle/active transitions ■ Transition time to active is a function of the warm boot time after the detection of a wake event	■ Internal timer ■ External GPIO input signal transition

Sleep (Optimized for Response Time)	■ Low power consumption
	  □ All blocks powered, utilizes clock gating
	  □ HomePlug PHY off, HomePlug MAC on
	■ Not capable of processing Powerline activity
	■ Capable of receiving host wake commands
	■ Transition time to active is a function of the warm boot time after the detection of a wake event
	■ > 75% power savings over the Active state
		■ Internal timers
		■ External GPIO input signal transition

Active	■ Highest power consumption under one of three conditions transmit, receive or idle ■ Capable for full operation at maximum bandwidth available based upon the environment ■ Capable of dropping to lower power-state based upon traffic patterns or host messages ■ Transition time to DeepSleep or Sleep Power Mode within 1 s of sleep command or event	

To implement the power states shown in Table 4-2, the QCA7000 includes four Power Management states. Sleep and deep sleep are low power modes to reduce the chipset power consumption significantly from more active power consumption states.

In the sleep state, all QCA7000 logic except the power management unit (PMU), the SRAM containing the primary CPU execution image, some Analog IP and a few I/O cells are put into an inactive but powered state. Software and timers or external events from the GPIO interface are used to wake-up the device.

In the deep sleep state, all QCA7000 logic except the power management unit (PMU), the SRAM containing the primary CPU execution image, some Analog IP and a few I/O cells are powered off by the PMU. Timers or GPIO are used to wake-up the device.

4.4 Boot Options

The QCA7000 contains an embedded ARM926 processor that requires Firmware (FW) loaded from and external device or host processor source. FW must be loaded to enable data transfer/processing to and from the Powerline. As this firmware does not reside on-chip, the QCA7000 boot sequence requires the ability to download configuration and code from an external device like a Non Volatile Memory NVM (flash) device using the Master SPI bus or the SPI Slave Bus Port from a host processor.

Straps on the QCA7000 specify which method is used to access FW. All applications of the QCA7000 can boot from flash using the SPI Master Port if NVM is present. Reading NVM Flash (connected through pins SPI_CLK, SPI_DO, SPI_DI, and SPI_CS_L) loads FW immediately after RESET_L goes high. The QCA7000 can boot from an external host device over the SPI Slave port interface using a sequence of low level software instructions residing in the QCA7000 ROM. These are MME command packets.

Once FW is loaded and running in the QCA7000 from any source it begins communicating over any and all I/O ports including the Powerline. Powerline commands can program or re-program the local NVM device if available. There are several methods then of updating FW using a sequence of simple MME packets. To boot the chip, an applet is first downloaded to configure the internal hardware. Next, the chip downloads the firmware and then hands CPU control over to this program to start the Powerline network. At this point the Powerline network has full control of the QCA7000. In the manufacturing environment preprogram the NVM device before assembly.

The QCA7000 supports SPI flash NVM devices supporting the ST SPI-flash command-set. See Table 4-3. for qualified NVM memory devices

Table 4-3 QCA7000 FLASH Recommended Devices

Vendor	Part Number	Speed Grade	Memory Size	Comments
Atmel	AT26DF161-SU	100 MHz	16-Mbits	[1]Not for new designs
Atmel	AT26DF161A-SU	70 MHz	16-Mbits	[1]
Numonyx	M25P80-VMW6TP	75 MHz	8-Mbits	[1]
Numonyx	M25P16-VMW6TP	75 MHz	16-Mbits	[1]
Macronix	MX25L8005	70 MHz	8-Mbits	[1]
Macronix	MX25L1605	86 MHz	16-Mbits	[1]

1. Verified for use with the INT6400

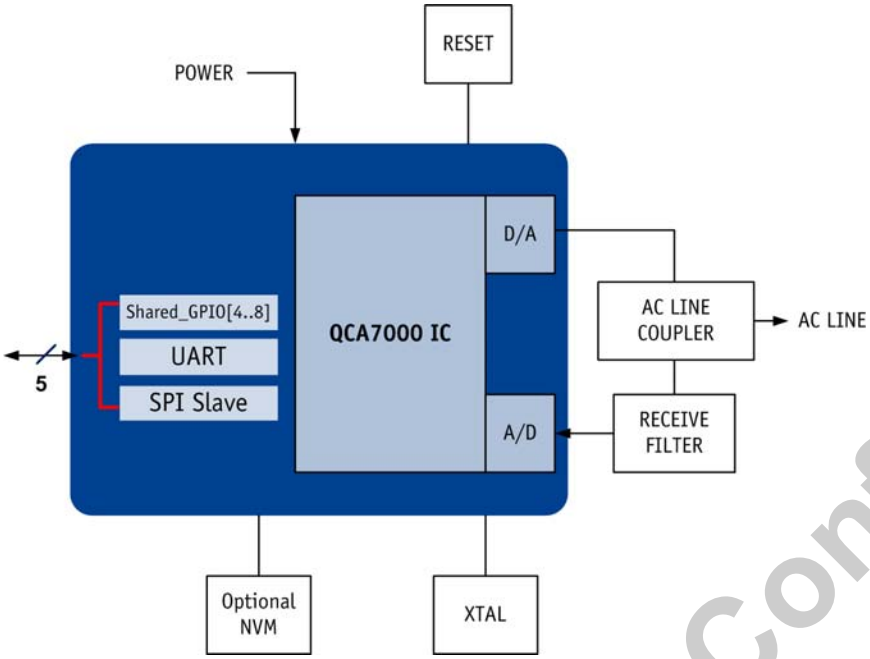


Figure 4-1 QCA7000 Powerline Station

4.5 Serial Interfaces

The QCA7000 includes multiple serial interfaces:

- UART
- GPIO
- SPI Slave
- SPI Master (SPI) for NVM -flash

The UART supports four signal pins for various applications: TX Data, RX Data, Request to Send (RTS) and Clear to Send (CTS). The use of RTS and CTS is optional. The UART does not support any Infra-red Data Association (IrDA) functionality.

The General Purpose Input/Output (GPIO) is available for use for discrete sensing and control.

The SPI slave port shares its I/O with the UART, and Shared_GPIOs. Their operation is mutually exclusive.

The Serial Peripheral Interface (SPI) master port has one chip select, just for boot from NVM-flash. The SPI master port supports the SPI bus which is always used for boot from NVM-Flash.

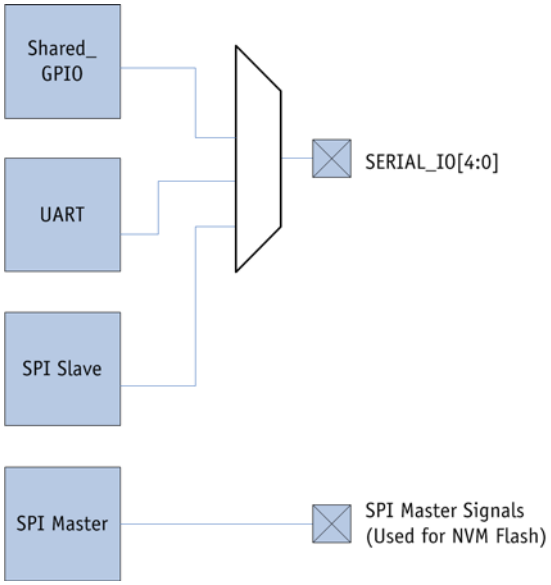


Figure 4-2 Serial I/O Options

CPU oversees operation of the integrated HPGP PHY via an interface that carries control/status and transmits and receives data packets.

General-purpose I/O pins are available to drive light emitting diodes (LED) to indicate status, user reset, and network-attach events. A dedicated sub-system is responsible for power-management functions on the QCA7000. Two on-board phase locked loops (PLL) and a built-in crystal oscillator cell are used to generate the required system clocks from a single external 25 MHz crystal. Various loop-back modes support manufacturing test.

Table 4-4 Peripheral Pin-out Options

Pin	Symbol	Configuration		
		SPI Slave	UART	Shared_GPIO
67	SPI_CLK	SPI Master Clock Output		
66	SPI_DO	SPI Master Data Output		
3	SPI_DI	SPI Master Data Input		
65	SPI_CS_L	SPI Master Chip Select #1		
20	SERIAL_IO[0]	SPI Slave Interrupt	Shared_GPIO[4]	Shared_GPIO[4]
19	SERIAL_IO[1]	SPI Slave Clock	RTS/SERIAL_IO_0	Shared_GPIO[5]
16	SERIAL_IO[2]	SPI Slave CS	CTS SERIAL_IO_1/	Shared_GPIO[6]
15	SERIAL_IO[3]	SPI Slave TXD	TXD/SERIAL_O_2	Shared_GPIO[7]
14	SERIAL_IO[4]	SPI Slave RXD	RXD/SERIAL_I_3	Shared_GPIO[8]

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5-1 summarizes the absolute maximum ratings and Table 5-2 lists the recommended operating conditions for the QCA7000.

Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

Table 5-1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
Electrical				
VCORE	Core Supply Voltage	-0.3	1.32	V
VPLL_1	PLL Analog Power	-0.3	1.32	V
VDDIO	I/O Supply Voltage	-0.3	3.63	V
VPLL_3	Analog PLL Supply Voltage	-0.3	3.63	V
AVDD_1	Analog Power 1 V	-0.3	1.32	V
AVDD_3	Analog Power 3 V	-0.3	3.63	V
XTALx, PLLx	PLL lines	Vss-0.3	Vpll_1+0.3	V
ADCx, DACx	Analog lines	Vss-0.3	AVDD_1+0.3	V
Digital	All other digital lines	Vss-0.3	Vddio+0.3	V
T_{store}	Storage Temperature	-40	+150	ºC
T_j	Junction Temperature	—	+125	ºC
ESD Immunity	Human Body Model	—	2.0	kV

5.2 Recommended Operating Conditions

Table 5-2 Recommended Operating Conditions [1]

Symbol	Parameter	Min	Typ	Max	Units
VCORE	Core Supply Voltage	1.14	1.2	1.26	V
VDDIO	QCA7000 I/O Supply Voltage	3.13	3.3	3.46	V
AVDD_1	Analog Power 1.2 V	1.14	1.2	1.26	V
AVDD_3	Analog Power 3.3 V	3.13	3.3	3.46	V
Tcase[2]	Top of Case Temperature (Standard temperature range)	0	—	105	ºC
	Top of Case Temperature (Industrial temperature range)	-40	—	110	ºC
Psi_{JT}[2]	Thermal Parameter	—	2.8	—	ºC/W

1. Power supply voltages may be applied or removed in any sequence during power up or power down.
2. For the QCA7000 8x8 mm 68-Pin QFN package the IC will operate at its respective Tcase temperature range provided required PCB footprint and thermal design layout is used. See Qualcomm Atheros reference design board layout.

5.3 QCA7000 Power Supply Requirements

Table 5-3 QCA7000 Typical Power Supply Requirements[1, 2]

Symbol	Parameter	Supply Voltage (V)	Transmit Mode Current (mA)	Receive Mode Current (mA)
VCORE	QCA7000 Core Supply Voltage (Standard temperature range)	1.2	100	130
	QCA7000 Core Supply Voltage (Industrial temperature range)		138	135
VDDIO	Total for VDDIO, VDDIO_E and VDDIO_D (Standard temperature range)	3.3	215	150
	Total for VDDIO, VDDIO_E and VDDIO_D (Industrial temperature range)		243	162

1. Data in Table 5-3 is typical. Process variation and operating temperature may increase current draw. Ensure the power supply design has sufficient margin. Refer to the PL16 Embedded Evaluation PCB power supply design. ASSUMPTION: QCA7000 PL16 Embedded Evaluation PCB 6005311.
2. Tcase condition = +25ºC and power supply voltages at nominal.

Table 5-4 QCA7000 Typical Total IC Power[1, 2]

Device	Transmit Mode Power (mW)	Receive Mode Power (mW)	Sleep Mode Power (mW)
QCA7000 (Standard temperature range)	830	655	100
QCA7000 (Industrial temperature range)	969	696	

1. Data in Table 5-4 is typical. Process variation and operating temperature may increase power consumption. Ensure the power supply design has sufficient margin. Refer to the PL16 Embedded Evaluation PCB power supply design.
2. Tcase condition = +25ºC and power supply voltages at nominal.

5.4 DC Switching Thresholds

Table 5-5 DC Switching Thresholds

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IL}	Low-level input voltage		—	0.8	V
V_{IH}	High-level input voltage		2.0	—	V
V_{OL}	Low-level output voltage	I_{OL}= 4 mA, 12 mA[1]	—	0.4	V
V_{OH}	High-level output voltage	I_{OH} = -4 mA, -12 mA[2]	2.4	—	V
XTALOUT V_{IL}	XTALOUT low-level input voltage		--	0.2	V
XTALOUT V_{IH}	XTALOUT high-level input voltage		0.9	--	V
I_{IL}	Low-level input current	V_I = Gnd	-1	—	µA
I_{IH}	High-level input current	V_I = Vdd	—	1	µA
I_{OZ}	High-impedance output current	Gnd ≤ VI ≥ Vdd	-1	+1	µA

1. IOL = 12 mA for all GPIOs
   IOL = 4 mA for all other interfaces
2. IOH = -12 mA for all GPIOs.
   IOH = -4 mA for all other interfaces

5.5 Crystal Specifications

Table 5-6 Crystal Specifications

Parameters	Values	
Frequency	25 MHz	
Frequency Tolerance @ +25°C	±10 ppm Max.	
Frequency Stability: 0°C to +70°C	±10 ppm Max.	
Crystal Cut	AT Strip	
Effective Series Resistance	15 Ω Typ., 50 Ω Max.	
Shunt Capacitance	7 pF Max.	
Mode of Operation	Fundamental	
Aging	±3 ppm/year Max.	
Storage Temperature	-40°C to +85°C	
Operating Temperature	0°C to +70°C	
Package Type	HC-49/U	SMD
Recommended Parts	ECS-250-1B-4X-F-C	7M25000013
Load Capacitance (CL)	18 pF	10 pF
Recommended Drive Level	100 µW Typ.	100 µW Typ., 200 µW Max.

6 Timing Constraints

6.1 System Clock and Reset Timing

6.1.1 QCA7000 Crystal Oscillator

The QCA7000 IC requires a 25 MHz Clock Signal for a master time base. All timing is derived from this signal. This signal is normally derived from a 25 MHz crystal attached to the XTAL_IN and XTAL_OUT pins 37 and 38 respectively. See schematic 60005311 for details. The two trim capacitors (C185 and C286) are nominally 4.7 pF but these values are dependent on part spacing and layout details that vary depending on board design. The designer must measure the master oscillator frequency and adjust these two trim capacitors to deliver the correct frequency for any new board design. Accuracy of the master oscillator is essential to correct operation of all PLC designs. See Section 6.1.2 for accuracy details. An external 25 MHz Clock Signal can be used rather than the integrated oscillator. Refer to the *PL16 Hardware Reference Guide* for External Oscillator configurations.

Table 6-1 System Clock and Reset Timing Specifications

Parameter		Min	Typ	Max	Units
25.0 MHz Oscillator					
t_{CLKp}	OSCIN Period	40.000 - 23 ppm	—	40.000 + 23 ppm	ns
Tr/Tf	Rise/Fall Time (20% to 80%)	—	—	5	ns
Duty_CLK	Duty Cycle for OSIN	45	50	55	%
tosc	Oscillator Start-Up Time	—	0.75	—	ms
Internal Reset					
t_{RSTa}[1]	Internal Reset Time	4000			Clock Cycles
GPIO Configuration and Reset Timing					
t_{GPIO_SETUP}	GPIO Config. SETUP	2000	—	—	ns
t_{GPIO_HOLD}	GPIO Config. HOLD	1000	—	—	ns
t_{RSTa}	RESET_L	—	—	—	µs

1. Internal reset is active after power is applied and goes inactive after 4000 clock cycles if both DVDD and VDD voltages meet minimum specifications. See marker (C) in the timing see Figure 6-1.

6.1.2 Master Time Base Accuracy

The accuracy of this signal must meet the HomePlug standard. Initial accuracy as the QCA7000 is powered-on must be ±10 ppm at specified operating voltage. Additionally the 25 MHz signal may drift an additional ±10 ppm over the operating temperature range. In addition the frequency may vary ±3 ppm per year to account for aging of the crystal. See Table 5-6 and Table 6-1 for details.

6.1.3 External Clock Input

A nominal 1.1 Vpp clock signal may be applied to XTAL_OUT (Pin 38). The XTAL_IN (Pin 37) must be pulled to ground through a zero ohm resistor for proper QCA7000 circuit bias and to turn off the internal oscillator circuit. See schematic 60005311 for details and always use the latest Qualcomm Atheros documents for component values and circuit arrangements. OSCIN is a critical signal. To achieve optimum system performance there must be no deviation from the recommend circuit. The accuracy of the external oscillator must be within ±25 ppm of 25 MHz over time and temperature.

Table 6-2 External Oscillator Input Timing Requirements

Symbol	Parameter	Min	Typ	Max	Units
T_{LOW}	Active Low time	18	1/(2F)	1/F-T_{LOW}	ns
T_{HIGH}	Active High Time	18	1/(2F)	1/F-T_{HIGH}	ns
T_R	Rise time	—	—	5	ns
T_F	Fall time	—	—	5	ns

Two on-board PLLs use the Master Time Base signal to generate the required internal QCA7000 system clocks. See the *PL16 Hardware Reference Guide* for details on accurately measuring the QCA7000 25 MHz Clock Signal.

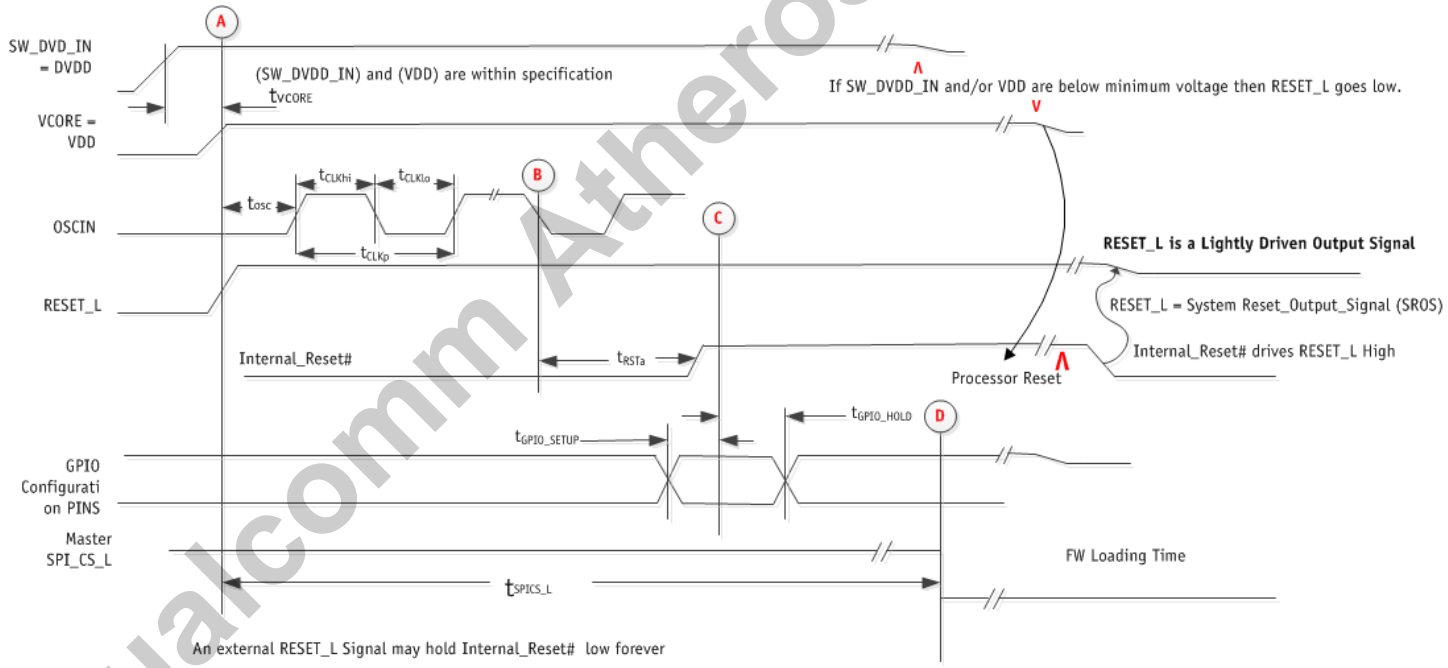


Figure 6-1 System Clock and Reset Timing

The RESET_L pin is an input signal and a lightly driven output. There is no need to drive the RESET_L pin in most standalone applications.

6.2 Zero Crossing Detector Timing

Zero Crossing is internal to the QCA7000 IC.

Table 6-3 Zero Crossing Detector Timing Specifications

Symbol	Parameter	Min	Typ	Max	Units
T_{LOW}	Active Low time	400	1/(2F)	1/F-T_{LOW}	µs
T_{HIGH}	Active High Time	400	1/(2F)	1/F-T_{HIGH}	µs
T_R	Rise time	1	—	1,000	µs
T_F	Fall time	1	—	1,000	µs
T_{OFFSET}	Offset from zero crossing	0	—	1/F	
F_{60}	60 Hz frequency tolerance	1	[1]	[1]	%
F_{50}	50 Hz frequency tolerance	[1]	[1]	[1]	%

1. Frequency accuracy determination is a firmware function. Consult the applicable firmware technical reference manual for this information.

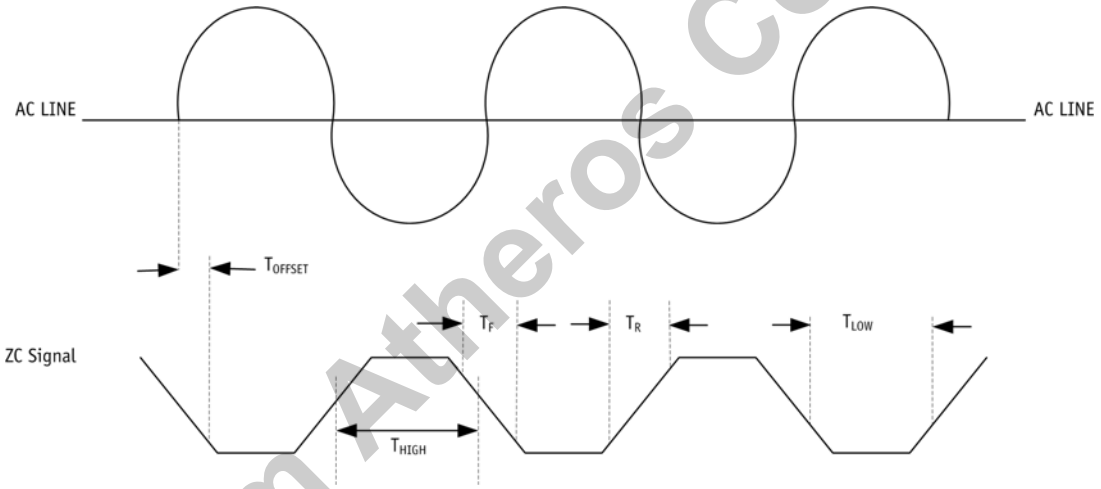


Figure 6-2 ZC_IN Timing

6.3 SPI Master Bus Timing (Boot FLASH)

Table 6-4 SPI Master Timing Specifications

Parameter		Min	Max	Units
t_{CLKp}	SPI_CLK Period	25	—	ns
t_{CLKhi}	SPI_CLK High Time	11	—	ns
t_{CLKlo}	SPI_CLK Low Time	11	—	ns
t_{OV}	Output Valid Time	5	—	ns
t_{OH}	Output Hold Time	5	—	ns
t_{SU}	Input Setup Time	5	—	ns
t_H	Input Hold Time	5	—	ns

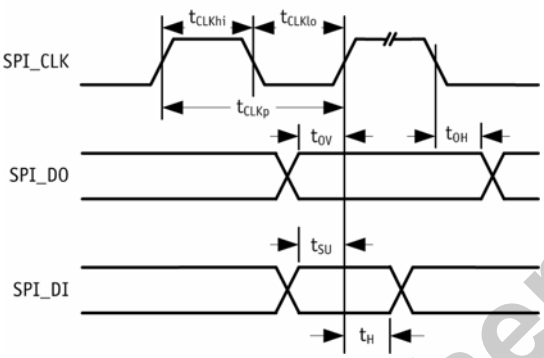


Figure 6-3 SPI Timing Diagram

6.4 SPI Slave Bus Timing

Table 6-5 SPI Slave Timing Specifications

Parameter		Min	Max	Units
t_{CLKp}	SPI Slave CLK Period	83.3	—	ns
t_{CLKhi}	SPI Slave CLK High Time	39	—	ns
t_{CLKlo}	SPI Slave CLK Low Time	39	—	ns
t_{OV}	Output Valid Time	—	SPI Slave CLK Negedge + 7 ns	ns
t_{OH}	Output Hold Time	SPI Slave CLK Negedge	—	ns
t_{SU}	Input Setup Time	—	3	ns
t_H	Input Hold Time	1	—	ns

7 Package Dimensions

The QCA7000 is packaged in a 68-pin QFN package. The body size is 8 mm by 8 mm. The package drawings and dimensions are provided in Figure 7-1, Table 7-1 and Figure 7-2, Table 7-2.

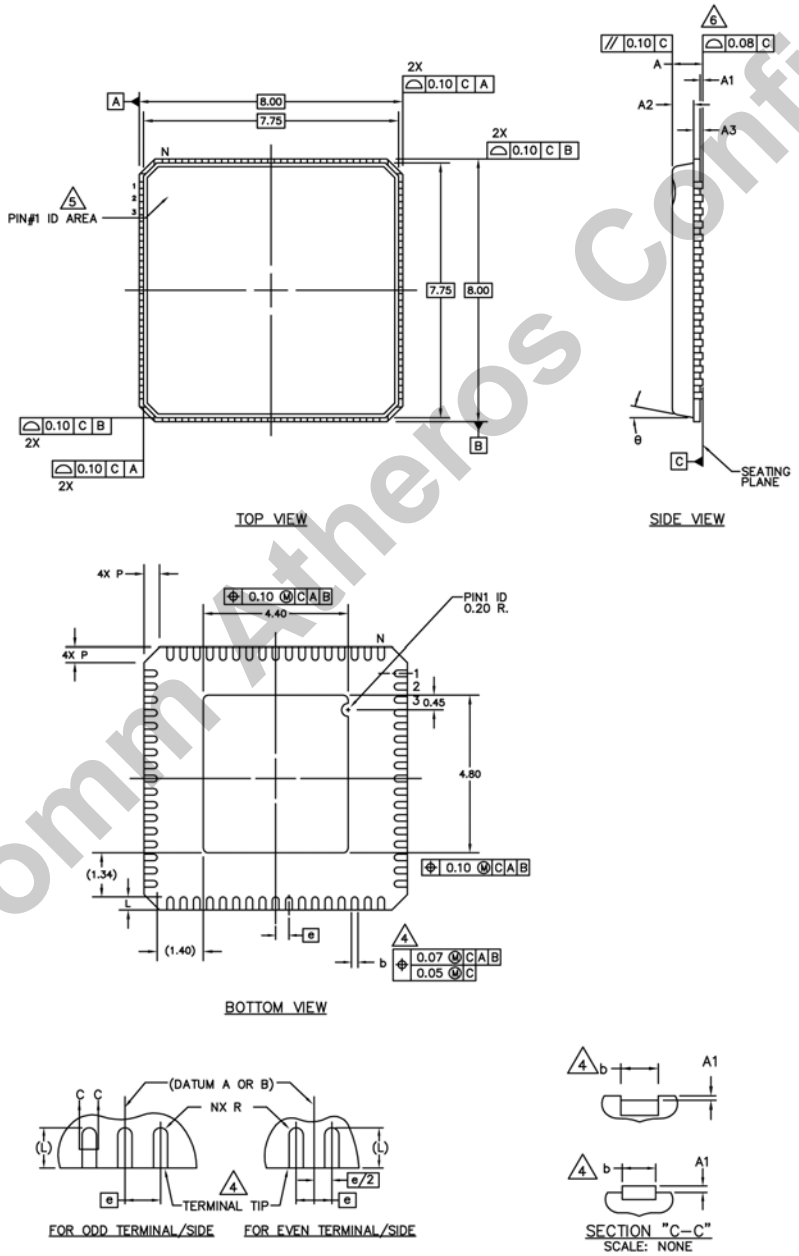


Figure 7-1 Detailed QCA7000 QFN1 Package Dimensions

Table 7-1 Common Dimensions QFN1 [8]

Symbol	Min.	Nom.	Max.	Note
A	0.80	0.85	0.90	
A1	0.00	0.01	0.05	[6]
A2	0.60	0.65	0.70	
A3		0.20 REF.		
q	0	—	12º	
P	0.24	0.42	0.60	
e		0.40 BSC		
N		68		[3]
L	0.30	0.40	0.50	
b	0.15	0.20	0.25	

NOTES:

[1]. Die thickness allowable is 0.305 mm maximum (0.012 inches maximum)

[2]. Dimensioning and tolerances conform to ASME Y14.5M. - 1994.

[3]. N is the number of terminals

[4]. Dimension b applies to plated terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.

[5]. The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body.

[6]. Unilateral coplanarity zone applies to the exposed pad as well as the terminals.

[7]. Package warpage max 0.08 mm.

[8]. All dimensions are in millimeters.

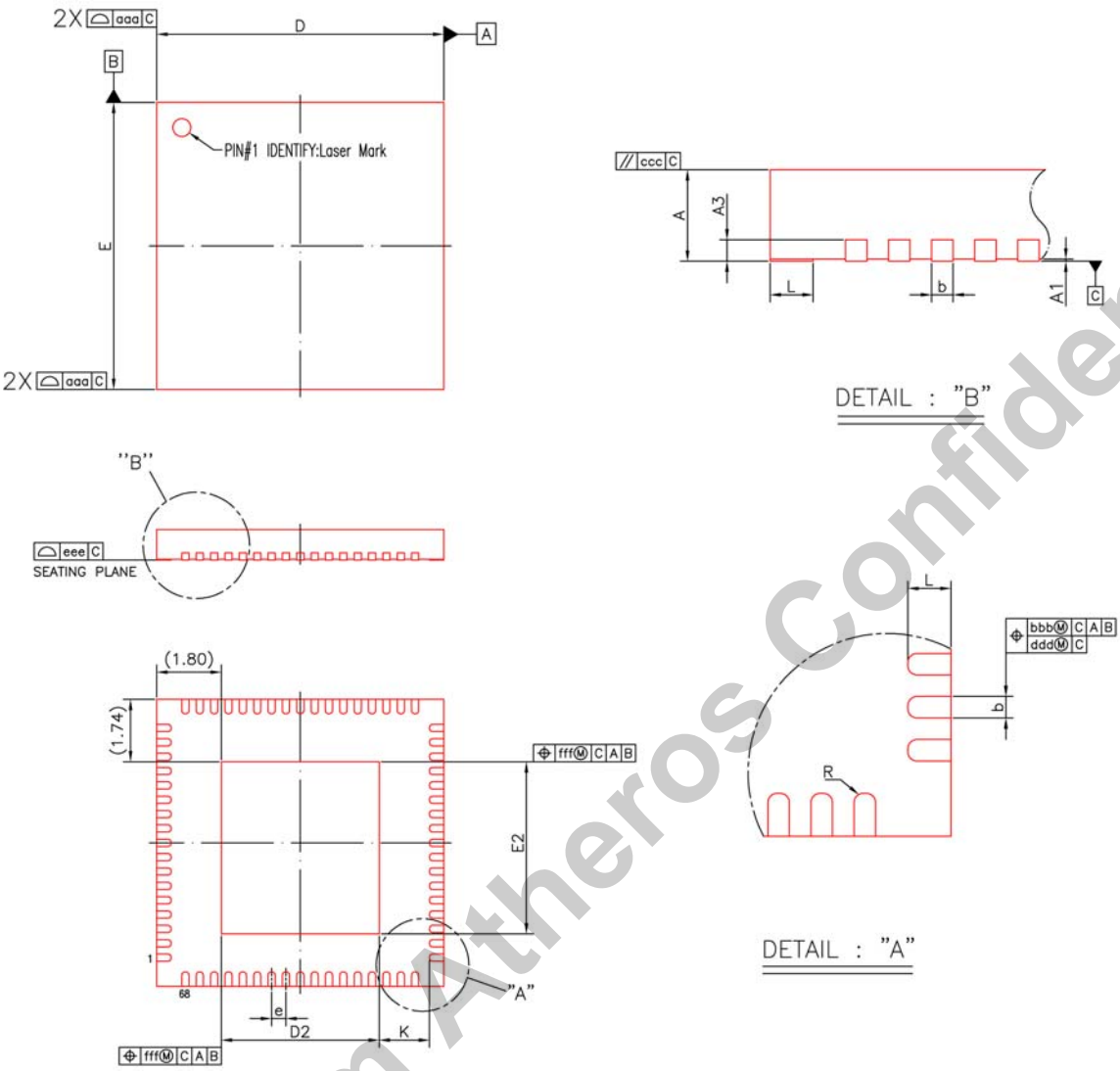


Figure 7-2 Detailed QCA7000 QFN2 Package Dimensions

Table 7-2 Common Dimensions QFN2

Symbol	Min.	Nom.	Max.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF.	
b	0.15	0.20	0.25
D/E	7.90	8.00	8.10
D2	4.25	4.40	4.55
E2	4.65	4.80	4.95
e		0.40 BSC	
L	0.30	0.40	0.50
R	0.075	—	—
K	0.20	—	—
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

NOTES:

[1]. Controlling dimension: millimeters.

[2]. Reference document: JEDEC MO-220.

8 Ordering Information

The order number QCA7000-AL3C specifies a lead-free standard-temperature version of the QCA7000.

The order number QCA7000-AL3C-R specifies a lead-free standard-temperature version of the QCA7000 in tape and reel.

The order number QCA7000-AL3B specifies a lead-free industrial-temperature version of the QCA7000.

The order number QCA7000-AL3B-R specifies a lead-free industrial-temperature version of the QCA7000 in tape and reel.