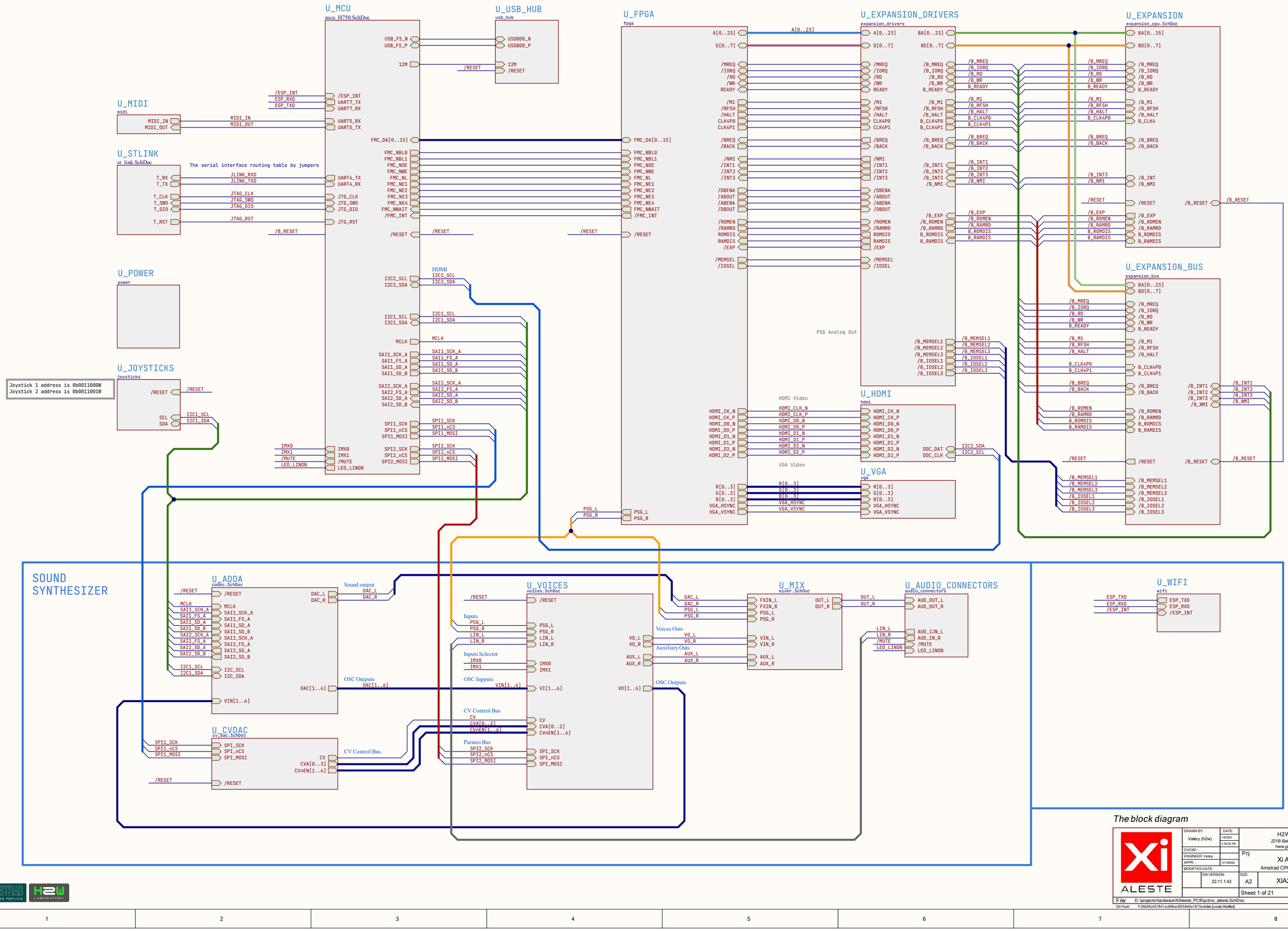
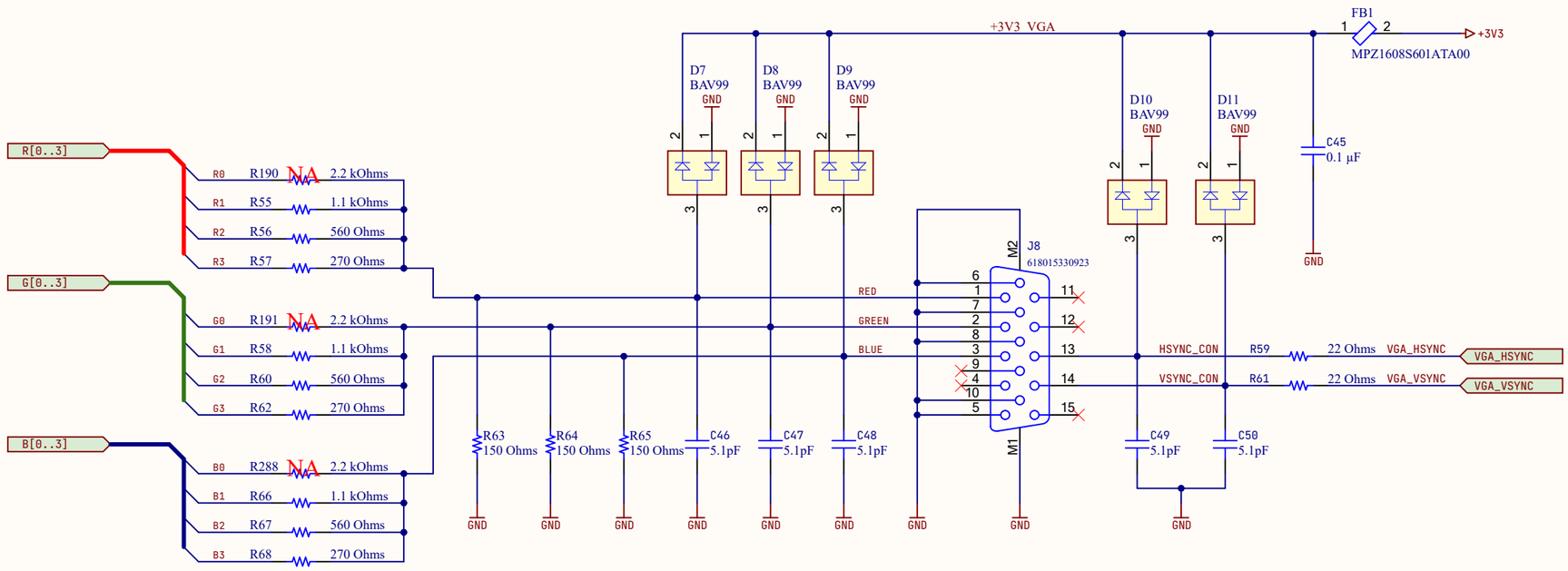

U_MCU
mcu_H750.SchDoc
U_USB_HUB
usb_hub
U_FPGA
fpga
U_EXPANSION_DRIVERS
expansion_drivers
U_EXPANSION
expansion_cpu.SchDoc
U_MIDI
midi
U_STLINK
st_link.SchDoc
The serial interface routing table by jumpers
U_POWER
power
U_JOYSTICKS
joysticks
Joystick 1 address is 0b001100@W
Joystick 2 address is 0b0011001W
HDMI
U_HDMI
hdmi
HDMI Video
U_VGA
vga
VGA Video
PSG Analog Out
U_EXPANSION_BUS
expansion_bus
SOUND SYNTHESIZER
U_ADDA
codec.SchDoc
Sound output
U_VOICES
voices.SchDoc
Inputs
Voices Outs
Auxiliary Outs
Inputs Selector
OSC Inpputs
OSC Outputs
CV Control Bus
Params Bus
U_MIX
mixer.SchDoc
U_AUDIO_CONNECTORS
audio_connectors
U_CVDAC
cv_dac.SchDoc
U_WIFI
wifi
The block diagram
H2W Lab
221B Baker Street
hww.github.io
Xi Aleste
Amstrad CPC6128 Replica
XIA2022
r1.0
Sheet 1 of 21
File: D:\projects\hardware\XiAleste_PCB\pcb\xi_aleste.SchDoc

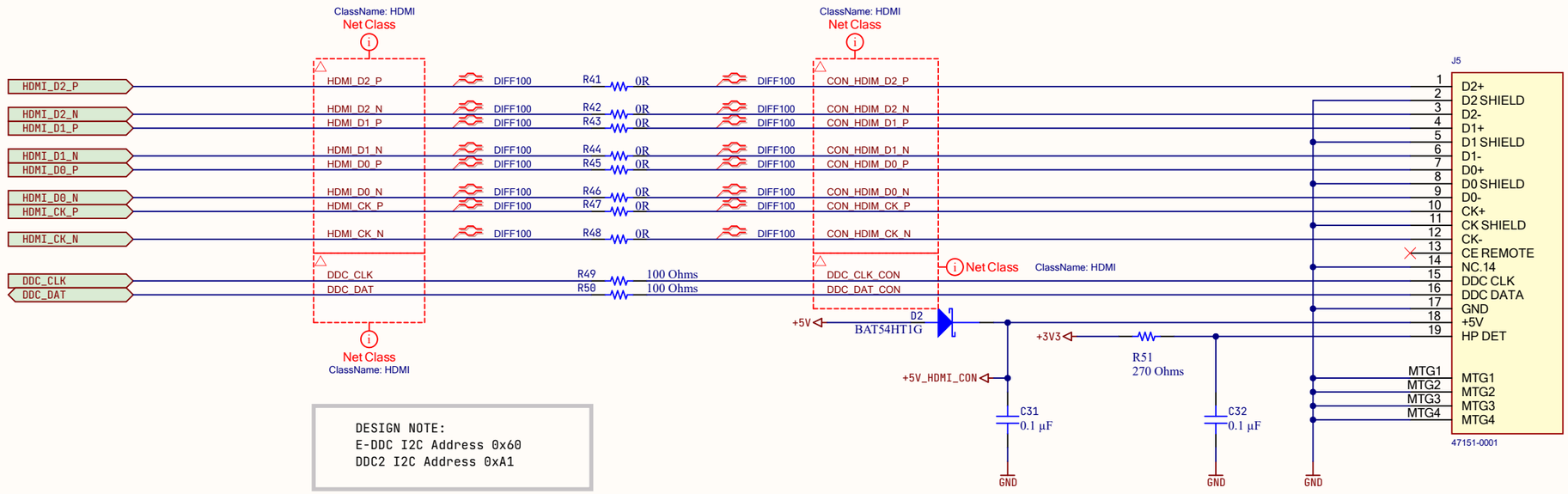


Analog video output

DRAWN BY: Valery (h2w)	DATE: 1/8/2023 2:30:55 PM	H2W Lab *221B Baker Street* *hww.github.io*	
CHCKD: -			
ENGINEER: Valery		Prj: Xi Aleste Amstrad CPC6128 Replica	
APPR: -	12/18/2022		
MODIFYED DATE:			
	SW VERSION: 22.11.1.43	SIZE: A3	XIA2022 REV: r1.0
		Sheet 3 of 21	

File: D:\projects\hardware\XiAleste_PCB\pcb\vga.SchDoc

Git Hash: f126b06c457841cc896ac9f258d6a1873cc4cfab [Locally Modified]



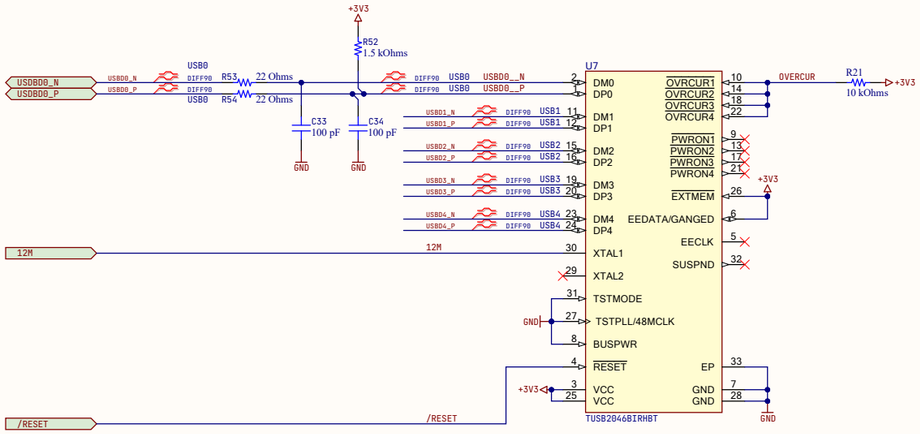
DESIGN NOTE:
E-DDC I2C Address 0x60
DDC2 I2C Address 0xA1

Digital video output

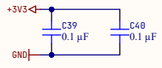
DRAWN BY: Valery (h2w)	DATE: 1/8/2023 2:30:55 PM	H2W Lab *221B Baker Street* *hww.github.io*	
CHCKD: -			
ENGINEER: Valery		Prj: Xi Aleste Amstrad CPC6128 Replica	
APPR: -	12/18/2022		
MODIFYED DATE:			
	SW VERSION: 22.11.1.43	SIZE: A3	XIA2022 REV: r1.0
		Sheet 4 of 21	

File: D:\projects\hardware\XiAleste_PCB\pcb\hdmi.SchDoc
Git Hash: f126b06c457841cc896ac9f258d6a1873cc4cfab [Locally Modified]

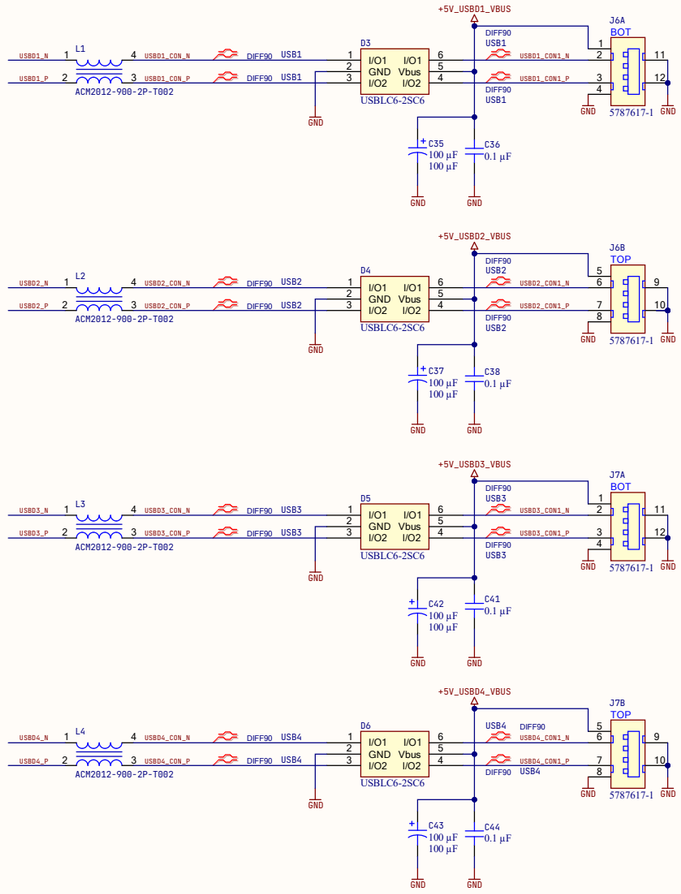
4-port USB 2.0 12-Mbps USB full-speed hub



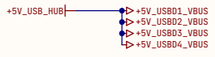
Decoupling



USBD 1-4 FROM HUB



USB POWER



USB Hub

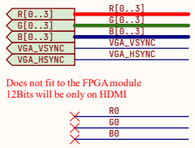
DRAWN BY: Valery (h2w)	DATE: 1/6/2023 2:30:56 PM	H2W Lab *221B Baker Street* *hww.github.io*	
CHKD: -			
ENGINEER: Valery		Prj: Xi Aleste Amstrad CPC6128 Replica	
APPR: -	1/7/2023		
MODIFYED DATE:			
SW VERSION: 22.11.1.43	SIZE: A2	XIA2022	REV: r1.0
		Sheet 5 of 21	

File: D:\projects\hardware\XiAleste_PCB\pcb\usb_hub.SchDoc

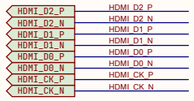
Git Hash: f126b06c457841cc896ac9f258d6a1873cc4dab [Locally Modified]

(21)

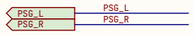
VGA OUTPUT (13 or 16)



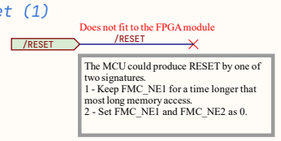
HDMA OUTPUT (8)



PSG Output (2)

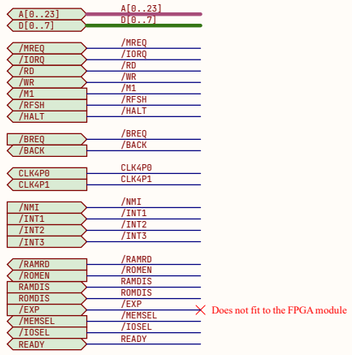


Reset (1)



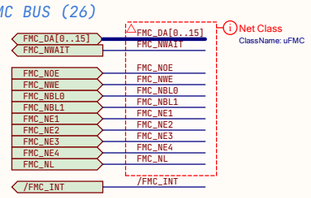
(82)

Z80 INTERFACE (52)

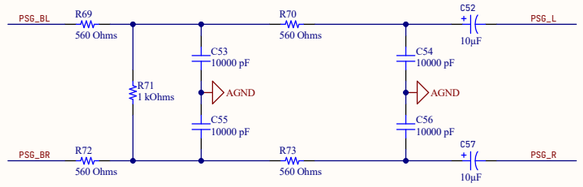


BUS DRIVERS (4)

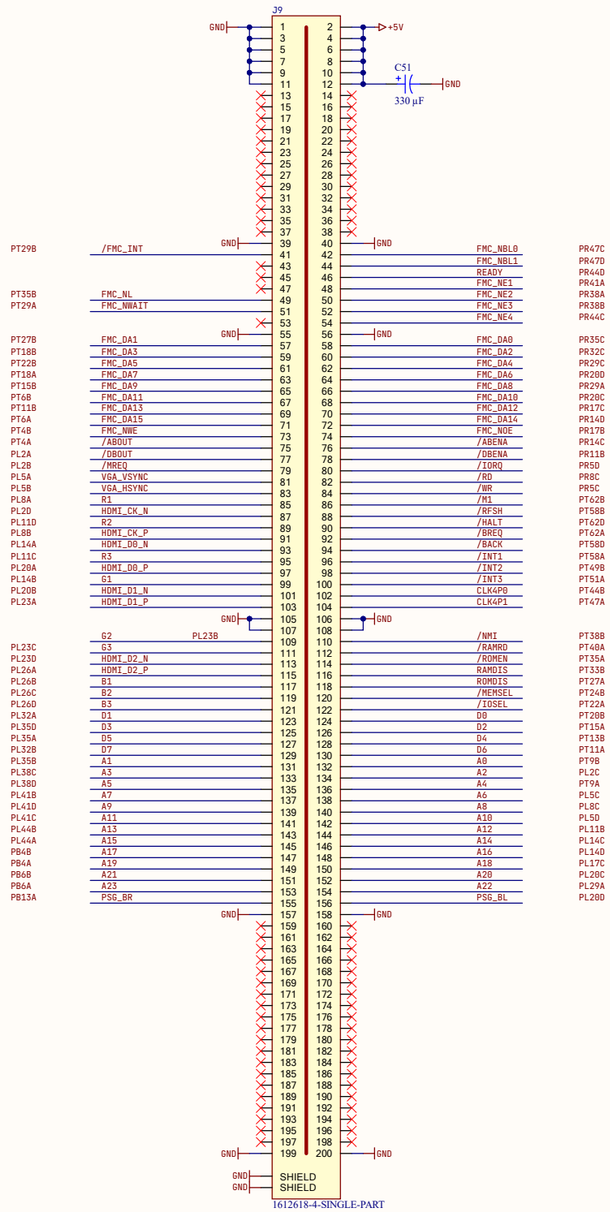
FMC BUS (26)



AUDIO DAC



FPGA SOCKET



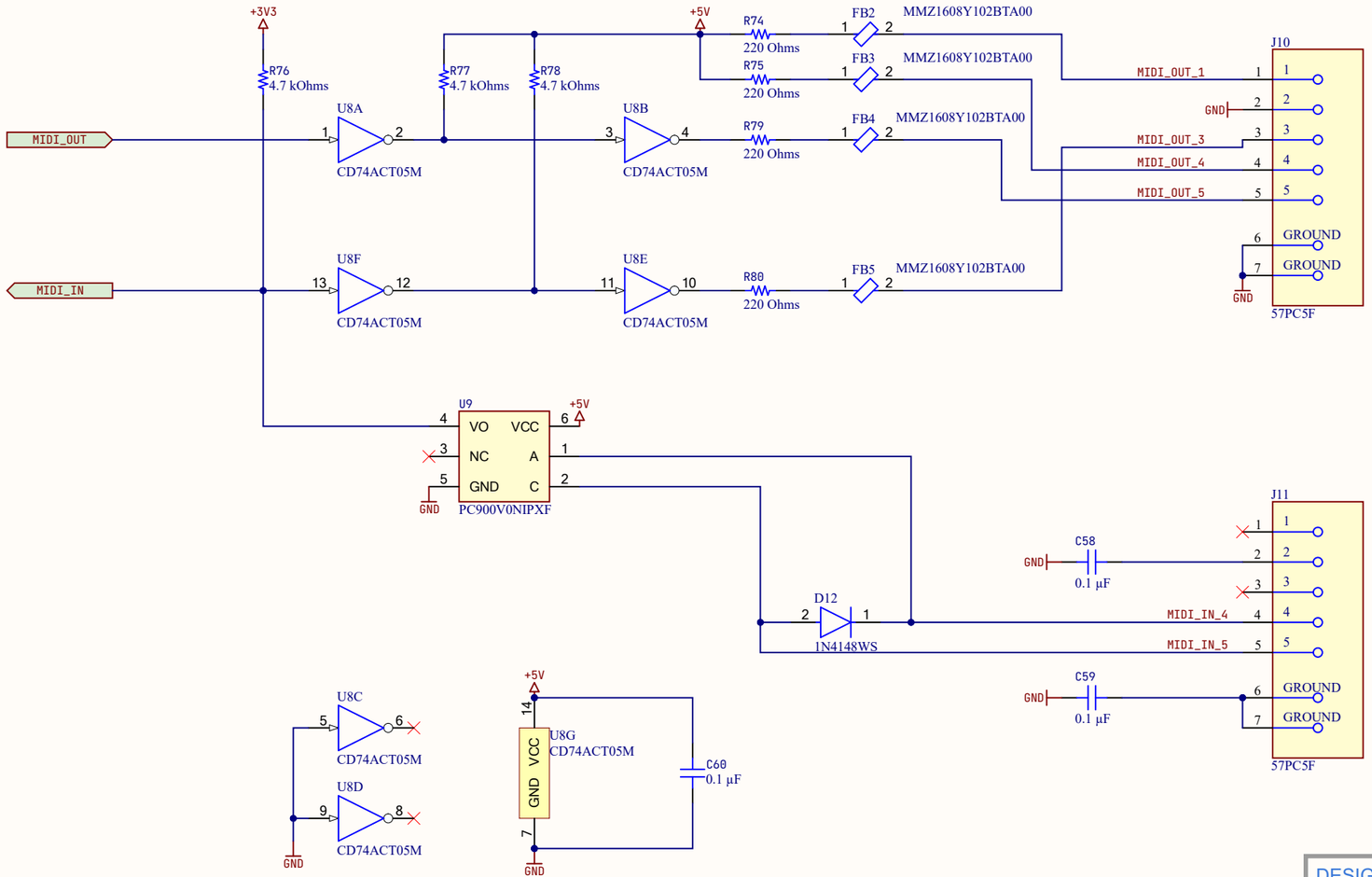
FPGA Socket

DRAWN BY: Valery (h2w)	DATE: 1/8/2023 2:30:56 PM	H2W Lab *221B Baker Street* *hww.github.io*			
CHCKD: -		Prj: Xi Aleste Amstrad CPC6128 Replica			
ENGINEER: Valery					
APPR: -	1/7/2023				
MODIFYED DATE:					
	SW VERSION: 22.11.1.43	SIZE: A2	XIA2022	REV: r1.0	
		Sheet 6 of 21			

File: D:\projects\hardware\XiAleste_PCB\pcb\fpga.SchDoc

Git Hash: f126b06c457841cc896ac9f258d6a1873cc4dab [Locally Modified]

MIDI Interface



DESIGN NOTES:

The recomendations taken from
https://www.midi.org/specifications-old/item/midi-din-electrical-specification

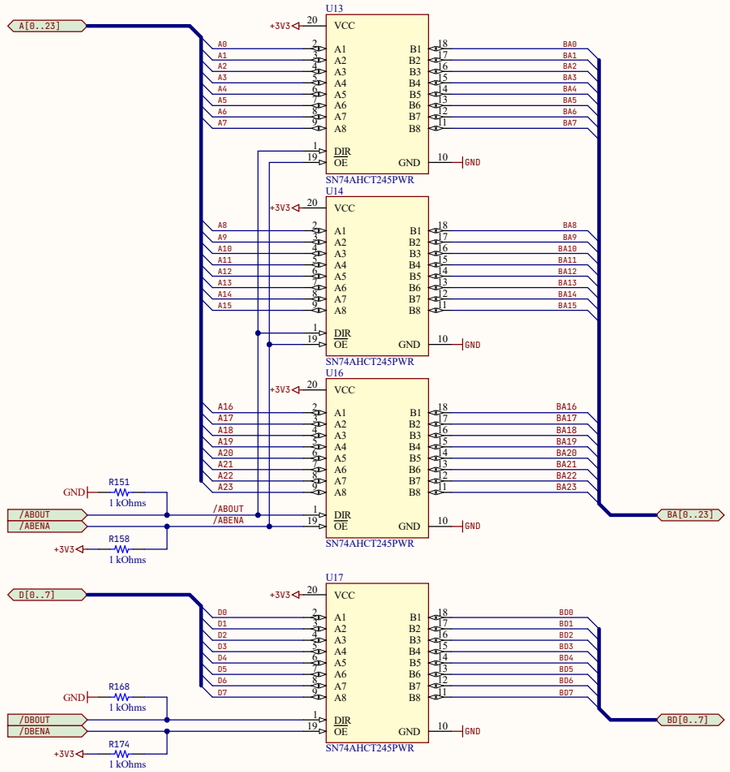
Musical Instrument Digital Interface

DRAWN BY: Valery (h2w)	DATE: 1/8/2023 2:30:56 PM	H2W Lab *221B Baker Street* *hww.github.io*	
CHCKD: -			
ENGINEER: Valery		Prj: Xi Aleste Amstrad CPC6128 Replica	
APPR: -	1/7/2023		
MODIFYED DATE:			
SW VERSION: 22.11.1.43	SIZE: A3	XIA2022	REV: r1.0
	Sheet 7 of 21		

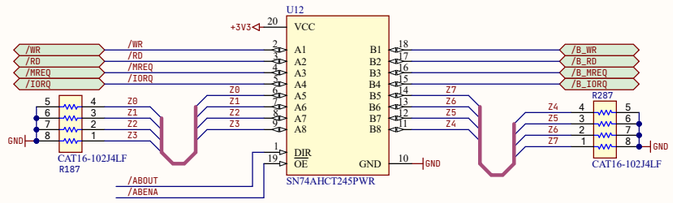
File: D:\projects\hardware\XiAleste_PCB\pcb\midi.SchDoc

Git Hash: f126b06c457841cc896ac9f258d6a1873cc4fab [Locally Modified]

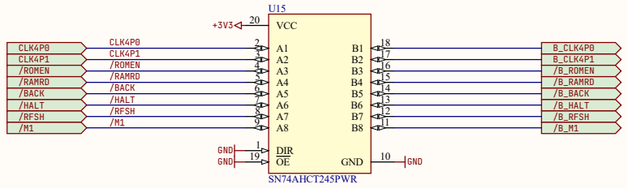
CPU BUS DRIVERS



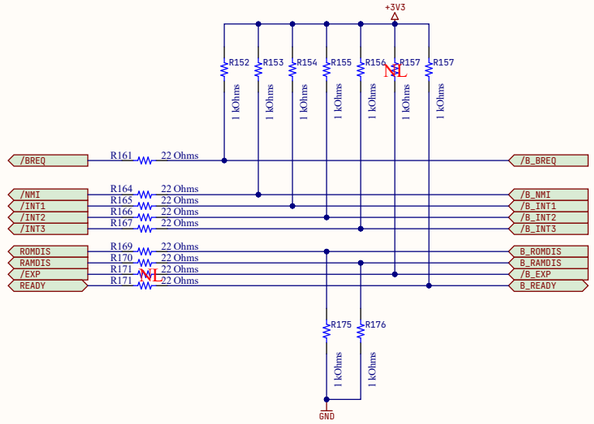
SIGNALS DISABLED BY BUSREQUEST



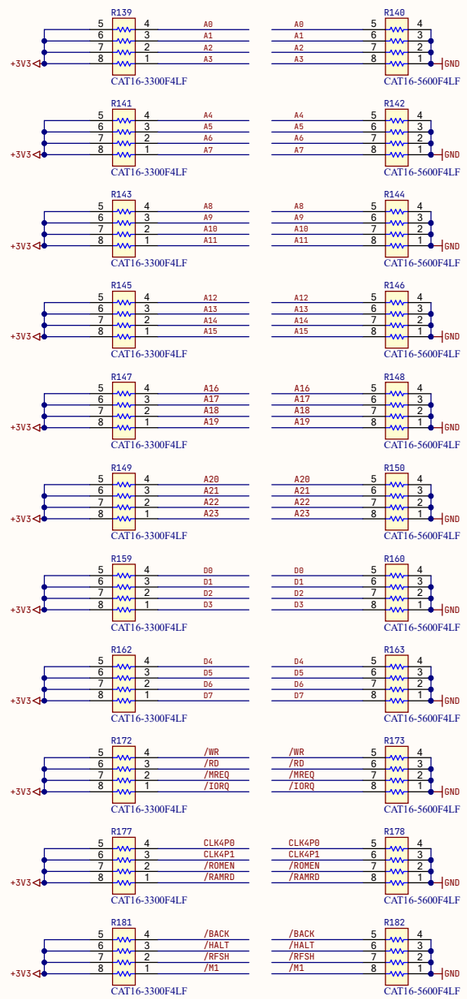
PERSISTANT SIGNALS



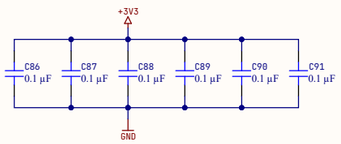
Unbuffered bus wires



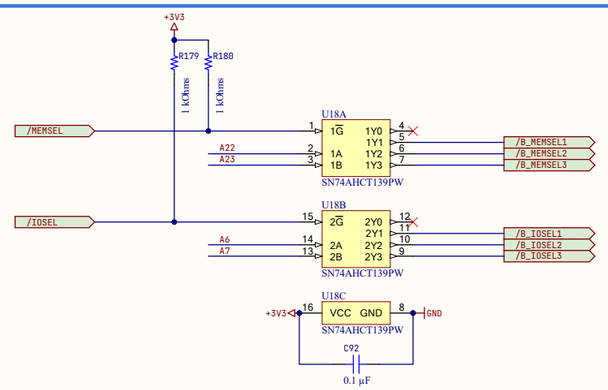
BUS TERMINATION



Decoupling



SLOT NUMBER DECODER



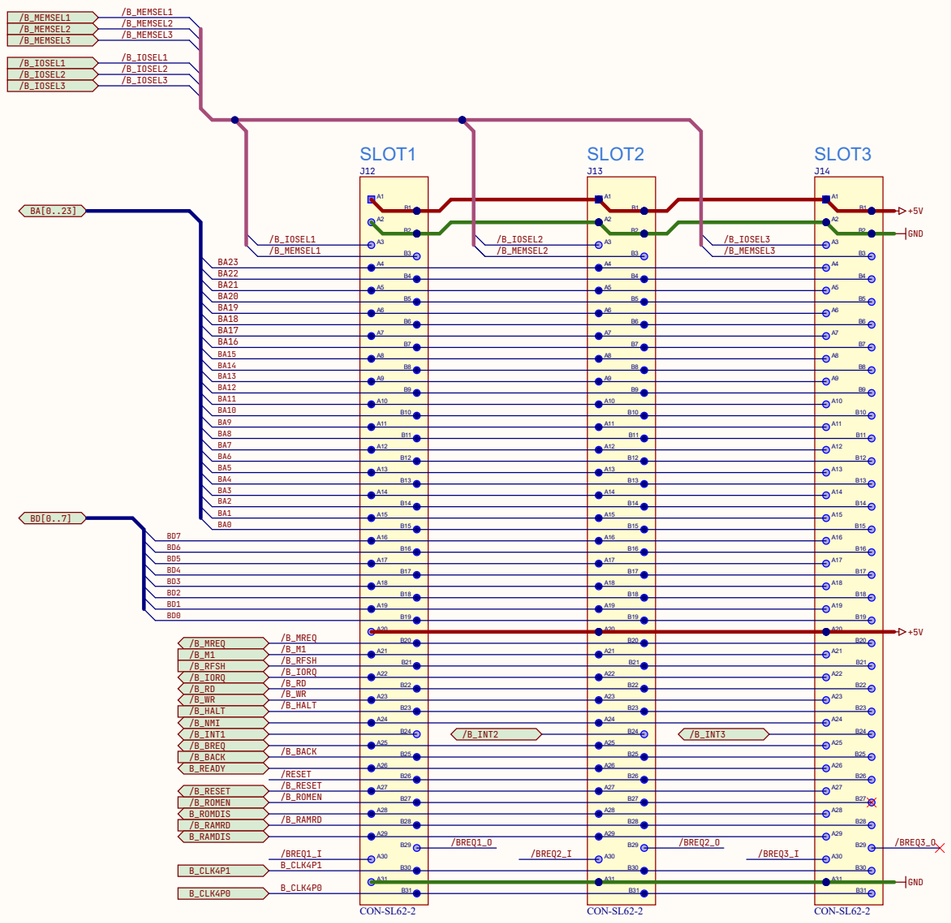
DESIGN NOTES:

(1) With using the slot system from the MSX platform.
(2) The Slot 0:0 is the ROM of Amstrad CPC platform.
(3) The slot 0:1 is the RAM of the Amstrad CPC platform.
(4) The slots 1:X-3:X are expansion slots.

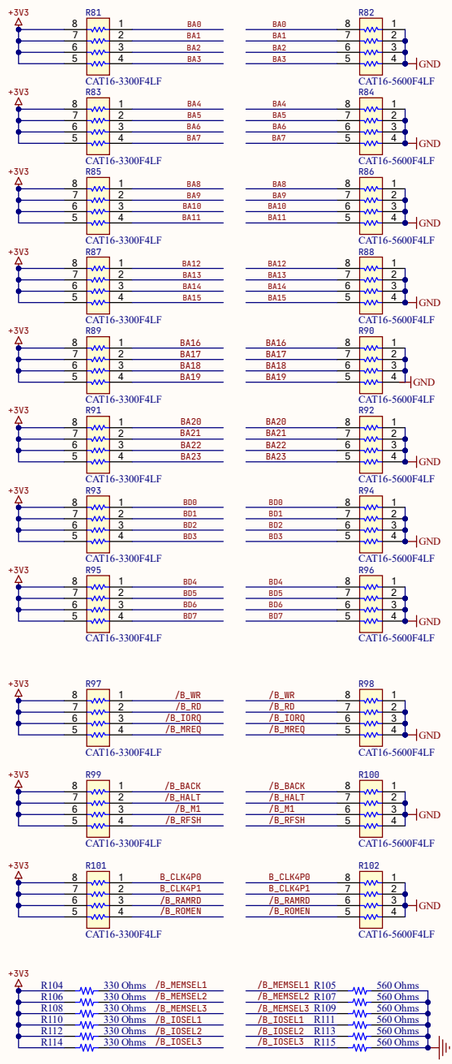
The expansion bus drivers

DRAWN BY: Valery (h2w)	DATE: 1/8/2023 2:30:58 PM	H2W Lab *2218 Baker Street* *hww.github.io*	
CHCKD: -			
ENGINEER: Valery		Prj: Xi Aleste Amstrad CPC6128 Replica	
APPR: -	1/8/2023		
MODIFYED DATE:			
	SW VERSION: 22.11.1.43	SIZE: A2	XIA2022 REV: r1.0
		Sheet 8 of 21	

File: D:\projects\hardware\XiAleste_PCB\pcb\expansion_drivers.SchDoc
Git Hash: f126b06c457841cc896ac9f258d6a1873cce4dab [Locally Modified]



BUS PULL UP



DESIGN NOTES

It is required to modify the Amstrad CPC 128 expansion slot, as well as to use the best of what has been implemented in the Aleste 520EX. Therefore, the following technical solutions were assumed:

1. It is possible to remove all unnecessary things from Amstrad CPC and Aleste 520EX. For example: sound output and light pen.

2. It is necessary to make better power supply - to increase number of outputs. Put the power signals side by side for easier wiring of the daughter board.

3. It is permissible to freely modify the pinout connector preserving the spirit of CPC and Aleste 520EX.

4. Add the ability to use multiple cards with DMA -- Multi-Master Bus. Better, for geographic prioritization, equip the connector with pins ID0 and ID1. Which will tell the card its geographic address -- slot number. Slot 0 is reserved for the motherboard.

5. Adapt the MSX slot system to Aleste and the use of DMA. Extend the slot system to the IOSPACE output space. Add the ability to use a simple IO space decoder, for this, add a /IOCS peg which is zero only when accessing the space reserved for slots.

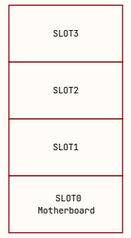
6. Provide in the bus the ability to quickly get a mask of interrupts. To do this add the /INTCS signal. The daughter cards set the data bit to zero on the card number: D[ID] = /INTCS ? Z : /CARD_INT;

7. Add one or two additional clock signals.

8. To prioritize, add pins for interrupt and bus request chains. If necessary, place a dispenser on the motherboard.

8. The NMI signal will be a signal of the hardware error. So the Bain function in the interrupt routine is to analyze the issue and report to the system or HALT the computer.

Diagram 1 - The memory map



9. It is possible to create the system with one, two or three slots. The CPC 129 connector coulrd be oimmited.

Diagram 2 - Mini ITX Form Factor

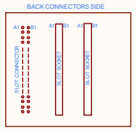
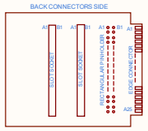
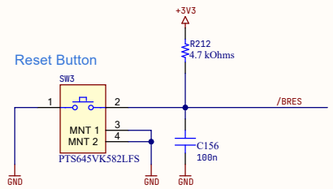


Diagram 3 - Non Standard Form Factor

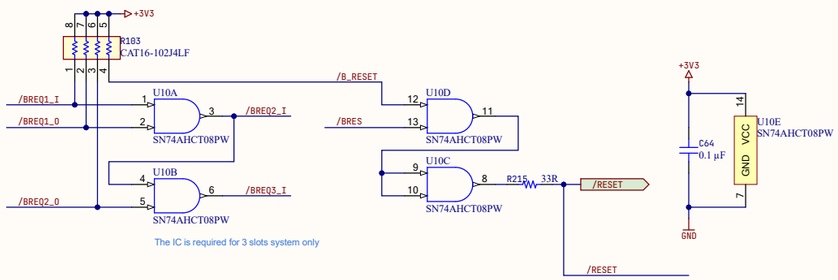


Buttons



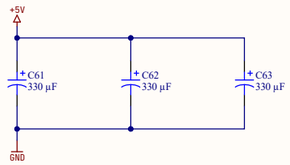
BUS ARBITER

DESIGN NOTE
Used the daisy-chain similar to Apple IIGS but with this arbiter on the motherboard.



The IC is required for 3 slots system only

PER CONNECTOR DECOUPLING

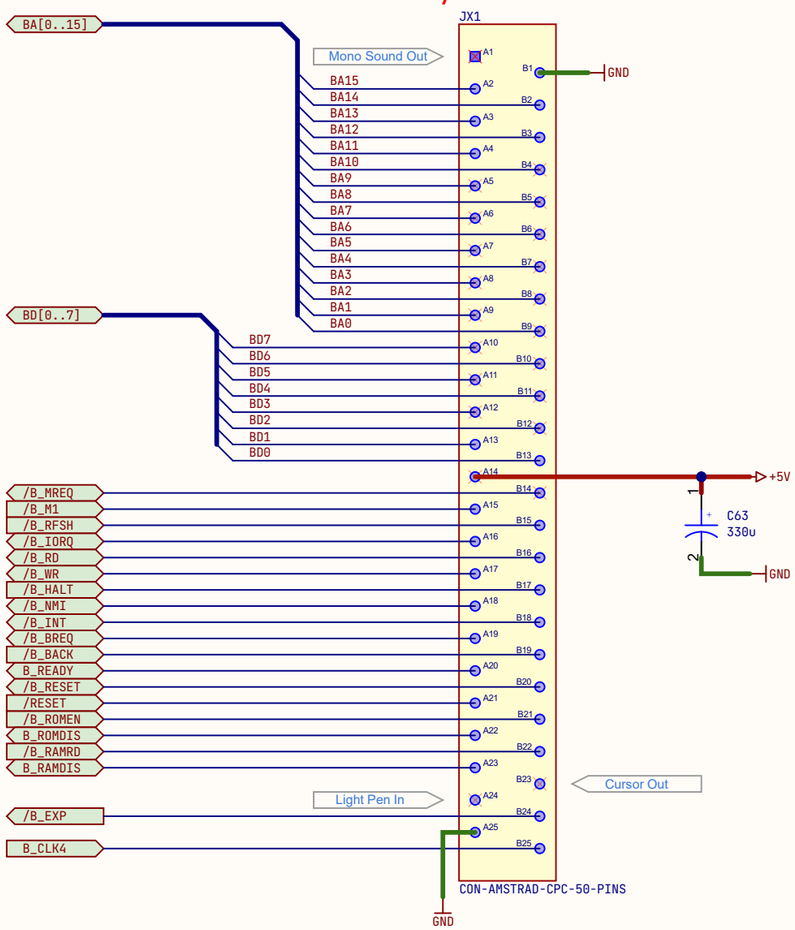


XiAleste expansion bus

DRAWN BY: Valery (h2w)	DATE: 1/8/2023 2:30:57 PM	H2W Lab *2218 Baker Street* *hww.github.io*	
CHCKD: -			
ENGINEER: Valery		Prj: Xi Aleste Amstrad CPC6128 Replica	
APPR: -	1/8/2023		
MODIFYED DATE:			
SW VERSION: 22.11.1.43	SIZE: A2	XIA2022	REV: r1.0
	Sheet 9 of 21		
File: D:\projects\hardware\XiAleste_PCB\pcb\expansion_bus.SchDoc			
Git Hash: f126b06c457841cc896ac9258d6a1873cc4dab [Locally Modified]			

The Amstrad CPC Processor Direct Connector

Dont Layout On Mini iTX



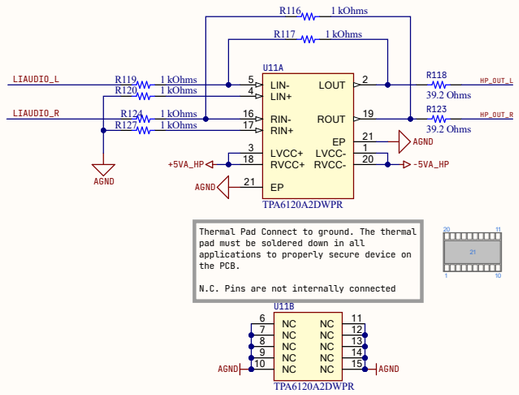
DESIGN NOTES:

1. The edge connector fully support the Amstrad CPC 128. But it omit a cursor and mono sound out.
2. The NMI signal in the XiAleste will be a signal of the hardware error. So the main function in the interrupt routine is to analyze the issue and report to the system or HALT the computer.
4. The CPC expansion has the pin READY connected through 82ohm to the GATE-ARRAY's output pin. It makes the READY pin as output. The Aleste 520ex has the serial resistor value significantly bigger, and it makes this pin as BIDIR. In the XiAleste this pin will be just an input pin.

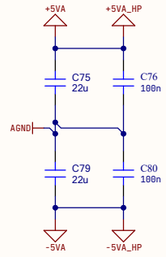
Amstrad expansion connector

DRAWN BY: Valery (h2w)	DATE: 1/8/2023 2:30:57 PM	H2W Lab *221B Baker Street hww.github.io*	
CHCKD: -			
ENGINEER: Valery		Prj: Xi Aleste	
APPR: -	1/8/2023		
MODIFYED DATE:			
	SW VERSION: 22.11.1.43	SIZE: A3	XIA2022 REV: r1.0
		Sheet 10 of 21	
File: D:\projects\hardware\XiAleste_PCB\pcb\expansion_cpu.SchDoc			
Git Hash: f126b06c457841cc896ac9f258d6a1873cc4cfab [Locally Modified]			

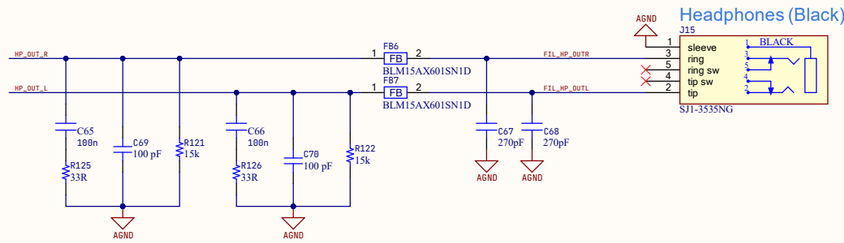
Headphones Amplifier



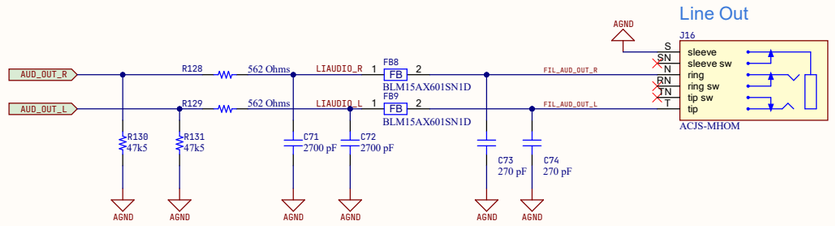
Headphones Amplifier Decoupling



Headphones

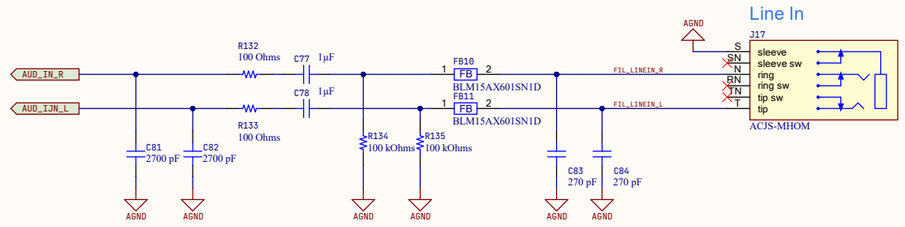


Line Out

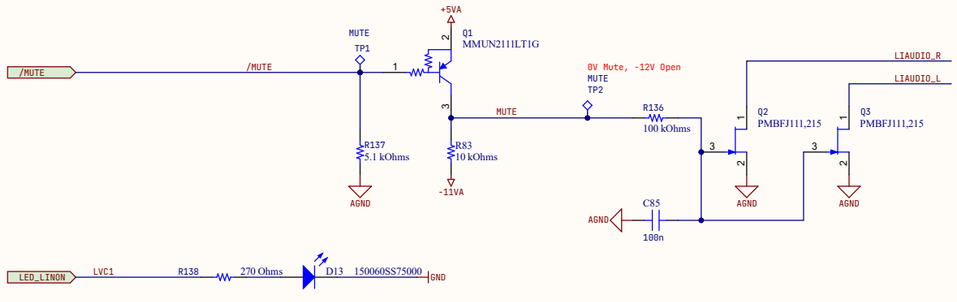


DESIGN NOTE:
Source for the audio filters is http://www.cirrus.com/en/pubs/rdDatasheet/CDB4207_DB1.pdf

Line In

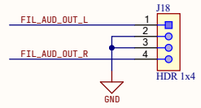


MUTE DRIVER



The line in mode enabled (Slow blink on mute)

Line Out (Internal)

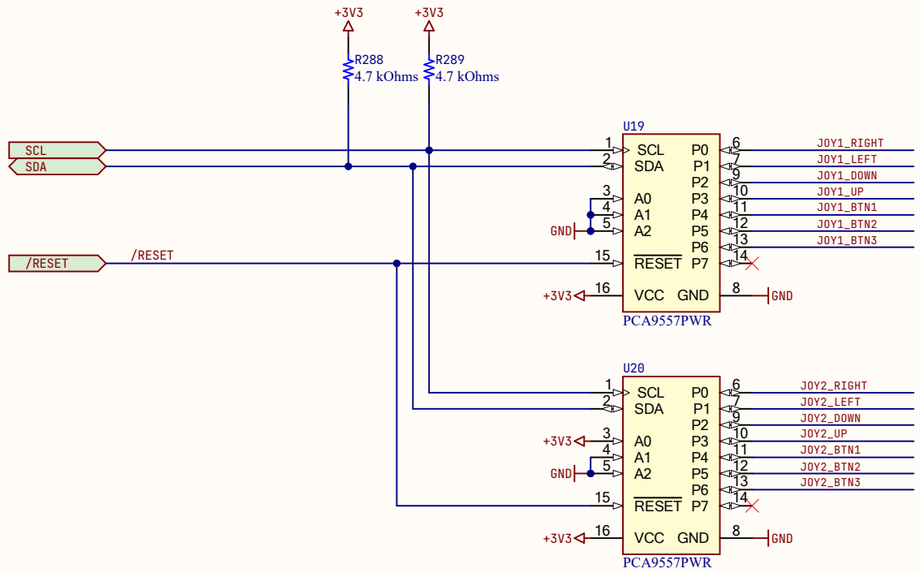


Audio connectors and headphones amplifier

DRAWN BY: Valery (h2w)	DATE: 1/8/2023 2:30:57 PM	H2W Lab *2218 Baker Street* *hww.github.io*	
CHCKD: -		Prj: Xi Aleste Amstrad CPC6128 Replica	
ENGINEER: Valery			
APPR: -	1/8/2023		
MODIFYED DATE:			
SW VERSION: 22.11.1.43		SIZE: A2	XIA2022 REV: r1.0
		Sheet 11 of 21	

File: D:\projects\hardware\XiAleste_PCB\pcb\audio_connectors.SchDoc
Git Hash: f126b06c457841cc896ac9f258d6a1873cc4dab [Locally Modified]

JOYSTICK BUS

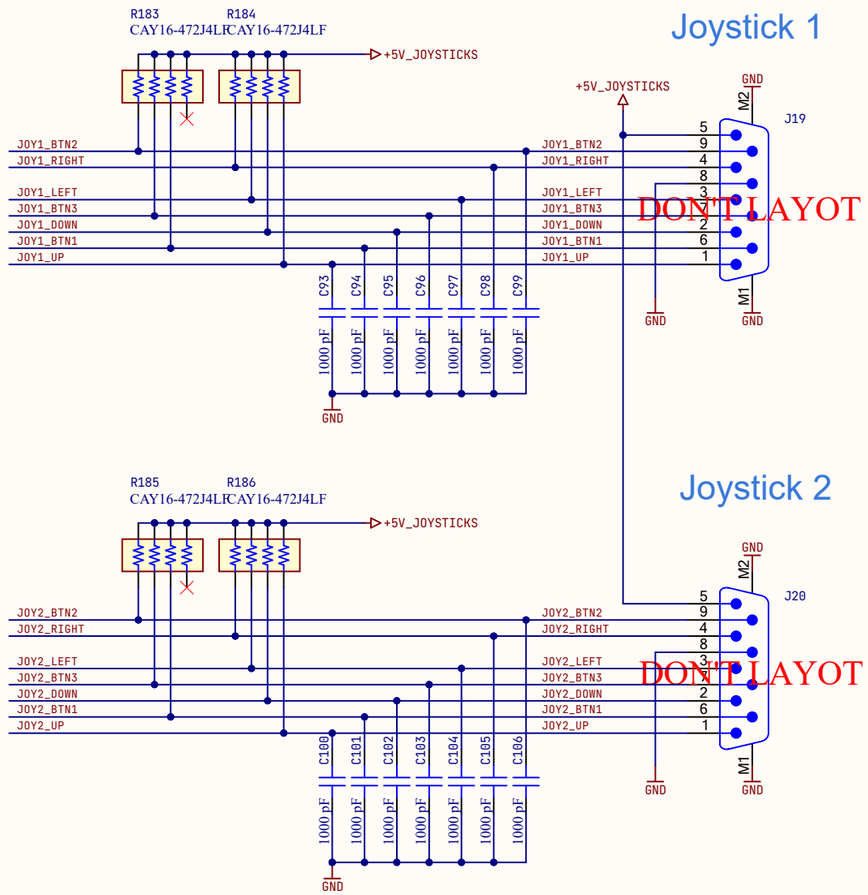


DESIGN NOTE

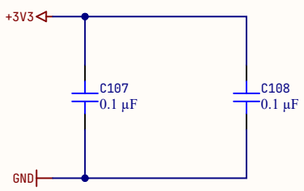
The device address is 0b0011_xxxW

Joystick 1 address is 0b0011_000W
Jovstick 2 address is 0b0011 001W

GAME CONTROLLERS

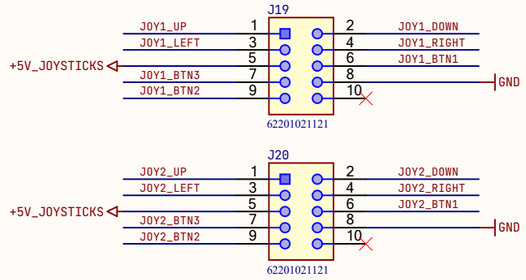


Decoupling



The alternative connectors

Use this connector instead of DB9 when there are not enought space on the board



Joysticks interface

ALESTE	DRAWN BY: Valery (h2w)	DATE: 1/8/2023 2:30:57 PM	H2W Lab *221B Baker Street* *hww.github.io*
	CHCKD: -		
	ENGINEER: Valery		Prj: Xi Aleste Amstrad CPC6128 Replica
	APPR: -	1/8/2023	
	MODIFYED DATE:		
	SW VERSION: 22.11.1.43	SIZE: A3	XIA2022 REV: r1.0
			Sheet 12 of 21
File: D:\projects\hardware\XiAleste_PCB\pcb\joysticks.SchDoc			
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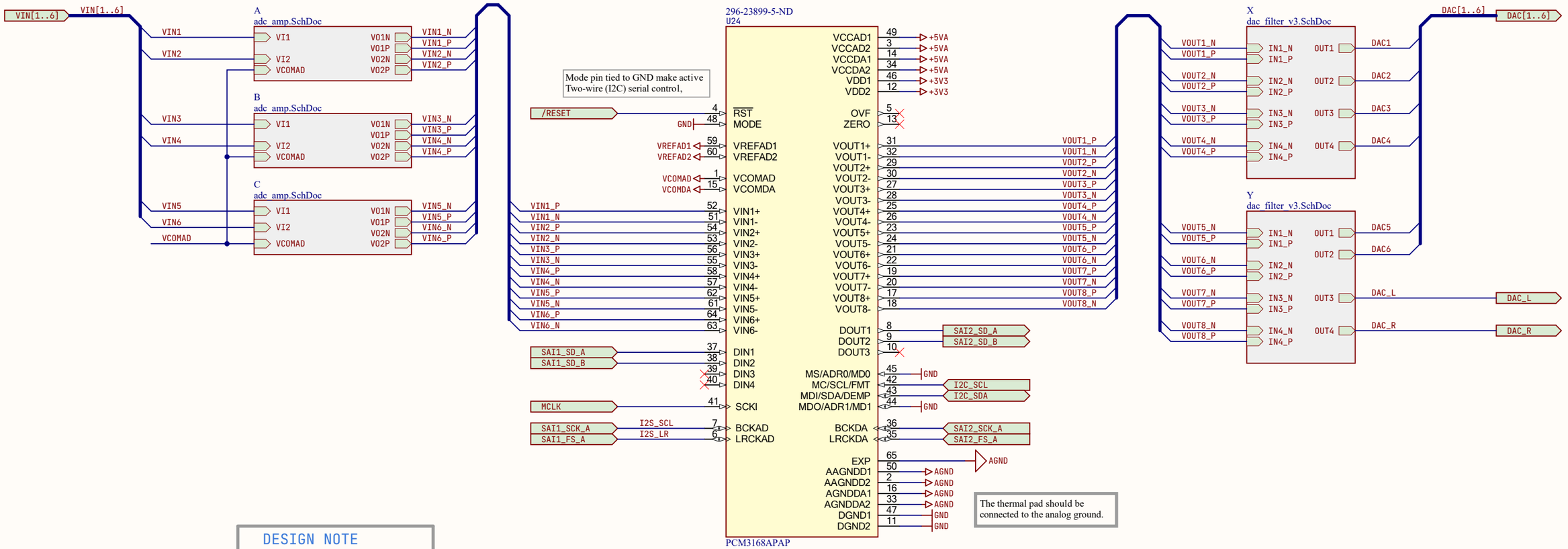
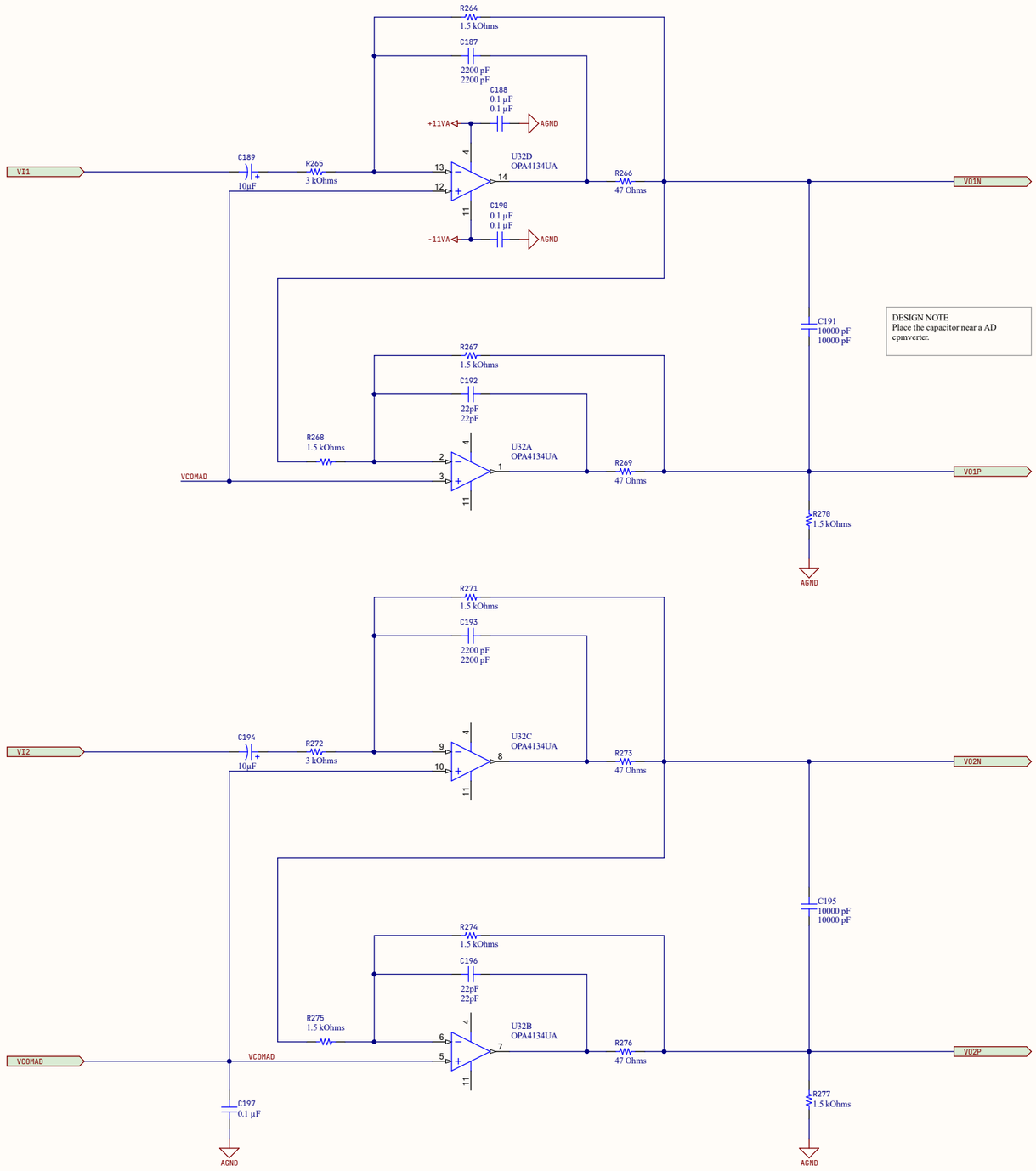

VIN[1..6]
VIN[1..6]
VIN1
VIN2
VIN3
VIN4
VIN5
VIN6
VCOMAD
A
adc_amp.SchDoc
VI1
VI2
VCOMAD
VO1N
VO1P
VO2N
VO2P
VIN1_N
VIN1_P
VIN2_N
VIN2_P
B
adc_amp.SchDoc
VIN3_N
VIN3_P
VIN4_N
VIN4_P
C
adc_amp.SchDoc
VIN5_N
VIN5_P
VIN6_N
VIN6_P
296-23899-5-ND
U24
Mode pin tied to GND make active
Two-wire (I2C) serial control,
/RESET
GND
VREFAD1
VREFAD2
VCOMAD
VCOMDA
VIN1_P
VIN1_N
VIN2_P
VIN2_N
VIN3_P
VIN3_N
VIN4_P
VIN4_N
VIN5_P
VIN5_N
VIN6_P
VIN6_N
SAI1_SD_A
SAI1_SD_B
MCLK
SAI1_SCK_A
SAI1_FS_A
I2S_SCL
I2S_LR
RST
MODE
VREFAD1
VREFAD2
VCOMAD
VCOMDA
VIN1+
VIN1-
VIN2+
VIN2-
VIN3+
VIN3-
VIN4+
VIN4-
VIN5+
VIN5-
VIN6+
VIN6-
DIN1
DIN2
DIN3
DIN4
SCKI
BCKAD
LRCKAD
VCCAD1
VCCAD2
VCCDA1
VCCDA2
VDD1
VDD2
+5VA
+3V3
OVF
ZERO
VOUT1+
VOUT1-
VOUT2+
VOUT2-
VOUT3+
VOUT3-
VOUT4+
VOUT4-
VOUT5+
VOUT5-
VOUT6+
VOUT6-
VOUT7+
VOUT7-
VOUT8+
VOUT8-
DOUT1
DOUT2
DOUT3
SAI2_SD_A
SAI2_SD_B
MS/ADR0/MD0
MC/SCL/FMT
MDI/SDA/DEMP
MDO/ADR1/MD1
I2C_SCL
I2C_SDA
BCKDA
LRCKDA
SAI2_SCK_A
SAI2_FS_A
EXP
AGND
AAGNDD1
AAGNDD2
AGNDDA1
AGNDDA2
DGND1
DGND2
PCM3168APAP
The thermal pad should be
connected to the analog ground.
X
dac_filter_v3.SchDoc
Y
dac_filter_v3.SchDoc
IN1_N
IN1_P
IN2_N
IN2_P
IN3_N
IN3_P
IN4_N
IN4_P
OUT1
OUT2
OUT3
OUT4
DAC[1..6]
DAC1
DAC2
DAC3
DAC4
DAC5
DAC6
DAC_L
DAC_R
DESIGN NOTE
Address is: 0b1000_1xxw
Where bits:
xx A0,A1
w Write
Result address is: 0b1000_100w
C121 2.2 µF
C122 0.1 µF 0.1 µF
C123 2.2 µF
C124 0.1 µF 0.1 µF
C125 2.2 µF
C126 0.1 µF 0.1 µF
C127 2.2 µF
C128 0.1 µF 0.1 µF
C129 2.2 µF
C130 0.1 µF 0.1 µF
C131 2.2 µF
C132 0.1 µF 0.1 µF
C133 2.2 µF
C134 0.1 µF 0.1 µF
C135 2.2 µF
C136 0.1 µF 0.1 µF
C137 2.2 µF
C138 0.1 µF 0.1 µF
C139 2.2 µF
C140 0.1 µF 0.1 µF
AMSTRAD CPC128 REPLICA
H2W LABORATORY
Audio coded
XiALESTE
DRAWN BY: Valery (h2w)
DATE: 1/8/2023 2:30:58 PM
CHCKD: -
ENGINEER: Valery
APPR: -
APPR: 1/8/2023
MODIFYED DATE:
SW VERSION: 22.11.1.43
H2W Lab
221B Baker Street
hww.github.io
Prj:
Xi Aleste
Amstrad CPC6128 Replica
SIZE: A3
XIA2022
REV: r1.0
Sheet 13 of 21
File: D:\projects\hardware\XiAleste_PCB\pcb\codec.SchDoc
Git Hash: f126b06c457841cc896ac9f258d6a1873cc4fab [Locally Modified]

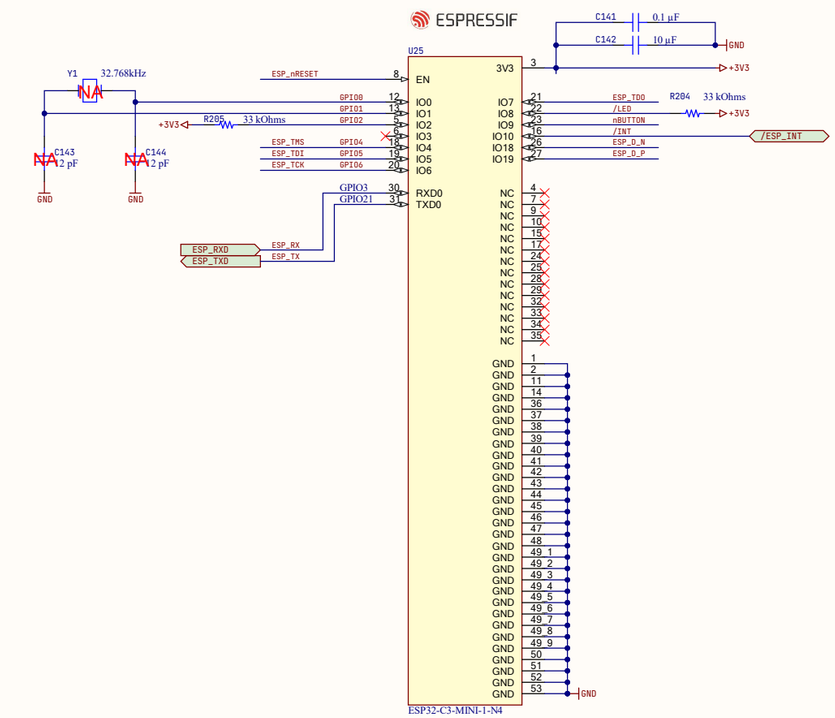


AD Converters/Filters

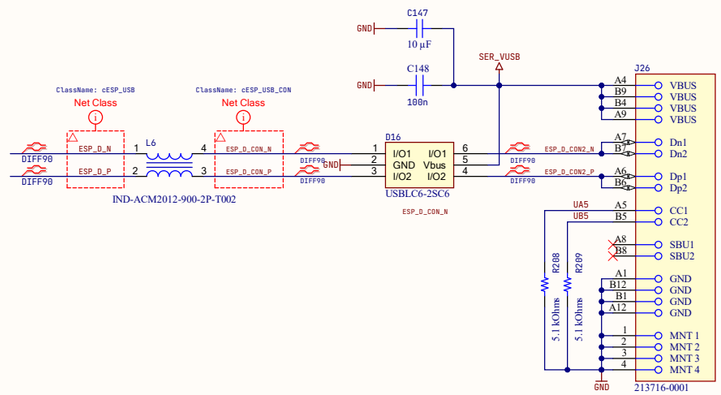
DRAWN BY: Valery (h2w)	DATE: 1/8/2023 2:30:58 PM	H2W Lab *221B Baker Street* *hww.github.io*	
CHCKD: -			
ENGINEER: Valery		Prj: Xi Aleste Amstrad CPC6128 Replica	
APPR: -	1/7/2023		
MODIFYED DATE:			
SW VERSION: 22.11.1.43		SIZE: A2	XIA2022 REV: r1.0
		Sheet 15 of 21	

File: D:\projects\hardware\XiAleste_PCB\pcb\adc_amp.SchDoc
Git Hash: f126b06c457841cc896ac9f258d5a1873ccdda [Locally Modified]

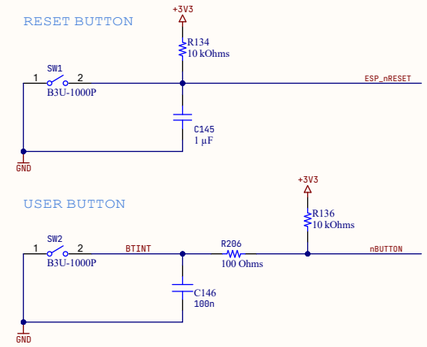
WIFI CONTROLLER



USB CONNECTOR

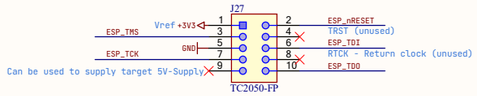


BUTTONS



WIFI LED

ESP JTAG INTERFACE



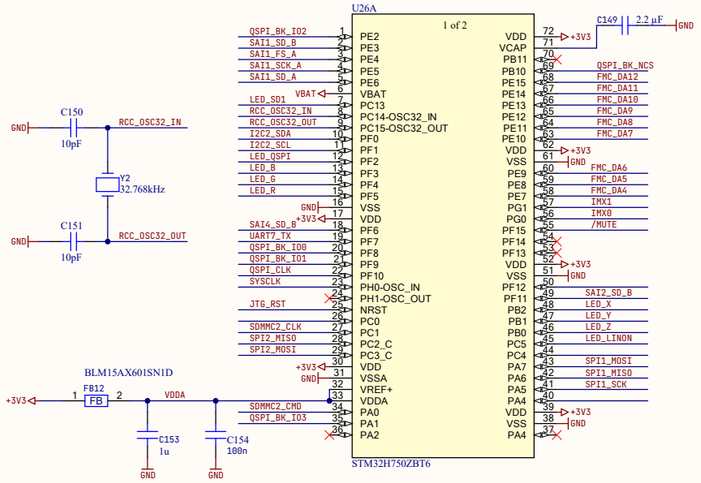
Take note that the ESP32-C3 does not support SWD
The JTAG port on the ESP32-C3 is an industry-standard JTAG port which lacks (and does not need) the TRST pin.

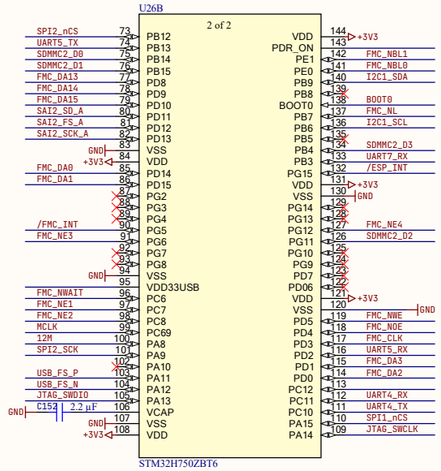
WiFi Controller

DRAWN BY: Valery (h2w)	DATE: 1/8/2023 2:30:58 PM	H2W Lab *2218 Baker Street* *hww.github.io*	
CHCKD: -		Prj: Xi Aleste Amstrad CPC6128 Replica	
ENGINEER: Valery			
APPR: -	1/8/2023		
MODIFYED DATE:			
SW VERSION: 22.11.1.43		SIZE: A2	XIA2022 REV: r1.0
		Sheet 16 of 21	

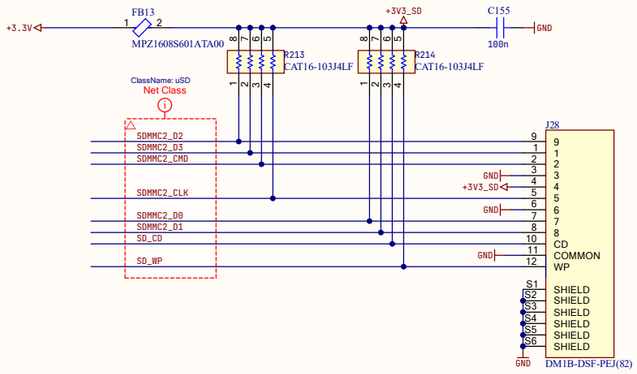
File: D:\projects\hardware\XiAleste_PCB\pcb\wifi.SchDoc
Git Hash: f126b06c457841cc896ac9f258d6a1873cc4dab [Locally Modified]

Microcontroller

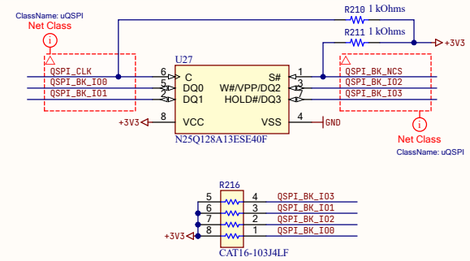




SD/MMC Card 1

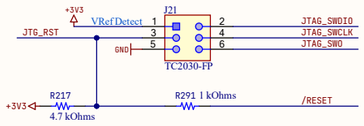


Quad SPI ROM

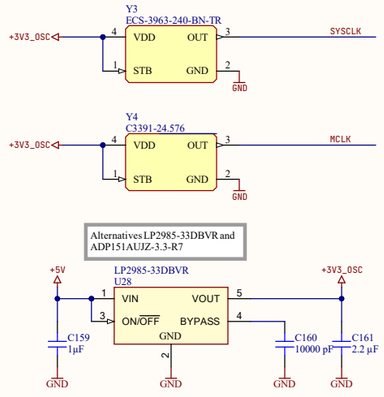


JTAG

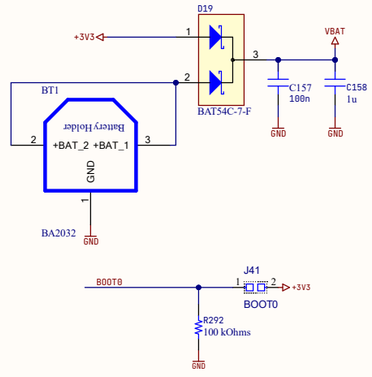
Target header



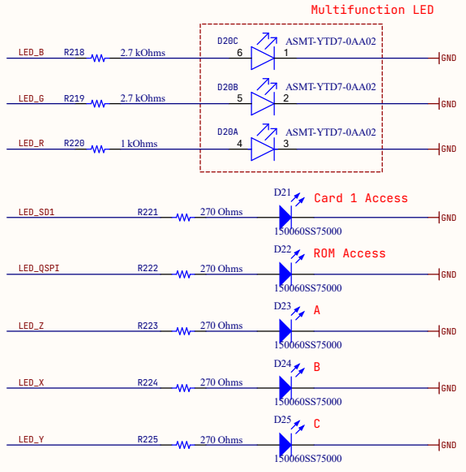
DAC & System Clock



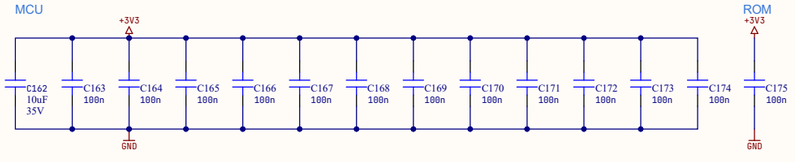
RTC POWER

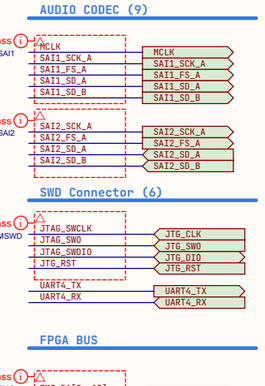


LEDs



Decoupling





Digital Signal Processor

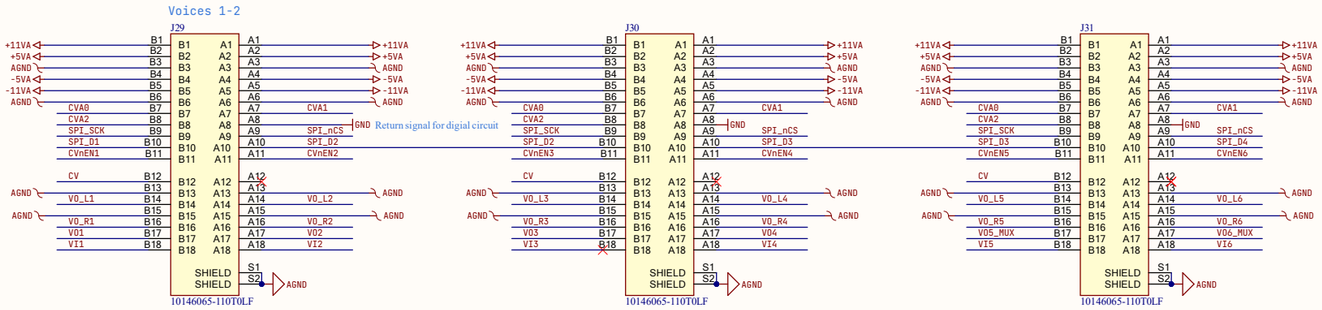
DRAWN BY: Valery (h2w)	DATE: 1/8/2023 2:30:58 PM	H2W Lab *221B Baker Street hww.github.io*	
CHCKD: -		Prj:	Xi Aleste
ENGINEER: Valery			Amstrad CPC6128 Replica
APPR: -	1/8/2023		
MODIFIED DATE:			
SW VERSION: 22.11.1.43	SIZE: A2	XIA2022	REV: r1.0
		Sheet 17 of 21	

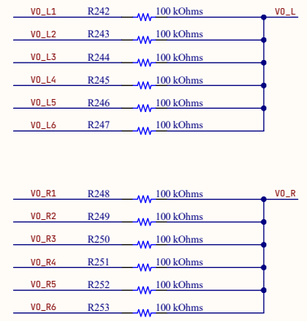
File: D:\projects\hardware\XiAleste_PCB\pcb\mcu_H750.SchDoc

Git Hash: f126b06c457841cc896ac9f25b6e1873cc4dab [Locally Modified]

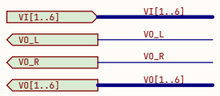
VOICE BOARDS CONNECTORS

Voices 1-2



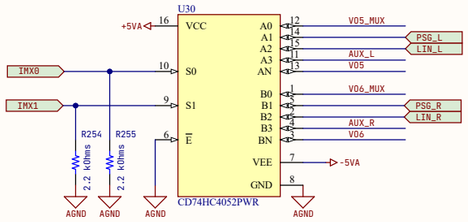


The voices inputs and outputs

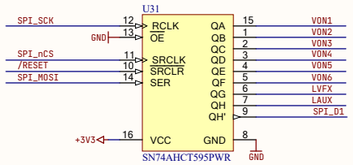


A contol volage signals

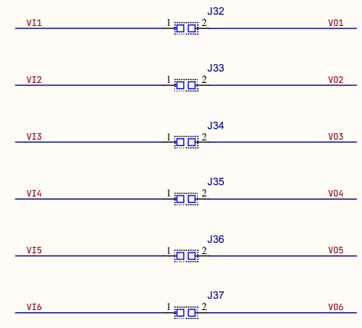
The line in or voice 6 switcher



Voice enable bits to display or use for analog boards

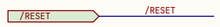


The dveloper's options

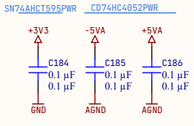


SPI For Control Bits

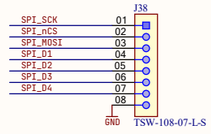
Additional signals



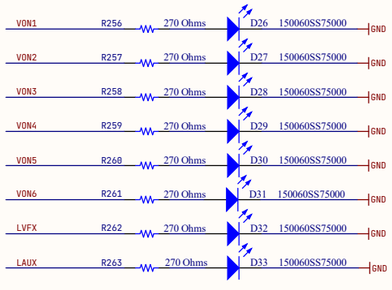
Decoupling



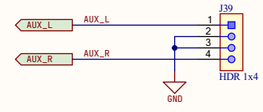
Debug uinterface



Display a voice by LED



AUXILIARY INPUT



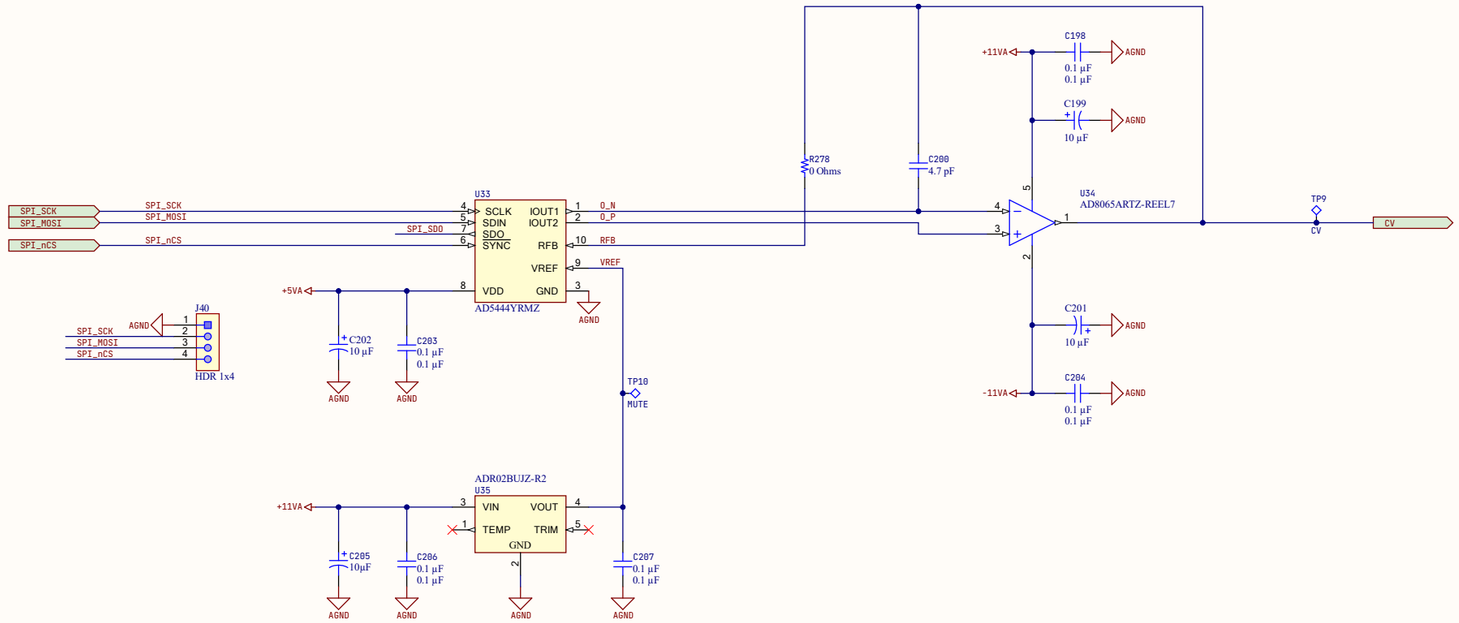
DESIGN NOTES

The voice board should store CB and CV values with the 74HC259 and HCT4051.
74HC259 -- Has 3 bits address, data source and /write strobe. Also it has the /RESET bit.
HCT4051 -- has 3 bits address and single /strobe. Second one

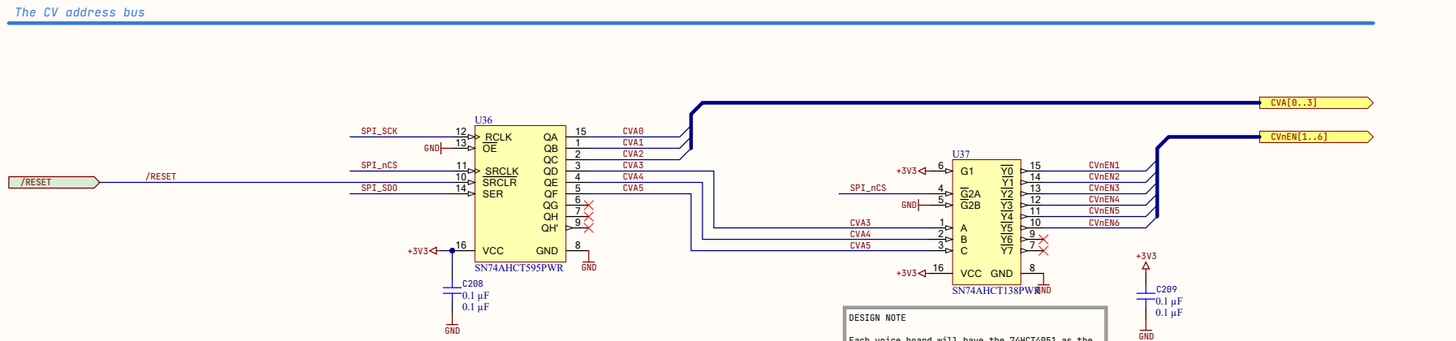
Sound expantion bus

DRAWN BY: Valery (h2w)	DATE: 1/8/2023 2:30:59 PM	H2W Lab *221B Baker Street* *hww.github.io*	
CHCKD: -		Prj: Xi Aleste Amstrad CPC6128 Replica	
ENGINEER: Valery			
APPR: -	1/8/2023		
MODIFYED DATE:			
SW VERSION: 22.11.1.43		SIZE: A2	XIA2022 REV: r1.0
		Sheet 18 of 21	
File: D:\projects\hardware\XiAleste_PCB\pcb\voices.SchDoc			
Git Hash: f128b06e457841cd896ac9f2b5da1873ccdda [Locally Modified]			

The CV address bus



The CV address bus



DESIGN NOTE

Each voice board will have the 74HCT4051 as the C-based voltage memory. This chip requires low level for enabling.

DESIGN NOTE

The MCU has a value (Master Inter Data Idleness). For the memo:

Master Inter Data Idleness

Specifies minimum time delay (expressed in SPI clock cycles periods) inserted between two consecutive data frames in master mode This parameter can be a value of SPI Master Inter-Data IdelenessIn any case

DESIGN NOTES

DAC Voltage

The DAC is used in the unipolar mode. The Vout = 0-Vref. Output Voltage Settling Timeis about 100ns.
The voltage is updating on the rising edge of /SYNC signal.

DAC Timing diagram

The falling edge of SCLK shifts the DAC register. The rising edge of SYNC will apply the value and form the CV in about 100-200ns. The same for the SN74AHCT595PWR. The /SYNCPH2 signal allows the DAC value to be written to the sampling and storage device.

Control voltage DA converter

DRAWN BY: Valery (h2w)	DATE: 1/8/2023 2:30:59 PM	H2W Lab *2218 Baker Street* *hww.github.io*	
CHCKD: -		Prj: Xi Aleste Amstrad CPC6128 Replica	
ENGINEER: Valery			
APPR: -	1/7/2023		
MODIFYED DATE:			
	SW VERSION: 22.11.1.43	SIZE: A2	XIA2022 REV: r1.0
		Sheet 19 of 21	

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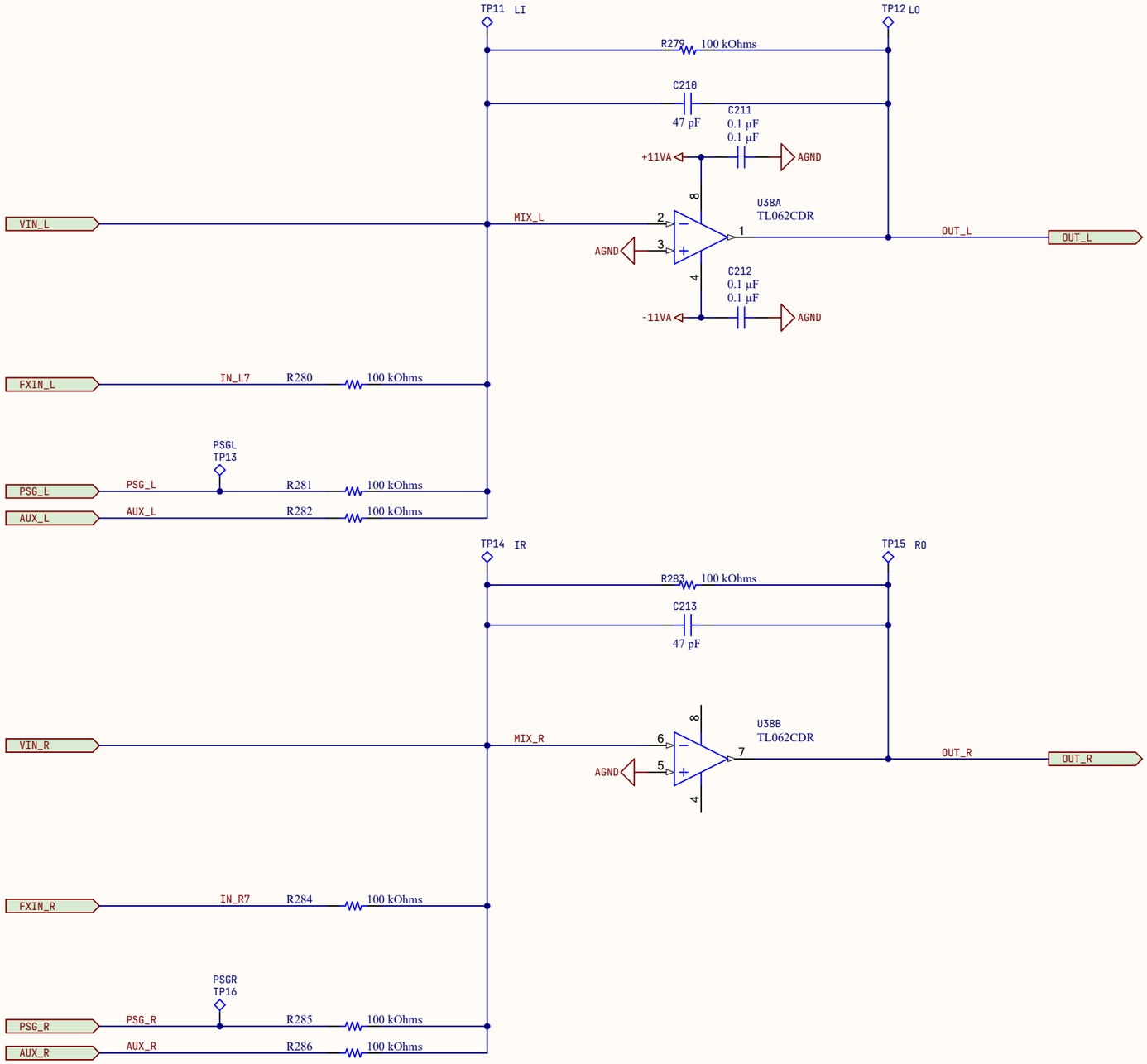

The audio mixer

DRAWN BY: Valery (h2w)	DATE: 1/8/2023 2:30:59 PM	H2W Lab *221B Baker Street* *hww.github.io*	
CHCKD: -			
ENGINEER: Valery		Prj: Xi Aleste Amstrad CPC6128 Replica	
APPR: -	12/18/2022		
MODIFYED DATE:			
	SW VERSION: 22.11.1.43	SIZE: A3	XIA2022 REV: r1.0
		Sheet 20 of 21	

File: D:\projects\hardware\XiAleste_PCB\pcb\mixer.SchDoc

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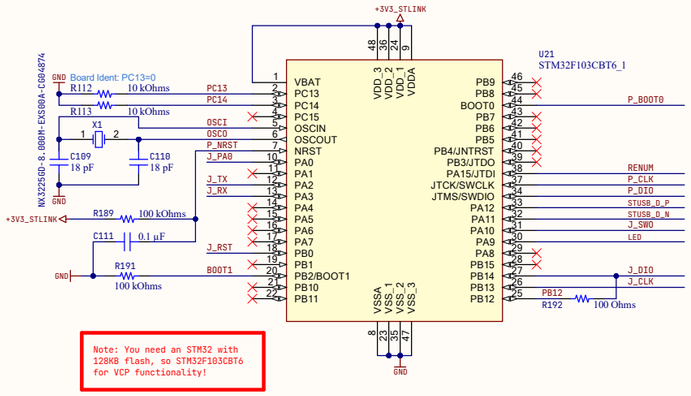
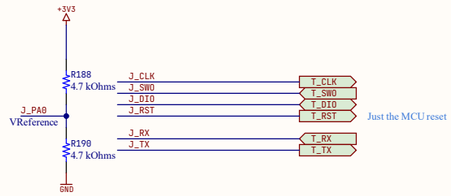
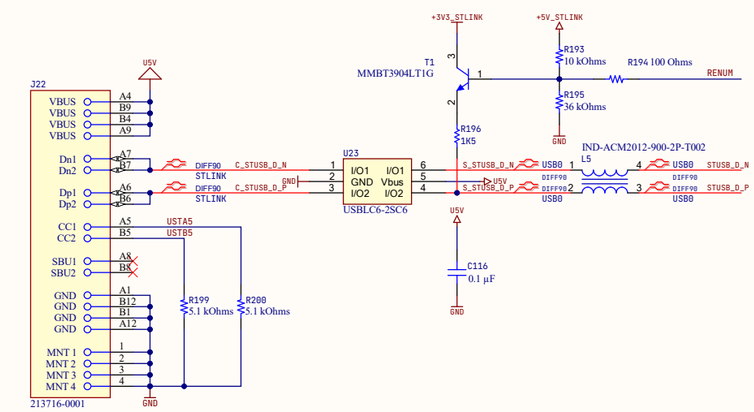
Microcontroller



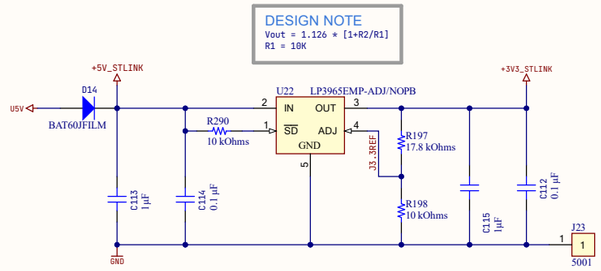
SWD & Serial to DSP



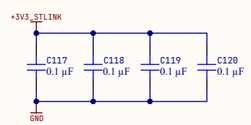
USB STLink



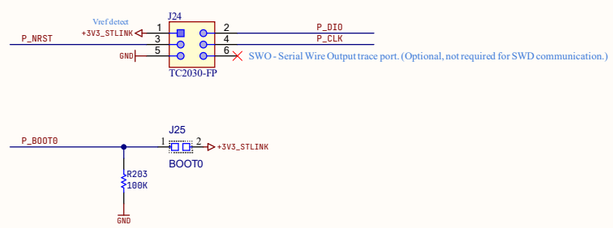
Power



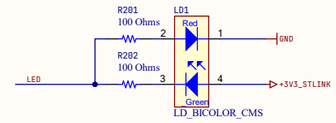
Decoupling



Programming Interface



Two color LED



STLink v2.1

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CHCKD: -			
ENGINEER: Valery		Prj: Xi Aleste Amstrad CPC6128 Replica	
APPR: -	1/8/2023		
MODIFYED DATE:			
SW VERSION: 22.11.1.43		SIZE: A2 / XIA2022	REV: r1.0
		Sheet 21 of 21	
File: D:\projects\hardware\Xi\Aleste_PCB\pcb\st_link.SchDoc			
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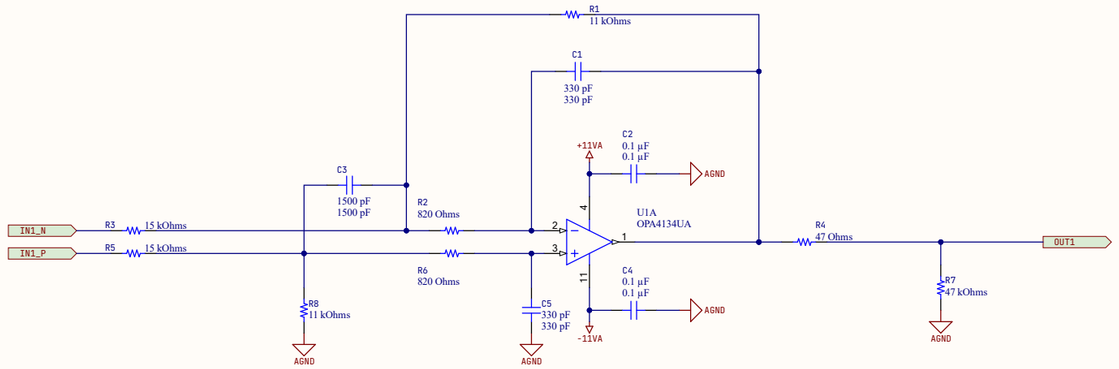

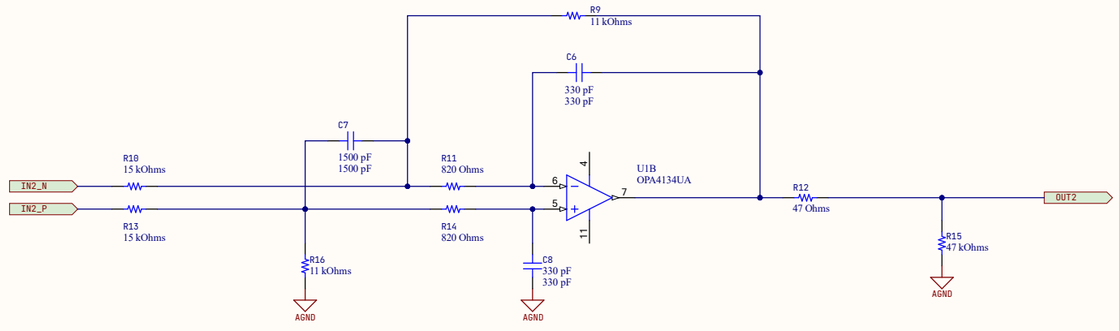

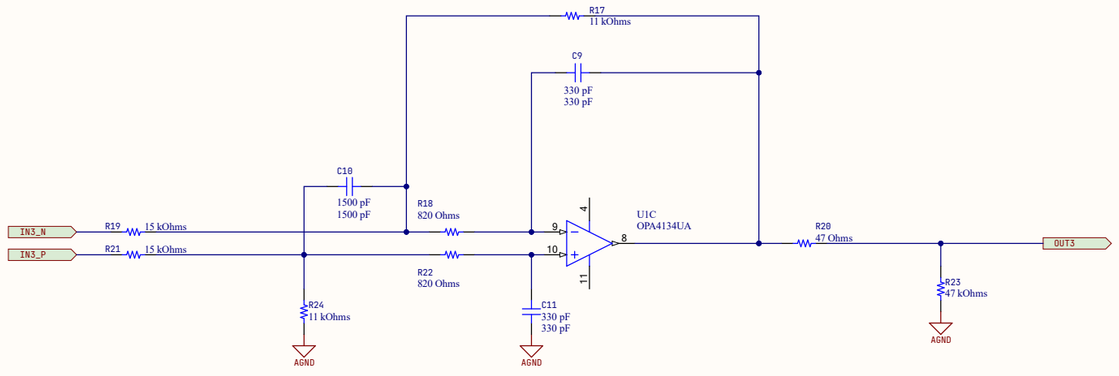

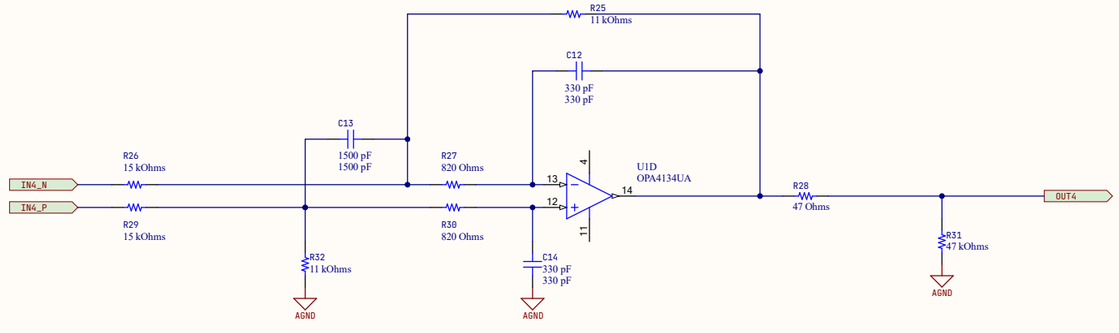

DA Filters

DRAWN BY: Valery (h2w)	DATE: 1/6/2023 2:30:59 PM	H2W Lab *2218 Baker Street* *hww.github.io*	
CHKD: -		Prj: Xi Aleste Amstrad CPC6128 Replica	
ENGINEER: Valery			
APPR: -	1/7/2023		
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		Sheet 23 of 23	

File: D:\projects\hardware\XiAleste_PCB\pcb\dac_filter_v3.SchDoc

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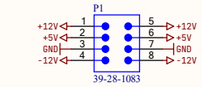
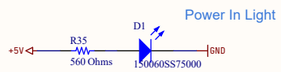
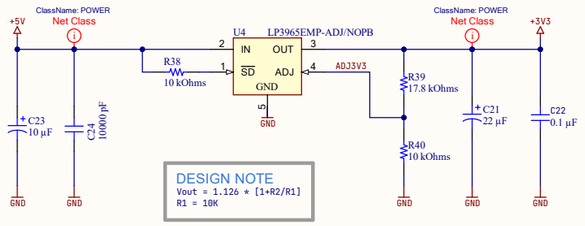
POWER INPUT

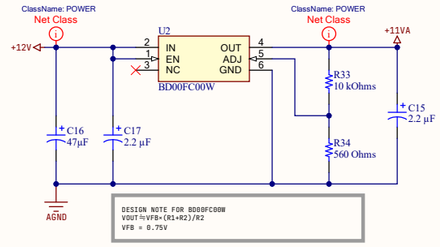


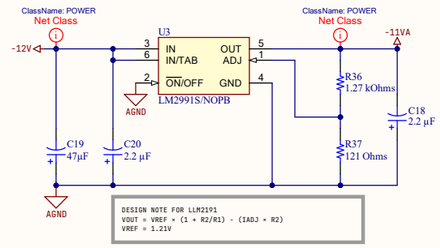


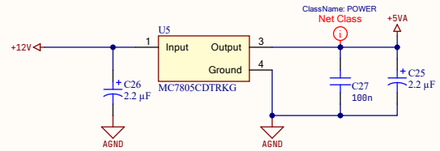
POWER REGULATORS

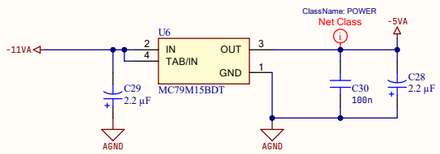


ANALOG POWER

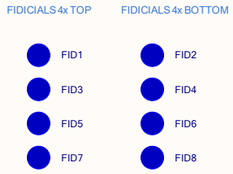




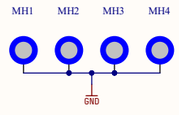




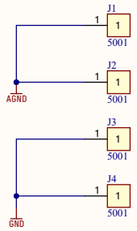
FIDUCIALS



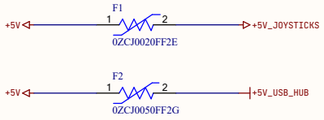
MOUNTING HOLES



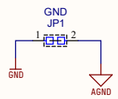
GROUND TEST POINTS



FUSES



GROUNDS CONNECTION



DESIGN NOTES

The main goal of the project is to design a musical version of a computer from the 1980s. This imposes higher power requirements. To power the analog circuits you need a 15V (or 12V) bi-polar supply and a current of about 500mA (15W).The digital circuit requires 5V with a current of 1-2A (10W). The 5V voltage should be maximally (but cheaply) isolated from the analog voltage.

There are two power supplys match to this board:

1) PT-65C (65W) (5, 15, -15) (0.47.0, 0.22.6, 0.00.7)
2) PT-65B (65W) (5, 12, -12) (0.47.0, 0.22.6, 0.00.7)

The second variant requires to decrease +-14V to +-11V.

The board will be powered via a six-wire cable. The ground and +5V will use two wires each and the +15 and -15 will use only one wire.
Approximate pin assignment:

1) +15V
2) +5V
3) +5V
4) Ground
5) Ground
6) -15V

The motherboard should have LDO regulators for +-14V (or +-11V) and for analog +-5V.

The power circuit

DRAWN BY: Valery (h2w)	DATE: 1/8/2023 2:31:00 PM	H2W Lab *2218 Baker Street* *hww.github.io*	
CHKD: -		Prj: Xi Aleste Amstrad CPC6128 Replica	
ENGINEER: Valery			
APPR: -	1/8/2023		
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SW VERSION: 22.11.1.43		SIZE: A2	XIA2022 REV: r1.0
		Sheet * of *	

File: D:\projects\hardware\XiAleste_PCB\pcb\power.SchDoc
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Jumbers and accessories

REF	TYPE	DESCRIPTION	PAGE
SW3	Tactile Button	System reset	expansion_bus
J18	PLS4	Line out	ausio_connectors
SW1	Tactile Button	ESP32 Reset	wifi
SW2	Tactile Button	ESP32 Auxiliary button (Multifunction)	wifi
J21	TC2030-FP	SWD form the main ARM Based DSP	mcu_h750
J32-37	6 x PLS2	The loop back for voice boards (developing board only)	voices
J38	PLS8	SPI connector for the voice controls	voices
J39	PLS4	Auxiliary sound input	voices
J40	PLS4	SPI interface for CV DA Converter	cv_dac
J24	TC2030-FP	SWD for STLink microcontroller	st_link
J25	PLS2	BOOT0 for STLink microcontroller	st_link
D1	LED	Power in LED	power
D13	LED	The line input enabled (slow blink on MUTE)	audio_connectors
D15	LED	WiFi traffic and errors signal	wifi
D20	LED	The multifunctional RGB LED	mcu_h750
D21-D25	LED	The LEDs for SDCard, QuadSPI Flash and auxiliarty A,B,C	mcu_h750
LD1	2 Colors LED	STLink LED	st_link

Connectors

REF	TYPE	DESCRIPTION	PAGE
P1,P2	Mini-Fit	Power in	power
J8	DSUB15	VGA output	vga
J5	HDMI	HDMI output	hdmi
J6,J7	2xUSB	USB connectors	usb_hub
J9	SODIMM	FPGA Module Connector	fpga
J10,J11	DIN5	MIDI Interface	midi
J12-J14	3 x 62POS 2.54 Socket	Expansion bus	expansion_bus
JX1	Edge connector	Amstrad CPC expansion	expansion_cpu
J15	JACK 3.5mm	Headphones	ausio_connectors
J16	Jack 6.35	Line out	ausio_connectors
J17	Jack 6.35	Line in	ausio_connectors
J19-J20	2 x PLD10	Joysticks	joysticks
J26	USB TypeC	ESP32 Firmware Update	wifi
J28	SD Card	Secure Data Card Reader	mcu
J29-J31	3 x PCIe x1	The voice boards expansion bus	voices
J22	USB Type C	ST Link usb connector	st_link

ECO Log

ECO NUMBER	DESCRIPTION	DATE

Signal Glossary TODO

PAGES	DESCRIPTION	PAGES

PAGES	DESCRIPTION	PAGES

Key Components

REF	CHIP	DESCRIPTION	PAGE
U7	TUSB2046BIRHBT	4-Port Full-Speed USB Hub	usb_hub
U11	TPA6120A2DWPR	The headphones amplifier	audio_connectors
U19-U20	PCA9557PWR	Remote 8-Bit I2C and SMBus Low-Power I/O Expander	joysticks
U24	PCM3168APAP	24-bit Multi-channel Audio CODEC 6ch-in/8ch-out	codec
U25	ESP32-C3-MINI-1-N4	RISC V WiFi microcontroller	wifi
U26	STM32H750ZBT6	ARM based DSP	mcu_h750
U27	N25Q128A13ESE40F	128 Mb (x1/x2/x4) Serial NOR Flash Memory with Multi I/O, 108 MHz	mcu_h750
U33	AD5444YRMZ	Single 12-Bit High Bandwidth Multiplying Digital-to-Analog Converter	cv_dac
U21	STM32F103CBT6	Medium-density performance line ARM-based 32-bit MCU with 64KB Flash	st_link
U12-17	SN74AHCT245PWR	Octal bus transceivers with tri-state outputs	expansion_drivers

The title page

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CHCKD: -
ENGINEER: Valery
APPR: - 1/8/2023
MODIFYED DATE:
SW VERSION: 22.11.1.43

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Prj: Xi Aleste
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SIZE: A2 XIA2022 REV: r1.0

Sheet * of *

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