Power MOSFET Basics: Understanding Gate Charge and Using it to Assess Switching Performance

INTRODUCTION

This note is part of a series of application notes that define the fundamental behavior of MOSFETs, both as standalone devices and as switching devices implemented in a Switch Mode Power Supply (SMPS). Vishay Application Note AN-605 [1] provides a basic description of the MOSFET and the terminology behind the device, including definitions and physical structure. AN-850 [2] provides a broad, physical description of the switching process. This application note goes into more detail on the switching behavior of the MOSFET when used in a practical application circuit and attempts to enable the reader / designer to choose the right device for the application using the minimum available information from the datasheet. The note goes through several methods of assessing the switching performance of the MOSFET and compares these methods against practical results. Several definitions used within the text are drawn from application note AN-605.

SWITCHING THE MOSFET IN ISOLATION

Using Capacitance

To get a fundamental understanding of the switching behavior of a MOSFET, it is best first to consider the device in isolation and without any external influences. Under these conditions, an equivalent circuit of the MOSFET gate is illustrated in Fig. 1, where the gate consists of an internal gate resistance (R_g), and two input capacitors (C_{gs} and C_{gd}). With this simple equivalent circuit it is possible to obtain the output voltage response for a step gate voltage.

The voltage V_{GS} is the actual voltage at the gate of the device, and it is this point that should be considered when analyzing the switching behavior. Throughout this note upper case subscripts will refer to rated or applied voltages and currents, while measured or time varying quantities will be designated by lower case subscripts. For example the variable gate drain capacitance is designated as C_{gd} while its corresponding charge will be designated as Q_{GD}.

If a step input is applied at V_{GS}, then the following holds true:

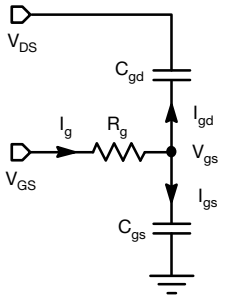

Fig. 1 - An Equivalent MOSFET Gate Circuit Showing Just C_{gs}, C_{gd}, and R_g

$$I_g = \frac{V_{GS} - V_{gs}}{R_g} \quad (1)$$

$$I_g = I_{gs} + I_{gd} \quad (2)$$

$$I_{gs} = C_{gs} \times \frac{dV_{gs}}{dt} \quad (3)$$

Since V_{DS} is fixed

$$I_{gd} = C_{gd} \times \frac{d(V_{gs} - V_{DS})}{dt}$$

$$= C_{gd} \times \frac{dV_{gs}}{dt} \quad (4)$$

$$I_g = \frac{V_{GS} - V_{gs}}{R_g} = I_{gs} + I_{gd}$$

therefore

$$I_g = C_{gs}\frac{dV_{gs}}{dt} + C_{gd}\frac{dV_{gs}}{dt}$$

$$= (C_{gs} + C_{gd})\frac{dV_{gs}}{dt} \quad (5)$$

and

$$\frac{dV_{gs}}{V_{GS} - V_{gs}} = \frac{dt}{R_g \times (C_{gs} + C_{gd})} \quad (6)$$

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giving

$$-\ln(V_{GS} - V_{gs}) = \frac{t}{R_g \times (C_{gs} + C_{gd})} + K \quad (7)$$

$$V_{gs} = V_{GS} - K \times e^{\frac{-t}{R_g \times (C_{gs} + C_{gd})}} \quad (8)$$

at t = 0 s, V_{GS} = 0 V, solving for K,

$$V_{gs} = V_{GS}\left(1 - e^{\frac{-t}{R_g \times (C_{gs} + C_{gd})}}\right) \quad (9)$$

We define two parameters R_G and C_{iss} to simplify the equations. R_G is the effective total gate resistance defined as the sum of internal gate resistance R_g of the MOSFET and any external resistance R_{gext} that is part of the gate drive circuitry. C_{iss} is the effective input capacitance of the MOSFET as seen by the gate drive circuit.

$R_G = R_g + R_{gext}$ and $C_{iss} = C_{gs} + C_{gd}$

Rewriting equation (9) with effective values of gate resistance and capacitance

$$e^{-\frac{t}{R_G C_{iss}}} = 1 - \frac{V_{gs}}{V_{GS}}$$

In most cases the parameter of importance is not the actual gate voltage but the time taken to reach it.

$$t = R_G C_{iss} \times \ln\left(\frac{1}{1 - \frac{V_{gs}}{V_{GS}}}\right) \quad (10)$$

While the RC circuit of Fig. 1 is rather simple, when the MOSFET is considered with additional parasitics, it becomes increasingly difficult to manipulate these equations manually. Therefore a method of analyzing a practical circuit is required. If the second order or parasitic components are ignored, then it is possible to come up with analytical solutions for formulas for the turn-on and turn-off time periods of the MOSFET. These are given in equations (11) through to (16) and the resulting waveforms are shown in Fig. 2 and Fig. 3. These equations are based on those developed in [3], V_{TH} is the MOSFET threshold voltage, and V_{gp} is the gate plateau voltage.

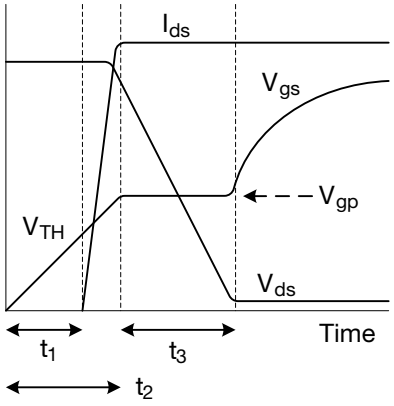

Fig. 2 - Turn-On Transient of the MOSFET

$$t_1 = R_G C_{iss} \times \ln\left(\frac{1}{1 - \frac{V_{TH}}{V_{GS}}}\right) \quad (11)$$

$$t_2 = R_G C_{iss} \times \ln\left(\frac{1}{1 - \frac{V_{gp}}{V_{GS}}}\right) \quad (12)$$

and

$$t_3 = R_G C_{gd} \times \frac{V_{DS}}{V_{GS} - V_{gp}} \quad (13)$$

This gives accurate t_1 and t_2 when using datasheet values, but the time period t_3 is difficult to calculate since C_{gd} changes with V_{ds}. During t_3, gate voltage V_{gs} is constant at V_{gp} and all of the gate current goes to discharge C_{gd} from V_{DS} to almost zero. The drain source voltage across the MOSFET when conducting full load current is considered negligible compared to V_{DS} voltage across the MOSFET when it is off.

Using the same principles for turn-off, the formulas for the switching transients are given below:

$$t_4 = R_G C_{iss} \times \ln\left(\frac{V_{GS}}{V_{gp}}\right) \quad (14)$$

$$t_5 = R_G C_{gd} \times \frac{V_{DS}}{V_{gp}} \quad (15)$$

$$t_6 = R_G C_{iss} \times \ln\left(\frac{V_{gp}}{V_{TH}}\right) \quad (16)$$

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In this instance, t_4 and t_6 can be calculated accurately, but it is the formula for t_5 which is more difficult to solve, since during this time period V_{DS} will change, causing C_{gs} to also change. Therefore some method is required to calculate t_3 and t_5 without using the dynamic C_{gd}.

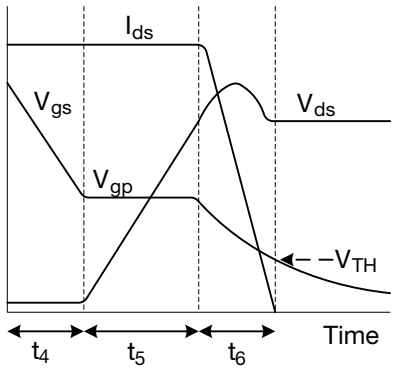

Fig. 3 - Turn-Off Transient of the MOSFET

Using Gate Charge to Determine Switching Time

Looking at the gate charge waveform in Fig. 4, Q_{GS} is defined as the charge from the origin to the start of the Miller Plateau V_{gp}; Q_{GD} is defined as the charge from V_{gp} to the end of the plateau; and Q_G is defined as the charge from the origin to the point on the curve at which the driving voltage V_{GS} equals the actual gate voltage of the device. [4]

The rise in V_{gs} during t_2 (Fig. 2) is brought about by charging C_{gs} and C_{gd}. During this time V_{ds} does not change and as such C_{gd} and C_{ds} stay relatively constant, since they vary as a function of V_{ds}. At this time C_{gs} is generally larger than C_{gd} and therefore the majority of drive current flows into C_{gs} rather than into C_{gd}. This current, through C_{gd} and C_{ds}, depends on the time derivative of the product of the capacitance and its voltage. The gate charge can therefore be assumed to be Q_{GS}. The next part of the waveform is the Miller Plateau. It is generally accepted that the point at which the gate charge figure goes into the plateau region coincides with the peak value of the drain current. However, the knee in the gate charge actually depends on the product (C_{gd} x V_{gd}) with respect to time [4]. This means if there is a small value of drain current and large value of output impedance, then I_{DS} can actually reach its maximum value after the left knee occurs. However, it can be assumed that the maximum value of the current will be close to this knee point and throughout this application note it is assumed that the gate voltage at the knee point corresponds to the load current, I_{DS}.

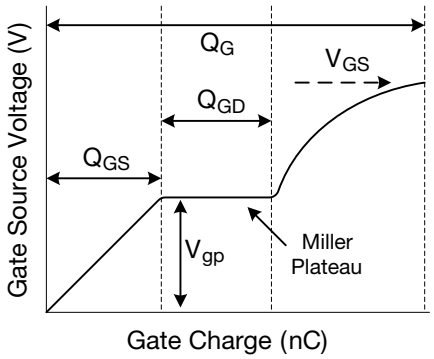

Fig. 4 - Sketch Showing Breakdown of Gate Charge

The slope of the Miller Plateau is generally shown to have a zero, or a near-zero slope, but this gradient depends on the division of drive current between C_{gd} and C_{gs}. If the slope is non-zero then some of the drive current is flowing into C_{gs}. If the slope is zero then all the drive current is flowing into C_{gd}. This happens if the C_{gd} x V_{gd} product increases very quickly and all the drive current is being used to accommodate the change in voltage across C_{gd}. As such, Q_{GD} is the charge injected into the gate during the time the device is in the Miller Plateau.

It should be noted that once the plateau is finished (when V_{ds} reaches its on-state value), C_{gd} becomes constant again and the bulk of the current flows into C_{gs}. The gradient is not as steep as it was in the first period t_2, because C_{gd} is much larger and closer in magnitude to that of C_{gs}.

Combination of Gate Charge and Capacitance to Obtain Switching Times

The objective of this note is to use datasheet values to predict the switching times of the MOSFET and hence allow the estimation of switching losses. Since it is the time from the end of t_1 to the end of t_3 that causes the turn-on loss, it is necessary to obtain this time (Fig. 2). Combining 11 and 12 it is possible to obtain the rise time of the current ($t_{ir} = t_2 - t_1$) and because V_{ds} stays constant during this time then it is possible to use the specified datasheet value of C_{iss} at the appropriate V_{DS} value.

$$t_{ir} = t_2 - t_1$$

$$= R_G C_{iss\ at\ V_{DS}} \times \ln\left(\frac{V_{GS} - V_{TH}}{V_{GS} - V_{gp}}\right) \quad (17)$$

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It is often stated in the literature that $V_{TH} + I_{DS}/g_{fs}$ can be substituted for V_{gp}. While technically correct, the users should be aware that transconductance is not constant but varies with load. The datasheet value for V_{TH} is specified at a low value of I_{DS}, at which the V_{gp} tends to be higher than the calculated value. Using the value of V_{gp} from the gate charge curves is recommended for accurate results.

It is difficult to use a value of C_{gd} for the fall time period of V_{ds} ($t_{vf} = t_3$). Therefore if the datasheet value of gate charge Q_{GD} is used and divided by the voltage swing seen on the drain connection V_{DS} then this effectively gives a value for C_{gd} based on the datasheet transient.

$$t_{vf} = t_3 = R_G \times \frac{Q_{GD(D)}}{V_{DS(D)}} \times \frac{V_{DS}}{(V_{GS} - V_{gp})} \quad (18)$$

Similarly for the turn-off transition, the voltage rise time ($t_{vr} = t_5$) is:

$$t_{vr} = t_5 = R_G \times \frac{Q_{GD(D)}}{V_{DS(D)}} \times \frac{V_{DS}}{V_{gp}} \quad (19)$$

The current fall time ($t_{if} = t_6$) is:

$$t_{ir} = t_6 = R_G C_{iss\ at\ V_{DS}} \times \ln\left(\frac{V_{gp}}{V_{TH}}\right) \quad (20)$$

TABLE 1 - WORKED EXAMPLE FOR SWITCHING TRANSIENTS: SiRA04DP

MOSFET PARAMETERS	MIN.	TYP.	MAX.	UNIT
$V_{DS(D)}$	13.5	15	16.5	V
$I_{DS(D)}$	9	10	11	A
$R_{DS(on)}$	1.45	1.8	2.15	mΩ
V_{TH}	1.1	1.7	2.2	V
V_{gp}	2.4	2.6	2.8	
C_{iss} at V_{DS}	2880	3600	4320	pF
C_{iss} at 0 V	3200	4000	4800	
Q_{GD}	3	4	5	nC
R_g	0.3	1.3	2.5	Ω
g_{fs}	80	100	120	S
Datasheet Values for Switching Times				
$t_{d(on)}$	-	12	24	ns
t_r	-	10	20	
$t_{d(off)}$	-	30	60	
t_f	-	8	16	

Comparing Equations with Datasheet Values

The definition of the turn-on and turn-off times given in the datasheet can be seen in Fig. 5. These definitions can be equated to the equations described above and are shown here:

$$t_{d(on)} \cong t_1 + t_{ir} \quad (21)$$

$$t_r \cong t_{vf} \quad (22)$$

$$t_{d(off)} \cong t_4 \quad (23)$$

$$t_f \cong t_{vr} \quad (24)$$

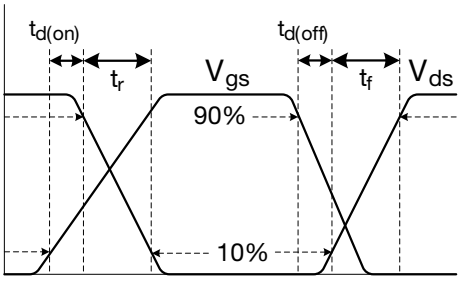

Fig. 5 - Sketch Showing Definition of Turn-On and Turn-Off Times

TABLE 2 - MEASUREMENT OF SWITCHING TRANSIENT: SiRA04DP

Circuit Conditions				
V_{DS}	10.5	12	13.5	V
V_{GS}	4.5	5	5.5	
I_{DS}	14	15	16	A
R_{gext}	340	350	360	Ω
Calculations				
t_1 (equation 11)	275	526	800	ns
t_{ir} (equation 17)	197	403	755	
t_{vf} (equation 18)	378	469	549	
t_4 (equation 14)	685	919	1175	
t_{vr} (equation 19)	331	433	530	
t_{if} (equation 20)	236	538	1222	
$t_{d(on)}$ (= $t_1 + t_{ir}$)	472	929	1555	
t_r (= t_{vf})	378	469	549	
$t_{d(off)}$ (= t_4)	685	919	1175	
t_f (= t_{vr})	331	433	530	
Measured Values				
t_{ir}	-	330	-	ns
t_{vf}	-	560	-	
t_{vr}	-	648	-	
t_{if}	-	250	-	

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Comparing Equations with Measured Switching Transients

The datasheet switching transients are measured with a resistive load and are not truly representative of a practical circuit. As such the device will not behave according to the ideal operation described above. Therefore, calculations were done for actual circuit conditions shown below. For purposes of illustration, a large value of R_{gext} is selected here to deliberately slow down the switching transient. The aim is to reduce excessive ringing in the waveforms and measure the rise and fall times more accurately.

V_{DS} = 12 V, I_{DS} = 15 A, V_{GS} = 5 V, and R_{gext} = 350 Ω

The minimum switching transients were calculated using the appropriate value of the parameters, which resulted in producing the shortest switching transient value. In some circumstances this meant that the maximum value of a parameter was used to calculate the minimum switching transient and vice versa for the maximum switching transients.

Actual switching waveforms were measured, and these are shown in Fig. 6 and Fig. 7. These switching transients are for the SiRA04 turned on and off with an inductive load. The voltage fall time t_{vf} was measured starting from the time current reached the peak I_{DS}. The dip prior to current peak is the di/dt drop in the parasitic inductances of the circuit and should be excluded from the voltage fall time.

Table 2 also shows the comparison between the calculations and the measured transients. It is seen that the measured voltage transients are relatively on the higher side while the current rise and fall times are lower than calculated. While there is good agreement between calculated and measured transients for voltage, the difference for current transients is wider. The differences are also more pronounced at turn off

The current transients were calculated using V_{TH} which is based on a low I_{DS} value of 250 µA. The oscilloscope measurements lack the resolution to make measurements at that level. For switching loss calculations, the extra time interval may be ignored as the current is quite low.

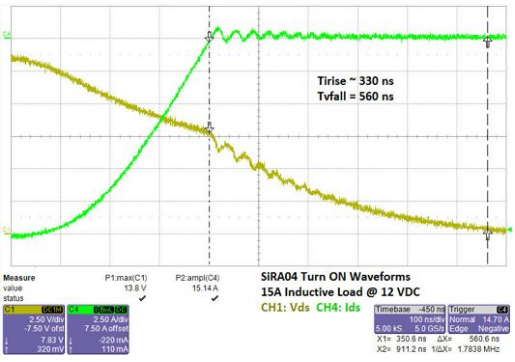

Fig. 6 - Measured Current and Voltage Turn-On Switching Transient

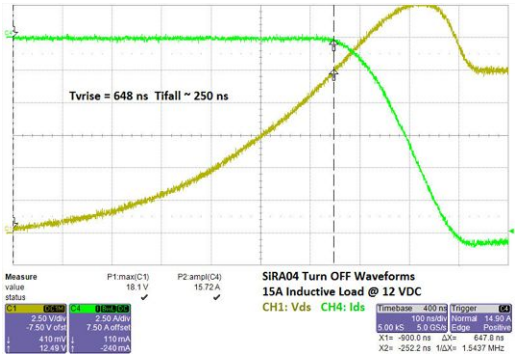

Fig. 7 - Measured Current and Voltage Turn-Off Switching Transient

Limitations of the Driving Circuit

The switching times of the MOSFET are affected not only by the parasitic elements, but also by the driving circuit. Under the conditions described above, it was assumed that the gate circuit does not limit the switching performance of the power MOSFET. For example, with a MOSFET p-channel and n-channel driver, it is possible that the theoretical current into the gate will be larger than that which the driver is able to supply. There are several ways in which a MOSFET driver can be realized and this goes beyond the study of this application note. The formulas described in the text are used to gauge the switching times and therefore estimate the switching losses without navigating complex formulas, models, and expensive simulation software. However, large discrepancies between the calculated and the measured current transients can also occur because the calculations assume an ideal situation with respect to source inductance of the package. Therefore, further consideration has to be taken for the current rise and fall times, and this is described below.

Current Transients

One major parameter that should be considered into the equations is the package inductance of the MOSFET. This will slow the current transient and can be taken into account with relative ease if a few assumptions are made. Since the load current will generally be much larger than the gate current, it is assumed that all the current through the package inductance will be I_{DS}. Therefore it can be shown that the voltage across the package inductance of the MOSFET during turn-on will be:

$$V_{src} = L_{src}\frac{\Delta I_{DS}}{\Delta t} = \frac{g_{fs}L_{src}}{R_G C_{iss\ at\ V_{DS}}} \times$$

$$(V_{GS} - V_{TH}) \times \left(1 - e^{-\frac{t}{R_G C_{iss\ at\ V_{DS}}}}\right) \qquad (25)$$

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This is the voltage that occurs from the current transient and as such subtracts from the gate voltage and hence slows down the current transient. It has been shown in [5] that there is an upper limit to V_{src}, given by V_{TH}.

In the test set up, source inductance was kept to the minimum with good routing practices, and also a large value of R_{gext} was used for illustration purposes. Therefore, source inductance drop and its influence on current rise and fall times are not significant. However, in real applications with low gate resistances, effects of V_{src} need to be taken into account as explained below.

If equation 25 is subtracted from V_{GS} and solved for time, the t_{ir} transient duration is:

$$t_{ir} = R_G C_{iss\ at\ V_{DS}} \times \ln\left[\left(1 + \frac{g_{fs} L_{src}}{R_G C_{iss\ at\ V_{DS}}}\right) \times \frac{V_{GS} - V_{TH}}{V_{GS} - V_{gp}}\right] \quad (26)$$

Applying the same principle for t_{if} results in a current transient as follows:

$$t_{if} = R_G C_{iss\ at\ V_{DS}} \times \ln\left[\left(1 + \frac{g_{fs} L_{src}}{R_G C_{iss\ at\ V_{DS}}}\right) \times \frac{V_{GP}}{V_{TH}}\right] \quad (27)$$

CONCLUSION

This application note shows good approximations for the rise and fall times of the power MOSFET, when evaluated in isolation. Datasheet values for the formulas derived can be used to get a reasonable indication of the switching performance of the MOSFET as well as the switching losses. However, as illustrated in Fig. 2 and Fig. 3, the ideal switching transients will always be shorter than those actually achieved, so the maximum parameters from the datasheet should always be used to give realistic results.

REFERENCES

1. Vishay AN-605, “Power MOSFET Basics: Understanding MOSFET Characteristics” www.vishay.com/doc?71933
2. Vishay AN-850, “Power MOSFET Basics: Understanding the Turn ON Process.” www.vishay.com/doc?68214
3. B. J. Baliga, “Power Semiconductor Devices”
4. “Gate Charge Principles and Usage”, Power Electronics Technology Europe. Issue 3, 2002.
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