Zynq-7000 All Programmable SoC (Z-7030, Z-7035, Z-7045, and Z-7100): DC and AC Switching Characteristics

DS191 (v1.17) November 24, 2015 **Product Specification**

Introduction

The Zynq®-7000 All Programmable SoCs are available in -3, -2, -2LI, -1, and -1LQ speed grades, with -3 having the highest performance. The -2LI devices operate at programmable logic (PL) V_{CCINT}/V_{CCBRAM} = 0.95V and are screened for lower maximum static power. The speed specification of a -2LI device is the same as that of a -2 device. The -1LQ devices operate at the same voltage and speed as the -1Q devices and are screened for lower power. Zynq-7000 device DC and AC characteristics are specified in commercial, extended, industrial, and expanded (Q-temp) temperature ranges. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1 speed grade industrial device are the same as for a -1 speed grade commercial device). However, only selected speed grades and/or devices are available in the commercial, extended, or industrial temperature ranges.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

The available device/package combinations are outlined in:

- Zynq-7000 All Programmable SoC Overview (DS190)
- Defense-grade Zynq-7000Q All Programmable SoC Overview (DS196)
- XA Zynq-7000 All Programmable SoC Overview (DS188)

This Zynq-7000 AP SoC data sheet, which covers the specifications for the XC7Z030, XA7Z030, XQ7Z030, XC7Z035, XC7Z045, XQ7Z045, XC7Z100, and XQ7Z100 complements the Zynq-7000 AP SoC documentation suite available on the Xilinx website at www.xilinx.com/zynq.

DC Characteristics

Table 1: **Absolute Maximum Ratings** (1)

Symbol	Description	Min	Max	Units
Processing System (PS)				
V_{CCPINT}	PS internal logic supply voltage	–0.5	1.1	V
V_{CCPAUX}	PS auxiliary supply voltage	–0.5	2.0	V
V_{CCPLL}	PS PLL supply	–0.5	2.0	V
V_{CCO_DDR}	PS DDR I/O supply	–0.5	2.0	V
V_{CCO_MIO} (2)	PS MIO I/O supply	–0.5	3.6	V
V_{PREF}	PS input reference voltage	–0.5	2.0	V
V_{PIN} (2)(3)(4)(5)	PS MIO I/O input voltage	–0.40	V_{CCO_MIO} + 0.55	V
	PS DDR I/O input voltage	–0.55	V_{CCO_DDR} + 0.55	V
Programmable Logic (PL)				
V_{CCINT}	PL internal supply voltage	–0.5	1.1	V
V_{CCBRAM}	PL supply voltage for the block RAM memories	–0.5	1.1	V
V_{CCAUX}	PL auxiliary supply voltage	–0.5	2.0	V
V_{CCO}	PL output drivers supply voltage for HR I/O banks	–0.5	3.6	V
	PL output drivers supply voltage for HP I/O banks	–0.5	2.0	V
V_{CCAUX_IO} (4)	Auxiliary supply voltage	–0.5	2.06	V

Table 1: **Absolute Maximum Ratings (1) *(Cont'd)***

Symbol	Description	Min	Max	Units
V_{REF}	Input reference voltage	–0.5	2.0	V
V_{IN}(3)(4)(5)	I/O input voltage for HR I/O banks	–0.40	V_{CCO} + 0.55	V
	I/O input voltage for HP I/O banks	–0.55	V_{CCO} + 0.55	V
	I/O input voltage (when V_{CCO} = 3.3V) for V_{REF} and differential I/O standards except TMDS_33(6)	–0.40	2.625	V
V_{CCBATT}	Key memory battery backup supply	–0.5	2.0	V
GTX Transceiver				
$V_{MGTAVCC}$	Analog supply voltage for the GTX transmitter and receiver circuits	–0.5	1.1	V
$V_{MGTAVTT}$	Analog supply voltage for the GTX transmitter and receiver termination circuits	–0.5	1.32	V
$V_{MGTVCCAUX}$	Auxiliary analog Quad PLL (QPLL) voltage supply for the GTX transceivers	–0.5	1.935	V
$V_{MGTREFCLK}$	GTX transceiver reference clock absolute input voltage	–0.5	1.32	V
$V_{MGTAVTTRCAL}$	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	–0.5	1.32	V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	–0.5	1.26	V
$I_{DCIN-FLOAT}$	DC input current for receiver input pins DC coupled RX termination = floating	–	14	mA
$I_{DCIN-MGTAVTT}$	DC input current for receiver input pins DC coupled RX termination = $V_{MGTAVTT}$	–	12	mA
$I_{DCIN-GND}$	DC input current for receiver input pins DC coupled RX termination = GND	–	6.5	mA
$I_{DCOUT-FLOAT}$	DC output current for transmitter pins DC coupled RX termination = floating	–	14	mA
$I_{DCOUT-MGTAVTT}$	DC output current for transmitter pins DC coupled RX termination = $V_{MGTAVTT}$	–	12	mA
XADC				
V_{CCADC}	XADC supply relative to GNDADC	–0.5	2.0	V
V_{REFP}	XADC reference input relative to GNDADC	–0.5	2.0	V
Temperature				
T_{STG}	Storage temperature (ambient)	–65	150	°C
T_{SOL}	Maximum soldering temperature for Pb/Sn component bodies(7)	–	+220	°C
	Maximum soldering temperature for Pb-free component bodies(7)	–	+260	°C
T_j	Maximum junction temperature(7)	–	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. Applies to both MIO supply banks V_{CCO_MIO0} and V_{CCO_MIO1}.
3. The lower absolute voltage specification always applies.
4. For I/O operation, refer to the *7 Series FPGAs SelectIO Resources User Guide* (UG471) or the *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585).
5. The maximum limit applies to DC signals. For maximum undershoot and overshoot AC specifications, see Table 4 and Table 5.
6. See Table 12 for TMDS_33 specifications.
7. For soldering guidelines and thermal considerations, see the *Zynq-7000 All Programmable SoC Packaging and Pinout Specification* (UG865).

Table 2: **Recommended Operating Conditions (1)(2)**

Symbol	Description	Min	Typ	Max	Units
PS					
V_{CCPINT}(3)	PS internal logic supply voltage	0.95	1.00	1.05	V
V_{CCPAUX}	PS auxiliary supply voltage	1.71	1.80	1.89	V
V_{CCPLL}	PS PLL supply voltage	1.71	1.80	1.89	V
V_{CCO_DDR}	PS DDR supply voltage	1.14	–	1.89	V
V_{CCO_MIO}(4)	PS supply voltage for MIO banks	1.71	–	3.465	V
V_{PIN}(5)	PS DDR and MIO I/O input voltage	–0.20	–	V_{CCO_DDR} + 0.20 V_{CCO_MIO} + 0.20	V
PL					
V_{CCINT}(6)	PL internal supply voltage	0.97	1.00	1.03	V
	PL -2LI (0.95V) internal supply voltage	0.93	0.95	0.97	V
V_{CCBRAM}(6)	PL block RAM supply voltage	0.97	1.00	1.03	V
	PL -2LI (0.95V) block RAM supply voltage	0.93	0.95	0.97	V
V_{CCAUX}	PL auxiliary supply voltage	1.71	1.80	1.89	V
V_{CCO}(7)(8)	PL supply voltage for HR I/O banks	1.14	–	3.465	V
	PL supply voltage for HP I/O banks	1.14	–	1.89	V
V_{CCAUX_IO}(9)	PL auxiliary supply voltage when set to 1.8V	1.71	1.80	1.89	V
	PL auxiliary supply voltage when set to 2.0V	1.94	2.00	2.06	V
V_{IN}(5)	I/O input voltage	–0.20	–	V_{CCO} + 0.20	V
	I/O input voltage (when V_{CCO} = 3.3V) for V_{REF} and differential I/O standards except TMDS_33(10)	–0.20	–	2.625	V
I_{IN}(11)	Maximum current through any (PS or PL) pin in a powered or unpowered bank when forward biasing the clamp diode	–	–	10	mA
V_{CCBATT}(12)	Battery voltage	1.0	–	1.89	V
GTX Transceiver					
$V_{MGTAVCC}$(13)	Analog supply voltage for the GTX transceiver QPLL frequency range ≤ 10.3125 GHz(14)(15)	0.97	1.0	1.08	V
	Analog supply voltage for the GTX transceiver QPLL frequency range > 10.3125 GHz	1.02	1.05	1.08	
$V_{MGTAVTT}$(13)	Analog supply voltage for the GTX transmitter and receiver termination circuits	1.17	1.2	1.23	V
$V_{MGTVCCAUX}$(13)	Auxiliary analog QPLL voltage supply for the transceivers	1.75	1.80	1.85	V
$V_{MGTAVTTRCAL}$(13)	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	1.17	1.2	1.23	V
XADC					
V_{CCADC}	XADC supply relative to GNDADC	1.71	1.80	1.89	V
V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V

Table 2: **Recommended Operating Conditions (1)(2) *(Cont'd)***

Symbol	Description	Min	Typ	Max	Units
Temperature					
T_j	Junction temperature operating range for commercial (C) temperature devices	0	–	85	°C
	Junction temperature operating range for extended (E) temperature devices	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices	–40	–	100	°C
	Junction temperature operating range for expanded (Q) temperature devices	–40	–	125	°C

Notes:

1. All voltages are relative to ground. The PL and PS share a common ground.
2. For the design of the power distribution system consult the *Zynq-7000 All Programmable SoC PCB Design Guide* (UG933).
3. When the processor cores operate $F_{CPU\_6X4X\_621\_MAX}$ at 1 GHz (-3E speed grade) or when the DDR interface operates at 1333 Mb/s, the V_{CCPINT} minimum is 0.97V and the V_{CCPINT} maximum is 1.03V.
4. Applies to both MIO supply banks V_{CCO_MIO0} and V_{CCO_MIO1}.
5. The lower absolute voltage specification always applies.
6. V_{CCINT} and V_{CCBRAM} should be connected to the same supply.
7. Configuration data is retained even if V_{CCO} drops to 0V.
8. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V at ±5%.
9. For more information, refer to the V_{CCAUX_IO} section of the *7 Series FPGAs SelectIO Resources User Guide* (UG471) or the *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585).
10. See Table 12 for TMDS_33 specifications.
11. A total of 200 mA per PS or PL bank should not be exceeded.
12. V_{CCBATT} is required only when using bitstream encryption. If battery is not used, connect V_{CCBATT} to either ground or V_{CCAUX}.
13. Each voltage listed requires the filter circuit described in the *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476).
14. For data rates ≤ 10.3125 Gb/s, $V_{MGTAVCC}$ should be 1.0V ±3% for lower power consumption.
15. For lower power consumption, $V_{MGTAVCC}$ should be 1.0V ±3% over the entire CPLL frequency range.

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Min	Typ[1]	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.75	–	–	V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	1.5	–	–	V
I_{REF}	PS_DDR_VREF 0/1, PS_MIO_VREF, and V_{REF} leakage current per pin	–	–	15	µA
I_L	Input or output leakage current per pin (sample-tested)	–	–	15	µA
C_{IN}[2]	PL die input capacitance at the pad	–	–	8	pF
C_{PIN}[2]	PS die input capacitance at the pad	–	–	8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 3.3V	90	–	330	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 2.5V	68	–	250	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.8V	34	–	220	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.5V	23	–	150	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.2V	12	–	120	µA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 3.3V	68	–	330	µA
	Pad pull-down (when selected) @ V_{IN} = 1.8V	45	–	180	µA
I_{CCADC}	Analog supply current, analog circuits in powered up state	–	–	25	mA
I_{BATT}[3]	Battery supply current	–	–	150	nA
R_{IN_TERM}[4]	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_40)	28	40	55	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_50)	35	50	65	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_60)	44	60	83	Ω
n	Temperature diode ideality factor	–	1.010	–	–
r	Temperature diode series resistance	–	2	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. Termination resistance to a V_{CCO}/2 level.

Table 4: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for PS I/O and PL HR I/O Banks(1)(2)**

AC Voltage Overshoot	% of UI @–40°C to 125°C	AC Voltage Undershoot	% of UI @–40°C to 125°C
V_{CCO} + 0.55	100	–0.40	100
		–0.45	61.7
		–0.50	25.8
		–0.55	11.0
V_{CCO} + 0.60	46.6	–0.60	4.77
V_{CCO} + 0.65	21.2	–0.65	2.10
V_{CCO} + 0.70	9.75	–0.70	0.94
V_{CCO} + 0.75	4.55	–0.75	0.43
V_{CCO} + 0.80	2.15	–0.80	0.20
V_{CCO} + 0.85	1.02	–0.85	0.09
V_{CCO} + 0.90	0.49	–0.90	0.04
V_{CCO} + 0.95	0.24	–0.95	0.02

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. The peak voltage of the overshoot or undershoot, and the duration above V_{CCO} + 0.20V or below GND – 0.20V, must not exceed the values in this table.

Table 5: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for PL HP I/O Banks(1)(2)**

AC Voltage Overshoot	% of UI at –40°C to 125°C	AC Voltage Undershoot	% of UI at –40°C to 125°C
V_{CCO} + 0.55	100	–0.55	100
V_{CCO} + 0.60	50.0(3)	–0.60	50.0(3)
V_{CCO} + 0.65	50.0(3)	–0.65	50.0(3)
V_{CCO} + 0.70	47.0	–0.70	50.0(3)
V_{CCO} + 0.75	21.2	–0.75	50.0(3)
V_{CCO} + 0.80	9.71	–0.80	50.0(3)
V_{CCO} + 0.85	4.51	–0.85	28.4
V_{CCO} + 0.90	2.12	–0.90	12.7
V_{CCO} + 0.95	1.01	–0.95	5.79

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. The peak voltage of the overshoot or undershoot, and the duration above V_{CCO} + 0.20V or below GND – 0.20V, must not exceed the values in this table.
3. For UI lasting less than 20 µs.

Table 6: **Typical Quiescent Supply Current**

Symbol	Description	Device	Speed Grade								Units
			-3E	-2E	-2I	-2LI	-1C	-1I	-1Q	-1LQ	
$I_{CCPINTQ}$	PS quiescent V_{CCPINT} supply current	XC7Z030	122	122	122	79	122	122	N/A	N/A	mA
		XC7Z035	122	122	122	79	122	122	N/A	N/A	mA
		XC7Z045	122	122	122	79	122	122	N/A	N/A	mA
		XC7Z100	N/A	N/A	122	79	N/A	122	N/A	N/A	mA
		XA7Z030	N/A	N/A	N/A	N/A	N/A	122	122	N/A	mA
		XQ7Z030	N/A	N/A	122	79	N/A	122	122	N/A	mA
		XQ7Z045	N/A	N/A	122	79	N/A	122	122	122	mA
		XQ7Z100	N/A	N/A	122	79	N/A	122	N/A	N/A	mA
$I_{CCPAUXQ}$	PS quiescent V_{CCPAUX} supply current	XC7Z030	13	13	13	11	13	13	N/A	N/A	mA
		XC7Z035	13	13	13	11	13	13	N/A	N/A	mA
		XC7Z045	13	13	13	11	13	13	N/A	N/A	mA
		XC7Z100	N/A	N/A	13	11	N/A	13	N/A	N/A	mA
		XA7Z030	N/A	N/A	N/A	N/A	N/A	13	13	N/A	mA
		XQ7Z030	N/A	N/A	13	11	N/A	13	13	N/A	mA
		XQ7Z045	N/A	N/A	13	11	N/A	13	13	13	mA
		XQ7Z100	N/A	N/A	13	11	N/A	13	N/A	N/A	mA
I_{CCDDRQ}	PS quiescent V_{CCO_DDR} supply current	XC7Z030	4	4	4	4	4	4	N/A	N/A	mA
		XC7Z035	4	4	4	4	4	4	N/A	N/A	mA
		XC7Z045	4	4	4	4	4	4	N/A	N/A	mA
		XC7Z100	N/A	N/A	4	4	N/A	4	N/A	N/A	mA
		XA7Z030	N/A	N/A	N/A	N/A	N/A	4	4	N/A	mA
		XQ7Z030	N/A	N/A	4	4	N/A	4	4	N/A	mA
		XQ7Z045	N/A	N/A	4	4	N/A	4	4	4	mA
		XQ7Z100	N/A	N/A	4	4	N/A	4	N/A	N/A	mA
I_{CCINTQ}	PL quiescent V_{CCINT} supply current	XC7Z030	246	246	246	141	246	246	N/A	N/A	mA
		XC7Z035	611	611	611	351	611	611	N/A	N/A	mA
		XC7Z045	611	611	611	351	611	611	N/A	N/A	mA
		XC7Z100	N/A	N/A	795	457	N/A	795	N/A	N/A	mA
		XA7Z030	N/A	N/A	N/A	N/A	N/A	246	246	N/A	mA
		XQ7Z030	N/A	N/A	246	141	N/A	246	246	N/A	mA
		XQ7Z045	N/A	N/A	611	351	N/A	611	611	611	mA
		XQ7Z100	N/A	N/A	795	457	N/A	795	N/A	N/A	mA

Table 6: **Typical Quiescent Supply Current *(Cont'd)***

Symbol	Description	Device	Speed Grade								Units
			-3E	-2E	-2I	-2LI	-1C	-1I	-1Q	-1LQ	
I_{CCAUXQ}	PL quiescent V_{CCAUX} supply current	XC7Z030	56	56	56	50	56	56	N/A	N/A	mA
		XC7Z035	131	131	131	117	131	131	N/A	N/A	mA
		XC7Z045	131	131	131	117	131	131	N/A	N/A	mA
		XC7Z100	N/A	N/A	165	148	N/A	165	N/A	N/A	mA
		XA7Z030	N/A	N/A	N/A	N/A	N/A	56	56	N/A	mA
		XQ7Z030	N/A	N/A	56	50	N/A	56	56	N/A	mA
		XQ7Z045	N/A	N/A	131	117	N/A	131	131	131	mA
		XQ7Z100	N/A	N/A	165	148	N/A	165	N/A	N/A	mA
I_{CCAUX_IOQ}	PL quiescent V_{CCAUX_IO} supply current	XC7Z030	2	2	2	1	2	2	N/A	N/A	mA
		XC7Z035	2	2	2	1	2	2	N/A	N/A	mA
		XC7Z045	2	2	2	1	2	2	N/A	N/A	mA
		XC7Z100	N/A	N/A	2	1	N/A	2	N/A	N/A	mA
		XA7Z030	N/A	N/A	N/A	N/A	N/A	2	2	N/A	mA
		XQ7Z030	N/A	N/A	2	1	N/A	2	2	N/A	mA
		XQ7Z045	N/A	N/A	2	1	N/A	2	2	2	mA
		XQ7Z100	N/A	N/A	2	1	N/A	2	N/A	N/A	mA
I_{CCOQ}	PL quiescent V_{CCO} supply current	XC7Z030	4	4	4	4	4	4	N/A	N/A	mA
		XC7Z035	4	4	4	4	4	4	N/A	N/A	mA
		XC7Z045	4	4	4	4	4	4	N/A	N/A	mA
		XC7Z100	N/A	N/A	4	4	N/A	4	N/A	N/A	mA
		XA7Z030	N/A	N/A	N/A	N/A	N/A	4	4	N/A	mA
		XQ7Z030	N/A	N/A	4	4	N/A	4	4	N/A	mA
		XQ7Z045	N/A	N/A	4	4	N/A	4	4	4	mA
		XQ7Z100	N/A	N/A	4	4	N/A	4	N/A	N/A	mA
$I_{CCBRAMQ}$	PL quiescent V_{CCBRAM} supply current	XC7Z030	11	11	11	6	11	11	N/A	N/A	mA
		XC7Z035	23	23	23	13	23	23	N/A	N/A	mA
		XC7Z045	23	23	23	13	23	23	N/A	N/A	mA
		XC7Z100	N/A	N/A	33	19	N/A	33	N/A	N/A	mA
		XA7Z030	N/A	N/A	N/A	N/A	N/A	11	11	N/A	mA
		XQ7Z030	N/A	N/A	11	6	N/A	11	11	N/A	mA
		XQ7Z045	N/A	N/A	23	13	N/A	23	23	23	mA
		XQ7Z100	N/A	N/A	33	19	N/A	33	N/A	N/A	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to estimate static power consumption for conditions other than those specified.

PS Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCPINT}, V_{CCPAUX}, and V_{CCPLL} together, then the PS V_{CCO} supplies (V_{CCO_MIO0}, V_{CCO_MIO1}, and V_{CCO_DDR}) to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The PS_POR_B input is required to be asserted to GND during the power-on sequence until V_{CCPINT}, V_{CCPAUX} and V_{CCO_MIO0} have reached minimum operating levels to ensure PS eFUSE integrity. For additional information about PS_POR_B timing requirements refer to Resets.

The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCPAUX}, V_{CCPLL}, and the PS V_{CCO} supplies (V_{CCO_MIO0}, V_{CCO_MIO1}, and V_{CCO_DDR}) have the same recommended voltage levels, then they can be powered by the same supply and ramped simultaneously. Xilinx recommends powering V_{CCPLL} with the same supply as V_{CCPAUX}, with an optional ferrite bead filter. Before V_{CCPINT} reaches 0.80V at least one of the four following conditions is required during the power-off stage: the PS_POR_B input is asserted to GND, the reference clock to the PS_CLK input is disabled, V_{CCPAUX} is lower than 0.70V, or V_{CCO_MIO0} is lower than 0.90V. The condition must be held until V_{CCPINT} reaches 0.40V to ensure PS eFUSE integrity.

For V_{CCO_MIO0} and V_{CCO_MIO1} voltages of 3.3V:

- The voltage difference between V_{CCO_MIO0} /V_{CCO_MIO1} and V_{CCPAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

PL Power-On/Off Power Supply Sequencing

The recommended power-on sequence for the PL is V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, V_{CCAUX_IO}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX}, V_{CCAUX_IO}, and V_{CCO} have the same recommended voltage levels then they can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

The recommended power-on sequence to achieve minimum current draw for the GTX transceivers is V_{CCINT}, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT}, $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

- When $V_{MGTAVTT}$ is powered before $V_{MGTAVCC}$ and $V_{MGTAVTT} - V_{MGTAVCC} > 150$ mV and $V_{MGTAVCC} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 460 mA per transceiver during $V_{MGTAVCC}$ ramp up. The duration of the current draw can be up to 0.3 x $T_{MGTAVCC}$ (ramp time from GND to 90% of $V_{MGTAVCC}$). The reverse is true for power-down.
- When $V_{MGTAVTT}$ is powered before V_{CCINT} and $V_{MGTAVTT} - V_{CCINT} > 150$ mV and $V_{CCINT} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 50 mA per transceiver during V_{CCINT} ramp up. The duration of the current draw can be up to 0.3 x T_{VCCINT} (ramp time from GND to 90% of V_{CCINT}). The reverse is true for power-down.

There is no recommended sequence for supplies not shown.

PS—PL Power Sequencing

The PS and PL power supplies are fully independent. PS power supplies (V_{CCPINT}, V_{CCPAUX}, V_{CCPLL}, V_{CCO_DDR}, V_{CCO_MIO0}, and V_{CCO_MIO1}) can be powered before or after any PL power supplies. The PS and PL power regions are isolated to prevent damage.

Power Supply Requirements

Table 7 shows the minimum current, in addition to I_{CCQ}, that is required by Zynq-7000 devices for proper power-on and configuration. If the current minimums shown in Table 6 and Table 7 are met, the device powers on after all five supplies have passed through their power-on reset threshold voltages. The Zynq-7000 device must not be configured until after V_{CCINT} is applied. Once initialized and configured, use the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to estimate current drain on these supplies.

Table 7: **Power-On Current for Zynq-7000 Devices**

Device	$I_{CCPINTMIN}$	$I_{CCPAUXMIN}$	$I_{CCDDRMIN}$	$I_{CCINTMIN}$	$I_{CCAUXMIN}$	I_{CCOMIN}	I_{CCAUX_IOMIN}	$I_{CCBRAMMIN}$	Units
XC7Z030	$I_{CCPINTQ}$ + 70 mA	$I_{CCPAUXQ}$ + 40 mA	I_{CCDDRQ} + 130 mA per bank	I_{CCINTQ} + 900 mA	I_{CCAUXQ} + 60 mA	I_{CCOQ} + 90 mA per bank	$I_{CCOAUXIOQ}$ + 40 mA per bank	$I_{CCBRAMQ}$ + 90 mA	mA
XC7Z035	$I_{CCPINTQ}$ + 70 mA	$I_{CCPAUXQ}$ + 40 mA	I_{CCDDRQ} + 130 mA per bank	I_{CCINTQ} + 1400 mA	I_{CCAUXQ} + 60 mA	I_{CCOQ} + 90 mA per bank	$I_{CCOAUXIOQ}$ + 40 mA per bank	$I_{CCBRAMQ}$ + 90 mA	mA
XC7Z045	$I_{CCPINTQ}$ + 70 mA	$I_{CCPAUXQ}$ + 40 mA	I_{CCDDRQ} + 130 mA per bank	I_{CCINTQ} + 1400 mA	I_{CCAUXQ} + 60 mA	I_{CCOQ} + 90 mA per bank	$I_{CCOAUXIOQ}$ + 40 mA per bank	$I_{CCBRAMQ}$ + 90 mA	mA
XC7Z100	$I_{CCPINTQ}$ + 70 mA	$I_{CCPAUXQ}$ + 40 mA	I_{CCDDRQ} + 130 mA per bank	I_{CCINTQ} + 2200 mA	I_{CCAUXQ} + 60 mA	I_{CCOQ} + 90 mA per bank	$I_{CCOAUXIOQ}$ + 40 mA per bank	$I_{CCBRAMQ}$ + 90 mA	mA
XA7Z030	$I_{CCPINTQ}$ + 70 mA	$I_{CCPAUXQ}$ + 40 mA	I_{CCDDRQ} + 130 mA per bank	I_{CCINTQ} + 900 mA	I_{CCAUXQ} + 60 mA	I_{CCOQ} + 90 mA per bank	$I_{CCOAUXIOQ}$ + 40 mA per bank	$I_{CCBRAMQ}$ + 90 mA	mA
XQ7Z030	$I_{CCPINTQ}$ + 70 mA	$I_{CCPAUXQ}$ + 40 mA	I_{CCDDRQ} + 130 mA per bank	I_{CCINTQ} + 900 mA	I_{CCAUXQ} + 60 mA	I_{CCOQ} + 90 mA per bank	$I_{CCOAUXIOQ}$ + 40 mA per bank	$I_{CCBRAMQ}$ + 90 mA	mA
XQ7Z045	$I_{CCPINTQ}$ + 70 mA	$I_{CCPAUXQ}$ + 40 mA	I_{CCDDRQ} + 130 mA per bank	I_{CCINTQ} + 1400 mA	I_{CCAUXQ} + 60 mA	I_{CCOQ} + 90 mA per bank	$I_{CCOAUXIOQ}$ + 40 mA per bank	$I_{CCBRAMQ}$ + 90 mA	mA
XQ7Z100	$I_{CCPINTQ}$ + 70 mA	$I_{CCPAUXQ}$ + 40 mA	I_{CCDDRQ} + 130 mA per bank	I_{CCINTQ} + 2200 mA	I_{CCAUXQ} + 60 mA	I_{CCOQ} + 90 mA per bank	$I_{CCOAUXIOQ}$ + 40 mA per bank	$I_{CCBRAMQ}$ + 90 mA	mA

Table 8: **Power Supply Ramp Time**

Symbol	Description	Conditions	Min	Max	Units
$T_{VCCPINT}$	Ramp time from GND to 90% of V_{CCPINT}		0.2	50	ms
$T_{VCCPAUX}$	Ramp time from GND to 90% of V_{CCPAUX}		0.2	50	ms
T_{VCCO_DDR}	Ramp time from GND to 90% of V_{CCO_DDR}		0.2	50	ms
T_{VCCO_MIO}	Ramp time from GND to 90% of V_{CCO_MIO}		0.2	50	ms
T_{VCCINT}	Ramp time from GND to 90% of V_{CCINT}		0.2	50	ms
T_{VCCO}	Ramp time from GND to 90% of V_{CCO}		0.2	50	ms
T_{VCCAUX}	Ramp time from GND to 90% of V_{CCAUX}		0.2	50	ms
T_{VCCAUX_IO}	Ramp time from GND to 90% of V_{CCAUX_IO}		0.2	50	ms
$T_{VCCBRAM}$	Ramp time from GND to 90% of V_{CCBRAM}		0.2	50	ms
$T_{VCCO2VCCAUX}$	Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625V$ and $V_{CCO\_MIO} - V_{CCPAUX} > 2.625V$	$T_J = 125°C$[1]	–	300	ms
		$T_J = 100°C$[1]	–	500	ms
		$T_J = 85°C$[1]	–	800	ms
$T_{MGTAVCC}$	Ramp time from GND to 90% of $V_{MGTAVCC}$		0.2	50	ms
$T_{MGTAVTT}$	Ramp time from GND to 90% of $V_{MGTAVTT}$		0.2	50	ms

Table 8: **Power Supply Ramp Time *(Cont'd)***

Symbol	Description	Conditions	Min	Max	Units
$T_{MGTVCCAUX}$	Ramp time from GND to 90% of $V_{MGTVCCAUX}$		0.2	50	ms

Notes:

1. Based on 240,000 power cycles with nominal V_{CCO} of 3.3V or 36,500 power cycles with a worst case V_{CCO} of 3.465V.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

PS I/O Levels

Table 9: **PS DC Input and Output Levels(1)**

Bank	I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
		V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
MIO	LVCMOS18	–0.300	35% V_{CCO_MIO}	65% V_{CCO_MIO}	V_{CCO_MIO} + 0.300	0.450	V_{CCO_MIO} – 0.450	8	–8
MIO	LVCMOS25	–0.300	0.700	1.700	V_{CCO_MIO} + 0.300	0.400	V_{CCO_MIO} – 0.400	8	–8
MIO	LVCMOS33	–0.300	0.800	2.000	3.450	0.400	V_{CCO_MIO} – 0.400	8	–8
MIO	HSTL_I_18	–0.300	V_{PREF} – 0.100	V_{PREF} + 0.100	V_{CCO_MIO} + 0.300	0.400	V_{CCO_MIO} – 0.400	8	–8
DDR	SSTL18_I	–0.300	V_{PREF} – 0.125	V_{PREF} + 0.125	V_{CCO_DDR} + 0.300	V_{CCO_DDR}/2 – 0.470	V_{CCO_DDR}/2 + 0.470	8	–8
DDR	SSTL15	–0.300	V_{PREF} – 0.100	V_{PREF} + 0.100	V_{CCO_DDR} + 0.300	V_{CCO_DDR}/2 – 0.175	V_{CCO_DDR}/2 + 0.175	13.0	–13.0
DDR	SSTL135	–0.300	V_{PREF} – 0.090	V_{PREF} + 0.090	V_{CCO_DDR} + 0.300	V_{CCO_DDR}/2 – 0.150	V_{CCO_DDR}/2 + 0.150	13.0	–13.0
DDR	HSUL_12	–0.300	V_{PREF} – 0.130	V_{PREF} + 0.130	V_{CCO_DDR} + 0.300	20% V_{CCO_DDR}	80% V_{CCO_DDR}	0.1	–0.1

Notes:

1. Tested according to relevant specifications.

Table 10: **PS Complementary Differential DC Input and Output Levels**

Bank	I/O Standard	V_{ICM}(1)			V_{ID}(2)		V_{OL}(3)	V_{OH}(4)	I_{OL}	I_{OH}
		V, Min	V,Typ	V, Max	V,Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DDR	DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.100	–0.100
DDR	DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO_DDR}/2) – 0.150	(V_{CCO_DDR}/2) + 0.150	13.0	–13.0
DDR	DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO_DDR}/2) – 0.175	(V_{CCO_DDR}/2) + 0.175	13.0	–13.0
DDR	DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO_DDR}/2) – 0.470	(V_{CCO_DDR}/2) + 0.470	8.00	–8.00

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q–$\overline{Q}$).
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

PL I/O Levels

Table 11: **SelectIO DC Input and Output Levels(1)(2)**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8	–8
HSTL_I_12	–0.300	V_{REF} – 0.080	V_{REF} + 0.080	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	6.3	–6.3
HSTL_I_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8	–8
HSTL_II	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	16	–16
HSTL_II_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	16	–16
HSUL_12	–0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 3	Note 3
LVCMOS15, LVDCI_15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	Note 4	Note 4
LVCMOS18, LVDCI_18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVCMOS25	–0.300	0.700	1.700	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 6	Note 6
LVCMOS33	–0.300	0.800	2.000	3.450	0.400	V_{CCO} – 0.400	Note 6	Note 6
LVTTL	–0.300	0.800	2.000	3.450	0.400	2.400	Note 7	Note 7
MOBILE_DDR	–0.300	20% V_{CCO}	80% V_{CCO}	V_{CCO} + 0.300	10% V_{CCO}	90% V_{CCO}	0.1	–0.1
PCI33_3	–0.400	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.500	10% V_{CCO}	90% V_{CCO}	1.5	–0.5
SSTL12	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.150	$V_{CCO}/2$ + 0.150	14.25	–14.25
SSTL135	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.150	$V_{CCO}/2$ + 0.150	13.0	–13.0
SSTL135_R	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.150	$V_{CCO}/2$ + 0.150	8.9	–8.9
SSTL15	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.175	$V_{CCO}/2$ + 0.175	13.0	–13.0
SSTL15_R	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.175	$V_{CCO}/2$ + 0.175	8.9	–8.9
SSTL18_I	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.470	$V_{CCO}/2$ + 0.470	8	–8
SSTL18_II	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.600	$V_{CCO}/2$ + 0.600	13.4	–13.4

Notes:

1. Tested according to relevant specifications.
2. 3.3V and 2.5V standards are only supported in HR I/O banks.
3. Supported drive strengths of 2, 4, 6, or 8 mA in HP I/O banks and 4, 8, or 12 mA in HR I/O banks.
4. Supported drive strengths of 2, 4, 6, 8, 12, or 16 mA in HP I/O banks and 4, 8, 12, or 16 mA in HR I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, 12, or 16 mA in HP I/O banks and 4, 8, 12, 16, or 24 mA in HR I/O banks.
6. Supported drive strengths of 4, 8, 12, or 16 mA
7. Supported drive strengths of 4, 8, 12, 16, or 24 mA
8. For detailed interface specific DC voltage levels, see the *7 Series FPGAs SelectIO Resources User Guide* (UG471).

Table 12: **Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM}[1]			V_{ID}[2]			V_{OCM}[3]			V_{OD}[4]		
	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max
BLVDS_25	0.300	1.200	1.425	0.100	–	–	–	1.250	–	Note 5		
MINI_LVDS_25	0.300	1.200	V_{CCAUX}	0.200	0.400	0.600	1.000	1.200	1.400	0.300	0.450	0.600
PPDS_25	0.200	0.900	V_{CCAUX}	0.100	0.250	0.400	0.500	0.950	1.400	0.100	0.250	0.400
RSDS_25	0.300	0.900	1.500	0.100	0.350	0.600	1.000	1.200	1.400	0.100	0.350	0.600
TMDS_33	2.700	2.965	3.230	0.150	0.675	1.200	V_{CCO}–0.405	V_{CCO}–0.300	V_{CCO}–0.190	0.400	0.600	0.800

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{OCM} is the output common mode voltage.
4. V_{OD} is the output differential voltage (Q – $\overline{Q}$).
5. V_{OD} for BLVDS will vary significantly depending on topology and loading.
6. LVDS_25 is specified in Table 14.
7. LVDS is specified in Table 15.

Table 13: **Complementary Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM}[1]			V_{ID}[2]		V_{OL}[3]	V_{OH}[4]	I_{OL}	I_{OH}
	V, Min	V, Typ	V, Max	V, Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DIFF_HSTL_I	0.300	0.750	1.125	0.100	–	0.400	V_{CCO}–0.400	8.00	–8.00
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO}–0.400	8.00	–8.00
DIFF_HSTL_II	0.300	0.750	1.125	0.100	–	0.400	V_{CCO}–0.400	16.00	–16.00
DIFF_HSTL_II_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO}–0.400	16.00	–16.00
DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.100	–0.100
DIFF_MOBILE_DDR	0.300	0.900	1.425	0.100	–	10% V_{CCO}	90% V_{CCO}	0.100	–0.100
DIFF_SSTL12	0.300	0.600	0.850	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	14.25	–14.25
DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	13.0	–13.0
DIFF_SSTL135_R	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	8.9	–8.9
DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	13.0	–13.0
DIFF_SSTL15_R	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	8.9	–8.9
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.470	(V_{CCO}/2) + 0.470	8.00	–8.00
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.600	(V_{CCO}/2) + 0.600	13.4	–13.4

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

LVDS DC Specifications (LVDS_25)

The LVDS_25 standard is available in the HR I/O banks.

Table 14: **LVDS_25 DC Specifications(1)**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.375	2.500	2.625	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.700	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.300	1.200	1.500	V

Notes:

1. Differential inputs for LVDS_25 can be placed in banks with V_{CCO} levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide* (UG471) for more information.

LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks.

Table 15: **LVDS DC Specifications(1)**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		1.710	1.800	1.890	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.825	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25V	100	350	600	mV
V_{ICM}	Input Common-Mode Voltage	Differential input voltage = ±350 mV	0.300	1.200	1.425	V

Notes:

1. Differential inputs for LVDS can be placed in banks with V_{CCO} levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide* (UG471) for more information.

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the ISE® Design Suite 14.7 and Vivado® Design Suite 2015.4 as outlined in Table 16.

Table 16: **Zynq-7000 All Programmable SoC Speed Specification Version By Device**

ISE 14.7	Vivado 2015.4	Device
1.08	1.11	XC7Z030 and XC7Z045
N/A	1.11	XC7Z035 and XC7Z100
N/A	1.09	XA7Z030
1.06	1.10	XQ7Z030 and XQ7Z045
N/A	1.10	XQ7Z100

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Zynq-7000 devices.

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 17 correlates the current status of each Zynq-7000 device on a per speed grade basis.

Table 17: **Zynq-7000 Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC7Z030			-3, -2, -2LI, -1
XC7Z035			-3, -2, -2LI, -1
XC7Z045			-3, -2, -2LI, -1
XC7Z100			-2, -2LI, -1
XA7Z030			-1I, -1Q

Table 17: **Zynq-7000 Device Speed Grade Designations *(Cont'd)***

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XQ7Z030			-2I, -2LI, -1I, -1Q
XQ7Z045			-2I, -2LI, -1I, -1Q, -1LQ
XQ7Z100			-2I, -2LI, -1I

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 18 lists the production released Zynq-7000 device, speed grade, and the minimum corresponding supported speed specification version and software revisions. The software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 18: **Zynq-7000 Device Production Software and Speed Specification Release**

<table>
<tr><th rowspan="2">Device</th><th colspan="8">Speed Grade Designations</th></tr>
<tr><th>-3E</th><th>-2E</th><th>-2I</th><th>-2LI</th><th>-1C</th><th>-1I</th><th>-1Q</th><th>-1LQ</th></tr>
<tr><td>XC7Z030</td><td colspan="3">ISE tools 14.5 v1.06 and Vivado tools 2013.1 v1.06</td><td>Vivado tools 2014.4 v1.11</td><td colspan="2">ISE tools 14.5 v1.06 and Vivado tools 2013.1 v1.06</td><td>N/A</td><td>N/A</td></tr>
<tr><td>XC7Z035</td><td colspan="6">Vivado tools 2014.4 v1.11</td><td>N/A</td><td>N/A</td></tr>
<tr><td>XC7Z045</td><td colspan="3">ISE tools 14.5 v1.06 and Vivado tools 2013.1 v1.06</td><td>Vivado tools 2014.4 v1.11</td><td colspan="2">ISE tools 14.5 v1.06 and Vivado tools 2013.1 v1.06</td><td>N/A</td><td>N/A</td></tr>
<tr><td>XC7Z100</td><td>N/A</td><td>N/A</td><td>Vivado tools 2013.2 v1.07</td><td>Vivado tools 2014.4 v1.11</td><td>N/A</td><td>Vivado tools 2013.2 v1.07</td><td>N/A</td><td>N/A</td></tr>
<tr><td>XA7Z030</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td colspan="2">Vivado tools 2014.2 v1.08</td><td>N/A</td></tr>
<tr><td>XQ7Z030</td><td>N/A</td><td>N/A</td><td rowspan="2">ISE tools 14.7 v1.06 and Vivado tools 2013.3 v1.06</td><td rowspan="3">Vivado tools 2015.4 v1.10</td><td>N/A</td><td colspan="2" rowspan="2">ISE tools 14.7 v1.06 and Vivado tools 2013.3 v1.06</td><td>N/A</td></tr>
<tr><td>XQ7Z045</td><td>N/A</td><td>N/A</td><td>N/A</td><td>Vivado tools 2015.2 v1.09</td></tr>
<tr><td>XQ7Z100</td><td>N/A</td><td>N/A</td><td>Vivado tools 2015.4 v1.10</td><td>N/A</td><td>Vivado tools 2015.2 v1.09</td><td>N/A</td><td>N/A</td></tr>
</table>

Selecting the Correct Speed Grade and Voltage in the Vivado Tools

It is important to select the correct device speed grade and voltage in the Vivado tools for the device that you are selecting.

To select the -3, -2, or -1 (PL 1.0V) speed specifications in the Vivado tools, select the **Zynq-7000**, **XA Zynq-7000**, or **Defense Grade Zynq-7000** sub-family, and then select the part name that is the device name followed by the package name followed by the speed grade. For example, select the **xc7z030fbg676-3** part name for the XC7Z030 device in the FBG676 package and -3 speed grade.

To select the -2LI (PL 0.95V) speed specifications in the Vivado tools, select the **Zynq-7000** sub-family and then select the part name that is the device name followed by an *i* followed by the package name followed by the speed grade. For example, select the **xc7z030ifbg676-2L** part name for the XC7Z030 device in the FBG676 package and -2LI (PL 0.95V) speed grade. The -2LI (PL 0.95V) speed specifications are not supported in the ISE tools.

A similar part naming convention applies to the speed specifications selection in the ISE tools for supported devices. See Table 18 for the subset of Zynq-7000 devices supported in the ISE tools.

PS Performance Characteristics

For further design requirement details, refer to the *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585).

Table 19: **CPU Clock Domains Performance**

Symbol	Clock Ratio	Description	Speed Grade				Units
			-3E	-2E/-2I/-2LI	-1C/-1I	-1Q/-1LQ	
$F_{CPU\_6X4X\_621\_MAX}$ (1)(2)	6:2:1	Maximum CPU clock frequency	1000	800	667	667	MHz
$F_{CPU\_3X2X\_621\_MAX}$		Maximum CPU_3X clock frequency	500	400	333	333	MHz
$F_{CPU\_2X\_621\_MAX}$		Maximum CPU_2X clock frequency	333	266	222	222	MHz
$F_{CPU\_1X\_621\_MAX}$		Maximum CPU_1X clock frequency	167	133	111	111	MHz
$F_{CPU\_6X4X\_421\_MAX}$ (1)	4:2:1	Maximum CPU clock frequency	710	600	533	533	MHz
$F_{CPU\_3X2X\_421\_MAX}$		Maximum CPU_3X clock frequency	355	300	267	267	MHz
$F_{CPU\_2X\_421\_MAX}$		Maximum CPU_2X clock frequency	355	300	267	267	MHz
$F_{CPU\_1X\_421\_MAX}$		Maximum CPU_1X clock frequency	178	150	133	133	MHz

Notes:

1. The maximum frequency during BootROM execution is 500 MHz across all speed specifications.
2. When the processor cores operate $F_{CPU\_6X4X\_621\_MAX}$ at 1 GHz (-3E speed grade), the V_{CCPINT} minimum is 0.97V and the V_{CCPINT} maximum is 1.03V.

Table 20: **PS DDR Clock Domains Performance**(1)

Symbol	Description	Speed Grade				Units
		-3E	-2E/-2I/-2LI	-1C/-1I	-1Q/-1LQ	
F_{DDR3_MAX}	Maximum DDR3 interface performance	1333(2)	1066	1066	1066	Mb/s
F_{DDR3L_MAX}	Maximum DDR3L interface performance	1066	1066	1066	1066	Mb/s
F_{DDR2_MAX}	Maximum DDR2 interface performance	800	800	800	800	Mb/s
F_{LPDDR2_MAX}	Maximum LPDDR2 interface performance	800	800	800	800	Mb/s
F_{DDRCLK_2XMAX}	Maximum DDR_2X clock frequency	444	408	355	355	MHz

Notes:

1. All performance numbers apply to both internal and external V_{REF} configurations.
2. When a DDR interface operates at 1333 Mb/s, the V_{CCPINT} minimum is 0.97V and the V_{CCPINT} maximum is 1.03V.

Table 21: **PS-PL Interface Performance**

Symbol	Description	Min	Max	Units
$F_{EMIOGEMCLK}$	EMIO gigabit Ethernet controller maximum frequency	–	125	MHz
$F_{EMIOSDCLK}$	EMIO SD controller maximum frequency	–	25	MHz
$F_{EMIOSPICLK}$	EMIO SPI controller maximum frequency	–	25	MHz
$F_{EMIOJTAGCLK}$	EMIO JTAG controller maximum frequency	–	20	MHz
$F_{EMIOTRACECLK}$	EMIO trace controller maximum frequency	–	125	MHz
F_{FTMCLK}	Fabric trace monitor maximum frequency	–	125	MHz
$F_{EMIODMACLK}$	DMA maximum frequency	–	100	MHz
F_{AXI_MAX}	Maximum AXI interface performance	–	250	MHz

PS Switching Characteristics

Clocks

Table 22: **System Reference Clock Input Requirements**

Symbol	Description	Min	Typ	Max	Units
$T_{JTPSCLK}$	PS_CLK RMS clock jitter tolerance	–	–	±0.5	%
$T_{DCPSCLK}$	PS_CLK duty cycle	40	–	60	%
$T_{RFPSCLK}$	PS_CLK rise and fall time	–	–	6	ns
F_{PSCLK}	PS_CLK frequency	30	–	60	MHz

Table 23: **PS PLL Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3E	-2E/-2I/-2LI	-1C/-1I	-1Q/-1LQ	
T_{LOCK_PSPLL}	PLL maximum lock time	60	60	60	60	µs
F_{PSPLL_MAX}	PLL maximum output frequency	2000	1800	1600	1600	MHz
F_{PSPLL_MIN}	PLL minimum output frequency	780	780	780	780	MHz

Resets

Table 24: **PS Reset Assertion Timing Requirements**

Symbol	Description	Min	Typ	Max	Units
T_{PSPOR}	Required PS_POR_B assertion time(1)	100	–	–	µs
T_{PSRST}	Required PS_SRST_B assertion time	3	–	–	PS_CLK Clock Cycles

Notes:

1. PS_POR_B needs to be asserted low until PS supply voltages reach minimum levels.

The PS_POR_B deassertion must meet the following requirements to avoid coinciding with the secure lockdown window. Figure 1 shows the timing relationship between PS_POR_B and the last power supply ramp (V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, or V_{CCO} in bank 0). T_{SLW} minimum and maximum parameters define the beginning and end, respectively, of the secure lockdown window relative to the last PL power supply reaching 250 mV. The PS_POR_B must not be deasserted within the secure lockdown window.

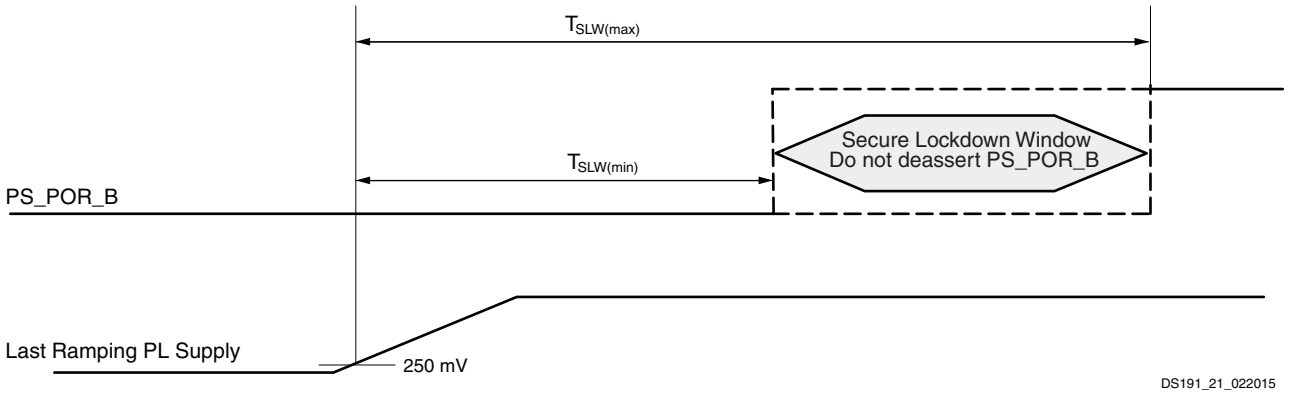

Figure 1: **PS_POR_B and Power Supply Ramp Timing Requirements**

Table 25: **PS Reset/Power Supply Timing Requirements**

Symbol	Description	PS_CLK Frequency (MHz)	Min	Max	Units
T_{SLW}[1]	128 KB CRC eFUSE disabled and PLL enabled. Default configuration	30	12	39	ms
		33.33	12	40	ms
		60	13	40	ms
	128 KB CRC eFUSE disabled and PLL in bypass.	30	–32	13	ms
		33.33	–27	13	ms
		60	–9	25	ms
	128 KB CRC eFUSE enabled and PLL enabled.[2]	30	–19	9	ms
		33.33	–16	12	ms
		60	–3	25	ms
	128 KB CRC eFUSE enabled and PLL in bypass.[2]	30	–830	–788	ms
		33.33	–746	–705	ms
		60	–408	–374	ms

Notes:

1. Valid for power supply ramp times of less than 6 ms. For ramp times longer than 6 ms, see the BootROM Performance section of the *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585).
2. If any PS and PL power supplies are tied together, observe the PS_POR_B assertion time requirement (T_{PSPOR}) in Table 24 and its accompanying note.

PS Configuration

Table 26: **Processor Configuration Access Port Switching Characteristics**

Symbol	Description	Min	Typ	Max	Units
F_{PCAPCK}	Maximum processor configuration access port (PCAP) frequency	–	–	100	MHz

DDR Memory Interfaces

Table 27: **DDR3 Interface Switching Characteristics (1333 Mb/s)[1]**

Symbol	Description	Min	Max	Units
$T_{DQVALID}$[2]	Input data valid window	450	–	ps
T_{DQDS}[3]	Output DQ to DQS skew	95	–	ps
T_{DQDH}[4]	Output DQS to DQ skew	222	–	ps
T_{DQSS}	Output clock to DQS skew	–0.11	0.08	T_{CK}
T_{CACK}[5]	Command/address output setup time with respect to CLK	465	–	ps
T_{CKCA}[6]	Command/address output hold time with respect to CLK	528	–	ps

Notes:

1. Recommended V_{CCO_DDR} = 1.5V ±5%.
2. Measurement is taken from V_{REF} to V_{REF}.
3. Measurement is taken from either the rising edge of DQ that crosses V_{IH}(AC) or the falling edge of DQ that crosses V_{IL}(AC) to V_{REF} of DQS.
4. Measurement is taken from either the rising edge of DQ that crosses V_{IL}(DC) or the falling edge of DQ that crosses V_{IH}(DC) to V_{REF} of DQS.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IH}(AC) or the falling edge of CMD/ADDR that crosses V_{IL}(AC) to V_{REF} of CLK.
6. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IL}(DC) or the falling edge of CMD/ADDR that crosses V_{IH}(DC) to V_{REF} of CLK.

Table 28: **DDR3 Interface Switching Characteristics (1066 Mb/s)(1)**

Symbol	Description	Min	Max	Units
$T_{DQVALID}$(2)	Input data valid window	450	–	ps
T_{DQDS}(3)	Output DQ to DQS skew	100	–	ps
T_{DQDH}(4)	Output DQS to DQ skew	350	–	ps
T_{DQSS}	Output clock to DQS skew	–0.10	0.10	T_{CK}
T_{CACK}(5)	Command/address output setup time with respect to CLK	560	–	ps
T_{CKCA}(6)	Command/address output hold time with respect to CLK	658	–	ps

Notes:

1. Recommended V_{CCO_DDR} = 1.5V ±5%.
2. Measurement is taken from V_{REF} to V_{REF}.
3. Measurement is taken from either the rising edge of DQ that crosses V_{IH}(AC) or the falling edge of DQ that crosses V_{IL}(AC) to V_{REF} of DQS.
4. Measurement is taken from either the rising edge of DQ that crosses V_{IL}(DC) or the falling edge of DQ that crosses V_{IH}(DC) to V_{REF} of DQS.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IH}(AC) or the falling edge of CMD/ADDR that crosses V_{IL}(AC) to V_{REF} of CLK.
6. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IL}(DC) or the falling edge of CMD/ADDR that crosses V_{IH}(DC) to V_{REF} of CLK.

Table 29: **DDR3L Interface Switching Characteristics (1066 Mb/s)(1)**

Symbol	Description	Min	Max	Units
$T_{DQVALID}$(2)	Input data valid window	450	–	ps
T_{DQDS}(3)	Output DQ to DQS skew	189	–	ps
T_{DQDH}(4)	Output DQS to DQ skew	267	–	ps
T_{DQSS}	Output clock to DQS skew	–0.13	0.04	T_{CK}
T_{CACK}(5)	Command/address output setup time with respect to CLK	410	–	ps
T_{CKCA}(6)	Command/address output hold time with respect to CLK	629	–	ps

Notes:

1. Recommended V_{CCO_DDR} = 1.35V ±5%.
2. Measurement is taken from V_{REF} to V_{REF}.
3. Measurement is taken from either the rising edge of DQ that crosses V_{IH}(AC) or the falling edge of DQ that crosses V_{IL}(AC) to V_{REF} of DQS.
4. Measurement is taken from either the rising edge of DQ that crosses V_{IL}(DC) or the falling edge of DQ that crosses V_{IH}(DC) to V_{REF} of DQS.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IH}(AC) or the falling edge of CMD/ADDR that crosses V_{IL}(AC) to V_{REF} of CLK.
6. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IL}(DC) or the falling edge of CMD/ADDR that crosses V_{IH}(DC) to V_{REF} of CLK.

Table 30: **DDR3L Interface Switching Characteristics (800 Mb/s)(1)**

Symbol	Description	Min	Max	Units
$T_{DQVALID}$(2)	Input data valid window	500	–	ps
T_{DQDS}(3)	Output DQ to DQS skew	321	–	ps
T_{DQDH}(4)	Output DQS to DQ skew	380	–	ps
T_{DQSS}	Output clock to DQS skew	–0.12	0.04	T_{CK}
T_{CACK}(5)	Command/address output setup time with respect to CLK	636	–	ps

Table 30: **DDR3L Interface Switching Characteristics (800 Mb/s)(1) *(Cont'd)***

Symbol	Description	Min	Max	Units
T_{CKCA}(6)	Command/address output hold time with respect to CLK	853	–	ps

Notes:

1. Recommended V_{CCO_DDR} = 1.35V ±5%.
2. Measurement is taken from V_{REF} to V_{REF}.
3. Measurement is taken from either the rising edge of DQ that crosses V_{IH}(AC) or the falling edge of DQ that crosses V_{IL}(AC) to V_{REF} of DQS.
4. Measurement is taken from either the rising edge of DQ that crosses V_{IL}(DC) or the falling edge of DQ that crosses V_{IH}(DC) to V_{REF} of DQS.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IH}(AC) or the falling edge of CMD/ADDR that crosses V_{IL}(AC) to V_{REF} of CLK.
6. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IL}(DC) or the falling edge of CMD/ADDR that crosses V_{IH}(DC) to V_{REF} of CLK.

Table 31: **LPDDR2 Interface Switching Characteristics (800 Mb/s)(1)**

Symbol	Description	Min	Max	Units
$T_{DQVALID}$(2)	Input data valid window	500	–	ps
T_{DQDS}(3)	Output DQ to DQS skew	111	–	ps
T_{DQDH}(4)	Output DQS to DQ skew	318	–	ps
T_{DQSS}	Output clock to DQS skew	0.91	1.10	T_{CK}
T_{CACK}(5)	Command/address output setup time with respect to CLK	132	–	ps
T_{CKCA}(6)	Command/address output hold time with respect to CLK	363	–	ps

Notes:

1. Recommended V_{CCO_DDR} = 1.2V ±5%.
2. Measurement is taken from V_{REF} to V_{REF}.
3. Measurement is taken from either the rising edge of DQ that crosses V_{IH}(AC) or the falling edge of DQ that crosses V_{IL}(AC) to V_{REF} of DQS.
4. Measurement is taken from either the rising edge of DQ that crosses V_{IL}(DC) or the falling edge of DQ that crosses V_{IH}(DC) to V_{REF} of DQS.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IH}(AC) or the falling edge of CMD/ADDR that crosses V_{IL}(AC) to V_{REF} of CLK.
6. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IL}(DC) or the falling edge of CMD/ADDR that crosses V_{IH}(DC) to V_{REF} of CLK.

Table 32: **LPDDR2 Interface Switching Characteristics (400 Mb/s)(1)**

Symbol	Description	Min	Max	Units
$T_{DQVALID}$(2)	Input data valid window	500	–	ps
T_{DQDS}(3)	Output DQ to DQS skew	561	–	ps
T_{DQDH}(4)	Output DQS to DQ skew	852	–	ps
T_{DQSS}	Output clock to DQS skew	0.91	1.08	T_{CK}
T_{CACK}(5)	Command/address output setup time with respect to CLK	617	–	ps
T_{CKCA}(6)	Command/address output hold time with respect to CLK	918	–	ps

Notes:

1. Recommended V_{CCO_DDR} = 1.2V ±5%.
2. Measurement is taken from V_{REF} to V_{REF}.
3. Measurement is taken from either the rising edge of DQ that crosses V_{IH}(AC) or the falling edge of DQ that crosses V_{IL}(AC) to V_{REF} of DQS.
4. Measurement is taken from either the rising edge of DQ that crosses V_{IL}(DC) or the falling edge of DQ that crosses V_{IH}(DC) to V_{REF} of DQS.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IH}(AC) or the falling edge of CMD/ADDR that crosses V_{IL}(AC) to V_{REF} of CLK.
6. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IL}(DC) or the falling edge of CMD/ADDR that crosses V_{IH}(DC) to V_{REF} of CLK.

Table 33: **DDR2 Interface Switching Characteristics (800 Mb/s)(1)**

Symbol	Description	Min	Max	Units
$T_{DQVALID}$(2)	Input data valid window	500	–	ps
T_{DQDS}(3)	Output DQ to DQS skew	147	–	ps
T_{DQDH}(4)	Output DQS to DQ skew	376	–	ps
T_{DQSS}	Output clock to DQS skew	–0.07	0.08	T_{CK}
T_{CACK}(5)	Command/address output setup time with respect to CLK	732	–	ps
T_{CKCA}(6)	Command/address output hold time with respect to CLK	938	–	ps

Notes:

1. Recommended V_{CCO_DDR} = 1.8V ±5%.
2. Measurement is taken from V_{REF} to V_{REF}.
3. Measurement is taken from either the rising edge of DQ that crosses V_{IH}(AC) or the falling edge of DQ that crosses V_{IL}(AC) to V_{REF} of DQS.
4. Measurement is taken from either the rising edge of DQ that crosses V_{IL}(DC) or the falling edge of DQ that crosses V_{IH}(DC) to V_{REF} of DQS.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IH}(AC) or the falling edge of CMD/ADDR that crosses V_{IL}(AC) to V_{REF} of CLK.
6. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IL}(DC) or the falling edge of CMD/ADDR that crosses V_{IH}(DC) to V_{REF} of CLK.

Table 34: **DDR2 Interface Switching Characteristics (400 Mb/s)(1)**

Symbol	Description	Min	Max	Units
$T_{DQVALID}$(2)	Input data valid window	500	–	ps
T_{DQDS}(3)	Output DQ to DQS skew	385	–	ps
T_{DQDH}(4)	Output DQS to DQ skew	662	–	ps
T_{DQSS}	Output clock to DQS skew	–0.11	0.06	T_{CK}
T_{CACK}(5)	Command/address output setup time with respect to CLK	1760	–	ps
T_{CKCA}(6)	Command/address output hold time with respect to CLK	1739	–	ps

Notes:

1. Recommended V_{CCO_DDR} = 1.8V ±5%.
2. Measurement is taken from V_{REF} to V_{REF}.
3. Measurement is taken from either the rising edge of DQ that crosses V_{IH}(AC) or the falling edge of DQ that crosses V_{IL}(AC) to V_{REF} of DQS.
4. Measurement is taken from either the rising edge of DQ that crosses V_{IL}(DC) or the falling edge of DQ that crosses V_{IH}(DC) to V_{REF} of DQS.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IH}(AC) or the falling edge of CMD/ADDR that crosses V_{IL}(AC) to V_{REF} of CLK.
6. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IL}(DC) or the falling edge of CMD/ADDR that crosses V_{IH}(DC) to V_{REF} of CLK.

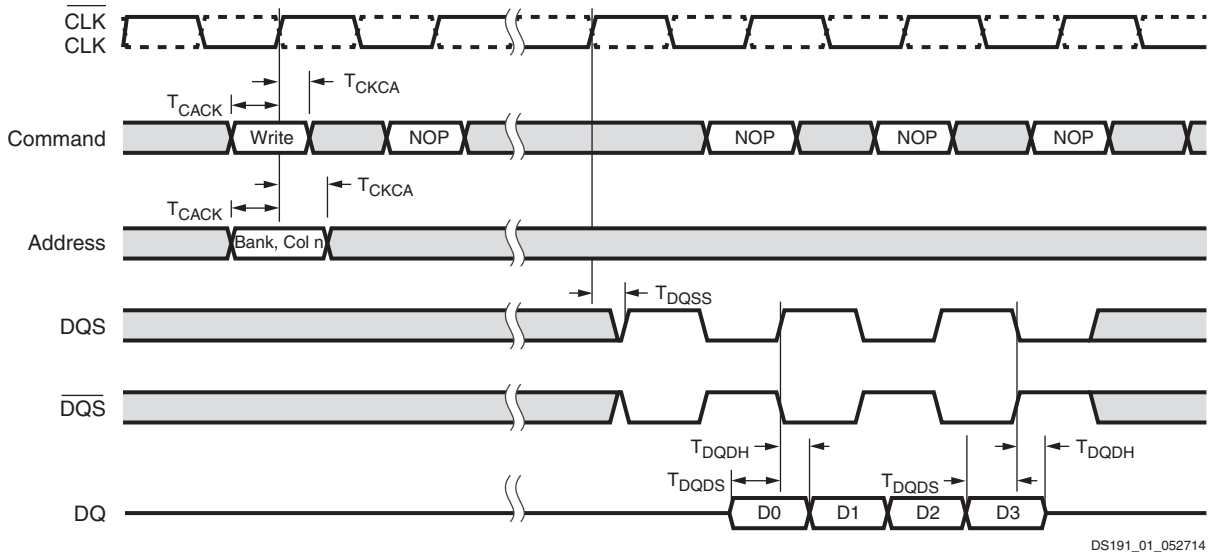

Figure 2: **DDR Output Timing Diagram**

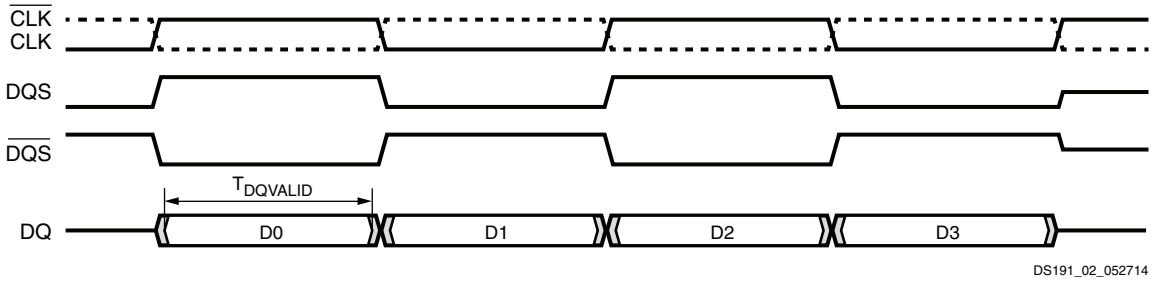

Figure 3: **DDR Input Timing Diagram**

Static Memory Controller

Table 35: **SMC Interface Delay Characteristics[1][2]**

Symbol	Description	Min	Max	Units
$T_{NANDDOUT}$	NAND_IO output delay from last register to pad	4.12	6.45	ns
$T_{NANDALE}$	NAND_ALE output delay from last register to pad	5.08	6.33	ns
$T_{NANDCLE}$	NAND_CLE output delay from last register to pad	4.87	6.40	ns
T_{NANDWE}	NAND_WE_B output delay from last register to pad	4.69	5.89	ns
T_{NANDRE}	NAND_RE_B output delay from last register to pad	5.12	6.44	ns
T_{NANDCE}	NAND_CE_B output delay from last register to pad	4.68	5.89	ns
$T_{NANDDIN}$	NAND_IO setup time and input delay from pad to first register	1.48	3.09	ns
$T_{NANDBUSY}$	NAND_BUSY setup time and input delay from pad to first register	2.48	3.33	ns
T_{SRAMA}	SRAM_A output delay from last register to pad	3.94	5.73	ns
$T_{SRAMDOUT}$	SRAM_DQ output delay from last register to pad	4.66	6.45	ns
T_{SRAMCE}	SRAM_CE output delay from last register to pad	4.57	5.95	ns
T_{SRAMOE}	SRAM_OE_B output delay from last register to pad	4.79	6.13	ns
$T_{SRAMBLS}$	SRAM_BLS_B output delay from last register to pad	5.25	6.74	ns
T_{SRAMWE}	SRAM_WE_B output delay from last register to pad	5.12	6.48	ns
$T_{SRAMDIN}$	SRAM_DQ setup time and input delay from pad to first register	1.93	3.05	ns
$T_{SRAMWAIT}$	SRAM_WAIT setup time and input delay from pad to first register	2.26	3.15	ns
$F_{SMC\_REF\_CLK}$	SMC reference clock frequency	–	100	MHz

Notes:

1. All parameters do not include the package flight time and register controlled delays.
2. Refer to the ARM® PrimeCell® Static Memory Controller (PL350 series) Technical Reference Manual for more SMC timing details.

Quad-SPI Interfaces

Table 36: **Quad-SPI Interface Switching Characteristics**

Symbol	Description	Load Conditions	Min	Max	Units
Feedback Clock Enabled					
$T_{DCQSPICLK1}$	Quad-SPI clock duty cycle	All[1][2]	44	56	%
$T_{QSPICKO1}$	Data and slave select output delay	15 pF[1]	–0.10[3]	2.30	ns
		30 pF[2]	–1.00	3.80	
$T_{QSPIDCK1}$	Input data setup time	15 pF[1]	2.00	–	ns
		30 pF[2]	3.30	–	
$T_{QSPICKD1}$	Input data hold time	15 pF[1]	1.30	–	ns
		30 pF[2]	1.50	–	
$T_{QSPISSCLK1}$	Slave select asserted to next clock edge	All[1][2]	1	–	$F_{QSPI\_REF\_CLK}$ cycle
$T_{QSPICLKSS1}$	Clock edge to slave select deasserted	All[1][2]	1	–	$F_{QSPI\_REF\_CLK}$ cycle
$F_{QSPICLK1}$	Quad-SPI device clock frequency	15 pF[1]	–	100[4]	MHz
		30 pF[2]	–	70[4]	
Feedback Clock Disabled					
$T_{DCQSPICLK2}$	Quad-SPI clock duty cycle	All[1][2]	44	56	%
$T_{QSPICKO2}$	Data and slave select output delay	15 pF[1]	–0.10	3.80	ns
		30 pF[2]	–1.00	3.80	ns
$T_{QSPIDCK2}$	Input data setup time	All[1][2]	6	–	ns
$T_{QSPICKD2}$	Input data hold time	All[1][2]	12.5	–	ns
$T_{QSPISSCLK2}$	Slave select asserted to next clock edge	All[1][2]	1	–	$F_{QSPI\_REF\_CLK}$ cycle
$T_{QSPICLKSS2}$	Clock edge to slave select deasserted	All[1][2]	1	–	$F_{QSPI\_REF\_CLK}$ cycle
$F_{QSPICLK2}$	Quad-SPI device clock frequency	All[1][2]	–	40	MHz
Feedback Clock Enabled or Disabled					
$F_{QSPI\_REF\_CLK}$	Quad-SPI reference clock frequency	All[1][2]	–	200	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads, feedback clock pin has no load. Quad-SPI single slave select 4-bit I/O mode.
2. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 30 pF loads in 4-bit stacked I/O configuration, feedback clock pin has no load. Quad-SPI single slave select 4-bit I/O mode.
3. The $T_{QSPICKO1}$ is an effective value. Use it to compute the available memory device input setup and hold timing budgets based on the given device clock-out duty-cycle limits.
4. Requires appropriate component selection/board design.

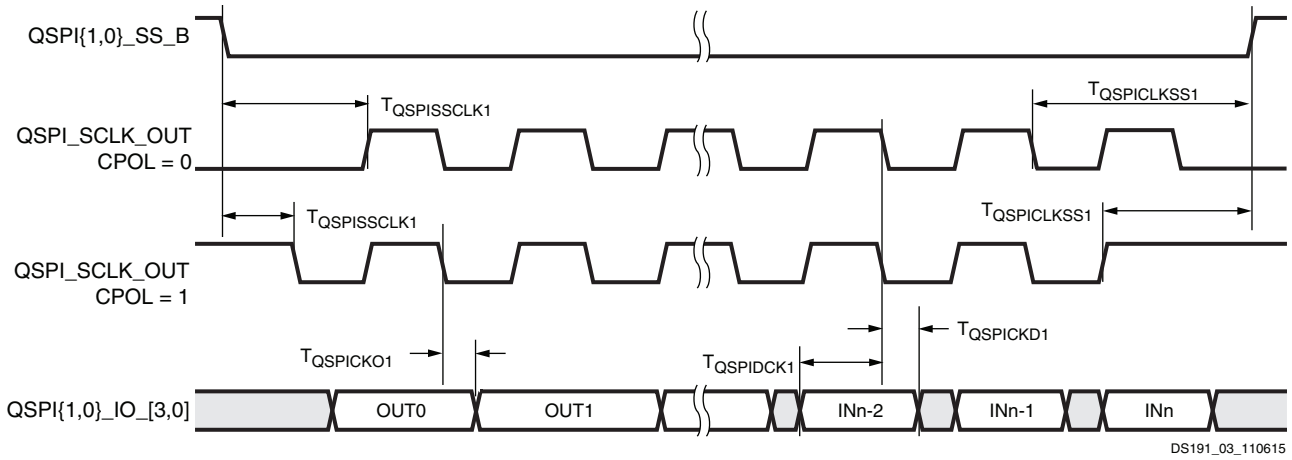

Figure 4: **Quad-SPI Interface (Feedback Clock Enabled) Timing Diagram**

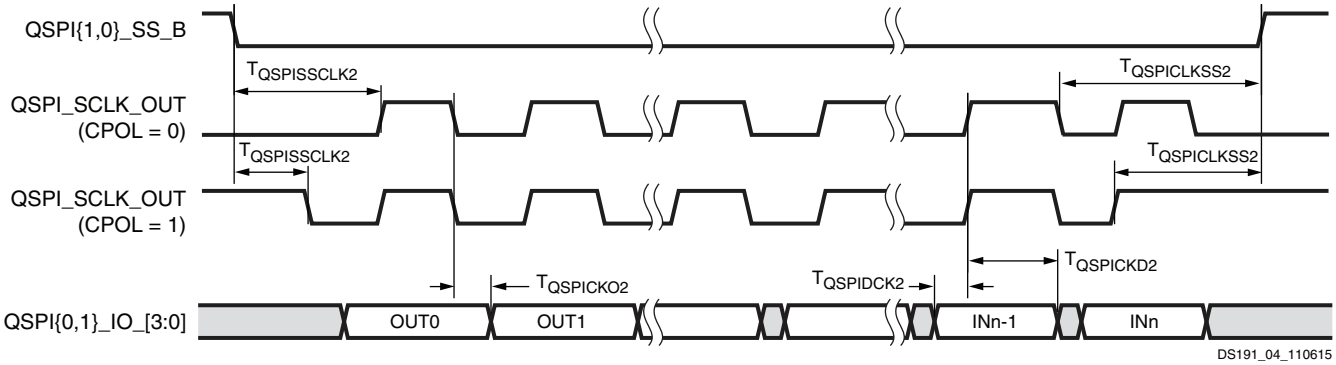

Figure 5: **Quad-SPI Interface (Feedback Clock Disabled) Timing Diagram**

ULPI Interfaces

Table 37: **ULPI Interface Clock Receiving Mode Switching Characteristics**(1)(2)

Symbol	Description	Min	Typ	Max	Units
$T_{ULPIDCK}$	Input setup to ULPI clock, all inputs	3.00	–	–	ns
$T_{ULPICKD}$	Input hold to ULPI clock, all inputs	1.00	–	–	ns
$T_{ULPICKO}$	ULPI clock to output valid, all outputs	1.70	–	8.86	ns
$F_{ULPICLK}$	ULPI device clock frequency	–	60	–	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads, 60 MHz device clock frequency.
2. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

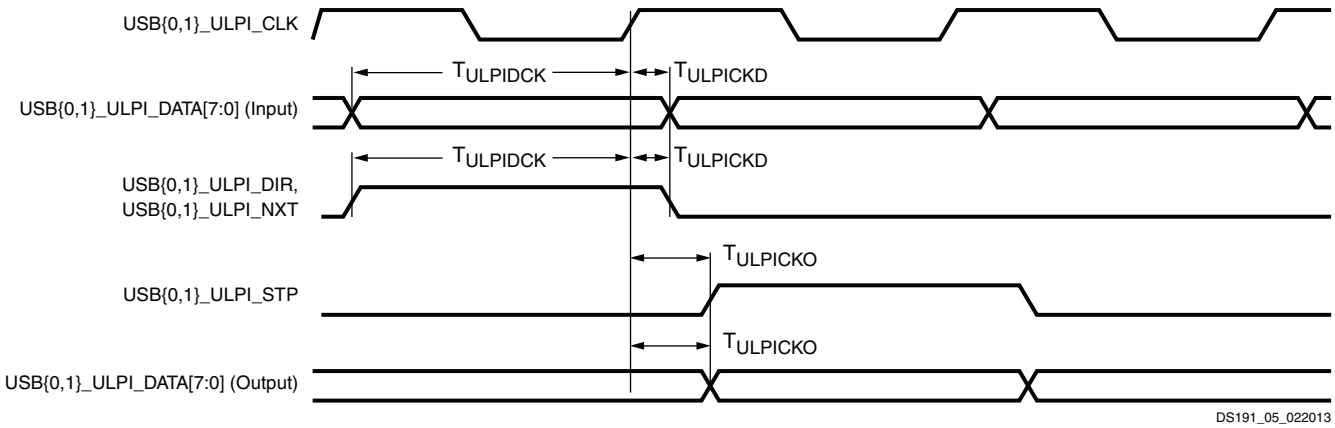

Figure 6: **ULPI Interface Timing Diagram**

RGMII and MDIO Interfaces

Table 38: **RGMII and MDIO Interface Switching Characteristics(1)(2)(3)**

Symbol	Description	Min	Typ	Max	Units
$T_{DCGETXCLK}$	Transmit clock duty cycle	45	–	55	%
$T_{GEMTXCKO}$	RGMII_TX_D[3:0], RGMII_TX_CTL output clock to out time	–0.50	–	0.50	ns
$T_{GEMRXDCK}$	RGMII_RX_D[3:0], RGMII_RX_CTL input setup time	0.80	–	–	ns
$T_{GEMRXCKD}$	RGMII_RX_D[3:0], RGMII_RX_CTL input hold time	0.80	–	–	ns
$T_{MDIOCLK}$	MDC output clock period	400	–	–	ns
$T_{MDIOCKH}$	MDC clock High time	160	–	–	ns
$T_{MDIOCKL}$	MDC clock Low time	160	–	–	ns
$T_{MDIODCK}$	MDIO input data setup time	80	–	–	ns
$T_{MDIOCKD}$	MDIO input data hold time	0	–	–	ns
$T_{MDIOCKO}$	MDIO data output delay	–20	–	170	ns
$F_{GETXCLK}$	RGMII_TX_CLK transmit clock frequency	–	125	–	MHz
$F_{GERXCLK}$	RGMII_RX_CLK receive clock frequency	–	125	–	MHz
$F_{ENET\_REF\_CLK}$	Ethernet reference clock frequency	–	125	–	MHz

Notes:

1. Test conditions: LVCMOS25, fast slew rate, 8 mA drive strength, 15 pF loads. Values in this table are specified during 1000 Mb/s operation.
2. LVCMOS25 slow slew rate and LVCMOS33 are not supported.
3. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

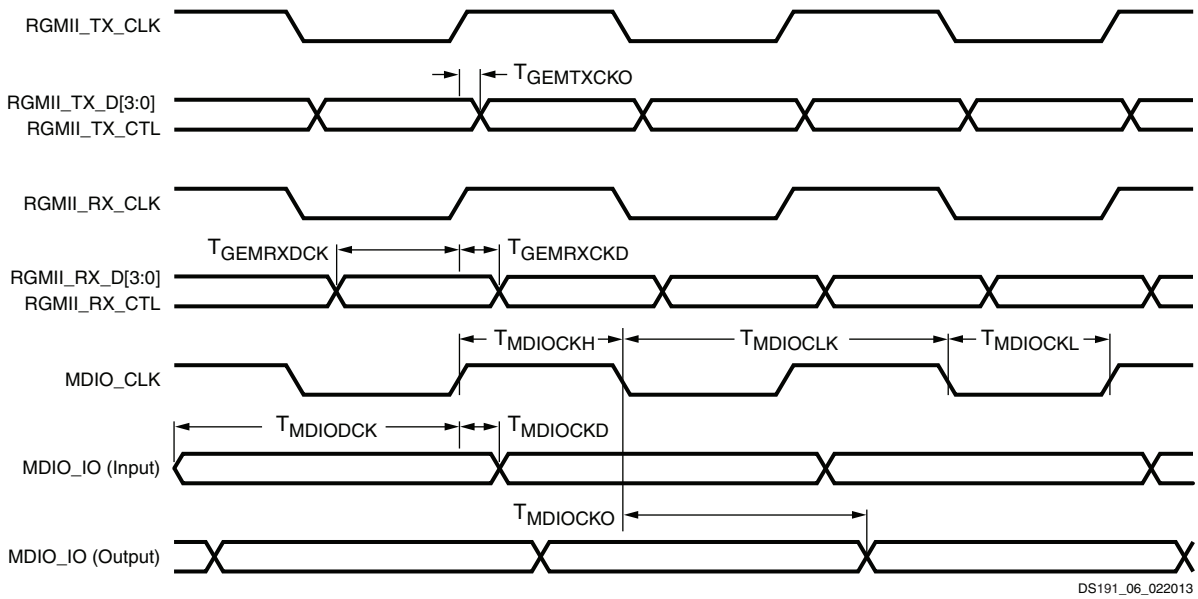

Figure 7: **RGMII Interface Timing Diagram**

SD/SDIO Interfaces

Table 39: **SD/SDIO Interface High Speed Mode Switching Characteristics(1)**

Symbol	Description	Min	Typ	Max	Units
$T_{DCSDHSCLK}$	SD device clock duty cycle	–	50	–	%
$T_{SDHSCKO}$	Clock to output delay, all outputs	2.00	–	12.00	ns
$T_{SDHSDCK}$	Input setup time, all inputs	3.00	–	–	ns
$T_{SDHSCKD}$	Input hold time, all inputs	1.05	–	–	ns
$F_{SD\_REF\_CLK}$	SD reference clock frequency	–	–	125	MHz
$F_{SDHSCLK}$	High speed mode SD device clock frequency	0	–	50	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

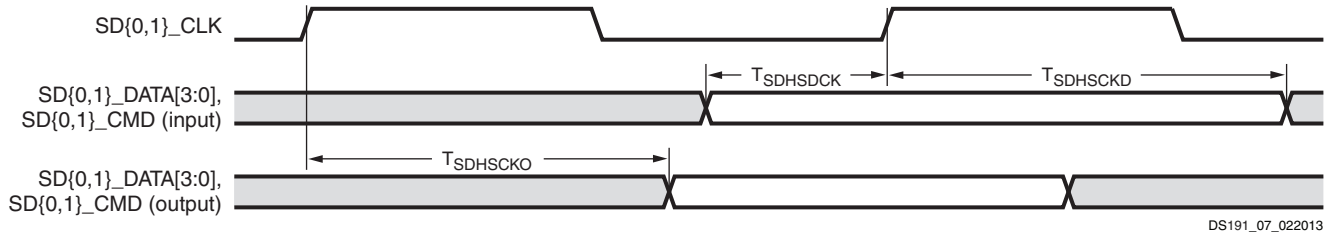

Figure 8: **SD/SDIO Interface High Speed Mode Timing Diagram**

Table 40: **SD/SDIO Interface Switching Characteristics(1)**

Symbol	Description	Min	Typ	Max	Units
$T_{DCSDSCLK}$	SD device clock duty cycle	–	50	–	%
T_{SDSCKO}	Clock to output delay, all outputs	2.00	–	12.00	ns
T_{SDSDCK}	Input setup time, all inputs	4.00	–	–	ns
T_{SDSCKD}	Input hold time, all inputs	3.00	–	–	ns
$F_{SD\_REF\_CLK}$	SD reference clock frequency	–	–	125	MHz
$F_{SDIDCLK}$	Clock frequency in identification mode	–	–	400	KHz
F_{SDSCLK}	Standard mode SD device clock frequency	0	–	25	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

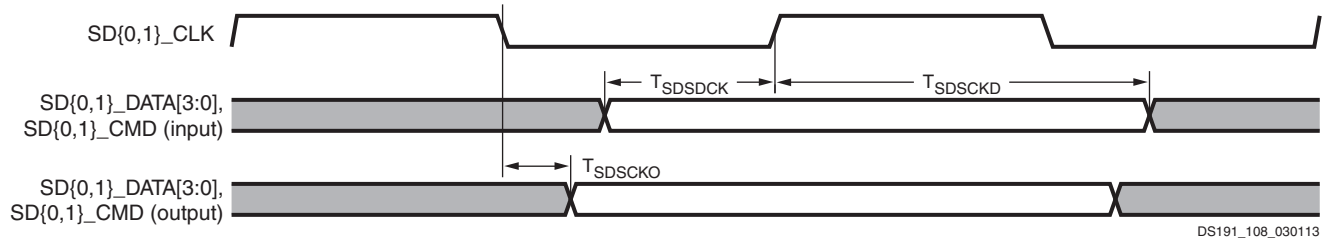

Figure 9: **SD/SDIO Interface Standard Mode Timing Diagram**

I2C Interfaces

Table 41: **I2C Fast Mode Interface Switching Characteristics(1)**

Symbol	Description	Min	Typ	Max	Units
$T_{DCI2CFCLK}$	I2C{0,1}SCL duty cycle	–	50	–	%
$T_{I2CFCKO}$	I2C{0,1}SDAO clock to out delay	–	–	900	ns
$T_{I2CFDCK}$	I2C{0,1}SDAI setup time	100	–	–	ns
$F_{I2CFCLK}$	I2C{0,1}SCL clock frequency	–	–	400	KHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

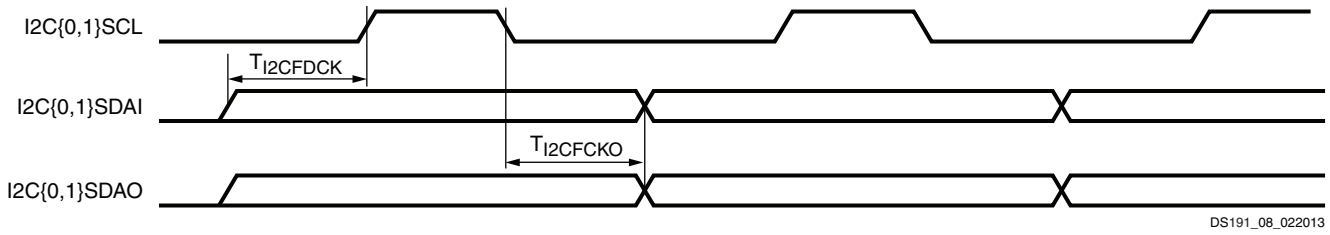

Figure 10: **I2C Fast Mode Interface Timing Diagram**

Table 42: **I2C Standard Mode Interface Switching Characteristics(1)**

Symbol	Description	Min	Typ	Max	Units
$T_{DCI2CSCLK}$	I2C{0,1}SCL duty cycle	–	50	–	%
$T_{I2CSCKO}$	I2C{0,1}SDAO clock to out delay	–	–	3450	ns
$T_{I2CSDCK}$	I2C{0,1}SDAI setup time	250	–	–	ns
$F_{I2CSCLK}$	I2C{0,1}SCL clock frequency	–	–	100	KHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

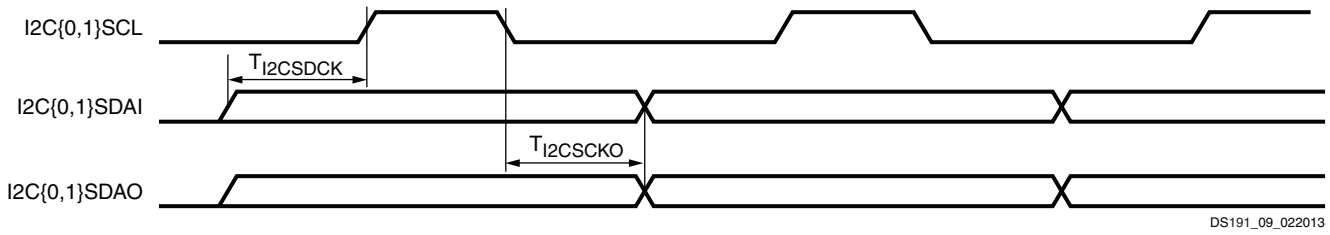

Figure 11: **I2C Standard Mode Interface Timing Diagram**

SPI Interfaces

Table 43: **SPI Master Mode Interface Switching Characteristics(1)**

Symbol	Description	Min	Typ	Max	Units
$T_{DCMSPICLK}$	SPI master mode clock duty cycle	–	50	–	%
$T_{MSPIDCK}$	Input setup time for SPI{0,1}_MISO	2.00	–	–	ns
$T_{MSPICKD}$	Input hold time for SPI{0,1}_MISO	8.20	–	–	ns
$T_{MSPICKO}$	Output delay for SPI{0,1}_MOSI and SPI{0,1}_SS	–3.10	–	3.90	ns
$T_{MSPISSCLK}$	Slave select asserted to first active clock edge	1	–	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{MSPICLKSS}$	Last active clock edge to slave select deasserted	0.5	–	–	$F_{SPI\_REF\_CLK}$ cycles
$F_{MSPICLK}$	SPI master mode device clock frequency	–	–	50.00	MHz
$F_{SPI\_REF\_CLK}$	SPI reference clock frequency	–	–	200.00	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

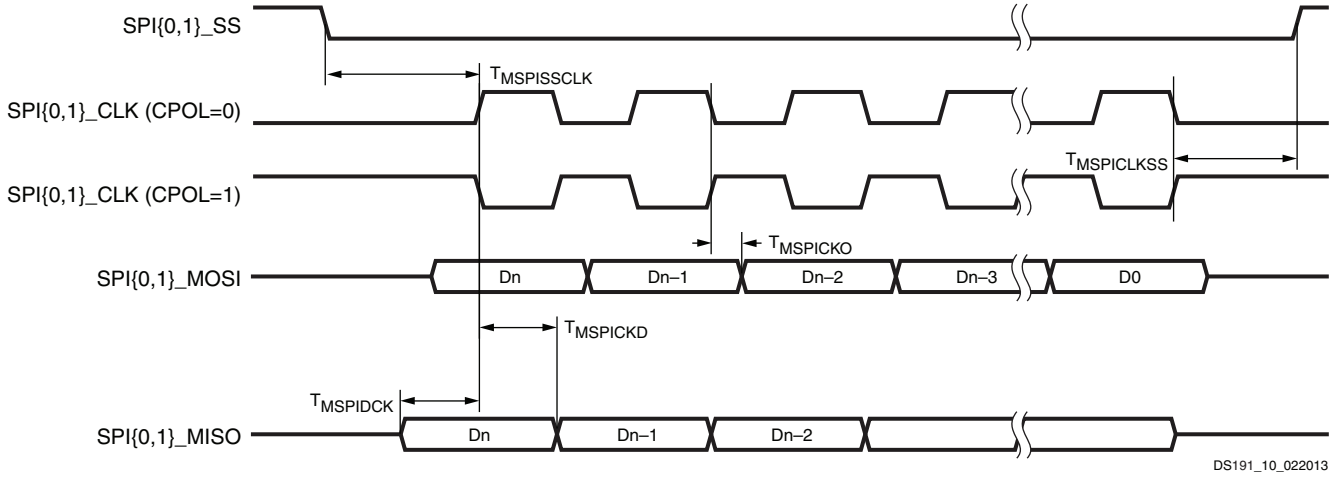

Figure 12: **SPI Master (CPHA = 0) Interface Timing Diagram**

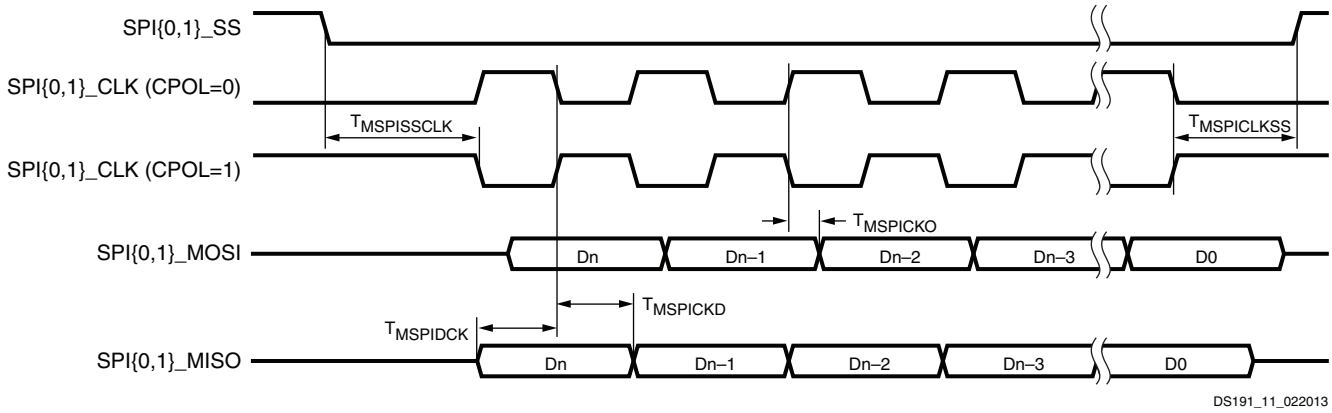

Figure 13: **SPI Master (CPHA = 1) Interface Timing Diagram**

Table 44: **SPI Slave Mode Interface Switching Characteristics(1)(2)**

Symbol	Description	Min	Max	Units
$T_{SSPIDCK}$	Input setup time for SPI{0,1}_MOSI and SPI{0,1}_SS	1	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{SSPICKD}$	Input hold time for SPI{0,1}_MOSI and SPI{0,1}_SS	1	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{SSPICKO}$	Output delay for SPI{0,1}_MISO	0	2.6	$F_{SPI\_REF\_CLK}$ cycles
$T_{SSPISSCLK}$	Slave select asserted to first active clock edge	1	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{SSPICLKSS}$	Last active clock edge to slave select deasserted	1	–	$F_{SPI\_REF\_CLK}$ cycles
$F_{SSPICLK}$	SPI slave mode device clock frequency	–	25	MHz
$F_{SPI\_REF\_CLK}$	SPI reference clock frequency	–	200	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.
2. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

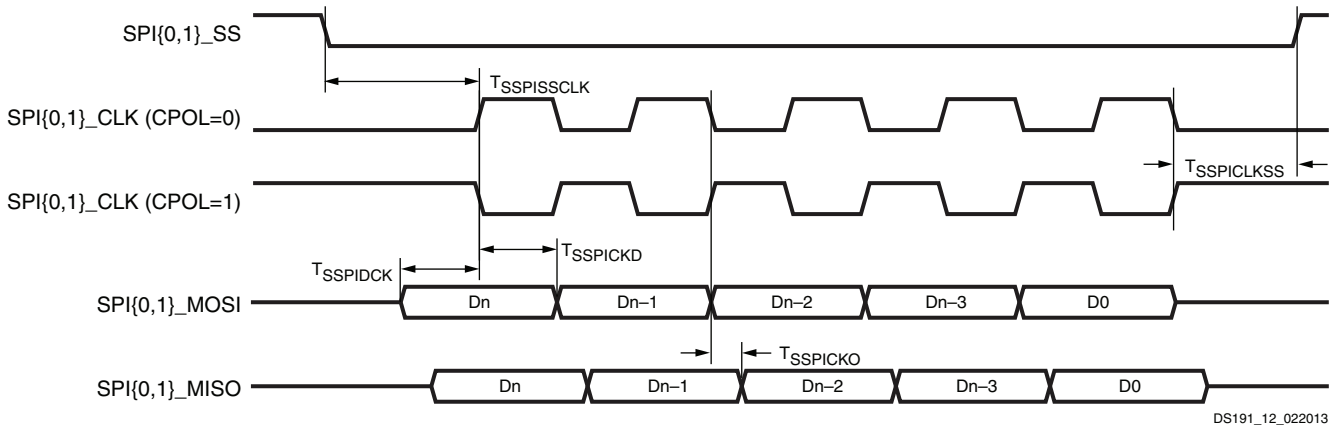

Figure 14: **SPI Slave (CPHA = 0) Interface Timing Diagram**

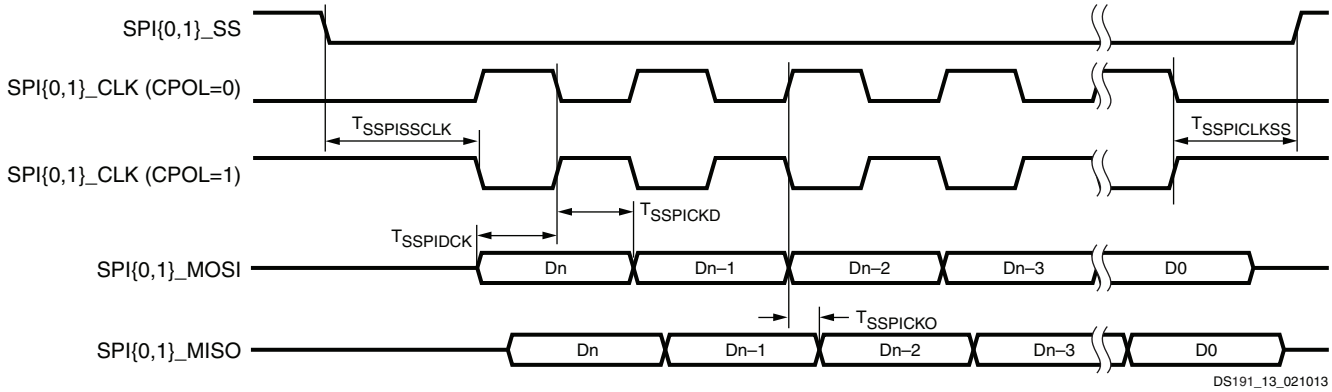

Figure 15: **SPI Slave (CPHA = 1) Interface Timing Diagram**

CAN Interfaces

Table 45: **CAN Interface Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
$T_{PWCANRX}$	Minimum receive pulse width	1	–	µs
$T_{PWCANTX}$	Minimum transmit pulse width	1	–	µs
$F_{CAN\_REF\_CLK}$	Internally sourced CAN reference clock frequency	–	100	MHz
	Externally sourced CAN reference clock frequency	–	40	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

PJTAG Interfaces

Table 46: **PJTAG Interface(1)(2)**

Symbol	Description	Min	Max	Units
$T_{PJTAGDCK}$	PJTAG input setup time	2.4	–	ns
$T_{PJTAGCKD}$	PJTAG input hold time	2.0	–	ns
$T_{PJTAGCKO}$	PJTAG clock to out delay	–	12.5	ns
$T_{PJTAGCLK}$	PJTAG clock frequency	–	20	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.
2. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

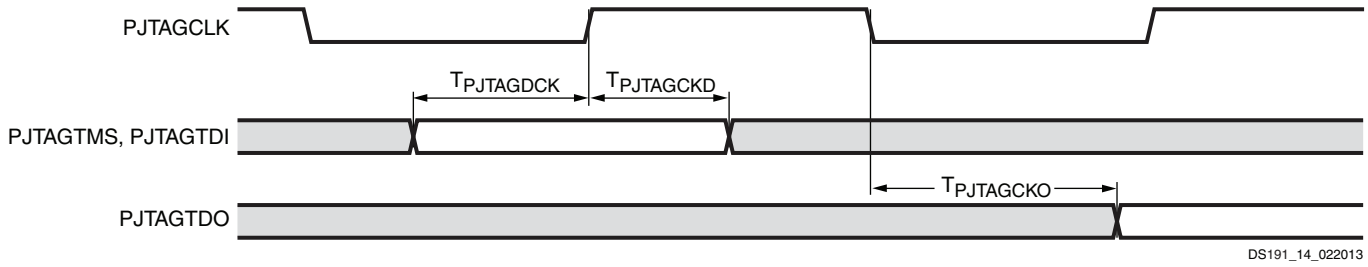

Figure 16: **PJTAG Interface Timing Diagram**

UART Interfaces

Table 47: **UART Interface Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
$BAUD_{TXMAX}$	Maximum transmit baud rate	–	1	Mb/s
$BAUD_{RXMAX}$	Maximum receive baud rate	–	1	Mb/s
$F_{UART\_REF\_CLK}$	UART reference clock frequency	–	100	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

GPIO Interfaces

Table 48: **GPIO Banks Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
$T_{PWGPIOH}$	Input high pulse width	10 x 1/cpu1x	–	µs
$T_{PWGPIOL}$	Input low pulse width	10 x 1/cpu1x	–	µs

Notes:

1. Pulse width requirement for interrupt.

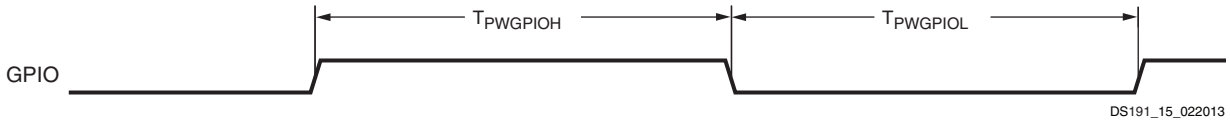

Figure 17: **GPIO Interface Timing Diagram**

Trace Interface

Table 49: **Trace Interface Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
T_{TCECKO}	Trace clock to output delay, all outputs	–1.4	1.5	ns
$T_{DCTCECLK}$	Trace clock duty cycle	40	60	%
F_{TCECLK}	Trace clock frequency	–	80	MHz

Notes:

1. Test conditions: LVCMOS25, fast slew rate, 8 mA drive strength, 15 pF loads.

Triple Timer Counter Interface

Table 50: **Triple Timer Counter interface Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
$T_{PWTTCOCLK}$	Triple timer counter output clock pulse width	2 x 1/cpu1x	–	ns
$F_{TTCOCLK}$	Triple timer counter output clock frequency	–	cpu1x/4	MHz
$T_{TTCICLKH}$	Triple timer counter input clock high pulse width	1.5 x 1/cpu1x	–	ns
$T_{TTCICLKL}$	Triple timer counter input clock low pulse width	1.5 x 1/cpu1x	–	ns
$F_{TTCICLK}$	Triple timer counter input clock frequency	–	cpu1x/3	MHz

Notes:

1. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

Watchdog Timer

Table 51: **Watchdog Timer Switching Characteristics**

Symbol	Description	Min	Max	Units
F_{WDTCLK}(1)	Watchdog timer input clock frequency	–	10	MHz

Notes:

1. Applies to external input clock through MIO pin only.

PL Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in the PL. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the AC Switching Characteristics, page 15. In each table, the I/O bank type is either High Performance (HP) or High Range (HR).

Table 52: **PL Networking Applications Interface Performances**

Description	I/O Bank Type	Speed Grade				Units
		-3E	-2E/-2I/-2LI	-1C/-1I	-1Q/-1LQ	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	HR	710	710	625	625	Mb/s
	HP	710	710	625	625	Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14)	HR	1250	1250	950	950	Mb/s
	HP	1600	1400	1250	1250	Mb/s
SDR LVDS receiver (SFI-4.1)(1)	HR	710	710	625	625	Mb/s
	HP	710	710	625	625	Mb/s
DDR LVDS receiver (SPI-4.2)(1)	HR	1250	1250	950	950	Mb/s
	HP	1600	1400	1250	1250	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

Table 53 provides the maximum data rates for applicable memory standards using the Zynq-7000 AP SoC memory PHY. The final performance of the memory interface is determined through a complete design implemented in the Vivado or ISE Design Suite, following guidelines in the *Zynq-7000 AP SoC and 7 Series Devices Memory Interface Solutions User Guide* (UG586).

Table 53: **Maximum Physical Interface (PHY) Rate for Memory Interfaces IP available with the Memory Interface Generator (FF and RF Packages)(1)(2)**

Memory Standard	I/O Bank Type	V_{CCAUX_IO}	Speed Grade					Units
			-3E	-2E/-2I	-2LI	-1C/-1I	-1Q/-1LQ	
4:1 Memory Controllers								
DDR3	HP	2.0V	1866(3)	1866(3)	1600	1600	1066	Mb/s
	HP	1.8V	1600	1333	1333	1066	800	Mb/s
	HR	N/A	1066	1066	1066	800	800	Mb/s
DDR3L	HP	2.0V	1600	1600	1600	1333	1066	Mb/s
	HP	1.8V	1333	1066	1066	800	800	Mb/s
	HR	N/A	800	800	800	667	N/A	Mb/s
DDR2	HP	2.0V	800	800	800	800	667	Mb/s
	HP	1.8V	800	800	800	800	667	Mb/s
	HR	N/A	800	800	800	800	533	Mb/s
RLDRAM III	HP	2.0V	800	667	667	667	550	MHz
	HP	1.8V	550	500	500	450	400	MHz
	HR	N/A	N/A					
2:1 Memory Controllers								
DDR3	HP	2.0V	1066	1066	1066	800	667	Mb/s
	HP	1.8V						Mb/s
	HR	N/A						Mb/s
DDR3L	HP	2.0V	1066	1066	1066	800	667	Mb/s
	HP	1.8V						Mb/s
	HR	N/A	800	800	800	667	N/A	Mb/s
DDR2	HP	2.0V	800	800	800	800	667	Mb/s
	HP	1.8V					667	
	HR	N/A					533	
QDR II+(4)	HP	2.0V	550	500	500	450	300	MHz
	HP	1.8V						
	HR	N/A	500	450	450	400	300	MHz
RLDRAM II	HP	2.0V	533	500	500	450	400	MHz
	HP	1.8V						
	HR	N/A						
LPDDR2	HP	2.0V	667	667	667	667	533	Mb/s
	HP	1.8V						Mb/s
	HR	N/A						Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see the *Zynq-7000 AP SoC and 7 Series Devices Memory Interface Solutions User Guide* (UG586).
2. When using the internal V_{REF}, the maximum data rate is 800 Mb/s (400 MHz).
3. For designs using 1866 Mb/s components, contact Xilinx Technical Support.
4. The maximum QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations. Burst length 2 (BL = 2) implementations are limited to 333 MHz for all speed grades and I/O bank types.

Table 54: **Maximum Physical Interface (PHY) Rate for Memory Interfaces IP available with the Memory Interface Generator (FB, RB, and SB Packages)(1)(2)**

Memory Standard	I/O Bank Type	V_{CCAUX_IO}(3)	Speed Grade				Units
			-3E	-2E/-2I/-2LI	-1C/-1I	-1Q	
4:1 Memory Controllers							
DDR3	HP	N/A	1333	1066	800	800	Mb/s
	HR	N/A	1066	800	800	800	Mb/s
DDR3L	HP	N/A	1066	800	667	667	Mb/s
	HR	N/A	800	800	667	N/A	Mb/s
DDR2	HP	N/A	800	800	800	667	Mb/s
	HR	N/A	800	667	667	533	Mb/s
RLDRAM III	HP	N/A	550	500	450	350	MHz
	HR	N/A	N/A				
2:1 Memory Controllers							
DDR3	HP	N/A	1066	1066	800	667	Mb/s
	HR	N/A	1066	800	800	667	Mb/s
DDR3L	HP	N/A	1066	800	667	667	Mb/s
	HR	N/A	800	800	667	N/A	Mb/s
DDR2	HP	N/A	800	800	800	667	Mb/s
	HR	N/A	800	667	667	533	Mb/s
QDR II+(4)	HP	N/A	550	500	450	300	MHz
	HR	N/A	450	400	350	300	MHz
RLDRAM II	HP	N/A	533	500	450	400	MHz
	HR	N/A					
LPDDR2	HP	N/A	667	667	667	400	Mb/s
	HR	N/A	667	667	533	400	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see the *Zynq-7000 AP SoC and 7 Series Devices Memory Interface Solutions User Guide* (UG586).
2. When using the internal V_{REF}, the maximum data rate is 800 Mb/s (400 MHz).
3. FB, RB, and SB packages do not have separate V_{CCAUX_IO} supply pins to adjust the pre-driver voltage of the HP I/O banks.
4. The maximum QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations. Burst length 2 (BL = 2) implementations are limited to 333 MHz for all speed grades and I/O bank types.

PL Switching Characteristics

IOB Pad Input/Output/3-State

Table 55 (high-range IOB (HR)) and Table 56 (high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than T_{IOTP} when the DCITERMDISABLE pin is used. In HR I/O banks, the IN_TERM termination turn-on time is always faster than T_{IOTP} when the INTERMDISABLE pin is used.

Table 55: **IOB High Range (HR) Switching Characteristics**

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3E	-2E/-2I/ -2LI	-1C/-1I	-1Q/ -1LQ	-3E	-2E/-2I/ -2LI	-1C/-1I	-1Q/ -1LQ	-3E	-2E/-2I/ -2LI	-1C/-1I	-1Q/ -1LQ	
LVTTL_S4	1.31	1.42	1.64	1.64	3.77	3.90	4.00	4.00	3.52	3.67	3.86	3.86	ns
LVTTL_S8	1.31	1.42	1.64	1.64	3.50	3.64	3.73	3.73	3.26	3.40	3.60	3.60	ns
LVTTL_S12	1.31	1.42	1.64	1.64	3.49	3.62	3.72	3.72	3.24	3.39	3.58	3.58	ns
LVTTL_S16	1.31	1.42	1.64	1.64	3.03	3.17	3.26	3.26	2.79	2.93	3.13	3.13	ns
LVTTL_S24	1.31	1.42	1.64	1.64	3.25	3.39	3.48	3.48	3.01	3.15	3.35	3.35	ns
LVTTL_F4	1.31	1.42	1.64	1.64	3.22	3.36	3.45	3.45	2.98	3.12	3.32	3.32	ns
LVTTL_F8	1.31	1.42	1.64	1.64	2.71	2.84	2.93	2.93	2.46	2.61	2.80	2.80	ns
LVTTL_F12	1.31	1.42	1.64	1.64	2.69	2.82	2.92	2.92	2.44	2.59	2.79	2.79	ns
LVTTL_F16	1.31	1.42	1.64	1.64	2.57	2.85	3.15	3.15	2.33	2.61	3.02	3.02	ns
LVTTL_F24	1.31	1.42	1.64	1.64	2.41	2.64	2.89	3.04	2.16	2.41	2.76	2.91	ns
LVDS_25	0.64	0.68	0.80	0.87	1.36	1.47	1.55	1.55	1.11	1.24	1.41	1.41	ns
MINI_LVDS_25	0.68	0.70	0.79	0.87	1.36	1.47	1.55	1.55	1.11	1.24	1.41	1.41	ns
BLVDS_25	0.65	0.69	0.80	0.85	1.83	2.02	2.20	2.57	1.59	1.79	2.07	2.44	ns
RSDS_25	0.63	0.68	0.79	0.87	1.36	1.48	1.55	1.55	1.11	1.24	1.41	1.41	ns
PPDS_25	0.65	0.69	0.80	0.87	1.36	1.49	1.58	1.58	1.11	1.25	1.45	1.45	ns
TMDS_33	0.72	0.76	0.86	0.90	1.43	1.54	1.60	1.60	1.18	1.31	1.47	1.47	ns
PCI33_3	1.28	1.41	1.65	1.65	2.71	3.08	3.52	3.52	2.46	2.84	3.39	3.39	ns
HSUL_12_S	0.63	0.64	0.71	0.85	1.77	1.90	2.00	2.00	1.52	1.67	1.86	1.86	ns
HSUL_12_F	0.63	0.64	0.71	0.85	1.26	1.40	1.50	1.50	1.01	1.16	1.37	1.37	ns
DIFF_HSUL_12_S	0.58	0.61	0.70	0.84	1.55	1.68	1.78	1.78	1.30	1.45	1.65	1.65	ns
DIFF_HSUL_12_F	0.58	0.61	0.70	0.84	1.16	1.28	1.35	1.35	0.92	1.04	1.21	1.21	ns
MOBILE_DDR_S	0.64	0.66	0.74	0.74	2.58	2.91	3.31	3.31	2.33	2.68	3.17	3.17	ns
MOBILE_DDR_F	0.64	0.66	0.74	0.74	1.91	2.13	2.36	2.36	1.66	1.89	2.23	2.23	ns
DIFF_MOBILE_DDR_S	0.63	0.66	0.75	0.75	2.51	2.84	3.24	3.24	2.26	2.61	3.10	3.10	ns
DIFF_MOBILE_DDR_F	0.63	0.66	0.75	0.75	1.89	2.11	2.34	2.34	1.64	1.88	2.21	2.21	ns
HSTL_I_S	0.61	0.64	0.73	0.84	1.55	1.69	1.80	1.80	1.30	1.46	1.67	1.67	ns

Table 55: **IOB High Range (HR) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3E	-2E/-2I/ -2LI	-1C/-1I	-1Q/ -1LQ	-3E	-2E/-2I/ -2LI	-1C/-1I	-1Q/ -1LQ	-3E	-2E/-2I/ -2LI	-1C/-1I	-1Q/ -1LQ	
HSTL_II_S	0.61	0.64	0.73	0.84	1.21	1.34	1.43	1.61	0.96	1.11	1.30	1.47	ns
HSTL_I_18_S	0.64	0.67	0.76	0.85	1.28	1.39	1.45	1.45	1.04	1.16	1.31	1.32	ns
HSTL_II_18_S	0.64	0.67	0.76	0.85	1.18	1.31	1.40	1.57	0.93	1.08	1.27	1.44	ns
DIFF_HSTL_I_S	0.63	0.67	0.77	0.84	1.42	1.54	1.61	1.78	1.17	1.31	1.48	1.65	ns
DIFF_HSTL_II_S	0.63	0.67	0.77	0.84	1.15	1.24	1.27	1.61	0.91	1.01	1.14	1.47	ns
DIFF_HSTL_I_18_S	0.65	0.69	0.78	0.84	1.27	1.38	1.43	1.45	1.03	1.14	1.30	1.32	ns
DIFF_HSTL_II_18_S	0.65	0.69	0.78	0.85	1.14	1.23	1.26	1.57	0.90	1.00	1.13	1.44	ns
HSTL_I_F	0.61	0.64	0.73	0.84	1.10	1.19	1.23	1.31	0.85	0.96	1.10	1.18	ns
HSTL_II_F	0.61	0.64	0.73	0.84	1.05	1.18	1.28	1.31	0.80	0.95	1.15	1.18	ns
HSTL_I_18_F	0.64	0.67	0.76	0.85	1.05	1.18	1.28	1.36	0.80	0.95	1.15	1.22	ns
HSTL_II_18_F	0.64	0.67	0.76	0.85	1.03	1.14	1.23	1.32	0.78	0.90	1.10	1.19	ns
DIFF_HSTL_I_F	0.63	0.67	0.77	0.84	1.09	1.18	1.22	1.31	0.84	0.95	1.09	1.18	ns
DIFF_HSTL_II_F	0.63	0.67	0.77	0.84	1.02	1.11	1.14	1.31	0.77	0.88	1.01	1.18	ns
DIFF_HSTL_I_18_F	0.65	0.69	0.78	0.84	1.08	1.17	1.21	1.36	0.83	0.94	1.07	1.22	ns
DIFF_HSTL_II_18_F	0.65	0.69	0.78	0.85	1.01	1.10	1.13	1.32	0.76	0.87	1.00	1.19	ns
LVCMOS33_S4	1.31	1.40	1.60	1.60	3.77	3.90	4.00	4.00	3.52	3.67	3.86	3.86	ns
LVCMOS33_S8	1.31	1.40	1.60	1.60	3.49	3.62	3.72	3.72	3.24	3.39	3.58	3.58	ns
LVCMOS33_S12	1.31	1.40	1.60	1.60	3.05	3.18	3.28	3.28	2.80	2.95	3.15	3.15	ns
LVCMOS33_S16	1.31	1.40	1.60	1.60	3.06	3.43	3.88	3.88	2.81	3.20	3.75	3.75	ns
LVCMOS33_F4	1.31	1.40	1.60	1.60	3.22	3.36	3.45	3.45	2.98	3.12	3.32	3.32	ns
LVCMOS33_F8	1.31	1.40	1.60	1.60	2.71	2.84	2.93	2.93	2.46	2.61	2.80	2.80	ns
LVCMOS33_F12	1.31	1.40	1.60	1.60	2.57	2.85	3.15	3.15	2.33	2.61	3.02	3.02	ns
LVCMOS33_F16	1.31	1.40	1.60	1.60	2.44	2.69	2.96	2.96	2.19	2.45	2.82	2.82	ns
LVCMOS25_S4	1.08	1.16	1.32	1.35	3.08	3.22	3.31	3.31	2.84	2.98	3.18	3.18	ns
LVCMOS25_S8	1.08	1.16	1.32	1.35	2.85	2.98	3.07	3.08	2.60	2.75	2.94	2.94	ns
LVCMOS25_S12	1.08	1.16	1.32	1.35	2.44	2.57	2.67	2.67	2.19	2.34	2.54	2.54	ns
LVCMOS25_S16	1.08	1.16	1.32	1.35	2.79	2.92	3.01	3.01	2.54	2.68	2.88	2.88	ns
LVCMOS25_F4	1.08	1.16	1.32	1.35	2.71	2.84	2.93	2.93	2.46	2.61	2.80	2.80	ns
LVCMOS25_F8	1.08	1.16	1.32	1.35	2.14	2.28	2.37	2.37	1.90	2.04	2.24	2.24	ns
LVCMOS25_F12	1.08	1.16	1.32	1.35	2.15	2.29	2.52	2.52	1.91	2.05	2.38	2.38	ns
LVCMOS25_F16	1.08	1.16	1.32	1.35	1.92	2.17	2.45	2.45	1.67	1.94	2.32	2.32	ns
LVCMOS18_S4	0.64	0.66	0.74	0.95	1.55	1.68	1.78	1.78	1.30	1.45	1.65	1.65	ns
LVCMOS18_S8	0.64	0.66	0.74	0.95	2.14	2.28	2.37	2.37	1.90	2.04	2.24	2.24	ns
LVCMOS18_S12	0.64	0.66	0.74	0.95	2.14	2.28	2.37	2.37	1.90	2.04	2.24	2.24	ns
LVCMOS18_S16	0.64	0.66	0.74	0.95	1.49	1.62	1.72	1.72	1.24	1.39	1.58	1.58	ns
LVCMOS18_S24	0.64	0.66	0.74	0.95	1.74	1.92	2.08	2.22	1.50	1.69	1.95	2.08	ns

Table 55: **IOB High Range (HR) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3E	-2E/-2I/ -2LI	-1C/-1I	-1Q/ -1LQ	-3E	-2E/-2I/ -2LI	-1C/-1I	-1Q/ -1LQ	-3E	-2E/-2I/ -2LI	-1C/-1I	-1Q/ -1LQ	
LVCMOS18_F4	0.64	0.66	0.74	0.95	1.38	1.51	1.61	1.64	1.13	1.28	1.47	1.50	ns
LVCMOS18_F8	0.64	0.66	0.74	0.95	1.64	1.78	1.87	1.87	1.40	1.54	1.74	1.74	ns
LVCMOS18_F12	0.64	0.66	0.74	0.95	1.64	1.78	1.87	1.87	1.40	1.54	1.74	1.74	ns
LVCMOS18_F16	0.64	0.66	0.74	0.95	1.52	1.68	1.81	1.81	1.28	1.45	1.68	1.68	ns
LVCMOS18_F24	0.64	0.66	0.74	0.95	1.34	1.46	1.55	2.09	1.09	1.23	1.42	1.96	ns
LVCMOS15_S4	0.66	0.69	0.81	0.93	1.86	2.00	2.09	2.09	1.62	1.76	1.96	1.96	ns
LVCMOS15_S8	0.66	0.69	0.81	0.93	2.05	2.18	2.28	2.28	1.80	1.95	2.14	2.15	ns
LVCMOS15_S12	0.66	0.69	0.81	0.93	1.83	2.03	2.23	2.23	1.59	1.80	2.10	2.10	ns
LVCMOS15_S16	0.66	0.69	0.81	0.93	1.76	1.95	2.13	2.13	1.52	1.72	1.99	1.99	ns
LVCMOS15_F4	0.66	0.69	0.81	0.93	1.63	1.76	1.86	1.86	1.38	1.53	1.72	1.72	ns
LVCMOS15_F8	0.66	0.69	0.81	0.93	1.79	1.99	2.18	2.18	1.55	1.76	2.05	2.05	ns
LVCMOS15_F12	0.66	0.69	0.81	0.93	1.40	1.54	1.65	1.65	1.15	1.31	1.52	1.52	ns
LVCMOS15_F16	0.66	0.69	0.81	0.93	1.37	1.51	1.61	1.89	1.13	1.27	1.48	1.75	ns
LVCMOS12_S4	0.88	0.91	1.00	1.17	2.53	2.67	2.76	2.76	2.29	2.43	2.63	2.63	ns
LVCMOS12_S8	0.88	0.91	1.00	1.17	2.05	2.18	2.28	2.28	1.80	1.95	2.14	2.15	ns
LVCMOS12_S12	0.88	0.91	1.00	1.17	1.75	1.89	1.98	1.98	1.51	1.65	1.85	1.85	ns
LVCMOS12_F4	0.88	0.91	1.00	1.17	1.94	2.07	2.17	2.17	1.69	1.84	2.04	2.04	ns
LVCMOS12_F8	0.88	0.91	1.00	1.17	1.50	1.64	1.73	1.73	1.26	1.40	1.60	1.60	ns
LVCMOS12_F12	0.88	0.91	1.00	1.17	1.54	1.71	1.87	1.87	1.29	1.48	1.74	1.74	ns
SSTL135_S	0.61	0.64	0.73	0.85	1.27	1.40	1.50	1.53	1.02	1.17	1.36	1.40	ns
SSTL15_S	0.61	0.64	0.73	0.73	1.24	1.37	1.47	1.53	0.99	1.14	1.33	1.40	ns
SSTL18_I_S	0.64	0.67	0.76	0.84	1.59	1.74	1.85	1.85	1.34	1.50	1.72	1.72	ns
SSTL18_II_S	0.64	0.67	0.76	0.85	1.27	1.40	1.50	1.50	1.02	1.17	1.36	1.36	ns
DIFF_SSTL135_S	0.59	0.61	0.73	0.85	1.27	1.40	1.50	1.53	1.02	1.17	1.36	1.40	ns
DIFF_SSTL15_S	0.63	0.67	0.77	0.85	1.24	1.37	1.47	1.53	0.99	1.14	1.33	1.40	ns
DIFF_SSTL18_I_S	0.65	0.69	0.78	0.85	1.50	1.63	1.72	1.82	1.26	1.40	1.59	1.69	ns
DIFF_SSTL18_II_S	0.65	0.69	0.78	0.85	1.13	1.22	1.25	1.50	0.88	0.99	1.12	1.36	ns
SSTL135_F	0.61	0.64	0.73	0.85	1.04	1.17	1.26	1.31	0.79	0.93	1.13	1.18	ns
SSTL15_F	0.61	0.64	0.73	0.73	1.04	1.17	1.26	1.26	0.79	0.93	1.13	1.13	ns
SSTL18_I_F	0.64	0.67	0.76	0.84	1.12	1.22	1.26	1.34	0.88	0.99	1.13	1.21	ns
SSTL18_II_F	0.64	0.67	0.76	0.85	1.05	1.18	1.28	1.32	0.80	0.95	1.15	1.19	ns
DIFF_SSTL135_F	0.59	0.61	0.73	0.85	1.04	1.17	1.26	1.31	0.79	0.93	1.13	1.18	ns
DIFF_SSTL15_F	0.63	0.67	0.77	0.85	1.04	1.17	1.26	1.26	0.79	0.93	1.13	1.13	ns
DIFF_SSTL18_I_F	0.65	0.69	0.78	0.85	1.10	1.19	1.23	1.34	0.85	0.96	1.10	1.21	ns
DIFF_SSTL18_II_F	0.65	0.69	0.78	0.85	1.02	1.10	1.14	1.32	0.77	0.87	1.00	1.19	ns

Table 56: **IOB High Performance (HP) Switching Characteristics**

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3E	-2E/-2I/ -2LI	-1C/-1I	-1Q/ -1LQ	-3E	-2E/-2I/ -2LI	-1C/-1I	-1Q/ -1LQ	-3E	-2E/-2I/ -2LI	-1C/-1I	-1Q/ -1LQ	
LVDS	0.75	0.79	0.92	0.96	1.05	1.17	1.24	1.26	0.88	1.01	1.08	1.10	ns
HSUL_12_S	0.69	0.72	0.82	0.98	1.65	1.84	2.05	2.05	1.48	1.68	1.89	1.89	ns
HSUL_12_F	0.69	0.72	0.82	0.98	1.39	1.54	1.68	1.68	1.22	1.38	1.52	1.52	ns
DIFF_HSUL_12_S	0.69	0.72	0.82	0.98	1.65	1.84	2.05	2.05	1.48	1.68	1.89	1.89	ns
DIFF_HSUL_12_F	0.69	0.72	0.82	0.98	1.39	1.54	1.68	1.68	1.22	1.38	1.52	1.52	ns
DIFF_HSUL_12_DCI_S	0.69	0.72	0.82	0.82	1.78	1.91	2.05	2.05	1.61	1.76	1.89	1.89	ns
DIFF_HSUL_12_DCI_F	0.69	0.72	0.82	0.82	1.56	1.67	1.76	1.76	1.39	1.51	1.60	1.60	ns
HSTL_I_S	0.68	0.72	0.82	0.90	1.15	1.28	1.38	1.38	0.98	1.12	1.22	1.22	ns
HSTL_II_S	0.68	0.72	0.82	0.90	1.05	1.17	1.26	1.27	0.88	1.01	1.10	1.11	ns
HSTL_I_18_S	0.70	0.72	0.82	0.95	1.12	1.24	1.34	1.34	0.95	1.08	1.18	1.18	ns
HSTL_II_18_S	0.70	0.72	0.82	0.90	1.06	1.18	1.26	1.27	0.89	1.02	1.10	1.11	ns
HSTL_I_12_S	0.68	0.72	0.82	0.96	1.14	1.27	1.37	1.37	0.97	1.11	1.21	1.21	ns
HSTL_I_DCI_S	0.68	0.72	0.82	0.90	1.11	1.23	1.33	1.33	0.94	1.07	1.17	1.17	ns
HSTL_II_DCI_S	0.68	0.72	0.82	0.85	1.05	1.17	1.26	1.26	0.88	1.01	1.10	1.10	ns
HSTL_II_T_DCI_S	0.70	0.72	0.82	0.82	1.15	1.28	1.38	1.38	0.98	1.12	1.22	1.22	ns
HSTL_I_DCI_18_S	0.70	0.72	0.82	0.90	1.11	1.23	1.33	1.33	0.94	1.07	1.17	1.17	ns
HSTL_II_DCI_18_S	0.70	0.72	0.82	0.82	1.05	1.16	1.24	1.24	0.88	1.00	1.08	1.08	ns
HSTL_II _T_DCI_18_S	0.70	0.72	0.82	0.84	1.11	1.23	1.33	1.34	0.94	1.07	1.17	1.18	ns
DIFF_HSTL_I_S	0.75	0.79	0.92	1.02	1.15	1.28	1.38	1.38	0.98	1.12	1.22	1.22	ns
DIFF_HSTL_II_S	0.75	0.79	0.92	1.02	1.05	1.17	1.26	1.32	0.88	1.01	1.10	1.16	ns
DIFF_HSTL_I_DCI_S	0.75	0.79	0.92	0.92	1.15	1.28	1.38	1.38	0.98	1.12	1.22	1.22	ns
DIFF_HSTL_II_DCI_S	0.75	0.79	0.92	0.92	1.05	1.17	1.26	1.26	0.88	1.01	1.10	1.10	ns
DIFF_HSTL_I_18_S	0.75	0.79	0.92	0.98	1.12	1.24	1.34	1.34	0.95	1.08	1.18	1.18	ns
DIFF_HSTL_II_18_S	0.75	0.79	0.92	0.99	1.06	1.18	1.26	1.32	0.89	1.02	1.10	1.16	ns
DIFF_HSTL_I_DCI_18_S	0.75	0.79	0.92	0.92	1.11	1.23	1.33	1.33	0.94	1.07	1.17	1.17	ns
DIFF_HSTL_II_DCI_18_S	0.75	0.79	0.92	0.93	1.05	1.16	1.24	1.26	0.88	1.00	1.08	1.10	ns
DIFF_HSTL_II _T_DCI_18_S	0.75	0.79	0.92	0.92	1.11	1.23	1.33	1.33	0.94	1.07	1.17	1.17	ns
HSTL_I_F	0.68	0.72	0.82	0.90	1.02	1.14	1.22	1.22	0.85	0.98	1.06	1.06	ns
HSTL_II_F	0.68	0.72	0.82	0.90	0.97	1.08	1.15	1.15	0.80	0.92	0.99	0.99	ns
HSTL_I_18_F	0.70	0.72	0.82	0.95	1.04	1.16	1.24	1.24	0.87	1.00	1.08	1.08	ns
HSTL_II_18_F	0.70	0.72	0.82	0.90	0.98	1.09	1.16	1.20	0.81	0.94	1.00	1.03	ns
HSTL_I_12_F	0.68	0.72	0.82	0.96	1.02	1.13	1.21	1.21	0.85	0.97	1.05	1.05	ns
HSTL_I_DCI_F	0.68	0.72	0.82	0.90	1.04	1.16	1.24	1.24	0.87	1.00	1.08	1.08	ns
HSTL_II_DCI_F	0.68	0.72	0.82	0.85	0.97	1.08	1.15	1.15	0.80	0.92	0.99	0.99	ns
HSTL_II_T_DCI_F	0.70	0.72	0.82	0.82	1.02	1.14	1.22	1.22	0.85	0.98	1.06	1.06	ns
HSTL_I_DCI_18_F	0.70	0.72	0.82	0.90	1.04	1.16	1.24	1.24	0.87	1.00	1.08	1.08	ns
HSTL_II_DCI_18_F	0.70	0.72	0.82	0.82	0.98	1.09	1.16	1.16	0.81	0.93	1.00	1.00	ns
HSTL_II _T_DCI_18_F	0.70	0.72	0.82	0.84	1.04	1.16	1.24	1.24	0.87	1.00	1.08	1.08	ns

Table 56: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3E	-2E/-2I/ -2LI	-1C/-1I	-1Q/ -1LQ	-3E	-2E/-2I/ -2LI	-1C/-1I	-1Q/ -1LQ	-3E	-2E/-2I/ -2LI	-1C/-1I	-1Q/ -1LQ	
DIFF_HSTL_I_F	0.75	0.79	0.92	1.02	1.02	1.14	1.22	1.22	0.85	0.98	1.06	1.06	ns
DIFF_HSTL_II_F	0.75	0.79	0.92	1.02	0.97	1.08	1.15	1.20	0.80	0.92	0.99	1.03	ns
DIFF_HSTL_I_DCI_F	0.75	0.79	0.92	0.92	1.02	1.14	1.22	1.22	0.85	0.98	1.06	1.06	ns
DIFF_HSTL_II_DCI_F	0.75	0.79	0.92	0.92	0.97	1.08	1.15	1.15	0.80	0.92	0.99	0.99	ns
DIFF_HSTL_I_18_F	0.75	0.79	0.92	0.98	1.04	1.16	1.24	1.24	0.87	1.00	1.08	1.08	ns
DIFF_HSTL_II_18_F	0.75	0.79	0.92	0.99	0.98	1.09	1.16	1.24	0.81	0.94	1.00	1.08	ns
DIFF_HSTL_I_DCI_18_F	0.75	0.79	0.92	0.92	1.04	1.16	1.24	1.24	0.87	1.00	1.08	1.08	ns
DIFF_HSTL_II_DCI_18_F	0.75	0.79	0.92	0.93	0.98	1.09	1.16	1.18	0.81	0.93	1.00	1.02	ns
DIFF_HSTL_II _T_DCI_18_F	0.75	0.79	0.92	0.92	1.04	1.16	1.24	1.24	0.87	1.00	1.08	1.08	ns
LVCMOS18_S2	0.47	0.50	0.60	0.90	3.95	4.28	4.85	4.85	3.78	4.13	4.69	4.69	ns
LVCMOS18_S4	0.47	0.50	0.60	0.90	2.67	2.98	3.43	3.43	2.50	2.82	3.27	3.27	ns
LVCMOS18_S6	0.47	0.50	0.60	0.90	2.14	2.38	2.72	2.72	1.97	2.22	2.56	2.56	ns
LVCMOS18_S8	0.47	0.50	0.60	0.90	1.98	2.21	2.52	2.52	1.81	2.05	2.36	2.36	ns
LVCMOS18_S12	0.47	0.50	0.60	0.90	1.70	1.91	2.17	2.17	1.53	1.75	2.01	2.01	ns
LVCMOS18_S16	0.47	0.50	0.60	0.90	1.57	1.75	1.97	1.97	1.40	1.59	1.81	1.81	ns
LVCMOS18_F2	0.47	0.50	0.60	0.90	3.50	3.87	4.48	4.48	3.33	3.71	4.32	4.32	ns
LVCMOS18_F4	0.47	0.50	0.60	0.90	2.23	2.50	2.87	2.87	2.06	2.34	2.71	2.71	ns
LVCMOS18_F6	0.47	0.50	0.60	0.90	1.80	2.00	2.26	2.26	1.63	1.84	2.09	2.09	ns
LVCMOS18_F8	0.47	0.50	0.60	0.90	1.46	1.72	2.04	2.04	1.29	1.56	1.88	1.88	ns
LVCMOS18_F12	0.47	0.50	0.60	0.90	1.26	1.40	1.53	1.53	1.09	1.24	1.37	1.37	ns
LVCMOS18_F16	0.47	0.50	0.60	0.90	1.19	1.33	1.44	1.66	1.02	1.17	1.28	1.50	ns
LVCMOS15_S2	0.59	0.62	0.73	0.88	3.55	3.89	4.45	4.45	3.38	3.73	4.29	4.29	ns
LVCMOS15_S4	0.59	0.62	0.73	0.88	2.45	2.70	3.06	3.06	2.28	2.54	2.90	2.90	ns
LVCMOS15_S6	0.59	0.62	0.73	0.88	2.24	2.51	2.88	2.88	2.07	2.35	2.72	2.72	ns
LVCMOS15_S8	0.59	0.62	0.73	0.88	1.91	2.16	2.49	2.49	1.74	2.00	2.32	2.32	ns
LVCMOS15_S12	0.59	0.62	0.73	0.88	1.77	1.98	2.23	2.23	1.60	1.82	2.07	2.07	ns
LVCMOS15_S16	0.59	0.62	0.73	0.88	1.62	1.81	2.02	2.02	1.45	1.65	1.86	1.86	ns
LVCMOS15_F2	0.59	0.62	0.73	0.88	3.38	3.69	4.18	4.18	3.21	3.53	4.02	4.02	ns
LVCMOS15_F4	0.59	0.62	0.73	0.88	2.04	2.21	2.44	2.44	1.87	2.06	2.27	2.27	ns
LVCMOS15_F6	0.59	0.62	0.73	0.88	1.47	1.74	2.09	2.09	1.30	1.58	1.93	1.93	ns
LVCMOS15_F8	0.59	0.62	0.73	0.88	1.31	1.46	1.61	1.61	1.14	1.30	1.45	1.45	ns
LVCMOS15_F12	0.59	0.62	0.73	0.88	1.21	1.34	1.45	1.45	1.04	1.18	1.29	1.29	ns
LVCMOS15_F16	0.59	0.62	0.73	0.88	1.18	1.31	1.41	1.68	1.01	1.15	1.25	1.52	ns
LVCMOS12_S2	0.64	0.67	0.78	1.04	3.38	3.80	4.48	4.48	3.21	3.64	4.31	4.31	ns
LVCMOS12_S4	0.64	0.67	0.78	1.04	2.62	2.94	3.43	3.43	2.45	2.78	3.27	3.27	ns
LVCMOS12_S6	0.64	0.67	0.78	1.04	2.05	2.33	2.72	2.72	1.88	2.17	2.56	2.56	ns
LVCMOS12_S8	0.64	0.67	0.78	1.04	1.94	2.18	2.51	2.51	1.77	2.02	2.34	2.34	ns

Table 56: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3E	-2E/-2I/ -2LI	-1C/-1I	-1Q/ -1LQ	-3E	-2E/-2I/ -2LI	-1C/-1I	-1Q/ -1LQ	-3E	-2E/-2I/ -2LI	-1C/-1I	-1Q/ -1LQ	
LVCMOS12_F2	0.64	0.67	0.78	1.04	2.84	3.15	3.62	3.62	2.67	2.99	3.46	3.46	ns
LVCMOS12_F4	0.64	0.67	0.78	1.04	1.97	2.18	2.44	2.44	1.80	2.02	2.28	2.28	ns
LVCMOS12_F6	0.64	0.67	0.78	1.04	1.33	1.51	1.70	1.70	1.16	1.35	1.54	1.54	ns
LVCMOS12_F8	0.64	0.67	0.78	1.04	1.27	1.42	1.55	1.55	1.10	1.26	1.39	1.39	ns
LVDCI_18	0.47	0.50	0.60	0.87	1.99	2.15	2.35	2.35	1.82	1.99	2.19	2.19	ns
LVDCI_15	0.59	0.62	0.73	0.92	1.98	2.23	2.58	2.58	1.81	2.07	2.41	2.41	ns
LVDCI_DV2_18	0.47	0.50	0.60	0.88	1.99	2.15	2.34	2.34	1.82	1.99	2.18	2.18	ns
LVDCI_DV2_15	0.59	0.62	0.73	0.88	1.98	2.23	2.58	2.58	1.81	2.07	2.41	2.41	ns
HSLVDCI_18	0.68	0.72	0.82	0.90	1.99	2.15	2.35	2.35	1.82	1.99	2.19	2.19	ns
HSLVDCI_15	0.68	0.72	0.82	0.93	1.98	2.23	2.58	2.58	1.81	2.07	2.41	2.41	ns
SSTL18_I_S	0.68	0.72	0.82	0.95	1.02	1.15	1.24	1.24	0.85	0.99	1.08	1.08	ns
SSTL18_II_S	0.68	0.72	0.82	1.01	1.17	1.29	1.37	1.38	1.00	1.13	1.21	1.22	ns
SSTL18_I_DCI_S	0.68	0.72	0.82	0.87	0.92	1.06	1.17	1.18	0.75	0.90	1.01	1.02	ns
SSTL18_II_DCI_S	0.68	0.72	0.82	0.82	0.88	0.98	1.08	1.12	0.71	0.83	0.92	0.96	ns
SSTL18_II_T_DCI_S	0.68	0.72	0.82	0.98	0.92	1.06	1.17	1.18	0.75	0.90	1.01	1.02	ns
SSTL15_S	0.68	0.72	0.82	0.82	0.94	1.06	1.15	1.16	0.77	0.91	0.99	1.00	ns
SSTL15_DCI_S	0.68	0.72	0.82	0.90	0.94	1.06	1.15	1.16	0.77	0.90	0.99	1.00	ns
SSTL15_T_DCI_S	0.68	0.72	0.82	0.87	0.94	1.06	1.15	1.15	0.77	0.90	0.99	0.99	ns
SSTL135_S	0.69	0.72	0.82	0.93	0.97	1.10	1.19	1.20	0.80	0.94	1.03	1.03	ns
SSTL135_DCI_S	0.69	0.72	0.82	0.85	0.97	1.09	1.19	1.20	0.80	0.93	1.03	1.03	ns
SSTL135_T_DCI_S	0.69	0.72	0.82	0.93	0.97	1.09	1.19	1.20	0.80	0.93	1.03	1.03	ns
SSTL12_S	0.69	0.72	0.82	1.02	0.96	1.09	1.18	1.18	0.79	0.93	1.02	1.02	ns
SSTL12_DCI_S	0.69	0.72	0.82	0.90	1.03	1.17	1.27	1.27	0.86	1.01	1.11	1.11	ns
SSTL12_T_DCI_S	0.69	0.72	0.82	0.88	1.03	1.17	1.27	1.27	0.86	1.01	1.11	1.11	ns
DIFF_SSTL18_I_S	0.75	0.79	0.92	0.99	1.02	1.15	1.24	1.29	0.85	0.99	1.08	1.13	ns
DIFF_SSTL18_II_S	0.75	0.79	0.92	0.93	1.17	1.29	1.37	1.40	1.00	1.13	1.21	1.24	ns
DIFF_SSTL18_I_DCI_S	0.75	0.79	0.92	0.92	0.92	1.06	1.17	1.24	0.75	0.90	1.01	1.08	ns
DIFF_SSTL18_II_DCI_S	0.75	0.79	0.92	0.96	0.88	0.98	1.08	1.18	0.71	0.83	0.92	1.02	ns
DIFF_SSTL18_II_T_DCI_S	0.75	0.79	0.92	0.92	0.92	1.06	1.17	1.24	0.75	0.90	1.01	1.08	ns
DIFF_SSTL15_S	0.68	0.72	0.82	0.99	0.94	1.06	1.15	1.16	0.77	0.91	0.99	1.00	ns
DIFF_SSTL15_DCI_S	0.68	0.72	0.82	0.96	0.94	1.06	1.15	1.16	0.77	0.90	0.99	1.00	ns
DIFF_SSTL15_T_DCI_S	0.68	0.72	0.82	0.88	0.94	1.06	1.15	1.23	0.77	0.90	0.99	1.07	ns
DIFF_SSTL135_S	0.69	0.72	0.82	1.09	0.97	1.10	1.19	1.20	0.80	0.94	1.03	1.03	ns
DIFF_SSTL135_DCI_S	0.69	0.72	0.82	0.90	0.97	1.09	1.19	1.20	0.80	0.93	1.03	1.03	ns
DIFF_SSTL135_T_DCI_S	0.69	0.72	0.82	0.84	0.97	1.09	1.19	1.27	0.80	0.93	1.03	1.11	ns
DIFF_SSTL12_S	0.69	0.72	0.82	0.96	0.96	1.09	1.18	1.18	0.79	0.93	1.02	1.02	ns
DIFF_SSTL12_DCI_S	0.69	0.72	0.82	0.87	1.03	1.17	1.27	1.27	0.86	1.01	1.11	1.11	ns
DIFF_SSTL12_T_DCI_S	0.69	0.72	0.82	0.96	1.03	1.17	1.27	1.27	0.86	1.01	1.11	1.11	ns

Table 56: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3E	-2E/-2I/ -2LI	-1C/-1I	-1Q/ -1LQ	-3E	-2E/-2I/ -2LI	-1C/-1I	-1Q/ -1LQ	-3E	-2E/-2I/ -2LI	-1C/-1I	-1Q/ -1LQ	
SSTL18_I_F	0.68	0.72	0.82	0.95	0.94	1.06	1.15	1.15	0.77	0.91	0.99	0.99	ns
SSTL18_II_F	0.68	0.72	0.82	1.01	0.97	1.09	1.16	1.21	0.80	0.93	1.00	1.05	ns
SSTL18_I_DCI_F	0.68	0.72	0.82	0.87	0.89	1.02	1.10	1.15	0.72	0.86	0.94	0.99	ns
SSTL18_II_DCI_F	0.68	0.72	0.82	0.82	0.89	1.02	1.10	1.10	0.72	0.86	0.94	0.94	ns
SSTL18_II_T_DCI_F	0.68	0.72	0.82	0.98	0.89	1.02	1.10	1.15	0.72	0.86	0.94	0.99	ns
SSTL15_F	0.68	0.72	0.82	0.82	0.89	1.01	1.09	1.09	0.72	0.85	0.93	0.93	ns
SSTL15_DCI_F	0.68	0.72	0.82	0.90	0.89	1.01	1.09	1.12	0.72	0.85	0.93	0.96	ns
SSTL15_T_DCI_F	0.68	0.72	0.82	0.87	0.89	1.01	1.09	1.12	0.72	0.85	0.93	0.96	ns
SSTL135_F	0.69	0.72	0.82	0.93	0.88	1.00	1.08	1.12	0.71	0.85	0.92	0.96	ns
SSTL135_DCI_F	0.69	0.72	0.82	0.85	0.89	1.00	1.08	1.12	0.72	0.85	0.92	0.96	ns
SSTL135_T_DCI_F	0.69	0.72	0.82	0.93	0.89	1.00	1.08	1.12	0.72	0.85	0.92	0.96	ns
SSTL12_F	0.69	0.72	0.82	1.02	0.88	1.00	1.08	1.12	0.71	0.84	0.92	0.96	ns
SSTL12_DCI_F	0.69	0.72	0.82	0.90	0.91	1.03	1.11	1.11	0.74	0.88	0.95	0.95	ns
SSTL12_T_DCI_F	0.69	0.72	0.82	0.88	0.91	1.03	1.11	1.12	0.74	0.88	0.95	0.96	ns
DIFF_SSTL18_I_F	0.75	0.79	0.92	0.99	0.94	1.06	1.15	1.23	0.77	0.91	0.99	1.07	ns
DIFF_SSTL18_II_F	0.75	0.79	0.92	0.93	0.97	1.09	1.16	1.24	0.80	0.93	1.00	1.08	ns
DIFF_SSTL18_I_DCI_F	0.75	0.79	0.92	0.92	0.89	1.02	1.10	1.23	0.72	0.86	0.94	1.07	ns
DIFF_SSTL18_II_DCI_F	0.75	0.79	0.92	0.96	0.89	1.02	1.10	1.16	0.72	0.86	0.94	1.00	ns
DIFF_SSTL18_II_T_DCI_F	0.75	0.79	0.92	0.92	0.89	1.02	1.10	1.24	0.72	0.86	0.94	1.08	ns
DIFF_SSTL15_F	0.68	0.72	0.82	0.99	0.89	1.01	1.09	1.09	0.72	0.85	0.93	0.93	ns
DIFF_SSTL15_DCI_F	0.68	0.72	0.82	0.96	0.89	1.01	1.09	1.12	0.72	0.85	0.93	0.96	ns
DIFF_SSTL15_T_DCI_F	0.68	0.72	0.82	0.88	0.89	1.01	1.09	1.20	0.72	0.85	0.93	1.03	ns
DIFF_SSTL135_F	0.69	0.72	0.82	1.09	0.88	1.00	1.08	1.12	0.71	0.85	0.92	0.96	ns
DIFF_SSTL135_DCI_F	0.69	0.72	0.82	0.90	0.89	1.00	1.08	1.12	0.72	0.85	0.92	0.96	ns
DIFF_SSTL135_T_DCI_F	0.69	0.72	0.82	0.84	0.89	1.00	1.08	1.20	0.72	0.85	0.92	1.03	ns
DIFF_SSTL12_F	0.69	0.72	0.82	0.96	0.88	1.00	1.08	1.12	0.71	0.84	0.92	0.96	ns
DIFF_SSTL12_DCI_F	0.69	0.72	0.82	0.87	0.91	1.03	1.11	1.11	0.74	0.88	0.95	0.95	ns
DIFF_SSTL12_T_DCI_F	0.69	0.72	0.82	0.96	0.91	1.03	1.11	1.18	0.74	0.88	0.95	1.02	ns

Table 57 specifies the values of T_{IOTPHZ} and $T_{IOIBUFDISABLE}$. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{IOIBUFDISABLE}$ is described as the IOB delay from IBUFDISABLE to O output. In HP I/O banks, the internal DCI termination turn-off time is always faster than T_{IOTPHZ} when the DCITERMDISABLE pin is used. In HR I/O banks, the internal IN_TERM termination turn-off time is always faster than T_{IOTPHZ} when the INTERMDISABLE pin is used.

Table 57: **IOB 3-state Output Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3E	-2E/-2I/-2LI	-1C/-1I	-1Q/-1LQ	
T_{IOTPHZ}	T input to pad high-impedance	0.76	0.86	0.99	0.99	ns
$T_{IOIBUFDISABLE\_HR}$	IBUF turn-on time from IBUFDISABLE to O output for HR I/O banks	1.72	1.89	2.14	2.14	ns
$T_{IOIBUFDISABLE\_HP}$	IBUF turn-on time from IBUFDISABLE to O output for HP I/O banks	1.31	1.46	1.76	1.76	ns

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 58 shows the test setup parameters used for measuring input delay.

Table 58: **Input Delay Measurement Methodology**

Description	I/O Standard Attribute	V_L (1)(2)	V_H (1)(2)	V_{MEAS} (1)(4)(6)	V_{REF} (1)(3)(5)
LVCMOS, 1.2V	LVCMOS12	0.1	1.1	0.6	–
LVCMOS, 1.5V	LVCMOS15	0.1	1.4	0.75	–
LVCMOS, 1.8V	LVCMOS18	0.1	1.7	0.9	–
LVCMOS, 2.5V	LVCMOS25	0.1	2.4	1.25	–
LVCMOS, 3.3V	LVCMOS33	0.1	3.2	1.75	–
LVTTL, 3.3V	LVTTL	0.1	3.2	1.75	–
MOBILE_DDR, 1.8V	MOBILE_DDR	0.1	1.7	0.9	–
PCI33, 3.3V	PCI33_3	0.1	3.2	1.32	–
HSTL (High-Speed Transceiver Logic), Class I, 1.2V	HSTL_I_12	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.60
HSTL, Class I & II, 1.5V	HSTL_I, HSTL_II	V_{REF} – 0.65	V_{REF} + 0.65	V_{REF}	0.75
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	V_{REF} – 0.8	V_{REF} + 0.8	V_{REF}	0.90
HSUL (High-Speed Unterminated Logic), 1.2V	HSUL_12	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.60
SSTL (Stub Terminated Transceiver Logic), 1.2V	SSTL12	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.60
SSTL, 1.35V	SSTL135, SSTL135_R	V_{REF} – 0.575	V_{REF} + 0.575	V_{REF}	0.675
SSTL, 1.5V	SSTL15, SSTL15_R	V_{REF} – 0.65	V_{REF} + 0.65	V_{REF}	0.75
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	V_{REF} – 0.8	V_{REF} + 0.8	V_{REF}	0.90
DIFF_MOBILE_DDR, 1.8V	DIFF_MOBILE_DDR	0.9 – 0.125	0.9 + 0.125	0 (6)	–
DIFF_HSTL, Class I, 1.2V	DIFF_HSTL_I_12	0.6 – 0.125	0.6 + 0.125	0 (6)	–
DIFF_HSTL, Class I & II,1.5V	DIFF_HSTL_I, DIFF_HSTL_II	0.75 – 0.125	0.75 + 0.125	0 (6)	–
DIFF_HSTL, Class I & II, 1.8V	DIFF_HSTL_I_18, DIFF_HSTL_II_18	0.9 – 0.125	0.9 + 0.125	0 (6)	–
DIFF_HSUL, 1.2V	DIFF_HSUL_12	0.6 – 0.125	0.6 + 0.125	0 (6)	–
DIFF_SSTL, 1.2V	DIFF_SSTL12	0.6 – 0.125	0.6 + 0.125	0 (6)	–
DIFF_SSTL135/DIFF_SSTL135_R, 1.35V	DIFF_SSTL135, DIFF_SSTL135_R	0.675 – 0.125	0.675 + 0.125	0 (6)	–
DIFF_SSTL15/DIFF_SSTL15_R, 1.5V	DIFF_SSTL15, DIFF_SSTL15_R	0.75 – 0.125	0.75 + 0.125	0 (6)	–
DIFF_SSTL18_I/DIFF_SSTL18_II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	0.9 – 0.125	0.9 + 0.125	0 (6)	–
LVDS (Low-Voltage Differential Signaling), 1.8V	LVDS	0.9 – 0.125	0.9 + 0.125	0 (6)	–
LVDS_25, 2.5V	LVDS_25	1.2 – 0.125	1.2 + 0.125	0 (6)	–
BLVDS_25, 2.5V	BLVDS_25	1.25 – 0.125	1.25 + 0.125	0 (6)	–
MINI_LVDS_25, 2.5V	MINI_LVDS_25	1.25 – 0.125	1.25 + 0.125	0 (6)	–
PPDS_25	PPDS_25	1.25 – 0.125	1.25 + 0.125	0 (6)	–
RSDS_25	RSDS_25	1.25 – 0.125	1.25 + 0.125	0 (6)	–

Table 58: **Input Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	V_L (1)(2)	V_H (1)(2)	V_{MEAS} (1)(4)(6)	V_{REF} (1)(3)(5)
TMDS_33	TMDS_33	3 – 0.125	3 + 0.125	0(6)	–

Notes:

1. The input delay measurement methodology parameters for LVDCI are the same for LVCMOS standards of the same voltage. Input delay measurement methodology parameters for HSLVDCI are the same as for HSTL_II standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between $V_L$and V_H.
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 18.
6. The value given is the differential input voltage.

Output Delay Measurements

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 18 and Figure 19.

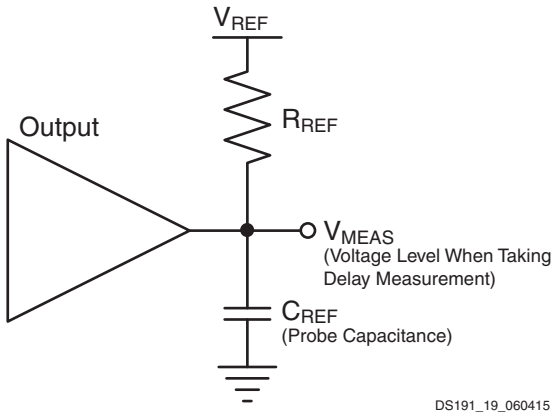

Figure 18: **Single-Ended Test Setup**

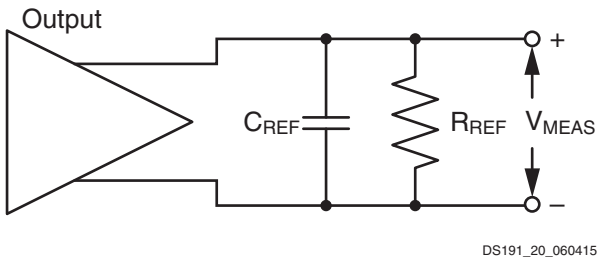

Figure 19: **Differential Test Setup**

Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from Table 59.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.

5. Compare the results of step 2 and step 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 59: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVCMOS, 1.2V	LVCMOS12	1M	0	0.6	0
LVCMOS/LVDCI/HSLVDCI, 1.5V	LVCMOS15, LVDCI_15, HSLVDCI_15	1M	0	0.75	0
LVCMOS/LVDCI/HSLVDCI, 1.8V	LVCMOS18, LVDCI_15, HSLVDCI_18	1M	0	0.9	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 3.3V	LVCMOS33	1M	0	1.65	0
LVTTL, 3.3V	LVTTL	1M	0	1.65	0
PCI33, 3.3V	PCI33_3	25	10	1.65	0
HSTL (High-Speed Transceiver Logic), Class I, 1.2V	HSTL_I_12	50	0	V_{REF}	0.6
HSTL, Class I, 1.5V	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II, 1.5V	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSUL (High-Speed Unterminated Logic), 1.2V	HSUL_12	50	0	V_{REF}	0.6
SSTL12, 1.2V	SSTL12	50	0	V_{REF}	0.6
SSTL135/SSTL135_R, 1.35V	SSTL135, SSTL135_R	50	0	V_{REF}	0.675
SSTL15/SSTL15_R, 1.5V	SSTL15, SSTL15_R	50	0	V_{REF}	0.75
SSTL (Stub Series Terminated Logic), Class I & Class II, 1.8V	SSTL18_I, SSTL18_II	50	0	V_{REF}	0.9
DIFF_MOBILE_DDR, 1.8V	DIFF_MOBILE_DDR	50	0	V_{REF}	0.9
DIFF_HSTL, Class I, 1.2V	DIFF_HSTL_I_12	50	0	V_{REF}	0.6
DIFF_HSTL, Class I & II, 1.5V	DIFF_HSTL_I, DIFF_HSTL_II	50	0	V_{REF}	0.75
DIFF_HSTL, Class I & II, 1.8V	DIFF_HSTL_I_18, DIFF_HSTL_II_18	50	0	V_{REF}	0.9
DIFF_HSUL_12, 1.2V	DIFF_HSUL_12	50	0	V_{REF}	0.6
DIFF_SSTL12, 1.2V	DIFF_SSTL12	50	0	V_{REF}	0.6
DIFF_SSTL135/DIFF_SSTL135_R, 1.35V	DIFF_SSTL135, DIFF_SSTL135_R	50	0	V_{REF}	0.675
DIFF_SSTL15/DIFF_SSTL15_R, 1.5V	DIFF_SSTL15, DIFF_SSTL15_R	50	0	V_{REF}	0.75
DIFF_SSTL18, Class I & II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	50	0	V_{REF}	0.9
LVDS (Low-Voltage Differential Signaling), 1.8V	LVDS	100	0	0[2]	0
LVDS, 2.5V	LVDS_25	100	0	0[2]	0
BLVDS (Bus LVDS), 2.5V	BLVDS_25	100	0	0[2]	0
Mini LVDS, 2.5V	MINI_LVDS_25	100	0	0[2]	0
PPDS_25	PPDS_25	100	0	0[2]	0
RSDS_25	RSDS_25	100	0	0[2]	0
TMDS_33	TMDS_33	50	0	0[2]	3.3

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Input/Output Logic Switching Characteristics

Table 60: **ILOGIC Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3E	-2E/-2I/ -2LI	-1C/-1I	-1Q/ -1LQ	
Setup/Hold						
T_{ICE1CK}/T_{ICKCE1}	CE1 pin setup/hold with respect to CLK	0.42/0.00	0.48/0.00	0.67/0.00	0.67/0.00	ns
T_{ISRCK}/T_{ICKSR}	SR pin setup/hold with respect to CLK	0.53/0.01	0.61/0.01	0.99/0.01	0.99/0.01	ns
$T_{IDOCKE2}/T_{IOCKDE2}$	D pin setup/hold with respect to CLK without delay (HP I/O banks only)	0.01/0.27	0.01/0.29	0.01/0.34	0.01/0.34	ns
$T_{IDOCKDE2}/T_{IOCKDDE2}$	DDLY pin setup/hold with respect to CLK (using IDELAY) (HP I/O banks only)	0.01/0.27	0.02/0.29	0.02/0.34	0.02/0.34	ns
$T_{IDOCKE3}/T_{IOCKDE3}$	D pin setup/hold with respect to CLK without delay (HR I/O banks only)	0.01/0.27	0.01/0.29	0.01/0.34	0.01/0.34	ns
$T_{IDOCKDE3}/T_{IOCKDDE3}$	DDLY pin setup/hold with respect to CLK (using IDELAY) (HR I/O banks only)	0.01/0.27	0.02/0.29	0.02/0.34	0.02/0.34	ns
Combinatorial						
T_{IDIE2}	D pin to O pin propagation delay, no delay (HP I/O banks only)	0.09	0.10	0.12	0.12	ns
T_{IDIDE2}	DDLY pin to O pin propagation delay (using IDELAY) (HP I/O banks only)	0.10	0.11	0.13	0.13	ns
T_{IDIE3}	D pin to O pin propagation delay, no delay (HR I/O banks only)	0.09	0.10	0.12	0.12	ns
T_{IDIDE3}	DDLY pin to O pin propagation delay (using IDELAY) (HR I/O banks only)	0.10	0.11	0.13	0.13	ns
Sequential Delays						
T_{IDLOE2}	D pin to Q1 pin using flip-flop as a latch without delay (HP I/O banks only)	0.36	0.39	0.45	0.45	ns
$T_{IDLODE2}$	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY) (HP I/O banks only)	0.36	0.39	0.45	0.45	ns
T_{IDLOE3}	D pin to Q1 pin using flip-flop as a latch without delay (HR I/O banks only)	0.36	0.39	0.45	0.45	ns
$T_{IDLODE3}$	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY) (HR I/O banks only)	0.36	0.39	0.45	0.45	ns
T_{ICKQ}	CLK to Q outputs	0.47	0.50	0.58	0.58	ns
$T_{RQ\_ILOGICE2}$	SR pin to OQ/TQ out (HP I/O banks only)	0.84	0.94	1.16	1.16	ns
$T_{GSRQ\_ILOGICE2}$	Global set/reset to Q outputs (HP I/O banks only)	7.60	7.60	10.51	10.51	ns
$T_{RQ\_ILOGICE3}$	SR pin to OQ/TQ out (HR I/O banks only)	0.84	0.94	1.16	1.16	ns
$T_{GSRQ\_ILOGICE3}$	Global set/reset to Q outputs (HR I/O banks only)	7.60	7.60	10.51	10.51	ns
Set/Reset						
$T_{RPW\_ILOGICE2}$	Minimum pulse width, SR inputs (HP I/O banks only)	0.54	0.63	0.63	0.63	ns, Min
$T_{RPW\_ILOGICE3}$	Minimum pulse width, SR inputs (HR I/O banks only)	0.54	0.63	0.63	0.63	ns, Min

Table 61: **OLOGIC Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3E	-2E/-2I/ -2LI	-1C/-1I	-1Q/ -1LQ	
Setup/Hold						
T_{ODCK}/T_{OCKD}	D1/D2 pins setup/hold with respect to CLK	0.45/–0.13	0.50/–0.13	0.58/–0.13	0.58/–0.13	ns
T_{OOCECK}/T_{OCKOCE}	OCE pin setup/hold with respect to CLK	0.28/0.03	0.29/0.03	0.45/0.03	0.45/0.03	ns
T_{OSRCK}/T_{OCKSR}	SR pin setup/hold with respect to CLK	0.32/0.18	0.38/0.18	0.70/0.18	0.70/0.18	ns
T_{OTCK}/T_{OCKT}	T1/T2 pins setup/hold with respect to CLK	0.49/–0.16	0.56/–0.16	0.68/–0.16	0.68/–0.13	ns
T_{OTCECK}/T_{OCKTCE}	TCE pin setup/hold with respect to CLK	0.28/0.01	0.30/0.01	0.45/0.01	0.45/0.06	ns
Combinatorial						
T_{ODQ}	D1 to OQ out or T1 to TQ out	0.73	0.81	0.97	0.97	ns
Sequential Delays						
T_{OCKQ}	CLK to OQ/TQ out	0.41	0.43	0.49	0.49	ns
$T_{RQ\_OLOGICE2}$	SR pin to OQ/TQ out (HP I/O banks only)	0.63	0.70	0.83	0.83	ns
$T_{GSRQ\_OLOGICE2}$	Global set/reset to Q outputs (HP I/O banks only)	7.60	7.60	10.51	10.51	ns
$T_{RQ\_OLOGICE3}$	SR pin to OQ/TQ out (HR I/O banks only)	0.63	0.70	0.83	0.83	ns
$T_{GSRQ\_OLOGICE3}$	Global set/reset to Q outputs (HR I/O banks only)	7.60	7.60	10.51	10.51	ns
Set/Reset						
$T_{RPW\_OLOGICE2}$	Minimum pulse width, SR inputs (HP I/O banks only)	0.54	0.54	0.63	0.63	ns, Min
$T_{RPW\_OLOGICE3}$	Minimum pulse width, SR inputs (HR I/O banks only)	0.54	0.54	0.63	0.63	ns, Min

Input Serializer/Deserializer Switching Characteristics

Table 62: **ISERDES Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3E	-2E/-2I/ -2LI	-1C/-1I	-1Q/ -1LQ	
Setup/Hold for Control Lines						
$T_{ISCCK\_BITSLIP}$/ $T_{ISCKC\_BITSLIP}$	BITSLIP pin setup/hold with respect to CLKDIV	0.01/0.12	0.02/0.13	0.02/0.15	0.02/0.15	ns
T_{ISCCK_CE} / T_{ISCKC_CE}(2)	CE pin setup/hold with respect to CLK (for CE1)	0.39/–0.02	0.44/–0.02	0.63/–0.02	0.63/–0.02	ns
T_{ISCCK_CE2} / T_{ISCKC_CE2}(2)	CE pin setup/hold with respect to CLKDIV (for CE2)	–0.12/0.29	–0.12/0.31	–0.12/0.35	–0.12/0.35	ns
Setup/Hold for Data Lines						
T_{ISDCK_D} /T_{ISCKD_D}	D pin setup/hold with respect to CLK	–0.02/0.11	–0.02/0.12	–0.02/0.15	–0.02/0.15	ns
T_{ISDCK_DDLY} /T_{ISCKD_DDLY}	DDLY pin setup/hold with respect to CLK (using IDELAY)(1)	–0.02/0.11	–0.02/0.12	–0.02/0.15	–0.02/0.15	ns
$T_{ISDCK\_D\_DDR}$ /$T_{ISCKD\_D\_DDR}$	D pin setup/hold with respect to CLK at DDR mode	–0.02/0.11	–0.02/0.12	–0.02/0.15	–0.02/0.15	ns
$T_{ISDCK\_DDLY\_DDR}$/ $T_{ISCKD\_DDLY\_DDR}$	D pin setup/hold with respect to CLK at DDR mode (using IDELAY)(1)	0.11/0.11	0.12/0.12	0.15/0.15	0.15/0.15	ns
Sequential Delays						
T_{ISCKO_Q}	CLKDIV to out at Q pin	0.46	0.47	0.58	0.58	ns
Propagation Delays						
T_{ISDO_DO}	D input to DO output pin	0.09	0.10	0.12	0.12	ns

Notes:

1. Recorded at 0 tap value.
2. T_{ISCCK_CE2} and T_{ISCKC_CE2} are reported as T_{ISCCK_CE}/T_{ISCKC_CE} in the timing report.

Output Serializer/Deserializer Switching Characteristics

Table 63: **OSERDES Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3E	-2E/-2I/ -2LI	-1C/-1I	-1Q/ -1LQ	
Setup/Hold						
T_{OSDCK_D}/T_{OSCKD_D}	D input setup/hold with respect to CLKDIV	0.37/0.02	0.40/0.02	0.55/0.02	0.55/0.02	ns
T_{OSDCK_T}/T_{OSCKD_T}(1)	T input setup/hold with respect to CLK	0.49/–0.15	0.56/–0.15	0.68/–0.15	0.68/–0.15	ns
T_{OSDCK_T2}/T_{OSCKD_T2}(1)	T input setup/hold with respect to CLKDIV	0.27/–0.15	0.30/–0.15	0.34/–0.15	0.34/–0.15	ns
T_{OSCCK_OCE}/T_{OSCKC_OCE}	OCE input setup/hold with respect to CLK	0.28/0.03	0.29/0.03	0.45/0.03	0.45/0.03	ns
T_{OSCCK_S}	SR (reset) input setup with respect to CLKDIV	0.41	0.46	0.75	0.75	ns
T_{OSCCK_TCE}/T_{OSCKC_TCE}	TCE input setup/hold with respect to CLK	0.28/0.01	0.30/0.01	0.45/0.01	0.45/0.01	ns
Sequential Delays						
T_{OSCKO_OQ}	Clock to out from CLK to OQ	0.35	0.37	0.42	0.42	ns
T_{OSCKO_TQ}	Clock to out from CLK to TQ	0.41	0.43	0.49	0.49	ns
Combinatorial						
T_{OSDO_TTQ}	T input to TQ out	0.73	0.81	0.97	0.97	ns

Notes:

1. T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in the timing report.

Input/Output Delay Switching Characteristics

Table 64: **Input/Output Delay Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3E	-2E/-2I/ -2LI	-1C/-1I	-1Q/ -1LQ	
IDELAYCTRL						
T_{DLYCCO_RDY}	Reset to ready for IDELAYCTRL	3.22	3.22	3.22	3.22	µs
$F_{IDELAYCTRL\_REF}$	Attribute REFCLK frequency = 200.0(1)	200	200	200	200	MHz
	Attribute REFCLK frequency = 300.0(1)	300	300	N/A	N/A	MHz
	Attribute REFCLK frequency = 400.0(1)	400	400	N/A	N/A	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	±10	MHz
$T_{IDELAYCTRL\_RPW}$	Minimum reset pulse width	52.00	52.00	52.00	52.00	ns
IDELAY/ODELAY						
$T_{IDELAYRESOLUTION}$	IDELAY/ODELAY chain delay resolution	1/(32 x 2 x F_{REF})				ps
$T_{IDELAYPAT\_JIT}$ and $T_{ODELAYPAT\_JIT}$	Pattern dependent period jitter in delay chain for clock pattern.(2)	0	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)(3)	±5	±5	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)(4)	±9	±9	±9	±9	ps per tap
$T_{IDELAY\_CLK\_MAX}$/ $T_{ODELAY\_CLK\_MAX}$	Maximum frequency of CLK input to IDELAY/ODELAY	800	800	710	710	MHz
T_{IDCCK_CE} / T_{IDCKC_CE}	CE pin setup/hold with respect to C for IDELAY	0.11/0.10	0.14/0.12	0.18/0.14	0.18/0.14	ns
T_{ODCCK_CE} / T_{ODCKC_CE}	CE pin setup/hold with respect to C for ODELAY	0.14/0.03	0.16/0.04	0.19/0.05	0.19/0.05	ns
T_{IDCCK_INC}/ T_{IDCKC_INC}	INC pin setup/hold with respect to C for IDELAY	0.10/0.14	0.12/0.16	0.14/0.20	0.14/0.20	ns
T_{ODCCK_INC}/ T_{ODCKC_INC}	INC pin setup/hold with respect to C for ODELAY	0.10/0.07	0.12/0.08	0.13/0.09	0.13/0.09	ns
T_{IDCCK_RST}/ T_{IDCKC_RST}	RST pin setup/hold with respect to C for IDELAY	0.13/0.08	0.14/0.10	0.16/0.12	0.16/0.12	ns
T_{ODCCK_RST}/ T_{ODCKC_RST}	RST pin setup/hold with respect to C for ODELAY	0.16/0.04	0.19/0.06	0.24/0.08	0.24/0.08	ns
$T_{IDDO\_IDATAIN}$	Propagation delay through IDELAY	Note 5	Note 5	Note 5	Note 5	ps
$T_{ODDO\_ODATAIN}$	Propagation delay through ODELAY	Note 5	Note 5	Note 5	Note 5	ps

Notes:

1. Average tap delay at 200 MHz = 78 ps, at 300 MHz = 52 ps, and at 400 MHz = 39 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY/ODELAY tap setting. See the timing report for actual values.

Table 65: **IO_FIFO Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3E	-2E/-2I/-2LI	-1C/-1I	-1Q/-1LQ	
IO_FIFO Clock to Out Delays						
T_{OFFCKO_DO}	RDCLK to Q outputs	0.51	0.56	0.63	0.63	ns
T_{CKO_FLAGS}	Clock to IO_FIFO flags	0.59	0.62	0.81	0.81	ns
Setup/Hold						
T_{CCK_D}/T_{CKC_D}	D inputs to WRCLK	0.43/–0.01	0.47/–0.01	0.53/–0.01	0.53/0.09	ns
$T_{IFFCCK\_WREN}/T_{IFFCKC\_WREN}$	WREN to WRCLK	0.39/–0.01	0.43/–0.01	0.50/–0.01	0.50/–0.01	ns
$T_{OFFCCK\_RDEN}/T_{OFFCKC\_RDEN}$	RDEN to RDCLK	0.49/0.01	0.53/0.02	0.61/0.02	0.61/0.02	ns
Minimum Pulse Width						
$T_{PWH\_IO\_FIFO}$	RESET, RDCLK, WRCLK	0.81	0.92	1.08	1.08	ns
$T_{PWL\_IO\_FIFO}$	RESET, RDCLK, WRCLK	0.81	0.92	1.08	1.08	ns
Maximum Frequency						
F_{MAX}	RDCLK and WRCLK	533.05	470.37	400.00	400.00	MHz

CLB Switching Characteristics

Table 66: **CLB Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3E	-2E/-2I/-2LI	-1C/-1I	-1Q/-1LQ	
Combinatorial Delays						
T_{ILO}	An – Dn LUT address to A	0.05	0.05	0.06	0.06	ns, Max
T_{ILO_2}	An – Dn LUT address to AMUX/CMUX	0.15	0.16	0.19	0.19	ns, Max
T_{ILO_3}	An – Dn LUT address to BMUX_A	0.24	0.25	0.30	0.30	ns, Max
T_{ITO}	An – Dn inputs to A – D Q outputs	0.58	0.61	0.74	0.74	ns, Max
T_{AXA}	AX inputs to AMUX output	0.38	0.40	0.49	0.49	ns, Max
T_{AXB}	AX inputs to BMUX output	0.40	0.42	0.52	0.52	ns, Max
T_{AXC}	AX inputs to CMUX output	0.39	0.41	0.50	0.50	ns, Max
T_{AXD}	AX inputs to DMUX output	0.43	0.44	0.52	0.52	ns, Max
T_{BXB}	BX inputs to BMUX output	0.31	0.33	0.40	0.40	ns, Max
T_{BXD}	BX inputs to DMUX output	0.38	0.39	0.47	0.47	ns, Max
T_{CXC}	CX inputs to CMUX output	0.27	0.28	0.34	0.34	ns, Max
T_{CXD}	CX inputs to DMUX output	0.33	0.34	0.41	0.41	ns, Max
T_{DXD}	DX inputs to DMUX output	0.32	0.33	0.40	0.40	ns, Max
Sequential Delays						
T_{CKO}	Clock to AQ – DQ outputs	0.26	0.27	0.32	0.32	ns, Max
T_{SHCKO}	Clock to AMUX – DMUX outputs	0.32	0.32	0.39	0.39	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK						
T_{AS}/T_{AH}	A_N – D_N input to CLK on A – D flip-flops	0.01/0.12	0.02/0.13	0.03/0.18	0.03/0.24	ns, Min
T_{DICK}/T_{CKDI}	A_X – D_X input to CLK on A – D flip-flops	0.04/0.14	0.04/0.14	0.05/0.20	0.05/0.26	ns, Min
	A_X – D_X input through MUXs and/or carry logic to CLK on A – D flip-flops	0.36/0.10	0.37/0.11	0.46/0.16	0.46/0.22	ns, Min
$T_{CECK\_CLB}/T_{CKCE\_CLB}$	CE input to CLK on A – D flip-flops	0.19/0.05	0.20/0.05	0.25/0.05	0.25/0.11	ns, Min
T_{SRCK}/T_{CKSR}	SR input to CLK on A – D flip-flops	0.30/0.05	0.31/0.07	0.37/0.09	0.37/0.22	ns, Min
Set/Reset						
T_{SRMIN}	SR input minimum pulse width	0.52	0.78	1.04	1.04	ns, Min
T_{RQ}	Delay from SR input to AQ – DQ flip-flops	0.38	0.38	0.46	0.46	ns, Max
T_{CEO}	Delay from CE input to AQ – DQ flip-flops	0.34	0.35	0.43	0.43	ns, Max
F_{TOG}	Toggle frequency (for export control)	1818	1818	1818	1818	MHz

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 67: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3E	-2E/-2I/-2LI	-1C/-1I	-1Q/-1LQ	
Sequential Delays						
T_{SHCKO}(1)	Clock to A – B outputs	0.68	0.70	0.85	0.85	ns, Max
T_{SHCKO_1}	Clock to AMUX – BMUX outputs	0.91	0.95	1.15	1.15	ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{DS_LRAM}/T_{DH_LRAM}	A – D inputs to CLK	0.45/0.23	0.45/0.24	0.54/0.27	0.54/0.28	ns, Min
T_{AS_LRAM}/T_{AH_LRAM}	Address An inputs to clock	0.13/0.50	0.14/0.50	0.17/0.58	0.17/0.61	ns, Min
	Address An inputs through MUXs and/or carry logic to clock	0.40/0.16	0.42/0.17	0.52/0.23	0.52/0.29	ns, Min
T_{WS_LRAM}/T_{WH_LRAM}	WE input to clock	0.29/0.09	0.30/0.09	0.36/0.09	0.36/0.11	ns, Min
$T_{CECK\_LRAM}/T_{CKCE\_LRAM}$	CE input to CLK	0.29/0.09	0.30/0.09	0.37/0.09	0.37/0.11	ns, Min
Clock CLK						
T_{MPW_LRAM}	Minimum pulse width	0.68	0.77	0.91	0.91	ns, Min
T_{MCP}	Minimum clock period	1.35	1.54	1.82	1.82	ns, Min

Notes:

1. T_{SHCKO} also represents the CLK to XMUX output. Refer to the timing report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 68: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3E	-2E/-2I/-2LI	-1C/-1I	-1Q/-1LQ	
Sequential Delays						
T_{REG}	Clock to A – D outputs	0.96	0.98	1.20	1.20	ns, Max
T_{REG_MUX}	Clock to AMUX – DMUX output	1.19	1.23	1.50	1.50	ns, Max
T_{REG_M31}	Clock to DMUX output via M31 output	0.89	0.91	1.10	1.10	ns, Max
Setup and Hold Times Before/After Clock CLK						
$T_{WS\_SHFREG}/T_{WH\_SHFREG}$	WE input	0.26/0.09	0.27/0.09	0.33/0.09	0.33/0.11	ns, Min
$T_{CECK\_SHFREG}/T_{CKCE\_SHFREG}$	CE input to CLK	0.27/0.09	0.28/0.09	0.33/0.09	0.33/0.11	ns, Min
$T_{DS\_SHFREG}/T_{DH\_SHFREG}$	A – D inputs to CLK	0.28/0.26	0.28/0.26	0.33/0.30	0.33/0.36	ns, Min
Clock CLK						
T_{MPW_SHFREG}	Minimum pulse width	0.55	0.65	0.78	0.78	ns, Min

Block RAM and FIFO Switching Characteristics

Table 69: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3E	-2E/-2I/-2LI	-1C/-1I	-1Q/-1LQ	
Block RAM and FIFO Clock-to-Out Delays						
T_{RCKO_DO} and $T_{RCKO\_DO\_REG}$[1]	Clock CLK to DOUT output (without output register)[2][3]	1.57	1.80	2.08	2.08	ns, Max
	Clock CLK to DOUT output (with output register)[4][5]	0.54	0.63	0.75	0.75	ns, Max
$T_{RCKO\_DO\_ECC}$ and $T_{RCKO\_DO\_ECC\_REG}$	Clock CLK to DOUT output with ECC (without output register)[2][3]	2.35	2.58	3.26	3.26	ns, Max
	Clock CLK to DOUT output with ECC (with output register)[4][5]	0.62	0.69	0.80	0.80	ns, Max
$T_{RCKO\_DO\_CASCOUT}$ and $T_{RCKO\_DO\_CASCOUT\_REG}$	Clock CLK to DOUT output with Cascade (without output register)[2]	2.21	2.45	2.80	2.80	ns, Max
	Clock CLK to DOUT output with Cascade (with output register)[4]	0.98	1.08	1.24	1.24	ns, Max
T_{RCKO_FLAGS}	Clock CLK to FIFO flags outputs[6]	0.65	0.74	0.89	0.89	ns, Max
$T_{RCKO\_POINTERS}$	Clock CLK to FIFO pointers outputs[7]	0.79	0.87	0.98	0.98	ns, Max
$T_{RCKO\_PARITY\_ECC}$	Clock CLK to ECCPARITY in ECC encode only mode	0.66	0.72	0.80	0.80	ns, Max
$T_{RCKO\_SDBIT\_ECC}$ and $T_{RCKO\_SDBIT\_ECC\_REG}$	Clock CLK to BITERR (without output register)	2.17	2.38	3.01	3.01	ns, Max
	Clock CLK to BITERR (with output register)	0.57	0.65	0.76	0.76	ns, Max
$T_{RCKO\_RDADDR\_ECC}$ and $T_{RCKO\_RDADDR\_ECC\_REG}$	Clock CLK to RDADDR output with ECC (without output register)	0.64	0.74	0.90	0.90	ns, Max
	Clock CLK to RDADDR output with ECC (with output register)	0.71	0.79	0.92	0.92	ns, Max
Setup and Hold Times Before/After Clock CLK						
$T_{RCCK\_ADDRA}/T_{RCKC\_ADDRA}$	ADDR inputs[8]	0.38/0.27	0.42/0.28	0.48/0.31	0.48/0.38	ns, Min
$T_{RDCK\_DI\_WF\_NC}/T_{RCKD\_DI\_WF\_NC}$	Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode[9]	0.49/0.51	0.55/0.53	0.63/0.57	0.63/0.57	ns, Min
$T_{RDCK\_DI\_RF}/T_{RCKD\_DI\_RF}$	Data input setup/hold time when block RAM is configured in READ_FIRST mode[9]	0.17/0.25	0.19/0.29	0.21/0.35	0.21/0.35	ns, Min
$T_{RDCK\_DI\_ECC}/T_{RCKD\_DI\_ECC}$	DIN inputs with block RAM ECC in standard mode[9]	0.42/0.37	0.47/0.39	0.53/0.43	0.53/0.58	ns, Min
$T_{RDCK\_DI\_ECCW}/T_{RCKD\_DI\_ECCW}$	DIN inputs with block RAM ECC encode only[9]	0.79/0.37	0.87/0.39	0.99/0.43	0.99/0.58	ns, Min
$T_{RDCK\_DI\_ECC\_FIFO}/T_{RCKD\_DI\_ECC\_FIFO}$	DIN inputs with FIFO ECC in standard mode[9]	0.89/0.47	0.98/0.50	1.12/0.54	1.12/0.69	ns, Min
$T_{RCCK\_INJECTBITERR}/T_{RCKC\_INJECTBITERR}$	Inject single/double bit error in ECC mode	0.49/0.30	0.55/0.31	0.63/0.34	0.63/0.43	ns, Min
T_{RCCK_EN}/T_{RCKC_EN}	Block RAM Enable (EN) input	0.30/0.17	0.33/0.18	0.38/0.20	0.38/0.32	ns, Min
$T_{RCCK\_REGCE}/T_{RCKC\_REGCE}$	CE input of output register	0.21/0.13	0.25/0.13	0.31/0.14	0.31/0.19	ns, Min
$T_{RCCK\_RSTREG}/T_{RCKC\_RSTREG}$	Synchronous RSTREG input	0.25/0.06	0.27/0.06	0.29/0.06	0.29/0.14	ns, Min
$T_{RCCK\_RSTRAM}/T_{RCKC\_RSTRAM}$	Synchronous RSTRAM input	0.27/0.35	0.29/0.37	0.31/0.39	0.31/0.39	ns, Min
$T_{RCCK\_WEA}/T_{RCKC\_WEA}$	Write Enable (WE) input (Block RAM only)	0.38/0.15	0.41/0.16	0.46/0.17	0.46/0.29	ns, Min

Table 69: **Block RAM and FIFO Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3E	-2E/-2I/-2LI	-1C/-1I	-1Q/-1LQ	
$T_{RCCK\_WREN}/T_{RCKC\_WREN}$	WREN FIFO inputs	0.39/0.25	0.39/0.30	0.40/0.37	0.40/0.49	ns, Min
$T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$	RDEN FIFO inputs	0.36/0.26	0.36/0.30	0.37/0.37	0.37/0.49	ns, Min
Reset Delays						
T_{RCO_FLAGS}	Reset RST to FIFO flags/pointers(10)	0.76	0.83	0.93	0.93	ns, Max
$T_{RREC\_RST}/T_{RREM\_RST}$	FIFO reset recovery and removal timing(11)	1.59/–0.68	1.76/–0.68	2.01/–0.68	2.01/–0.68	ns, Max
Maximum Frequency						
$F_{MAX\_BRAM\_WF\_NC}$	Block RAM (Write first and No change modes) When not in SDP RF mode	601.32	543.77	458.09	458.09	MHz
$F_{MAX\_BRAM\_RF\_PERFORMANCE}$	Block RAM (Read first, Performance mode) When in SDP RF mode but no address overlap between port A and port B	601.32	543.77	458.09	458.09	MHz
$F_{MAX\_BRAM\_RF\_DELAYED\_WRITE}$	Block RAM (Read first, Delayed_write mode) When in SDP RF mode and there is possibility of overlap between port A and port B addresses	528.26	477.33	400.80	400.80	MHz
$F_{MAX\_CAS\_WF\_NC}$	Block RAM Cascade (Write first, No change mode) When cascade but not in RF mode	551.27	493.93	408.00	408.00	MHz
$F_{MAX\_CAS\_RF\_PERFORMANCE}$	Block RAM Cascade (Read first, Performance mode) When in cascade with RF mode and no possibility of address overlap/one port is disabled	551.27	493.93	408.00	408.00	MHz
$F_{MAX\_CAS\_RF\_DELAYED\_WRITE}$	When in cascade RF mode and there is a possibility of address overlap between port A and port B	478.24	427.35	350.88	350.88	MHz
F_{MAX_FIFO}	FIFO in all modes without ECC	601.32	543.77	458.09	458.09	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration	484.26	430.85	351.12	351.12	MHz

Notes:

1. The timing report shows all of these parameters as T_{RCKO_DO}.
2. T_{RCKO_DOR} includes T_{RCKO_DOW}, T_{RCKO_DOPR}, and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with DO_REG = 0.
4. T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
6. T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY}, T_{RCKO_AFULL}, T_{RCKO_EMPTY}, T_{RCKO_FULL}, T_{RCKO_RDERR}, T_{RCKO_WRERR}.
7. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. These parameters include both A and B inputs as well as the parity inputs of A and B.
10. T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

DSP48E1 Switching Characteristics

Table 70: **DSP48E1 Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3E	-2E/-2I/-2LI	-1C/-1I	-1Q/-1LQ	
Setup and Hold Times of Data/Control Pins to the Input Register Clock						
$T_{DSPDCK\_A\_AREG}$/ $T_{DSPCKD\_A\_AREG}$	A input to A register CLK	0.24/0.12	0.27/0.14	0.31/0.16	0.33/0.18	ns
$T_{DSPDCK\_B\_BREG}$/$T_{DSPCKD\_B\_BREG}$	B input to B register CLK	0.28/0.13	0.32/0.14	0.39/0.15	0.41/0.18	ns
$T_{DSPDCK\_C\_CREG}$/$T_{DSPCKD\_C\_CREG}$	C input to C register CLK	0.15/0.15	0.17/0.17	0.20/0.20	0.20/0.22	ns
$T_{DSPDCK\_D\_DREG}$/$T_{DSPCKD\_D\_DREG}$	D input to D register CLK	0.21/0.19	0.27/0.22	0.35/0.26	0.35/0.27	ns
$T_{DSPDCK\_ACIN\_AREG}$/$T_{DSPCKD\_ACIN\_AREG}$	ACIN input to A register CLK	0.21/0.12	0.24/0.14	0.27/0.16	0.30/0.16	ns
$T_{DSPDCK\_BCIN\_BREG}$/$T_{DSPCKD\_BCIN\_BREG}$	BCIN input to B register CLK	0.22/0.13	0.25/0.14	0.30/0.15	0.32/0.15	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock						
$T_{DSPDCK\_\{A, B\}\_MREG\_MULT}$/ $T_{DSPCKD\_\{A, B\}\_MREG\_MULT}$	{A, B} input to M register CLK using multiplier	2.04/–0.01	2.34/–0.01	2.79/–0.01	2.79/–0.01	ns
$T_{DSPDCK\_\{A, D\}\_ADREG}$/ $T_{DSPCKD\_\{A, D\}\_ADREG}$	{A, D} input to AD register CLK	1.09/–0.02	1.25/–0.02	1.49/–0.02	1.49/–0.02	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock						
$T_{DSPDCK\_\{A, B\}\_PREG\_MULT}$/ $T_{DSPCKD\_\{A, B\}\_PREG\_MULT}$	{A, B} input to P register CLK using multiplier	3.41/–0.24	3.90/–0.24	4.64/–0.24	4.64/–0.24	ns
$T_{DSPDCK\_D\_PREG\_MULT}$/ $T_{DSPCKD\_D\_PREG\_MULT}$	D input to P register CLK using multiplier	3.33/–0.62	3.81/–0.62	4.53/–0.62	4.53/–0.62	ns
$T_{DSPDCK\_\{A, B\}\_PREG}$/ $T_{DSPCKD\_\{A, B\}\_PREG}$	A or B input to P register CLK not using multiplier	1.47/–0.24	1.68/–0.24	2.00/–0.24	2.00/–0.24	ns
$T_{DSPDCK\_C\_PREG}$/ $T_{DSPCKD\_C\_PREG}$	C input to P register CLK not using multiplier	1.30/–0.22	1.49/–0.22	1.78/–0.22	1.78/–0.22	ns
$T_{DSPDCK\_PCIN\_PREG}$/ $T_{DSPCKD\_PCIN\_PREG}$	PCIN input to P register CLK	1.12/–0.13	1.28/–0.13	1.52/–0.13	1.52/–0.13	ns
Setup and Hold Times of the CE Pins						
$T_{DSPDCK\_\{CEA, CEB\}\_\{AREG, BREG\}}$/ $T_{DSPCKD\_\{CEA, CEB\}\_\{AREG, BREG\}}$	{CEA; CEB} input to {A; B} register CLK	0.30/0.05	0.36/0.06	0.44/0.09	0.44/0.09	ns
$T_{DSPDCK\_CEC\_CREG}$/ $T_{DSPCKD\_CEC\_CREG}$	CEC input to C register CLK	0.24/0.08	0.29/0.09	0.36/0.11	0.36/0.11	ns
$T_{DSPDCK\_CED\_DREG}$/ $T_{DSPCKD\_CED\_DREG}$	CED input to D register CLK	0.31/–0.02	0.36/–0.02	0.44/–0.02	0.44/0.02	ns
$T_{DSPDCK\_CEM\_MREG}$/ $T_{DSPCKD\_CEM\_MREG}$	CEM input to M register CLK	0.26/0.15	0.29/0.17	0.33/0.20	0.33/0.20	ns
$T_{DSPDCK\_CEP\_PREG}$/ $T_{DSPCKD\_CEP\_PREG}$	CEP input to P register CLK	0.31/0.01	0.36/0.01	0.45/0.01	0.45/0.01	ns
Setup and Hold Times of the RST Pins						
$T_{DSPDCK\_\{RSTA, RSTB\}\_\{AREG, BREG\}}$/ $T_{DSPCKD\_\{RSTA, RSTB\}\_\{AREG, BREG\}}$	{RSTA, RSTB} input to {A, B} register CLK	0.34/0.10	0.39/0.11	0.47/0.13	0.47/0.14	ns
$T_{DSPDCK\_RSTC\_CREG}$/ $T_{DSPCKD\_RSTC\_CREG}$	RSTC input to C register CLK	0.06/0.22	0.07/0.24	0.08/0.26	0.08/0.26	ns
$T_{DSPDCK\_RSTD\_DREG}$/ $T_{DSPCKD\_RSTD\_DREG}$	RSTD input to D register CLK	0.37/0.06	0.42/0.06	0.50/0.07	0.50/0.07	ns
$T_{DSPDCK\_RSTM\_MREG}$/ $T_{DSPCKD\_RSTM\_MREG}$	RSTM input to M register CLK	0.18/0.18	0.20/0.21	0.23/0.24	0.23/0.24	ns
$T_{DSPDCK\_RSTP\_PREG}$/ $T_{DSPCKD\_RSTP\_PREG}$	RSTP input to P register CLK	0.24/0.01	0.26/0.01	0.30/0.01	0.30/0.11	ns
Combinatorial Delays from Input Pins to Output Pins						
$T_{DSPDO\_A\_CARRYOUT\_MULT}$	A input to CARRYOUT output using multiplier	3.21	3.69	4.39	4.39	ns
$T_{DSPDO\_D\_P\_MULT}$	D input to P output using multiplier	3.15	3.61	4.30	4.30	ns

Table 70: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3E	-2E/-2I/-2LI	-1C/-1I	-1Q/-1LQ	
$T_{DSPDO\_A\_P}$	A input to P output not using multiplier	1.30	1.48	1.76	1.76	ns
$T_{DSPDO\_C\_P}$	C input to P output	1.13	1.30	1.55	1.55	ns
Combinatorial Delays from Input Pins to Cascading Output Pins						
$T_{DSPDO\_\{A; B\}\_\{ACOUT; BCOUT\}}$	{A, B} input to {ACOUT, BCOUT} output	0.47	0.53	0.63	0.63	ns
$T_{DSPDO\_\{A, B\}\_CARRYCASCOUT\_MULT}$	{A, B} input to CARRYCASCOUT output using multiplier	3.44	3.94	4.69	4.69	ns
$T_{DSPDO\_D\_CARRYCASCOUT\_MULT}$	D input to CARRYCASCOUT output using multiplier	3.36	3.85	4.58	4.58	ns
$T_{DSPDO\_\{A, B\}\_CARRYCASCOUT}$	{A, B} input to CARRYCASCOUT output not using multiplier	1.50	1.72	2.04	2.04	ns
$T_{DSPDO\_C\_CARRYCASCOUT}$	C input to CARRYCASCOUT output	1.34	1.53	1.83	1.83	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins						
$T_{DSPDO\_ACIN\_P\_MULT}$	ACIN input to P output using multiplier	3.09	3.55	4.24	4.24	ns
$T_{DSPDO\_ACIN\_P}$	ACIN input to P output not using multiplier	1.16	1.33	1.59	1.59	ns
$T_{DSPDO\_ACIN\_ACOUT}$	ACIN input to ACOUT output	0.32	0.37	0.45	0.45	ns
$T_{DSPDO\_ACIN\_CARRYCASCOUT\_MULT}$	ACIN input to CARRYCASCOUT output using multiplier	3.30	3.79	4.52	4.52	ns
$T_{DSPDO\_ACIN\_CARRYCASCOUT}$	ACIN input to CARRYCASCOUT output not using multiplier	1.37	1.57	1.87	1.87	ns
$T_{DSPDO\_PCIN\_P}$	PCIN input to P output	0.94	1.08	1.29	1.29	ns
$T_{DSPDO\_PCIN\_CARRYCASCOUT}$	PCIN input to CARRYCASCOUT output	1.15	1.32	1.57	1.57	ns
Clock to Outs from Output Register Clock to Output Pins						
$T_{DSPCKO\_P\_PREG}$	CLK PREG to P output	0.33	0.35	0.39	0.39	ns
$T_{DSPCKO\_CARRYCASCOUT\_PREG}$	CLK PREG to CARRYCASCOUT output	0.44	0.50	0.59	0.59	ns
Clock to Outs from Pipeline Register Clock to Output Pins						
$T_{DSPCKO\_P\_MREG}$	CLK MREG to P output	1.42	1.64	1.96	1.96	ns
$T_{DSPCKO\_CARRYCASCOUT\_MREG}$	CLK MREG to CARRYCASCOUT output	1.63	1.87	2.24	2.24	ns
$T_{DSPCKO\_P\_ADREG\_MULT}$	CLK ADREG to P output using multiplier	2.30	2.63	3.13	3.13	ns
$T_{DSPCKO\_CARRYCASCOUT\_ADREG\_MULT}$	CLK ADREG to CARRYCASCOUT output using multiplier	2.51	2.87	3.41	3.41	ns

Table 70: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3E	-2E/-2I/-2LI	-1C/-1I	-1Q/-1LQ	
Clock to Outs from Input Register Clock to Output Pins						
$T_{DSPCKO\_P\_AREG\_MULT}$	CLK AREG to P output using multiplier	3.34	3.83	4.55	4.55	ns
$T_{DSPCKO\_P\_BREG}$	CLK BREG to P output not using multiplier	1.39	1.59	1.88	1.88	ns
$T_{DSPCKO\_P\_CREG}$	CLK CREG to P output not using multiplier	1.43	1.64	1.95	1.95	ns
$T_{DSPCKO\_P\_DREG\_MULT}$	CLK DREG to P output using multiplier	3.32	3.80	4.51	4.51	ns
Clock to Outs from Input Register Clock to Cascading Output Pins						
$T_{DSPCKO\_\{ACOUT;\ BCOUT\}\_\{AREG;\ BREG\}}$	CLK (ACOUT, BCOUT) to {A,B} register output	0.55	0.62	0.74	0.74	ns
$T_{DSPCKO\_CARRYCASCOUT\_\{AREG,\ BREG\}\_MULT}$	CLK (AREG, BREG) to CARRYCASCOUT output using multiplier	3.55	4.06	4.84	4.84	ns
$T_{DSPCKO\_CARRYCASCOUT\_BREG}$	CLK BREG to CARRYCASCOUT output not using multiplier	1.60	1.82	2.16	2.16	ns
$T_{DSPCKO\_CARRYCASCOUT\_DREG\_MULT}$	CLK DREG to CARRYCASCOUT output using multiplier	3.52	4.03	4.79	4.79	ns
$T_{DSPCKO\_CARRYCASCOUT\_CREG}$	CLK CREG to CARRYCASCOUT output	1.64	1.88	2.23	2.23	ns
Maximum Frequency						
F_{MAX}	With all registers used	741.84	650.20	547.95	547.95	MHz
F_{MAX_PATDET}	With pattern detector	627.35	549.75	463.61	463.61	MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG	412.20	360.75	303.77	303.77	MHz
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect	374.25	327.65	276.01	276.01	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG}$	Without ADREG	468.82	408.66	342.70	342.70	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$	Without ADREG with pattern detect	468.82	408.66	342.70	342.70	MHz
$F_{MAX\_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG)	306.84	267.81	225.02	225.02	MHz
$F_{MAX\_NOPIPELINEREG\_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect	285.23	249.13	209.38	209.38	MHz

Clock Buffers and Networks

Table 71: **Global Clock Switching Characteristics (Including BUFGCTRL)**

Symbol	Description	Speed Grade				Units
		-3E	-2E/-2I/-2LI	-1C/-1I	-1Q/-1LQ	
$T_{BCCCK\_CE}/T_{BCCKC\_CE}$(1)	CE pins setup/hold	0.12/0.30	0.14/0.38	0.26/0.38	0.26/0.92	ns
T_{BCCCK_S}/T_{BCCKC_S}(1)	S pins setup/hold	0.12/0.30	0.14/0.38	0.26/0.38	0.26/0.92	ns
T_{BCCKO_O}(2)	BUFGCTRL delay from I0/I1 to O	0.08	0.10	0.12	0.12	ns
Maximum Frequency						
F_{MAX_BUFG}	Global clock tree (BUFG)	741.00	710.00	625.00	625.00	MHz

Notes:

1. T_{BCCCK_CE} and T_{BCCKC_CE} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BGCKO_O} (BUFG delay from I0 to O) values are the same as T_{BCCKO_O} values.

Table 72: **Input/Output Clock Switching Characteristics (BUFIO)**

Symbol	Description	Speed Grade				Units
		-3E	-2E/-2I/-2LI	-1C/-1I	-1Q/-1LQ	
T_{BIOCKO_O}	Clock to out delay from I to O	1.04	1.14	1.32	1.32	ns
Maximum Frequency						
F_{MAX_BUFIO}	I/O clock tree (BUFIO)	800.00	800.00	710.00	710.00	MHz

Table 73: **Regional Clock Buffer Switching Characteristics (BUFR)**

Symbol	Description	Speed Grade				Units
		-3E	-2E/-2I/-2LI	-1C/-1I	-1Q/-1LQ	
T_{BRCKO_O}	Clock to out delay from I to O	0.60	0.65	0.77	0.77	ns
$T_{BRCKO\_O\_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	0.30	0.32	0.38	0.38	ns
T_{BRDO_O}	Propagation delay from CLR to O	0.71	0.75	0.96	0.96	ns
Maximum Frequency						
F_{MAX_BUFR}(1)	Regional clock tree (BUFR)	600.00	540.00	450.00	450.00	MHz

Notes:

1. The maximum input frequency to the BUFR and BUFMR is the BUFIO F_{MAX} frequency.

Table 74: **Horizontal Clock Buffer Switching Characteristics (BUFH)**

Symbol	Description	Speed Grade				Units
		-3E	-2E/-2I-2LI	-1C/-1I	-1Q/-1LQ	
T_{BHCKO_O}	BUFH delay from I to O	0.10	0.11	0.13	0.13	ns
$T_{BHCCK\_CE}/T_{BHCKC\_CE}$	CE pin setup and hold	0.20/0.16	0.23/0.20	0.38/0.21	0.38/0.79	ns
Maximum Frequency						
F_{MAX_BUFH}	Horizontal clock buffer (BUFH)	741.00	710.00	625.00	625.00	MHz

Table 75: **Duty-Cycle Distortion and Clock-Tree Skew**

Symbol	Description	Device	Speed Grade								Units
			-3E	-2E	-2I	-2LI	-1C	-1I	-1Q	-1LQ	
T_{DCD_CLK}	Global clock tree duty-cycle distortion(1)	All	0.20	0.20	0.20	0.20	0.20	0.20	0.20	0.20	ns
T_{CKSKEW}	Global clock tree skew(2)	XC7Z030	0.29	0.36	0.36	0.36	0.37	0.37	N/A	N/A	ns
		XC7Z035	0.43	0.54	0.54	0.54	0.57	0.57	N/A	N/A	ns
		XC7Z045	0.43	0.54	0.54	0.54	0.57	0.57	N/A	N/A	ns
		XC7Z100	N/A	N/A	0.54	0.54	N/A	0.56	N/A	N/A	ns
		XA7Z030	N/A	N/A	N/A	N/A	N/A	0.37	0.37	N/A	ns
		XQ7Z030	N/A	N/A	0.36	0.36	N/A	0.37	0.37	N/A	ns
		XQ7Z045	N/A	N/A	0.54	0.54	N/A	0.57	0.57	0.57	ns
		XQ7Z100	N/A	N/A	0.54	0.54	N/A	0.56	N/A	N/A	ns
T_{DCD_BUFIO}	I/O clock tree duty-cycle distortion	All	0.12	0.12	0.12	0.12	0.12	0.12	0.12	0.12	ns
$T_{BUFIOSKEW}$	I/O clock tree skew across one clock region	All	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02	ns
T_{DCD_BUFR}	Regional clock tree duty-cycle distortion	All	0.15	0.15	0.15	0.15	0.15	0.15	0.15	0.15	ns

Notes:

1. These parameters represent the worst-case duty-cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty-cycle distortion that might be caused by asymmetrical rise/fall times.
2. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx Timing Analyzer tools to evaluate application specific clock skew.

MMCM Switching Characteristics

Table 76: **MMCM Specification**

Symbol	Description	Speed Grade				Units
		-3E	-2E/-2I/-2LI	-1C/-1I	-1Q/-1LQ	
$MMCM\_F_{INMAX}$	Maximum input clock frequency	1066.00	933.00	800.00	800.00	MHz
$MMCM\_F_{INMIN}$	Minimum input clock frequency	10.00	10.00	10.00	10.00	MHz
$MMCM\_F_{INJITTER}$	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max				
$MMCM\_F_{INDUTY}$	Allowable input duty cycle: 10—49 MHz	25.00	25.00	25.00	25.00	%
	Allowable input duty cycle: 50—199 MHz	30.00	30.00	30.00	30.00	%
	Allowable input duty cycle: 200—399 MHz	35.00	35.00	35.00	35.00	%
	Allowable input duty cycle: 400—499 MHz	40.00	40.00	40.00	40.00	%
	Allowable input duty cycle: >500 MHz	45.00	45.00	45.00	45.00	%
$MMCM\_F_{MIN\_PSCLK}$	Minimum dynamic phase-shift clock frequency	0.01	0.01	0.01	0.01	MHz
$MMCM\_F_{MAX\_PSCLK}$	Maximum dynamic phase-shift clock frequency	550.00	500.00	450.00	450.00	MHz
$MMCM\_F_{VCOMIN}$	Minimum MMCM VCO frequency	600.00	600.00	600.00	600.00	MHz
$MMCM\_F_{VCOMAX}$	Maximum MMCM VCO frequency	1600.00	1440.00	1200.00	1200.00	MHz
$MMCM\_F_{BANDWIDTH}$	Low MMCM bandwidth at typical(1)	1.00	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical(1)	4.00	4.00	4.00	4.00	MHz
$MMCM\_T_{STATPHAOFFSET}$	Static phase offset of the MMCM outputs(2)	0.12	0.12	0.12	0.12	ns

Table 76: **MMCM Specification *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3E	-2E/-2I/-2LI	-1C/-1I	-1Q/-1LQ	
$MMCM\_T_{OUTJITTER}$	MMCM output jitter	Note 3				
$MMCM\_T_{OUTDUTY}$	MMCM output clock duty-cycle precision(4)	0.20	0.20	0.20	0.20	ns
$MMCM\_T_{LOCKMAX}$	MMCM maximum lock time	100.00	100.00	100.00	100.00	µs
$MMCM\_F_{OUTMAX}$	MMCM maximum output frequency	1066.00	933.00	800.00	800.00	MHz
$MMCM\_F_{OUTMIN}$	MMCM minimum output frequency(5)(6)	4.69	4.69	4.69	4.69	MHz
$MMCM\_T_{EXTFDVAR}$	External clock feedback variation	< 20% of clock input period or 1 ns Max				
$MMCM\_RST_{MINPULSE}$	Minimum reset pulse width	5.00	5.00	5.00	5.00	ns
$MMCM\_F_{PFDMAX}$	Maximum frequency at the phase frequency detector	550.00	500.00	450.00	450.00	MHz
$MMCM\_F_{PFDMIN}$	Minimum frequency at the phase frequency detector	10.00	10.00	10.00	10.00	MHz
$MMCM\_T_{FBDELAY}$	Maximum delay in the feedback path	3 ns Max or one CLKIN cycle				
MMCM Switching Characteristics Setup and Hold						
$T_{MMCMDCK\_PSEN}$/ $T_{MMCMCKD\_PSEN}$	Setup and hold of phase-shift enable	1.04/0.00	1.04/0.00	1.04/0.00	1.04/0.00	ns
$T_{MMCMDCK\_PSINCDEC}$/ $T_{MMCMCKD\_PSINCDEC}$	Setup and hold of phase-shift increment/decrement	1.04/0.00	1.04/0.00	1.04/0.00	1.04/0.00	ns
$T_{MMCMCKO\_PSDONE}$	Phase shift clock-to-out of PSDONE	0.59	0.68	0.81	0.81	ns
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK						
$T_{MMCMDCK\_DADDR}$/ $T_{MMCMCKD\_DADDR}$	DAADR setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
$T_{MMCMDCK\_DI}$/ $T_{MMCMCKD\_DI}$	DI setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
$T_{MMCMDCK\_DEN}$/ $T_{MMCMCKD\_DEN}$	DEN setup/hold	1.76/0.00	1.97/0.00	2.29/0.00	2.29/0.00	ns, Min
$T_{MMCMDCK\_DWE}$/ $T_{MMCMCKD\_DWE}$	DWE setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
$T_{MMCMCKO\_DRDY}$	CLK to out of DRDY	0.65	0.72	0.99	0.99	ns, Max
F_{DCK}	DCLK frequency	200.00	200.00	200.00	200.00	MHz, Max

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard. See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.
6. When CLKOUT4_CASCADE = TRUE, $MMCM\_F_{OUTMIN}$ is 0.036 MHz.

PLL Switching Characteristics

Table 77: **PLL Specification**

Symbol	Description	Speed Grade				Units
		-3E	-2E/-2I/-2LI	-1C/-1I	-1Q/-1LQ	
PLL_F_{INMAX}	Maximum input clock frequency	1066.00	933.00	800.00	800.00	MHz
PLL_F_{INMIN}	Minimum input clock frequency	19.00	19.00	19.00	19.00	MHz
PLL_$F_{INJITTER}$	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max				
PLL_F_{INDUTY}	Allowable input duty cycle: 19—49 MHz	25.00	25.00	25.00	25.00	%
	Allowable input duty cycle: 50—199 MHz	30.00	30.00	30.00	30.00	%
	Allowable input duty cycle: 200—399 MHz	35.00	35.00	35.00	35.00	%
	Allowable input duty cycle: 400—499 MHz	40.00	40.00	40.00	40.00	%
	Allowable input duty cycle: >500 MHz	45.00	45.00	45.00	45.00	%
PLL_F_{VCOMIN}	Minimum PLL VCO frequency	800.00	800.00	800.00	800.00	MHz
PLL_F_{VCOMAX}	Maximum PLL VCO frequency	2133.00	1866.00	1600.00	1600.00	MHz
PLL_$F_{BANDWIDTH}$	Low PLL bandwidth at typical(1)	1.00	1.00	1.00	1.00	MHz
	High PLL bandwidth at typical(1)	4.00	4.00	4.00	4.00	MHz
PLL_$T_{STATPHAOFFSET}$	Static phase offset of the PLL outputs(2)	0.12	0.12	0.12	0.12	ns
PLL_$T_{OUTJITTER}$	PLL output jitter(3)	Note 1				
PLL_$T_{OUTDUTY}$	PLL output clock duty-cycle precision(4)	0.20	0.20	0.20	0.20	ns
PLL_$T_{LOCKMAX}$	PLL maximum lock time	100.00	100.00	100.00	100.00	µs
PLL_F_{OUTMAX}	PLL maximum output frequency	1066.00	933.00	800.00	800.00	MHz
PLL_F_{OUTMIN}	PLL minimum output frequency(5)	6.25	6.25	6.25	6.25	MHz
PLL_$T_{EXTFDVAR}$	External clock feedback variation	< 20% of clock input period or 1 ns Max				
PLL_$RST_{MINPULSE}$	Minimum reset pulse width	5.00	5.00	5.00	5.00	ns
PLL_F_{PFDMAX}	Maximum frequency at the phase frequency detector	550.00	500.00	450.00	450.00	MHz
PLL_F_{PFDMIN}	Minimum frequency at the phase frequency detector	19.00	19.00	19.00	19.00	MHz
PLL_$T_{FBDELAY}$	Maximum delay in the feedback path	3 ns Max or one CLKIN cycle				
Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK						
T_{PLLCCK_DADDR}/ T_{PLLCKC_DADDR}	Setup and hold of D address	1.25/0.15	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T_{PLLCCK_DI}/ T_{PLLCKC_DI}	Setup and hold of D input	1.25/0.15	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T_{PLLCCK_DEN}/ T_{PLLCKC_DEN}	Setup and hold of D enable	1.76/0.00	1.97/0.00	2.29/0.00	2.29/0.00	ns, Min
T_{PLLCCK_DWE}/ T_{PLLCKC_DWE}	Setup and hold of D write enable	1.25/0.15	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T_{PLLCKO_DRDY}	CLK to out of DRDY	0.65	0.72	0.99	0.99	ns, Max
F_{DCK}	DCLK frequency	200.00	200.00	200.00	200.00	MHz, Max

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard. See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.

Device Pin-to-Pin Output Parameter Guidelines

Table 78: **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)**

Symbol	Description	Device	Speed Grade								Units
			-3E	-2E	-2I	-2LI	-1C	-1I	-1Q	-1LQ	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flops, Fast Slew Rate, *without* MMCM/PLL.											
T_{ICKOF}	Clock-capable clock input and OUTFF at pins/banks closest to the BUFGs *without* MMCM/PLL (near clock region)	XC7Z030	5.32	5.85	5.85	5.85	6.55	6.55	N/A	N/A	ns
		XC7Z035	5.27	5.78	5.78	5.78	6.48	6.48	N/A	N/A	ns
		XC7Z045	5.27	5.78	5.78	5.78	6.48	6.48	N/A	N/A	ns
		XC7Z100	N/A	N/A	5.91	5.91	N/A	6.62	N/A	N/A	ns
		XA7Z030	N/A	N/A	N/A	N/A	N/A	6.55	6.55	N/A	ns
		XQ7Z030	N/A	N/A	5.85	5.85	N/A	6.55	6.55	N/A	ns
		XQ7Z045	N/A	N/A	5.78	5.78	N/A	6.48	6.48	6.48	ns
		XQ7Z100	N/A	N/A	5.91	5.91	N/A	6.62	N/A	N/A	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Refer to the Die Level Bank Numbering Overview section of *Zynq-7000 All Programmable SoC Packaging and Pinout Specification* (UG865).

Table 79: **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)**

Symbol	Description	Device	Speed Grade								Units
			-3E	-2E	-2I	-2LI	-1C	-1I	-1Q	-1LQ	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flops, Fast Slew Rate, *without* MMCM/PLL.											
$T_{ICKOFFAR}$	Clock-capable clock input and OUTFF at pins/banks farthest from the BUFGs *without* MMCM/PLL (far clock region)	XC7Z030	5.32	5.85	5.85	5.85	6.55	6.55	N/A	N/A	ns
		XC7Z035	5.88	6.46	6.46	6.46	7.23	7.23	N/A	N/A	ns
		XC7Z045	5.88	6.46	6.46	6.46	7.23	7.23	N/A	N/A	ns
		XC7Z100	N/A	N/A	6.59	6.59	N/A	7.37	N/A	N/A	ns
		XA7Z030	N/A	N/A	N/A	N/A	N/A	6.55	6.55	N/A	ns
		XQ7Z030	N/A	N/A	5.85	5.85	N/A	6.55	6.55	N/A	ns
		XQ7Z045	N/A	N/A	6.46	6.46	N/A	7.23	7.23	7.23	ns
		XQ7Z100	N/A	N/A	6.59	6.59	N/A	7.37	N/A	N/A	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Refer to the Die Level Bank Numbering Overview section of *Zynq-7000 All Programmable SoC Packaging and Pinout Specification* (UG865).

Table 80: **Clock-Capable Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade								Units
			-3E	-2E	-2I	-2LI	-1C	-1I	-1Q	-1LQ	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flops, Fast Slew Rate, *with* MMCM.											
$T_{ICKOFMMCMCC}$	Clock-capable clock input and OUTFF *with* MMCM	XC7Z030	0.92	0.92	0.92	0.92	0.92	0.92	N/A	N/A	ns
		XC7Z035	0.97	0.97	0.97	0.97	0.97	0.97	N/A	N/A	ns
		XC7Z045	0.97	0.97	0.97	0.97	0.97	0.97	N/A	N/A	ns
		XC7Z100	N/A	N/A	0.96	0.96	N/A	0.96	N/A	N/A	ns
		XA7Z030	N/A	N/A	N/A	N/A	N/A	0.92	0.92	N/A	ns
		XQ7Z030	N/A	N/A	0.92	0.92	N/A	0.92	0.92	N/A	ns
		XQ7Z045	N/A	N/A	0.97	0.97	N/A	0.97	0.97	0.97	ns
		XQ7Z100	N/A	N/A	0.96	0.96	N/A	0.96	N/A	N/A	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 81: **Clock-Capable Clock Input to Output Delay With PLL**

Symbol	Description	Device	Speed Grade								Units
			-3E	-2E	-2I	-2LI	-1C	-1I	-1Q	-1LQ	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flops, Fast Slew Rate, *with* PLL.											
$T_{ICKOFPLLCC}$	Clock-capable clock input and OUTFF *with* PLL	XC7Z030	0.81	0.81	0.81	0.81	0.81	0.81	N/A	N/A	ns
		XC7Z035	0.86	0.86	0.86	0.86	0.86	0.86	N/A	N/A	ns
		XC7Z045	0.86	0.86	0.86	0.86	0.86	0.86	N/A	N/A	ns
		XC7Z100	N/A	N/A	0.85	0.85	N/A	0.85	N/A	N/A	ns
		XA7Z030	N/A	N/A	N/A	N/A	N/A	0.81	0.81	N/A	ns
		XQ7Z030	N/A	N/A	0.81	0.81	N/A	0.81	0.81	N/A	ns
		XQ7Z045	N/A	N/A	0.86	0.86	N/A	0.86	0.86	0.86	ns
		XQ7Z100	N/A	N/A	0.85	0.85	N/A	0.85	N/A	N/A	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

Table 82: **Pin-to-Pin, Clock-to-Out using BUFIO**

Symbol	Description	Speed Grade				Units
		-3E	-2E/-2I/-2LI	-1C/-1I	-1Q/-1LQ	
$T_{ICKOFCS}$	Clock-to-out of I/O clock for HR I/O banks	4.93	5.52	6.20	6.20	ns
	Clock-to-out of I/O clock for HP I/O banks	4.85	5.44	6.11	6.11	ns

Device Pin-to-Pin Input Parameter Guidelines

Table 83: **Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks**

Symbol	Description	Device	Speed Grade								Units
			-3E	-2E	-2I	-2LI	-1C	-1I	-1Q	-1LQ	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1)											
T_{PSFD}/ T_{PHFD}	Full delay (legacy delay or default delay) global clock input and IFF(2) without MMCM/PLL with ZHOLD_DELAY on HR I/O banks	XC7Z030	3.04/ –0.34	3.16/ –0.34	3.16/ –0.34	3.16/ –0.34	3.40/ –0.34	3.40/ –0.34	N/A	N/A	ns
		XC7Z035	3.50/ –0.47	3.67/ –0.47	3.67/ –0.47	3.67/ –0.47	3.97/ –0.47	3.97/ –0.47	N/A	N/A	ns
		XC7Z045	3.50/ –0.47	3.67/ –0.47	3.67/ –0.47	3.67/ –0.47	3.97/ –0.47	3.97/ –0.47	N/A	N/A	ns
		XC7Z100	N/A	N/A	3.81/ –0.52	3.81/ –0.52	N/A	4.13/ –0.52	N/A	N/A	ns
		XA7Z030	N/A	N/A	N/A	N/A	N/A	3.40/ –0.34	3.40/ –0.34	N/A	ns
		XQ7Z030	N/A	N/A	3.16/ –0.34	3.16/ –0.34	N/A	3.40/ –0.34	3.40/ –0.34	N/A	ns
		XQ7Z045	N/A	N/A	3.67/ –0.47	3.67/ –0.47	N/A	3.97/ –0.47	3.97/ –0.47	3.97/ –0.47	ns
		XQ7Z100	N/A	N/A	3.81 –0.52	3.81 –0.52	N/A	4.13/ –0.52	N/A	N/A	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch.

Table 84: **Clock-Capable Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	Speed Grade								Units
			-3E	-2E	-2I	-2LI	-1C	-1I	-1Q	-1LQ	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1)											
$T_{PSMMCMCC}$/ $T_{PHMMCMCC}$	No delay clock-capable clock input and IFF(2) with MMCM	XC7Z030	2.41/ –0.23	2.68/ –0.23	2.68/ –0.23	2.68/ –0.23	2.95/ –0.23	2.95/ –0.23	N/A	N/A	ns
		XC7Z035	2.73/ –0.09	3.00/ –0.09	3.00/ –0.09	3.00/ –0.09	3.32/ –0.09	3.32/ –0.09	N/A	N/A	ns
		XC7Z045	2.73/ –0.09	3.00/ –0.09	3.00/ –0.09	3.00/ –0.09	3.32/ –0.09	3.32/ –0.09	N/A	N/A	ns
		XC7Z100	N/A	N/A	3.00/ –0.10	3.00/ –0.09	N/A	3.32/ –0.10	N/A	N/A	ns
		XA7Z030	N/A	N/A	N/A	N/A	N/A	2.95/ –0.23	2.95/ –0.23	N/A	ns
		XQ7Z030	N/A	N/A	2.68/ –0.23	2.68/ –0.23	N/A	2.95/ –0.23	2.95/ –0.23	N/A	ns
		XQ7Z045	N/A	N/A	3.00/ –0.09	3.00/ –0.09	N/A	3.32/ –0.09	3.32/ –0.09	3.32/ –0.09	ns
		XQ7Z100	N/A	N/A	3.00/ –0.10	3.00/ –0.09	N/A	3.32/ –0.10	N/A	N/A	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 85: **Clock-Capable Clock Input Setup and Hold With PLL**

Symbol	Description	Device	Speed Grade								Units
			-3E	-2E	-2I	-2LI	-1C	-1I	-1Q	-1LQ	
Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard.(1)											
$T_{PSPLLCC}$/ $T_{PHPLLCC}$	No delay clock-capable clock input and IFF(2) with PLL	XC7Z030	2.71/ –0.34	3.02/ –0.34	3.02/ –0.34	3.02/ –0.34	3.29/ –0.34	3.29/ –0.34	N/A	N/A	ns
		XC7Z035	2.91/ –0.20	3.24/ –0.20	3.24/ –0.20	3.24/ –0.20	3.53/ –0.20	3.53/ –0.20	N/A	N/A	ns
		XC7Z045	2.91/ –0.20	3.24/ –0.20	3.24/ –0.20	3.24/ –0.20	3.53/ –0.20	3.53/ –0.20	N/A	N/A	ns
		XC7Z100	N/A	N/A	3.24/ –0.21	3.24/ –0.21	N/A	3.53/ –0.21	N/A	N/A	ns
		XA7Z030	N/A	N/A	N/A	N/A	N/A	3.29/ –0.34	3.29/ –0.34	N/A	ns
		XQ7Z030	N/A	N/A	3.02/ –0.34	3.02/ –0.34	N/A	3.29/ –0.34	3.29/ –0.34	N/A	ns
		XQ7Z045	N/A	N/A	3.24/ –0.20	3.24/ –0.20	N/A	3.53/ –0.20	3.53/ –0.20	3.53/ –0.20	ns
		XQ7Z100	N/A	N/A	3.24/ –0.21	3.24/ –0.21	N/A	3.53/ –0.21	N/A	N/A	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 86: **Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO**

Symbol	Description	Speed Grade				Units
		-3E	-2E/-2I-2LI	-1C/-1I	-1Q/-1LQ	
Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard.						
T_{PSCS}/T_{PHCS}	Setup/hold of I/O clock for HR I/O banks	–0.36/1.36	–0.36/1.50	–0.36/1.70	–0.36/1.70	ns
	Setup/hold of I/O clock for HP I/O banks	–0.34/1.39	–0.34/1.53	–0.34/1.73	–0.34/1.73	ns

Table 87: **Sample Window**

Symbol	Description	Speed Grade				Units
		-3E	-2E/-2I/-2LI	-1C/-1I	-1Q/-1LQ	
T_{SAMP}	Sampling error at receiver pins(1)	0.51	0.56	0.61	0.61	ns
T_{SAMP_BUFIO}	Sampling error at receiver pins using BUFIO(2)	0.30	0.35	0.40	0.40	ns

Notes:

1. This parameter indicates the total sampling error of the PL DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the PL DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for PL clock transmitter and receiver data-valid windows.

Table 88: **Package Skew**

Symbol	Description	Device	Package	Value	Units
$T_{PKGSKEW}$	Package skew(1)	XC7Z030	SBG485/SBV485	113	ps
			FBG484/FBV484	113	ps
			FBG676/FBV676	113	ps
			FFG676/FFV676	136	ps
		XC7Z035	FBG676/FBV676	159	ps
			FFG676/FFV676	158	ps
			FFG900/FFV900	191	ps
		XC7Z045	FBG676/FBV676	159	ps
			FFG676/FFV676	158	ps
			FFG900/FFV900	191	ps
		XC7Z100	FFG900/FFV900	161	ps
			FFG1156/FFV1156	165	ps
		XA7Z030	FBG484/FBV484	113	ps
		XQ7Z030	RB484	113	ps
			RF676	136	ps
		XQ7Z045	RF676/RFG676	158	ps
			RF900	191	ps
		XQ7Z100	RF900	161	ps
			RF1156	165	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

GTX Transceiver Specifications

GTX Transceiver DC Input and Output Levels

Table 89 summarizes the DC specifications of the GTX transceivers in Zynq-7000 devices. Consult the *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476) for further details.

Table 89: **GTX Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPOUT}	Differential peak-to-peak output voltage(1)	Transmitter output swing is set to maximum setting	1000	–	–	mV
$V_{CMOUTDC}$	DC common mode output voltage.	Equation based	$V_{MGTAVTT} - DV_{PPOUT}/4$			mV
R_{OUT}	Differential output resistance		–	100	–	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	2	12	ps
DV_{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	>10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V_{IN}	Single-ended input voltage(2)	DC coupled $V_{MGTAVTT}$ = 1.2V	–200	–	$V_{MGTAVTT}$	mV
V_{CMIN}	Common mode input voltage	DC coupled $V_{MGTAVTT}$ = 1.2V	–	2/3 $V_{MGTAVTT}$	–	mV
R_{IN}	Differential input resistance		–	100	–	Ω
C_{EXT}	Recommended external AC coupling capacitor(3)		–	100	–	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in the *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476) and can result in values lower than reported in this table.
2. Voltage measured at the pin referenced to ground.
3. Other values can be used as appropriate to conform to specific protocols and standards.

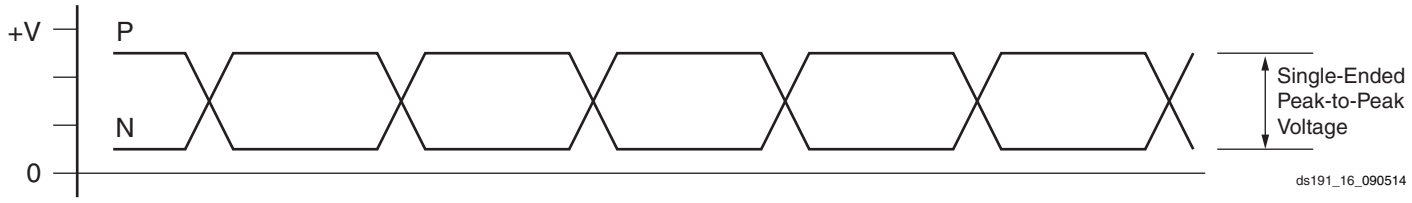

Figure 20: **Single-Ended Peak-to-Peak Voltage**

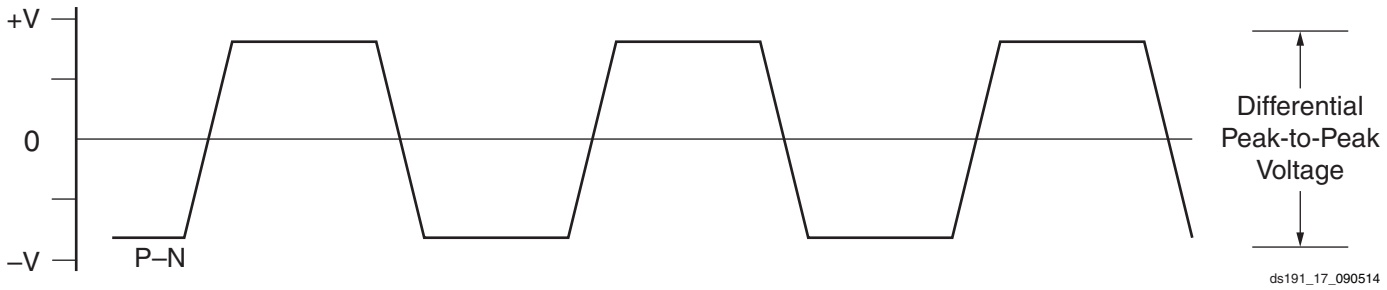

Figure 21: **Differential Peak-to-Peak Voltage**

Note: In Figure 21, differential peak-to-peak voltage = single-ended peak-to-peak voltage x 2.

Table 90 summarizes the DC specifications of the clock input of the GTX transceiver. Consult the *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476) for further details.

Table 90: **GTX Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	100	–	nF

GTX Transceiver Switching Characteristics

Consult the *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476) for further information. Performance specifications are divided between Table 91 and Table 92.

Table 91: **GTX Transceiver Performance for XC7Z030, XA7Z030, XC7Z035, XC7Z045, and XC7Z100 Devices by Package**

Symbol	Description	Output Divider	Speed Grade						Units
			-3E		-2E/-2I/-2LI		-1C/1I[1]		
			Package Type						
			FF	FB/SB	FF	FB/SB	FF	FB/SB	
F_{GTXMAX}[2]	Maximum GTX transceiver data rate		12.5	6.6	10.3125	6.6	8.0	6.6	Gb/s
F_{GTXMIN}[2]	Minimum GTX transceiver data rate		0.500	0.500	0.500	0.500	0.500	0.500	Gb/s
$F_{GTXCRANGE}$	CPLL line rate range	1	3.2–6.6						Gb/s
		2	1.6–3.3						Gb/s
		4	0.8–1.65						Gb/s
		8	0.5–0.825						Gb/s
		16	N/A						Gb/s
$F_{GTXQRANGE1}$	QPLL line rate range 1	1	5.93–8.0	5.93–6.6	5.93–8.0	5.93–6.6	5.93–8.0	5.93–6.6	Gb/s
		2	2.965–4.0		2.965–4.0		2.965–4.0		Gb/s
		4	1.4825–2.0		1.4825–2.0		1.4825–2.0		Gb/s
		8	0.74125–1.0		0.74125–1.0		0.74125–1.0		Gb/s
		16	N/A		N/A		N/A		Gb/s
$F_{GTXQRANGE2}$	QPLL line rate range 2[3]	1	9.8–12.5	N/A	9.8–10.3125	N/A	N/A		Gb/s
		2	4.9–6.25		4.9–5.15625		N/A		Gb/s
		4	2.45–3.125		2.45–2.578125		N/A		Gb/s
		8	1.225–1.5625		1.225–1.2890625		N/A		Gb/s
		16	0.6125–0.78125		0.6125–0.64453125		N/A		Gb/s
$F_{GCPLLRANGE}$	GTX transceiver CPLL frequency range		1.6–3.3		1.6–3.3		1.6–3.3		GHz
$F_{GQPLLRANGE1}$	GTX transceiver QPLL frequency range 1		5.93–8.0		5.93–8.0		5.93–8.0		GHz
$F_{GQPLLRANGE2}$	GTX transceiver QPLL frequency range 2		9.8–12.5		9.8–10.3125		N/A		GHz

Notes:

1. The -1 speed grade requires a 4-byte internal data width for operation above 5.0 Gb/s.
2. Data rates between 8.0 Gb/s and 9.8 Gb/s are not available.
3. For QPLL line rate range 2, the maximum line rate with the divider N set to 66 is 10.3125Gb/s.

Table 92: **GTX Transceiver Performance for the XQ7Z030, XQ7Z045, and XQ7Z100 Devices by Package**

Symbol	Description	Output Divider	Speed Grade						Units
			-2I		-1I[1]		-1Q/-1LQ[1]		
			Package Type						
			RF	RB	RF	RB	RF	RB	
F_{GTXMAX}[2]	Maximum GTX transceiver data rate		10.3125	6.6	8.0	6.6	8.0	6.6	Gb/s
F_{GTXMIN}[2]	Minimum GTX transceiver data rate		0.500	0.500	0.500	0.500	0.500	0.500	Gb/s
$F_{GTXCRANGE}$	CPLL line rate range	1	3.2–6.6						Gb/s
		2	1.6–3.3						Gb/s
		4	0.8–1.65						Gb/s
		8	0.5–0.825						Gb/s
		16	N/A						Gb/s
$F_{GTXQRANGE1}$	QPLL line rate range 1	1	5.93–8.0	5.93–6.6	5.93–8.0	5.93–6.6	5.93–8.0	5.93–6.6	Gb/s
		2	2.965–4.0		2.965–4.0		2.965–4.0		Gb/s
		4	1.4825–2.0		1.4825–2.0		1.4825–2.0		Gb/s
		8	0.74125–1.0		0.74125–1.0		0.74125–1.0		Gb/s
		16	N/A		N/A		N/A		Gb/s
$F_{GTXQRANGE2}$	QPLL line rate range 2[3]	1	9.8–10.3125	N/A	N/A		N/A		Gb/s
		2	4.9–5.15625		N/A		N/A		Gb/s
		4	2.45–2.578125		N/A		N/A		Gb/s
		8	1.225–1.2890625		N/A		N/A		Gb/s
		16	0.6125–0.64453125		N/A		N/A		Gb/s
$F_{GCPLLRANGE}$	GTX transceiver CPLL frequency range		1.6–3.3		1.6–3.3		1.6–3.3		GHz
$F_{GQPLLRANGE1}$	GTX transceiver QPLL frequency range 1		5.93–8.0		5.93–8.0		5.93–8.0		GHz
$F_{GQPLLRANGE2}$	GTX transceiver QPLL frequency range 2		9.8–10.3125		N/A		N/A		GHz

Notes:

1. The -1 speed grade requires a 4-byte internal data width for operation above 5.0 Gb/s.
2. Data rates between 8.0 Gb/s and 9.8 Gb/s are not available.
3. For QPLL line rate range 2, the maximum line rate with the divider N set to 66 is 10.3125Gb/s.

Table 93: **GTX Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3E	-2E/-2I/-2LI	-1C/-1I	-1Q/-1LQ	
$F_{GTXDRPCLK}$	GTXDRPCLK maximum frequency	175.01	175.01	156.25	156.25	MHz

Table 94: **GTX Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range	-3E speed grade	60	–	700	MHz
		All other speed grades	60	–	670	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	50	60	%

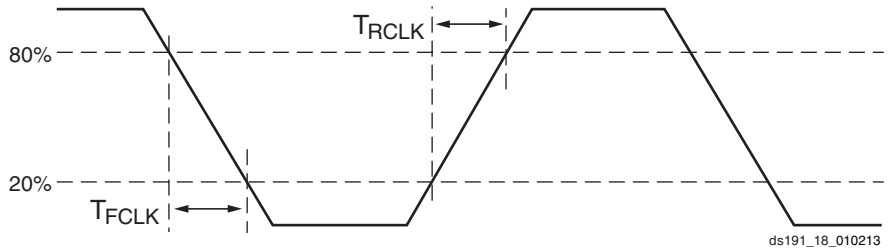

Figure 22: **Reference Clock Timing Parameters**

Table 95: **GTX Transceiver PLL/Lock Time Adaptation**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37×10^6	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–	50,000	2.3×10^6	UI

Table 96: **GTX Transceiver User Clock Switching Characteristics(1)(2)**

Symbol	Description	Data Width Conditions		Speed Grade (3)(4)				Units
		Internal Logic	Interconnect Logic	-3E	-2E/-2I/-2LI	-1C/-1I	-1Q/-1LQ	
F_{TXOUT}	TXOUTCLK maximum frequency			412.500	412.500	312.500	312.500	MHz
F_{RXOUT}	RXOUTCLK maximum frequency			412.500	412.500	312.500	312.500	MHz
F_{TXIN}	TXUSRCLK maximum frequency	16-bit	16-bit and 32-bit	412.500	412.500	312.500	312.500	MHz
		32-bit	32-bit	390.625	322.266	250.000	250.000	MHz
F_{RXIN}	RXUSRCLK maximum frequency	16-bit	16-bit and 32-bit	412.500	412.500	312.500	312.500	MHz
		32-bit	32-bit	390.625	322.266	250.000	250.000	MHz
F_{TXIN2}	TXUSRCLK2 maximum frequency	16-bit	16-bit	412.500	412.500	312.500	312.500	MHz
		16-bit and 32-bit	32-bit	390.625	322.266	250.000	250.000	MHz
		64-bit	64-bit	195.313	161.133	125.000	125.000	MHz
F_{RXIN2}	RXUSRCLK2 maximum frequency	16-bit	16-bit	412.500	412.500	312.500	312.500	MHz
		16-bit and 32-bit	32-bit	390.625	322.266	250.000	250.000	MHz
		64-bit	64-bit	195.313	161.133	125.000	125.000	MHz

Notes:

1. Clocking must be implemented as described in the *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476).
2. These frequencies are not supported for all possible transceiver configurations.
3. For speed grades -3 and -2, a 16-bit data path can only be used for speeds less than 6.6 Gb/s.
4. For speed grade -1, a 16-bit data path can only be used for speeds less than 5.0 Gb/s.

Table 97: **GTX Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTXTX}	Serial data rate range		0.500	–	F_{GTXMAX}	Gb/s
T_{RTX}	TX rise time	20%–80%	–	40	–	ps
T_{FTX}	TX fall time	80%–20%	–	40	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	500	ps
$V_{TXOOBVDPP}$	Electrical idle amplitude		–	–	15	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time		–	–	140	ns
$TJ_{12.5}$	Total jitter(2)(4)	12.5 Gb/s	–	–	0.28	UI
$DJ_{12.5}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$TJ_{11.18}$	Total jitter(2)(4)	11.18 Gb/s	–	–	0.28	UI
$DJ_{11.18}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$TJ_{10.3125}$	Total jitter(2)(4)	10.3125 Gb/s	–	–	0.28	UI
$DJ_{10.3125}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$TJ_{9.953}$	Total jitter(2)(4)	9.953 Gb/s	–	–	0.28	UI
$DJ_{9.953}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$TJ_{9.8}$	Total jitter(2)(4)	9.8 Gb/s	–	–	0.28	UI
$DJ_{9.8}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$TJ_{8.0}$	Total jitter(2)(4)	8.0 Gb/s	–	–	0.33	UI
$DJ_{8.0}$	Deterministic jitter(2)(4)		–	–	0.17	UI

Table 97: **GTX Transceiver Transmitter Switching Characteristics *(Cont'd)***

Symbol	Description	Condition	Min	Typ	Max	Units
$TJ_{6.6\_QPLL}$	Total jitter(2)(4)	6.6 Gb/s	–	–	0.28	UI
$DJ_{6.6\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$TJ_{6.6\_CPLL}$	Total jitter(3)(4)	6.6 Gb/s	–	–	0.30	UI
$DJ_{6.6\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.15	UI
$TJ_{5.0}$	Total jitter(3)(4)	5.0 Gb/s	–	–	0.33	UI
$DJ_{5.0}$	Deterministic jitter(3)(4)		–	–	0.15	UI
$TJ_{4.25}$	Total jitter(3)(4)	4.25 Gb/s	–	–	0.33	UI
$DJ_{4.25}$	Deterministic jitter(3)(4)		–	–	0.14	UI
$TJ_{3.75}$	Total jitter(3)(4)	3.75 Gb/s	–	–	0.34	UI
$DJ_{3.75}$	Deterministic jitter(3)(4)		–	–	0.16	UI
$TJ_{3.2}$	Total jitter(3)(4)	3.20 Gb/s(5)	–	–	0.2	UI
$DJ_{3.2}$	Deterministic jitter(3)(4)		–	–	0.1	UI
$TJ_{3.2L}$	Total jitter(3)(4)	3.20 Gb/s(6)	–	–	0.35	UI
$DJ_{3.2L}$	Deterministic jitter(3)(4)		–	–	0.16	UI
$TJ_{2.5}$	Total jitter(3)(4)	2.5 Gb/s(7)	–	–	0.20	UI
$DJ_{2.5}$	Deterministic jitter(3)(4)		–	–	0.08	UI
$TJ_{1.25}$	Total jitter(3)(4)	1.25 Gb/s(8)	–	–	0.15	UI
$DJ_{1.25}$	Deterministic jitter(3)(4)		–	–	0.06	UI
TJ_{500}	Total jitter(3)(4)	500 Mb/s	–	–	0.1	UI
DJ_{500}	Deterministic jitter(3)(4)		–	–	0.03	UI

Notes:

1. Using same REFCLK input with TX phase alignment enabled for up to 12 consecutive transmitters (three fully populated GTX Quads).
2. Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
4. All jitter values are based on a bit-error ratio of $1e^{-12}$.
5. CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
6. CPLL frequency at 1.6 GHz and TXOUT_DIV = 1.
7. CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
8. CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.

Table 98: **GTX Transceiver Receiver Switching Characteristics**

Symbol	Description		Min	Typ	Max	Units
F_{GTXRX}	Serial data rate		0.500	–	F_{GTXMAX}	Gb/s
$T_{RXELECIDLE}$	Time for RXELECIDLE to respond to loss or restoration of data		–	10	–	ns
$RX_{OOBVDPP}$	OOB detect threshold peak-to-peak		60	–	150	mV
RX_{SST}	Receiver spread-spectrum tracking(1)	Modulated @ 33 KHz	–5000	–	0	ppm
RX_{RL}	Run length (CID)		–	–	512	UI
RX_{PPMTOL}	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm
		Bit rates > 8.0 Gb/s	–200	–	200	ppm
SJ Jitter Tolerance(2)						
$JT\_SJ_{12.5}$	Sinusoidal jitter (QPLL)(3)	12.5 Gb/s	0.3	–	–	UI
$JT\_SJ_{11.18}$	Sinusoidal jitter (QPLL)(3)	11.18 Gb/s	0.3	–	–	UI
$JT\_SJ_{10.32}$	Sinusoidal jitter (QPLL)(3)	10.32 Gb/s	0.3	–	–	UI
$JT\_SJ_{9.95}$	Sinusoidal jitter (QPLL)(3)	9.95 Gb/s	0.3	–	–	UI
$JT\_SJ_{9.8}$	Sinusoidal jitter (QPLL)(3)	9.8 Gb/s	0.3	–	–	UI
$JT\_SJ_{8.0}$	Sinusoidal jitter (QPLL)(3)	8.0 Gb/s	0.44	–	–	UI
$JT\_SJ_{6.6\_QPLL}$	Sinusoidal jitter (QPLL)(3)	6.6 Gb/s	0.48	–	–	UI
$JT\_SJ_{6.6\_CPLL}$	Sinusoidal jitter (CPLL)(3)	6.6 Gb/s	0.44	–	–	UI
$JT\_SJ_{5.0}$	Sinusoidal jitter (CPLL)(3)	5.0 Gb/s	0.44	–	–	UI
$JT\_SJ_{4.25}$	Sinusoidal jitter (CPLL)(3)	4.25 Gb/s	0.44	–	–	UI
$JT\_SJ_{3.75}$	Sinusoidal jitter (CPLL)(3)	3.75 Gb/s	0.44	–	–	UI
$JT\_SJ_{3.2}$	Sinusoidal jitter (CPLL)(3)	3.2 Gb/s(4)	0.45	–	–	UI
$JT\_SJ_{3.2L}$	Sinusoidal jitter (CPLL)(3)	3.2 Gb/s(5)	0.45	–	–	UI
$JT\_SJ_{2.5}$	Sinusoidal jitter (CPLL)(3)	2.5 Gb/s(6)	0.5	–	–	UI
$JT\_SJ_{1.25}$	Sinusoidal jitter (CPLL)(3)	1.25 Gb/s(7)	0.5	–	–	UI
JT_SJ_{500}	Sinusoidal jitter (CPLL)(3)	500 Mb/s	0.4	–	–	UI
SJ Jitter Tolerance with Stressed Eye(2)						
$JT\_TJSE_{3.2}$	Total jitter with stressed eye(8)	3.2 Gb/s	0.70	–	–	UI
		6.6 Gb/s	0.70	–	–	UI
$JT\_SJSE_{3.2}$	Sinusoidal jitter with stressed eye(8)	3.2 Gb/s	0.1	–	–	UI
		6.6 Gb/s	0.1	–	–	UI

Notes:

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of $1e^{-12}$.
3. The frequency of the injected sinusoidal jitter is 10 MHz.
4. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. CPLL frequency at 1.6 GHz and RXOUT_DIV = 1.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
7. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
8. Composite jitter with RX and LPM or DFE mode.

GTX Transceiver Protocol Jitter Characteristics

For Table 99 through Table 104, the *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476) contains recommended settings for optimal usage of protocol specific characteristics.

Table 99: **Gigabit Ethernet Protocol Characteristics**

Description	Line Rate (Mb/s)	Min	Max	Units
Gigabit Ethernet Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	1250	–	0.24	UI
Gigabit Ethernet Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	1250	0.749	–	UI

Table 100: **XAUI Protocol Characteristics**

Description	Line Rate (Mb/s)	Min	Max	Units
XAUI Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	3125	–	0.35	UI
XAUI Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	3125	0.65	–	UI

Table 101: **PCI Express Protocol Characteristics**(1)

Standard	Description		Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation						
PCI Express Gen 1	Total transmitter jitter		2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter		5000	–	0.25	UI
PCI Express Gen 3	Total transmitter jitter uncorrelated		8000	–	31.25	ps
	Deterministic transmitter jitter uncorrelated			–	12	ps
PCI Express Receiver High Frequency Jitter Tolerance						
PCI Express Gen 1	Total receiver jitter tolerance		2500	0.65	–	UI
PCI Express Gen 2(2)	Receiver inherent timing error		5000	0.40	–	UI
	Receiver inherent deterministic timing error			0.30	–	UI
PCI Express Gen 3	Receiver sinusoidal jitter tolerance	0.03 MHz–1.0 MHz	8000	1.00	–	UI
		1.0 MHz–10 MHz		Note 3	–	UI
		10 MHz–100 MHz		0.10	–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. Using common REFCLK.
3. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20 dB/decade.

Table 102: **CEI-6G and CEI-11G Protocol Characteristics**

Description	Line Rate (Mb/s)	Interface	Min	Max	Units
CEI-6G Transmitter Jitter Generation					
Total transmitter jitter(1)	4976–6375	CEI-6G-SR	–	0.3	UI
		CEI-6G-LR	–	0.3	UI
CEI-6G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance(1)	4976–6375	CEI-6G-SR	0.6	–	UI
		CEI-6G-LR	0.95	–	UI
CEI-11G Transmitter Jitter Generation					
Total transmitter jitter(2)	9950–11100	CEI-11G-SR	–	0.3	UI
		CEI-11G-LR/MR	–	0.3	UI
CEI-11G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance(2)	9950–11100	CEI-11G-SR	0.65	–	UI
		CEI-11G-MR	0.65	–	UI
		CEI-11G-LR	0.825	–	UI

Notes:

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.
2. Tested at line rate of 9950 Mb/s using 155.46875 MHz reference clock and 11100 Mb/s using 173.4375 MHz reference clock.

Table 103: **SFP+ Protocol Characteristics**

Description	Line Rate (Mb/s)	Min	Max	Units
SFP+ Transmitter Jitter Generation				
Total transmitter jitter	9830.40(1)	–	0.28	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			
SFP+ Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	9830.40(1)	0.7	–	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			

Notes:

1. Line rated used for CPRI over SFP+ applications.

Table 104: **CPRI Protocol Characteristics**

Description	Line Rate (Mb/s)	Min	Max	Units
CPRI Transmitter Jitter Generation				
Total transmitter jitter	614.4	–	0.35	UI
	1228.8	–	0.35	UI
	2457.6	–	0.35	UI
	3072.0	–	0.35	UI
	4915.2	–	0.3	UI
	6144.0	–	0.3	UI
	9830.4	–	Note 1	UI
CPRI Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	614.4	0.65	–	UI
	1228.8	0.65	–	UI
	2457.6	0.65	–	UI
	3072.0	0.65	–	UI
	4915.2	0.95	–	UI
	6144.0	0.95	–	UI
	9830.4	Note 1	–	UI

Notes:

1. Tested per SFP+ specification, see Table 103.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:
http://www.xilinx.com/technology/protocols/pciexpress.htm

Table 105: **Maximum Performance for PCI Express Designs**

Symbol	Description	Speed Grade				Units
		-3E	-2E/-2I/-2LI	-1C/-1I	-1Q/-1LQ	
$F_{PIPECLK}$	Pipe clock maximum frequency	250	250	250	250	MHz
$F_{USERCLK}$	User clock maximum frequency	500	500	250	250	MHz
$F_{USERCLK2}$	User clock 2 maximum frequency	250	250	250	250	MHz
F_{DRPCLK}	DRP clock maximum frequency	250	250	250	250	MHz

Notes:

1. PCI Express x8 Gen 2 operation is only supported in -2 and -3 speed grades. Refer to *7 Series FPGAs Integrated Block for PCI Express Product Guide* (PG054) for specific supported core configurations.

XADC Specifications

Table 106: **XADC Specifications**

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V_{CCADC} = 1.8V ± 5%, V_{REFP} = 1.25V, V_{REFN} = 0V, ADCCLK = 26 MHz, –55°C ≤ T_j ≤ 125°C, Typical values at T_j=+40°C						
ADC Accuracy(1)						
Resolution			12	–	–	Bits
Integral Nonlinearity(2)	INL	–40°C ≤ T_j ≤ 100°C	–	–	±2	LSBs
		–55°C ≤ T_j < –40°C; 100°C < T_j ≤ 125°C	–	–	±3	LSBs
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs
Offset Error	Unipolar	–40°C ≤ T_j ≤ 100°C	–	–	±8	LSBs
		–55°C ≤ T_j < –40°C; 100°C < T_j ≤ 125°C	–	–	±12	LSBs
	Bipolar	–55°C ≤ T_j ≤ 125°C	–	–	±4	LSBs
Gain Error			–	–	±0.5	%
Offset Matching			–	–	4	LSBs
Gain Matching			–	–	0.3	%
Sample Rate			–	–	1	MS/s
Signal to Noise Ratio(2)	SNR	F_{SAMPLE} = 500KS/s, F_{IN} = 20KHz	60	–	–	dB
RMS Code Noise		External 1.25V reference	–	–	2	LSBs
		On-chip reference	–	3	–	LSBs
Total Harmonic Distortion(2)	THD	F_{SAMPLE} = 500KS/s, F_{IN} = 20KHz	70	–	–	dB
Analog Inputs(3)						
ADC Input Ranges		Unipolar operation	0	–	1	V
		Bipolar operation	–0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum External Channel Input Ranges		Adjacent analog channels set within these ranges should not corrupt measurements on adjacent channels	–0.1	–	V_{CCADC}	V
Auxiliary Channel Full Resolution Bandwidth	FRBW		250	–	–	KHz
On-Chip Sensors						
Temperature Sensor Error		–40°C ≤ T_j ≤ 100°C	–	–	±4	°C
		–55°C ≤ T_j < –40°C; 100°C < T_j ≤ 125°C	–	–	±6	°C
Supply Sensor Error		–40°C ≤ T_j ≤ 100°C	–	–	±1	%
		–55°C ≤ T_j < –40°C; 100°C < T_j ≤ 125°C	–	–	±2	%
Conversion Rate(4)						
Conversion Time - Continuous	t_{CONV}	Number of ADCCLK cycles	26	–	32	Cycles
Conversion Time - Event	t_{CONV}	Number of CLK cycles	–	–	21	Cycles
DRP Clock Frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1	–	26	MHz
DCLK Duty Cycle			40	–	60	%

Table 106: **XADC Specifications *(Cont'd)***

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
XADC Reference[5]						
External Reference	V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-Chip Reference		Ground V_{REFP} pin to AGND, –40°C ≤ T_j ≤ 100°C	1.2375	1.25	1.2625	V
		Ground V_{REFP} pin to AGND, –55°C ≤ T_j < –40°C; 100°C < T_j ≤ 125°C	1.225	1.25	1.275	V

Notes:

1. Offset and gain errors are removed by enabling the XADC automatic gain calibration feature. The values are specified for when this feature is enabled.
2. Only specified for bitstream option XADCEnhancedLinearity = ON.
3. See the ADC chapter in the *7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480) for a detailed description.
4. See the Timing chapter in the *7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480) for a detailed description.
5. Any variation in the reference voltage from the nominal V_{REFP} = 1.25V and V_{REFN} = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted.

Configuration Switching Characteristics

Table 107: **Configuration Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3E	-2E/-2I/-2LI	-1C/-1I	-1Q/-1LQ	
Power-up Timing Characteristics						
T_{PL}[1]	Program latency	5.00	5.00	5.00	5.00	ms, Max
T_{POR}	Power-on reset (50 ms ramp rate time)	10/50	10/50	10/50	10/50	ms, Min/Max
	Power-on reset (1 ms ramp rate time) with the power-on reset override function disabled; (`devcfg.CTRL.PCFG_POR_CNT_4K = 0`).[2]	10/35	10/35	10/35	10/35	ms, Min/Max
	Power-on reset (1 ms ramp rate time) with the power-on reset override function enabled; (`devcfg.CTRL.PCFG_POR_CNT_4K = 1`).[2]	2/8	2/8	2/8	2/8	ms, Min/Max
$T_{PROGRAM}$	Program pulse width	250.00	250.00	250.00	250.00	ns, Min
Boundary-Scan Port Timing Specifications						
T_{TAPTCK}/T_{TCKTAP}	TMS and TDI setup/hold	3.00/2.00	3.00/2.00	3.00/2.00	3.00/2.00	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output	7.00	7.00	7.00	7.00	ns, Max
F_{TCK}	TCK frequency	66.00	66.00	66.00	66.00	MHz, Max
Internal Configuration Access Port						
F_{ICAPCK}	Internal configuration access port (ICAPE2)	100.00	100.00	100.00	100.00	MHz, Max
Device DNA Access Port						
F_{DNACK}	DNA access port (DNA_PORT)	100.00	100.00	100.00	100.00	MHz, Max

Notes:

1. To support longer delays in configuration, use the design solutions described in the *7 Series FPGA Configuration User Guide* (UG470).
2. For non-secure boot only. Measurement is made when the PS is already powered and stable, before power cycling the PL.

eFUSE Programming Conditions

Table 108 lists the programming conditions specifically for eFUSE. For more information, see the *7 Series FPGA Configuration User Guide* (UG470).

Table 108: **eFUSE Programming Conditions(1)**

Symbol	Description	Min	Typ	Max	Units
I_{PLFS}	PL V_{CCAUX} supply current	–	–	115	mA
I_{PSFS}	PS V_{CCPAUX} supply current	–	–	115	mA
t_j	Temperature range	15	–	125	°C

Notes:

1. The Zynq-7000 devices must not be configured during eFUSE programming.

Revision History

The following table shows the revision history for this document:

Date	Version	Description
08/23/2012	1.0	Initial Xilinx release.
08/31/2012	1.1	Updated T_j and added Note 3 to Table 2. Updated R_{IN_TERM} in Table 3. Updated standards in Table 9. Revised PS Performance Characteristics section introduction. Updated values in Table 19. Added Note 4 to Table 36. Added notes to Table 38. Revised $F_{MSPICLK}$ in Table 43.
03/14/2013	1.2	Updated the AC Switching Characteristics based upon ISE tools 14.5 and Vivado tools 2013.1, both at v1.06 for the -3, -2, and -1 speed specifications throughout the document. Updated Table 17 and Table 18 for production release of the XC7Z045 in the -2 and -1 speed designations. Added the XC7Z100 device throughout document. Updated description in Introduction. Added Note 2 to Table 2. Updated V_{PIN} in Table 1 and Table 2. Clarified PS specifications for C_{PIN}(2) and removed Note 3 on I_{RPD} in Table 3. Updated Table 6. Updated Table 9, including removal of LVTTL, notes 2 and 3, and adding SSTL135. Added Table 10. Many enhancements and additions to the figures and tables in the PS Switching Characteristics section including adding notes with test conditions where applicable. Replaced or updated Table 19 through Table 21. Removed AXI Interconnects section. Updated Note 1 in Table 73. Updated Note 1 and Note 2 in Table 88. In Table 91, increased -1 speed grade (FF package) F_{GTXMAX} value from 6.6 Gb/s to 8.0 Gb/s. Updated the rows on offset error and gain error and matching in Table 106. Added Internal Configuration Access Port section to Table 107.
03/27/2013	1.3	In Table 7, changed $I_{CCINTMIN}$ value for the XC7Z030. Updated Table 17 and Table 18 for production release of the XC7Z030 in the -2 and -1 speed designations. In Table 53, updated the table title, LPDDR2 values, and removed Note 3. In Table 54, updated the table title and removed Note 4.
04/24/2013	1.4	Updated Table 17 and Table 18 for production release of the XC7Z030 and XC7Z045 in the -3 speed designations. Removed the *PS Power-on Reset* section. Updated the PS—PL Power Sequencing section. Clarified the load conditions in Table 36 by adding new data. In Table 1, revised V_{IN} (I/O input voltage) to match values in Table 4 and Table 5, and combined Note 4 with old Note 5 and then added new Note 6. Revised V_{IN} description and added Note 10, and updated Note 3 in Table 2. Updated first 3 rows in Table 4 and Table 5. Revised PCI33_3 voltage minimum in Table 11 to match values in Table 1, Table 4, and Table 5. Added Note 1 to Table 14 and Table 15. Added Note 2 to Table 20. Throughout the data sheet (Table 67, Table 68, and Table 83) removed the obvious note “A Zero “0” Hold Time listing indicates no hold time or a negative hold time.” Updated and clarified USRCLK data in Table 96.

Date	Version	Description
06/26/2013	1.5	Updated the AC Switching Characteristics based upon ISE tools 14.6 and Vivado tools 2013.2, both at v1.07 for the -3, -2, and -1 speed specifications throughout the document. Updated Table 17 and Table 18 for production release of the XC7Z100 in the -1 and -2 speed designations. In Table 1, updated I_{DCIN} section for cases when floating, at $V_{MGTAVTT}$, or GND and I_{DCOUT} for cases when floating and at $V_{MGTAVTT}$. Added Note 6 to Table 2. Added XC7Z100 values to Table 6 and Table 7. Increased the frequency of -2 speed grade for CPU clock performance (6:2:1) in Table 19. Updated the F_{DDR3L_MAX} value in Table 20. Moved Table 21 and added F_{AXI_MAX}. Removed Note 1 from Table 22. Updated the minimum $T_{DQVALID}$ values in Table 27 and Table 28. Added Table 29. In Table 40, corrected the F_{SDSCLK} maximum value and $F_{SDIDCLK}$ units typographical errors. Updated the description of F_{GTXRX} in Table 98.
09/12/2013	1.6	Added the SBG485 package to Table 88. Added USRCCLK Output section and clarified values for T_{POR} in Table 107. Added I_{PSFS} to Table 108. Updated Notice of Disclaimer.
11/26/2013	1.7	Added specifications for the Zynq-7000Q devices (XQ7Z030 and XQ7Z045) with the -1Q speed specification/temperature range. Removed Note 1 and Note 2 from Table 7. Added Table 16. In Table 36, updated $T_{QSPICKO1}$. Added Table 92. Updated Table 106 specifications. In Table 107, removed the USRCCLK Output section, added T_{PL}, $T_{PROGRAM}$, Note 1, and the Device DNA Access Port section, and updated the T_{POR} description.
03/03/2014	1.8	Added Note 4 to V_{CCAUX_IO} in Table 1. Updated Note 8 in Table 2 and added Note 9. Added Note 2 to Table 4. Added Note 2 and Note 3 to Table 5. Clarified description in Table 14 and Table 15. Updated Table 16. Moved the XQ7Z030 (all speed specifications/temperature ranges) to production release in Table 17 and Table 18. Added HSUL_12_F, DIFF_HSUL_12_F, MOBILE_DDR_S, MOBILE_DDR_F, DIFF_MOBILE_DDR_S, and DIFF_MOBILE_DDR_F standards to and updated values in Table 55. Added HSUL_12_F, DIFF_HSUL_12_F, DIFF_HSUL_12_DCI_S, and DIFF_HSUL_12_DCI_F standards to and updated values in Table 56. Added data for the RF900 and the SBG485 packages in Table 88. Added Note 1 to Table 105.
04/02/2014	1.9	Updated Table 17 and Table 18 for production release of the XQ7Z045 in all speed designations. Updated the speed specifications for T_{IOTP} and removed notes from Table 55 and Table 56.
06/04/2014	1.10	Added the XA7Z030 devices (-1I and -1Q) in the FBG484 package throughout the document. In Table 4 and Table 5, updated Note 2 per the customer notice XCN14014: *7 Series FPGA and Zynq-7000 AP SoC I/O Undershoot Voltage Data Sheet Update*. Updated Note 3 in Table 6. Updated for clarification the DDR timing diagrams in Figure 2 and Figure 3. Removed Note 1 from Table 105.
09/23/2014	1.11	Removed 1.8V as descriptor of HP I/O banks and 3.3V as descriptor of HR I/O banks throughout. Updated Note 3 in Table 6. In PL Power-On/Off Power Supply Sequencing, added sentence about there being no recommended sequence for supplies not shown. In PS—PL Power Sequencing, removed list of PL power supplies. In Table 17, moved -1I and -1Q XA7Z030 speed grades from Preliminary to Production. In Table 18, added production software for XA7Z030 -1I and -1Q speed grades. Updated $F_{CPU\_3X2X\_621\_MAX}$, $F_{CPU\_2X\_621\_MAX}$, $F_{CPU\_6X4X\_421\_MAX}$, and $F_{CPU\_1X\_421\_MAX}$ values in Table 19. In Table 22, removed typical value and added maximum value for $T_{RFPSCLK}$. Added note about measurement being taken from V_{REF} to V_{REF} in Table 27 to Table 34. Added Note 3 to Table 53. Added I/O Standard Adjustment Measurement Methodology. In Table 64, added attribute REFCLK frequency of 400 MHz to $F_{IDELAYCTRL\_REF}$ and average tap delay at 400 MHz to Note 1. Updated description of T_{ICKOF} in Table 78 and added Note 2. Updated description of $T_{ICKOFFAR}$ in Table 79 and added Note 2. In Table 89, moved DV_{PPOUT} value of 1000 mV from Max to Min column, updated V_{IN} DC parameter description, and added Note 2. Added *peak-to-peak* to labels in Figure 20 and Figure 21. Added note after Figure 21. Added Note 1 to Table 105.
10/09/2014	1.12	Added XC7Z035 device. Added -2LI speed grade throughout. Updated Introduction. Added -2LI (0.95V) to description of V_{CCINT} and V_{CCBRAM}, and added PL to description of V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, V_{CCO} and V_{CCAUX_IO} in Table 2. Added Note 1 to Table 18.
11/19/2014	1.13	Added V_{CCBRAM} and XA Zynq-7000 All Programmable SoC Overview to Introduction. Updated the AC Switching Characteristics based upon Vivado 2014.4. Updated Vivado software version in Table 16. In Table 17, moved all speed grades from Advance to Production. In Table 18, added Vivado 2014.4 software version for -2LI speed grade in XC7Z030 and XC7Z045 devices and -3E, -2E, -2I, -2LI, -1C, and -1I speed grades in XC7Z035 device, and removed table note. Added Selecting the Correct Speed Grade and Voltage in the Vivado Tools. Added Note 1 to Table 51.

Date	Version	Description
02/23/2015	1.14	Updated descriptions of V_{CCPINT} in Table 1 and Table 2. In Table 14, changed maximum V_{ICM} value from 1.425V to 1.500V. Updated Table 24 title. Added Figure 1 and Table 25. Updated first sentence in PL Power-On/Off Power Supply Sequencing. In Table 36, updated minimum $T_{QSPIDCK2}$ and $T_{QSPICKD2}$ to 6 ns and 12.5 ns, respectively, and removed note 5. In Table 70, updated symbols for $T_{DSPDCK\_\{A, B\}\_MREG\_MULT}/T_{DSPCKD\_\{A, B\}\_MREG\_MULT}$, $T_{DSPDCK\_\{A, D\}\_ADREG}/T_{DSPCKD\_\{A, D\}\_ADREG}$, $T_{DSPDCK\_\{A, B\}\_PREG\_MULT}/T_{DSPCKD\_\{A, B\}\_PREG\_MULT}$, $T_{DSPDCK\_\{A, B\}\_PREG}/T_{DSPCKD\_\{A, B\}\_PREG}$, $T_{DSPDCK\_\{CEA, CEB\}\_\{AREG, BREG\}}/T_{DSPCKD\_\{CEA, CEB\}\_\{AREG, BREG\}}$, and $T_{DSPDCK\_\{RSTA, RSTB\}\_\{AREG, BREG\}}/T_{DSPCKD\_\{RSTA, RSTB\}\_\{AREG, BREG\}}$. In Table 76, updated descriptions of $T_{MMCMDCK\_DADDR}/T_{MMCMCKD\_DADDR}$, $T_{MMCMDCK\_DI}/T_{MMCMCKD\_DI}$, $T_{MMCMDCK\_DEN}/T_{MMCMCKD\_DEN}$, and $T_{MMCMDCK\_DWE}/T_{MMCMCKD\_DWE}$. Added descriptive row to Table 86. Removed minimum sample rate specification from Table 106.
06/23/2015	1.15	Added XQ7Z100 device throughout. Added -1LQ speed grade to XQ7Z045 device. Updated the AC Switching Characteristics based upon ISE tools 14.7 and Vivado tools 2015.2. Updated Table 53 title to refer to FF packages. Updated Table 54 title and Note 3 to refer to FB, RB, and SB packages. Removed “FPGA” from labels in Figure 18 and Figure 19. Added SBV485, FBV484, FBV676, FFV676, FFV900, FFV1156, RFG676, and RF1156 packages to Table 88. Removed note about PCI-SIG 3.0 from Table 101.
09/28/2015	1.16	Updated data sheet per the customer notice XCN15034: *Zynq-7000 AP SoC Requirement for the PS Power-Off Sequence*. Updated PS Power-On/Off Power Supply Sequencing. Added $F_{SMC\_REF\_CLK}$ to Table 35. Changed -2E and -1C speed grade XC7Z100 devices to N/A in Table 6, Table 18, Table 75, Table 78 to Table 81, and Table 83 to Table 85. Added introductory paragraph before Table 53 and updated Note 3.
11/24/2015	1.17	Updated quiescent supply currents for XQ7Z030, XQ7Z045, and XQ7Z100 in Table 6. Updated the AC Switching Characteristics based upon Vivado 2015.4. In Table 17, added -2LI speed grade to production column for XQ7Z030 and XQ7Z045, and added -2I and -2LI speed grades to production column for XQ7Z100. In Table 18, added Vivado 2015.4 software version to -2LI speed grade column for XQ7Z030, XQ7Z045, and XQ7Z100, and -2I speed grade column for XQ7Z100. In Figure 4 and Figure 5, added extra clock pulse on QSPI_SCLK_OUT. In Table 75, added T_{CKSKEW} for XQ7Z030, XQ7Z045, and XQ7Z100 at -2LI speed grade, and XQ7Z100 at -2I speed grade. Updated device pin-to-pin output parameter tables (Table 78 to Table 81) and input parameter tables (Table 83 to Table 85) for XQ7Z030, XQ7Z045, and XQ7Z100 at -2LI and -2I speed grades.

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