Hi3518 HD IP Camera SoC

Data Sheet

Issue 01

Date 2013-02-05

HiSilicon Technologies Co., Ltd.

Address: Huawei Industrial Base
Bantian, Longgang
Shenzhen 518129
People's Republic of China

Website: http://www.hisilicon.com

Email: support@hisilicon.com

Contents

About This Document

Purpose

This document describes the features, logical structures, functions, operating modes, and related registers of each module of the Hi3518. This document also describes the interface timings and related parameter in diagrams. In addition, this document details the pins, pin usages, performance parameters, and package of the Hi3518.

Related Version

The following table lists the product version related to this document.

Product Name	Version
Hi3518	V100

Intended Audience

This document is intended for:

- Design and maintenance personnel for electronics
- Sales personnel for electronic components

Conventions

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
 DANGER	Indicates a hazard with a high level of risk which, if not avoided, will result in death or serious injury.

Symbol	Description
 WARNING	Indicates a hazard with a medium or low level of risk that, if not avoided, could result in minor or moderate injury.
 CAUTION	Indicates a potentially hazardous situation, which if not avoided, could result in equipment damage, data loss, performance degradation, or unexpected results.
TIP	Indicates a tip that may help you solve a problem or save time.
 NOTE	Provides additional information to emphasize or supplement important points of the main text.

General Conventions

The general conventions that may be found in this document are defined as follows.

Convention	Description
Times New Roman	Normal paragraphs are in Times New Roman.
Boldface	Names of files, directories, folders, and users are in **boldface**. For example, log in as user **root**.
Italic	Book titles are in *italics*.
`Courier New`	Examples of information displayed on the screen are in `Courier New`.

Table Content Conventions

The table content conventions that may be found in this document are defined as follows.

Content	Description
–	The cell is blank.
*	The content in this cell is configurable.

Notes

Register Attributes

The register attributes that may be found in this document are defined as follows.

Symbol	Description	Symbol	Description
RO	The register is read-only.	RW	The register is read/write.
RC	The register is cleared on a read.	WC	The register can be read. The register is cleared when 1 is written. The register keeps unchanged when 0 is written.

Reset Value Conventions

In the register definition tables:

- If the reset value (for the Reset row) of a bit is "?", the reset value is undefined.
- If the reset values of one or multiple bits are "?", the total reset value of a register is undefined and is marked as "-".

Numerical System

The expressions of data capacity, frequency, and data rate are described as follows.

Type	Symbol	Value
Data capacity (such as the RAM capacity)	K	1024
	M	1,048,576
	G	1,073,741,824
Frequency, data rate	k	1000
	M	1,000,000
	G	1,000,000,000

The expressions of addresses and data are described as follows.

Symbol	Example	Description
0x	0xFE04, 0x18	Address or data in hexadecimal
0b	0b000, 0b00 00000000	Data or sequence in binary (register description is excluded.)
X	00X, 1XX	In data expression, X indicates 0 or 1. For example, 00X indicates 000 or 001 and 1XX indicates 100, 101, 110, or 111.

Others

All frequencies in this document all comply with the SDH standard. The shortened frequency names and the corresponding nominal frequencies are as follows.

Shortened Frequency Name	Nominal Frequency
19 M	19.44 MHz
38 M	38.88 MHz
77 M	77.76 MHz
622 M	622.08 MHz

Change History

Changes between document issues are cumulative. Therefore, the latest document issue contains all changes made in previous issues.

Issue 01(2013-02-05)

This issue is the tihrd official release, which incorporates the following changes:

Chapter 10 Video Interfaces

In section 10.1.3.2, the descriptions of the DC interface timings are updated.

Issue 00B05 (2012-12-26)

Chapter 1 Introduction

The DDR frequency is changed to 400 MHz, and the CPU frequency is changed to 440 MHz.

In section 1.2.4, the description of bit rate control in CBR, VBR, or ABR mode is modified.

Chapter 3 System

In section 3.9.4.6, the description of RTC automatic temperature counting correction is modified.

The descriptions of RTC_SAR_CTRL, OUTSIDE_TEMP, DIE_TEMP, and TEMP_SEL are modified.

The reset value for PERIPHCTRL12 is modified.

Chapter 4 Memory Interfaces

The descriptions of DDRC_EMRS01 and DDRC_EMRS23 are modified.

The DDRC_QOSCFG0 register is deleted.

DDRC_QOS is set as the command priority configuration register for the DDRC, and meanings of each bit are modified.

Chapter 10 Video Interfaces

The reset values for the offset addresses 0xC4AC and 0xC4B0 are modified.

Issue 00B04 (2012-11-25)

This issue is the third draft release, which incorporates the following changes:

Chapter 1 Introduction

In section 1.2.9, the digital watermark function is deleted.

Chapter 2 Hardware

In section 2.6, power consumption parameters and temperature and thermal resistance parameters are added.

Chapter 3 System

In section 3.9.4.4, the descriptions of the operations to be performed are updated.

Chapter 4 Memory Interfaces

In section 4.1.4.3, step 16 is updated and notes are added.

In section 4.1.4.4, step 17 is updated and notes are added.

In section 4.1.6, the descriptions of the DDRC_PUB_MR0, DDRC_PUB_MR1, DDRC_PUB_MR2, and DDRC_PUB_MR3 registers are updated.

Chapter 7 Video and Graphics Processing

In section 7.2.2, the image width described in the image processing by block condition is changed from 960 to 512.

Chapter 10 Video Interfaces

In section 10.3.1.2, the norm descriptions of the horizontal and vertical timings for ITU-R BT.601 YCbCr4:2:2 are changed.

Chapter 13 Peripherals

In section 13.9.3, the descriptions of calculating the number of high levels are updated.

Issue 00B03 (2012-10-30)

This issue is the second draft release, which incorporates the following changes:

Chapter 3 System

In section 3.1, the descriptions of the POR module are added.

In section 3.4.5, the descriptions of PERIPHCTRL14 bit[16], PERIPHCTRL14 bit[17], PERIPHCTRL14 bit[20], PERIPHCTRL14 bit[21], and PERIPHCTRL15 bit[0] are updated.

In section 3.6.5.2, the descriptions of CHAN0_CFG bit[0] and CHAN0_CFG bit [1] are updated.

In section 3.9.6, RTC_SAR_CTRL bit[7:2] are reserved.

Chapter 5 ETH

In sections 5.1 and section 5.2, the descriptions of the RMII are added.

In Table 5-2, RMII signals are added and MII signals are updated.

In section 5.5, the registers UD_MAC_EEE_TIMER, UD_MAC_EEE_LINK_STATUS, and UD_MAC_EEE_CLK_CNT are added. The descriptions of UD_MAC_EEE_ENA bit[1], UD_MAC_EEE_ENA bit[31:4], and UD_MAC_EEE_INTEN bit[5:9] are added.

Chapter 10 Video Interfaces

In section 10.2.3.11, the descriptions of the VDAC non-load interrupt are added.

Chapter 11 ISP

Figure 11-1 is updated.

In section 11.2.2, the green equalization module is added.

Issue 00B02 (2012-09-20)

This issue is the first draft release.

Contents

Figures

Tables

1 Introduction

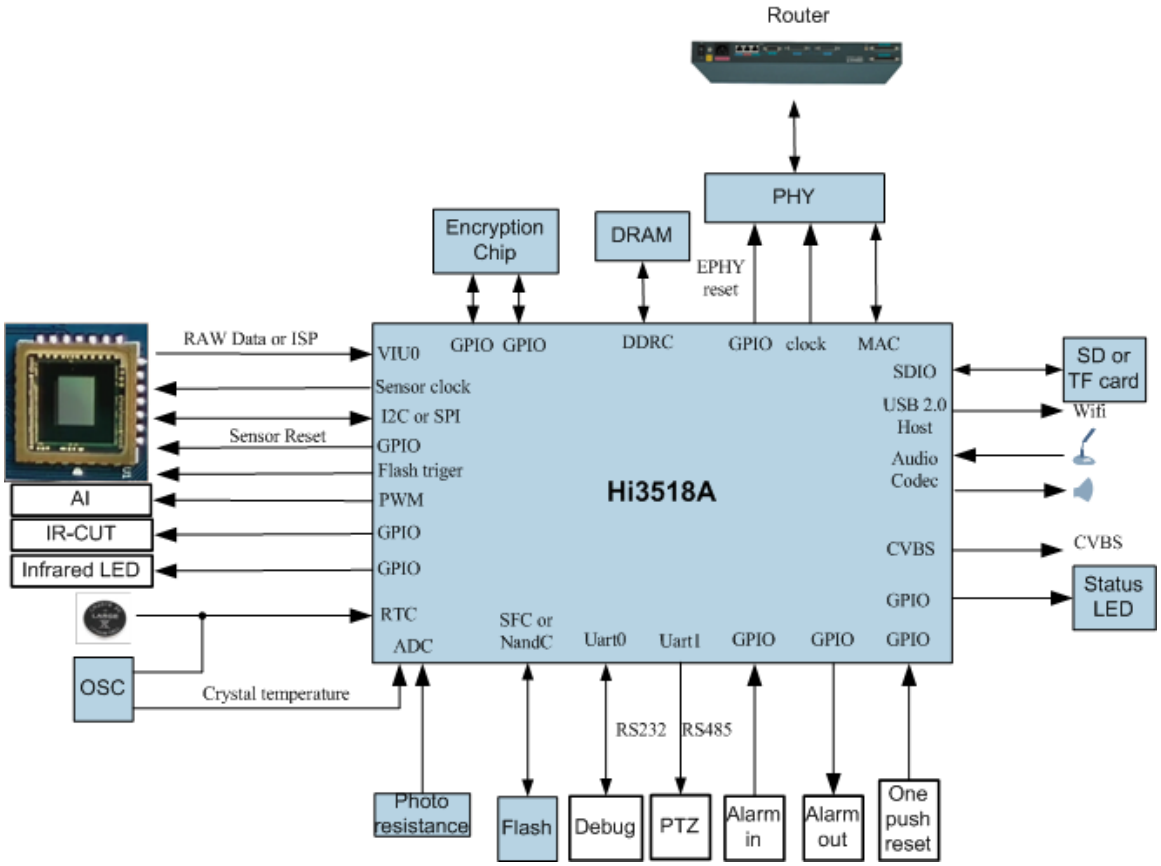
1.1 Application Scenarios

As a professional middle- and low-range system-on-chip (SoC), the Hi3518 is designed for the IP camera. Based on application requirements, the Hi3518 is classified into Hi3518A (for professional use) and Hi3518C (for consumer use). The Hi3518 encodes multiple streams in H.264 format at 720p@30 fps and provides superior image signal processing (ISP) performance, high encoded video quality, and a high-performance intelligent acceleration engine. With these features, the Hi3518 meets customers' requirements for product functions, performance, and image quality, and helps customers significantly reduce the engineering bill of materials (EBOM) costs. The following describes typical 720p IP camera solutions.

1.1.1 Hi3518A IP Camera Solution

Figure 1-1 shows the block diagram of the Hi3518A IP camera solution.

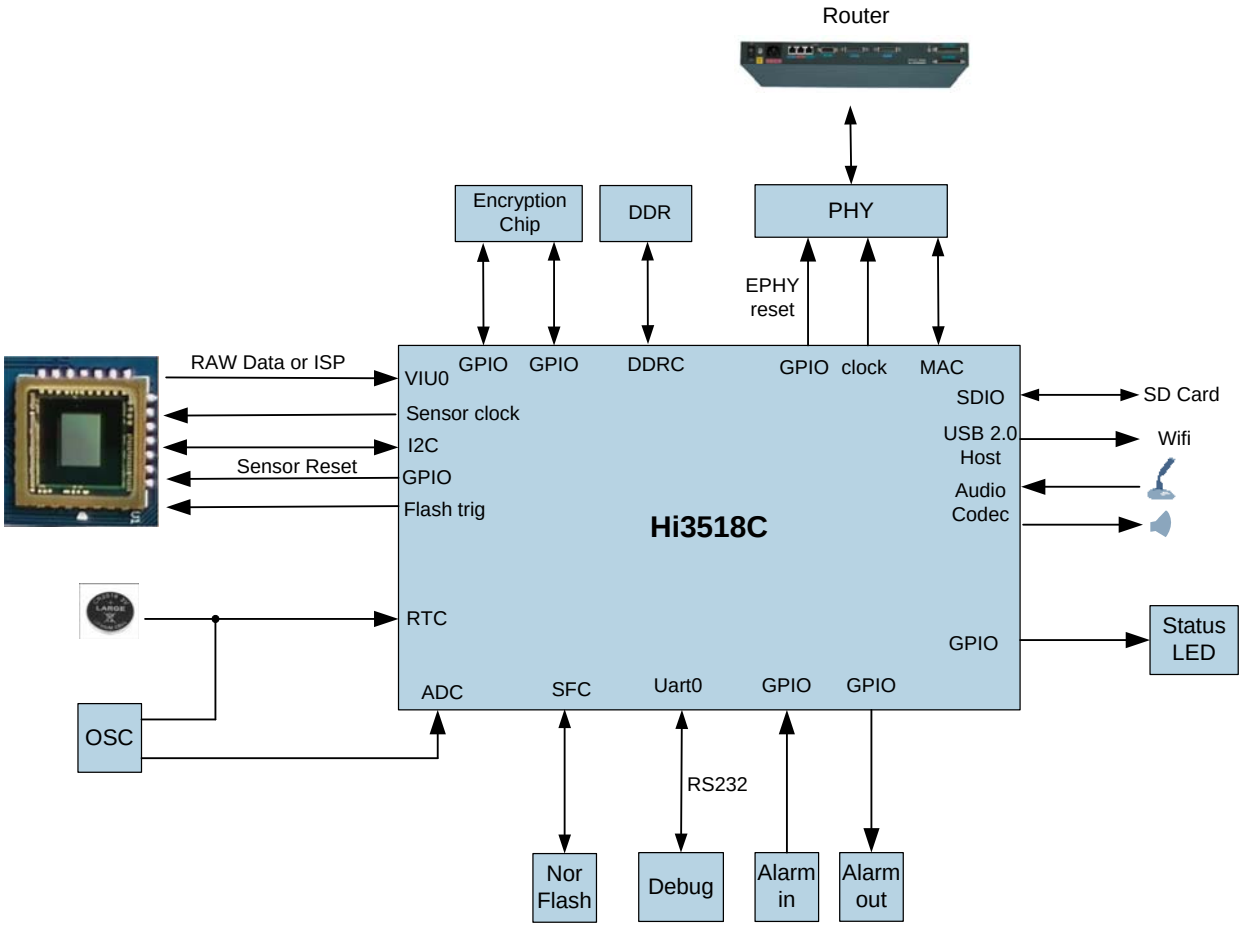
Figure 1-1 Block diagram of the Hi3518A IP camera solution



1.1.2 Hi3518C IP Camera Solution

Figure 1-2 shows the block diagram of the Hi3518C IP camera solution

Figure 1-2 Block diagram of the Hi3518C IP camera solution



1.2 Architecture

1.2.1 Overview

Figure 1-3 and Figure 1-4 show the logic block diagrams of the Hi3518A and Hi3518C respectively.

Figure 1-3 Logic block diagram of the Hi3518A

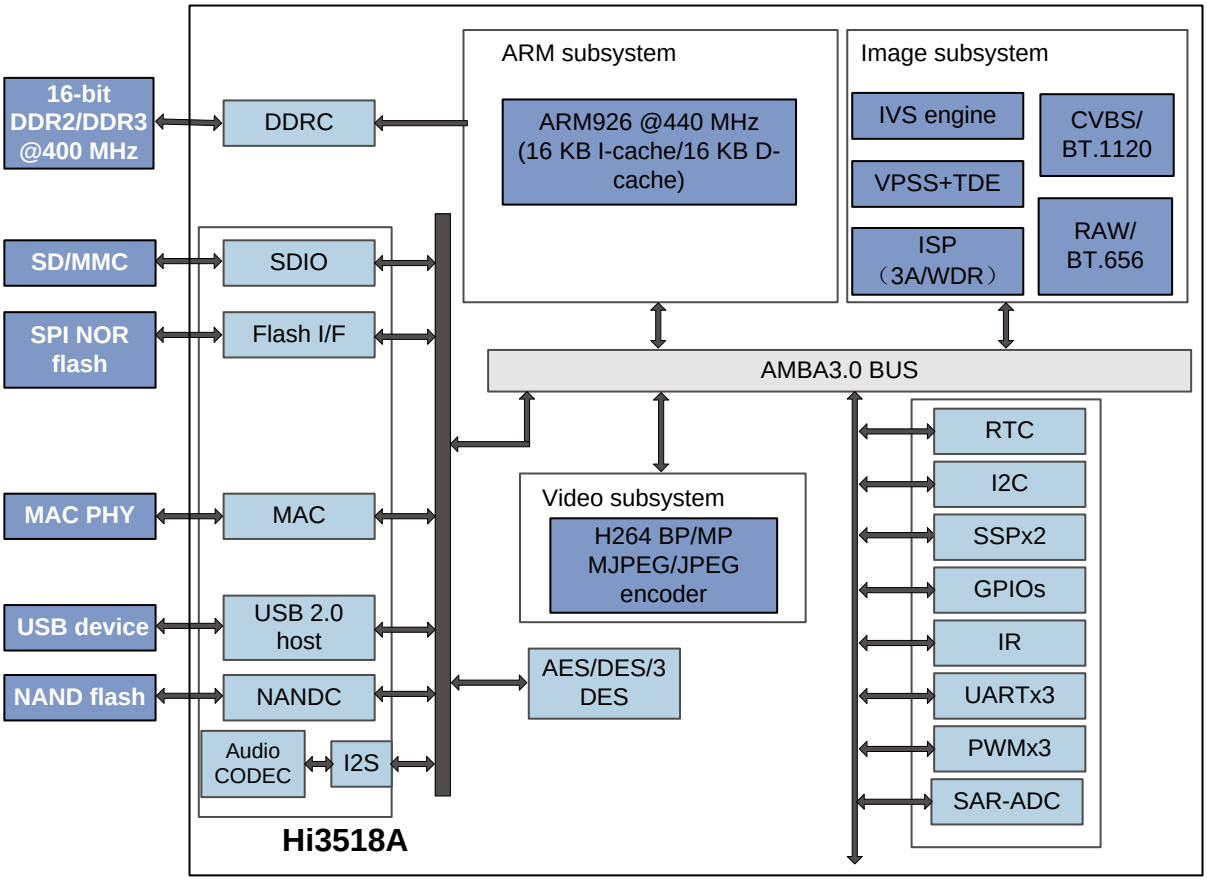
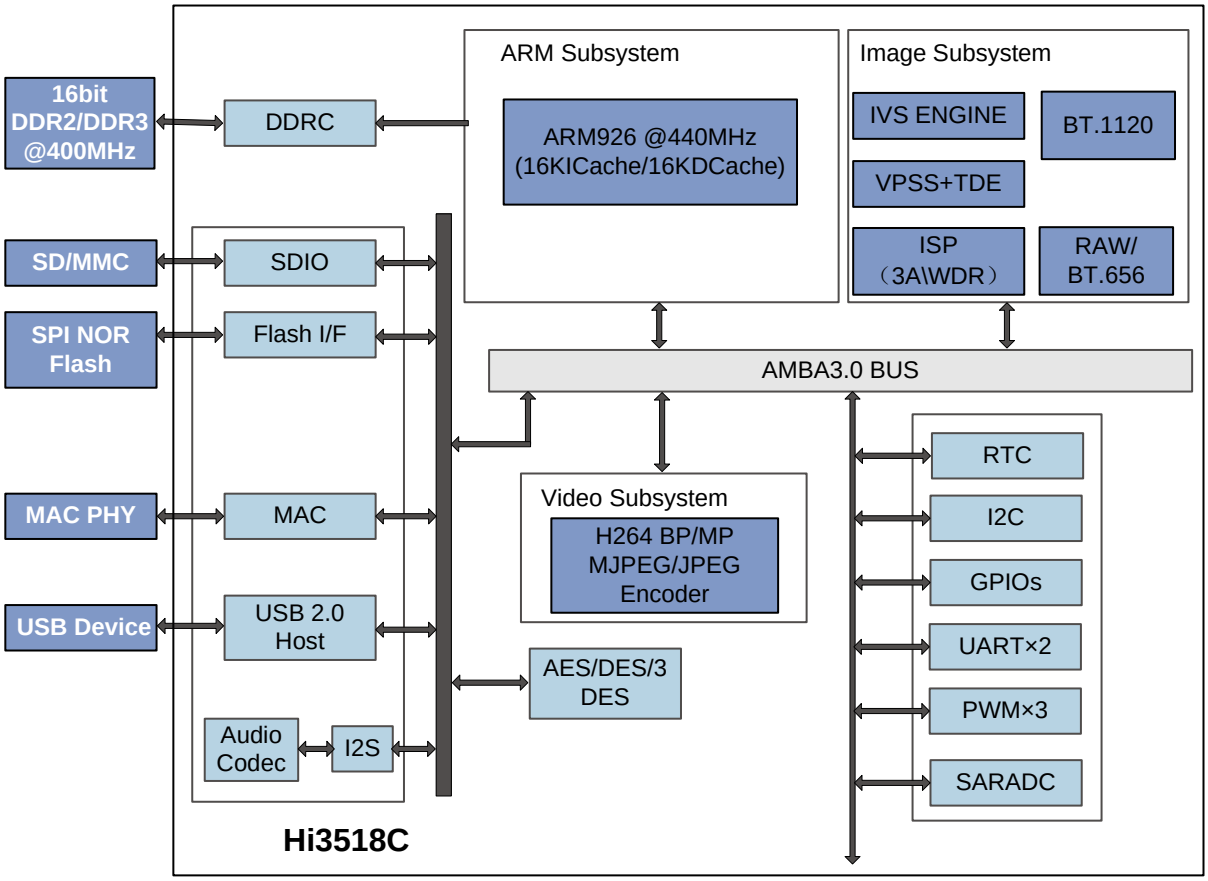


Figure 1-4 Logic block diagram of the Hi3518C



1.2.2 Processor Core

The Hi3518 processor core is an ARM core that provides a maximum of 440 MHz frequency and 16 KB instruction cache (I-cache) and 16 KB data cache (D-cache). 2K ITCM

1.2.3 Video Encoding Specifications

The following are supported encoding specifications:

- H.264 baseline profile encoding
- H.264 main profile encoding
- MJPEG/JPEG baseline encoding

1.2.4 Video Encoding

The following describes the video encoding performance:

- A maximum of 2-megapixel resolution for H.264 encoding
- For the Hi3518A, real-time encoding of H.264 and JPEG streams: 720p@30 fps+VGA@30 fps+QVGA@30 fps+720p@1fs JPEG snapshot. For the Hi3518C, real-time encoding of H.264 and JPEG streams: 720p@30fps+QVGA@30 fps+720p@1 fps JPEG snapshot
- JPEG snapshot at 720p@30 fps

- Supports constant bit rate (CBR) mode and variable bit rate (VBR) mode.
- Supports the output bit rate ranging from 32 kbit/s to 40 Mbit/s.
- Encoding frame rate ranging from 1/16 fps to 30 fps
- Encoding of eight regions of interest (ROIs)
- On-screen display (OSD) overlay of eight regions before encoding

1.2.5 Intelligent Video Engine

The integrated intelligent video engine (IVE) supports various intelligent analysis applications such as motion detection, boundary security, and video diagnosis.

1.2.6 Video and Graphic Processing

The following describes the video and graphic processing performance:

- Video pre-processing, including 3D denoising, image enhancement, edge enhancement, and de-interlacing
- Anti-flicker for output videos and graphics
- 1/8x to 8x video scaling
- 1/2x to 2x graphic scaling
- OSD overlay of eight regions before encoding
- Hardware graphics overlay post-processing for the videos at two layers (video layer and graphics layer 1)

1.2.7 ISP

The image signal processor (ISP) has the following features:

- Automatic exposure (AE), automatic white balance (AWB), and automatic focus (AF) for the Hi3518A, and AE and AWB for the Hi3518C. These features can be adjusted.
- Highlight compensation, backlight compensation, gamma correction, and color enhancement
- Defect pixel correction, denoising, and digital image stabilizer
- Anti-fog
- Lens distortion correction
- Image rotation by 90° or 270° (not supported by the Hi3518C)
- Mirror and flip
- Digital wide dynamic range (WDR) and tone mapping
- ISP tuning tools on the PC

1.2.8 Audio Encoding and Decoding

The following describes the audio encoding and decoding performance:

- Software decoding complying with multiple protocols
- G.711, ADPCM, and G.726 hardware encoding
- Echo cancellation

1.2.9 Security Engine

Advanced encryption standard (AES), data encryption standard (DES), and triple data encryption standard (3DES) algorithms

1.2.10 Video Interfaces

The following describes video input (VI) and video output (VO) interfaces:

- VI interfaces
  - 8-, 10-, or 12-bit RGB bayer inputs, a maximum of 74.25 MHz clock frequency
  - BT.1120 and BT.656
  - Connected to mainstream high-definition (HD) complementary metal-oxide semiconductors (CMOS) sensors provided by SONY, Aptina, OmniVision, and Panasonic
  - Connected to charge coupled device (CCD) sensors
  - Various sensor levels
  - Programmable sensor clock output
  - At most 2-megapixel input resolution
- VO interfaces
  - One composite video broadcast signal (CVBS) output for automatic load detection (not supported by the Hi3518C)
  - One BT.1120 VO interface for connecting to an external high-definition multimedia interface (HDMI) or serial digital interface (SDI), a maximum of 1080p@30 fps

1.2.11 Audio Interface

The integrated audio CODEC supports 16-bit voice inputs and outputs.

1.2.12 Ethernet Port

The Hi3518 provides one media access control (MAC) port. It has the following features:

- Reduced media independent interface (RGMII) or media independent interface (MII) mode
- 10/100 Mbit/s full-duplex or half-duplex mode
- Physical (PHY) clock output

1.2.13 Peripheral Interfaces

The following describes peripheral interfaces:

- Power-on-reset (POR)
- One high-precision real-time clock (RTC)
- One dual-channel analog-to-digital converter (ADC)
- Three universal asynchronous receiver transmitter (UART) interfaces for the Hi3518A and two UART interfaces for the Hi3518C
- Two serial peripheral interfaces (not supported by the Hi3518C)
- One infrared (IR) interface (not supported by the Hi3518C), one inter-integrated circuit (I^2C) interface, and general-purpose input/output (GPIO) interfaces

- Three pulse-width modulation (PWM) interfaces
- One secure digital input/output 2.0 (SDIO 2.0) interface, supporting secure digital high capacity (SDHC)
- One universal serial bus 2.0 (USB 2.0) host port

1.2.14 Memory Interfaces

The following describes memory interfaces:

- One 16-bit double-data rate 2 (DDR2) or DDR3 synchronous dynamic random access memory (SDRAM) controller interface
  - A maximum of 400 MHz frequency
  - A maximum of 256 MB capacity (128 MB for the Hi3518C)
- SPI NOR flash interface
  - 1-, 2-, or 4-bit SPI NOR flash
  - One chip select (CS)
- NAND flash interface (not supported by the Hi3518C)
  - 8-bit data width
  - Single-level cell SLC or multi-level cell (MLC)
  - 1-, 4-, or 24-bit error checking and correcting (ECC) mode
  - Components with 8 GB capacity or larger

1.2.15 Configurable Boot Modes

The Hi3518A can boot from the SPI NOR flash or NAND flash, whereas the Hi3518C can boot only from the SPI NOR flash.

1.2.16 SDK

The following describes the software development kit (SDK):

- Linux -3.0.y-based SDK
- High-performance H.264 PC decoding library

1.2.17 Physical Specifications

The following describes physical specifications:

- Power consumption
  - Typical power consumption of 700 mW
  - Multi-level power-saving control
- Operating voltages
  - 1.2 V core voltage
  - 3.3 V I/O voltage, and 3.8 V margin voltage
  - 1.5 V or 1.8 V DDR2/DDR3 SDRAM interface voltage
- Package

  Hi3518A
  - Compliance with restriction of the use of certain hazardous substances (RoHS), thin profile ball grid array 293 (FCBGA293)

- Ball pitch: 0.65 mm (0.03 in.)
- Body size: 13 mm x 13 mm x 1.37 mm (0.51 in. x 0.51 in. x 0.05 in.)

Hi3518C

- Compliance with RoHS, expose pad (Epad) quad flat package (QFP)
- Ball pitch: 0.4 mm (0.02 in.)
- Body size: 20 mm x 20 mm x 1.0 mm (0.79 in. x 0.79 in. x 0.04 in.)

1.3 Boot Modes

The Hi3518 supports the following boot modes:

- Booting from an external NAND flash (supported only by the Hi3518A)
- Booting from an external SPI NOR flash

1.3.1 Booting from the NAND Flash

When the Hi3518 boots from the NAND flash, the external memory is a NAND flash. To enable the Hi3518 to boot from the NAND flash mounted on the NANF flash controller (NANDC) interface, set the external pin BOOT_SEL (multiplexed with the external pin MDCK) to 1.

1.3.2 Booting from the SPI NOR Flash

When the Hi3518 boots from the SPI NOR flash, the external memory is an SPI NOR flash. To enable the Hi3518 to boot from the SPI NOR flash mounted on the SPI flash controller (SFC) interface, set the external pin BOOT_SEL (multiplexed with the external pin MDCK) to 0.

1.3.3 Address Space Mapping

Table 1-1 describes the address space mapping.

Table 1-1 Address space mapping

Start Address	End Address	Function	Capacity	Remarks
0xA000_0000	0xFFFF_FFFF	Reserved	None	None
0x8000_0000	0x8FFF_FFFF	Address space for connecting the DDR to an external DDR	256 MB	None
0x5C00_0000	0x7FFF_FFFF	Reserved	None	None
0x5800_0000	0x5BFF_FFFF	Storage space of the SPI flash	64 MB	None
0x5400_0000	0x57FF_FFFF	Reserved	None	None

Start Address	End Address	Function	Capacity	Remarks
0x5000_0000	0x53FF_FFFF	Storage space of the NAND flash	64 MB	This space is available for the Hi3518A and is reserved for the Hi3518C.
0x206E_0000	0x4FFF_FFFF	Reserved	None	None
0x206D_0000	0x206D_FFFF	DDR test module	64 KB	None
0x206C_0000	0x206C_FFFF	Motion detection (MD) register	64 KB	None
0x2067_0000	0x206B_FFFF	Reserved	None	None
0x2066_0000	0x2066_FFFF	JPEG encoder (JPGE) register	64 KB	None
0x2063_0000	0x2065_FFFF	Reserved	None	None
0x2062_0000	0x2062_FFFF	Video encoding (VENC) register	64 KB	None
0x2061_0000	0x2061_FFFF	Two-dimensional engine (TDE) register	64 KB	None
0x2060_0000	0x2060_FFFF	Video process subsystem (VPSS) register	64 KB	None
0x205F_0000	0x205F_FFFF	Reserved	None	None
0x205E_0000	0x205E_FFFF	IVE register	64 KB	None
0x205D_0000	0x205D_FFFF	Reserved	None	None
0x205C_0000	0x205C_FFFF	Video display (VDP) register	64 KB	None
0x2058_0000	0x205B_FFFF	Video capture (VICAP) register	256 KB	None
0x2020_0000	0x2057_FFFF	Reserved	None	None
0x201F_0000	0x201F_FFFF	GPIO11 register	64 KB	None
0x201E_0000	0x201E_FFFF	GPIO10 register	64 KB	None
0x201D_0000	0x201D_FFFF	GPIO9 register	64 KB	None
0x201C_0000	0x201C_FFFF	GPIO8 register	64 KB	None
0x201B_0000	0x201B_FFFF	GPIO7 register	64 KB	None
0x201A_0000	0x201A_FFFF	GPIO6 register	64 KB	None
0x2019_0000	0x2019_FFFF	GPIO5 register	64 KB	None
0x2018_0000	0x2018_FFFF	GPIO4 register	64 KB	None

Start Address	End Address	Function	Capacity	Remarks
0x2017_0000	0x2017_FFFF	GPIO3 register	64 KB	None
0x2016_0000	0x2016_FFFF	GPIO2 register	64 KB	None
0x2015_0000	0x2015_FFFF	GPIO1 register	64 KB	None
0x2014_0000	0x2014_FFFF	GPIO0 register	64 KB	None
0x2013_0000	0x2013_FFFF	PWM0/1 register	64 KB	None
0x2012_0000	0x2012_FFFF	DDR_PHY register	64 KB	None
0x2011_0000	0x2011_FFFF	DDRC register	64 KB	None
0x2010_0000	0x2010_FFFF	Reserved	64 KB	None
0x200F_0000	0x200F_FFFF	IO configuration register	64 KB	None
0x200E_0000	0x200E_FFFF	SPI1 register	64 KB	This space is available for the Hi3518A and is reserved for the Hi3518C.
0x200D_0000	0x200D_FFFF	I^2C register	64 KB	None
0x200C_0000	0x200C_FFFF	SPI0 register	64 KB	This space is available for the Hi3518A and is reserved for the Hi3518C.
0x200B_0000	0x200B_FFFF	Successive approximation (SAR) ADC register	64 KB	None
0x200A_0000	0x200A_FFFF	UART2 register	64 KB	This space is available for the Hi3518A and is reserved for the Hi3518C.
0x2009_0000	0x2009_FFFF	UART1 register	64 KB	None
0x2008_0000	0x2008_FFFF	UART0 register	64 KB	None
0x2007_0000	0x2007_FFFF	IR register	64 KB	None
0x2006_0000	0x2006_FFFF	RTC register	64 KB	None
0x2005_0000	0x2005_FFFF	SYS_CTRL register	64 KB	None
0x2004_0000	0x2004_FFFF	WDG register	64 KB	None
0x2003_0000	0x2003_FFFF	CRG register	64 KB	None
0x2002_0000	0x2002_FFFF	Reserved	64 KB	None
0x2001_0000	0x2001_FFFF	Timer2/3 register	64 KB	None
0x2000_0000	0x2000_FFFF	Timer0/1 register	64 KB	None
0x1015_0000	0x1FFF_FFFF	Reserved	None	None

Start Address	End Address	Function	Capacity	Remarks
0x1014_0000	0x1014_FFFF	Vector interrupt controller (VIC) register	64 KB	None
0x100E_0000	0x1013_FFFF	Reserved	None	None
0x100D_0000	0x100D_FFFF	Direct memory access control (DMAC) register	64 KB	None
0x100C_0000	0x100C_FFFF	CIPHER register	64 KB	None
0x100B_0000	0x100B_FFFF	USB enhanced host controller interface (EHCI) register	64 KB	None
0x100A_0000	0x100A_FFFF	USB open host controller interface (OHCI) register	64 KB	None
0x1009_0000	0x1009_FFFF	Ethernet (ETH) register	64 KB	None
0x1005_0000	0x1008_FFFF	Reserved	None	None
0x1004_0000	0x1004_FFFF	Sonic input/output (SIO) register	64 KB	None
0x1003_0000	0x1003_FFFF	Reserved	None	None
0x1002_0000	0x1002_FFFF	SDIO register	64 KB	None
0x1001_0000	0x1001_FFFF	SPI NOR flash register	64 KB	None
0x1000_0000	0x1000_FFFF	NAND flash register	64 KB	This space is available for the Hi3518A and is reserved for the Hi3518C.
0x0400_0000	0x0FFF_FFFF	Reserved	None	None
0x0000_0000	0x03FF_FFFF	During address remapping, the address space points to the boot address space. When address remapping is cleared, the address space points to the tightly-coupled memory (TCM).	64 MB	The boot address space varies according to the setting of the BOOT_SEL. 0: The boot address space is the storage space of the SPI NOR flash. 1: The boot address space is the storage space of the NAND flash (supported only by the Hi3518A).

Contents

Figures

Tables

2 Hardware

2.1 Package and Pinout

2.1.1 Package

The Hi3518A uses the package of thin profile ball grid array (TFBGA). It has 293 pins, its body size is 13 mm x 13 mm x 1.37 mm (0.51 in. x 0.51 in. x 0.05 in.), and its ball pitch is 0.65 mm (0.03 in.). Figure 2-1 to Figure 2-4 show the package of the Hi3518A. Table 2-1 lists the package dimensions of the Hi3518A.

Figure 2-1 Top view

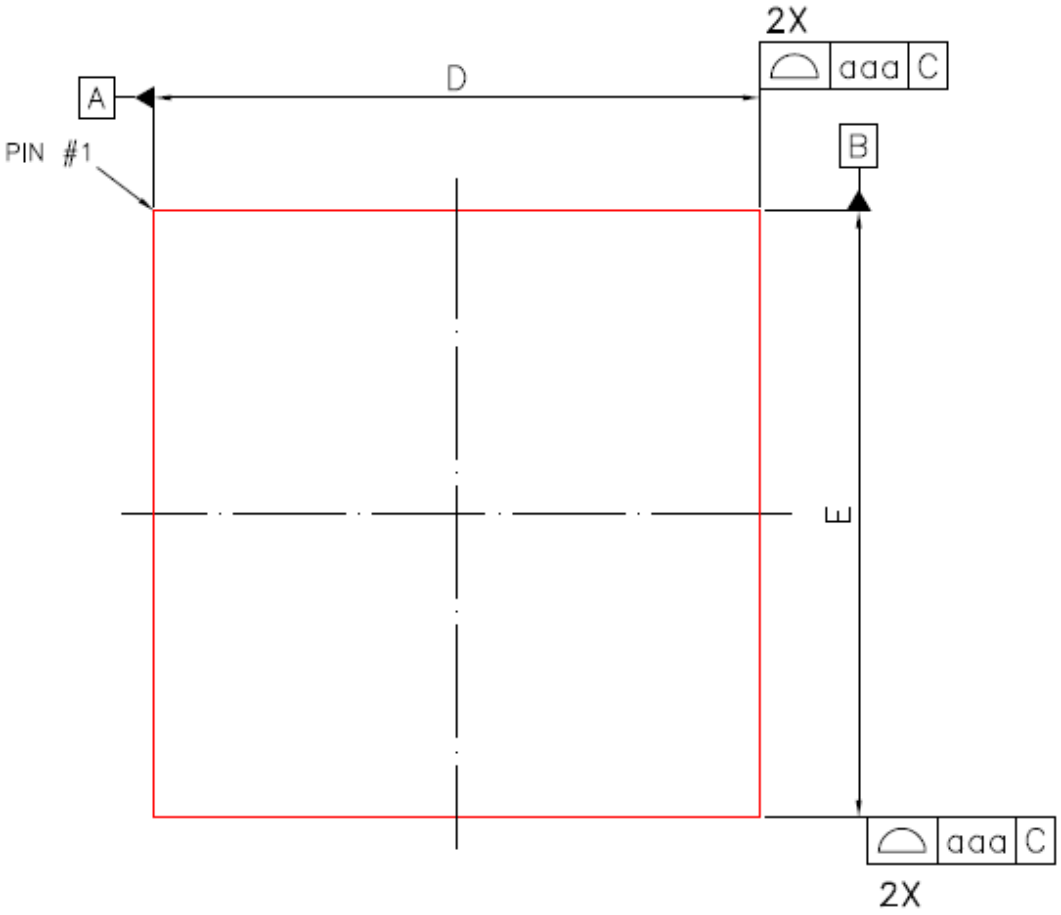


Figure 2-2 Bottom view

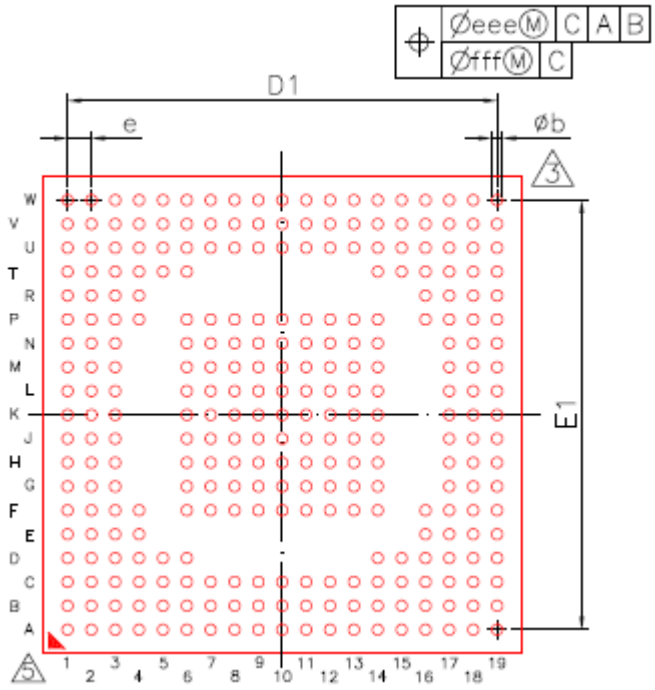


Figure 2-3 Side view

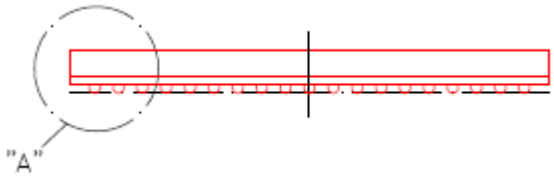


Figure 2-4 Enlarged view of detail "A"

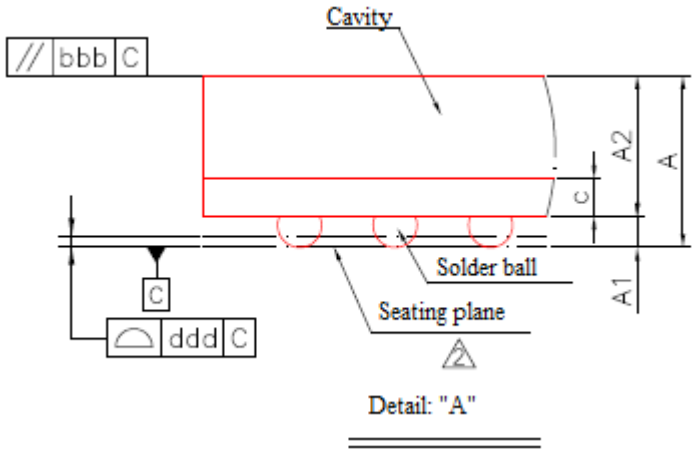


Table 2-1 Package dimensions

Parameter	Dimensions (mm)		
	Min	Typ	Max
A	None	None	1.37
A1	0.16	0.21	0.26
A2	0.91	0.96	1.01
c	0.22	0.26	0.30
D	12.90	13.00	13.10
E	12.90	13.00	13.10
D1	None	11.70	None
E1	None	11.70	None
e	None	0.65	None
b	0.25	0.30	0.35
aaa	0.15		
ccc	0.10		
ddd	0.08		
eee	0.15		
fff	0.08		
MD/ME	19/19		

2.1.2 Pinout

Table 2-2 lists the number of each type of pins on the Hi3518A.

Table 2-2 Hi3518A pins

Pin Type	Quantity
Input/Output (I/O)	172
Digital power	31
Digital ground (GND)	71
Others/Analog power	9
Others/Analog GND	7
Double-data rate (DDR) reference power	3

Pin Type	Quantity
Total	293

Pin Maps

Figure 2-5 to Figure 2-8 show pin maps.

Figure 2-5 Pin map part 1 (A1–K10)

	1	2	3	4	5	6	7	8	9	10
A	DVSS	DDR_A1	DDR_A11	DDR_DQ6	DDR_DQ5	DDR_DQS0_P	DDR_DQ2	DDR_DQ3	DDR_DQ14	DDR_DQ12
B	DDR_CLK0_P	DDR_CLK0_N	DDR_A8	DDR_CKE	DDR_DQ7	DDR_DQS0_N	DDR_DM0	DDR_DQ1	DDR_DQ8	DDR_DQ10
C	DVSS	DVSS	DDR_A10	DDR_A4	DDR_DQ4	DVSS	DDR_VDDQ	DDR_DQ0	DVSS	DDR_VREF1
D	DDR_BA2	DDR_RAS_N	DDR_ZQ	DDR_A6	DVSS	DDR_VREF0				
E	DDR_A12	DDR_WE_N	DDR_BA1	DVSS						
F	DDR_A2	DDR_A0	DDR_CAS_N	DDR_VDDQ		DVDD12	DVDD12	DVDD12	DDR_VDDQ	DDR_VDDQ
G	DDR_A9	DDR_A3	DDR_ODT			DDR_VREF2	DVSS	DVSS	DVSS	DVSS
H	DDR_A13	DDR_A5	DDR_BA0			DDR_VDDQ	DVSS	DVSS	DVSS	DVSS
J	DDR_CS_N	DDR_RESET_N	DDR_A7			DVDD12	DVSS	DVSS	DVSS	DVSS
K	NF_DQ1	DVSS	NF_DQ0			DVDD12	DVSS	DVSS	DVSS	DVSS

Figure 2-6 Pin map part 2 (A1–K19)

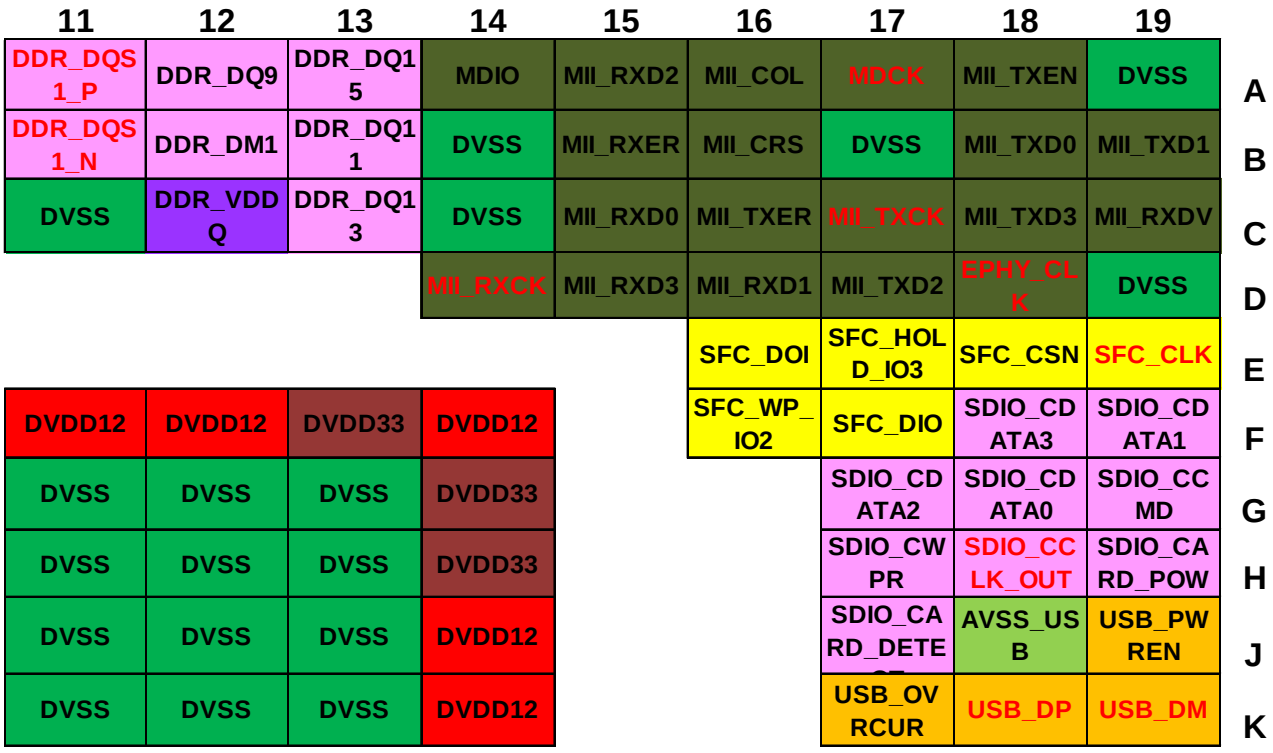


Figure 2-7 Pin map part 3 (L1–W10)

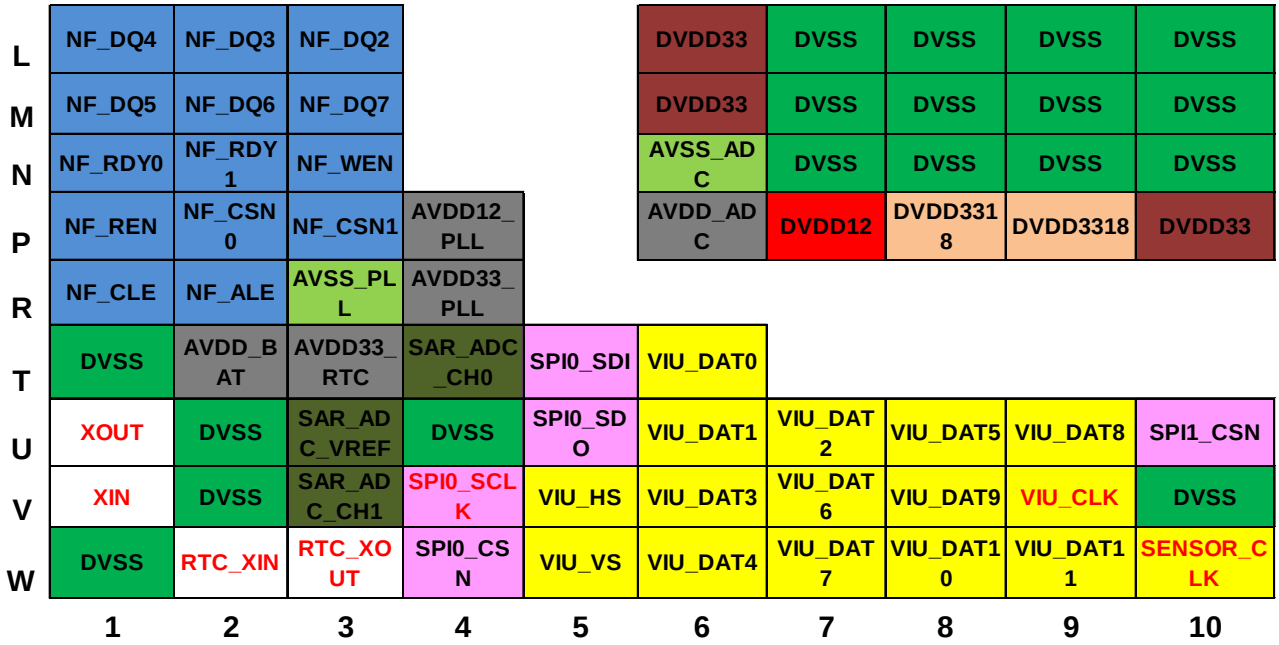
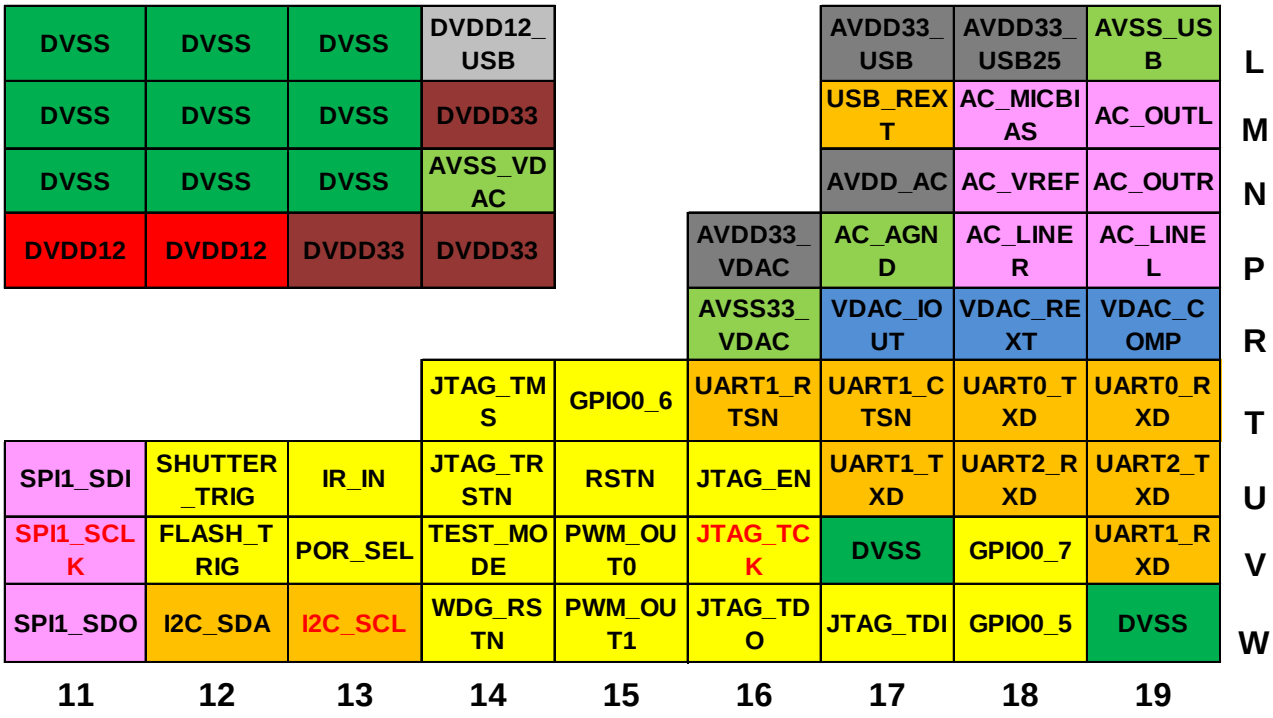


Figure 2-8 Pin map part 4 (L11–W19)



Pin Arrangement

Table 2-3 lists the Hi3518A pins in sequence.

Table 2-3 Hi3518A pins

Pin Position	Name	Pin Position	Name
A1	DVSS	K11	DVSS
A2	DDR_A1	K12	DVSS
A3	DDR_A11	K13	DVSS
A4	DDR_DQ6	K14	DVDD12
A5	DDR_DQ5	K17	USB_OVRCUR
A6	DDR_DQS0_P	K18	USB_DP
A7	DDR_DQ2	K19	USB_DM
A8	DDR_DQ3	L1	NF_DQ4
A9	DDR_DQ14	L2	NF_DQ3
A10	DDR_DQ12	L3	NF_DQ2
A11	DDR_DQS1_P	L6	DVDD33

Pin Position	Name	Pin Position	Name
A12	DDR_DQ9	L7	DVSS
A13	DDR_DQ15	L8	DVSS
A14	MDIO	L9	DVSS
A15	MII_RXD2	L10	DVSS
A16	MII_COL	L11	DVSS
A17	MDCK	L12	DVSS
A18	MII_TXEN	L13	DVSS
A19	DVSS	L14	DVDD12_USB
B1	DDR_CLK0_P	L17	AVDD33_USB
B2	DDR_CLK0_N	L18	AVDD33_USB25
B3	DDR_A8	L19	AVSS_USB
B4	DDR_CKE	M1	NF_DQ5
B5	DDR_DQ7	M2	NF_DQ6
B6	DDR_DQS0_N	M3	NF_DQ7
B7	DDR_DM0	M6	DVDD33
B8	DDR_DQ1	M7	DVSS
B9	DDR_DQ8	M8	DVSS
B10	DDR_DQ10	M9	DVSS
B11	DDR_DQS1_N	M10	DVSS
B12	DDR_DM1	M11	DVSS
B13	DDR_DQ11	M12	DVSS
B14	DVSS	M13	DVSS
B15	MII_RXER	M14	DVDD33
B16	MII_CRS	M17	USB_REXT
B17	DVSS	M18	AC_MICBIAS
B18	MII_TXD0	M19	AC_OUTL
B19	MII_TXD1	N1	NF_RDY0
C1	DVSS	N2	NF_RDY1
C2	DVSS	N3	NF_WEN
C3	DDR_A10	N6	AVSS_ADC

Pin Position	Name	Pin Position	Name
C4	DDR_A4	N7	DVSS
C5	DDR_DQ4	N8	DVSS
C6	DVSS	N9	DVSS
C7	DDR_VDDQ	N10	DVSS
C8	DDR_DQ0	N11	DVSS
C9	DVSS	N12	DVSS
C10	DDR_VREF1	N13	DVSS
C11	DVSS	N14	AVSS_VDAC
C12	DDR_VDDQ	N17	AVDD_AC
C13	DDR_DQ13	N18	AC_VREF
C14	DVSS	N19	AC_OUTR
C15	MII_RXD0	P1	NF_REN
C16	MII_TXER	P2	NF_CSN0
C17	MII_TXCK	P3	NF_CSN1
C18	MII_TXD3	P4	AVDD12_PLL
C19	MII_RXDV	P6	AVDD_ADC
D1	DDR_BA2	P7	DVDD12
D2	DDR_RAS_N	P8	DVDD3318
D3	DDR_ZQ	P9	DVDD3318
D4	DDR_A6	P10	DVDD33
D5	DVSS	P11	DVDD12
D6	DDR_VREF0	P12	DVDD12
D14	MII_RXCK	P13	DVDD33
D15	MII_RXD3	P14	DVDD33
D16	MII_RXD1	P16	AVDD33_VDAC
D17	MII_TXD2	P17	AC_AGND
D18	EPHY_CLK	P18	AC_LINER
D19	DVSS	P19	AC_LINEL
E1	DDR_A12	R1	NF_CLE
E2	DDR_WE_N	R2	NF_ALE

Pin Position	Name	Pin Position	Name
E3	DDR_BA1	R3	AVSS_PLL
E4	DVSS	R4	AVDD33_PLL
E16	SFC_DOI	R16	AVSS33_VDAC
E17	SFC_HOLD_IO3	R17	VDAC_IOUT
E18	SFC_CSN	R18	VDAC_REXT
E19	SFC_CLK	R19	VDAC_COMP
F1	DDR_A2	T1	DVSS
F2	DDR_A0	T2	AVDD_BAT
F3	DDR_CAS_N	T3	AVDD33_RTC
F4	DDR_VDDQ	T4	SAR_ADC_CH0
F6	DVDD12	T5	SPI0_SDI
F7	DVDD12	T6	VIU_DAT0
F8	DVDD12	T14	JTAG_TMS
F9	DDR_VDDQ	T15	GPIO0_6
F10	DDR_VDDQ	T16	UART1_RTSN
F11	DVDD12	T17	UART1_CTSN
F12	DVDD12	T18	UART0_TXD
F13	DVDD33	T19	UART0_RXD
F14	DVDD12	U1	XOUT
F16	SFC_WP_IO2	U2	DVSS
F17	SFC_DIO	U3	SAR_ADC_VREF
F18	SDIO_CDATA3	U4	DVSS
F19	SDIO_CDATA1	U5	SPI0_SDO
G1	DDR_A9	U6	VIU_DAT1
G2	DDR_A3	U7	VIU_DAT2
G3	DDR_ODT	U8	VIU_DAT5
G6	DDR_VREF2	U9	VIU_DAT8
G7	DVSS	U10	SPI1_CSN
G8	DVSS	U11	SPI1_SDI
G9	DVSS	U12	SHUTTER_TRIG

Pin Position	Name	Pin Position	Name
G10	DVSS	U13	IR_IN
G11	DVSS	U14	JTAG_TRSTN
G12	DVSS	U15	RSTN
G13	DVSS	U16	JTAG_EN
G14	DVDD33	U17	UART1_TXD
G17	SDIO_CDATA2	U18	UART2_RXD
G18	SDIO_CDATA0	U19	UART2_TXD
G19	SDIO_CCMD	V1	XIN
H1	DDR_A13	V2	DVSS
H2	DDR_A5	V3	SAR_ADC_CH1
H3	DDR_BA0	V4	SPI0_SCLK
H6	DDR_VDDQ	V5	VIU_HS
H7	DVSS	V6	VIU_DAT3
H8	DVSS	V7	VIU_DAT6
H9	DVSS	V8	VIU_DAT9
H10	DVSS	V9	VIU_CLK
H11	DVSS	V10	DVSS
H12	DVSS	V11	SPI1_SCLK
H13	DVSS	V12	FLASH_TRIG
H14	DVDD33	V13	POR_SEL
H17	SDIO_CWPR	V14	TEST_MODE
H18	SDIO_CCLK_OUT	V15	PWM_OUT0
H19	SDIO_CARD_POWER_EN	V16	JTAG_TCK
J1	DDR_CS_N	V17	DVSS
J2	DDR_RESET_N	V18	GPIO0_7
J3	DDR_A7	V19	UART1_RXD
J6	DVDD12	W1	DVSS
J7	DVSS	W2	RTC_XIN
J8	DVSS	W3	RTC_XOUT
J9	DVSS	W4	SPI0_CSN

Pin Position	Name	Pin Position	Name
J10	DVSS	W5	VIU_VS
J11	DVSS	W6	VIU_DAT4
J12	DVSS	W7	VIU_DAT7
J13	DVSS	W8	VIU_DAT10
J14	DVDD12	W9	VIU_DAT11
J17	SDIO_CARD_DETECT	W10	SENSOR_CLK
J18	AVSS_USB	W11	SPI1_SDO
J19	USB_PWREN	W12	I2C_SDA
K1	NF_DQ1	W13	I2C_SCL
K2	DVSS	W14	WDG_RSTN
K3	NF_DQ0	W15	PWM_OUT1
K6	DVDD12	W16	JTAG_TDO
K7	DVSS	W17	JTAG_TDI
K8	DVSS	W18	GPIO0_5
K9	DVSS	W19	DVSS
K10	DVSS		

2.2 Pin Descriptions

2.2.1 Pin Types

Table 2-4 describes the input/output (I/O) pin types.

Table 2-4 I/O pin types

I/O Type	Description
I	Input signal
I_{PD}	Input signal, internal pull-down
I_{PU}	Input signal, internal pull-up
I_S	Input signal with Schmitt trigger
I_{SPD}	Input signal with Schmitt trigger, internal pull-down
I_{SPU}	Input signal with Schmitt trigger, internal pull-up

I/O Type	Description
O	Output signal
O_{OD}	Output open drain (OD)
I/O	Bidirectional (input/output) signal
I_{PD}/O	Bidirectional signal, input pull-down
I_{PU}/O	Bidirectional signal, input pull-up
I_{SPU}/O	Bidirectional signal with Schmitt trigger, input pull-up
I_{PD}/O_{OD}	Bidirectional signal, input pull-down and output OD
I_{PU}/O_{OD}	Bidirectional signal, input pull-up and output OD
I_S/O	Bidirectional signal, input with Schmitt trigger
I_S/O_{OD}	Bidirectional signal, input with Schmitt trigger and output OD
CIN	Crystal oscillator input
COUT	Crystal oscillator output
P	Power supply
G	Ground (GND)

2.2.2 Pin Details

SYS Pins

Table 2-5 describes system (SYS) pins.

Table 2-5 SYS pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
V1	XIN	I	None	3.3	Crystal input
U1	XOUT	O	None	3.3	Crystal output
W14	WDG_RSTN	O_{OD}	4	3.3	Watchdog reset, active low, and OD output
V13	POR_SEL	I_{SPD}	None	3.3	Reset select. 0: reset during internal POR power-on 1: reset by using the external rest pin
U15	RSTN	I_{SPU}	None	3.3	System power-on reset input, active low

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
V14	TEST_MODE	I_{SPD}	None	3.3	Mode select. 0: functional mode 1: test mode

JTAG Pins

Table 2-6 describes Joint Test Action Group (JTAG) pins.

Table 2-6 JTAG pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
U16	JTAG_EN	I_{PD}	None	3.3	JTAG pin enable. 0: disabled 1: enabled
V16	JTAG_TCK	I_{PD}/O	4	3.3	**Function 0: GPIO0_1** General-purpose input/output (GPIO) **Function 1: JTAG_TCK** JTAG clock input **Function 2: TEMPER_DQ** Temperature measurement. It is used to communicate with the external temperature measurement chip.
W17	JTAG_TDI	I_{PU}/O	4	3.3	**Function 0: GPIO0_4** GPIO **Function 1: JTAG_TDI** JTAG data input **Function 2: TEMPER_DQ** Temperature measurement. It is used to communicate with the external temperature measurement chip.
W16	JTAG_TDO	I_{PD}/O	8	3.3	**Function 0: GPIO0_3** GPIO **Function 1: JTAG_TDO** JTAG data output **Function 2: TEMPER_DQ**

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					Temperature measurement. It is used to communicate with the external temperature measurement chip.
T14	JTAG_TMS	I_{PU}/O	4	3.3	**Function 0: GPIO0_2** GPIO **Function 1: JTAG_TMS** JTAG mode select input **Function 2: TEMPER_DQ** Temperature measurement. It is used to communicate with the external temperature measurement chip.
U14	JTAG_TRSTN	I_{PD}/O	4	3.3	**Function 0: GPIO0_0** GPIO **Function 1: JTAG_TRSTN** JTAG reset input **Function 2: TEMPER_DQ** Temperature measurement. It is used to communicate with the external temperature measurement chip.

DDR Pins

Table 2-7 describes DDR power pins.

Table 2-7 DDR power pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
C7, C12, F4, F9, F10, H6	DDR_VDDQ	P	None	1.8/1.5	DDR I/O power
D6 C10 G6	DDR_VREF0 DDR_VREF1 DDR_VREF2	P	None	0.5 x DDR_VDDQ	DDR reference voltage

Table 2-8 describes DDR signal pins.

Table 2-8 DDR signal pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
F2	DDR_A0	O	None	1.8/1.5	Address signal 0 of the DDR synchronous dynamic random access memory (SDRAM)
A2	DDR_A1	O	None	1.8/1.5	Address signal 1 of the DDR SDRAM
F1	DDR_A2	O	None	1.8/1.5	Address signal 2 of the DDR SDRAM
G2	DDR_A3	O	None	1.8/1.5	Address signal 3 of the DDR SDRAM
C4	DDR_A4	O	None	1.8/1.5	Address signal 4 of the DDR SDRAM
H2	DDR_A5	O	None	1.8/1.5	Address signal 5 of the DDR SDRAM
D4	DDR_A6	O	None	1.8/1.5	Address signal 6 of the DDR SDRAM
J3	DDR_A7	O	None	1.8/1.5	Address signal 7 of the DDR SDRAM
B3	DDR_A8	O	None	1.8/1.5	Address signal 8 of the DDR SDRAM
G1	DDR_A9	O	None	1.8/1.5	Address signal 9 of the DDR SDRAM
C3	DDR_A10	O	None	1.8/1.5	Address signal 10 of the DDR SDRAM
A3	DDR_A11	O	None	1.8/1.5	Address signal 11 of the DDR SDRAM
E1	DDR_A12	O	None	1.8/1.5	Address signal 12 of the DDR SDRAM
H1	DDR_A13	O	None	1.8/1.5	Address signal 13 of the DDR SDRAM
H3	DDR_BA0	O	None	1.8/1.5	Bank address signal 0 of the DDR SDRAM
E3	DDR_BA1	O	None	1.8/1.5	Bank address signal 1 of the DDR SDRAM
D1	DDR_BA2	O	None	1.8/1.5	Bank address signal 2 of the DDR SDRAM
F3	DDR_CAS_N	O	None	1.8/1.5	Column address select of the DDR SDRAM

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
B4	DDR_CKE	O	None	1.8/1.5	DDR SDRAM clock enable
B2	DDR_CLK0_N	O	None	1.8/1.5	Negative differential clock 0 of the DDR SDRAM
B1	DDR_CLK0_P	O	None	1.8/1.5	Positive differential clock 0 of the DDR SDRAM
J1	DDR_CS_N	O	None	1.8/1.5	DDR SDRAM chip select (CS)
B7	DDR_DM0	I/O	None	1.8/1.5	Data mask signal 0 of the DDR SDRAM
B12	DDR_DM1	I/O	None	1.8/1.5	Data mask signal 1 of the DDR SDRAM
C8	DDR_DQ0	I/O	None	1.8/1.5	Data line 0 of the DDR SDRAM
B8	DDR_DQ1	I/O	None	1.8/1.5	Data line 1 of the DDR SDRAM
A7	DDR_DQ2	I/O	None	1.8/1.5	Data line 2 of the DDR SDRAM
A8	DDR_DQ3	I/O	None	1.8/1.5	Data line 3 of the DDR SDRAM
C5	DDR_DQ4	I/O	None	1.8/1.5	Data line 4 of the DDR SDRAM
A5	DDR_DQ5	I/O	None	1.8/1.5	Data line 5 of the DDR SDRAM
A4	DDR_DQ6	I/O	None	1.8/1.5	Data line 6 of the DDR SDRAM
B5	DDR_DQ7	I/O	None	1.8/1.5	Data line 7 of the DDR SDRAM
B9	DDR_DQ8	I/O	None	1.8/1.5	Data line8 of the DDR SDRAM
A12	DDR_DQ9	I/O	None	1.8/1.5	Data line 9 of the DDR SDRAM
B10	DDR_DQ10	I/O	None	1.8/1.5	Data line 10 of the DDR SDRAM
B13	DDR_DQ11	I/O	None	1.8/1.5	Data line 11 of the DDR SDRAM
A10	DDR_DQ12	I/O	None	1.8/1.5	Data line 12 of the DDR SDRAM
C13	DDR_DQ13	I/O	None	1.8/1.5	Data line 13 of the DDR SDRAM

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
A9	DDR_DQ14	I/O	None	1.8/1.5	Data line 14 of the DDR SDRAM
A13	DDR_DQ15	I/O	None	1.8/1.5	Data line 15 of the DDR SDRAM
B6	DDR_DQS0_N	I/O	None	1.8/1.5	Negative data strobe (DQS) signal 0 of the DDR, corresponding to DQ[7:0]
A6	DDR_DQS0_P	I/O	None	1.8/1.5	Positive DQS signal 0 of the DDR, corresponding to DQ[7:0]
B11	DDR_DQS1_N	I/O	None	1.8/1.5	Negative DQS signal 1 of the DDR, corresponding to DQ[15:8]
A11	DDR_DQS1_P	I/O	None	1.8/1.5	Positive DQS signal 1 of the DDR, corresponding to DQ[15:8]
G3	DDR_ODT	None	None	None	Connect to an external matched reference resistor
D2	DDR_RAS_N	O	None	1.8/1.5	Row address select of the DDR SDRAM
J2	DDR_RESET_N	O	None	1.8/1.5	Reset signal of the DDR3 SDRAM
E2	DDR_WE_N	O	None	1.8/1.5	DDR SDRAM write enable
D3	DDR_ZQ	None	None	None	Resistor interface on the matched impedance calibration circuit of the DDR23 Lite physical layer (PHY), for connecting to a 240 Ω external resistor

ETH Pin

Table 2-9 describes the EPHY_CLK pin.

Table 2-9 EPHY_CLK pin

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
D18	EPHY_CL	I/O	8	3.3	**Function 0: GPIO1_3**

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
	K				GPIO **Function 1: EPHY_CLK** Working clock of the media independent interface (MII) PHY **Function 2: VOU1120_DATA2** BT.1120 luminance signal output

Table 2-10 describes management data input/output (MDIO) pins.

Table 2-10 MDIO pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
A17	MDCK	I_{PD}/O	8	3.3	**Function 0: GPIO3_6** GPIO **Function 1: MDCK** MDIO clock output **Function 2: VOU1120_DATA6** BT.1120 luminance signal output **Function 3: BOOT_SEL** Storage medium select for booting. 0: storage space of the SPI flash 1: storage space of the NAND flash
A14	MDIO	I/O	8	3.3	**Function 0: GPIO3_7** GPIO **Function 1: MDIO** MDIO input/output **Function 2: VOU1120_DATA14** BT.1120 chrominance signal output

Table 2-11 describes MII pins.

Table 2-11 MII pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
A16	MII_COL	I/O	8	3.3	**Function 0: GPIO3_1**

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					GPIO **Function 1: MII_COL** MII collision indicator **Function 2: VOU1120_DATA9** BT.1120 chrominance signal output
B16	MII_CRS	I/O	8	3.3	**Function 0: GPIO3_0** GPIO **Function 1: MII_CRS** MII carrier sense signal **Function 2: VOU1120_DATA10** BT.1120 chrominance signal output
D14	MII_RXCK	I/O	12	3.3	**Function 0: GPIO3_2** GPIO **Function 1: MII_RXCK** MII receive (RX) clock **Function 2: VOU1120_CLK** BT.1120 clock output
C15	MII_RXD0	I/O	8	3.3	**Function 0: GPIO4_0** GPIO **Function 1: MII_RXD0** Reduced media independent interface (RMII) or MII RX data **Function 2: VOU1120_DATA12** BT.1120 chrominance signal output
D16	MII_RXD1	I/O	8	3.3	**Function 0: GPIO4_1** GPIO **Function 1: MII_RXD1** RMII or MII RX data **Function 2: VOU1120_DATA8** BT.1120 chrominance signal output
A15	MII_RXD2	I/O	8	3.3	**Function 0: GPIO4_2** GPIO **Function 1: MII_RXD2** MII RX data **Function 2: VOU1120_DATA11** BT.1120 chrominance signal output
D15	MII_RXD3	I/O	8	3.3	**Function 0: GPIO4_3**

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					GPIO **Function 1: MII_RXD3** MII RX data **Function 2: VOU1120_DATA15** BT.1120 chrominance signal output
C19	MII_RXDV	I/O	8	3.3	**Function 0: GPIO3_4** GPIO **Function 1: MII_RXDV** MII RX data validity indicator **Function 2: VOU1120_DATA1** BT.1120 luminance signal output
B15	MII_RXER	I/O	4	3.3	**Function 0: GPIO2_7** GPIO **Function 1: MII_RXER** RX error. It indicates that the received data is incorrect, and the PHY can discard the data.
C17	MII_TXCK	I/O	12	3.3	**Function 0: GPIO3_3** GPIO **Function 1: MII_TXCK** MII transmit (TX) clock **Function 2: VOU1120_DATA7** BT.1120 luminance signal output **Function 3: RMII_CLK** RMII clock
B18	MII_TXD0	I/O	8	3.3	**Function 0: GPIO4_4** GPIO **Function 1: MII_TXD0** RMII or MII TX data **Function 2: VOU1120_DATA4** BT.1120 luminance signal output
B19	MII_TXD1	I/O	8	3.3	**Function 0: GPIO4_5** GPIO **Function 1: MII_TXD1** RMII or MII TX data **Function 2: VOU1120_DATA0** BT.1120 luminance signal output

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
D17	MII_TXD2	I/O	8	3.3	**Function 0: GPIO4_6** GPIO **Function 1: MII_TXD2** MII TX data **Function 2: VOU1120_DATA13** BT.1120 chrominance signal output
C18	MII_TXD3	I/O	8	3.3	**Function 0: GPIO4_7** GPIO **Function 1: MII_TXD3** MII TX data **Function 2: VOU1120_DATA3** BT.1120 luminance signal output
A18	MII_TXEN	I/O	8	3.3	**Function 0: GPIO3_5** GPIO **Function 1: MII_TXEN** MII TX data enable **Function 2: VOU1120_DATA5** BT.1120 luminance signal output
C16	MII_TXER	I/O	4	3.3	**Function 0: GPIO2_6** GPIO **Function 1: MII_TXER** TX error. It indicates that the received data is incorrect, and the PHY can discard the data.

SFC Pins

Table 2-12 describes SPI flash controller (SFC) pins.

Table 2-12 SFC pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
E19	SFC_CLK	I_{PD}/O	12	3.3	**Function 0: SFC_CLK** Clock signal transmitted to the SPI flash. The high level or low level can be configured when the clock is not switched.

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					Function 1: GPIO7_2 GPIO **Function 2: SFC_ADDR_MODE** Default address mode of the SFC. 0: 3-byte address mode 1: 4-byte address mode
E18	SFC_CSN	I/O	4	3.3	CS 0, active low
F17	SFC_DIO	I/O	8	3.3	**Function 0: SFC_DIO** Data output signal in standard serial peripheral interface (SPI) mode Data I/O signal in dual-SPI mode Data I/O signal in quad-SPI mode **Function 1: GPIO7_0** GPIO
E16	SFC_DOI	I/O	8	3.3	**Function 0: SFC_DOI** Data input signal in standard SPI mode Data I/O signal in dual-SPI mode Data I/O signal in quad-SPI mode **Function 1: GPIO7_3** GPIO
E17	SFC_HOLD_IO3	I/O	8	3.3	**Function 0: SFC_HOLD_IO3** Hold function in standard SPI mode, active low Hold function in dual-SPI mode, active low Data I/O signal in quad-SPI mode **Function 1: GPIO7_4** GPIO
F16	SFC_WP_IO2	I/O	8	3.3	**Function 0: SFC_WP_IO2** Write protection function in standard SPI mode, active low Write protection function in dual-SPI mode, active low Data I/O signal in quad-SPI mode **Function 1: GPIO7_1** GPIO

NFC Pins

Table 2-13 describes NAND flash controller (NFC) pins.

Table 2-13 NFC pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
R2	NF_ALE	I_{PD}/O	8	3.3	**Function 0: NF_ALE** Address latch signal of the NAND flash **Function 1: GPIO8_6** GPIO **Function 2: NF_BOOT_PIN2** This signal is used to configure the NAND flash by working with NF_BOOT_PIN0, NF_BOOT_PIN1, NF_BOOT_PIN3, and NF_BOOT_PIN4, and is valid only during power-on. For details, see the description of NF_BOOT_PIN0.
R1	NF_CLE	I_{PD}/O	8	3.3	**Function 0: NF_CLE** Command latch signal of the NAND flash **Function 1: GPIO8_5** GPIO **Function 2: NF_BOOT_PIN1** This signal is used to configure the NAND flash by working with NF_BOOT_PIN0, NF_BOOT_PIN2, NF_BOOT_PIN3, and NF_BOOT_PIN4, and is valid only during power-on. For details, see the description of NF_BOOT_PIN0.
P2	NF_CSN0	I/O	8	3.3	**Function 0: NF_CSN0** NAND flash CS, active low. This pin is used to mount the NAND flash for booting the system. **Function 1: GPIO8_3** GPIO
P3	NF_CSN1	I/O	8	3.3	**Function 0: NF_CSN1** NAND flash CS, active low. This pin is used to mount the NAND flash for booting the system. **Function 1: GPIO8_4** GPIO

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
K3	NF_DQ0	I/O	8	3.3	**Function 0: NF_DQ0** Data bus of the NAND flash **Function 1: GPIO9_0** GPIO
K1	NF_DQ1	I/O	8	3.3	**Function 0: NF_DQ1** Data bus of the NAND flash **Function 1: GPIO9_1** GPIO
L3	NF_DQ2	I/O	8	3.3	**Function 0: NF_DQ2** Data bus of the NAND flash **Function 1: GPIO9_2** GPIO
L2	NF_DQ3	I/O	8	3.3	**Function 0: NF_DQ3** Data bus of the NAND flash **Function 1: GPIO9_3** GPIO
L1	NF_DQ4	I/O	8	3.3	**Function 0: NF_DQ4** Data bus of the NAND flash **Function 1: GPIO9_4** GPIO
M1	NF_DQ5	I/O	8	3.3	**Function 0: NF_DQ5** Data bus of the NAND flash **Function 1: GPIO9_5** GPIO
M2	NF_DQ6	I/O	8	3.3	**Function 0: NF_DQ6** Data bus of the NAND flash **Function 1: GPIO9_6** GPIO
M3	NF_DQ7	I/O	8	3.3	**Function 0: NF_DQ7** Data bus of the NAND flash **Function 1: GPIO9_7** GPIO
N1	NF_RDY0	I_{PU}/O	8	3.3	**Function 0: NF_RDY0** Status indicator of the NAND flash. 0: busy 1: idle

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					Function 1: GPIO8_0 GPIO
N2	NF_RDY1	I_{PU}/O	8	3.3	**Function 0: NF_RDY1** Status indicator of the NAND flash. 0: busy 1: idle **Function 1: GPIO8_1** GPIO
P1	NF_REN	I_{PU}/O	12	3.3	**Function 0: NF_REN** Read enable signal of the NAND flash, active low **Function 1: GPIO8_2** GPIO **Function 2: NF_BOOT_PIN0** NAND flash type configuration, active only during power-on. The 5-bit signal is locked during power-on. Then the internal logic decodes this signal to obtain the parameter values of the NAND flash such as PAGE_SIZE, ECC_TYPE, BLOCK_SIZE, and ADDR_NUM. For details, see the *Hi3518 720p HD IP Camera SoC Data Sheet*. The page size is 2 KB, the error correcting code (ECC) mode is 1-bit mode, the page/block is 64, and the NAND flash has five addresses by default.
N3	NF_WEN	I_{PD}/O	12	3.3	**Function 0: NF_WEN** Write enable signal of the NAND flash, active low **Function 1: GPIO8_7** GPIO **Function 2: NF_BOOT_PIN3** This signal is used to configure the NAND flash by working with NF_BOOT_PIN0, NF_BOOT_PIN1, NF_BOOT_PIN2, and NF_BOOT_PIN4, and is valid only during power-on. For details, see the description of NF_BOOT_PIN0.

SDIO Pins

Table 2-14 describes secure digital input/output (SDIO) pins.

Table 2-14 SDIO pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
J17	SDIO_CARD_DETECT	I_{PU}/O	4	3.3	**Function 0: GPIO6_0** GPIO **Function 1: SDIO_CARD_DETECT** Card detection signal, active low
H19	SDIO_CARD_POWER_EN	I_{PD}/O	4	3.3	**Function 0: GPIO6_1** GPIO **Function 1: SDIO_CARD_POWER_EN** Power enable signal. The value 1 indicates power on.
H18	SDIO_CCLK_OUT	I_{PD}/O	12	3.3	**Function 0: GPIO1_1** GPIO **Function 1: SDIO_CCLK_OUT** Output working clock for the card
G19	SDIO_CCMD	I_{PU}/O	8	3.3	**Function 0: GPIO6_3** GPIO **Function 1: SDIO_CCMD** Card command
G18	SDIO_CDATA0	I_{PU}/O	8	3.3	**Function 0: GPIO6_4** GPIO **Function 1: SDIO_CDATA0** Card data **Function 2: CLK_TEST_OUT0** Main test clock output **Function 3: CLK_TEST_OUT1** Main test clock output **Function 4:**

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					CLK_TEST_OUT2 Main test clock output **Function 5: CLK_TEST_OUT3** Main test clock output
F19	SDIO_CDATA1	I_{PU}/O	8	3.3	**Function 0: PLL_TEST_OUT0** Phase-locked loop (PLL) test clock output **Function 1: SDIO_CDATA1** Card data **Function 2: GPIO6_5** GPIO **Function 3: PLL_TEST_OUT1** PLL test clock output **Function 4: PLL_TEST_OUT2** PLL test clock output **Function 5: PLL_TEST_OUT3** PLL test clock output **Function 6: RTC_TEST_CLK** Real-time clock (RTC) test clock output
G17	SDIO_CDATA2	I_{PU}/O	8	3.3	**Function 0: GPIO6_6** GPIO **Function 1: SDIO_CDATA2** Card data
F18	SDIO_CDATA3	I_{PU}/O	8	3.3	**Function 0: GPIO6_7** GPIO **Function 1: SDIO_CDATA3** Card data
H17	SDIO_CWPR	I_{PD}/O	4	3.3	**Function 0: GPIO6_2** GPIO **Function 1: SDIO_CWPR**

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					Card write protection detection

USB Pins

Table 2-15 describes universal serial bus (USB) pins.

Table 2-15 USB pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
L17	AVDD33_USB	P	None	3.3	USB analog power
L18	AVDD33_USB25	P	None	3.3	USB analog power, for internally converting the voltage into 2.5 V
J18, L19	AVSS_USB	G	None	None	USB analog GND
L14	DVDD12_USB	P	None	1.2	USB digital power
K19	USB_DM	I/O	None	0.4/3.3	USB port 0 D- signal. In high-speed mode, the maximum voltage of this port is 800 mV or 400 mV. In full-speed or low-speed mode, the voltage of this port is 3.3 V.
K18	USB_DP	I/O	None	0.4/3.3	USB port 0 D+ signal. In high-speed mode, the maximum voltage of this port is 800 mV or 400 mV. In full-speed or low-speed mode, the voltage of this port is 3.3 V.
M17	USB_REXT	I/O	None	3.3	USB external resistor interface, externally connecting to a 43.2 Ω ±1% resistor and then to GND
K17	USB_OVRCUR	I_{PD}/O	4	3.3	Function 0: GPIO5_0 GPIO Function 1: USB_OVRCUR Over-current indicator signal of the USB port, configurable level, and active high by default
J19	USB_PWREN	I_{PD}/O	8	3.3	**Function 0: GPIO5_1** GPIO **Function 1: USB_PWREN**

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					Power control output of the USB port, configurable level, and active low by default

Audio CODEC Pins

Table 2-16 describes audio CODEC pins.

Table 2-16 Audio CODEC pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
P19	AC_LINEL	I	None	3.3	Audio-left channel input of the audio interface
P18	AC_LINER	I	None	3.3	Audio-right channel input of the audio interface
M18	AC_MICBIAS	I/O	None	3.3	Microphone bias voltage, externally connecting to a 4.7 μF capacitor and then to GND
M19	AC_OUTL	O	None	3.3	Audio-left channel output of the audio interface
N19	AC_OUTR	O	None	3.3	Audio-right channel output of the audio interface
N18	AC_VREF	P	None	3.3	Audio reference voltage
P17	AC_AGND	G	None	None	Audio analog GND.
N17	AVDD_AC	P	None	3.3	Audio analog power

VI Pins

Table 2-17 describes sensor pins.

Table 2-17 VI pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
W10	SENSOR_CLK	I/O	24	1.8/3.3	**Function 0: GPIO1_2** GPIO

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					Function 1: SENSOR_CLK Sensor working clock
V9	VIU_CLK	I/O	4	1.8/3.3	**Function 0: VIU_CLK** Video input unit 0 (VIU 0) clock **Function 1: GPIO11_6** GPIO
T6	VIU_DAT0	I/O	4	1.8/3.3	**Function 0: VIU_DAT0** VIU 0 data input **Function 1: GPIO10_0** GPIO
U6	VIU_DAT1	I/O	4	1.8/3.3	**Function 0: VIU_DAT1** VIU 0 data input **Function 1: GPIO10_1** GPIO
U7	VIU_DAT2	I/O	4	1.8/3.3	**Function 0: VIU_DAT2** VIU 0 data input **Function 1: GPIO10_2** GPIO
V6	VIU_DAT3	I/O	4	1.8/3.3	**Function 0: VIU_DAT3** VIU 0 data input **Function 1: GPIO10_3** GPIO
W6	VIU_DAT4	I/O	4	1.8/3.3	**Function 0: VIU_DAT4** VIU 0 data input **Function 1: GPIO10_4** GPIO
U8	VIU_DAT5	I_{PD}/O	4	1.8/3.3	**Function 0: VIU_DAT5** VIU0 data input **Function 1: GPIO10_5** GPIO
V7	VIU_DAT6	I/O	4	1.8/3.3	**Function 0: VIU_DAT6** VIU0 data input **Function 1: GPIO10_6** GPIO
W7	VIU_DAT7	I/O	4	1.8/3.3	**Function 0: VIU_DAT7** VIU0 data input

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					Function 1: GPIO10_7 GPIO
U9	VIU_DAT8	I/O	4	1.8/3.3	**Function 0: VIU_DAT8** VIU0 data input **Function 1: GPIO11_0** GPIO
V8	VIU_DAT9	I/O	4	1.8/3.3	**Function 0: VIU_DAT9** VIU0 data input **Function 1: GPIO11_1** GPIO
W8	VIU_DAT10	I/O	4	1.8/3.3	**Function 0: VIU_DAT10** VIU0 data input **Function 1: GPIO11_2** GPIO
W9	VIU_DAT11	I/O	4	1.8/3.3	**Function 0: VIU_DAT11** VIU0 data input **Function 1: GPIO11_3** GPIO
V5	VIU_HS	I/O	4	1.8/3.3	**Function 0: VIU_HS** VIU 0 horizontal sync, active high **Function 1: GPIO11_4** GPIO
W5	VIU_VS	I/O	4	1.8/3.3	**Function 0: VIU_VS** VIU 0 vertical sync, active high **Function 1: GPIO11_5** GPIO

VDAC Pins

Table 2-18 describes video digital-to-analog converter (VDAC) pins.

Table 2-18 VDAC pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
R19	VDAC_COMP	O	None	3.3	VDAC compensation capacitor,

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					externally connecting to a 0.01 μF ceramic capacitor and a 10 μF tantalum capacitor in parallel and then to AVDD33_VDAC
R17	VDAC_IOUT	O	None	3.3	Composite video broadcast signal (CVBS) output
R18	VDAC_REXT	I/O	None	3.3	VDAC matched resistor interface, externally connecting to a 260 Ω resistor
P16	AVDD33_VDAC	P	None	3.3	VDAC analog power
N14	AVSS_VDAC	G	None	None	VDAC analog GND
R16	AVSS33_VDAC	G	None	None	VDAC analog GND

UART Pins

Table 2-19 describes universal asynchronous receiver transmitter 0 (UART 0) pins.

Table 2-19 UART 0 pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
T19	UART0_RXD	I_{PU}	None	3.3	UART 0 RX data
T18	UART0_TXD	I/O	4	3.3	UART 0 TX data

Table 2-20 describes UART 1 pins.

Table 2-20 UART 1 pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
T17	UART1_CTSN	I/O	4	3.3	**Function 0: GPIO2_4** GPIO **Function 1: UART1_CTSN** Modem state input: clear-to-send (CTS), active low

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
T16	UART1_RTSN	I/O	4	3.3	**Function 0: GPIO2_2** GPIO **Function 1: UART1_RTSN** Modem state output: request-to-send (RTS), active low. The reset value is 0.
V19	UART1_RXD	I_{PU}/O	4	3.3	**Function 0: GPIO2_3** GPIO **Function 1: UART1_RXD** UART 1 RX data
U17	UART1_TXD	I/O	4	3.3	**Function 0: GPIO2_5** GPIO **Function 1: UART1_TXD** UART 1 TX data

Table 2-21 describes UART 2 pins.

Table 2-21 UART 2 pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
U18	UART2_RXD	I_{PU}/O	4	3.3	**Function 0: GPIO7_6** GPIO **Function 1: UART2_RXD** UART 2 RX data
U19	UART2_TXD	I/O	4	3.3	**Function 0: GPIO7_7** GPIO **Function 1: UART2_TXD** UART 2 TX data

Camera Flash Pin

Table 2-22 describes the camera flash pin.

Table 2-22 Camera flash pin

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
V12	FLASH_TRIG	I/O	4	3.3	**Function 0: GPIO1_7** GPIO **Function 1: FLASH_TRIG** Camera flash control

Shutter Pin

Table 2-23 describes the shutter pin.

Table 2-23 Shutter pin

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
U12	SHUTTER_TRIG	I/O	4	3.3	**Function 0: GPIO1_0** GPIO **Function 1: SHUTTER_TRIG** Shutter control

SPI Pins

Table 2-24 describes SPI 0 pins.

Table 2-24 SPI 0 pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
W4	SPI0_CSN	I_{PD}/O	8	1.8/3.3	**Function 0: SPI0_CSN** SPI CS 0 output **Function 1: NF_BOOT_PIN4** This signal is used to configure the NAND flash by working with NF_BOOT_PIN0, NF_BOOT_PIN1, NF_BOOT_PIN2, and NF_BOOT_PIN3, and is valid only during power-on. For details, see the description of NF_BOOT_PIN0.
V4	SPI0_SCLK	I/O	16	1.8/3.3	**Function 0: GPIO1_4** GPIO

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					Function 1: SPI0_SCLK SPI clock
T5	SPI0_SDI	I_{PD}/O	8	1.8/3.3	**Function 0: GPIO1_6** GPIO **Function 1: SPI0_SDI** SPI data input
U5	SPI0_SDO	I/O	12	1.8/3.3	**Function 0: GPIO1_5** GPIO **Function 1: SPI0_SDO** SPI data output
P8	DVDD3318	P	None	1.8/3.3	Digital power
P9	DVDD3318	P	None	1.8/3.3	Digital power

Table 2-25 describes SPI 1 pins.

Table 2-25 SPI 1 pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
U10	SPI1_CSN	I/O	4	3.3	**Function 0: GPIO5_7** GPIO **Function 1: SPI1_CSN** SPI CS 0 output
V11	SPI1_SCLK	I/O	12	3.3	**Function 0: GPIO5_4** GPIO **Function 1: SPI1_SCLK** SPI clock
U11	SPI1_SDI	I_{PD}/O	4	3.3	**Function 0: GPIO5_6** GPIO **Function 1: SPI1_SDI** SPI data input
W11	SPI1_SDO	I/O	8	3.3	**Function 0: GPIO5_5** GPIO **Function 1: SPI1_SDO**

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					SPI data output

I²C Pins

Table 2-26 describes inter-integrated circuit (I^2C) pins.

Table 2-26 I^2C pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
W13	I2C_SCL	I/O_{OD}	8	3.3	**Function 0: GPIO2_1** GPIO **Function 1: I2C_SCL** I^2C bus clock, OD output
W12	I2C_SDA	I/O_{OD}	8	3.3	**Function 0: GPIO2_0** GPIO **Function 1: I2C_SDA** I^2C bus data/address, OD output

IR Pin

Table 2-27 describes the infrared (IR) pin.

Table 2-27 IR pin

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
U13	IR_IN	I_{PU}/O	4	3.3	**Function 0: IR_IN** Infrared input **Function 1: GPIO7_5** GPIO

PWM Pins

Table 2-28 describes pulse width modulation (PWM) pins.

Table 2-28 PWM pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
V15	PWM_OUT0	I/O	4	3.3	**Function 0: GPIO5_2** GPIO **Function 1: PWM_OUT0** PWM output 0
W15	PWM_OUT1	I/O	4	3.3	**Function 0: GPIO5_3** GPIO **Function 1: PWM_OUT1** PWM output 1

GPIO Pins

Table 2-29 describes GPIO pins.

Table 2-29 GPIO pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
W18	GPIO0_5	I/O	4	3.3	**Function 0: SVB_PWM** SVB control signal output **Function 1: GPIO0_5** GPIO **Function 2: TEMPER_DQ** Temperature measurement. It is used to communicate with the external temperature measurement chip.
T15	GPIO0_6	I/O	4	3.3	**Function 0: GPIO0_6** GPIO **Function 1: SVB_PWM** SVB control signal output **Function 2: TEMPER_DQ** Temperature measurement. It is used to communicate with the external temperature measurement chip.
V18	GPIO0_7	I/O	4	3.3	**Function 0: SYS_RSTN_OUT** System reset output **Function 1: GPIO0_7** GPIO

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					Function 2: TEMPER_DQ Temperature measurement. It is used to communicate with the external temperature measurement chip.

SAR_ADC Pins

Table 2-30 describes SAR_ADC pins.

Table 2-30 SAR_ADC pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
T4	SAR_ADC_CH0	I	None	3.3	SAR_ADC channel 0
V3	SAR_ADC_CH1	I	None	3.3	SAR_ADC channel 1
U3	SAR_ADC_VREF	P	None	3.3	SAR_ADC reference voltage
P6	AVDD_ADC	P	None	3.3	SAR_ADC analog power
N6	AVSS_ADC	G	None	None	SAR_ADC analog GND

RTC Pins

Table 2-31 describes RTC pins.

Table 2-31 RTC pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
W2	RTC_XIN	I	None	3.3	RTC crystal input
W3	RTC_XOUT	O	None	3.3	RTC crystal output
T2	AVDD_BAT	P	None	3.3	RTC battery power
T3	AVDD33_RTC	P	None	3.3	RTC analog power

Power Pins and GND Pins

Table 2-32 describes power pins and GND pins.

Table 2-32 Power pins and GND pins

Pin Position	Pin Name	Type	Voltage (V)	Description
P4	AVDD12_PLL	P	1.2	1.2 V PLL analog power
R4	AVDD33_PLL	P	3.3	3.3 V PLL analog power
R3	AVSS_PLL	G	None	PLL analog GND
F6, F7, F8, F11, F12, F14, J6, J14, K6, K14, P7, P11, P12	DVDD12	P	1.2	Core power
F13, G14, H14, L6, M6, M14, P10, P13, P14	DVDD33	P	3.3	3.3 V I/O digital power
P8, P9	DVDD3318	P	3.3/1.8	3.3 V or 1.8 V I/O digital power
A1, A19, B14, B17, C1, C2, C6, C9, C11, C14, D5, D19, E4, G7, G8, G9, G10, G11, G12, G13, H7, H8, H9, H10, H11, H12, H13, J7, J8, J9, J10, J11, J12, J13, K2, K7, K8, K9, K10, K11, K12, K13, L7, L8, L9, L10, L11, L12, L13, M7, M8, M9, M10, M11, M12, M13, N7, N8, N9, N10, N11, N12, N13, T1, U2, U4, V2, V10, V17, W1, W19	DVSS	G	None	Digital GND

2.3 Pin Multiplexing Control Registers

2.3.1 Summary of Multiplexing Control Registers

Table 2-33 describes multiplexing registers.

Table 2-33 Summary of multiplexing control registers (base address:0x200F_0000)

Offset Address	Register	Description	Page
0x000	muxctrl_reg0	Multiplexing control register for the SHUTTER_TRIG pin	2-44
0x004	muxctrl_reg1	Multiplexing control register for the SDIO_CCLK_OUT pin	2-45
0x008	muxctrl_reg2	Multiplexing control register for the SENSOR_CLK pin	2-45
0x00C	muxctrl_reg3	Multiplexing control register for the SPI0_SCLK pin	2-45

Offset Address	Register	Description	Page
0x010	muxctrl_reg4	Multiplexing control register for the SPI0_SDO pin	2-46
0x014	muxctrl_reg5	Multiplexing control register for the SPI0_SDI pin	2-46
0x018	muxctrl_reg6	Multiplexing control register for the I2C_SDA pin	2-47
0x01C	muxctrl_reg7	Multiplexing control register for the I2C_SCL pin	2-47
0x020	muxctrl_reg8	Multiplexing control register for the UART1_RTSN pin	2-48
0x024	muxctrl_reg9	Multiplexing control register for the UART1_RXD pin	2-48
0x028	muxctrl_reg10	Multiplexing control register for the UART1_CTSN pin	2-49
0x02C	muxctrl_reg11	Multiplexing control register for the UART1_TXD pin	2-49
0x030	muxctrl_reg12	Multiplexing control register for the MII_CRS pin	2-50
0x034	muxctrl_reg13	Multiplexing control register for the MII_COL pin	2-50
0x038	muxctrl_reg14	Multiplexing control register for the MII_RXD3 pin	2-51
0x03C	muxctrl_reg15	Multiplexing control register for the MII_RXD2 pin	2-51
0x040	muxctrl_reg16	Multiplexing control register for the MII_RXD1 pin	2-52
0x044	muxctrl_reg17	Multiplexing control register for the MII_RXD0 pin	2-52
0x048	muxctrl_reg18	Multiplexing control register for the MII_TXD3 pin	2-53
0x04C	muxctrl_reg19	Multiplexing control register for the MII_TXD2 pin	2-53
0x050	muxctrl_reg20	Multiplexing control register for the MII_TXD1 pin	2-54
0x054	muxctrl_reg21	Multiplexing control register for the MII_TXD0 pin	2-54
0x058	muxctrl_reg22	Multiplexing control register for the MII_RXCK pin	2-55
0x05C	muxctrl_reg23	Multiplexing control register for the MII_TXCK pin	2-55
0x060	muxctrl_reg24	Multiplexing control register for the MII_RXDV pin	2-55
0x064	muxctrl_reg25	Multiplexing control register for the MII_TXEN pin	2-56
0x068	muxctrl_reg26	Multiplexing control register for the MII_TXER pin	2-56
0x06C	muxctrl_reg27	Multiplexing control register for the MII_RXER pin	2-57
0x070	muxctrl_reg28	Multiplexing control register for the EPHY_CLK pin	2-57
0x074	muxctrl_reg29	Multiplexing control register for the MDCK pin	2-58
0x078	muxctrl_reg30	Multiplexing control register for the MDIO pin	2-58
0x07C	muxctrl_reg31	Multiplexing control register for the FLASH_TRIG	2-58

Offset Address	Register	Description	Page
		pin	
0x080	muxctrl_reg32	Multiplexing control register for the SDIO_CARD_DETECT pin	2-59
0x084	muxctrl_reg33	Multiplexing control register for the SDIO_CARD_POWER_EN pin	2-59
0x088	muxctrl_reg34	Multiplexing control register for the SDIO_CWPR pin	2-60
0x08C	muxctrl_reg35	Multiplexing control register for the SDIO_CCMD pin	2-60
0x090	muxctrl_reg36	Multiplexing control register for the SDIO_CDATA0 pin	2-60
0x094	muxctrl_reg37	Multiplexing control register for the SDIO_CDATA1 pin	2-61
0x098	muxctrl_reg38	Multiplexing control register for the SDIO_CDATA2 pin	2-61
0x09C	muxctrl_reg39	Multiplexing control register for the SDIO_CDATA3 pin	2-62
0x0A0	muxctrl_reg40	Multiplexing control register for the SFC_DIO pin	2-62
0x0A4	muxctrl_reg41	Multiplexing control register for the SFC_WP_IO2 pin	2-63
0x0A8	muxctrl_reg42	Multiplexing control register for the SFC_CLK pin	2-63
0x0AC	muxctrl_reg43	Multiplexing control register for the SFC_DOI pin	2-63
0x0B0	muxctrl_reg44	Multiplexing control register for the SFC_HOLD_IO3 pin	2-64
0x0B4	muxctrl_reg45	Multiplexing control register for the USB_OVRCUR pin	2-64
0x0B8	muxctrl_reg46	Multiplexing control register for the USB_PWREN pin	2-65
0x0BC	muxctrl_reg47	Multiplexing control register for the PWM_OUT0 pin	2-65
0x0C0	muxctrl_reg48	Multiplexing control register for the PWM_OUT1 pin	2-66
0x0C4	muxctrl_reg49	Multiplexing control register for the IR_IN pin	2-66
0x0C8	muxctrl_reg50	Multiplexing control register for the NF_DQ0 pin	2-67
0x0CC	muxctrl_reg51	Multiplexing control register for the NF_DQ1 pin	2-67
0x0D0	muxctrl_reg52	Multiplexing control register for the NF_DQ2 pin	2-68

Offset Address	Register	Description	Page
0x0D4	muxctrl_reg53	Multiplexing control register for the NF_DQ3 pin	2-68
0x0D8	muxctrl_reg54	Multiplexing control register for the NF_DQ4 pin	2-69
0x0DC	muxctrl_reg55	Multiplexing control register for the NF_DQ5 pin	2-69
0x0E0	muxctrl_reg56	Multiplexing control register for the NF_DQ6 pin	2-70
0x0E4	muxctrl_reg57	Multiplexing control register for the NF_DQ7 pin	2-70
0x0E8	muxctrl_reg58	Multiplexing control register for the NF_RDY0 pin	2-71
0x0EC	muxctrl_reg59	Multiplexing control register for the NF_RDY1 pin	2-71
0x0F0	muxctrl_reg60	Multiplexing control register for the NF_REN pin	2-72
0x0F4	muxctrl_reg61	Multiplexing control register for the NF_CSN0 pin	2-72
0x0F8	muxctrl_reg62	Multiplexing control register for the NF_CSN1 pin	2-73
0x0FC	muxctrl_reg63	Multiplexing control register for the NF_CLE pin	2-73
0x100	muxctrl_reg64	Multiplexing control register for the NF_ALE pin	2-74
0x104	muxctrl_reg65	Multiplexing control register for the NF_WEN pin	2-74
0x108	muxctrl_reg66	Multiplexing control register for the UART2_RXD pin	2-75
0x10C	muxctrl_reg67	Multiplexing control register for the UART2_TXD pin	2-75
0x110	muxctrl_reg68	Multiplexing control register for the SPI1_SCLK pin	2-76
0x114	muxctrl_reg69	Multiplexing control register for the SPI1_SDO pin	2-76
0x118	muxctrl_reg70	Multiplexing control register for the SPI1_SDI pin	2-77
0x11C	muxctrl_reg71	Multiplexing control register for the SPI1_CSN pin	2-77
0x120	muxctrl_reg72	Multiplexing control register for the JTAG_TRSTN pin	2-78
0x124	muxctrl_reg73	Multiplexing control register for the JTAG_TCK pin	2-78
0x128	muxctrl_reg74	Multiplexing control register for the JTAG_TMS pin	2-79
0x12C	muxctrl_reg75	Multiplexing control register for the JTAG_TDO pin	2-79
0x130	muxctrl_reg76	Multiplexing control register for the JTAG_TDI pin	2-80
0x134	muxctrl_reg77	Multiplexing control register for the GPIO0_5 pin	2-80
0x138	muxctrl_reg78	Multiplexing control register for the GPIO0_6 pin	2-81
0x13C	muxctrl_reg79	Multiplexing control register for the GPIO0_7 pin	2-81
0x140	muxctrl_reg80	Multiplexing control register for the VIU_CLK pin	2-82

Offset Address	Register	Description	Page
0x144	muxctrl_reg81	Multiplexing control register for the VIU_VS pin	2-82
0x148	muxctrl_reg82	Multiplexing control register for the VIU_HS pin	2-83
0x14C	muxctrl_reg83	Multiplexing control register for the VIU_DAT11 pin	2-83
0x150	muxctrl_reg84	Multiplexing control register for the VIU_DAT10 pin	2-84
0x154	muxctrl_reg85	Multiplexing control register for the VIU_DAT9 pin	2-84
0x158	muxctrl_reg86	Multiplexing control register for the VIU_DAT8 pin	2-85
0x15C	muxctrl_reg87	Multiplexing control register for the VIU_DAT7 pin	2-85
0x160	muxctrl_reg88	Multiplexing control register for the VIU_DAT6 pin	2-86
0x164	muxctrl_reg89	Multiplexing control register for the VIU_DAT5 pin	2-86
0x168	muxctrl_reg90	Multiplexing control register for the VIU_DAT4 pin	2-87
0x16C	muxctrl_reg91	Multiplexing control register for the VIU_DAT3 pin	2-87
0x170	muxctrl_reg92	Multiplexing control register for the VIU_DAT2 pin	2-88
0x174	muxctrl_reg93	Multiplexing control register for the VIU_DAT1 pin	2-88
0x178	muxctrl_reg94	Multiplexing control register for the VIU_DAT0 pin	2-89

2.3.2 Register Description

muxctrl_reg0

muxctrl_reg0 is a multiplexing control register for the SHUTTER_TRIG pin.

Offset Address	Register Name	Total Reset Value
0x000	muxctrl_reg0	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								muxctrl_reg0
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg0	Multiplexing for the SHUTTER_TRIG pin. 0: GPIO1_0 1: SHUTTER_TRIG

muxctrl_reg1

muxctrl_reg1 is a multiplexing control register for the SDIO_CCLK_OUT pin.

Offset Address	Register Name	Total Reset Value
0x004	muxctrl_reg1	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							muxctrl_reg1
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg1	Multiplexing for the SDIO_CCLK_OUT pin. 0: GPIO1_1 1: SDIO_CCLK_OUT

muxctrl_reg2

muxctrl_reg2 is a multiplexing control register for the SENSOR_CLK pin.

Offset Address	Register Name	Total Reset Value
0x008	muxctrl_reg2	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							muxctrl_reg2
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg2	Multiplexing for the SENSOR_CLK pin. 0: GPIO1_2 1: SENSOR_CLK

muxctrl_reg3

muxctrl_reg3 is a multiplexing control register for the SPI0_SCLK pin.

Offset Address	Register Name	Total Reset Value
0x00C	muxctrl_reg3	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg3
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg3	Multiplexing for the SPI0_SCLK pin. 0: GPIO1_4 1: SPI0_SCLK

muxctrl_reg4

muxctrl_reg4 is a multiplexing control register for the SPI0_SDO pin.

Offset Address	Register Name	Total Reset Value
0x010	muxctrl_reg4	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg4
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg4	Multiplexing for the SPI0_SDO pin. 0: GPIO1_5 1: SPI0_SDO

muxctrl_reg5

muxctrl_reg5 is a multiplexing control register for the SPI0_SDI pin.

Offset Address	Register Name	Total Reset Value
0x014	muxctrl_reg5	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg5
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg5	Multiplexing for the SPI0_SDI pin. 0: GPIO1_6 1: SPI0_SDI

muxctrl_reg6

muxctrl_reg6 is a multiplexing control register for the I2C_SDA pin.

Offset Address	Register Name	Total Reset Value
0x018	muxctrl_reg6	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg6
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg6	Multiplexing for the I2C_SDA pin. 0: GPIO2_0 1: I2C_SDA

muxctrl_reg7

muxctrl_reg7 is a multiplexing control register for the I2C_SCL pin.

Offset Address	Register Name	Total Reset Value
0x01C	muxctrl_reg7	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg7
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg7	Multiplexing for the I2C_SCL pin. 0: GPIO2_1 1: I2C_SCL

muxctrl_reg8

muxctrl_reg8 is a multiplexing control register for the UART1_RTSN pin.

Offset Address	Register Name	Total Reset Value
0x020	muxctrl_reg8	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg8
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg8	Multiplexing for the UART1_RTSN pin. 0: GPIO2_2 1: UART1_RTSN

muxctrl_reg9

muxctrl_reg9 is a multiplexing control register for the UART1_RXD pin.

Offset Address	Register Name	Total Reset Value
0x024	muxctrl_reg9	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg9
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg9	Multiplexing for the UART1_RXD pin. 0: GPIO2_3 1: UART1_RXD

muxctrl_reg10

muxctrl_reg10 is a multiplexing control register for the UART1_CTSN pin.

Offset Address	Register Name	Total Reset Value
0x028	muxctrl_reg10	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg10
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg10	Multiplexing for the UART1_CTSN pin. 0: GPIO2_4 1: UART1_CTSN

muxctrl_reg11

muxctrl_reg11 is a multiplexing control register for the UART1_TXD pin.

Offset Address	Register Name	Total Reset Value
0x02C	muxctrl_reg11	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg1
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg11	Multiplexing for the UART1_TXD pin. 0: GPIO2_5 1: UART1_TXD

muxctrl_reg12

muxctrl_reg12 is a multiplexing control register for the MII_CRS pin.

Offset Address	Register Name	Total Reset Value
0x030	muxctrl_reg12	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg12	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg12	Multiplexing for the MII_CRS pin. 00: GPIO3_0 01: MII_CRS 10: VOU1120_DATA10 Other values: reserved

muxctrl_reg13

muxctrl_reg13 is a multiplexing control register for the MII_COL pin.

Offset Address	Register Name	Total Reset Value
0x034	muxctrl_reg13	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg13	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg13	Multiplexing for the MII_COL pin. 00: GPIO3_1 01: MII_COL 10: VOU1120_DATA9 Other values: reserved

muxctrl_reg14

muxctrl_reg14 is a multiplexing control register for the MII_RXD3 pin.

Offset Address	Register Name	Total Reset Value
0x038	muxctrl_reg14	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg14	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg14	Multiplexing for the MII_RXD3 pin. 00: GPIO4_3 01: MII_RXD3 10: VOU1120_DATA15 Other values: reserved

muxctrl_reg15

muxctrl_reg15 is a multiplexing control register for the MII_RXD2 pin.

Offset Address	Register Name	Total Reset Value
0x03C	muxctrl_reg15	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg15	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg15	Multiplexing for the MII_RXD2 pin. 00: GPIO4_2 01: MII_RXD2 10: VOU1120_DATA11 Other values: reserved

muxctrl_reg16

muxctrl_reg16 is a multiplexing control register for the MII_RXD1 pin.

Offset Address	Register Name	Total Reset Value
0x040		0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg16	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg16	Multiplexing for the MII_RXD1 pin. 00: GPIO4_1 01: MII_RXD1 10: VOU1120_DATA8 Other values: reserved

muxctrl_reg17

muxctrl_reg17 is a multiplexing control register for the MII_RXD0 pin.

Offset Address	Register Name	Total Reset Value
0x044	muxctrl_reg17	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg17	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg17	Multiplexing for the MII_RXD0 pin. 00: GPIO4_0 01: MII_RXD0 10: VOU1120_DATA12 Other values: reserved

muxctrl_reg18

muxctrl_reg18 is a multiplexing control register for the MII_TXD3 pin.

Offset Address	Register Name	Total Reset Value
0x048	muxctrl_reg18	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg18	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg18	Multiplexing for the MII_TXD3 pin. 00: GPIO4_7 01: MII_TXD3 10: VOU1120_DATA3 Other values: reserved

muxctrl_reg19

muxctrl_reg19 is a multiplexing control register for the MII_TXD2 pin.

Offset Address	Register Name	Total Reset Value
0x04C	muxctrl_reg19	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg19	

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg19	Multiplexing for the MII_TXD2 pin. 00: GPIO4_6 01: MII_TXD2 10: VOU1120_DATA13 Other values: reserved

muxctrl_reg20

muxctrl_reg20 is a multiplexing control register for the MII_TXD1 pin.

Offset Address	Register Name	Total Reset Value
0x050	muxctrl_reg20	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg20	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg20	Multiplexing for the MII_TXD1 pin. 00: GPIO4_5 01: MII_TXD1 10: VOU1120_DATA0 Other values: reserved

muxctrl_reg21

muxctrl_reg21 is a multiplexing control register for the MII_TXD0 pin.

Offset Address	Register Name	Total Reset Value
0x054	muxctrl_reg21	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg21	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg21	Multiplexing for the MII_TXD0 pin. 00: GPIO4_4 01: MII_TXD0

			10: VOU1120_DATA4 Other values: reserved

muxctrl_reg22

muxctrl_reg22 is a multiplexing control register for the MII_RXCK pin.

Offset Address	Register Name	Total Reset Value
0x058	muxctrl_reg22	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg22	Multiplexing for the MII_RXCK pin. 00: GPIO3_2 01: MII_RXCK 10: VOU1120_CLK Other values: reserved

muxctrl_reg23

muxctrl_reg23 is a multiplexing control register for the MII_TXCK pin.

Offset Address	Register Name	Total Reset Value
0x05C	muxctrl_reg23	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg23	Multiplexing for the MII_TXCK pin. 00: GPIO3_3 01: MII_TXCK 10: VOU1120_DATA7 11: RMII_CLK

muxctrl_reg24

muxctrl_reg24 is a multiplexing control register for the MII_RXDV pin.

Offset Address	Register Name	Total Reset Value
0x060	muxctrl_reg24	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg24	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg24	Multiplexing for the MII_RXDV pin. 00: GPIO3_4 01: MII_RXDV 10: VOU1120_DATA1 Other values: reserved

muxctrl_reg25

muxctrl_reg25 is a multiplexing control register for the MII_TXEN pin.

Offset Address	Register Name	Total Reset Value
0x064	muxctrl_reg25	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg25	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg25	Multiplexing for the MII_TXEN pin. 00: GPIO3_5 01: MII_TXEN 10: VOU1120_DATA5 Other values: reserved

muxctrl_reg26

muxctrl_reg26 is a multiplexing control register for the MII_TXER pin.

Offset Address	Register Name	Total Reset Value
0x068	muxctrl_reg26	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg26	

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg26	Multiplexing for the MII_TXER pin. 0: GPIO2_6 1: MII_TXER

muxctrl_reg27

muxctrl_reg27 is a multiplexing control register for the MII_RXER pin.

Offset Address	Register Name	Total Reset Value
0x06C	muxctrl_reg27	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxc
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg27	Multiplexing for the MII_RXER pin. 0: GPIO2_7 1: MII_RXER

muxctrl_reg28

muxctrl_reg28 is a multiplexing control register for the EPHY_CLK pin.

Offset Address	Register Name	Total Reset Value
0x070	muxctrl_reg28	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxc	trl_re
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg28	Multiplexing for the EPHY_CLK pin. 00: GPIO1_3 01: EPHY_CLK 10: VOU1120_DATA2 Other values: reserved

muxctrl_reg29

muxctrl_reg29 is a multiplexing control register for the MDCK pin.

Offset Address	Register Name	Total Reset Value
0x074	muxctrl_reg29	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg29	Multiplexing for the MDCK pin. 00: GPIO3_6 01: MDCK 10: VOU1120_DATA6 11: BOOT_SEL

muxctrl_reg30

muxctrl_reg30 is a multiplexing control register for the MDIO pin.

Offset Address	Register Name	Total Reset Value
0x078	muxctrl_reg30	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg30	Multiplexing for the MDIO pin. 00: GPIO3_7 01: MDIO 10: VOU1120_DATA14 Other values: reserved

muxctrl_reg31

muxctrl_reg31 is a multiplexing control register for the FLASH_TRIG pin.

Offset Address	Register Name	Total Reset Value
0x07C	muxctrl_reg31	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxc
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg31	Multiplexing for the FLASH_TRIG pin. 0: GPIO1_7 1: FLASH_TRIG

muxctrl_reg32

muxctrl_reg32 is a multiplexing control register for the SDIO_CARD_DETECT pin.

Offset Address	Register Name	Total Reset Value
0x080	muxctrl_reg32	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxc
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg32	Multiplexing for the SDIO_CARD_DETECT pin. 0: GPIO6_0 1: SDIO_CARD_DETECT

muxctrl_reg33

muxctrl_reg33 is a multiplexing control register for the SDIO_CARD_POWER_EN pin.

Offset Address	Register Name	Total Reset Value
0x084	muxctrl_reg33	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxc
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg33	Multiplexing for the SDIO_CARD_POWER_EN pin. 0: GPIO6_1

			1: SDIO_CARD_POWER_EN

muxctrl_reg34

muxctrl_reg34 is a multiplexing control register for the SDIO_CWPR pin.

Offset Address	Register Name	Total Reset Value
0x088	muxctrl_reg34	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxc
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg34	Multiplexing for the SDIO_CWPR pin. 0: GPIO6_2 1: SDIO_CWPR

muxctrl_reg35

muxctrl_reg35 is a multiplexing control register for the SDIO_CCMD pin.

Offset Address	Register Name	Total Reset Value
0x08C	muxctrl_reg35	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxc
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg35	Multiplexing for the SDIO_CCMD pin. 0: GPIO6_3 1: SDIO_CCMD

muxctrl_reg36

muxctrl_reg36 is a multiplexing control register for the SDIO_CDATA0 pin.

Offset Address	Register Name	Total Reset Value
0x090	muxctrl_reg36	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													muxctrl_reg36		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[2:0]	RW	muxctrl_reg36	Multiplexing for the SDIO_CDATA0 pin. 000: GPIO6_4 001: SDIO_CDATA0 010: CLK_TEST_OUT0 011: CLK_TEST_OUT1 100: CLK_TEST_OUT2 101: CLK_TEST_OUT3 Other values: reserved

muxctrl_reg37

muxctrl_reg37 is a multiplexing control register for the SDIO_CDATA1 pin.

Offset Address	Register Name	Total Reset Value
0x094	muxctrl_reg37	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													muxctrl_reg37		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[2:0]	RW	muxctrl_reg37	Multiplexing for the SDIO_CDATA1 pin. 000: PLL_TEST_OUT0 001: SDIO_CDATA1 010: GPIO6_5 011: PLL_TEST_OUT1 100: PLL_TEST_OUT2 101: PLL_TEST_OUT3 110: RTC_TEST_CLK Other values: reserved

muxctrl_reg38

muxctrl_reg38 is a multiplexing control register for the SDIO_CDATA2 pin.

Offset Address	Register Name	Total Reset Value
0x098	muxctrl_reg38	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxc
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg38	Multiplexing for the SDIO_CDATA2 pin. 0: GPIO6_6 1: SDIO_CDATA2

muxctrl_reg39

muxctrl_reg39 is a multiplexing control register for the SDIO_CDATA3 pin.

Offset Address	Register Name	Total Reset Value
0x09C	muxctrl_reg39	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxc
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg39	Multiplexing for the SDIO_CDATA3 pin. 0: GPIO6_7 1: SDIO_CDATA3

muxctrl_reg40

muxctrl_reg40 is a multiplexing control register for the SFC_DIO pin.

Offset Address	Register Name	Total Reset Value
0x0A0	muxctrl_reg40	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxc
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg40	Multiplexing for the SFC_DIO pin. 0: SFC_DIO

			1: GPIO7_0

muxctrl_reg41

muxctrl_reg41 is a multiplexing control register for the SFC_WP_IO2 pin.

Offset Address	Register Name	Total Reset Value
0x0A4	muxctrl_reg41	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxc
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg41	Multiplexing for the SFC_WP_IO2 pin. 0: SFC_WP_IO2 1: GPIO7_1

muxctrl_reg42

muxctrl_reg42 is a multiplexing control register for the SFC_CLK pin.

Offset Address	Register Name	Total Reset Value
0x0A8	muxctrl_reg42	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxc	trl_re
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg42	Multiplexing for the SFC_CLK pin. 00: SFC_CLK 01: GPIO7_2 10: SFC_ADDR_MODE Other values: reserved

muxctrl_reg43

muxctrl_reg43 is a multiplexing control register for the SFC_DOI pin.

Offset Address	Register Name	Total Reset Value
0x0AC	muxctrl_reg43	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg43
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg43	Multiplexing for the SFC_DOI pin. 0: SFC_DOI 1: GPIO7_3

muxctrl_reg44

muxctrl_reg44 is a multiplexing control register for the SFC_HOLD_IO3 pin.

Offset Address	Register Name	Total Reset Value
0x0B0	muxctrl_reg44	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg44
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg44	Multiplexing for the SFC_HOLD_IO3 pin. 0: SFC_HOLD_IO3 1: GPIO7_4

muxctrl_reg45

muxctrl_reg45 is a multiplexing control register for the USB_OVRCUR pin.

Offset Address	Register Name	Total Reset Value
0x0B4	muxctrl_reg45	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							muxctrl_reg45
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg45	Multiplexing for the USB_OVRCUR pin. 0: GPIO5_0 1: USB_OVRCUR

muxctrl_reg46

muxctrl_reg46 is a multiplexing control register for the USB_PWREN pin.

Offset Address	Register Name	Total Reset Value
0x0B8	muxctrl_reg46	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							muxctrl_reg46
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg46	Multiplexing for the USB_PWREN pin. 0: GPIO5_1 1: USB_PWREN

muxctrl_reg47

muxctrl_reg47 is a multiplexing control register for the PWM_OUT0 pin.

Offset Address	Register Name	Total Reset Value
0x0BC	muxctrl_reg47	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							muxctrl_reg
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg47	Multiplexing for the PWM_OUT0 pin. 0: GPIO5_2 1: PWM_OUT0

muxctrl_reg48

muxctrl_reg48 is a multiplexing control register for the PWM_OUT1 pin.

Offset Address	Register Name	Total Reset Value
0x0C0	muxctrl_reg48	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							muxctrl_reg48
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg48	Multiplexing for the PWM_OUT1 pin. 0: GPIO5_3 1: PWM_OUT1

muxctrl_reg49

muxctrl_reg49 is a multiplexing control register for the IR_IN pin.

Offset Address	Register Name	Total Reset Value
0x0C4	muxctrl_reg49	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg49
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg49	Multiplexing for the IR_IN pin. 0: IR_IN 1: GPIO7_5

muxctrl_reg50

muxctrl_reg50 is a multiplexing control register for the NF_DQ0 pin.

Offset Address	Register Name	Total Reset Value
0x0C8	muxctrl_reg50	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg50
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg50	Multiplexing for the NF_DQ0 pin. 0: NF_DQ0 1: GPIO9_0

muxctrl_reg51

muxctrl_reg51 is a multiplexing control register for the NF_DQ1 pin.

Offset Address	Register Name	Total Reset Value
0x0CC	muxctrl_reg51	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg51
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg51	Multiplexing for the NF_DQ1 pin. 0: NF_DQ1 1: GPIO9_1

muxctrl_reg52

muxctrl_reg52 is a multiplexing control register for the NF_DQ2 pin.

Offset Address	Register Name	Total Reset Value
0x0D0	muxctrl_reg52	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg52
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg52	Multiplexing for the NF_DQ2 pin. 0: NF_DQ2 1: GPIO9_2

muxctrl_reg53

muxctrl_reg53 is a multiplexing control register for the NF_DQ3 pin.

Offset Address	Register Name	Total Reset Value
0x0D4	muxctrl_reg53	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg53	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg53	Multiplexing for the NF_DQ3 pin. 0: NF_DQ3 1: GPIO9_3

muxctrl_reg54

muxctrl_reg54 is a multiplexing control register for the NF_DQ4 pin.

Offset Address	Register Name	Total Reset Value
0x0D8	muxctrl_reg54	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg54	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg54	Multiplexing for the NF_DQ4 pin. 0: NF_DQ4 1: GPIO9_4

muxctrl_reg55

muxctrl_reg55 is a multiplexing control register for the NF_DQ5 pin.

Offset Address	Register Name	Total Reset Value
0x0DC	muxctrl_reg55	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg55
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg55	Multiplexing for the NF_DQ5 pin. 0: NF_DQ5 1: GPIO9_5

muxctrl_reg56

muxctrl_reg56 is a multiplexing control register for the NF_DQ6 pin.

Offset Address	Register Name	Total Reset Value
0x0E0	muxctrl_reg56	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg56
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg56	Multiplexing for the NF_DQ6 pin. 0: NF_DQ6 1: GPIO9_6

muxctrl_reg57

muxctrl_reg57 is a multiplexing control register for the NF_DQ7 pin.

Offset Address	Register Name	Total Reset Value
0x0E4	muxctrl_reg57	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg57
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg57	Multiplexing for the NF_DQ7 pin. 0: NF_DQ7 1: GPIO9_7

muxctrl_reg58

muxctrl_reg58 is a multiplexing control register for the NF_RDY0 pin.

Offset Address	Register Name	Total Reset Value
0x0E8	muxctrl_reg58	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg58
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg58	Multiplexing for the NF_RDY0 pin. 0: NF_RDY0 1: GPIO8_0

muxctrl_reg59

muxctrl_reg59 is a multiplexing control register for the NF_RDY1 pin.

Offset Address	Register Name	Total Reset Value
0x0EC	muxctrl_reg59	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg59
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg59	Multiplexing for the NF_RDY1 pin. 0: NF_RDY1 1: GPIO8_1

muxctrl_reg60

muxctrl_reg60 is a multiplexing control register for the NF_REN pin.

Offset Address	Register Name	Total Reset Value
0x0F0	muxctrl_reg60	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg60	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg60	Multiplexing for the NF_REN pin. 00: NF_REN 01: GPIO8_2 10: NF_BOOT_PIN0 Other values: reserved

muxctrl_reg61

muxctrl_reg61 is a multiplexing control register for the NF_CSN0 pin.

Offset Address	Register Name	Total Reset Value
0x0F4	muxctrl_reg61	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg61
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg61	Multiplexing for the NF_CSN0 pin. 0: NF_CSN0 1: GPIO8_3

muxctrl_reg62

muxctrl_reg62 is a multiplexing control register for the NF_CSN1 pin.

Offset Address	Register Name	Total Reset Value
0x0F8	muxctrl_reg62	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg6
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg62	Multiplexing for the NF_CSN1 pin. 0: NF_CSN1 1: GPIO8_4

muxctrl_reg63

muxctrl_reg63 is a multiplexing control register for the NF_CLE pin.

Offset Address	Register Name	Total Reset Value
0x0FC	muxctrl_reg63	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg63	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg63	Multiplexing for the NF_CLE pin. 00: NF_CLE 01: GPIO8_5 10: NF_BOOT_PIN1 Other values: reserved

muxctrl_reg64

muxctrl_reg64 is a multiplexing control register for the NF_ALE pin.

Offset Address	Register Name	Total Reset Value
0x100	muxctrl_reg64	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg64	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg64	Multiplexing for the NF_ALE pin. 00: NF_ALE 01: GPIO8_6 10: NF_BOOT_PIN2 Other values: reserved

muxctrl_reg65

muxctrl_reg65 is a multiplexing control register for the NF_WEN pin.

Offset Address	Register Name	Total Reset Value
0x104	muxctrl_reg65	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg65	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg65	Multiplexing for the NF_WEN pin. 00: NF_WEN 01: GPIO8_7 10: NF_BOOT_PIN3 Other values: reserved

muxctrl_reg66

muxctrl_reg66 is a multiplexing control register for the UART2_RXD pin.

Offset Address	Register Name	Total Reset Value
0x108	muxctrl_reg66	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg66
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg66	Multiplexing for the UART2_RXD pin. 0: GPIO7_6 1: UART2_RXD

muxctrl_reg67

muxctrl_reg67 is a multiplexing control register for the UART2_TXD pin.

Offset Address	Register Name	Total Reset Value
0x10C	muxctrl_reg67	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg6
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg67	Multiplexing for the UART2_TXD pin. 0: GPIO7_7 1: UART2_TXD

muxctrl_reg68

muxctrl_reg68 is a multiplexing control register for the SPI1_SCLK pin.

Offset Address	Register Name	Total Reset Value
0x110	muxctrl_reg68	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg6
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg68	Multiplexing for the SPI1_SCLK pin. 0: GPIO5_4 1: SPI1_SCLK

muxctrl_reg69

muxctrl_reg69 is a multiplexing control register for the SPI1_SDO pin.

Offset Address	Register Name	Total Reset Value
0x114	muxctrl_reg69	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg69
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg69	Multiplexing for the SPI1_SDO pin. 0: GPIO5_5 1: SPI1_SDO

muxctrl_reg70

muxctrl_reg70 is a multiplexing control register for the SPI1_SDI pin.

Offset Address	Register Name	Total Reset Value
0x118	muxctrl_reg70	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg70
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg70	Multiplexing for the SPI1_SDI pin. 0: GPIO5_6 1: SPI1_SDI

muxctrl_reg71

muxctrl_reg71 is a multiplexing control register for the SPI1_CSN pin.

Offset Address	Register Name	Total Reset Value
0x11C	muxctrl_reg71	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg71
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg71	Multiplexing for the SPI1_CSN pin. 0: GPIO5_7 1: SPI1_CSN

muxctrl_reg72

muxctrl_reg72 is a multiplexing control register for the JTAG_TRSTN pin.

Offset Address	Register Name	Total Reset Value
0x120	muxctrl_reg72	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg72
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg72	Multiplexing for the JTAG_TRSTN pin. 00: GPIO0_0 01: JTAG_TRSTN 10: TEMPER_DQ Other values: reserved

muxctrl_reg73

muxctrl_reg73 is a multiplexing control register for the JTAG_TCK pin.

Offset Address	Register Name	Total Reset Value
0x124	muxctrl_reg73	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg73	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg73	Multiplexing for the JTAG_TCK pin. 00: GPIO0_1 01: JTAG_TCK 10: TEMPER_DQ Other values: reserved

muxctrl_reg74

muxctrl_reg74 is a multiplexing control register for the JTAG_TMS pin.

Offset Address	Register Name	Total Reset Value
0x128	muxctrl_reg74	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg74	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg74	Multiplexing for the JTAG_TMS pin. 00: GPIO0_2 01: JTAG_TMS 10: TEMPER_DQ Other values: reserved

muxctrl_reg75

muxctrl_reg75 is a multiplexing control register for the JTAG_TDO pin.

Offset Address	Register Name	Total Reset Value
0x12C	muxctrl_reg75	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg75	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg75	Multiplexing for the JTAG_TDO pin. 00: GPIO0_3 01: JTAG_TDO 10: TEMPER_DQ Other values: reserved

muxctrl_reg76

muxctrl_reg76 is a multiplexing control register for the JTAG_TDI pin.

Offset Address	Register Name	Total Reset Value
0x130	muxctrl_reg76	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg76	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg76	Multiplexing for the JTAG_TDI pin. 00: GPIO0_4 01: JTAG_TDI 10: TEMPER_DQ Other values: reserved

muxctrl_reg77

muxctrl_reg77 is a multiplexing control register for the GPIO0_5 pin.

Offset Address	Register Name	Total Reset Value
0x134	muxctrl_reg77	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg77	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg77	Multiplexing for the GPIO0_5 pin. 00: SVB_PWM 01: GPIO0_5 10: TEMPER_DQ Other values: reserved

muxctrl_reg78

muxctrl_reg78 is a multiplexing control register for the GPIO0_6 pin.

Offset Address	Register Name	Total Reset Value
0x138	muxctrl_reg78	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg 78	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg78	Multiplexing for the GPIO0_6 pin. 00: GPIO0_6 01: SVB_PWM 10: TEMPER_DQ Other values: reserved

muxctrl_reg79

muxctrl_reg79 is a multiplexing control register for the GPIO0_7 pin.

Offset Address	Register Name	Total Reset Value
0x13C	muxctrl_reg79	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg79	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1:0]	RW	muxctrl_reg79	Multiplexing for the GPIO0_7 pin. 00: SYS_RSTN_OUT 01: GPIO0_7 10: TEMPER_DQ Other values: reserved

muxctrl_reg80

muxctrl_reg80 is a multiplexing control register for the VIU_CLK pin.

Offset Address	Register Name	Total Reset Value
0x140	muxctrl_reg80	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg80
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg80	Multiplexing for the VIU_CLK pin. 0: VIU_CLK 1: GPIO11_6

muxctrl_reg81

muxctrl_reg81 is a multiplexing control register for the VIU_VS pin.

Offset Address	Register Name	Total Reset Value
0x144	muxctrl_reg81	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg81
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg81	Multiplexing for the VIU_VS pin. 0: VIU_VS 1: GPIO11_5

muxctrl_reg82

muxctrl_reg82 is a multiplexing control register for the VIU_HS pin.

Offset Address	Register Name	Total Reset Value
0x148	muxctrl_reg82	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg82
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg82	Multiplexing for the VIU_HS pin. 0: VIU_HS 1: GPIO11_4

muxctrl_reg83

muxctrl_reg83 is a multiplexing control register for the VIU_DAT11 pin.

Offset Address	Register Name	Total Reset Value
0x14C	muxctrl_reg83	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg83
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg83	Multiplexing for the VIU_DAT11 pin. 0: VIU_DAT11 1: GPIO11_3

muxctrl_reg84

muxctrl_reg84 is a multiplexing control register for the VIU_DAT10 pin.

Offset Address	Register Name	Total Reset Value
0x150	muxctrl_reg84	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg84
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg84	Multiplexing for the VIU_DAT10 pin. 0: VIU_DAT10 1: GPIO11_2

muxctrl_reg85

muxctrl_reg85 is a multiplexing control register for the VIU_DAT9 pin.

Offset Address	Register Name	Total Reset Value
0x154	muxctrl_reg85	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg85
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg85	Multiplexing for the VIU_DAT9 pin. 0: VIU_DAT9 1: GPIO11_1

muxctrl_reg86

muxctrl_reg86 is a multiplexing control register for the VIU_DAT8 pin.

Offset Address	Register Name	Total Reset Value
0x158	muxctrl_reg86	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg86
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg86	Multiplexing for the VIU_DAT8 pin. 0: VIU_DAT8 1: GPIO11_0

muxctrl_reg87

muxctrl_reg87 is a multiplexing control register for the VIU_DAT7 pin.

Offset Address	Register Name	Total Reset Value
0x15C	muxctrl_reg87	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg87
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg87	Multiplexing for the VIU_DAT7 pin. 0: VIU_DAT7 1: GPIO10_7

muxctrl_reg88

muxctrl_reg88 is a multiplexing control register for the VIU_DAT6 pin.

Offset Address	Register Name	Total Reset Value
0x160	muxctrl_reg88	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg88
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg88	Multiplexing for the VIU_DAT6 pin. 0: VIU_DAT6 1: GPIO10_6

muxctrl_reg89

muxctrl_reg89 is a multiplexing control register for the VIU_DAT5 pin.

Offset Address	Register Name	Total Reset Value
0x164	muxctrl_reg89	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg89
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg89	Multiplexing for the VIU_DAT5 pin. 0: VIU_DAT5 1: GPIO10_5

muxctrl_reg90

muxctrl_reg90 is a multiplexing control register for the VIU_DAT4 pin.

Offset Address	Register Name	Total Reset Value
0x168	muxctrl_reg90	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg90
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg90	Multiplexing for the VIU_DAT4 pin. 0: VIU_DAT4 1: GPIO10_4

muxctrl_reg91

muxctrl_reg91 is a multiplexing control register for the VIU_DAT3 pin.

Offset Address	Register Name	Total Reset Value
0x16C	muxctrl_reg91	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							muxctrl_reg9
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg91	Multiplexing for the VIU_DAT3 pin. 0: VIU_DAT3 1: GPIO10_3

muxctrl_reg92

muxctrl_reg92 is a multiplexing control register for the VIU_DAT2 pin.

Offset Address	Register Name	Total Reset Value
0x170	muxctrl_reg92	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							muxctrl_reg92
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg92	Multiplexing for the VIU_DAT2 pin. 0: VIU_DAT2 1: GPIO10_2

muxctrl_reg93

muxctrl_reg93 is a multiplexing control register for the VIU_DAT1 pin.

Offset Address	Register Name	Total Reset Value
0x174	muxctrl_reg93	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg93
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg93	Multiplexing for the VIU_DAT1 pin. 0: VIU_DAT1 1: GPIO10_1

muxctrl_reg94

muxctrl_reg94 is a multiplexing control register for the VIU_DAT0 pin.

Offset Address	Register Name	Total Reset Value
0x178	muxctrl_reg94	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg9
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg94	Multiplexing for the VIU_DAT0 pin. 0: VIU_DAT0 1: GPIO10_0

2.4 Software Multiplexed Pins

VI

Table 2-34 lists the software multiplexed pins of the VI interface.

Table 2-34 Software multiplexed pins of the sensor

Pin Position	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
W10	SENSOR_CLK	muxctrl_reg2	GPIO1_2	SENSOR_CLK
V9	VIU_CLK	muxctrl_reg80	VIU_CLK	GPIO11_6
W5	VIU_VS	muxctrl_reg81	VIU_VS	GPIO11_5
V5	VIU_HS	muxctrl_reg82	VIU_HS	GPIO11_4
W9	VIU_DAT11	muxctrl_reg83	VIU_DAT11	GPIO11_3
W8	VIU_DAT10	muxctrl_reg84	VIU_DAT10	GPIO11_2
V8	VIU_DAT9	muxctrl_reg85	VIU_DAT9	GPIO11_1
U9	VIU_DAT8	muxctrl_reg86	VIU_DAT8	GPIO11_0
W7	VIU_DAT7	muxctrl_reg87	VIU_DAT7	GPIO10_7
V7	VIU_DAT6	muxctrl_reg88	VIU_DAT6	GPIO10_6
U8	VIU_DAT5	muxctrl_reg89	VIU_DAT5	GPIO10_5
W6	VIU_DAT4	muxctrl_reg90	VIU_DAT4	GPIO10_4
V6	VIU_DAT3	muxctrl_reg91	VIU_DAT3	GPIO10_3
U7	VIU_DAT2	muxctrl_reg92	VIU_DAT2	GPIO10_2
U6	VIU_DAT1	muxctrl_reg93	VIU_DAT1	GPIO10_1
T6	VIU_DAT0	muxctrl_reg94	VIU_DAT0	GPIO10_0

Table 2-35 describes the software multiplexed signals of the sensor.

Table 2-35 Software multiplexed signals of the sensor

Signal	Direction	Description
GPIO1_2	I/O	GPIO
GPIO10_0	I/O	GPIO
GPIO10_1	I/O	GPIO
GPIO10_2	I/O	GPIO
GPIO10_3	I/O	GPIO
GPIO10_4	I/O	GPIO
GPIO10_5	I/O	GPIO
GPIO10_6	I/O	GPIO
GPIO10_7	I/O	GPIO

Signal	Direction	Description
GPIO11_0	I/O	GPIO
GPIO11_1	I/O	GPIO
GPIO11_2	I/O	GPIO
GPIO11_3	I/O	GPIO
GPIO11_4	I/O	GPIO
GPIO11_5	I/O	GPIO
GPIO11_6	I/O	GPIO
SENSOR_CLK	O	Sensor working clock
VIU_CLK	I	VIU clock
VIU_DAT0	I	VIU data input
VIU_DAT1	I	VIU data input
VIU_DAT10	I	VIU data input
VIU_DAT11	I	VIU data input
VIU_DAT2	I	VIU data input
VIU_DAT3	I	VIU data input
VIU_DAT4	I	VIU data input
VIU_DAT5	I	VIU data input
VIU_DAT6	I	VIU data input
VIU_DAT7	I	VIU data input
VIU_DAT8	I	VIU data input
VIU_DAT9	I	VIU data input
VIU_HS	I	VIU horizontal sync, active high
VIU_VS	I	VIU vertical sync, active high

I²C

Table 2-36 lists the software multiplexed pins of the I²C interface.

Table 2-36 Software multiplexed pins of the I²C interface

Pin Position	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
W12	I2C_SDA	muxctrl_reg6	GPIO2_0	I2C_SDA

Pin Position	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
W13	I2C_SCL	muxctrl_reg7	GPIO2_1	I2C_SCL

Table 2-37 describes the software multiplexed signals of the I^2C interface.

Table 2-37 Software multiplexed signals of the I^2C interface

Signal	Direction	Description
GPIO2_0	I/O	GPIO
GPIO2_1	I/O	GPIO
I2C_SCL	I/O	I^2C bus clock, OD output
I2C_SDA	I/O	I^2C bus data/address, OD output

ETH

Table 2-38 lists the software multiplexed pins of the Ethernet (ETH) port.

Table 2-38 Software multiplexed pins of the ETH port

Pin Position	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2	Multiplexed Signal 3
B16	MII_CRS	muxctrl_reg12	GPIO3_0	MII_CRS	VOU1120_DATA10	None
A16	MII_COL	muxctrl_reg13	GPIO3_1	MII_COL	VOU1120_DATA9	None
D15	MII_RXD3	muxctrl_reg14	GPIO4_3	MII_RXD3	VOU1120_DATA15	None
A15	MII_RXD2	muxctrl_reg15	GPIO4_2	MII_RXD2	VOU1120_DATA11	None
D16	MII_RXD1	muxctrl_reg16	GPIO4_1	MII_RXD1	VOU1120_DATA8	None
C15	MII_RXD0	muxctrl_reg17	GPIO4_0	MII_RXD0	VOU1120_DATA12	None
C18	MII_TXD3	muxctrl_reg18	GPIO4_7	MII_TXD3	VOU1120_DATA3	None
D17	MII_TXD2	muxctrl_reg19	GPIO4_6	MII_TXD2	VOU1120_DATA13	None
B19	MII_TX	muxctrl_reg20	GPIO4_5	MII_TXD1	VOU1120_DATA0	None

Pin Position	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2	Multiplexed Signal 3
	D1					
B18	MII_TXD0	muxctrl_reg21	GPIO4_4	MII_TXD0	VOU1120_DATA4	None
D14	MII_RXCK	muxctrl_reg22	GPIO3_2	MII_RXCK	VOU1120_CLK	None
C17	MII_TXCK	muxctrl_reg23	GPIO3_3	MII_TXCK	VOU1120_DATA7	RMII_CLK
C19	MII_RXDV	muxctrl_reg24	GPIO3_4	MII_RXDV	VOU1120_DATA1	None
A18	MII_TXEN	muxctrl_reg25	GPIO3_5	MII_TXEN	VOU1120_DATA5	None
C16	MII_TXER	muxctrl_reg26	GPIO2_6	MII_TXER	None	None
B15	MII_RXER	muxctrl_reg27	GPIO2_7	MII_RXER	None	None
D18	EPHY_CLK	muxctrl_reg28	GPIO1_3	EPHY_CLK	VOU1120_DATA2	None
A17	MDCK	muxctrl_reg29	GPIO3_6	MDCK	VOU1120_DATA6	BOOT_SEL
A14	MDIO	muxctrl_reg30	GPIO3_7	MDIO	VOU1120_DATA14	None

Table 2-39 describes the software multiplexed signals of the ETH port.

Table 2-39 Software multiplexed signals of the ETH port

Signal	Direction	Description
BOOT_SEL	I	Storage medium select for booting. 0: storage space of the SPI flash 1: storage space of the NAND flash
EPHY_CLK	O	Working clock of the MII PHY
GPIO1_3	I/O	GPIO
GPIO2_6	I/O	GPIO
GPIO2_7	I/O	GPIO
GPIO3_0	I/O	GPIO
GPIO3_1	I/O	GPIO

Signal	Direction	Description
GPIO3_2	I/O	GPIO
GPIO3_3	I/O	GPIO
GPIO3_4	I/O	GPIO
GPIO3_5	I/O	GPIO
GPIO3_6	I/O	GPIO
GPIO3_7	I/O	GPIO
GPIO4_0	I/O	GPIO
GPIO4_1	I/O	GPIO
GPIO4_2	I/O	GPIO
GPIO4_3	I/O	GPIO
GPIO4_4	I/O	GPIO
GPIO4_5	I/O	GPIO
GPIO4_6	I/O	GPIO
GPIO4_7	I/O	GPIO
MDCK	O	MDIO clock output
MDIO	I/O	MDIO input/output
MII_COL	I	MII collision indicator
MII_CRS	I	MII carrier sense signal
MII_RXCK	I	MII RX clock
MII_RXD0	I	RMII or MII RX data
MII_RXD1	I	RMII or MII RX data
MII_RXD2	I	MII RX data
MII_RXD3	I	MII RX data
MII_RXDV	I	MII RX data validity indicator
MII_RXER	I	RX error. It indicates that the received data is incorrect, and the PHY can discard the data.
MII_TXCK	I	MII TX clock
MII_TXD0	O	RMII or MII TX data
MII_TXD1	O	RMII or MII TX data
MII_TXD2	O	MII TX data
MII_TXD3	O	MII TX data

Signal	Direction	Description
MII_TXEN	O	MII TX data enable
MII_TXER	O	TX error. It indicates that the received data is incorrect, and the PHY can discard the data.
RMII_CLK	I/O	RMII clock
VOU1120_CLK	O	BT.1120 clock output
VOU1120_DATA0	O	BT.1120 luminance signal output
VOU1120_DATA1	O	BT.1120 luminance signal output
VOU1120_DATA10	O	BT.1120 chrominance signal output
VOU1120_DATA11	O	BT.1120 chrominance signal output
VOU1120_DATA12	O	BT.1120 chrominance signal output
VOU1120_DATA13	O	BT.1120 chrominance signal output
VOU1120_DATA14	O	BT.1120 chrominance signal output
VOU1120_DATA15	O	BT.1120 chrominance signal output
VOU1120_DATA2	O	BT.1120 luminance signal output
VOU1120_DATA3	O	BT.1120 luminance signal output
VOU1120_DATA4	O	BT.1120 luminance signal output
VOU1120_DATA5	O	BT.1120 luminance signal output
VOU1120_DATA6	O	BT.1120 luminance signal output
VOU1120_DATA7	O	BT.1120 luminance signal output
VOU1120_DATA8	O	BT.1120 chrominance signal output
VOU1120_DATA9	O	BT.1120 chrominance signal output

FLASHLAMP

Table 2-40 lists the software multiplexed pin of the camera flash.

Table 2-40 Software multiplexed pin of the camera flash

Pin Position	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
V12	FLASH_TRIG	muxctrl_reg31	GPIO1_7	FLASH_TRIG

Table 2-41 describes the software multiplexed signals of the camera flash.

Table 2-41 Software multiplexed signals of the camera flash

Signal	Direction	Description
FLASH_TRIG	O	Camera flash control
GPIO1_7	I/O	GPIO

Shutter

Table 2-42 lists the software multiplexed pin of shutter.

Table 2-42 Software multiplexed pin of the shutter

Pin Position	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
U12	SHUTTER_TRIG	muxctrl_reg0	GPIO1_0	SHUTTER_TRIG

Table 2-43 describes the software multiplexed signals of the shutter.

Table 2-43 Software multiplexed signals of the shutter

Signal	Direction	Description
GPIO1_0	I/O	GPIO
SHUTTER_TRIG	O	Shutter control

SFC

Table 2-44 lists the software multiplexed pins of the SFC.

Table 2-44 Software multiplexed pins of the SFC

Pin Position	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2
F17	SFC_DIO	muxctrl_reg40	SFC_DIO	GPIO7_0	None
F16	SFC_WP_IO2	muxctrl_reg41	SFC_WP_IO2	GPIO7_1	None
E19	SFC_CLK	muxctrl_reg42	SFC_CLK	GPIO7_2	SFC_ADDR_MODE
E16	SFC_DOI	muxctrl_reg43	SFC_DOI	GPIO7_3	None
E17	SFC_HOLD_IO3	muxctrl_reg44	SFC_HOLD_IO3	GPIO7_4	None

Table 2-45 describes the software multiplexed signals of the SFC.

Table 2-45 Software multiplexed signals of the SFC

Signal	Direction	Description
GPIO7_0	I/O	GPIO
GPIO7_1	I/O	GPIO
GPIO7_2	I/O	GPIO
GPIO7_3	I/O	GPIO
GPIO7_4	I/O	GPIO
SFC_ADDR_MODE	I	Default address mode of the SFC. 0: 3-byte address mode 1: 4-byte address mode
SFC_CLK	O	Clock signal transmitted to the SPI flash. The high level or low level can be configured when the clock is not switched.
SFC_DIO	I/O	Data output signal in standard SPI mode Data I/O signal in dual-SPI mode Data I/O signal in quad-SPI mode
SFC_DOI	I/O	Data input signal in standard SPI mode Data I/O signal in dual-SPI mode Data I/O signal in quad-SPI mode
SFC_HOLD_IO3	I/O	Hold function in standard SPI mode, active low Hold function in dual-SPI mode, active low Data I/O signal in quad-SPI mode
SFC_WP_IO2	I/O	Write protection function in standard SPI mode, active low Write protection function in dual-SPI mode, active low Data I/O signal in quad-SPI mode

NFC

Table 2-46 lists the software multiplexed pins of the NFC.

Table 2-46 Software multiplexed pins of the NFC

Pin Position	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2
K3	NF_DQ0	muxctrl_reg50	NF_DQ0	GPIO9_0	None
K1	NF_DQ1	muxctrl_reg51	NF_DQ1	GPIO9_1	None
L3	NF_DQ2	muxctrl_reg52	NF_DQ2	GPIO9_2	None

Pin Position	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2
L2	NF_DQ3	muxctrl_reg53	NF_DQ3	GPIO9_3	None
L1	NF_DQ4	muxctrl_reg54	NF_DQ4	GPIO9_4	None
M1	NF_DQ5	muxctrl_reg55	NF_DQ5	GPIO9_5	None
M2	NF_DQ6	muxctrl_reg56	NF_DQ6	GPIO9_6	None
M3	NF_DQ7	muxctrl_reg57	NF_DQ7	GPIO9_7	None
N1	NF_RDY0	muxctrl_reg58	NF_RDY0	GPIO8_0	None
N2	NF_RDY1	muxctrl_reg59	NF_RDY1	GPIO8_1	None
P1	NF_REN	muxctrl_reg60	NF_REN	GPIO8_2	NF_BOOT_PIN0
P2	NF_CSN0	muxctrl_reg61	NF_CSN0	GPIO8_3	None
P3	NF_CSN1	muxctrl_reg62	NF_CSN1	GPIO8_4	None
R1	NF_CLE	muxctrl_reg63	NF_CLE	GPIO8_5	NF_BOOT_PIN1
R2	NF_ALE	muxctrl_reg64	NF_ALE	GPIO8_6	NF_BOOT_PIN2
N3	NF_WEN	muxctrl_reg65	NF_WEN	GPIO8_7	NF_BOOT_PIN3

Table 2-47 describes the software multiplexed signals of the NFC.

Table 2-47 Software multiplexed signals of the NFC

Signal	Direction	Description
GPIO8_0	I/O	GPIO
GPIO8_1	I/O	GPIO
GPIO8_2	I/O	GPIO
GPIO8_3	I/O	GPIO
GPIO8_4	I/O	GPIO
GPIO8_5	I/O	GPIO
GPIO8_6	I/O	GPIO
GPIO8_7	I/O	GPIO
GPIO9_0	I/O	GPIO
GPIO9_1	I/O	GPIO
GPIO9_2	I/O	GPIO
GPIO9_3	I/O	GPIO
GPIO9_4	I/O	GPIO

Signal	Direction	Description
GPIO9_5	I/O	GPIO
GPIO9_6	I/O	GPIO
GPIO9_7	I/O	GPIO
NF_ALE	O	Address latch signal of the NAND flash
NF_BOOT_PIN0	I	This signal is used to configure the NAND flash by working with NF_BOOT_PIN1, NF_BOOT_PIN2, and NF_BOOT_PIN3, and NF_BOOT_PIN4, and is valid only during power-on. The 5-bit signal is locked during power-on. Then the internal logic decodes this signal to obtain the parameter values of the NAND flash such as PAGE_SIZE, ECC_TYPE, BLOCK_SIZE, and ADDR_NUM. For details, see the *Hi3518 720p HD IP Camera SoC Data Sheet*. The page size is 2 KB, the ECC mode is 1-bit mode, the page/block is 64, and the NAND flash has five addresses by default.
NF_BOOT_PIN1	I	For details, see the description of NF_BOOT_PIN0.
NF_BOOT_PIN2	I	For details, see the description of NF_BOOT_PIN0.
NF_BOOT_PIN3	I	For details, see the description of NF_BOOT_PIN0.
NF_CLE	O	Command latch signal of the NAND flash
NF_CSN0	O	NAND flash CS, active low. This signal is used to mount the NAND flash for booting the system.
NF_CSN1	O	NAND flash CS, active low. This signal is used to mount the NAND flash for booting the system.
NF_DQ0	I/O	Data bus of the NAND flash
NF_DQ1	I/O	Data bus of the NAND flash
NF_DQ2	I/O	Data bus of the NAND flash
NF_DQ3	I/O	Data bus of the NAND flash
NF_DQ4	I/O	Data bus of the NAND flash
NF_DQ5	I/O	Data bus of the NAND flash
NF_DQ6	I/O	Data bus of the NAND flash
NF_DQ7	I/O	Data bus of the NAND flash
NF_RDY0	I	Status indicator of the NAND flash. 1: idle 0: busy
NF_RDY1	I	Status indicator of the NAND flash. 1: idle 0: busy

Signal	Direction	Description
NF_REN	O	Read enable signal of the NAND flash, active low
NF_WEN	O	Write enable signal of the NAND flash, active low

USB

Table 2-48 lists the software multiplexed pins of the USB port.

Table 2-48 Software multiplexed pins of the USB port

Pin Position	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
K17	USB_OVRCUR	muxctrl_reg45	GPIO5_0	USB_OVRCUR
J19	USB_PWREN	muxctrl_reg46	GPIO5_1	USB_PWREN

Table 2-49 describes the software multiplexed signals of the USB port.

Table 2-49 Software multiplexed signals of the USB port

Signal	Direction	Description
GPIO5_0	I/O	GPIO
GPIO5_1	I/O	GPIO
USB_OVRCUR	I	Over-current indicator signal of USB port 0, configurable level, and active high by default
USB_PWREN	O	Power control output of USB port 0, configurable level, and active low by default

PWM

Table 2-50 lists the software multiplexed pins of the PWM interface.

Table 2-50 Software multiplexed pins of the PWM interface

Pin Position	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
V15	PWM_OUT0	muxctrl_reg47	GPIO5_2	PWM_OUT0
W15	PWM_OUT1	muxctrl_reg48	GPIO5_3	PWM_OUT1

Table 2-51 describes the software multiplexed signals of the PWM interface.

Table 2-51 Software multiplexed signals of the PWM interface

Signal	Direction	Description
GPIO5_2	I/O	GPIO
GPIO5_3	I/O	GPIO
PWM_OUT0	O	PWM output 0
PWM_OUT1	O	PWM output 1

SDIO

Table 2-52 lists the software multiplexed pins of the SDIO interface.

Table 2-52 Software multiplexed pins of the SDIO interface

Pin Position	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signals 1–6
H18	SDIO_CCLK_OUT	muxctrl_reg1	GPIO1_1	1: SDIO_CCLK_OUT
J17	SDIO_CARD_DETECT	muxctrl_reg32	GPIO6_0	1: SDIO_CARD_DETECT
H19	SDIO_CARD_POWER_EN	muxctrl_reg33	GPIO6_1	1: SDIO_CARD_POWER_EN
H17	SDIO_CWPR	muxctrl_reg34	GPIO6_2	1: SDIO_CWPR
G19	SDIO_CCMD	muxctrl_reg35	GPIO6_3	1: SDIO_CCMD
G18	SDIO_CDATA0	muxctrl_reg36	GPIO6_4	1: SDIO_CDATA0 2: CLK_TEST_OUT0 3: CLK_TEST_OUT1 4: CLK_TEST_OUT2: 5: CLK_TEST_OUT3-
F19	SDIO_CDATA1	muxctrl_reg37	PLL_TEST_OUT0	1: SDIO_CDATA1 2: GPIO6_5 3: PLL_TEST_OUT1 4: PLL_TEST_OUT2 5: PLL_TEST_OUT3 6: RTC_TEST_CLK
G17	SDIO_CDATA2	muxctrl_reg38	GPIO6_6	1: SDIO_CDATA2
F18	SDIO_CDATA3	muxctrl_reg39	GPIO6_7	1: SDIO_CDATA3

Table 2-53 describes the software multiplexed signals of the SDIO interface.

Table 2-53 Software multiplexed signals of the SDIO interface

Signal	Direction	Description
CLK_TEST_OUT0	O	Main test clock output
CLK_TEST_OUT1	O	Main test clock output
CLK_TEST_OUT2	O	Main test clock output
CLK_TEST_OUT3	O	Main test clock output
GPIO1_1	I/O	GPIO
GPIO6_0	I/O	GPIO
GPIO6_1	I/O	GPIO
GPIO6_2	I/O	GPIO
GPIO6_3	I/O	GPIO
GPIO6_4	I/O	GPIO
GPIO6_5	I/O	GPIO
GPIO6_6	I/O	GPIO
GPIO6_7	I/O	GPIO
PLL_TEST_OUT0	O	PLL test clock output
PLL_TEST_OUT1	O	PLL test clock output
PLL_TEST_OUT2	O	PLL test clock output
PLL_TEST_OUT3	O	PLL test clock output
RTC_TEST_CLK	O	RTC test clock output
SDIO_CARD_DETECT	I	Card detection signal, active low
SDIO_CARD_POWER_EN	O	Power enable signal. The value 1 indicates power on.
SDIO_CCLK_OUT	O	Output working clock for the card
SDIO_CCMD	I/O	Card command
SDIO_CDATA0	I/O	Card data
SDIO_CDATA1	I/O	Card data
SDIO_CDATA2	I/O	Card data
SDIO_CDATA3	I/O	Card data
SDIO_CWPR	I	Card write protection detection

IR

Table 2-54 lists the software multiplexed pin of the IR interface.

Table 2-54 Software multiplexed pin of the IR interface

Pin Position	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
U13	IR_IN	muxctrl_reg49	IR_IN	GPIO7_5

Table 2-55 describes the software multiplexed signals of the IR interface.

Table 2-55 Software multiplexed signals of the IR interface

Signal	Direction	Description
GPIO7_5	I/O	GPIO
IR_IN	I	Infrared input

UART 1

Table 2-56 lists the software multiplexed pins of UART 1.

Table 2-56 Software multiplexed pins of UART 1

Pin Position	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
T16	UART1_RTSN	muxctrl_reg8	GPIO2_2	UART1_RTSN
V19	UART1_RXD	muxctrl_reg9	GPIO2_3	UART1_RXD
T17	UART1_CTSN	muxctrl_reg10	GPIO2_4	UART1_CTSN
U17	UART1_TXD	muxctrl_reg11	GPIO2_5	UART1_TXD

Table 2-57 describes the software multiplexed signals of UART 1.

Table 2-57 Software multiplexed signals of UART 1

Signal	Direction	Description
GPIO2_2	I/O	GPIO
GPIO2_3	I/O	GPIO
GPIO2_4	I/O	GPIO
GPIO2_5	I/O	GPIO

Signal	Direction	Description
UART1_CTSN	I	Modem state input: CTS, active low
UART1_RTSN	O	Modem state output: RTS, active low. The reset value is 0.
UART1_RXD	I	UART 1 RX data
UART1_TXD	O	UART 1 TX data

UART 2

Table 2-58 lists the software multiplexed pins of UART 2.

Table 2-58 Software multiplexed pins of UART 2

Pin Position	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
U18	UART2_RXD	muxctrl_reg66	GPIO7_6	UART2_RXD
U19	UART2_TXD	muxctrl_reg67	GPIO7_7	UART2_TXD

Table 2-59 describes the software multiplexed signals of UART 2.

Table 2-59 Software multiplexed signals of UART 2

Signal	Direction	Description
GPIO7_6	I/O	GPIO
GPIO7_7	I/O	GPIO
UART2_RXD	I	UART 2 RX data
UART2_TXD	O	UART 2 TX data

SPI 0

Table 2-60 lists the software multiplexed pins of SPI 0.

Table 2-60 Software multiplexed pins of SPI 0

Pin Position	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
V4	SPI0_SCLK	muxctrl_reg3	GPIO1_4	SPI0_SCLK
U5	SPI0_SDO	muxctrl_reg4	GPIO1_5	SPI0_SDO

Pin Position	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
T5	SPI0_SDI	muxctrl_reg5	GPIO1_6	SPI0_SDI

Table 2-61 describes the software multiplexed signals of SPI 0.

Table 2-61 Software multiplexed signals of SPI 0

Signal	Direction	Description
GPIO1_4	I/O	GPIO
GPIO1_5	I/O	GPIO
GPIO1_6	I/O	GPIO
SPI0_SCLK	I/O	SPI clock
SPI0_SDI	I	SPI data input
SPI0_SDO	O	SPI data output

SPI 1

Table 2-62 lists the software multiplexed pins of SPI 1.

Table 2-62 Software multiplexed pins of SPI 1

Pin Position	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
V11	SPI1_SCLK	muxctrl_reg68	GPIO5_4	SPI1_SCLK
W11	SPI1_SDO	muxctrl_reg69	GPIO5_5	SPI1_SDO
U11	SPI1_SDI	muxctrl_reg70	GPIO5_6	SPI1_SDI
U10	SPI1_CSN	muxctrl_reg71	GPIO5_7	SPI1_CSN

Table 2-63 describes the software multiplexed signals of SPI 1.

Table 2-63 Software multiplexed signals of SPI 1

Signal	Direction	Description
GPIO5_4	I/O	GPIO
GPIO5_5	I/O	GPIO
GPIO5_6	I/O	GPIO

Signal	Direction	Description
GPIO5_7	I/O	GPIO
SPI1_CSN	O	SPI CS 0 output
SPI1_SCLK	I/O	SPI clock
SPI1_SDI	I	SPI data input
SPI1_SDO	O	SPI data output

JTAG

Table 2-64 describes the software multiplexed pins of the JTAG interface.

Table 2-64 Software multiplexed pins of the JTAG interface

Pin Position	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2
U14	JTAG_TRSTN	muxctrl_reg72	GPIO0_0	JTAG_TRSTN	TEMPER_DQ
V16	JTAG_TCK	muxctrl_reg73	GPIO0_1	JTAG_TCK	TEMPER_DQ
T14	JTAG_TMS	muxctrl_reg74	GPIO0_2	JTAG_TMS	TEMPER_DQ
W16	JTAG_TDO	muxctrl_reg75	GPIO0_3	JTAG_TDO	TEMPER_DQ
W17	JTAG_TDI	muxctrl_reg76	GPIO0_4	JTAG_TDI	TEMPER_DQ

Table 2-65 describes the software multiplexed signals of the JTAG interface.

Table 2-65 Software multiplexed signals of the JTAG interface

Signal	Direction	Description
GPIO0_0	I/O	GPIO
GPIO0_1	I/O	GPIO
GPIO0_2	I/O	GPIO
GPIO0_3	I/O	GPIO
GPIO0_4	I/O	GPIO
JTAG_TCK	I	JTAG clock input
JTAG_TDI	I	JTAG data input
JTAG_TDO	O	JTAG data output

Signal	Direction	Description
JTAG_TMS	I	JTAG mode select input
JTAG_TRSTN	I	JTAG reset input
SYS_RSTN_OUT	O	System reset output
TEMPER_DQ	I/O	Temperature measurement. It is used to communicate with the external temperature measurement chip.

NOTE

The default function of the JTAG pin is selected by setting JTAG_EN (pull-up or pull-down).

- If JTAG_EN is 1'b0 (pull-down) during chip reset, the default function of the JTAG pin is GPIO. The function can be changed by configuring multiplexing control registers.
- If JTAG_EN is 1'b1 (pull-up) during chip reset, the default function of the JTAG pin is JTAG. The function can be changed by configuring multiplexing control registers.

GPIO

Table 2-66 lists the software multiplexed pins of the GPIO interface.

Table 2-66 Software multiplexed pins of the GPIO interface

Pin Position	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2
W18	GPIO0_5	muxctrl_reg77	SVB_PWM	GPIO0_5	TEMPER_DQ
T15	GPIO0_6	muxctrl_reg78	GPIO0_6	SVB_PWM	TEMPER_DQ
V18	GPIO0_7	muxctrl_reg79	SYS_RSTN_OUT	GPIO0_7	TEMPER_DQ

Table 2-67 describes the software multiplexed signals of the GPIO interface.

Table 2-67 Software multiplexed signals of the GPIO interface

Signal	Direction	Description
GPIO0_5	I/O	GPIO
GPIO0_6	I/O	GPIO
GPIO0_7	I/O	GPIO
SVB_PWM	O	SVB control signal output
SYS_RSTN_OUT	O	System reset output
TEMPER_DQ	I/O	Temperature measurement. It is used to communicate with the external temperature measurement chip.

2.5 Hardware Multiplexed Pins

SPI 0

Table 2-68 lists the hardware multiplexed pin of SPI 0.

Table 2-68 Hardware multiplexed pin of SPI 0

Pin Position	Pad Signal	Multiplexed Signal 1 (power_on == 1'b1)
W4	SPI0_CSN	NF_BOOT_PIN4

Table 2-69 describes the hardware multiplexed signal of SPI 0.

Table 2-69 Hardware multiplexed signal of SPI 0

Signal	Direction	Description
NF_BOOT_PIN4	I	This signal is used to configure the NAND flash by working with NF_BOOT_PIN0, NF_BOOT_PIN1, NF_BOOT_PIN2, and NF_BOOT_PIN3, and is valid only during power-on. For details, see the description of NF_BOOT_PIN0.

MDIO

Table 2-70 lists the hardware multiplexed pin of the MDIO interface.

Table 2-70 Hardware multiplexed pin of the MDIO interface

Pin Position	Pad Signal	Multiplexed Signal 1 (power_on == 1'b1)
A17	MDCK	BOOT_SEL

Table 2-71 describes the hardware multiplexed signal of the MDIO interface.

Table 2-71 Hardware multiplexed signal of the MDIO interface

Signal	Direction	Description
BOOT_SEL	I	Storage medium select for booting. 0: storage space of the SPI flash 1: storage space of the NAND flash

SFC

Table 2-72 lists the hardware multiplexed pin of the SFC.

Table 2-72 Hardware multiplexed pin of the SFC

Pin Position	Pad Signal	Multiplexed Signal 1 (power_on == 1'b1)
E19	SFC_CLK	SFC_ADDR_MODE

Table 2-73 describes the software multiplexed signal of the SFC.

Table 2-73 Hardware multiplexed signal of the SFC

Signal	Direction	Description
SFC_ADDR_MODE	I	Default address mode of the SFC. 0: 3-byte address mode 1: 4-byte address mode

NFC

Table 2-74 lists the hardware multiplexed pins of the NFC.

Table 2-74 Hardware multiplexed pins of the NFC

Pin Position	Pad Signal	Multiplexed Signal 1 (power_on == 1'b1)
P1	NF_REN	NF_BOOT_PIN0
R1	NF_CLE	NF_BOOT_PIN1
R2	NF_ALE	NF_BOOT_PIN2
N3	NF_WEN	NF_BOOT_PIN3

Table 2-75 describes the software multiplexed signals of the SFC.

Table 2-75 Hardware multiplexed signals of the SFC

Signal	Direction	Description
NF_BOOT_PIN0 NF_BOOT_PIN1 NF_BOOT_PIN2	I	NF_BOOT_PIN0, NF_BOOT_PIN1, NF_BOOT_PIN2, and NF_BOOT_PIN3 work together to configure the NAND flash. They are valid only during power-on.

Signal	Direction	Description
NF_BOOT_PIN3		Each signal is a 5-bit signal that is locked during power-on. Then the internal logic decodes this signal to obtain the parameter values of the NAND flash such as PAGE_SIZE, ECC_TYPE, BLOCK_SIZE, and ADDR_NUM. For details, see the *Hi3518 720p HD IP Camera SoC Data Sheet*. The page size is 2 KB, the ECC mode is 1-bit mode, the page/block is 64, and the NAND flash has five addresses by default.

2.6 Electrical Specifications

2.6.1 Power Consumption Specifications

Table 2-76 describes the power consumption specifications.

CAUTION

- The values for power consumption parameters are provided based on typical application scenarios.
- Design board power supplies by following the *Hi3518 Hardware Design User Guide*.

Table 2-76 Power consumption specifications

Type	Description	Typ	Max	Unit
Core power	Core power	None	None	mA
3.3V power	Interface power	None	None	mA
2.5V power	Interface power	None	None	mA
DVDD1518 power	Power supply of the DDR interface	None	None	mA

2.6.2 Temperature and Thermal Resistance Parameters

Table 2-77 describes the temperature and thermal resistance parameters.

NOTE

- The thermal resistance is provided in compliance with the JEDEC JESD51-2 standard. The actual system design and environment may be different.

- The chip junction temperature is proportional to the chip power consumption. Ensure that the junction temperature is appropriate to match power supplies.
- Design heat dissipation by following the *Hi3518 Hardware Design User Guide*.

Table 2-77 Hi3518A Temperature and thermal resistance parameters

Parameter	Symbol	Min	Typ	Max	Unit
Recommended ambient temperature	T_A	0	None	70	ºC
Limited junction temperature	T_{JMAX}	–20	None	110	ºC
Junction-to-ambient thermal resistance	θ_{JA}	None	27	None	ºC/W
Junction-to-board thermal resistance	θ_{JB}	None	10.7	None	ºC/W
Junction-to-case thermal resistance	θ_{JC}	None	6.9	None	ºC/W

2.6.3 Working Conditions

Table 2-78 describes the working conditions.

Table 2-78 Working conditions

Pin	Description	Min	Typ	Pin	Unit
DVDD12	Core power	-5%	1.2	+5%	V
DVDD33	I/O power	2.97	3.3	3.63	V
DVDD3318	I/O power	1.62	1.8	1.98	V
	I/O power	2.97	3.3	3.63	V
DDR_VDDQ	DDR2 I/O power	1.7	1.8	1.9	V
	DDR3 I/O power	1.425	1.5	1.575	V
DDR_REF0 DDR_REF1 DDR_REF2	DDR2/DDR3 reference voltage	0.49 x DDR_VDDQ	0.5 x DDR_VDDQ	0.51 x DDR_VDDQ	V
AVDD12_PLL	PLL digital power	1.08	1.2	1.32	V
AVDD33_PLL	PLL analog power	2.97	3.3	3.63	V
AVDD_ADC	SAR_ADC analog power	2.97	3.3	3.63	V
AVDD33_VDAC	VDAC analog power	2.97	3.3	3.63	V
AVDD_AC	Audio CODEC analog power	3	3.3	3.6	V

Pin	Description	Min	Typ	Pin	Unit
AVDD33_USB	USB analog power	–7%	3.3	+10%	V
AVDD33_USB25	USB analog power	–7%	3.3	+10%	V
AVDD_BAT	RTC battery power	1.6	3.0	3.0	V
AVDD33_RTC	RTC analog power	–10%	3.3	+10%	V

NOTE

AVDD33_VDAC is used only for the Hi3518A.

2.6.4 DC and AC Electrical Specifications

Table 2-79 and Table 2-80 describe the direct current (DC) electrical specifications.

Table 2-79 DC electrical specifications (DVDD33/DVDD33 = 3.3 V, incompatible with the 5 V input current)

Symbol	Description	Min	Typ	Max	Unit	Remarks
DVDD12	Core voltage	-5%	1.2	+5%	V	None
DVDD33 /DVDD3 318	Interface voltage	2.97	3.3	3.63	V	When DVDD3318 is 3.3 V, the I/O voltage of SPI0, VI, or sensor_clk is 3.3 V.
V_{IH}	Input high voltage	2.0	None	DVDD33 + 0.3	V	The interface is incompatible with the 5 V input current. The maximum voltage is (DVDD33 + 0.3) V.
V_{IL}	Input low voltage	–0.3	None	0.8	V	None
I_L	Input leakage current	None	None	±1	μA	None
I_{OZ}	Tristate output leakage current	None	None	±1	μA	None
V_{OH}	Output high voltage	2.4	None	None	V	None
V_{OL}	Output low voltage	None	None	0.4	V	None
R_{PU}	Internal pull-up resistor	33	41	62	kΩ	None
R_{PD}	Internal pull-down resistor	33	42	68	kΩ	None

Table 2-80 DC electrical specifications (DVDD3318 = 1.8 V)

Symbol	Description	Min	Typ	Max	Unit	Remarks
DVDD12	Core voltage	-5%	1.2	+5%	V	None
DVDD3318	Interface voltage	1.62	1.8	1.98	V	When DVDD3318 is 1.8 V, the I/O voltage of SPI0, VI, or sensor_clk is 1.8 V.
V_{IH}	Input high voltage	0.65 x DVDD3318	None	DVDD3318 + 0.3	V	None
V_{IL}	Input low voltage	–0.3	None	0.35 x DVDD3318	V	None
I_L	Input leakage current	None	None	±1	μA	None
I_{OZ}	Tristate output leakage current	None	None	±1	μA	None
V_{OH}	Output high voltage	DVDD3318 – 0.45	None	None	V	None
V_{OL}	Output low voltage	None	None	0.45	V	None
R_{PU}	Internal pull-up resistor	67	93	152	kΩ	None
R_{PD}	Internal pull-down resistor	64	92	170	kΩ	None

Table 2-81 describes the DC electrical specifications in DDR2 mode.

Table 2-81 DC electrical specifications in DDR2 SSTL18 mode (DDR_VDDQ = 1.8 V)

Symbol	Description	Min	Typ	Max	Unit	Remarks
DDR_VDDQ	Interface voltage	1.7	1.8	1.9	V	None
DDR_VREF	Reference voltage	0.49 x VDDQ	0.5 x VDDQ	0.51 x VDDQ	V	None
VTT	Termination voltage	DDR_VREF – 40	DDR_VREF	DDR_VREF + 40	mV	None
$V_{IH(DC)}$	Input high voltage	DDR_VREF +0.125	None	VDDQ + 0.3	V	None
$V_{IL(DC)}$	Input low voltage	–0.3	None	DDR_VREF – 0.125	V	None
V_{OH}	Output high voltage	VDDQ – 0.28	None	None	V	None

Symbol	Description	Min	Typ	Max	Unit	Remarks
V_{OL}	Output low voltage	None	None	VDDQ + 0.28	V	None
I_{OH}	Output high current	None	8.21	9.43	mA	The values are provided when the DDR drive impedance is 40 Ω and RTT is 75 Ω.
I_{OL}	Output low current	None	8.21	9.43	mA	The values are provided when the DDR drive impedance is 40 Ω and RTT is 75 Ω.

Table 2-82 describes the alternating current (AC) electrical specifications in DDR2 mode.

Table 2-82 AC electrical specifications in DDR2 mode (DDR_VDDQ = 1.8 V)

Symbol	Description	400–1067 Mbit/s		Unit
		Min	Max	
$V_{IH(AC)}$	AC input high voltage	DDR_VREF + 0.25	None	V
$V_{IL(AC)}$	AC input low voltage	None	DDR_VREF – 0.25	V

Table 2-83 describes the DC electrical specifications in DDR3 mode.

Table 2-83 DC electrical specifications in DDR3 SSTL15 mode (DDR_VDDQ = 1.5 V)

Symbol	Description	Min	Typ	Max	Unit	Remarks
DDR_VDDQ	Interface voltage	1.425	1.5	1.575	V	None
DDR_VREF	Reference voltage	0.49 x VDDQ	0.5 x VDDQ	0.51 x VDDQ	V	None
VTT	Termination voltage	DDR_VREF – 40	DDR_VREF	DDR_VREF + 40	mV	None
$V_{IH(DC)}$	Input high voltage	DDR_VREF + 0.1	None	VDDQ	V	None
$V_{IL(DC)}$	Input low voltage	–0.3	None	DDR_VREF – 0.1	V	None
V_{OH}	Output high voltage	VDDQ x 0.8	None	None	V	None

Symbol	Description	Min	Typ	Max	Unit	Remarks
V_{OL}	Output low voltage	None	None	0.2 x VDDQ	V	None
I_{OH}	Output high current	None	8.5	9.54	mA	The values are provided when the DDR drive impedance is 34 Ω and RTT is 60 Ω.
I_{OL}	Output low current	None	8.5	9.54	mA	The values are provided when the DDR drive impedance is 34 Ω and RTT is 60 Ω.

Table 2-84 describes the AC electrical specifications in DDR3 mode.

Table 2-84 AC electrical specifications in DDR3 mode (DDR_VDDQ = 1.5 V)

Symbol	Description	Min	Max	Unit
$V_{IH(AC)}$	Input high voltage	DDR_VREF + 0.175	None	V
$V_{IL(AC)}$	Input low voltage	None	DDR_VREF – 0.175	V

2.6.5 Power-On and Power-Off Sequence

To avoid over-current for I/O pins during power-on, you are advised to power on DVDD33 and DVDD12 in sequence. There is no requirement on the power-off sequence.

2.7 PCB Design Recommendations

For details about the printed circuit board (PCB) design, see the *Hi3518 Hardware Design User Guide*.

2.8 Interface Timings

2.8.1 DDR Interface Timings

2.8.1.1 Write Timings

Write Timings of dqs_out Relative to dq_out

In the write timing of dqs_out relative to dq_out, the major parameters are tDS and tDH. In DDR2-800, the value of tDS is 0.05 ns, and the value of tDH is 0.125 ns.

Figure 2-9 Write timing of dqs_out relative to dq_out for the DDR2

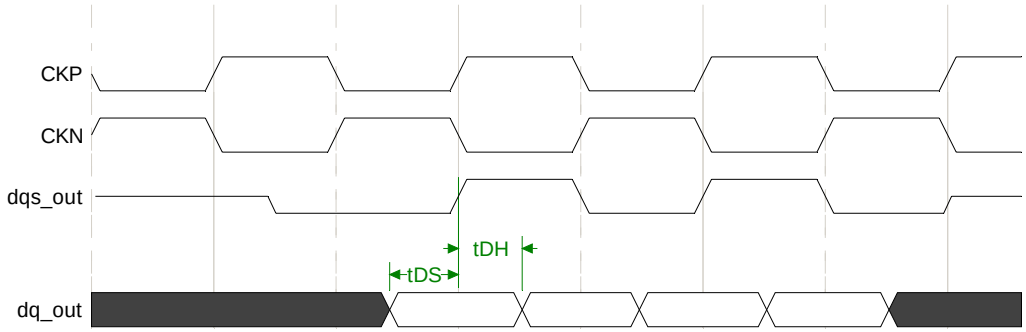
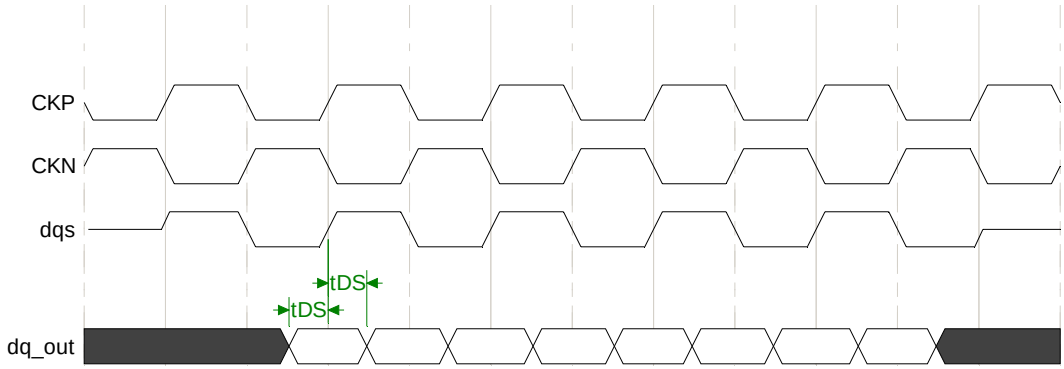


Figure 2-10 Write timing of dqs_out relative to dq_out for the DDR3



Write Timings of dqs_out Relative to CK

Figure 2-11 shows the write timing of dqs_out relative to CK for the DDR2, and Figure 2-12 shows the write timing of dqs_out relative to CK for the DDR3.

Figure 2-11 Write timing of dqs_out relative to CK for the DDR2

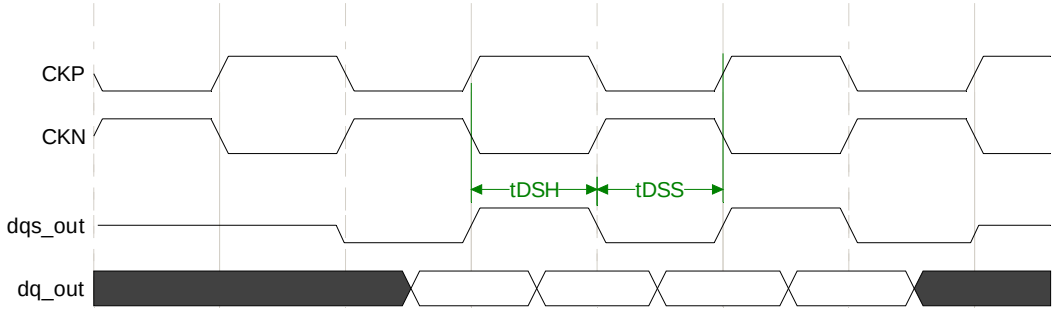
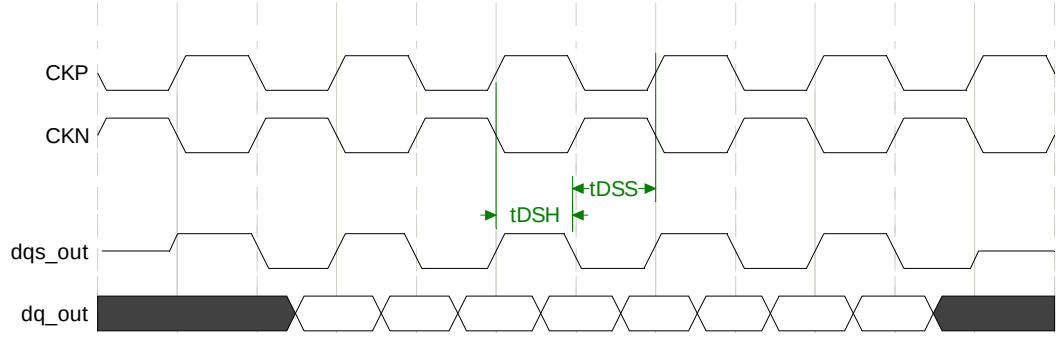


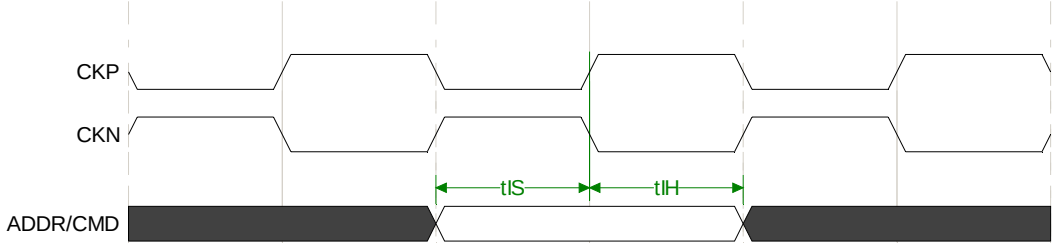
Figure 2-12 Write timing of dqs_out relative to CK for the DDR3



Write Timing of CMD/ADDR Relative to CK

Figure 2-13 shows the write timing of CMD/ADDR relative to CK.

Figure 2-13 Write timing of CMD/ADDR relative to CK



2.8.1.2 Read Timings

Read Timing of CMD/ADDR Relative to CK

The read timing of CMD/ADDR relative to CK is the same as the "Write Timing of CMD/ADDR Relative to CK".

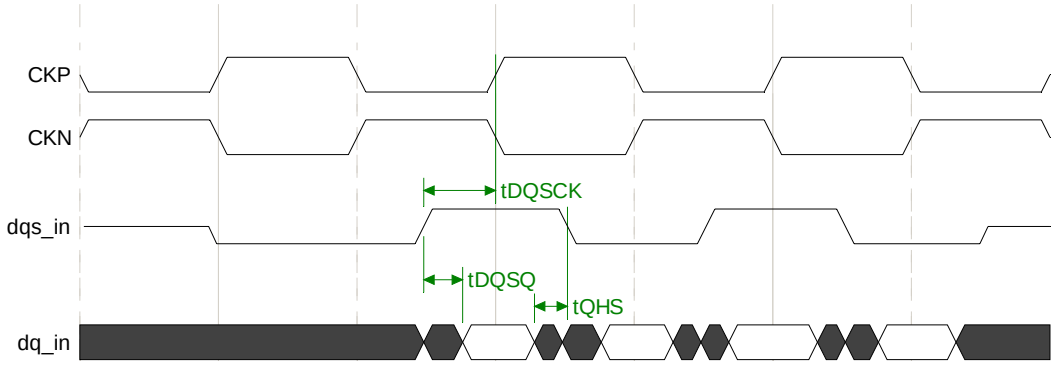
Read Timings of dqs_in Relative to dq_in

The read timings of dqs_in relative to dq_in are classified into the DDRn SDRAM output timing, dqs_in timing on the DDR PHY side, and dq_in timing on the DDR PHY side.

For the DDR SDRAM output timing, the phases of DQS and CK are the same in the ideal condition; however, there is a tDQSCK skew between DQS and CK. The value of tDQSCK is 0.35 ns. tDQSQ is the jitter of the last valid DQ relative to DQS and its value is 0.2 ns; tQHS is the jitter of the first valid DQ relative to DQS and its value is 0.3 ns.

Figure 2-14 shows the output timing of the DDRn SDRAM.

Figure 2-14 Output timing of the DDRn SDRAM



2.8.1.3 Timing Parameters

The timings of the DDR interface comply with the JEDEC standards including JESD79-2E and JESD79-3B standards. All the timings in this document are output on the DDR PHY side.

The Hi3518 is based on the timing parameters of the DDR2-800 and DDR3-1066 SDRAMs.

Table 2-85 and Table 2-86 describe the clock parameters of the DDR2-800 SDRAM.

Table 2-87 and Table 2-88 describe the clock parameters of the DDR3-1066 SDRAM.

Table 2-85 DDR2 clock parameters

Parameter	Typ	Unit
DDR clock frequency	400.00	MHz
PLL jitter	0.200	ns
PLL duty ratio	48.000	%
Clock skew	0.100	ns

Table 2-86 describes the parameters of the DDR2 SDRAM.

Table 2-86 Parameters for the DDR2-800 SDRAM

Parameter	Symbol	Typ	Unit
Setup time, DQS falling edge to DDR clock	tDSS	0.2	tCK
Hold time, DQS falling edge to DDR clock	tDSH	0.2	tCK
Setup time, DQ/DM to DQS	tDS	0.050	ns
Hold time, DQ/DM to DQS	tDH	0.125	ns
Skew between DQS and DQ	tDQSQ	0.200	ns
Data hold skew	tQHS	0.300	ns
Setup time, ADDR/CMD to DDR clock	tIS	0.175	ns
Hold time, ADDR/CMD to DDR clock	tIH	0.250	ns
Skew of DQS (output) to DDR clock	tDQSCK	0.350	ns

NOTE

For details about some timing parameters, see the following timing diagrams.

Table 2-87 DDR3 clock parameters

Parameter	Typ	Unit
DDR clock frequency	600.00	MHz
PLL jitter	0.200	ns
PLL duty ratio	47.000	%
Clock skew	0.100	ns

Table 2-88 Parameters for the DDR3-1066 SDRAM

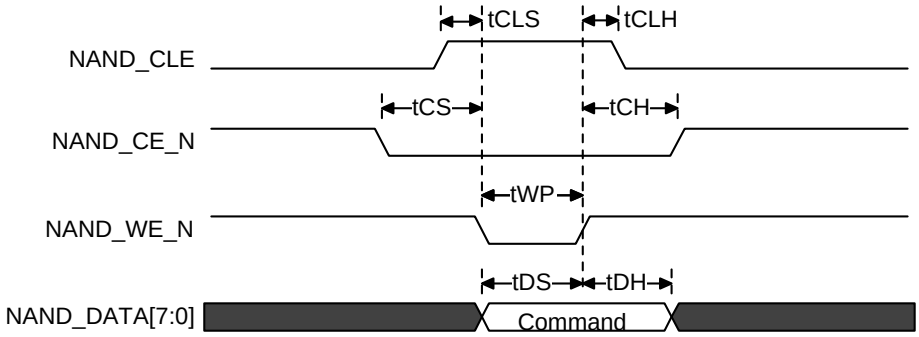
Parameter	Symbol	Typ	Unit
Setup time, DQS falling edge to DDR clock	tDSS	0.2	tCK
Hold time, DQS falling edge to DDR clock	tDSH	0.2	tCK
Setup time, DQ/DM to DQS	tDS	0.025	ns
Hold time, DQ/DM to DQS	tDH	0.100	ns
Skew between DQS and DQ	tDQSQ	0.150	ns
Setup time, ADDR/CMD to DDR clock	tIS	0.125	ns
Hold time, ADDR/CMD to DDR clock	tIH	0.200	ns
Skew of DQS (output) to DDR clock	tDQSCK	0.300	ns

2.8.2 NANDC Interface Timings

Command Cycle Timing

Figure 2-15 shows the NANDC command cycle timing.

Figure 2-15 NANDC command cycle timing



NOTE

The level widths of NAND_WE_N and NAND_RE_N can be set by configuring the NF_PULSE_WIDTH register of the NANDC. Some parameters in the timing diagrams of the NANDC interface vary depending on the settings of NF_PULSE_WIDTH. In the following tables, these parameters are marked with "Configurable."

Table 2-89 describes NANDC command cycle timing parameters.

Table 2-89 NANDC command cycle timing parameters

Parameter	Symbol	Mim	Max	Unit	Remarks
Setup time of NAND_CLE	tCLS	0	None	ns	None
Hold time of NAND_CLE	tCLH	10	None	ns	Configurable
Setup time of NAND_CE_N	tCS	0	None	ns	None
Hold time of NAND_CE_N	tCH	10	None	ns	Configurable
Pulse width of NAND_WE_N	tWP	15	None	ns	Configurable
Data setup time	tDS	10	None	ns	Configurable
Data hold time	tDH	10	None	ns	Configurable

Address Cycle Timing

Figure 2-16 shows the NANDC address cycle timing.

Figure 2-16 NANDC address cycle timing

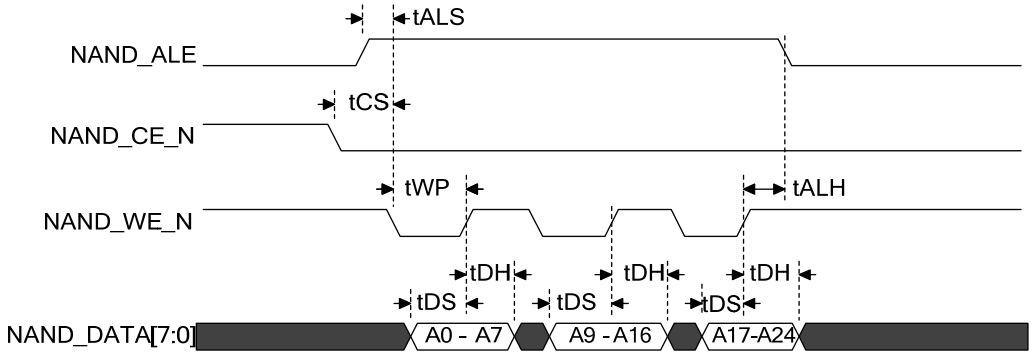


Table 2-90 describes the NANDC address cycle timing parameters.

Table 2-90 NANDC address cycle timing parameters

Parameter	Symbol	Mim	Max	Unit	Remarks
Setup time of NAND_CE_N	tCS	0	None	ns	None
Pulse width of NAND_WE_N	tWP	15	None	ns	Configurable
Setup time of NAND_ALE	tALS	0	None	ns	None
Hold time of NAND_ALE	tALH	10	None	ns	Configurable
Data setup time	tDS	10	None	ns	Configurable
Data hold time	tDH	10	None	ns	Configurable

Write Data Timing

Figure 2-17 shows the NANDC write data timing.

Figure 2-17 NANDC write data timing

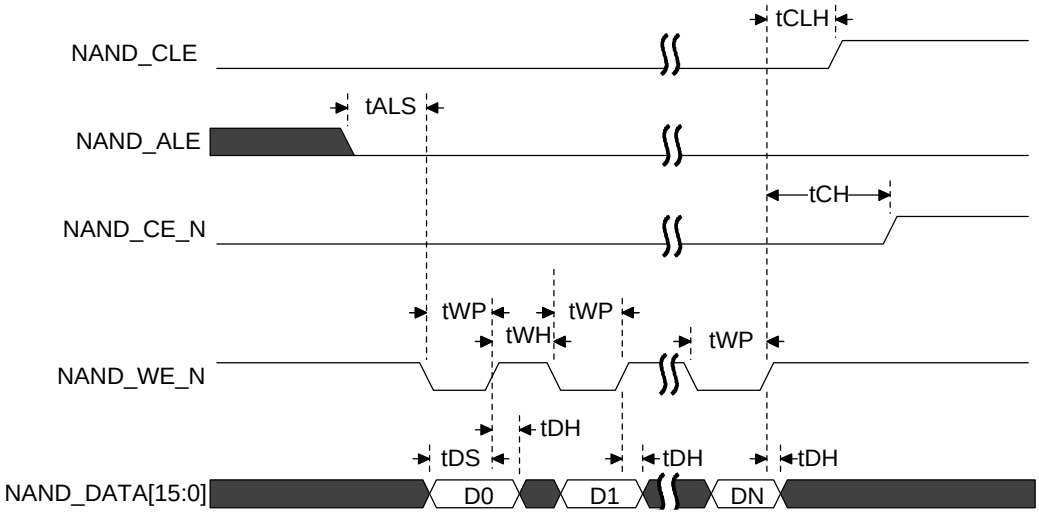


Table 2-91 describes the NANDC write data timing parameters.

Table 2-91 NANDC write data timing parameters

Parameter	Symbol	Min	Max	Unit	Remarks
Hold time of NAND_CLE	tCLH	10	None	ns	Configurable
Hold time of NAND_CE_N	tCH	10	None	ns	Configurable
Pulse width of NAND_WE_N	tWP	15	None	ns	Configurable
Setup time of NAND_ALE	tALS	0	None	ns	Configurable
Data setup time	tDS	10	None	ns	Configurable
Data hold time	tDH	10	None	ns	Configurable
High-level hold time of NAND_WE_N	tWH	15	None	ns	Configurable

Read Data Timing

Figure 2-18 shows the NANDC read data timing.

Figure 2-18 NANDC read data timing

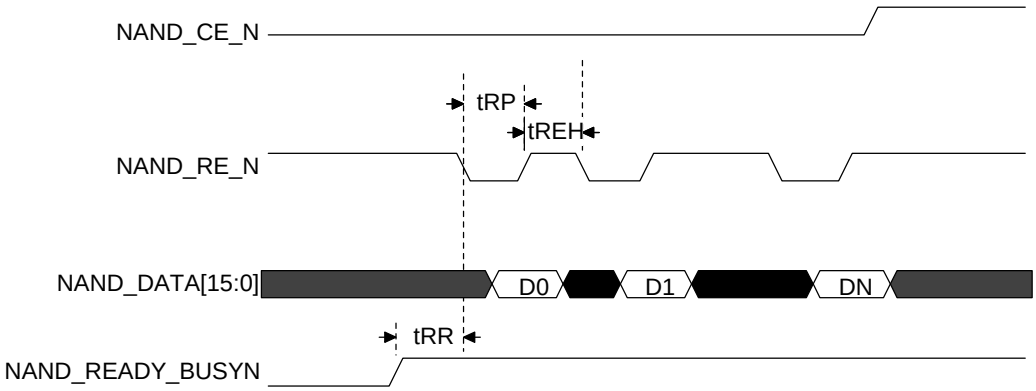


Table 2-92 describes the NANDC read data timing parameters.

Table 2-92 NANDC read data timing parameters

Parameter	Symbol	Min	Max	Unit	Remarks
Low-level wait time of NAND_RE_N	tRR	15	-	ns	Configurable
Pulse width of NAND_RE_N	tRP	15	-	ns	Configurable
High-level width of NAND_RE_N	tREH	15	-	ns	Configurable

NOTE

The tRR delay is configurable.

2.8.3 SFC Interface Timings

Figure 2-19 shows the SFC input timing.

Figure 2-19 SFC input timing

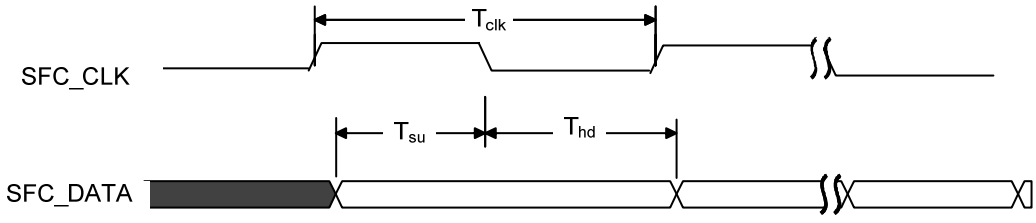


Table 2-93 describes the SFC input timing parameters.

Table 2-93 SFC input timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
Clock cycle of SFC_CLK	T_{clk}	16	None	83.2	ns

Parameter	Symbol	Min	Typ	Max	Unit
Input signal setup time	T_{su}	8	None	None	ns
Input signal hold time	T_{hd}	1.2	None	None	ns

Figure 2-20 shows the SFC output timing.

Figure 2-20 SFC output timing

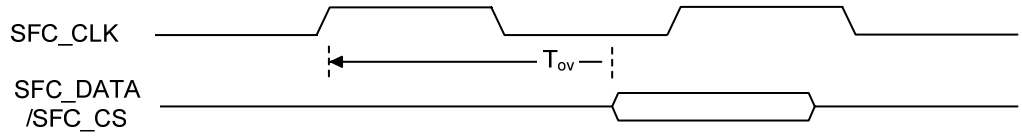


Table 2-94 describes the SFC output timing parameters.

Table 2-94 SFC output timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
Clock cycle of SFCCLK	T	16	None	83.2	ns
Output data signal delay	T_{ov}	–5	None	3.0	ns
Output CS signal delay	T_{ov}	–5	None	3.0	ns

2.8.4 Ethernet MAC Port Timings

MII Timings

The Hi3518 provides standard MIIs that comply with the MII timing standard. These interfaces are used to connect to the physical layer (PHY).

Figure 2-21 shows the 100 Mbit/s RX timing of the MII.

Figure 2-21 100 Mbit/s RX timing of the MII

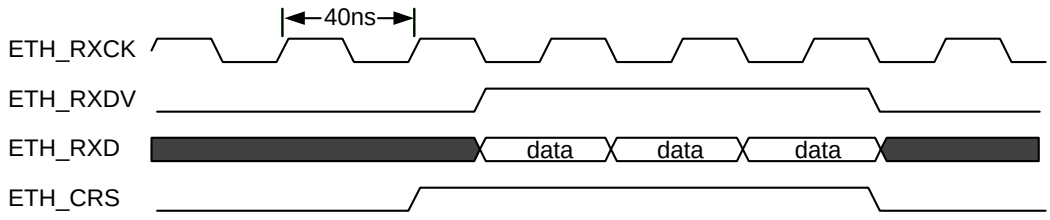


Figure 2-22 shows the 100 Mbit/s TX timing of the MII.

Figure 2-22 100 Mbit/s TX timing of the MII

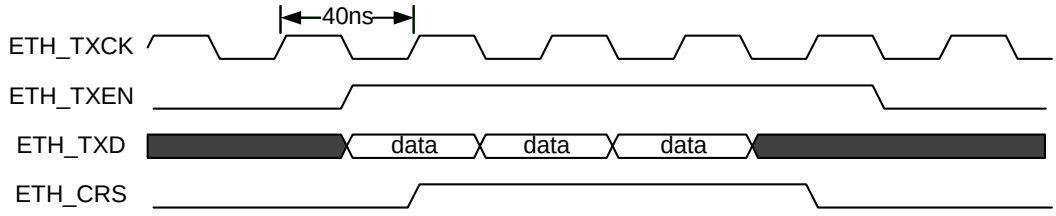


Figure 2-23 shows the 10 Mbit/s RX timing of the MII.

Figure 2-23 10 Mbit/s RX timing of the MII

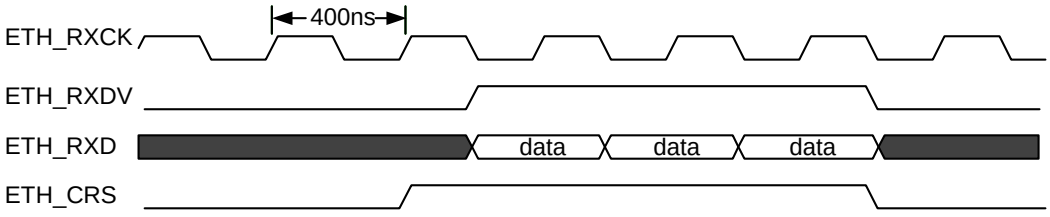


Figure 2-24 shows the 10 Mbit/s TX timing of the MII.

Figure 2-24 10 Mbit/s TX timing of the MII

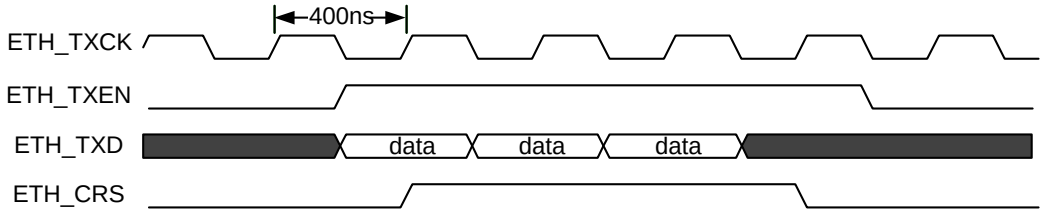


Figure 2-25 shows the RX timing parameters of the MII.

Figure 2-25 RX timing parameters of the MII

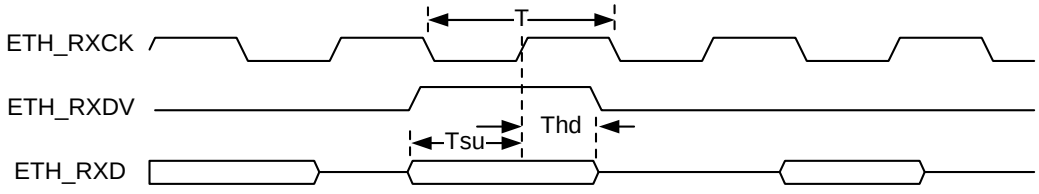


Figure 2-26 shows the TX timing parameters of the MII.

Figure 2-26 TX timing parameters of the MII

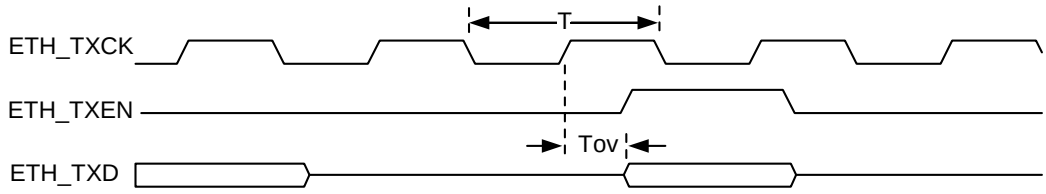


Table 2-95 describes the MII timing parameters.

Table 2-95 MII timing parameters

Parameter	Symbol	Signal	Min	Max	Unit
MII clock cycle MII signal setup time	T	RXCK、TXCK	400(10Mbit/s)	400	ns
			40(10Mbit/s)	40	
MII signal hold time	Tsu（RX）	RXER、RXDV、RXD[3:0]	6	None	ns
MII output signal delay	Thd（RX）	RXER、RXDV、RXD[3:0]	2	None	ns
MII clock cycle	Tov（MIITX）	TXD[3:0]、TXEN	2	8	ns

RMII Timings

Figure 2-27 shows the 100 Mbit/s RX timing of the RMII.

Figure 2-27 100 Mbit/s RX timing of the RMII

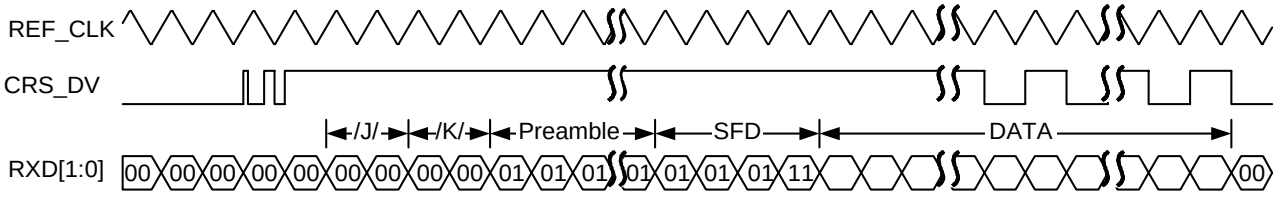


Figure 2-28 shows the 100 Mbit/s TX timing of the RMII interface.

Figure 2-28 100 Mbit/s TX timing of the RMII

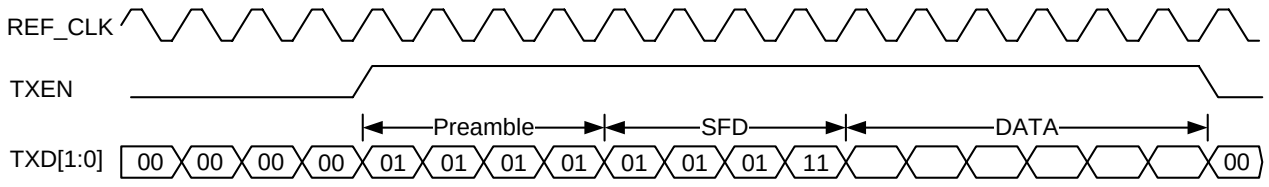


Figure 2-29 shows the 10 Mbit/s RX timing of the RMII.

Figure 2-29 10 Mbit/s RX timing of the RMII

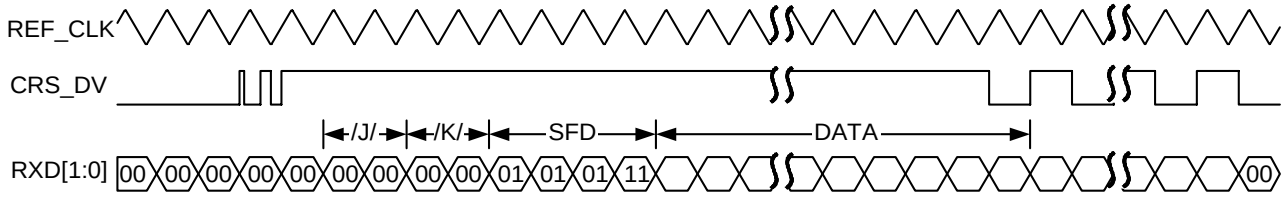


Figure 2-30 shows the 10 Mbit/s TX timing of the RMII.

Figure 2-30 10 Mbit/s TX timing of the RMII

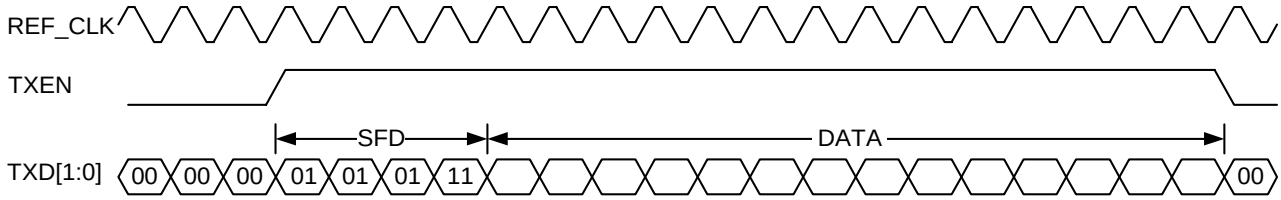


Figure 2-31 shows the timing parameters of the RMII.

Figure 2-31 Timing parameters of the RMII

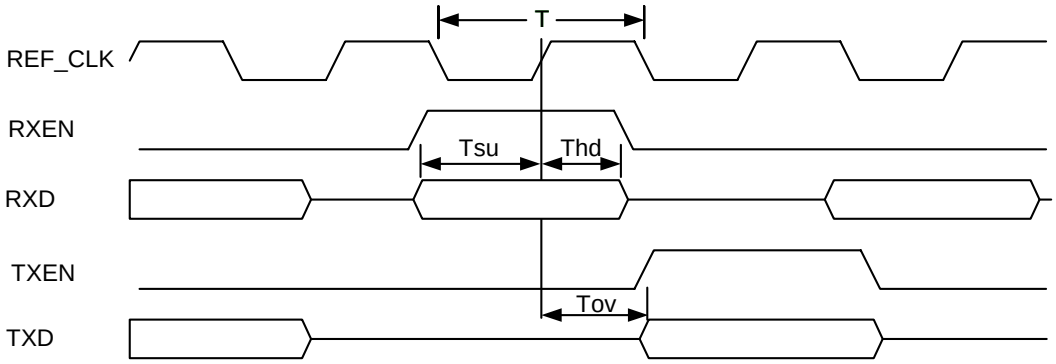


Table 2-96 describes the timing parameters of the RMII.

Table 2-96 Timing parameters of the RMII

Parameter	Symbol	Signal	Min	Max	Unit
Setup time of RMII signal	Tsu (RX)	CRS_DV/RXD[1:0]	4	None	ns
Hold time of RMII signal	Thd (RX)	CRS_DV/RXD[1:0]	2	None	ns
RMII output signal delay	Tov （RMIITX）	TXEN/TXD[1:0]	2	16	ns

MDIO Interface Timings

Figure 2-32 shows the read timing of the MDIO interface.

Figure 2-32 Read timing of the MDIO interface

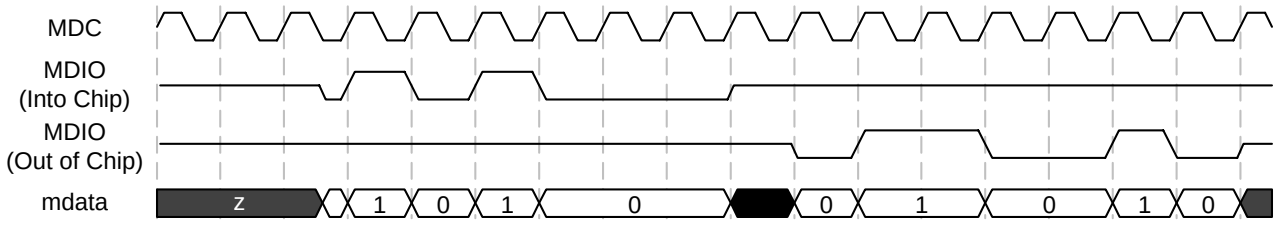


Figure 2-33 shows the write timing of the MDIO interface.

Figure 2-33 Write timing of the MDIO interface

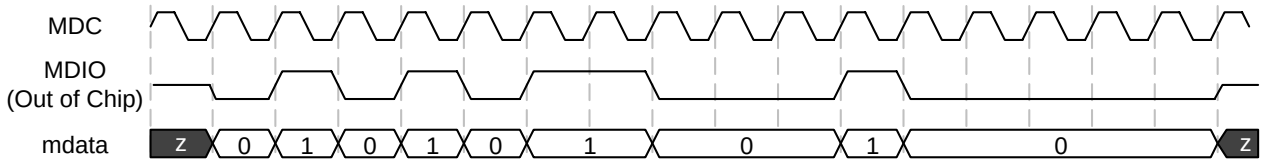


Figure 2-34 shows the RX timing parameters of the MDIO interface.

Figure 2-34 RX timing parameters of the MDIO interface

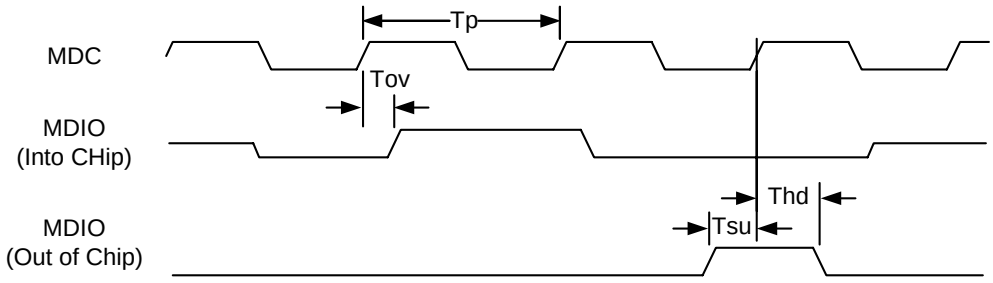


Table 2-97 describes the timing parameters of the MDIO interface.

Table 2-97 Timing parameters of the MDIO interface

Parameter	Symbol	Signal	Min	Max	Unit
MDIO data RX delay	Tov	MDIO	166	20833	ns
MDIO clock cycle	Tp	MDCK	333	41667	ns
MDIO data TX setup time	Tsu	MDIO	10	None	ns
MDIO data TX hold time	Thd	MDIO	10	None	ns

NOTE

The MDC clock cycle Tp can be changed by adjusting the MDC frequency (MDIO_RWCTRL[frq_dv]). To be specific, you can divide the frequency 150 MHz of the ETH working clock by 100, 50, or other values. Tov is related to the clock cycle Tp of the MDC, and its value is about Tmdc/2.

2.8.5 VI Interface Timing

The VI clock is supplied externally. All the VI interfaces are input interfaces in slave mode.

Figure 2-35 shows the VI interface timing.

Figure 2-35 VI interface timing

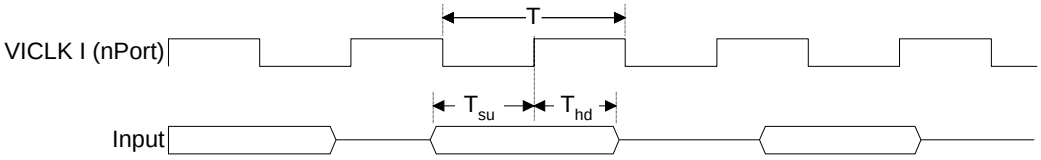


Table 2-98 describes the VI interface timing parameters.

Table 2-98 VI interface timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
VICLK clock cycle	T	13.48	-	-	ns
Input signal setup time	T_{su}	2.5	-	-	ns
Input signal hold time	T_{hd}	2.0	-	-	ns

2.8.6 VO Interface Timing

Figure 2-36 shows the VO interface timing.

Figure 2-36 VO interface timing

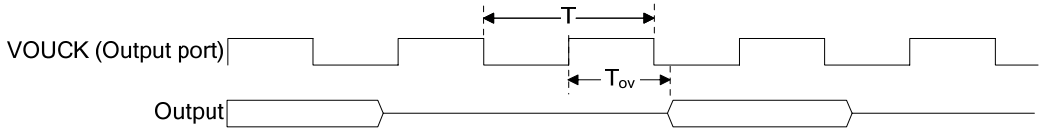


Table 2-99 describes the VO interface timing parameters.

Table 2-99 VO interface timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
VOCLK clock cycle	T	None	None	13.48	ns
Output signal delay	T_{ov}	3.5	None	8.8	ns

2.8.7 SIO Interface Timings

Figure 2-37 shows the I²S interface RX timing.

Figure 2-37 I²S interface RX timing

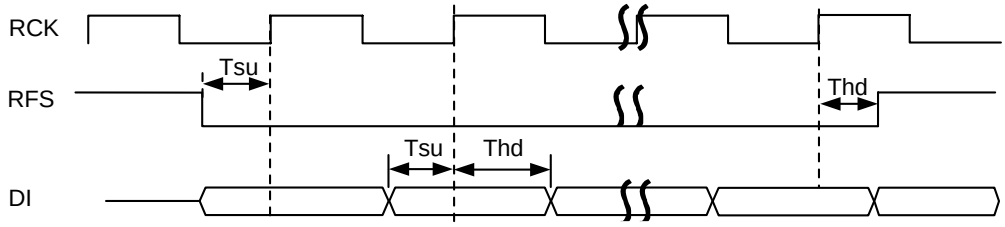


Figure 2-38 shows the I²S interface TX timing.

Figure 2-38 I²S interface TX timing

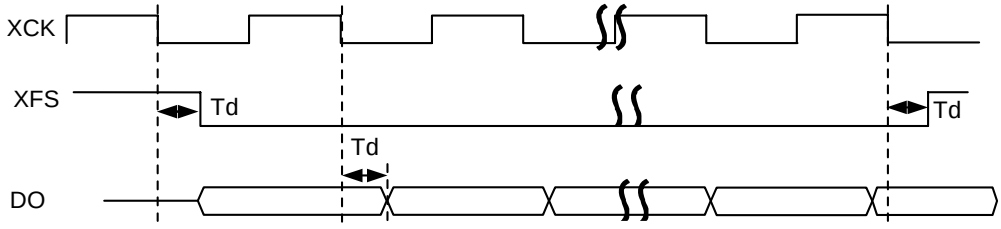


Table 2-100 describes the I²S interface timing parameters.

Table 2-100 I²S interface timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
Input signal setup time	T_{su}	10	None	None	ns

Parameter	Symbol	Min	Typ	Max	Unit
Input signal hold time	T_{hd}	10	None	None	ns
Output signal delay	T_d	0	None	8	ns

2.8.8 I²C Interface Timing

Figure 2-39 shows the I²C transfer timing.

Figure 2-39 I2C transfer timing

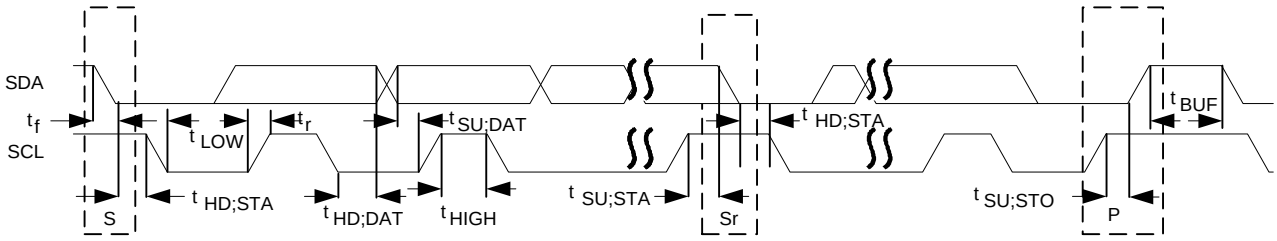


Table 2-101 describes the I²C interface timing parameters.

Table 2-101 I²C interface timing parameters

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
Serial clock (SCL) frequency	f_{SCL}	0	100	0	400	kHz
Start hold time	$t_{HD;STA}$	4.0	None	0.6	None	µs
SCL low-level cycle	t_{LOW}	4.7	None	1.3	None	µs
SCL high-level cycle	t_{HIGH}	4.0	None	0.6	None	µs
Start setup time	$t_{SU;STA}$	4.7	None	0.6	None	µs
Data hold time	$t_{HD;DAT}$	0	3.45	0	0.9	µs
Data setup time	$t_{SU;DAT}$	250	None	100	None	ns
Serial data (SDA) and SCL rising time	t_r	None	1000	$20 + 0.1C_b$	300	ns
SDA and SCL falling time	t_f	None	300	$20 + 0.1C_b$	300	ns
End setup time	$t_{SU;STO}$	4.0	None	0.6	None	µs
Bus release time from start to end	t_{BUF}	4.7	None	1.3	None	µs
Bus load	C_b	None	400	None	400	pF

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
Low-level noise tolerance	V_{nL}	$0.1V_{DD}$	None	$0.1V_{DD}$	None	V
High-level noise tolerance	V_{nH}	$0.2V_{DD}$	None	$0.2V_{DD}$	None	V

2.8.9 SPI Timings

NOTE

In Figure *Figure 2-40* to *Figure 2-42*, the conventions are as follows:

- MSB = most significant bit
- LSB = least significant bit
- SPI_CK(0):spo = 0
- SPI_CK(1):spo = 1

Figure 2-40 shows the SPI clock (SPICK) timing.

Figure 2-40 SPICK timing

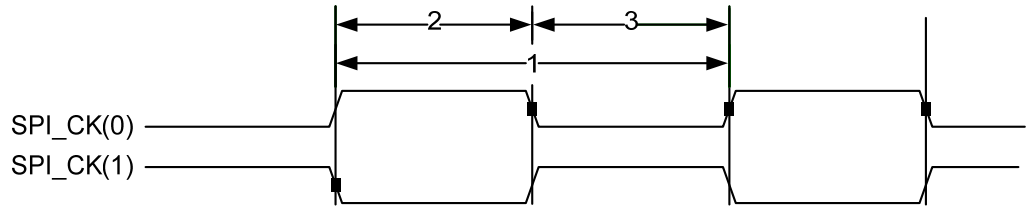


Figure 2-41 and Figure 2-42 show the SPI timings in master mode.

Figure 2-41 SPI timing in master mode (sph = 0)

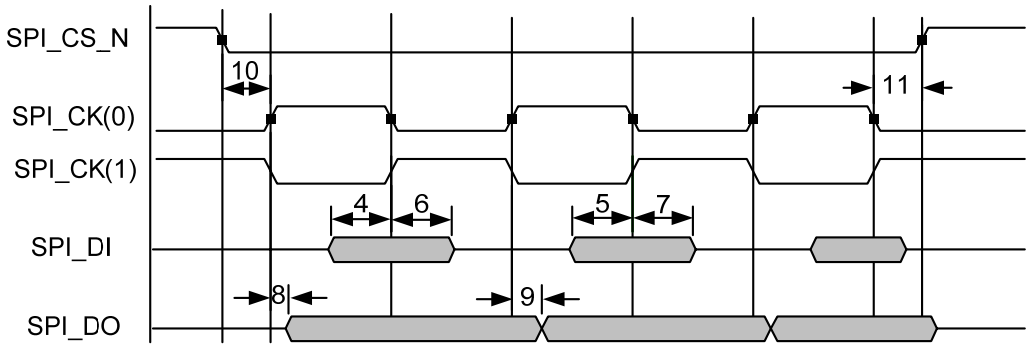


Figure 2-42 SPI timing in master mode (sph = 1)

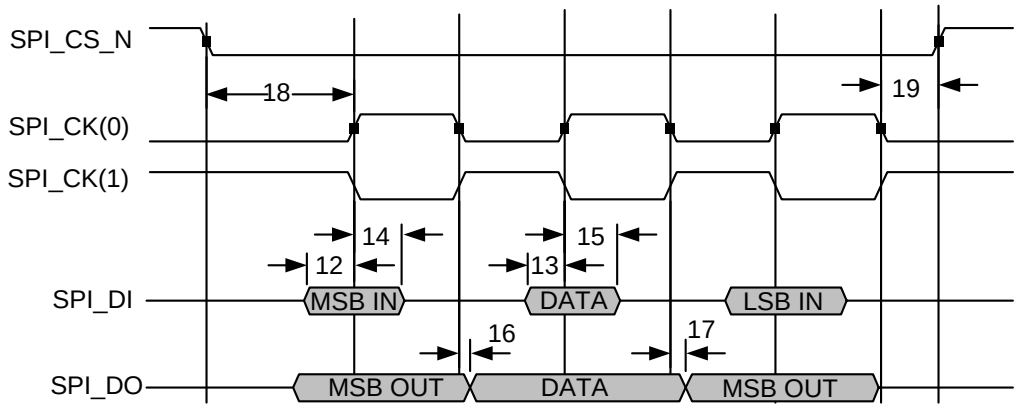


Table 2-102 describes the SPI timing parameters.

Table 2-102 SPI timing parameters

No.	Parameter	Symbol	Min	Typ	Max	Unit
1	Cycle time, SPI_CK	tc	None	None	None	ns
2	Pulse duration, SPI_CK high (all master modes)	tw1	None	None	None	ns
3	Pulse duration. SPI_CK low (all master modes)	tw2	None	None	None	ns
4	Setup time, SPI_DI (input) valid before SPI_CK (output) falling edge	tsu1	None	None	None	ns
5	Setup time, SPI_DI (in put) valid before SPICK (output) rising edge	tsu2	None	None	None	ns
6	Hold time, SPI_DI (input) valid after SPI_CK (output) falling edge	th1	None	None	None	ns
7	Hold time, SPI_DI (input) valid after SPI_CK (output) rising edge	th2	None	None	None	ns
8	Delay time, SPI_CK (output) rising edge to SPI_DO (output) transition	td1	None	None	None	ns
9	Delay time, SPI_CK (output) falling edge to SPI_DO (output) transition	td2	None	None	None	ns
10	Delay time, SPI_CS_N (output) falling edge to first SPI_CK (output) rising or falling edge	td3	None	None	None	ns
11	Delay time, SPI_CK (output) rising or falling edge to SPI_CS_N (output) rising edge	td4	None	None	None	ns
12	Setup time, SPI_DI (input) valid before	tsu3	None	None	None	ns

No.	Parameter	Symbol	Min	Typ	Max	Unit
	SPI_CK (output) rising edge					
13	Setup time, SPI_DI (in put) valid before SPI_CK (output) falling edge	tsu4	None	None	None	ns
14	Hold time, SPI_DI (input) valid after SPI_CK (output) rising edge	th3	None	None	None	ns
15	Hold time, SPI_DI (input) valid after SPI_CK (output) falling edge	th4	None	None	None	ns
16	Delay time, SPI_CK (output) falling edge to SPI_DO (output) transition	td5	None	None	None	ns
17	Delay time, SPI_CK (output) rising edge to SPI_DO (output) transition	td6	None	None	None	ns
18	Delay time, SPI_CS_N (output) falling edge to first SPI_CK (output) rising or falling edge	td7	None	None	None	ns
19	Delay time, SPI_CK (output) rising or falling edge to SPI_CS_N (output) rising edge	td8	None	None	None	ns

Contents

Figures

Tables

2 Hardware

2.1 Package and Pinout

2.1.1 Package

The Hi3518C uses the expose pad (Epad) quad flat package (QFP). It has 176 pins, its body size is 20 mm x 20 mm x 1.0 mm (0.79 in. x 0.79 in. x 0.04 in.), and its ball pitch is 0.4 mm (0.02 in.). Note that the pin length outside the QFQ is excluded, and the thickness is only the moulding thickness. Figure 2-1 to Figure 2-4 show the package of the Hi3518C. Table 2-1 lists the package dimensions of the Hi3518C.

Figure 2-1 Top view

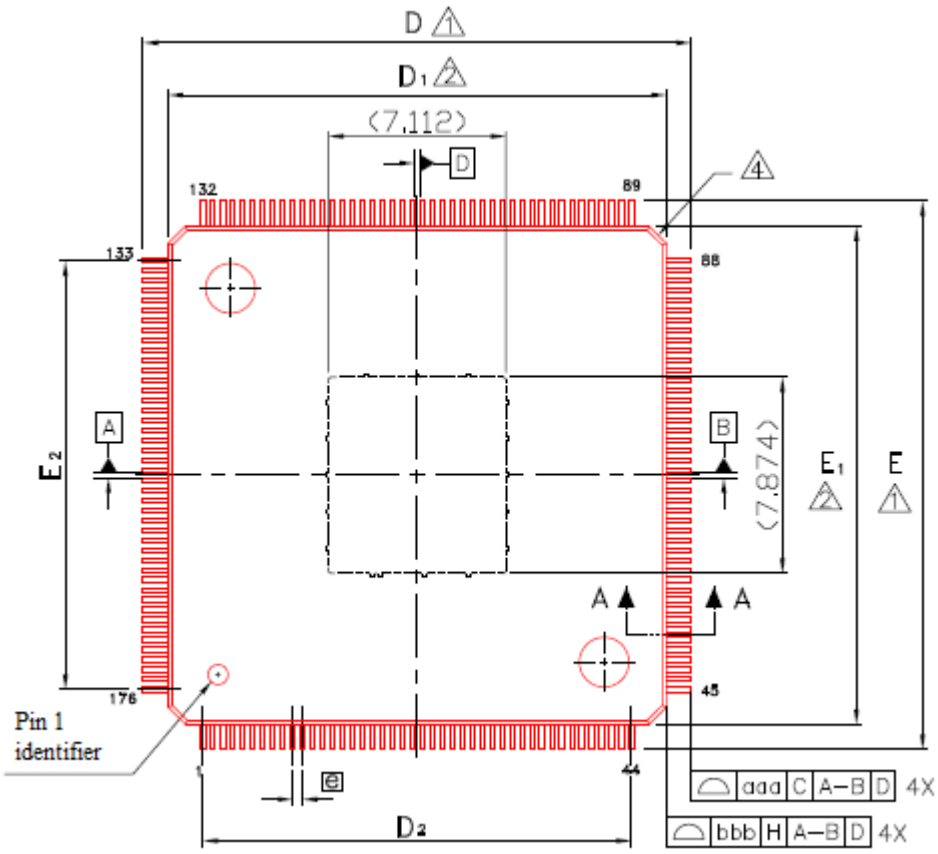


Figure 2-2 Side view

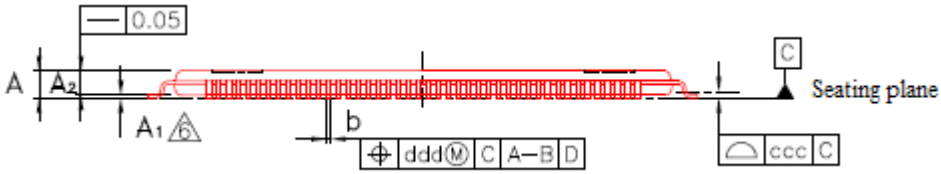


Figure 2-3 Enlarged view of detail "B"

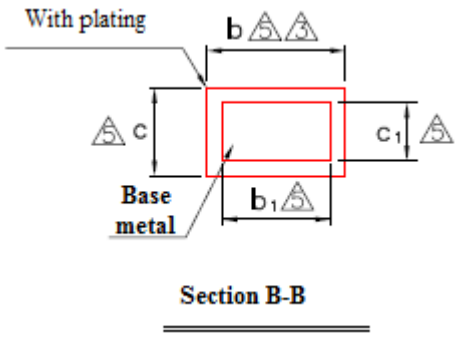


Figure 2-4 Enlarged view of detail "A"

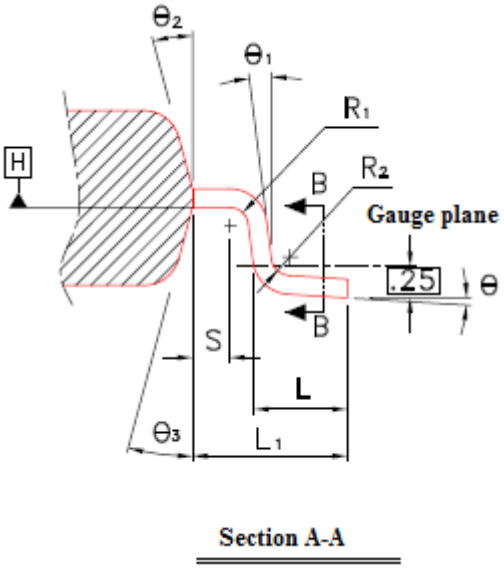


Table 2-1 Package dimensions

Parameter	Dimensions (mm)		
	Min	Typ	Max
A	1.00	1.10	1.20
A1	0.025	None	0.125
A2	0.95	1.00	1.05
b	0.13	0.18	0.23
b1	0.13	0.16	0.19
c	0.09	None	0.20
c1	0.09	None	0.16
D	22.00 BSC		
D1	20.00 BSC		
D2	17.20 BSC		
E	22.00 BSC		
E1	20.00 BSC		
E2	17.20 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
R1	0.08	None	None
R2	0.08	None	0.20
S	0.20	None	None
θ	0º	3.5º	7º
θ1	0º	None	None
θ2	11º	12º	13º
θ3	11º	12º	13º
aaa	0.20		
bbb	0.20		
ccc	0.08		
ddd	0.07		

2.1.2 Pinout

Table 2-2 lists the number of each type of pins on the Hi3518C (excluding Epad).

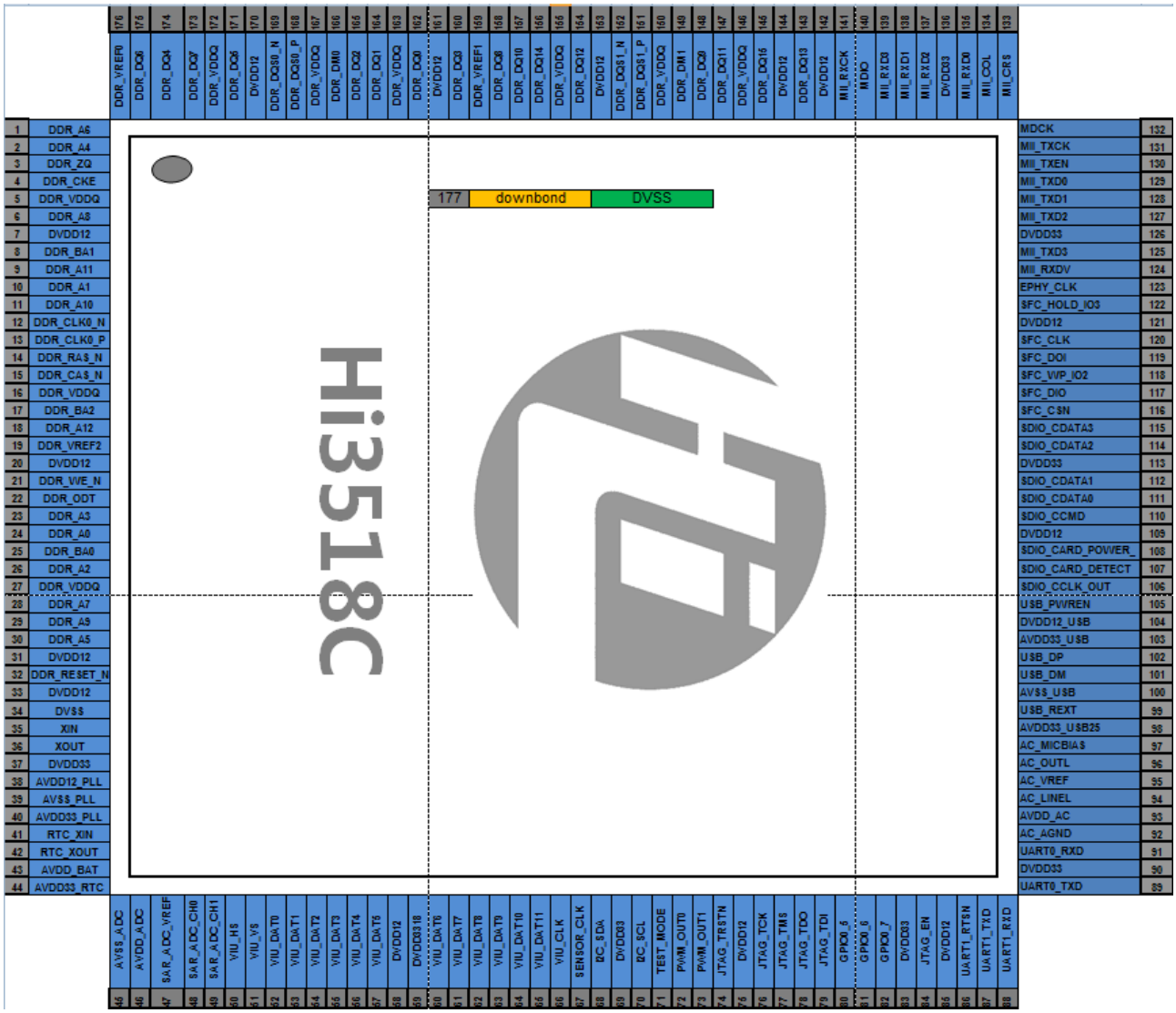
Table 2-2 Hi3518C pins

Pin Type	Quantity
Input/Output (I/O)	128
Digital power	32
Digital ground (GND)	1 lead + Epad
Others/Analog power	8
Others/Analog GND	4
Double-data rate (DDR) reference power	3
Total	176 (excluding Epad)

Pin Map

Figure 2-5 show the pin map.

Figure 2-5 Pin map (top view)



Pin Arrangement

Table 2-3 lists the Hi3518C pins in sequence.

Table 2-3 Pin arrangement

Pin Position	Name	Pin Position	Name
1	DDR_A6	90	DVDD33
2	DDR_A4	91	UART0_RXD
3	DDR_ZQ	92	AC_AGND
4	DDR_CKE	93	AVDD_AC
5	DDR_VDDQ	94	AC_LINEL

Pin Position	Name	Pin Position	Name
6	DDR_A8	95	AC_VREF
7	DVDD12	96	AC_OUTL
8	DDR_BA1	97	AC_MICBIAS
9	DDR_A11	98	AVDD33_USB25
10	DDR_A1	99	USB_REXT
11	DDR_A10	100	AVSS_USB
12	DDR_CLK0_N	101	USB_DM
13	DDR_CLK0_P	102	USB_DP
14	DDR_RAS_N	103	AVDD33_USB
15	DDR_CAS_N	104	DVDD12_USB
16	DDR_VDDQ	105	USB_PWREN
17	DDR_BA2	106	SDIO_CCLK_OUT
18	DDR_A12	107	SDIO_CARD_DETECT
19	DDR_VREF2	108	SDIO_CARD_POWER_EN
20	DVDD12	109	DVDD12
21	DDR_WE_N	110	SDIO_CCMD
22	DDR_ODT	111	SDIO_CDATA0
23	DDR_A3	112	SDIO_CDATA1
24	DDR_A0	113	DVDD33
25	DDR_BA0	114	SDIO_CDATA2
26	DDR_A2	115	SDIO_CDATA3
27	DDR_VDDQ	116	SFC_CSN
28	DDR_A7	117	SFC_DIO
29	DDR_A9	118	SFC_WP_IO2
30	DDR_A5	119	SFC_DOI
31	DVDD12	120	SFC_CLK
32	DDR_RESET_N	121	DVDD12
33	DVDD12	122	SFC_HOLD_IO3
34	DVSS	123	EPHY_CLK
35	XIN	124	MII_RXDV

Pin Position	Name	Pin Position	Name
36	XOUT	125	MII_TXD3
37	DVDD33	126	DVDD33
38	AVDD12_PLL	127	MII_TXD2
39	AVSS_PLL	128	MII_TXD1
40	AVDD33_PLL	129	MII_TXD0
41	RTC_XIN	130	MII_TXEN
42	RTC_XOUT	131	MII_TXCK
43	AVDD_BAT	132	MDCK
44	AVDD33_RTC	133	MII_CRS
45	AVSS_ADC	134	MII_COL
46	AVDD_ADC	135	MII_RXD0
47	SAR_ADC_VREF	136	DVDD33
48	SAR_ADC_CH0	137	MII_RXD2
49	SAR_ADC_CH1	138	MII_RXD1
50	VIU_HS	139	MII_RXD3
51	VIU_VS	140	MDIO
52	VIU_DAT0	141	MII_RXCK
53	VIU_DAT1	142	DVDD12
54	VIU_DAT2	143	DDR_DQ13
55	VIU_DAT3	144	DVDD12
56	VIU_DAT4	145	DDR_DQ15
57	VIU_DAT5	146	DDR_VDDQ
58	DVDD12	147	DDR_DQ11
59	DVDD3318	148	DDR_DQ9
60	VIU_DAT6	149	DDR_DM1
61	VIU_DAT7	150	DDR_VDDQ
62	VIU_DAT8	151	DDR_DQS1_P
63	VIU_DAT9	152	DDR_DQS1_N
64	VIU_DAT10	153	DVDD12
65	VIU_DAT11	154	DDR_DQ12
66	VIU_CLK	155	DDR_VDDQ

Pin Position	Name	Pin Position	Name
67	SENSOR_CLK	156	DDR_DQ14
68	I2C_SDA	157	DDR_DQ10
69	DVDD33	158	DDR_DQ8
70	I2C_SCL	159	DDR_VREF1
71	TEST_MODE	160	DDR_DQ3
72	PWM_OUT0	161	DVDD12
73	PWM_OUT1	162	DDR_DQ0
74	JTAG_TRSTN	163	DDR_VDDQ
75	DVDD12	164	DDR_DQ1
76	JTAG_TCK	165	DDR_DQ2
77	JTAG_TMS	166	DDR_DM0
78	JTAG_TDO	167	DDR_VDDQ
79	JTAG_TDI	168	DDR_DQS0_P
80	GPIO0_5	169	DDR_DQS0_N
81	GPIO0_6	170	DVDD12
82	GPIO0_7	171	DDR_DQ5
83	DVDD33	172	DDR_VDDQ
84	JTAG_EN	173	DDR_DQ7
85	DVDD12	174	DDR_DQ4
86	UART1_RTSN	175	DDR_DQ6
87	UART1_TXD	176	DDR_VREF0
88	UART1_RXD	177(Epad)	DVSS
89	UART0_TXD		

2.2 Pin Descriptions

2.2.1 Pin Types

Table 2-4 describes the input/output (I/O) pin types.

Table 2-4 I/O pin types

I/O Type	Description
I	Input signal
I_{PD}	Input signal, internal pull-down
I_{PU}	Input signal, internal pull-up
I_S	Input signal with Schmitt trigger
I_{SPD}	Input signal with Schmitt trigger, internal pull-down
I_{SPU}	Input signal with Schmitt trigger, internal pull-up
O	Output signal
O_{OD}	Output open drain (OD)
I/O	Bidirectional (input/output) signal
I_{PD}/O	Bidirectional signal, input pull-down
I_{PU}/O	Bidirectional signal, input pull-up
I_{SPU}/O	Bidirectional signal with Schmitt trigger, input pull-up
I_{PD}/O_{OD}	Bidirectional signal, input pull-down and output OD
I_{PU}/O_{OD}	Bidirectional signal, input pull-up and output OD
I_S/O	Bidirectional signal, input with Schmitt trigger
I_S/O_{OD}	Bidirectional signal, input with Schmitt trigger and output OD
CIN	Crystal oscillator input
COUT	Crystal oscillator output
P	Power supply
G	Ground (GND)

2.2.2 Pin Details

SYS Pins

Table 2-5 describes system (SYS) pins.

Table 2-5 SYS pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
35	XIN	I	None	3.3	Crystal input

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
36	XOUT	O	None	3.3	Crystal output
71	TEST_MODE	I_{SPD}	None	3.3	Mode select. 0: functional mode 1: test mode

JTAG Pins

Table 2-6 describes Joint Test Action Group (JTAG) pins.

Table 2-6 JTAG pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
84	JTAG_EN	I_{PD}	None	3.3	JTAG pin enable. 0: disabled 1: enabled
76	JTAG_TCK	I_{PD}/O	4	3.3	**Function 0: GPIO0_1** General-purpose input/output (GPIO) **Function 1: JTAG_TCK** JTAG clock input **Function 2: TEMPER_DQ** Temperature measurement. It is used to communicate with the external temperature measurement chip.
79	JTAG_TDI	I_{PU}/O	4	3.3	**Function 0: GPIO0_4** GPIO **Function 1: JTAG_TDI** JTAG data input **Function 2: TEMPER_DQ** Temperature measurement. It is used to communicate with the external temperature measurement chip.

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
78	JTAG_TDO	I_{PD}/O	8	3.3	**Function 0: GPIO0_3** GPIO **Function 1: JTAG_TDO** JTAG data output **Function 2: TEMPER_DQ** Temperature measurement. It is used to communicate with the external temperature measurement chip.
77	JTAG_TMS	I_{PU}/O	4	3.3	**Function 0: GPIO0_2** GPIO **Function 1: JTAG_TMS** JTAG mode select input. **Function 2: TEMPER_DQ** Temperature measurement. It is used to communicate with the external temperature measurement chip.
74	JTAG_TRSTN	I_{PD}/O	4	3.3	**Function 0: GPIO0_0** GPIO **Function 1: JTAG_TRSTN** JTAG reset input **Function 2: TEMPER_DQ** Temperature measurement. It is used to communicate with the external temperature measurement chip.

DDR Pins

Table 2-7 describes double-data rate (DDR) power pins.

Table 2-7 DDR power pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
5, 16, 27, 146, 150, 155, 163, 167, 172	DDR_VDDQ	P	None	1.8/1.5	DDR I/O power
176 159 19	DDR_VREF0 DDR_VREF1 DDR_VREF2	P	None	0.5 x DDR_VDDQ	DDR reference voltage

Table 2-8 describes DDR signal pins.

Table 2-8 DDR signal pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
24	DDR_A0	O	None	1.8/1.5	Address signal 0 of the DDR synchronous dynamic random access memory (SDRAM)
10	DDR_A1	O	None	1.8/1.5	Address signal 1 of the DDR SDRAM
26	DDR_A2	O	None	1.8/1.5	Address signal 2 of the DDR SDRAM
23	DDR_A3	O	None	1.8/1.5	Address signal 3 of the DDR SDRAM
2	DDR_A4	O	None	1.8/1.5	Address signal 4 of the DDR SDRAM
30	DDR_A5	O	None	1.8/1.5	Address signal 5 of the DDR SDRAM
1	DDR_A6	O	None	1.8/1.5	Address signal 6 of the DDR SDRAM
28	DDR_A7	O	None	1.8/1.5	Address signal 7 of the DDR SDRAM
6	DDR_A8	O	None	1.8/1.5	Address signal 8 of the DDR SDRAM
29	DDR_A9	O	None	1.8/1.5	Address signal 9 of the DDR SDRAM
11	DDR_A10	O	None	1.8/1.5	Address signal 10 of the DDR SDRAM

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
9	DDR_A11	O	None	1.8/1.5	Address signal 11 of the DDR SDRAM
18	DDR_A12	O	None	1.8/1.5	Address signal 12 of the DDR SDRAM
25	DDR_BA0	O	None	1.8/1.5	Bank address signal 0 of the DDR SDRAM
8	DDR_BA1	O	None	1.8/1.5	Bank address signal 1 of the DDR SDRAM
17	DDR_BA2	O	None	1.8/1.5	Bank address signal 2 of the DDR SDRAM
15	DDR_CAS_N	O	None	1.8/1.5	Column address select of the DDR SDRAM
4	DDR_CKE	O	None	1.8/1.5	DDR SDRAM clock enable
12	DDR_CLK0_N	O	None	1.8/1.5	Negative differential clock 0 of the DDR SDRAM
13	DDR_CLK0_P	O	None	1.8/1.5	Positive differential clock 0 of the DDR SDRAM
166	DDR_DM0	I/O	None	1.8/1.5	Data mask signal 0 of the DDR SDRAM
149	DDR_DM1	I/O	None	1.8/1.5	Data mask signal 1 of the DDR SDRAM
162	DDR_DQ0	I/O	None	1.8/1.5	Data line 0 of the DDR SDRAM
164	DDR_DQ1	I/O	None	1.8/1.5	Data line 1 of the DDR SDRAM
165	DDR_DQ2	I/O	None	1.8/1.5	Data line 2 of the DDR SDRAM
160	DDR_DQ3	I/O	None	1.8/1.5	Data line 3 of the DDR SDRAM
174	DDR_DQ4	I/O	None	1.8/1.5	Data line 4 of the DDR SDRAM
171	DDR_DQ5	I/O	None	1.8/1.5	Data line 5 of the DDR SDRAM
175	DDR_DQ6	I/O	None	1.8/1.5	Data line 6 of the DDR SDRAM

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
173	DDR_DQ7	I/O	None	1.8/1.5	Data line 7 of the DDR SDRAM
158	DDR_DQ8	I/O	None	1.8/1.5	Data line 8 of the DDR SDRAM
148	DDR_DQ9	I/O	None	1.8/1.5	Data line 9 of the DDR SDRAM
157	DDR_DQ10	I/O	None	1.8/1.5	Data line 10 of the DDR SDRAM
147	DDR_DQ11	I/O	None	1.8/1.5	Data line 11 of the DDR SDRAM
154	DDR_DQ12	I/O	None	1.8/1.5	Data line 12 of the DDR SDRAM
143	DDR_DQ13	I/O	None	1.8/1.5	Data line 13 of the DDR SDRAM
156	DDR_DQ14	I/O	None	1.8/1.5	Data line 14 of the DDR SDRAM
145	DDR_DQ15	I/O	None	1.8/1.5	Data line 15 of the DDR SDRAM
169	DDR_DQS0_N	I/O	None	1.8/1.5	Negative data strobe (DQS) signal 0 of the DDR, corresponding to DQ[7:0]
168	DDR_DQS0_P	I/O	None	1.8/1.5	Positive DQS signal 0 of the DDR, corresponding to DQ[7:0]
152	DDR_DQS1_N	I/O	None	1.8/1.5	Negative DQS signal 1 of the DDR, corresponding to DQ[15:8]
151	DDR_DQS1_P	I/O	None	1.8/1.5	Positive DQS signal 1 of the DDR, corresponding to DQ[15:8]
22	DDR_ODT	None	None	None	Connect to an external matched reference resistor
14	DDR_RAS_N	O	None	1.8/1.5	Row address select of the DDR SDRAM

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
32	DDR_RESET_N	O	None	1.8/1.5	Reset signal of the DDR3 SDRAM
21	DDR_WE_N	O	None	1.8/1.5	DDR SDRAM write enable
3	DDR_ZQ	None	None	None	Resistor interface on the matched impedance calibration circuit of the DDR23 Lite physical layer (PHY), for connecting to a 240 Ω external resistor

ETH Pins

Table 2-9 describes the EPHY_CLK pins.

Table 2-9 EPHY_CLK pin

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
123	EPHY_CLK	I/O	8	3.3	**Function 0: GPIO1_3** GPIO **Function 1: EPHY_CLK** Working clock of the media independent interface (MII) PHY **Function 2: VOU1120_DATA2** BT.1120 luminance signal output

Table 2-10 describes management data input/output (MDIO) pins.

Table 2-10 MDIO pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
132	MDCK	I_{PD}/O	8	3.3	**Function 0: GPIO3_6** GPIO **Function 1: MDCK** MDIO clock output

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					Function 2: VOU1120_DATA6 BT.1120 luminance signal output **Function 3: BOOT_SEL** Storage medium select for booting. 0: storage space of the serial peripheral interface (SPI) flash 1: reserved
140	MDIO	I/O	8	3.3	**Function 0: GPIO3_7** GPIO **Function 1: MDIO** MDIO input/output **Function 2: VOU1120_DATA14** BT.1120 chrominance signal output

Table 2-11 describes MII pins.

Table 2-11 MII pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
134	MII_COL	I/O	8	3.3	**Function 0: GPIO3_1** GPIO **Function 1: MII_COL** MII collision indicator **Function 2: VOU1120_DATA9** BT.1120 chrominance signal output
133	MII_CRS	I/O	8	3.3	**Function 0: GPIO3_0** GPIO **Function 1: MII_CRS** MII carrier sense signal **Function 2: VOU1120_DATA10** BT.1120 chrominance

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					signal output
141	MII_RXCK	I/O	12	3.3	**Function 0: GPIO3_2** GPIO **Function 1: MII_RXCK** MII receive (RX) clock **Function 2: VOU1120_CLK** BT.1120 clock output
135	MII_RXD0	I/O	8	3.3	**Function 0: GPIO4_0** GPIO **Function 1: MII_RXD0** Reduced media-independent interface (RMII) or MII RX data **Function 2: VOU1120_DATA12** BT.1120 chrominance signal output
138	MII_RXD1	I/O	8	3.3	**Function 0: GPIO4_1** GPIO **Function 1: MII_RXD1** RMII or MII RX data **Function 2: VOU1120_DATA8** BT.1120 chrominance signal output
137	MII_RXD2	I/O	8	3.3	**Function 0: GPIO4_2** GPIO **Function 1: MII_RXD2** MII RX data **Function 2: VOU1120_DATA11** BT.1120 chrominance signal output
139	MII_RXD3	I/O	8	3.3	**Function 0: GPIO4_3** GPIO

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					Function 1: MII_RXD3 MII RX data **Function 2: VOU1120_DATA15** BT.1120 chrominance signal output
124	MII_RXDV	I/O	8	3.3	**Function 0: GPIO3_4** GPIO **Function 1: MII_RXDV** MII RX data validity indicator **Function 2: VOU1120_DATA1** BT.1120 luminance signal output
131	MII_TXCK	I/O	12	3.3	**Function 0: GPIO3_3** GPIO **Function 1: MII_TXCK** MII transmit (TX) clock **Function 2: VOU1120_DATA7** BT.1120 luminance signal output **Function 3: RMII_CLK** RMII clock
129	MII_TXD0	I/O	8	3.3	**Function 0: GPIO4_4** GPIO **Function 1: MII_TXD0** RMII or MII TX data **Function 2: VOU1120_DATA4** BT.1120 luminance signal output
128	MII_TXD1	I/O	8	3.3	**Function 0: GPIO4_5** GPIO **Function 1: MII_TXD1**

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					RMII or MII TX data **Function 2: VOU1120_DATA0** BT.1120 luminance signal output
127	MII_TXD2	I/O	8	3.3	**Function 0: GPIO4_6** GPIO **Function 1: MII_TXD2** MII TX data **Function 2: VOU1120_DATA13** BT.1120 chrominance signal output
125	MII_TXD3	I/O	8	3.3	**Function 0: GPIO4_7** GPIO **Function 1: MII_TXD3** MII TX DATA **Function 2: VOU1120_DATA3** BT.1120 luminance signal output
130	MII_TXEN	I/O	8	3.3	**Function 0: GPIO3_5** GPIO **Function 1: MII_TXEN** MII TX data enable **Function 2: VOU1120_DATA5** BT.1120 luminance signal output

SFC Pins

Table 2-12 describes SPI flash controller (SFC) pins.

Table 2-12 SFC pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
120	SFC_CLK	I_{PD}/O	12	3.3	**Function 0: SFC_CLK** Clock signal transmitted to the SPI flash. The high level or low level can be configured when the clock is not switched. **Function 1: GPIO7_2** GPIO **Function 2: SFC_ADDR_MODE** Default address mode of the SFC. 0: 3-byte address mode 1: 4-byte address mode
116	SFC_CSN	I/O	4	3.3	Chip select 0 (CS 0), active low
117	SFC_DIO	I/O	8	3.3	**Function 0: SFC_DIO** Data output signal in standard SPI mode Data I/O signal in dual-SPI mode Data I/O signal in quad-SPI mode **Function 1: GPIO7_0** GPIO
119	SFC_DOI	I/O	8	3.3	**Function 0: SFC_DOI** Data input signal in standard SPI mode Data I/O signal in dual-SPI mode Data I/O signal in quad-SPI mode **Function 1: GPIO7_3**

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					GPIO
122	SFC_HOLD_IO3	I/O	8	3.3	**Function 0: SFC_HOLD_IO3** Hold function in standard SPI mode, active low Hold function in dual-SPI mode, active low Data I/O signal in quad-SPI mode **Function 1: GPIO7_4** GPIO
118	SFC_WP_IO2	I/O	8	3.3	**Function 0: SFC_WP_IO2** Write protection function in standard SPI mode, active low Write protection function in dual-SPI mode, active low Data I/O signal in quad-SPI mode **Function 1: GPIO7_1** GPIO

SDIO Pins

Table 2-13 describes secure digital input/output (SDIO) pins.

Table 2-13 SDIO pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
107	SDIO_CARD_DETECT	I_{PU}/O	4	3.3	**Function 0: GPIO6_0** GPIO **Function 1: SDIO_CARD_DETE**

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					CT Card detection signal, active low
108	SDIO_CARD_POWER_EN	I_{PD}/O	4	3.3	**Function 0: GPIO6_1** GPIO **Function 1: SDIO_CARD_POWER_EN** Power enable signal. The value 1 indicates power on.
106	SDIO_CCLK_OUT	I_{PD}/O	12	3.3	**Function 0: GPIO1_1** GPIO **Function 1: SDIO_CCLK_OUT** Output working clock for the card
110	SDIO_CCMD	I_{PU}/O	8	3.3	**Function 0: GPIO6_3** GPIO **Function 1: SDIO_CCMD** Card command
111	SDIO_CDATA0	I_{PU}/O	8	3.3	**Function 0: GPIO6_4** GPIO **Function 1: SDIO_CDATA0** Card data **Function 2: CLK_TEST_OUT0** Main test clock output **Function 3: CLK_TEST_OUT1** Main test clock output **Function 4: CLK_TEST_OUT2** Main test clock output **Function 5:**

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					CLK_TEST_OUT3 Main test clock output
112	SDIO_CDATA1	I_{PU}/O	8	3.3	**Function 0: PLL_TEST_OUT0** Phase-locked loop (PLL) test clock output **Function 1: SDIO_CDATA1** Card data **Function 2: GPIO6_5** GPIO **Function 3: PLL_TEST_OUT1** PLL test clock output **Function 4: PLL_TEST_OUT2** PLL test clock output **Function 5: PLL_TEST_OUT3** PLL test clock output **Function 6: RTC_TEST_CLK** Real-time clock (RTC) test clock output
114	SDIO_CDATA2	I_{PU}/O	8	3.3	**Function 0: GPIO6_6** GPIO **Function 1: SDIO_CDATA2** Card data
115	SDIO_CDATA3	I_{PU}/O	8	3.3	**Function 0: GPIO6_7** GPIO **Function 1: SDIO_CDATA3** Card data

USB Pins

Table 2-14 describes universal serial bus (USB) pins.

Table 2-14 USB pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
103	AVDD33_USB	P	None	3.3	USB analog power
98	AVDD33_USB25	P	None	3.3	USB analog power, for internally converting the voltage into 2.5 V
100	AVSS_USB	G	None	None	USB analog GND
104	DVDD12_USB	P	None	1.2	USB digital power
101	USB_DM	I/O	None	0.4/3.3	USB0 D- signal. In high-speed mode, the maximum voltage of this port is 800 mV or 400 mV. In full-speed or low-speed mode, the voltage of this port is 3.3 V.
102	USB_DP	I/O	None	0.4/3.3	USB0 D+ signal. In high-speed mode, the maximum voltage of this port is 800 mV or 400 mV. In full-speed or low-speed mode, the voltage of this port is 3.3 V.
99	USB_REXT	I/O	None	3.3	USB external resistor interface, externally connecting to a 43.2 Ω ±1% resistor and then to GND
105	USB_PWREN	I_{PD}/O	8	3.3	**Function 0: GPIO5_1** GPIO **Function 1: USB_PWREN** Power control output of the USB port, configurable level, and active low by default

Audio CODEC Pins

Table 2-15 describes audio CODEC pins

Table 2-15 Audio CODEC pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
94	AC_LINEL	I	None	3.3	Audio-left channel input of the audio interface
97	AC_MICBIAS	I/O	None	3.3	Microphone bias voltage, externally connecting to a 4.7 µF capacitor and then to GND
96	AC_OUTL	O	None	3.3	Audio-left channel output of the audio interface
95	AC_VREF	P	None	3.3	Audio reference voltage
92	AC_AGND	G	None	None	Audio analog GND.
93	AVDD_AC	P	None	3.3	Audio analog power

VI Pins

Table 2-16 describes sensor pins.

Table 2-16 VI pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
67	SENSOR_CLK	I/O	24	1.8/3.3	**Function 0: GPIO1_2** GPIO **Function 1: SENSOR_CLK** Sensor working clock
66	VIU_CLK	I/O	4	1.8/3.3	**Function 0: VIU_CLK** Video input unit 0 (VIU 0) clock **Function 1: GPIO11_6** GPIO

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
52	VIU_DAT0	I/O	4	1.8/3.3	**Function 0: VIU_DAT0** VIU 0 data input **Function 1: GPIO10_0** GPIO
53	VIU_DAT1	I/O	4	1.8/3.3	**Function 0: VIU_DAT1** VIU 0 data input **Function 1: GPIO10_1** GPIO
54	VIU_DAT2	I/O	4	1.8/3.3	**Function 0: VIU_DAT2** VIU 0 data input **Function 1: GPIO10_2** GPIO
55	VIU_DAT3	I/O	4	1.8/3.3	**Function 0: VIU_DAT3** VIU 0 data input **Function 1: GPIO10_3** GPIO
56	VIU_DAT4	I/O	4	1.8/3.3	**Function 0: VIU_DAT4** VIU 0 data input **Function 1: GPIO10_4** GPIO
57	VIU_DAT5	I_{PD}/O	4	1.8/3.3	**Function 0: VIU_DAT5** VIU 0 data input **Function 1: GPIO10_5** GPIO
60	VIU_DAT6	I/O	4	1.8/3.3	**Function 0: VIU_DAT6** VIU 0 data input **Function 1: GPIO10_6** GPIO
61	VIU_DAT7	I/O	4	1.8/3.3	**Function 0: VIU_DAT7** VIU 0 data input **Function 1: GPIO10_7** GPIO
62	VIU_DAT8	I/O	4	1.8/3.3	**Function 0: VIU_DAT8** VIU 0 data input **Function 1: GPIO11_0** GPIO

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
63	VIU_DAT9	I/O	4	1.8/3.3	**Function 0: VIU_DAT9** VIU 0 data input **Function 1: GPIO11_1** GPIO
64	VIU_DAT10	I/O	4	1.8/3.3	**Function 0: VIU_DAT10** VIU 0 data input **Function 1: GPIO11_2** GPIO
65	VIU_DAT11	I/O	4	1.8/3.3	**Function 0: VIU_DAT11** VIU 0 data input **Function 1: GPIO11_3** GPIO
50	VIU_HS	I/O	4	1.8/3.3	**Function 0: VIU_HS** VIU 0 horizontal sync, active high **Function 1: GPIO11_4** GPIO
51	VIU_VS	I/O	4	1.8/3.3	**Function 0: VIU_VS** VIU 0 vertical sync, active high **Function 1: GPIO11_5** GPIO

UART Pins

Table 2-17 describes universal asynchronous receiver transmitter 0 (UART0) pins.

Table 2-17 UART 0 pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
91	UART0_RXD	I_{PU}	None	3.3	UART 0 RX data
89	UART0_TXD	I/O	4	3.3	UART 0 TX data

Table 2-18 describes UART 1 pins.

Table 2-18 UART 1 pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
86	UART1_RTSN	I/O	4	3.3	**Function 0: GPIO2_2** GPIO **Function 1: UART1_RTSN** Modem state output: request-to-send (RTS), active low. The reset value is 0.
88	UART1_RXD	I_{PU}/O	4	3.3	**Function 0: GPIO2_3** GPIO **Function 1: UART1_RXD** UART 1 RX data
87	UART1_TXD	I/O	4	3.3	**Function 0: GPIO2_5** GPIO **Function 1: UART1_TXD** UART 1 TX data

I²C Pins

Table 2-19 describes inter-integrated circuit (I^2C) pins.

Table 2-19 I^2C pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
70	I2C_SCL	I/O_{OD}	8	3.3	**Function 0: GPIO2_1** GPIO **Function 1: I2C_SCL** I^2C bus clock, OD output
68	I2C_SDA	I/O_{OD}	8	3.3	**Function 0: GPIO2_0** GPIO **Function 1: I2C_SDA**

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					I^2C bus data/address, OD output

PWM Pins

Table 2-20 describes pulse width modulation (PWM) pins.

Table 2-20 PWM pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
72	PWM_OUT0	I/O	4	3.3	**Function 0: GPIO5_2** GPIO **Function 1: PWM_OUT0** PWM output 0
73	PWM_OUT1	I/O	4	3.3	**Function 0: GPIO5_3** GPIO **Function 1: PWM_OUT1** PWM output 1

GPIO Pins

Table 2-21 describes GPIO pins.

Table 2-21 GPIO pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
80	GPIO0_5	I/O	4	3.3	**Function 0: SVB_PWM** SVB control signal output **Function 1: GPIO0_5** GPIO **Function 2: TEMPER_DQ** Temperature measurement. It is used to communicate with the external temperature measurement chip.

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
81	GPIO0_6	I/O	4	3.3	**Function 0: GPIO0_6** GPIO **Function 1: SVB_PWM** SVB control signal output **Function 2: TEMPER_DQ** Temperature measurement. It is used to communicate with the external temperature measurement chip.
82	GPIO0_7	I/O	4	3.3	**Function 0: SYS_RSTN_OUT** System reset output **Function 1: GPIO0_7** GPIO **Function 2: TEMPER_DQ** Temperature measurement. It is used to communicate with the external temperature measurement chip.

SAR_ADC Pins

Table 2-22 describes SAR_ADC pins.

Table 2-22 SAR_ADC pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
48	SAR_ADC_CH0	I	None	3.3	SAR_ADC channel 0
49	SAR_ADC_CH1	I	None	3.3	SAR_ADC channel 1
47	SAR_ADC_VREF	P	None	3.3	SAR_ADC reference voltage
46	AVDD_ADC	P	None	3.3	SAR_ADC analog power
45	AVSS_ADC	G	None	None	SAR_ADC analog GND

RTC Pins

Table 2-23 describes RTC pins.

Table 2-23 RTC pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
41	RTC_XIN	I	None	3.3	RTC crystal input
42	RTC_XOUT	O	None	3.3	RTC crystal output
43	AVDD_BAT	P	None	3.3	RTC battery power
44	AVDD33_RTC	P	None	3.3	RTC analog power

Power Pins and GND Pins

Table 2-24 describes power pins and GND pins.

Table 2-24 Power pins and GND pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)
38	AVDD12_PLL	P	1.2	1.2 V PLL analog power
40	AVDD33_PLL	P	3.3	3.3 V PLL analog power
39	AVSS_PLL	G	None	PLL analog GND
7, 20, 31, 33, 58, 75, 85, 104, 109, 121, 142, 144, 153, 161, 170	DVDD12	P	1.2	Core power
37, 69, 83, 90, 113, 126, 136	DVDD33	P	3.3	3.3 V I/O digital power
59	DVDD3318	P	3.3/1.8	3.3 V or 1.8 V I/O digital power
34	DVSS	G	None	Digital GND

2.3 Pin Multiplexing Control Registers

2.3.1 Summary of Multiplexing Control Registers

Table 2-25 describes multiplexing control registers.

Table 2-25 Summary of multiplexing control registers (base address: 0x200F_0000)

Offset Address	Register	Description	Page
0x004	muxctrl_reg1	Multiplexing control register for the SDIO_CCLK_OUT pin	2-35
0x008	muxctrl_reg2	Multiplexing control register for the SENSOR_CLK pin	2-35
0x018	muxctrl_reg6	Multiplexing control register for the I2C_SDA pin	2-36
0x01C	muxctrl_reg7	Multiplexing control register for the I2C_SCL pin	2-36
0x020	muxctrl_reg8	Multiplexing control register for the UART1_RTSN pin	2-37
0x024	muxctrl_reg9	Multiplexing control register for the UART1_RXD pin	2-37
0x02C	muxctrl_reg11	Multiplexing control register for the UART1_TXD pin	2-38
0x030	muxctrl_reg12	Multiplexing control register for the MII_CRS pin	2-38
0x034	muxctrl_reg13	Multiplexing control register for the MII_COL pin	2-39
0x038	muxctrl_reg14	Multiplexing control register for the MII_RXD3 pin	2-39
0x03C	muxctrl_reg15	Multiplexing control register for the MII_RXD2 pin	2-40
0x040	muxctrl_reg16	Multiplexing control register for the MII_RXD1 pin	2-40
0x044	muxctrl_reg17	Multiplexing control register for the MII_RXD0 pin	2-41
0x048	muxctrl_reg18	Multiplexing control register for the MII_TXD3 pin	2-41
0x04C	muxctrl_reg19	Multiplexing control register for the MII_TXD2 pin	2-42
0x050	muxctrl_reg20	Multiplexing control register for the MII_TXD1 pin	2-42

Offset Address	Register	Description	Page
0x054	muxctrl_reg21	Multiplexing control register for the MII_TXD0 pin	2-43
0x058	muxctrl_reg22	Multiplexing control register for the MII_RXCK pin	2-43
0x05C	muxctrl_reg23	Multiplexing control register for the MII_TXCK pin	2-44
0x060	muxctrl_reg24	Multiplexing control register for the MII_RXDV pin	2-44
0x064	muxctrl_reg25	Multiplexing control register for the MII_TXEN pin	2-45
0x070	muxctrl_reg28	Multiplexing control register for the EPHY_CLK pin	2-45
0x074	muxctrl_reg29	Multiplexing control register for the MDCK pin	2-46
0x078	muxctrl_reg30	Multiplexing control register for the MDIO pin	2-46
0x080	muxctrl_reg32	Multiplexing control register for the SDIO_CARD_DETECT pin	2-47
0x084	muxctrl_reg33	Multiplexing control register for the SDIO_CARD_POWER_EN pin	2-47
0x08C	muxctrl_reg35	Multiplexing control register for the SDIO_CCMD pin	2-48
0x090	muxctrl_reg36	Multiplexing control register for the SDIO_CDATA0 pin	2-48
0x094	muxctrl_reg37	Multiplexing control register for the SDIO_CDATA1 pin	2-49
0x098	muxctrl_reg38	Multiplexing control register for the SDIO_CDATA2 pin	2-50
0x09C	muxctrl_reg39	Multiplexing control register for the SDIO_CDATA3 pin	2-50
0x0A0	muxctrl_reg40	Multiplexing control register for the SFC_DIO pin	2-50
0x0A4	muxctrl_reg41	Multiplexing control register for the SFC_WP_IO2 pin	2-51
0x0A8	muxctrl_reg42	Multiplexing control register for the SFC_CLK pin	2-51
0x0AC	muxctrl_reg43	Multiplexing control register for the SFC_DOI pin	2-52
0x0B0	muxctrl_reg44	Multiplexing control register for the SFC_HOLD_IO3 pin	2-52

Offset Address	Register	Description	Page
0x0B8	muxctrl_reg46	Multiplexing control register for the USB_PWREN pin	2-53
0x0BC	muxctrl_reg47	Multiplexing control register for the PWM_OUT0 pin	2-53
0x0C0	muxctrl_reg48	Multiplexing control register for the PWM_OUT1 pin	2-54
0x120	muxctrl_reg72	Multiplexing control register for the JTAG_TRSTN pin	2-54
0x124	muxctrl_reg73	Multiplexing control register for the JTAG_TCK pin	2-55
0x128	muxctrl_reg74	Multiplexing control register for the JTAG_TMS pin	2-55
0x12C	muxctrl_reg75	Multiplexing control register for the JTAG_TDO pin	2-56
0x130	muxctrl_reg76	Multiplexing control register for the JTAG_TDI pin	2-56
0x134	muxctrl_reg77	Multiplexing control register for the GPIO0_5 pin	2-57
0x138	muxctrl_reg78	Multiplexing control register for the GPIO0_6 pin	2-57
0x13C	muxctrl_reg79	Multiplexing control register for the GPIO0_7 pin	2-58
0x140	muxctrl_reg80	Multiplexing control register for the VIU_CLK pin	2-58
0x144	muxctrl_reg81	Multiplexing control register for the VIU_VS pin	2-59
0x148	muxctrl_reg82	Multiplexing control register for the VIU_HS pin	2-59
0x14C	muxctrl_reg83	Multiplexing control register for the VIU_DAT11 pin	2-60
0x150	muxctrl_reg84	Multiplexing control register for the VIU_DAT10 pin	2-60
0x154	muxctrl_reg85	Multiplexing control register for the VIU_DAT9 pin	2-61
0x158	muxctrl_reg86	Multiplexing control register for the VIU_DAT8 pin	2-61
0x15C	muxctrl_reg87	Multiplexing control register for the VIU_DAT7 pin	2-62

Offset Address	Register	Description	Page
0x160	muxctrl_reg88	Multiplexing control register for the VIU_DAT6 pin	2-62
0x164	muxctrl_reg89	Multiplexing control register for the VIU_DAT5 pin	2-63
0x168	muxctrl_reg90	Multiplexing control register for the VIU_DAT4 pin	2-63
0x16C	muxctrl_reg91	Multiplexing control register for the VIU_DAT3 pin	2-64
0x170	muxctrl_reg92	Multiplexing control register for the VIU_DAT2 pin	2-64
0x174	muxctrl_reg93	Multiplexing control register for the VIU_DAT1 pin	2-65
0x178	muxctrl_reg94	Multiplexing control register for the VIU_DAT0 pin	2-65

2.3.2 Register Description

muxctrl_reg1

muxctrl_reg1 is a multiplexing control register for the SDIO_CCLK_OUT pin.

Offset Address	Register Name	Total Reset Value
0x004	muxctrl_reg1	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg1
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg1	Multiplexing for the SDIO_CCLK_OUT pin. 0: GPIO1_1 1: SDIO_CCLK_OUT

muxctrl_reg2

muxctrl_reg2 is a multiplexing control register for the SENSOR_CLK pin.

Offset Address	Register Name	Total Reset Value
0x008	muxctrl_reg2	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg2
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg2	Multiplexing for the SENSOR_CLK pin. 0: GPIO1_2 1: SENSOR_CLK

muxctrl_reg6

muxctrl_reg6 is a multiplexing control register for the I2C_SDA pin.

Offset Address	Register Name	Total Reset Value
0x018	muxctrl_reg6	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg6
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg6	Multiplexing for the I2C_SDA pin. 0: GPIO2_0 1: I2C_SDA

muxctrl_reg7

muxctrl_reg7 is a multiplexing control register for the I2C_SCL pin.

Offset Address	Register Name	Total Reset Value
0x01C	muxctrl_reg7	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg7
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg7	Multiplexing for the I2C_SCL pin. 0: GPIO2_1 1: I2C_SCL

muxctrl_reg8

muxctrl_reg8 is a multiplexing control register for the UART1_RTSN pin.

Offset Address	Register Name	Total Reset Value
0x020	muxctrl_reg8	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg8
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg8	Multiplexing for the UART1_RTSN pin. 0: GPIO2_2 1: UART1_RTSN

muxctrl_reg9

muxctrl_reg9 is a multiplexing control register for the UART1_RXD pin.

Offset Address	Register Name	Total Reset Value
0x024	muxctrl_reg9	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg9
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg9	Multiplexing for the UART1_RXD pin. 0: GPIO2_3 1: UART1_RXD

muxctrl_reg11

muxctrl_reg11 is a multiplexing control register for the UART1_TXD pin.

Offset Address	Register Name	Total Reset Value
0x02C	muxctrl_reg11	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg11
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg11	Multiplexing for the UART1_TXD pin. 0: GPIO2_5 1: UART1_TXD

muxctrl_reg12

muxctrl_reg12 is a multiplexing control register for the MII_CRS pin.

Offset Address	Register Name	Total Reset Value
0x030	muxctrl_reg12	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg12	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1: 0]	RW	muxctrl_reg12	Multiplexing for the MII_CRS pin. 00: GPIO3_0 01: MII_CRS 10: VOU1120_DATA10 Other values: reserved

muxctrl_reg13

muxctrl_reg13 is a multiplexing control register for the MII_COL pin.

Offset Address	Register Name	Total Reset Value
0x034	muxctrl_reg13	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg13	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1: 0]	RW	muxctrl_reg13	Multiplexing for the MII_COL pin. 00: GPIO3_1 01: MII_COL 10: VOU1120_DATA9 Other values: reserved

muxctrl_reg14

muxctrl_reg14 is a multiplexing control register for the MII_RXD3 pin.

Offset Address	Register Name	Total Reset Value
0x038	muxctrl_reg14	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg14	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1: 0]	RW	muxctrl_reg14	Multiplexing for the MII_RXD3 pin. 00: GPIO4_3 01: MII_RXD3 10: VOU1120_DATA15 Other values: reserved

muxctrl_reg15

muxctrl_reg15 is a multiplexing control register for the MII_RXD2 pin.

Offset Address	Register Name	Total Reset Value
0x03C	muxctrl_reg15	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg15	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1: 0]	RW	muxctrl_reg15	Multiplexing for the MII_RXD2 pin. 00: GPIO4_2 01: MII_RXD2 10: VOU1120_DATA11 Other values: reserved

muxctrl_reg16

muxctrl_reg16 is a multiplexing control register for the MII_RXD1 pin.

Offset Address	Register Name	Total Reset Value
0x040	muxctrl_reg16	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg16	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1: 0]	RW	muxctrl_reg16	Multiplexing for the MII_RXD1 pin. 00: GPIO4_1 01: MII_RXD1 10: VOU1120_DATA8 Other values: reserved

muxctrl_reg17

muxctrl_reg17 is a multiplexing control register for the MII_RXD0 pin.

Offset Address	Register Name	Total Reset Value
0x044	muxctrl_reg17	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg17	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1: 0]	RW	muxctrl_reg17	Multiplexing for the MII_RXD0 pin. 00: GPIO4_0 01: MII_RXD0 10: VOU1120_DATA12 Other values: reserved

muxctrl_reg18

muxctrl_reg18 is a multiplexing control register for the MII_TXD3 pin.

Offset Address	Register Name	Total Reset Value
0x048	muxctrl_reg18	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg18	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1: 0]	RW	muxctrl_reg18	Multiplexing for the MII_TXD3 pin. 00: GPIO4_7 01: MII_TXD3 10: VOU1120_DATA3 Other values: reserved

muxctrl_reg19

muxctrl_reg19 is a multiplexing control register for the MII_TXD2 pin.

Offset Address	Register Name	Total Reset Value
0x04C	muxctrl_reg19	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg19	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1: 0]	RW	muxctrl_reg19	Multiplexing for the MII_TXD2 pin. 00: GPIO4_6 01: MII_TXD2 10: VOU1120_DATA13 Other values: reserved

muxctrl_reg20

muxctrl_reg20 is a multiplexing control register for the MII_TXD1 pin.

Offset Address	Register Name	Total Reset Value
0x050	muxctrl_reg20	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg20	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1: 0]	RW	muxctrl_reg20	Multiplexing for the MII_TXD1 pin. 00: GPIO4_5 01: MII_TXD1 10: VOU1120_DATA0 Other values: reserved

muxctrl_reg21

muxctrl_reg21 is a multiplexing control register for the MII_TXD0 pin.

Offset Address	Register Name	Total Reset Value
0x054	muxctrl_reg21	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg21	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1: 0]	RW	muxctrl_reg21	Multiplexing for the MII_TXD0 pin. 00: GPIO4_4 01: MII_TXD0 10: VOU1120_DATA4 Other values: reserved

muxctrl_reg22

muxctrl_reg22 is a multiplexing control register for the MII_RXCK pin.

Offset Address	Register Name	Total Reset Value
0x058	muxctrl_reg22	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg22	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1: 0]	RW	muxctrl_reg22	Multiplexing for the MII_RXCK pin. 00: GPIO3_2 01: MII_RXCK 10: VOU1120_CLK Other values: reserved

muxctrl_reg23

muxctrl_reg23 is a multiplexing control register for the MII_TXCK pin.

Offset Address	Register Name	Total Reset Value
0x05C	muxctrl_reg23	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg23	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1: 0]	RW	muxctrl_reg23	Multiplexing for the MII_TXCK pin. 00: GPIO3_3 01: MII_TXCK 10: VOU1120_DATA7 11: RMII_CLK

muxctrl_reg24

muxctrl_reg24 is a multiplexing control register for the MII_RXDV pin.

Offset Address	Register Name	Total Reset Value
0x060	muxctrl_reg24	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg24	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1: 0]	RW	muxctrl_reg24	Multiplexing for the MII_RXDV pin. 00: GPIO3_4 01: MII_RXDV 10: VOU1120_DATA1 Other values: reserved

muxctrl_reg25

muxctrl_reg25 is a multiplexing control register for the MII_TXEN pin.

Offset Address	Register Name	Total Reset Value
0x064	muxctrl_reg25	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg25	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1: 0]	RW	muxctrl_reg25	Multiplexing for the MII_TXEN pin. 00: GPIO3_5 01: MII_TXEN 10: VOU1120_DATA5 Other values: reserved

muxctrl_reg28

muxctrl_reg28 is a multiplexing control register for the EPHY_CLK pin.

Offset Address	Register Name	Total Reset Value
0x070	muxctrl_reg28	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg28	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1: 0]	RW	muxctrl_reg28	Multiplexing for the EPHY_CLK pin. 00: GPIO1_3 01: EPHY_CLK 10: VOU1120_DATA2 Other values: reserved

muxctrl_reg29

muxctrl_reg29 is a multiplexing control register for the MDCK pin.

Offset Address	Register Name	Total Reset Value
0x074	muxctrl_reg29	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg29	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1: 0]	RW	muxctrl_reg29	Multiplexing for the MDCK pin. 00: GPIO3_6 01: MDCK 10: VOU1120_DATA6 11: BOOT_SEL

muxctrl_reg30

muxctrl_reg30 is a multiplexing control register for the MDIO pin.

Offset Address	Register Name	Total Reset Value
0x078	muxctrl_reg30	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg30	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1: 0]	RW	muxctrl_reg30	Multiplexing for the MDIO pin. 00: GPIO3_7 01: MDIO 10: VOU1120_DATA14 Other values: reserved

muxctrl_reg32

muxctrl_reg32 is a multiplexing control register for the SDIO_CARD_DETECT pin.

Offset Address	Register Name	Total Reset Value
0x080	muxctrl_reg32	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg32
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg32	Multiplexing for the SDIO_CARD_DETECT pin. 0: GPIO6_0 1: SDIO_CARD_DETECT

muxctrl_reg33

muxctrl_reg33 is a multiplexing control register for the SDIO_CARD_POWER_EN pin.

Offset Address	Register Name	Total Reset Value
0x084	muxctrl_reg33	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg33
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg33	Multiplexing for the SDIO_CARD_POWER_EN pin. 0: GPIO6_1 1: SDIO_CARD_POWER_EN

muxctrl_reg35

muxctrl_reg35 is a multiplexing control register for the SDIO_CCMD pin.

Offset Address	Register Name	Total Reset Value
0x08C	muxctrl_reg35	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg35
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg35	Multiplexing for the SDIO_CCMD pin. 0: GPIO6_3 1: SDIO_CCMD

muxctrl_reg36

muxctrl_reg36 is a multiplexing control register for the SDIO_CDATA0 pin.

Offset Address	Register Name	Total Reset Value
0x090	muxctrl_reg36	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg36	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[2: 0]	RW	muxctrl_reg36	Multiplexing for the SDIO_CDATA0 pin. 000: GPIO6_4 001: SDIO_CDATA0 010: CLK_TEST_OUT0 011: CLK_TEST_OUT1 100: CLK_TEST_OUT2 101: CLK_TEST_OUT3 Other values: reserved

muxctrl_reg37

muxctrl_reg37 is a multiplexing control register for the SDIO_CDATA1 pin.

Offset Address	Register Name	Total Reset Value
0x094	muxctrl_reg37	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg37	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[2: 0]	RW	muxctrl_reg37	Multiplexing for the SDIO_CDATA1 pin. 000: PLL_TEST_OUT0 001: SDIO_CDATA1 010: GPIO6_5 011: PLL_TEST_OUT1 100: PLL_TEST_OUT2 101: PLL_TEST_OUT3 110: RTC_TEST_CLK

			Other values: reserved

muxctrl_reg38

muxctrl_reg38 is a multiplexing control register for the SDIO_CDATA2 pin.

Offset Address	Register Name	Total Reset Value
0x098	muxctrl_reg38	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg38
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg38	Multiplexing for the SDIO_CDATA2 pin. 0: GPIO6_6 1: SDIO_CDATA2

muxctrl_reg39

muxctrl_reg39 is a multiplexing control register for the SDIO_CDATA3 pin.

Offset Address	Register Name	Total Reset Value
0x09C	muxctrl_reg39	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg39
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg39	Multiplexing for the SDIO_CDATA3 pin. 0: GPIO6_7 1: SDIO_CDATA3

muxctrl_reg40

muxctrl_reg40 is a multiplexing control register for the SFC_DIO pin.

Offset Address	Register Name	Total Reset Value
0x0A0	muxctrl_reg40	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg40
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg40	Multiplexing for the SFC_DIO pin. 0: SFC_DIO 1: GPIO7_0

muxctrl_reg41

muxctrl_reg41 is a multiplexing control register for the SFC_WP_IO2 pin.

Offset Address	Register Name	Total Reset Value
0x0A4	muxctrl_reg41	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg41
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg41	Multiplexing for the SFC_WP_IO2 pin. 0: SFC_WP_IO2 1: GPIO7_1

muxctrl_reg42

muxctrl_reg42 is a multiplexing control register for the SFC_CLK pin.

Offset Address	Register Name	Total Reset Value
0x0A8	muxctrl_reg42	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								muxctrl_reg42
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[1: 0]	RW	muxctrl_reg42	Multiplexing for the SFC_CLK pin. 00: SFC_CLK 01: GPIO7_2 10: SFC_ADDR_MODE Other values: reserved

muxctrl_reg43

muxctrl_reg43 is a multiplexing control register for the SFC_DOI pin.

Offset Address	Register Name	Total Reset Value
0x0AC	muxctrl_reg43	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								muxctrl_reg43
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg43	Multiplexing for the SFC_DOI pin. 0: SFC_DOI 1: GPIO7_3

muxctrl_reg44

muxctrl_reg44 is a multiplexing control register for the SFC_HOLD_IO3 pin.

Offset Address	Register Name	Total Reset Value
0x0B0	muxctrl_reg44	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg44
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg44	Multiplexing for the SFC_HOLD_IO3 pin. 0: SFC_HOLD_IO3 1: GPIO7_4

muxctrl_reg46

muxctrl_reg46 is a multiplexing control register for the USB_PWREN pin.

Offset Address	Register Name	Total Reset Value
0x0B8	muxctrl_reg46	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg46
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg46	Multiplexing for the USB_PWREN pin. 0: GPIO5_1 1: USB_PWREN

muxctrl_reg47

muxctrl_reg47 is a multiplexing control register for the PWM_OUT0 pin.

Offset Address	Register Name	Total Reset Value
0x0BC	muxctrl_reg47	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg47
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg47	Multiplexing for the PWM_OUT0 pin. 0: GPIO5_2 1: PWM_OUT0

muxctrl_reg48

muxctrl_reg48 is a multiplexing control register for the PWM_OUT1 pin.

Offset Address	Register Name	Total Reset Value
0x0C0	muxctrl_reg48	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg48
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg48	Multiplexing for the PWM_OUT1 pin. 0: GPIO5_3 1: PWM_OUT1

muxctrl_reg72

muxctrl_reg72 is a multiplexing control register for the JTAG_TRSTN pin.

Offset Address	Register Name	Total Reset Value
0x120	muxctrl_reg72	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							muxctrl_reg72
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[1: 0]	RW	muxctrl_reg72	Multiplexing for the JTAG_TRSTN pin. 00: GPIO0_0 01: JTAG_TRSTN 10: TEMPER_DQ Other values: reserved

muxctrl_reg73

muxctrl_reg73 is a multiplexing control register for the JTAG_TCK pin.

Offset Address	Register Name	Total Reset Value
0x124	muxctrl_reg73	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							muxctrl_reg73
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[1: 0]	RW	muxctrl_reg73	Multiplexing for the JTAG_TCK pin. 00: GPIO0_1 01: JTAG_TCK 10: TEMPER_DQ Other values: reserved

muxctrl_reg74

muxctrl_reg74 is a multiplexing control register for the JTAG_TMS pin.

Offset Address	Register Name	Total Reset Value
0x128	muxctrl_reg74	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg74	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1: 0]	RW	muxctrl_reg74	Multiplexing for the JTAG_TMS pin. 00: GPIO0_2 01: JTAG_TMS 10: TEMPER_DQ Other values: reserved

muxctrl_reg75

muxctrl_reg75 is a multiplexing control register for the JTAG_TDO pin.

Offset Address	Register Name	Total Reset Value
0x12C	muxctrl_reg75	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg75	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1: 0]	RW	muxctrl_reg75	Multiplexing for the JTAG_TDO pin. 00: GPIO0_3 01: JTAG_TDO 10: TEMPER_DQ Other values: reserved

muxctrl_reg76

muxctrl_reg76 is a multiplexing control register for the JTAG_TDI pin.

Offset Address	Register Name	Total Reset Value
0x130	muxctrl_reg76	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg76	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1: 0]	RW	muxctrl_reg76	Multiplexing for the JTAG_TDI pin. 00: GPIO0_4 01: JTAG_TDI 10: TEMPER_DQ Other values: reserved

muxctrl_reg77

muxctrl_reg77 is a multiplexing control register for the GPIO0_5 pin.

Offset Address	Register Name	Total Reset Value
0x134	muxctrl_reg77	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg77	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1: 0]	RW	muxctrl_reg77	Multiplexing for the GPIO0_5 pin. 00: SVB_PWM 01: GPIO0_5 10: TEMPER_DQ Other values: reserved

muxctrl_reg78

muxctrl_reg78 is a multiplexing control register for the GPIO0_6 pin.

Offset Address	Register Name	Total Reset Value
0x138	muxctrl_reg78	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg78	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1: 0]	RW	muxctrl_reg78	Multiplexing for the GPIO0_6 pin. 00: GPIO0_6 01: SVB_PWM 10: TEMPER_DQ Other values: reserved

muxctrl_reg79

muxctrl_reg79 is a multiplexing control register for the GPIO0_7 pin.

Offset Address	Register Name	Total Reset Value
0x13C	muxctrl_reg79	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg79	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[1: 0]	RW	muxctrl_reg79	Multiplexing for the GPIO0_7 pin. 00: SYS_RSTN_OUT 01: GPIO0_7 10: TEMPER_DQ Other values: reserved

muxctrl_reg80

muxctrl_reg80 is a multiplexing control register for the VIU_CLK pin.

Offset Address	Register Name	Total Reset Value
0x140	muxctrl_reg80	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg80
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg80	Multiplexing for the VIU_CLK pin. 0: VIU_CLK 1: GPIO11_6

muxctrl_reg81

muxctrl_reg81 is a multiplexing control register for the VIU_VS pin.

Offset Address	Register Name	Total Reset Value
0x144	muxctrl_reg81	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg81
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg81	Multiplexing for the VIU_VS pin. 0: VIU_VS 1: GPIO11_5

muxctrl_reg82

muxctrl_reg82 is a multiplexing control register for the VIU_HS pin.

Offset Address	Register Name	Total Reset Value
0x148	muxctrl_reg82	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg82
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg82	Multiplexing for the VIU_HS pin. 0: VIU_HS 1: GPIO11_4

muxctrl_reg83

muxctrl_reg83 is a multiplexing control register for the VIU_DAT11 pin.

Offset Address	Register Name	Total Reset Value
0x14C	muxctrl_reg83	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg83
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg83	Multiplexing for the VIU_DAT11 pin. 0: VIU_DAT11 1: GPIO11_3

muxctrl_reg84

muxctrl_reg84 is a multiplexing control register for the VIU_DAT10 pin.

Offset Address	Register Name	Total Reset Value
0x150	muxctrl_reg84	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg84
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg84	Multiplexing for the VIU_DAT10 pin. 0: VIU_DAT10 1: GPIO11_2

muxctrl_reg85

muxctrl_reg85 is a multiplexing control register for the VIU_DAT9 pin.

Offset Address	Register Name	Total Reset Value
0x154	muxctrl_reg85	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg85
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg85	Multiplexing for the VIU_DAT9 pin. 0: VIU_DAT9 1: GPIO11_1

muxctrl_reg86

muxctrl_reg86 is a multiplexing control register for the VIU_DAT8 pin.

Offset Address	Register Name	Total Reset Value
0x158	muxctrl_reg86	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg86
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg86	Multiplexing for the VIU_DAT8 pin. 0: VIU_DAT8 1: GPIO11_0

muxctrl_reg87

muxctrl_reg87 is a multiplexing control register for the VIU_DAT7 pin.

Offset Address	Register Name	Total Reset Value
0x15C	muxctrl_reg87	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg87
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg87	Multiplexing for the VIU_DAT7 pin. 0: VIU_DAT7 1: GPIO10_7

muxctrl_reg88

muxctrl_reg88 is a multiplexing control register for the VIU_DAT6 pin.

Offset Address	Register Name	Total Reset Value
0x160	muxctrl_reg88	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg88
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg88	Multiplexing for the VIU_DAT6 pin. 0: VIU_DAT6 1: GPIO10_6

muxctrl_reg89

muxctrl_reg89 is a multiplexing control register for the VIU_DAT5 pin.

Offset Address	Register Name	Total Reset Value
0x164	muxctrl_reg89	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg89
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg89	Multiplexing for the VIU_DAT5 pin. 0: VIU_DAT5 1: GPIO10_5

muxctrl_reg90

muxctrl_reg90 is a multiplexing control register for the VIU_DAT4 pin.

Offset Address	Register Name	Total Reset Value
0x168	muxctrl_reg90	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg90
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg90	Multiplexing for the VIU_DAT4 pin. 0: VIU_DAT4 1: GPIO10_4

muxctrl_reg91

muxctrl_reg91 is a multiplexing control register for the VIU_DAT3 pin.

Offset Address	Register Name	Total Reset Value
0x16C	muxctrl_reg91	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg91
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg91	Multiplexing for the VIU_DAT3 pin. 0: VIU_DAT3 1: GPIO10_3

muxctrl_reg92

muxctrl_reg92 is a multiplexing control register for the VIU_DAT2 pin.

Offset Address	Register Name	Total Reset Value
0x170	muxctrl_reg92	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg92
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg92	Multiplexing for the VIU_DAT2 pin. 0: VIU_DAT2 1: GPIO10_2

muxctrl_reg93

muxctrl_reg93 is a multiplexing control register for the VIU_DAT1 pin.

Offset Address	Register Name	Total Reset Value
0x174	muxctrl_reg93	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg93
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg93	Multiplexing for the VIU_DAT1 pin. 0: VIU_DAT1 1: GPIO10_1

muxctrl_reg94

muxctrl_reg94 is a multiplexing control register for the VIU_DAT0 pin.

Offset Address	Register Name	Total Reset Value
0x178	muxctrl_reg94	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg94
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	muxctrl_reg94	Multiplexing for the VIU_DAT0 pin. 0: VIU_DAT0 1: GPIO10_0

2.4 Software Multiplexed Pins

Table 2-26lists the software multiplexed pins of the VI interface.

Table 2-26 Software multiplexed pins of the sensor

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
67	SENSOR_CLK	muxctrl_reg2	GPIO1_2	SENSOR_CLK
66	VIU_CLK	muxctrl_reg80	VIU_CLK	GPIO11_6
51	VIU_VS	muxctrl_reg81	VIU_VS	GPIO11_5
50	VIU_HS	muxctrl_reg82	VIU_HS	GPIO11_4
65	VIU_DAT11	muxctrl_reg83	VIU_DAT11	GPIO11_3
64	VIU_DAT10	muxctrl_reg84	VIU_DAT10	GPIO11_2
63	VIU_DAT9	muxctrl_reg85	VIU_DAT9	GPIO11_1
62	VIU_DAT8	muxctrl_reg86	VIU_DAT8	GPIO11_0
61	VIU_DAT7	muxctrl_reg87	VIU_DAT7	GPIO10_7
60	VIU_DAT6	muxctrl_reg88	VIU_DAT6	GPIO10_6
57	VIU_DAT5	muxctrl_reg89	VIU_DAT5	GPIO10_5

56	VIU_DAT4	muxctrl_reg90	VIU_DAT4	GPIO10_4
55	VIU_DAT3	muxctrl_reg91	VIU_DAT3	GPIO10_3
54	VIU_DAT2	muxctrl_reg92	VIU_DAT2	GPIO10_2
53	VIU_DAT1	muxctrl_reg93	VIU_DAT1	GPIO10_1
52	VIU_DAT0	muxctrl_reg94	VIU_DAT0	GPIO10_0

Table 2-27 describes the software multiplexed signals of the sensor.

Table 2-27 Software multiplexed signals of the sensor

Signal	Direction	Description
GPIO1_2	I/O	GPIO
GPIO10_0	I/O	GPIO
GPIO10_1	I/O	GPIO
GPIO10_2	I/O	GPIO
GPIO10_3	I/O	GPIO
GPIO10_4	I/O	GPIO
GPIO10_5	I/O	GPIO
GPIO10_6	I/O	GPIO
GPIO10_7	I/O	GPIO
GPIO11_0	I/O	GPIO
GPIO11_1	I/O	GPIO
GPIO11_2	I/O	GPIO
GPIO11_3	I/O	GPIO
GPIO11_4	I/O	GPIO
GPIO11_5	I/O	GPIO
GPIO11_6	I/O	GPIO
SENSOR_CLK	O	Sensor working clock
VIU_CLK	I	VIU clock
VIU_DAT0	I	VIU data input
VIU_DAT1	I	VIU data input
VIU_DAT10	I	VIU data input

Signal	Direction	Description
VIU_DAT11	I	VIU data input
VIU_DAT2	I	VIU data input
VIU_DAT3	I	VIU data input
VIU_DAT4	I	VIU data input
VIU_DAT5	I	VIU data input
VIU_DAT6	I	VIU data input
VIU_DAT7	I	VIU data input
VIU_DAT8	I	VIU data input
VIU_DAT9	I	VIU data input
VIU_HS	I	VIU horizontal sync, active high
VIU_VS	I	VIU vertical sync, active high

I²C

Table 2-28 lists the software multiplexed pins of the I²C interface.

Table 2-28 Software multiplexed pins of the I²C interface

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
68	I2C_SDA	muxctrl_reg6	GPIO2_0	I2C_SDA
70	I2C_SCL	muxctrl_reg7	GPIO2_1	I2C_SCL

Table 2-29 describes the software multiplexed signals of the I²C interface.

Table 2-29 Software multiplexed signals of the I²C interface

Signal	Direction	Description
GPIO2_0	I/O	GPIO
GPIO2_1	I/O	GPIO
I2C_SCL	I/O	I²C bus clock, OD output
I2C_SDA	I/O	I²C bus data/address, OD output

ETH

Table 2-30 lists the software multiplexed pins of the ETH port.

Table 2-30 Software multiplexed pins of the ETH port

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2	Multiplexed Signal 3
133	MII_CRS	muxctrl_reg12	GPIO3_0	MII_CRS	VOU1120_DATA 10	None
134	MII_COL	muxctrl_reg13	GPIO3_1	MII_COL	VOU1120_DATA 9	None
139	MII_RXD3	muxctrl_reg14	GPIO4_3	MII_RXD3	VOU1120_DATA 15	None
137	MII_RXD2	muxctrl_reg15	GPIO4_2	MII_RXD2	VOU1120_DATA 11	None
138	MII_RXD1	muxctrl_reg16	GPIO4_1	MII_RXD1	VOU1120_DATA 8	None
135	MII_RXD0	muxctrl_reg17	GPIO4_0	MII_RXD0	VOU1120_DATA 12	None
125	MII_TXD3	muxctrl_reg18	GPIO4_7	MII_TXD3	VOU1120_DATA 3	None
127	MII_TXD2	muxctrl_reg19	GPIO4_6	MII_TXD2	VOU1120_DATA 13	None
128	MII_TXD1	muxctrl_reg20	GPIO4_5	MII_TXD1	VOU1120_DATA 0	None
129	MII_TXD0	muxctrl_reg21	GPIO4_4	MII_TXD0	VOU1120_DATA 4	None
141	MII_RXCK	muxctrl_reg22	GPIO3_2	MII_RXCK	VOU1120_CLK	None
131	MII_TXCK	muxctrl_reg23	GPIO3_3	MII_TXCK	VOU1120_DATA 7	RMII_CLK
124	MII_RXDV	muxctrl_reg24	GPIO3_4	MII_RXDV	VOU1120_DATA 1	None
130	MII_TXEN	muxctrl_reg25	GPIO3_5	MII_TXEN	VOU1120_DATA 5	None
123	EPHY_CLK	muxctrl_reg28	GPIO1_3	EPHY_CLK	VOU1120_DATA 2	None
132	MDCK	muxctrl_reg29	GPIO3_6	MDCK	VOU1120_DATA 6	BOOT_SEL
140	MDIO	muxctrl_reg30	GPIO3_7	MDIO	VOU1120_DATA 14	None

Table 2-31 describes the software multiplexed signals of the ETH port.

Table 2-31 Software multiplexed signals of the ETH port

Signal	Direction	Description
BOOT_SEL	I	Storage medium select for booting. This signal must be pulled down, which indicates that the system boots from the SPI flash.
EPHY_CLK	O	Working clock of the MII PHY
GPIO1_3	I/O	GPIO
GPIO3_0	I/O	GPIO
GPIO3_1	I/O	GPIO
GPIO3_2	I/O	GPIO
GPIO3_3	I/O	GPIO
GPIO3_4	I/O	GPIO
GPIO3_5	I/O	GPIO
GPIO3_6	I/O	GPIO
GPIO3_7	I/O	GPIO
GPIO4_0	I/O	GPIO
GPIO4_1	I/O	GPIO
GPIO4_2	I/O	GPIO
GPIO4_3	I/O	GPIO
GPIO4_4	I/O	GPIO
GPIO4_5	I/O	GPIO
GPIO4_6	I/O	GPIO
GPIO4_7	I/O	GPIO
MDCK	O	MDIO clock output
MDIO	I/O	MDIO input/output
MII_COL	I	MII collision indicator
MII_CRS	I	MII carrier sense signal
MII_RXCK	I	MII RX clock
MII_RXD0	I	RMII or MII RX data
MII_RXD1	I	RMII or MII RX data
MII_RXD2	I	MII RX data

Signal	Direction	Description
MII_RXD3	I	MII RX data
MII_RXDV	I	MII RX data validity indicator
MII_TXCK	I	MII TX clock
MII_TXD0	O	RMII or MII TX data
MII_TXD1	O	RMII or MII TX data
MII_TXD2	O	MII TX DATA
MII_TXD3	O	MII TX DATA
MII_TXEN	O	MII TX DATA ENABLE
RMII_CLK	I/O	RMII clock
VOU1120_CLK	O	BT.1120 clock output
VOU1120_DATA0	O	BT.1120 luminance signal output
VOU1120_DATA1	O	BT.1120 luminance signal output
VOU1120_DATA10	O	BT.1120 chrominance signal output
VOU1120_DATA11	O	BT.1120 chrominance signal output
VOU1120_DATA12	O	BT.1120 chrominance signal output
VOU1120_DATA13	O	BT.1120 chrominance signal output
VOU1120_DATA14	O	BT.1120 chrominance signal output
VOU1120_DATA15	O	BT.1120 chrominance signal output
VOU1120_DATA2	O	BT.1120 luminance signal output
VOU1120_DATA3	O	BT.1120 luminance signal output
VOU1120_DATA4	O	BT.1120 luminance signal output
VOU1120_DATA5	O	BT.1120 luminance signal output
VOU1120_DATA6	O	BT.1120 luminance signal output
VOU1120_DATA7	O	BT.1120 luminance signal output
VOU1120_DATA8	O	BT.1120 chrominance signal output
VOU1120_DATA9	O	BT.1120 chrominance signal output

SFC

Table 2-32 lists the software multiplexed pins of the SFC.

Table 2-32 Software multiplexed pins of the SFC

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2
117	SFC_DIO	muxctrl_reg40	SFC_DIO	GPIO7_0	None
122	SFC_WP_IO2	muxctrl_reg41	SFC_WP_IO2	GPIO7_1	None
120	SFC_CLK	muxctrl_reg42	SFC_CLK	GPIO7_2	SFC_ADDR_MODE
119	SFC_DOI	muxctrl_reg43	SFC_DOI	GPIO7_3	None
122	SFC_HOLD_IO3	muxctrl_reg44	SFC_HOLD_IO3	GPIO7_4	None

Table 2-33 describes the software multiplexed signals of the SFC.

Table 2-33 Software multiplexed signals of the SFC

Signal	Direction	Description
GPIO7_0	I/O	GPIO
GPIO7_1	I/O	GPIO
GPIO7_2	I/O	GPIO
GPIO7_3	I/O	GPIO
GPIO7_4	I/O	GPIO
SFC_ADDR_MODE	I	Default address mode of the SFC. 0: 3-byte address mode 1: 4-byte address mode
SFC_CLK	O	Clock signal transmitted to the SPI flash. The high level or low level can be configured when the clock is not switched.
SFC_DIO	I/O	Data output signal in standard SPI mode Data I/O signal in dual-SPI mode Data I/O signal in quad-SPI mode
SFC_DOI	I/O	Data input signal in standard SPI mode Data I/O signal in dual-SPI mode Data I/O signal in quad-SPI mode
SFC_HOLD_IO3	I/O	Hold function in standard SPI mode, active low Hold function in dual-SPI mode, active low Data I/O signal in quad-SPI mode

Signal	Direction	Description
SFC_WP_IO2	I/O	Write protection function in standard SPI mode, active low Write protection function in dual-SPI mode, active low Data I/O signal in quad-SPI mode

USB

Table 2-34 lists the software multiplexed pin of the USB port.

Table 2-34 Software multiplexed pin of the USB port

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
105	USB_PWREN	muxctrl_reg46	GPIO5_1	USB_PWREN

Table 2-35 describes the software multiplexed signals of the USB port.

Table 2-35 Software multiplexed signals of the USB port

Signal	Direction	Description
GPIO5_1	I/O	GPIO
USB_PWREN	O	Power control output of USB port 0, configurable level, and active low by default

PWM

Table 2-36 lists the software multiplexed pins of the PWM interface.

Table 2-36 Software multiplexed pins of the PWM interface.

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
72	PWM_OUT0	muxctrl_reg47	GPIO5_2	PWM_OUT0
73	PWM_OUT1	muxctrl_reg48	GPIO5_3	PWM_OUT1

Table 2-37describes the software multiplexed signals of the PWM interface.

Table 2-37 Software multiplexed signals of the PWM interface

Signal	Direction	Description
GPIO5_2	I/O	GPIO
GPIO5_3	I/O	GPIO
PWM_OUT0	O	PWM output 0
PWM_OUT1	O	PWM output 1

SDIO

Table 2-38 lists the software multiplexed pins of the SDIO interface.

Table 2-38 Software multiplexed pins of the SDIO interface

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signals 1–6
106	SDIO_CCLK_OUT	muxctrl_reg1	GPIO1_1	1: SDIO_CCLK_OUT
107	SDIO_CARD_DETECT	muxctrl_reg32	GPIO6_0	1: SDIO_CARD_DETECT
108	SDIO_CARD_POWER_EN	muxctrl_reg33	GPIO6_1	1: SDIO_CARD_POWER_EN
110	SDIO_CCMD	muxctrl_reg35	GPIO6_3	1: SDIO_CCMD
111	SDIO_CDATA0	muxctrl_reg36	GPIO6_4	1: SDIO_CDATA0 2: CLK_TEST_OUT0 3: CLK_TEST_OUT1 4: CLK_TEST_OUT2: 5: CLK_TEST_OUT3-
112	SDIO_CDATA1	muxctrl_reg37	PLL_TEST_OUT0	1: SDIO_CDATA1 2: GPIO6_5 3: PLL_TEST_OUT1 4: PLL_TEST_OUT2 5: PLL_TEST_OUT3 6: RTC_TEST_CLK
114	SDIO_CDATA2	muxctrl_reg38	GPIO6_6	1: SDIO_CDATA2
115	SDIO_CDATA3	muxctrl_reg39	GPIO6_7	1: SDIO_CDATA3

Table 2-39 describes the software multiplexed signals of the SDIO interface.

Table 2-39 Software multiplexed signals of the SDIO interface

Signal	Direction	Description
CLK_TEST_OUT0	O	Main test clock output
CLK_TEST_OUT1	O	Main test clock output
CLK_TEST_OUT2	O	Main test clock output
CLK_TEST_OUT3	O	Main test clock output
GPIO1_1	I/O	GPIO
GPIO6_0	I/O	GPIO
GPIO6_1	I/O	GPIO
GPIO6_3	I/O	GPIO
GPIO6_4	I/O	GPIO
GPIO6_5	I/O	GPIO
GPIO6_6	I/O	GPIO
GPIO6_7	I/O	GPIO
PLL_TEST_OUT0	O	PLL test clock output
PLL_TEST_OUT1	O	PLL test clock output
PLL_TEST_OUT2	O	PLL test clock output
PLL_TEST_OUT3	O	PLL test clock output
RTC_TEST_CLK	O	RTC test clock output
SDIO_CARD_DETECT	I	Card detection signal, active low
SDIO_CARD_POWER_EN	O	Power enable signal. The value 1 indicates power on.
SDIO_CCLK_OUT	O	Output working clock for the card
SDIO_CCMD	I/O	Card command
SDIO_CDATA0	I/O	Card data
SDIO_CDATA1	I/O	Card data
SDIO_CDATA2	I/O	Card data
SDIO_CDATA3	I/O	Card data

UART1

Table 2-40 lists the software multiplexed pins of UART 1.

Table 2-40 Software multiplexed pins of UART 1

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
86	UART1_RTSN	muxctrl_reg8	GPIO2_2	UART1_RTSN
88	UART1_RXD	muxctrl_reg9	GPIO2_3	UART1_RXD
87	UART1_TXD	muxctrl_reg11	GPIO2_5	UART1_TXD

Table 2-41 describes the software multiplexed signals of UART 1.

Table 2-41 Software multiplexed signals of UART 1

Signal	Direction	Description
GPIO2_2	I/O	GPIO
GPIO2_3	I/O	GPIO
GPIO2_5	I/O	GPIO
UART1_RTSN	O	Modem state output: RTS, active low. The reset value is 0.
UART1_RXD	I	UART 1 RX data
UART1_TXD	O	UART 1 TX data

JTAG

Table 2-42 lists the software multiplexed pins of the JTAG interface.

Table 2-42 Software multiplexed pins of the JTAG interface

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2
74	JTAG_TRSTN	muxctrl_reg72	GPIO0_0	JTAG_TRSTN	TEMPER_DQ
76	JTAG_TCK	muxctrl_reg73	GPIO0_1	JTAG_TCK	TEMPER_DQ
77	JTAG_TMS	muxctrl_reg74	GPIO0_2	JTAG_TMS	TEMPER_DQ
78	JTAG_TDO	muxctrl_reg75	GPIO0_3	JTAG_TDO	TEMPER_DQ
79	JTAG_TDI	muxctrl_reg76	GPIO0_4	JTAG_TDI	TEMPER_DQ

Table 2-43 describes the software multiplexed signals of the JTAG interface.

Table 2-43 Software multiplexed signals of the JTAG interface

Signal	Direction	Description
GPIO0_0	I/O	GPIO
GPIO0_1	I/O	GPIO
GPIO0_2	I/O	GPIO
GPIO0_3	I/O	GPIO
GPIO0_4	I/O	GPIO
JTAG_TCK	I	JTAG clock input
JTAG_TDI	I	JTAG data input
JTAG_TDO	O	JTAG data output
JTAG_TMS	I	JTAG mode select input.
JTAG_TRSTN	I	JTAG reset input
SYS_RSTN_OUT	O	System reset output
TEMPER_DQ	I/O	Temperature measurement. It is used to communicate with the external temperature measurement chip.

NOTE

The default function of the JTAG pin is selected by setting JTAG_EN (pull-up or pull-down).

- If JTAG_EN is 1'b0 (pull-down) during chip reset, the default function of the JTAG pin is GPIO. The function can be changed by configuring multiplexing control registers.
- If JTAG_EN is 1'b1 (pull-up) during chip reset, the default function of the JTAG pin is JTAG. The function can be changed by configuring multiplexing control registers.

GPIO

Table 2-44 lists the software multiplexed pins of the GPIO interface.

Table 2-44 Software multiplexed pins of the GPIO interface

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2
80	GPIO0_5	muxctrl_reg77	SVB_PWM	GPIO0_5	TEMPER_DQ
81	GPIO0_6	muxctrl_reg78	GPIO0_6	SVB_PWM	TEMPER_DQ
82	GPIO0_7	muxctrl_reg79	SYS_RSTN_OUT	GPIO0_7	TEMPER_DQ

Table 2-45 describes the software multiplexed signals of the GPIO interface.

Table 2-45 Software multiplexed signals of the GPIO interface

Signal	Direction	Description
GPIO0_5	I/O	GPIO
GPIO0_6	I/O	GPIO
GPIO0_7	I/O	GPIO
SVB_PWM	O	SVB control signal output
SYS_RSTN_OUT	O	System reset output
TEMPER_DQ	I/O	Temperature measurement. It is used to communicate with the external temperature measurement chip.

2.5 Hardware Multiplexed Pins

MDIO

Table 2-46 lists the hardware multiplexed pin of the MDIO interface.

Table 2-46 Hardware multiplexed pin of the MDIO interface

Pin	Pad Signal	Multiplexed Signal 1 (power_on == 1'b1)
132	MDCK	BOOT_SEL

Table 2-47 describes the hardware multiplexed signal of the MDIO interface.

Table 2-47 Hardware multiplexed signal of the MDIO interface

Signal	Direction	Description
BOOT_SEL	I	Storage medium select for booting. This signal must be pulled down, which indicates that the system boots from the SPI flash.

SFC

Table 2-48 lists the hardware multiplexed pin of the SFC.

Table 2-48 Hardware multiplexed pin of the SFC

Pin	Pad Signal	Multiplexed Signal 1 (power_on == 1'b1)
120	SFC_CLK	SFC_ADDR_MODE

Table 2-49 describes the hardware multiplexed signal of the SFC.

Table 2-49 Hardware multiplexed signal of the SFC

Signal	Direction	Description
SFC_ADDR_MODE	I	Default address mode of the SFC. 0: 3-byte address mode 1: 4-byte address mode

2.6 Electrical Specifications

2.6.1 Power Supply Specifications

Table 2-50 describes the power consumption specifications.

CAUTION

- The values for power consumption parameters are provided based on typical application scenarios.
- Design board power supplies by following the *Hi3518 Hardware Design User Guide*.

Table 2-50 Power consumption specifications

Type	Description	Typ	Max	Unit
Core power	Core power	None	None	mA
3.3 V power	Interface power	None	None	mA
2.5V power	Interface power	None	None	mA
DVDD1518 power	Power supply of the DDR interface	None	None	mA

2.6.2 Temperature and Thermal Resistance Parameters

Table 2-51 describes the temperature and thermal resistance parameters.

NOTE

- The thermal resistance is provided in compliance with the JEDEC JESD51-2 standard. The actual system design and environment may be different.
- The chip junction temperature is proportional to the chip power consumption. Ensure that the junction temperature is appropriate to match power supplies.
- Design heat dissipation by following the *Hi3518 Hardware Design User Guide*.

Table 2-51 Hi3518C Temperature and thermal resistance parameters

Parameter	Symbol	Min	Typ	Max	Unit
Recommended ambient temperature	T_A	0	None	70	ºC
Limited junction temperature	T_{JMAX}	–20	None	110	ºC
Junction-to-ambient thermal resistance	θ_{JA}	None	25	None	ºC/W
Junction-to-board thermal resistance	θ_{JB}	None	8.5	None	ºC/W
Junction-to-case thermal resistance	θ_{JC}	None	5.5	None	ºC/W

2.6.3 Working Conditions

Table 2-52 describes working conditions.

Table 2-52 Working conditions

Symbol	Description	Min	Typ	Max	Unit
DVDD12	Core power	-5%	1.2	+5%	V
DVDD33	I/O power	2.97	3.3	3.63	V
DVDD3318	I/O power	1.62	1.8	1.98	V
	I/O power	2.97	3.3	3.63	V
DDR_VDDQ	DDR2 I/O power	1.7	1.8	1.9	V
	DDR3 I/O power	1.425	1.5	1.575	V
DDR_REF0 DDR_REF1 DDR_REF2	DDR2/DDR3 reference voltage	0.49 x DDR_VDDQ	0.5 x DDR_VDDQ	0.51 x DDR_VDDQ	V
AVDD12_PLL	PLL digital power	1.08	1.2	1.32	V

Symbol	Description	Min	Typ	Max	Unit
AVDD33_PLL	PLL analog power	2.97	3.3	3.63	V
AVDD_ADC	SAR_ADC analog power	2.97	3.3	3.63	V
AVDD_AC	Audio CODEC analog power	3	3.3	3.6V	V
AVDD33_USB	USB analog power	–7%	3.3	+10%	V
AVDD33_USB25	USB analog power	–7%	3.3	+10%	V
AVDD_BAT	RTC battery power	1.6v	3.0	3.0V	V
AVDD33_RTC	RTC analog power	–10%	3.3	+10%	V

2.6.4 DC and AC Electrical Specifications

Table 2-53 to Table 2-54 describes direct current (DC) electrical specifications.

Table 2-53 DC electrical specifications (DVDD33/DVDD3318 = 3.3 V, incompatible with the 5 V input current)

Symbol	Description	Min	Typ	Max	Unit	Remarks
DVDD12	Core voltage	-5%	1.2	+5%	V	None
DVDD33/DVDD3318	Interface voltage	2.97	3.3	3.63	V	When DVDD3318 is 3.3 V, the I/O voltage of SPI0, VI, or sensor_clk is 3.3 V.
V_{IH}	Input high voltage	2.0	None	DVDD33 + 0.3	V	The interface is incompatible with the 5 V input current. The maximum voltage is (DVDD33 + 0.3) V.
V_{IL}	Input low voltage	–0.3	None	0.8	V	None
I_L	Input leakage current	None	None	±1	μA	None
I_{OZ}	Tristate output leakage current	None	None	±1	μA	None

Symbol	Description	Min	Typ	Max	Unit	Remarks
V_{OH}	Output high voltage	2.4	None	None	V	None
V_{OL}	Output low voltage	None	None	0.4	V	None
R_{PU}	Internal pull-up resistor	33	41	62	kΩ	None
R_{PD}	Internal pull-down resistor	33	42	68	kΩ	None

Table 2-54 DC electrical specifications (DVDD3318 = 1.8 V)

Symbol	Description	Min	Typ	Max	Unit	Remarks
DVDD12	Core voltage	-5%	1.2	+5%	V	None
DVDD3318	Interface voltage	1.62	1.8	1.98	V	When DVDD3318 is 1.8 V, the I/O voltage of SPI0, VI, or sensor_clk is 1.8 V.
V_{IH}	Input high voltage	0.65 x DVDD3318	None	DVDD3318 + 0.3	V	None
V_{IL}	Input low voltage	–0.3	None	0.35 x DVDD3318	V	None
I_L	Input leakage current	None	None	±1	μA	None
I_{OZ}	Tristate output leakage current	None	None	±1	μA	None
V_{OH}	Output high voltage	DVDD3318 – 0.45	None	None	V	None
V_{OL}	Output low voltage	None	None	0.45	V	None
R_{PU}	Internal pull-up resistor	67	93	152	kΩ	None
R_{PD}	Internal pull-down resistor	64	92	170	kΩ	None

Table 2-55 describes the DC electrical specifications in DDR2 mode.

Table 2-55 DC electrical specifications in DDR2 SSTL18 mode (DDR_VDDQ = 1.8 V)

Symbol	Description	Min	Typ	Max	Unit	Remarks
DDR_VDDQ	Interface voltage	1.7	1.8	1.9	V	None
DDR_VREF	Reference voltage	0.49 x VDDQ	0.5 x VDDQ	0.51 x VDDQ	V	None
VTT	Termination voltage	DDR_VREF – 40	DDR_VREF	DDR_VREF + 40	mV	None
$V_{IH(DC)}$	Input high voltage	DDR_VREF+0.125	None	VDDQ + 0.3	V	None
$V_{IL(DC)}$	Input low voltage	–0.3	None	DDR_VREF – 0.125	V	None
V_{OH}	Output high voltage	VDDQ – 0.28	None	None	V	None
V_{OL}	Output low voltage	None	None	VDDQ + 0.28	V	None
I_{OH}	Output high current	None	8.21	9.43	mA	The values are provided when the DDR driver impedance is 40 Ω and RTT is 75 Ω.
I_{OL}	Output low current	None	8.21	9.43	mA	The values are provided when the DDR driver impedance is 40 Ω and RTT is 75 Ω.

Table 2-56 describes the alternating current (AC) electrical specifications in DDR2 mode.

Table 2-56 AC electrical specifications in DDR2 mode (DDR_VDDQ = 1.8 V)

Symbol	Description	400–1067 Mbit/s		Unit
		Min	Max	
$V_{IH(AC)}$	AC input high voltage	DDR_VREF + 0.25	None	V
$V_{IL(AC)}$	AC input low voltage	None	DDR_VREF – 0.25	V

Table 2-57 describes the DC electrical specifications in DDR3 mode.

Table 2-57 DC electrical specifications in DDR3 SSTL15 mode (DDR_VDDQ = 1.5 V)

Symbol	Description	Min	Typ	Max	Unit	Remarks
DDR_VDDQ	Interface voltage	1.425	1.5	1.575	V	None
DDR_VREF	Reference voltage	0.49 x VDDQ	0.5 x VDDQ	0.51 x VDDQ	V	None
VTT	Termination voltage	DDR_VREF – 40	DDR_VREF	DDR_VREF + 40	mV	None
$V_{IH(DC)}$	Input high voltage	DDR_VREF + 0.1	None	VDDQ	V	None
$V_{IL(DC)}$	Input low voltage	–0.3	None	DDR_VREF – 0.1	V	None
V_{OH}	Output high voltage	VDDQ x 0.8	None	None	V	None
V_{OL}	Output low voltage	None	None	0.2 x VDDQ	V	None
I_{OH}	Output high current	None	8.5	9.54	mA	The values are provided when the DDR driver impedance is 34 Ω and RTT is 60 Ω.

Symbol	Description	Min	Typ	Max	Unit	Remarks
I_{OL}	Output low current	None	8.5	9.54	mA	The values are provided when the DDR driver impedance is 34 Ω and RTT is 60 Ω.

Table 2-58 describes the AC electrical specifications in DDR3 mode.

Table 2-58 AC electrical specifications in DDR3 mode (DDR_VDDQ = 1.5 V)

Symbol	Parameter	Min	Max	Unit
$V_{IH(AC)}$	Input high voltage	DDR_VREF + 0.175	None	V
$V_{IL(AC)}$	Input low voltage	None	DDR_VREF – 0.175	V

2.6.5 Power-On and Power-Off Sequence

To avoid overcurrent for I/O pins during power-on, you are advised to power on DVDD33 and DVDD12 in sequence. There is no requirement on the power-off sequence.

2.7 PCB Design Recommendations

For details about the printed circuit board (PCB) design, see the *Hi3518 Hardware Design User Guide*.

2.8 Interface Timings

2.8.1 DDR Interface Timings

2.8.1.1 Write Timings

Write Timings of dqs_out Relative to dq_out

In the write timing of dqs_out relative to dq_out, the major parameters are tDS and tDH. In DDR2-800, the value of tDS is 0.05 ns, and the value of tDH is 0.125 ns.

Figure 2-6 Write timing of dqs_out relative to dq_out for the DDR2

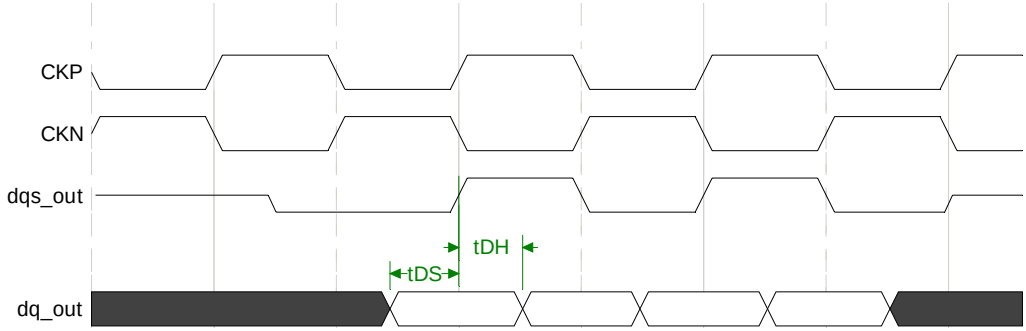
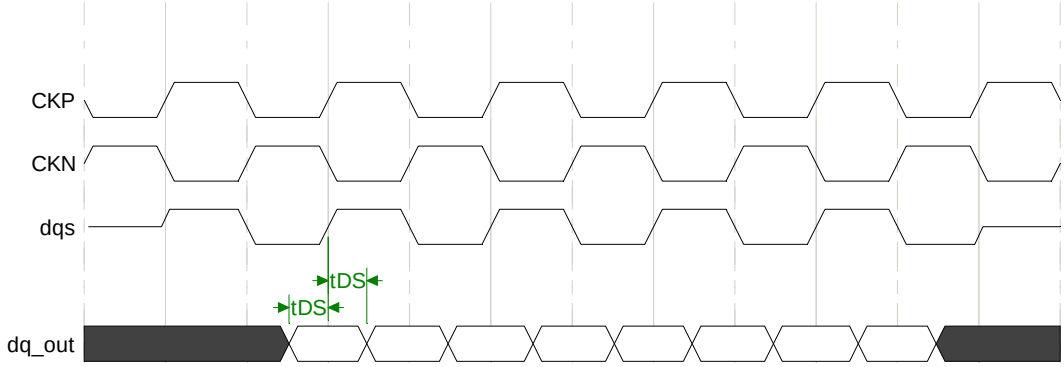


Figure 2-7 Write timing of dqs_out relative to dq_out for the DDR3



Write Timings of dqs_out Relative to CK

Figure 2-8 shows the write timing of dqs_out relative to CK for the DDR2, and Figure 2-9 shows the write timing of dqs_out relative to CK for the DDR3.

Figure 2-8 Write timing of dqs_out relative to CK for the DDR2

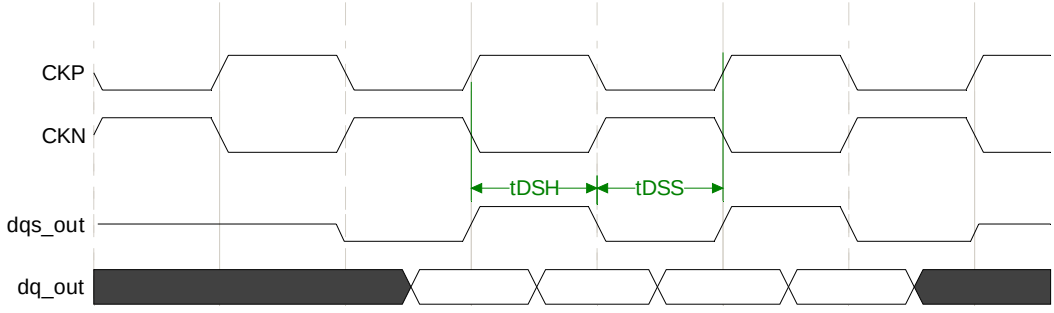
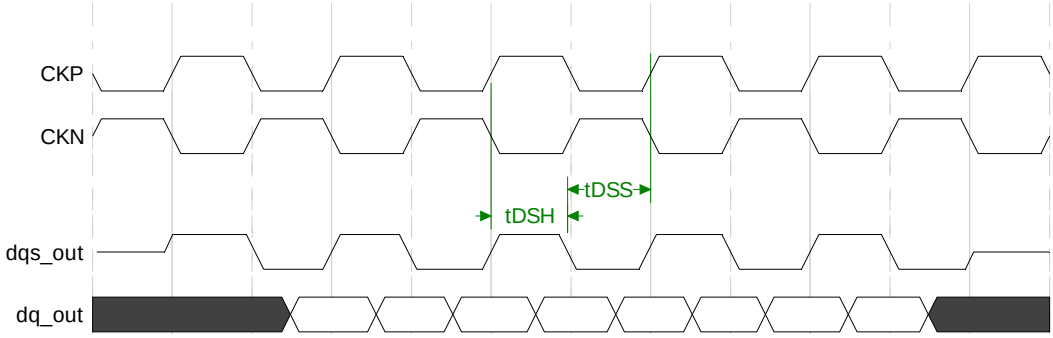


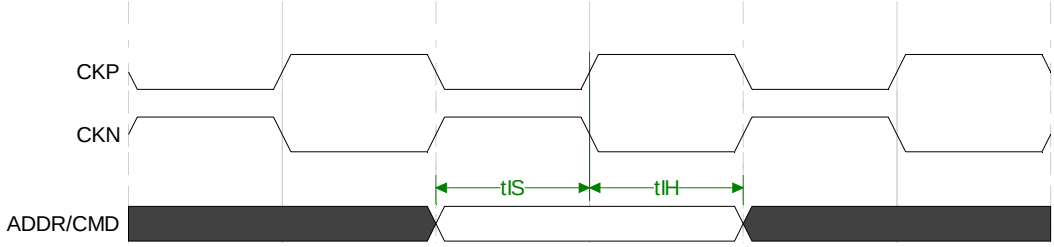
Figure 2-9 Write timing of dqs_out relative to CK for the DDR3



Write Timing of CMD/ADDR Relative to CK

Figure 2-10 shows the write timing of CMD/ADDR relative to CK.

Figure 2-10 Write timing of CMD/ADDR relative to CK



2.8.1.2 Read Timings

Read Timing of CMD/ADDR Relative to CK

The read timing of CMD/ADDR relative to CK is the same as the "Write Timing of CMD/ADDR Relative to CK".

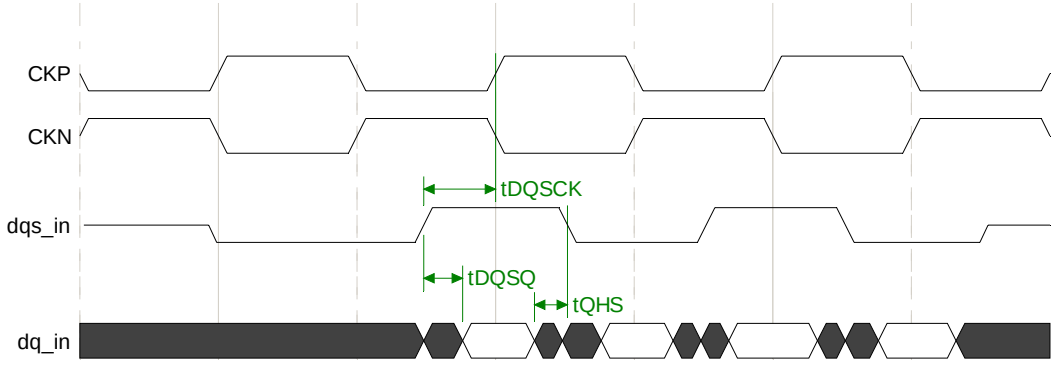
Read Timings of dqs_in Relative to dq_in

The read timings of dqs_in relative to dq_in are classified into the DDRn SDRAM output timing, dqs_in timing on the DDR PHY side, and dq_in timing on the DDR PHY side.

For the DDR SDRAM output timing, the phases of DQS and CK are the same in the ideal condition; however, there is a tDQSCK skew between DQS and CK. The value of tDQSCK is 0.35 ns. tDQSQ is the jitter of the last valid DQ relative to DQS and its value is 0.2 ns; tQHS is the jitter of the first valid DQ relative to DQS and its value is 0.3 ns.

Figure 2-11 shows the output timing of the DDRn SDRAM.

Figure 2-11 Output timing of the DDRn SDRAM



2.8.1.3 Timing Parameters

The timings of the DDR interface comply with the JEDEC standards including JESD79-2E and JESD79-3B standards. All the timings in this document are output on the DDR PHY side.

The Hi3518 is based on the timing parameters of the DDR2-800 and DDR3-1066 SDRAMs.

Table 2-59 and Table 2-60 describe the clock parameters of the DDR2-800 SDRAM.

Table 2-61 and Table 2-62 describe the clock parameters of the DDR3-1066 SDRAM.

Table 2-59 DDR2 clock parameters

Parameter	Typ	Unit
DDR clock frequency	400.00	MHz
PLL jitter	0.200	ns
PLL duty ratio	48.000	%
Clock skew	0.100	ns

Table 2-60 describes the parameters of the DDR2 SDRAM.

Table 2-60 Parameters for the DDR2-800 SDRAM

Parameter	Symbol	Typ	Unit
Setup time, DQS falling edge to DDR clock	tDSS	0.2	tCK
Hold time, DQS falling edge to DDR clock	tDSH	0.2	tCK
Setup time, DQ/DM to DQS	tDS	0.050	ns
Hold time, DQ/DM to DQS	tDH	0.125	ns
Skew between DQS and DQ	tDQSQ	0.200	ns
Data hold skew	tQHS	0.300	ns
Setup time, ADDR/CMD to DDR clock	tIS	0.175	ns

Parameter	Symbol	Typ	Unit
Hold time, ADDR/CMD to DDR clock	tIH	0.250	ns
Skew of DQS (output) to DDR clock	tDQSCK	0.350	ns

NOTE

For details about some timing parameters, see the following timing diagrams.

Table 2-61 DDR3 clock parameters

Parameter	Typ	Unit
DDR clock frequency	600.00	MHz
PLL jitter	0.200	ns
PLL duty ratio	47.000	%
Clock skew	0.100	ns

Table 2-62 Parameters for the DDR3-1066 SDRAM

Parameter	Symbol	Typ	Unit
Setup time, DQS falling edge to DDR clock	tDSS	0.2	tCK
Hold time, DQS falling edge to DDR clock	tDSH	0.2	tCK
Setup time, DQ/DM to DQS	tDS	0.025	ns
Hold time, DQ/DM to DQS	tDH	0.100	ns
Skew between DQS and DQ	tDQSQ	0.150	ns
Setup time, ADDR/CMD to DDR clock	tIS	0.125	ns
Hold time, ADDR/CMD to DDR clock	tIH	0.200	ns
Skew of DQS (output) to DDR clock	tDQSCK	0.300	ns

2.8.2 SFC Interface Timings

Figure 2-12 shows the SFC input timing.

Figure 2-12 SFC input timing

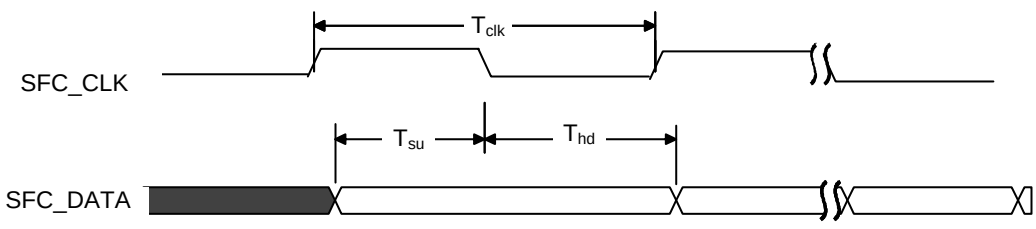


Table 2-63 describes the SFC input timing parameters.

Table 2-63 SFC input timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
Clock cycle of SFC_CLK	T_{clk}	16	None	83.2	ns
Input signal setup time	T_{su}	8	None	None	ns
Input signal hold time	T_{hd}	1.2	None	None	ns

Figure 2-13 shows the SFC output timing.

Figure 2-13 SFC output timing

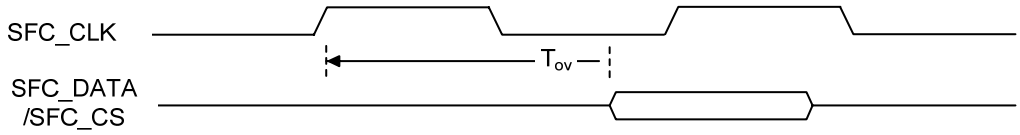


Table 2-64 describes the SFC output timing parameters.

Table 2-64 SFC output timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
Clock cycle of SFCCLK	T	16	None	83.2	ns
Output data signal delay	T_{ov}	–5	None	3.0	ns
Output CS signal delay	T_{ov}	–5	None	3.0	ns

2.8.3 Ethernet MAC Port Timings

MII Timings

The Hi3518 provides standard MIIs that comply with the MII timing standard. These interfaces are used to connect to the physical layer (PHY).

Figure 2-14 shows the 100 Mbit/s RX timing of the MII.

Figure 2-14 100 Mbit/s RX timing of the MII

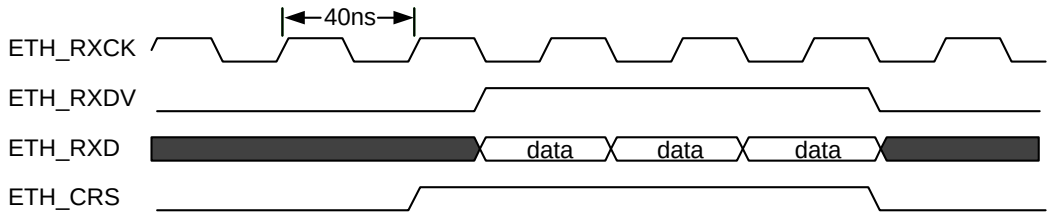


Figure 2-15 shows the 100 Mbit/s TX timing of the MII.

Figure 2-15 100 Mbit/s TX timing of the MII

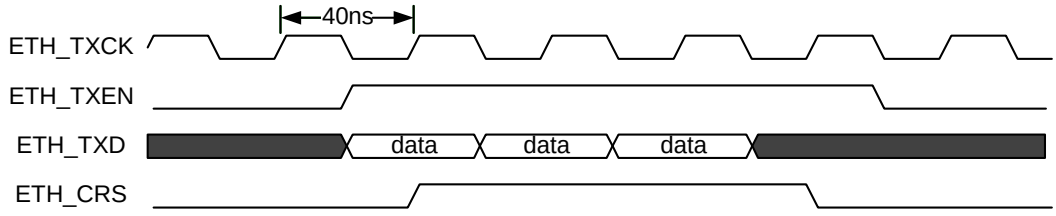


Figure 2-16 shows the 10 Mbit/s RX timing of the MII.

Figure 2-16 10 Mbit/s RX timing of the MII

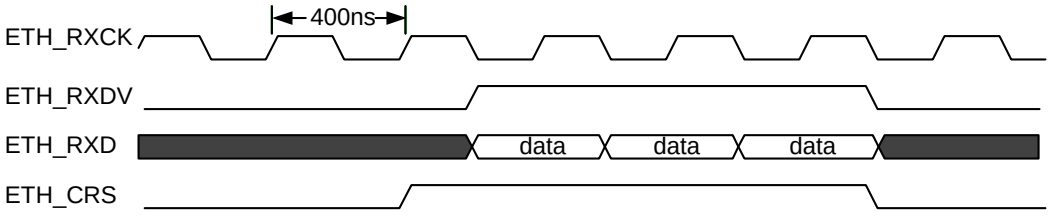


Figure 2-17 shows the 10 Mbit/s TX timing of the MII.

Figure 2-17 10 Mbit/s TX timing of the MII

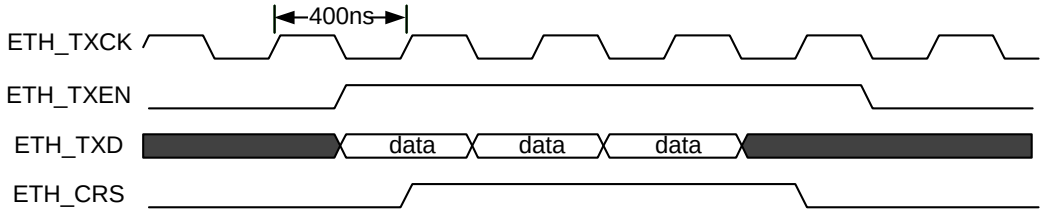


Figure 2-18 shows the RX timing parameters of the MII.

Figure 2-18 RX timing parameters of the MII

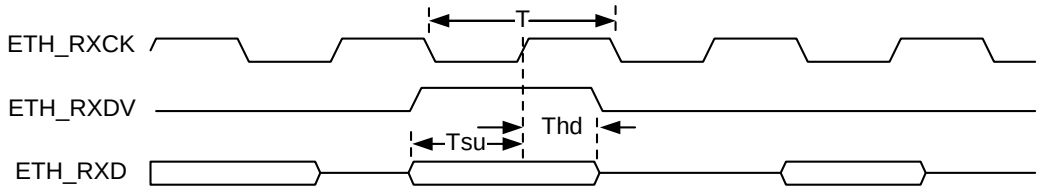


Figure 2-19 shows the TX timing parameters of the MII.

Figure 2-19 TX timing parameters of the MII

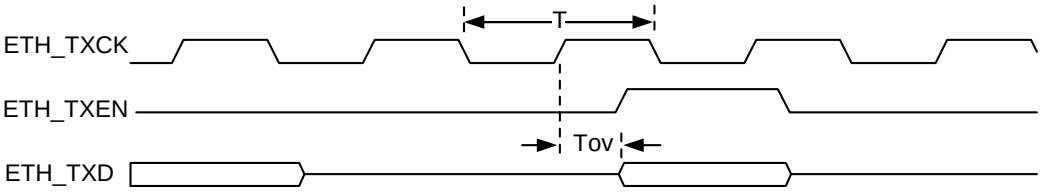


Table 2-65 describes the MII timing parameters.

Table 2-65 MII timing parameters

Parameter	Symbol	Signal	Min	Max	Unit
MII clock cycle	T	RXCK、TXCK	400(10Mbit/s)	400	ns
MII signal setup time			40(10Mbit/s)	40	
MII signal hold time	Tsu（RX）	RXER、RXDV、RXD[3:0]	6	None	ns
MII output signal delay	Thd（RX）	RXER、RXDV、RXD[3:0]	2	None	ns
MII clock cycle	Tov（MIITX）	TXD[3:0]、TXEN	2	8	ns

RMII Timings

Figure 2-20 shows the 100 Mbit/s RX timing of the RMII.

Figure 2-20 100 Mbit/s RX timing of the RMII

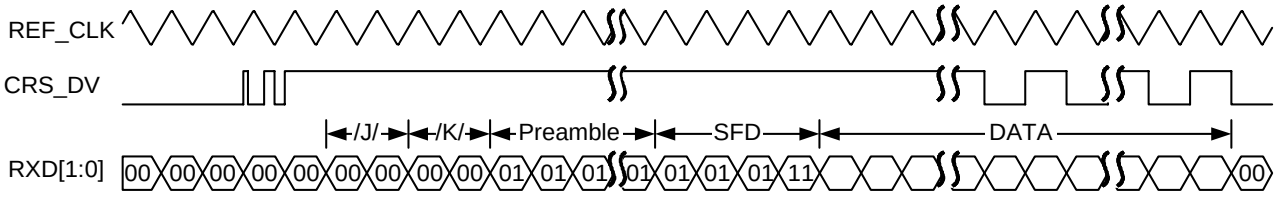


Figure 2-21 shows the 100 Mbit/s TX timing of the RMII interface.

Figure 2-21 100 Mbit/s TX timing of the RMII

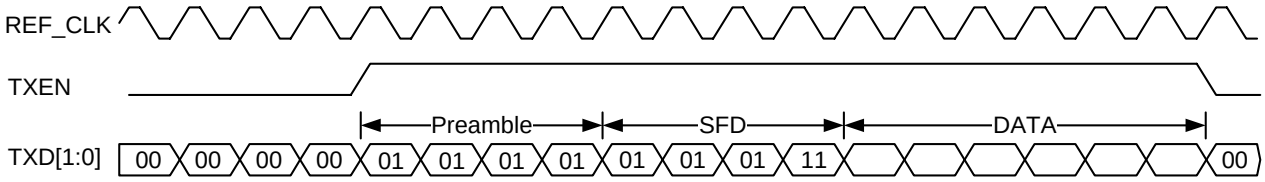


Figure 2-22 shows the 10 Mbit/s RX timing of the RMII.

Figure 2-22 10 Mbit/s RX timing of the RMII

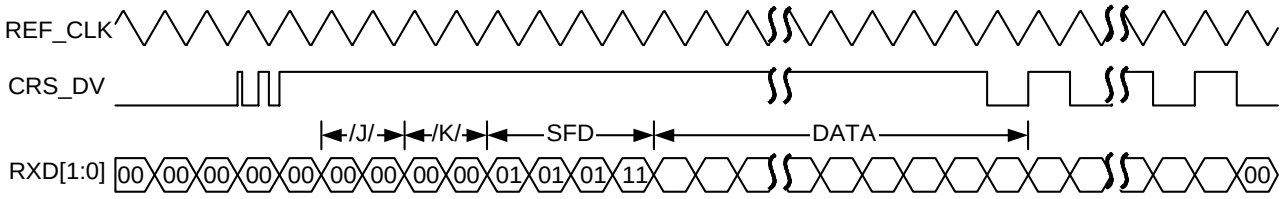


Figure 2-23 shows the 10 Mbit/s TX timing of the RMII.

Figure 2-23 10 Mbit/s TX timing of the RMII

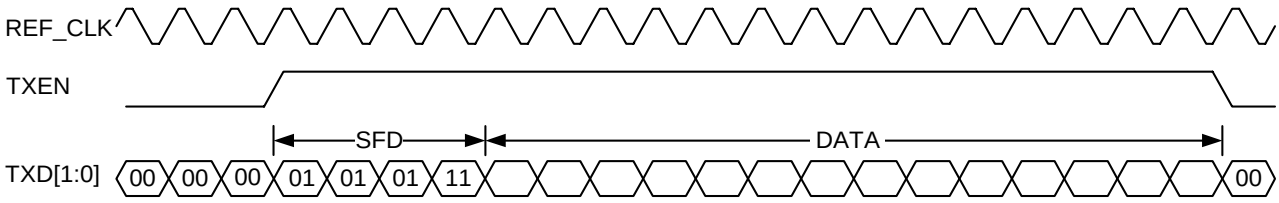


Figure 2-24 shows the timing parameters of the RMII.

Figure 2-24 Timing parameters of the RMII

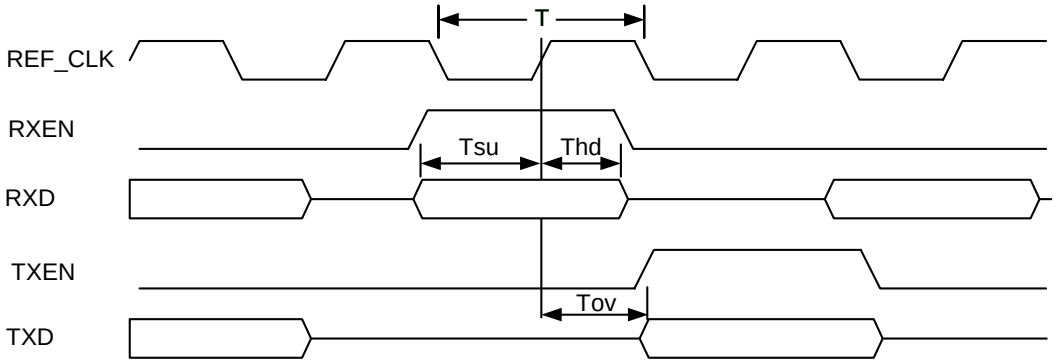


Table 2-66 describes the timing parameters of the RMII.

Table 2-66 Timing parameters of the RMII

Parameter	Symbol	Signal	Min	Max	Unit
Setup time of RMII signal	Tsu (RX)	CRS_DV/RXD[1:0]	4	None	ns
Hold time of RMII signal	Thd (RX)	CRS_DV/RXD[1:0]	2	None	ns
RMII output signal delay	Tov （RMIITX）	TXEN/TXD[1:0]	2	16	ns

MDIO Interface Timings

Figure 2-25 shows the read timing of the MDIO interface.

Figure 2-25 Read timing of the MDIO interface

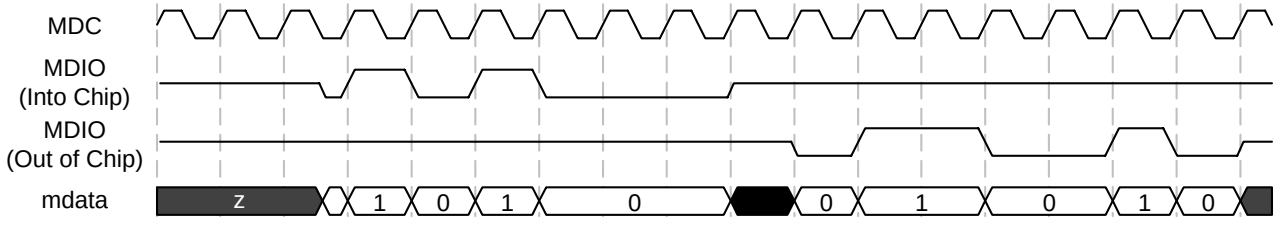


Figure 2-26 shows the write timing of the MDIO interface.

Figure 2-26 Write timing of the MDIO interface

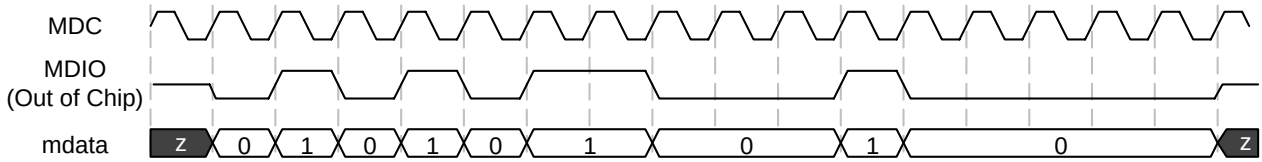


Figure 2-27 shows the RX timing parameters of the MDIO interface.

Figure 2-27 RX timing parameters of the MDIO interface

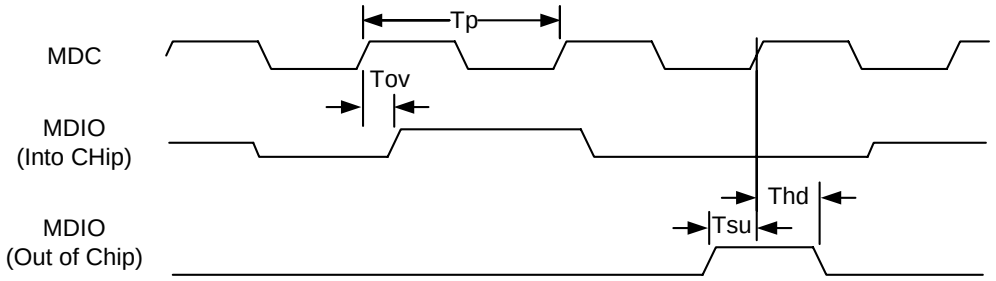


Table 2-67 describes the timing parameters of the MDIO interface.

Table 2-67 Timing parameters of the MDIO interface

Parameter	Symbol	Signal	Min	Max	Unit
MDIO data RX delay	Tov	MDIO	166	20833	ns
MDIO clock cycle	Tp	MDCK	333	41667	ns
MDIO data TX setup time	Tsu	MDIO	10	None	ns
MDIO data TX hold time	Thd	MDIO	10	None	ns

NOTE

The MDC clock cycle Tp can be changed by adjusting the MDC frequency (MDIO_RWCTRL[frq_dv]). To be specific, you can divide the frequency 150 MHz of the ETH working clock by 100, 50, or other values. Tov is related to the clock cycle Tp of the MDC, and its value is about Tmdc/2.

2.8.4 VI Interface Timing

The VI clock is supplied externally. All the VI interfaces are input interfaces in slave mode.

Figure 2-28 shows the VI interface timing.

Figure 2-28 VI interface timing

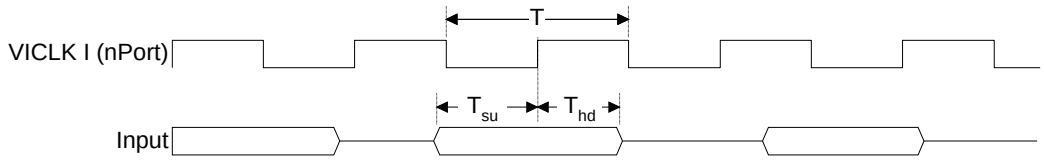


Table 2-68 describes the VI interface timing parameters.

Table 2-68 VI interface timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
VICLK clock cycle	T	13.48	-	-	ns
Input signal setup time	T_{su}	2.5	-	-	ns
Input signal hold time	T_{hd}	2.0	-	-	ns

2.8.5 VO Interface Timing

Figure 2-29 shows the VO interface timing.

Figure 2-29 VO interface timing

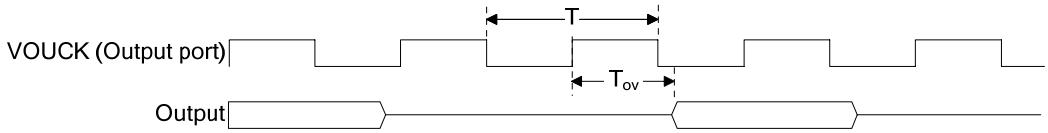


Table 2-69 describes the VO interface timing parameters.

Table 2-69 VO interface timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
VOCLK clock cycle	T	None	None	13.48	ns
Output signal delay	T_{ov}	3.5	None	8.8	ns

2.8.6 SIO Interface Timings

Figure 2-30 shows the I^2S interface RX timing.

Figure 2-30 I2S interface RX timing

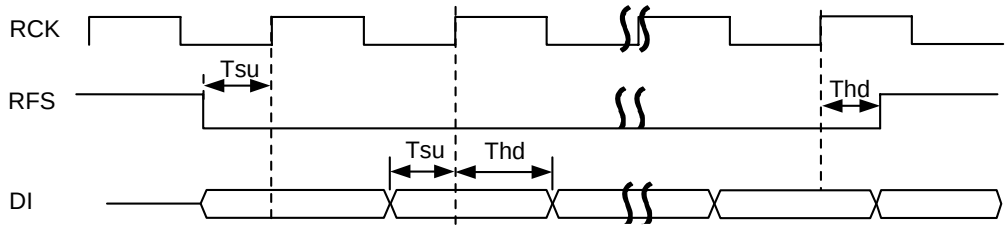


Figure 2-31 shows the I²S interface TX timing.

Figure 2-31 I2S interface TX timing

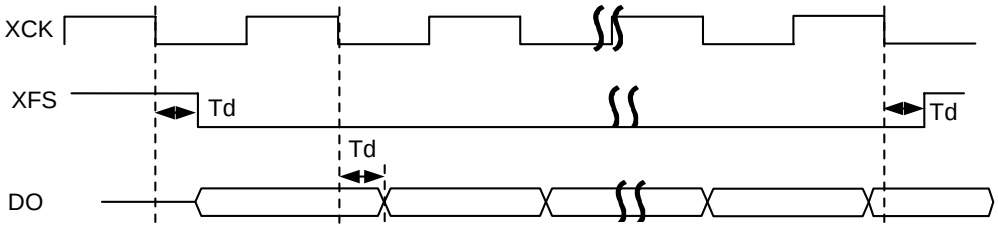


Table 2-70 describes the I²S interface timing parameters.

Table 2-70 I²S interface timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
Input signal setup time	T_{su}	10	None	None	ns
Input signal hold time	T_{hd}	10	None	None	ns
Output signal delay	T_d	0	None	8	ns

2.8.7 I2C Interface Timing

Figure 2-32 shows the I²C transfer timing.

Figure 2-32 I2C transfer timing

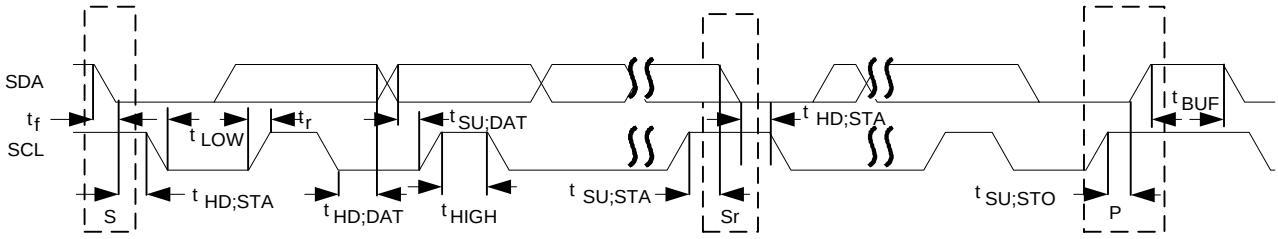


Table 2-71 describes the I²C interface timing parameters.

Table 2-71 I²C interface timing parameters

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
Serial clock (SCL) frequency	f_{SCL}	0	100	0	400	kHz
Start hold time	$t_{HD;STA}$	4.0	None	0.6	None	μs
SCL low-level cycle	t_{LOW}	4.7	None	1.3	None	μs
SCL high-level cycle	t_{HIGH}	4.0	None	0.6	None	μs
Start setup time	$t_{SU;STA}$	4.7	None	0.6	None	μs
Data hold time	$t_{HD;DAT}$	0	3.45	0	0.9	μs
Data setup time	$t_{SU;DAT}$	250	None	100	None	ns
Serial data (SDA) and SCL rising time	t_r	None	1000	$20 + 0.1C_b$	300	ns
SDA and SCL falling time	t_f	None	300	$20 + 0.1C_b$	300	ns
End setup time	$t_{SU;STO}$	4.0	None	0.6	None	μs
Bus release time from start to end	t_{BUF}	4.7	None	1.3	None	μs
Bus load	C_b	None	400	None	400	pF
Low-level noise tolerance	V_{nL}	$0.1V_{DD}$	None	$0.1V_{DD}$	None	V
High-level noise tolerance	V_{nH}	$0.2V_{DD}$	None	$0.2V_{DD}$	None	V

Figure 2-33 SPI timing in master mode (sph = 1)

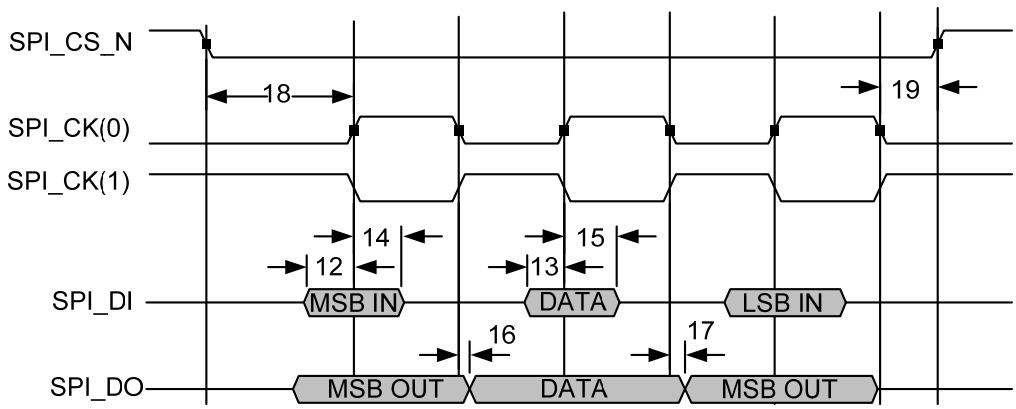


Table 2-72 describes the SPI timing parameters.

Table 2-72 SPI timing parameters

No.	Parameter	Symbol	Min	Typ	Max	Unit
1	Cycle time, SPI_CK	tc	None	None	None	ns
2	Pulse duration, SPI_CK high (all master modes)	tw1	None	None	None	ns
3	Pulse duration. SPI_CK low (all master modes)	tw2	None	None	None	ns
4	Setup time, SPI_DI (input) valid before SPI_CK (output) falling edge	tsu1	None	None	None	ns
5	Setup time, SPI_DI (in put) valid before SPICK (output) rising edge	tsu2	None	None	None	ns
6	Hold time, SPI_DI (input) valid after SPI_CK (output) falling edge	th1	None	None	None	ns
7	Hold time, SPI_DI (input) valid after SPI_CK (output) rising edge	th2	None	None	None	ns
8	Delay time, SPI_CK (output) rising edge to SPI_DO (output) transition	td1	None	None	None	ns
9	Delay time, SPI_CK (output) falling edge to SPI_DO (output) transition	td2	None	None	None	ns
10	Delay time, SPI_CS_N (output) falling edge to first SPI_CK (output) rising or falling edge	td3	None	None	None	ns
11	Delay time, SPI_CK (output) rising or falling edge to SPI_CS_N (output) rising edge	td4	None	None	None	ns
12	Setup time, SPI_DI (input) valid before SPI_CK (output) rising edge	tsu3	None	None	None	ns
13	Setup time, SPI_DI (in put) valid before SPI_CK (output) falling edge	tsu4	None	None	None	ns
14	Hold time, SPI_DI (input) valid after SPI_CK (output) rising edge	th3	None	None	None	ns
15	Hold time, SPI_DI (input) valid after SPI_CK (output) falling edge	th4	None	None	None	ns
16	Delay time, SPI_CK (output) falling edge to SPI_DO (output) transition	td5	None	None	None	ns

No.	Parameter	Symbol	Min	Typ	Max	Unit
17	Delay time, SPI_CK (output) rising edge to SPI_DO (output) transition	td6	None	None	None	ns
18	Delay time, SPI_CS_N (output) falling edge to first SPI_CK (output) rising or falling edge	td7	None	None	None	ns
19	Delay time, SPI_CK (output) rising or falling edge to SPI_CS_N (output) rising edge	td8	None	None	None	ns

Contents

Figures

Tables

3 System

3.1 Reset

3.1.1 Overview

The reset management module resets the entire chip and all functional modules in a unified manner as follows:

- Manages and controls power-on reset.
- Controls the system soft reset and the separate soft reset of each functional module.
- Synchronizes reset signals to the clock domain corresponding to each module.

The reset management module also generates reset signals for each internal functional module.

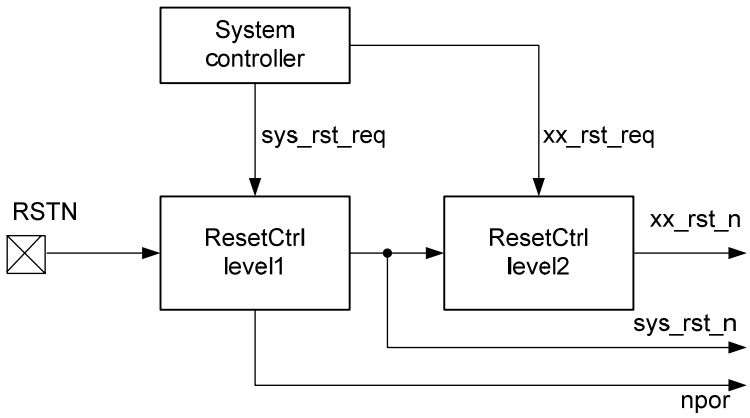
NOTE

The Hi3518A supports power-on reset by using the external chip pins or the internal power-on reset (POR) module, which is specified by the POR_SEL pin. The Hi3518C supports power-on rest only by using the internal POR module.

3.1.2 Reset Control

Figure 3-1 shows the diagram of controlling reset signals.

Figure 3-1 Diagram of controlling reset signals



NOTE

- RSTN: power-on reset signal. This signal is derived from the input pin RSTN of the chip or the internal POR module.
- sys_rst_req: global soft reset request signal. This signal is derived from the system controller.
- xx_rst_req: separate soft reset request signal of each submodule. This signal is derived from the clock and reset generator (CRG) system controller.
- xx_rst_n, sys_rst_n, and npor: reset signals.

Table 3-1 Types of reset signals

Type	Generation Mode	Function
Global hard reset signal (npor)	Derived from the RSTN reset pin or the internal POR module.	Globally resets the entire Hi3518.
Global soft reset signal (syn_rst_n)	Derived from the global soft reset register of the software configuration system controller.	Globally resets all the modules of the Hi3518 excluding the clock reset circuit and the test circuit.
Submodule reset signal (xx_rst_n)	Derived from the submodule reset control register of the CRG system controller.	Separately resets each submodule of the Hi3518.

3.1.3 Reset Configuration

Power-On Reset

The RSTN is the functional reset input/output (IO) pin of the Hi3518. To implement power-on reset, the following conditions must be met:

- The power-on reset IO pin inputs a low-level pulse.
- The clock input by the XIN pin of the crystal oscillator clock works properly.
- The low pulse width of the power-on reset signal is longer than 12 XIN clock cycles.

System Reset

The system is reset in either of the following ways:

- Power-on reset
- Global soft reset, controlled by the system controller

Soft Reset

The soft reset is controlled by configuring the corresponding system controller. For details about configurations, see the description of the reset register for each module.

CAUTION

- After a system soft reset request is sent, the circuit reset is deasserted after at least 360 system clock cycles.
- The separate soft reset of each module is not automatically deasserted. For example, if a module is reset after 1 is written to the related bit, the reset of this module is deasserted only when the related bit is set to 0.

3.2 Clock

3.2.1 Overview

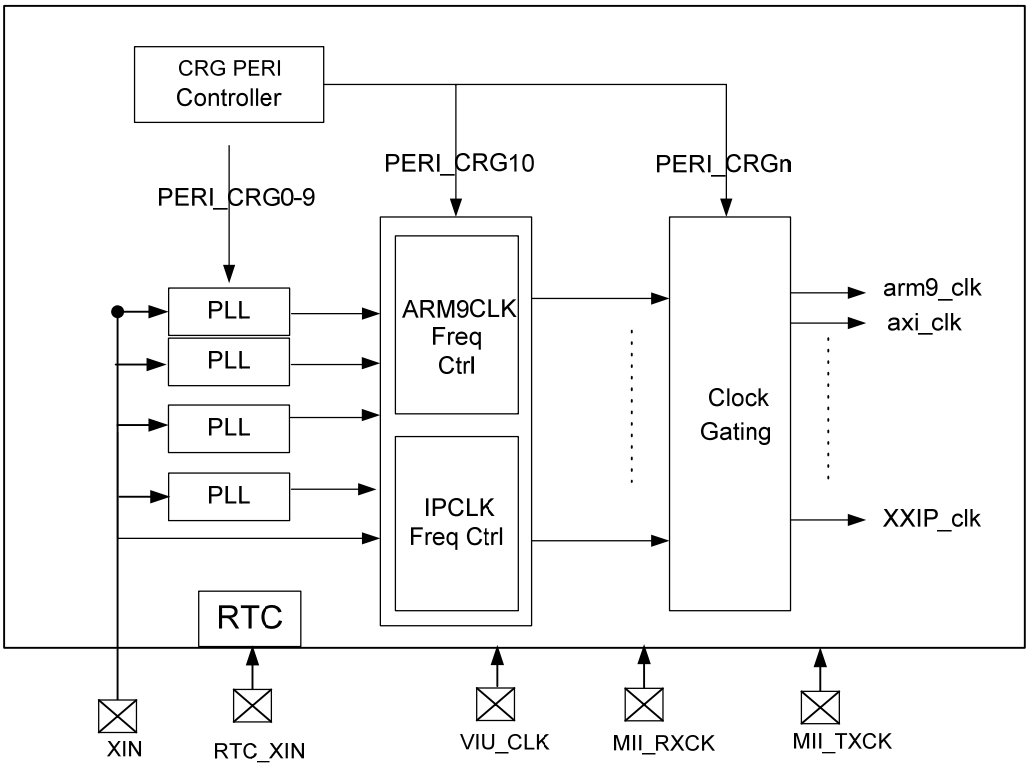
The clock management module manages clock input, clock generation, and clock control in a unified manner as follows:

- Manages and controls clock inputs
- Divides and controls clock frequencies
- Generates working clocks for each module

3.2.2 Clock Control Block Diagram

Figure 3-2 shows the functional block diagram of the clock management module.

Figure 3-2 Functional block diagram of the clock management module



The inputs of the clock management module are as follows:

- Clock inputs from the XIN, RTC_XIN, VIU_CLK, MII_RXCK, and MII_TXCK pins.
  - XIN is the phase-locked loop (PLL) input clock that connects only to the 24 MHz crystal.
  - RTC_XIN is the input clock of the internal real-time clock (RTC) module, and it always connects to a 32 kHz crystal.
  - VIU_CLK is a video input (VI) clock.
  - MII_RXCK and MII_TXCK are the interface clocks of the ETH module.
- Clock control registers derived from the CRG system controller.
  - PLL frequency configuration
  - IP clock frequency configuration
  - Clock gating configuration

The clock management module consists of the following parts:

- PLL unit. This unit is used to generate ARM9 clock, bus clock, and the clocks required by peripherals.
- Control units including the ARM9 frequency control unit (ARM9 Freq Ctrl) and module clock frequency control unit (IPCLK Freq Ctrl)
- Clock gating management unit

3.2.3 Clock Configuration

PLL Configuration

The Hi3518 has four internal PLLs. Each PLL uses two configuration registers. See Table 3-2.

Table 3-2 Configuration registers corresponding to Hi3518 PLLs

PLL	Configuration Register 1	Configuration Register 0
APLL	PERI_CRG0	PERI_CRG1
VPLL0	PERI_CRG2	PERI_CRG3
BPLL	PERI_CRG4	PERI_CRG5
EPLL	PERI_CRG8	PERI_CRG9

Table 3-3 shows the mapping between PLLs and functional modules.

Table 3-3 Mapping between PLLs and functional modules

PLL	Output Pin of Each PLL	Function
APLL	FOUTPOSTDIV	Generates the ARM9 working clock. The default clock is a 440 MHz clock
APLL	FOUTPOSTDIV	• Generates the DDR working clock. The default clock is a 440 MHz clock • Generates the advanced eXtensible interface (AXI) bus clock by dividing the DDR clock by 2. • Generates the advanced peripheral bus (APB) clock by dividing the DDR clock by 4.
VPLL0	FOUTVCO	The default clock is a 1188 MHz clock. • The 1188 MHz clock is divided by 6 to generate a 198 MHz clock to act as the source clock of the VPSS and TDE module. • The 1188 MHz clock is divided by 12 to generate a 99 MHz clock to act as the source clock of the MDU, NFC, and CIPHER module.
	FOUT2	The default clock is a 74.25 MHz clock. It acts as the working clock of the video display high definition (VDP HD) module.
EPLL	FOUTVCO	The default clock is a 1350 MHz clock. • The 1350 MHz clock is divided by 2 to generate a 675 MHz clock to act as the source clock of the SIO MCLK. • The 1350 MHz clock is divided by 6 to generate a 225 MHz clock to act as the working clock of the VEDU, JPGE, and VAPU module. • The 1350 MHz clock is divided by 12 to generate a 112.5 MHz clock to act as the source clock of the SFC module. • The 1350 MHz clock is divided to generate a 54 MHz clock to act as the source clock of the video display standard definition (VDP SD). • The 1350 MHz clock is divided to generate a 27 MHz clock to act as the source clock of the sensor output clock.
	FOUTPOSTDIV	The default clock is a 150 MHz clock. It is divided by 3 to generate a 50 MHz clock to act as the working clock or source clock of the SDIO and ETH RMII.

All PLLs use the input crystal oscillator clock of the XIN pin as the input clock. For details on how to calculate PLL output frequencies, see Table 3-4.

Table 3-4 Methods of calculating PLL output frequencies

PLL Pin	Formula	Remarks
FREF	PLL input reference clock	The input clock must be 24 MHz.
FOUTVCO	FREF x (fbdiv + frac/2^24)/refdiv	PLL working frequency. It must be greater than 600 MHz but less than or equal to 1.6 GHz.
FOUTPOSTDIV	FOUTVCO/(pstdiv1 x pstdiv2)	None
FOUT1ph0	FOUTVCO/(pstdiv1 x pstdiv2 x 2)	None
FOUT2	FOUTVCO/(pstdiv1 x pstdiv2 x 4)	None
FOUT3	FOUTVCO/(pstdiv1 x pstdiv2 x 6)	None
FOUT4	FOUTVCO/(pstdiv1 x pstdiv2 x 8)	None

The following is an example using VPLL0. VPLL0 outputs the FOUT2 to the VDP, the VDP works in HD mode, and the working clock required by the VDP is 74.25 MHz.

If postdiv2 is 2 and postdiv1 is 2, the value of FOUTVCO is 1188 MHz.

If refdiv is 2, the value of FOUTVCO is calculated as follows: 24 x (fbdiv + frac/2^24)/2 = 1188 MHz.

Based on the preceding results, fbdiv is 99 and frac is 000000.

Frequency Configurations of ARM9/DDR clocks

Table 3-5 describes the frequency configurations of ARM9/DDR clocks.

Table 3-5 Frequency configurations of ARM9 clocks

Signal	Description
cpuclk_loaden	CPU clock DFS frequency division configuration enable. To change the frequency division configuration, perform the following steps: 1 Write a new frequency division configuration value. 2 Write 0 to veduclk_loaden. 3 Write 1 to veduclk_loaden. This signal can be controlled by configuring PERI_CRG10 bit[10].

Signal	Description
cpuclk_skipcfg	CPU clock DFS frequency division configuration. N: N-beat clocks are disabled every 32-beat CPU clocks.This signal can be controlled by configuring PERI_CRG16 bit[9:5]. The source working clock of CPU is 440 MHz. If cpuclk_skipcfg is set to 00, CPU works in full-speed mode; if cpuclk_skipcfg is set to 01, CPU works in speed-down mode. The actual frequency is calculated as follows: 440 x 31/32 = 426.25 MHz This rule applies to the configurations.

Table 3-6 shows the mapping between the states of the system controller and clocks.

Table 3-6 Mapping between the states of the system controller and clocks

System Controller State	Enable State of the 46.875 kHz Clock	Enable State of the 24 MHz Crystal Oscillator	Enable State of the APLL	System Clock State
Normal	Enabled	Enabled	Enabled	The working clocks of the ARM subsystem are derived from the PLL.
Slow	Enabled	Enabled	Disabled	The working clocks of the ARM subsystem are derived from the 24 MHz crystal oscillator.
Doze	Enabled	Enabled	Disabled	The working clocks of the ARM subsystem are derived from the 46.875 kHz clock. The 46.875 kHz clock is generated by dividing the 24 MHz crystal oscillator.

Frequency Configurations of Module Clocks

Table 3-7 describes the frequency configurations of video capture (VICAP) clocks.

Table 3-7 Frequency configurations of VICAP clocks

Signal	Description
vi_selftest	Clock source select for VI self tests. This signal can be controlled by configuring PERI_CRG11 bit[7].

Signal	Description
vi_pctrl	VI input associated clock phase control. The value range of n is 0–3. The normal phase clock is selected by default. 0: normal phase clock 1: reverse phase clock This signal can be controlled by configuring PERI_CRG11 bit[6].

Table 3-8 describes the frequency configurations of VDP clocks and sensor output clock.

Table 3-8 Frequency configurations of VDP clocks and sensor output clock

Signal	Description
hd_sd_sel	VO mode select. 0: SD 1: HD This signal can be controlled by configuring PERI_CRG13 bit[12].
vohd_out_pctrl	VOU HD output associated clock phase control. 0: normal phase clock 1: reverse phase clock This signal can be controlled by configuring PERI_CRG13 bit[4].
sense_cksel	Sensor output clock. 000: 12 MHz 001: 24 MHz 010: 27 MHz 011: 54 MHz 100: 13.5 MHz 101: 27 MHz 110: 37.125 MHz 111: 74.25 MHz This signal can be controlled by configuring PERI_CRG12 bit[2:0].

Table 3-9 describes the frequency configurations of VEDU clocks.

Table 3-9 Frequency configurations of VEDU clocks

Signal	Description
veduclk_loaden	VEDU clock frequency division configuration enable. To change the frequency division configuration, perform the following steps: 1 Write a new frequency division configuration value. 2 Write 0 to veduclk_loaden. 3 Write 1 to veduclk_loaden. This signal can be controlled by configuring PERI_CRG16 bit[9].
veduclk_skipcfg	VEDU clock frequency division configuration. N: N-beat clocks are disabled every 32-beat VEDU clocks.This signal can be controlled by configuring PERI_CRG16 bit[8:4]. The source working clock of VEDU is 225 MHz. If veduclk_skipcfg is set to 00, VEDU works in full-speed mode; if veduclk_skipcfg is set to 01, VEDU works in speed-down mode. The actual frequency is calculated as follows: 225 x 31/32 = 218 MHz This rule applies to the configurations.

Table 3-10 describes the frequency configurations of VPSS clocks.

Table 3-10 Frequency configurations of VPSS clocks

Signal	Description
vpssclk_loaden	VPSS clock frequency division configuration enable. To change the frequency division configuration, perform the following steps: 1 Write a new frequency division configuration value. 2 Write 0 to vpssclk_loaden. 3 Write 1 to vpssclk_loaden. This signal can be controlled by configuring PERI_CRG18 bit[9].
vpssclk_skipcfg	VPSS clock frequency division configuration. N: N-beat clocks are disabled every 32-beat VPSS clocks. This signal can be controlled by configuring PERI_CRG18 bit[8:4]. The source working clock of VPSS is 198 MHz. If vpssclk_skipcfg is set to 00, VPSS works in full-speed mode; if vpssclk_skipcfg is set to 01, VPSS works in speed-down mode. The actual frequency is calculated as follows: 198 x 31/32 = 192 MHz This rule applies to the configurations.

Table 3-11 describes the frequency configurations of TDE clocks.

Table 3-11 Frequency configurations of TDE clocks

Signal	Description
tdeclk_loaden	TDE clock frequency division configuration enable. To change the frequency division configuration, perform the following steps: 1 Write a new frequency division configuration value. 2 Write 0 to tdeclk_loaden. 3 Write 1 to tdeclk_loaden. This signal can be controlled by configuring PERI_CRG22 bit[9].
tdeclk_skipcfg	TDE clock frequency division configuration. N: N-beat clocks are disabled every 32-beat TDE clocks. This signal can be controlled by configuring PERI_CRG22 bit[8:4]. The source working clock of the TDE is 198 MHz. If tdeclk_skipcfg is set to 00, the TDE works in full-speed mode; if tdeclk_skipcfg is set to 01, the TDE works in speed-down mode. The actual frequency is calculated as follows: 198 x 31/32 = 192 MHz This rule applies to the configurations.

Table 3-12 describes the frequency configurations of JPGE clocks.

Table 3-12 Frequency configurations of JPGE clocks

Signal	Description
jpgeclk_loaden	JPGE clock frequency division configuration enable. To change the frequency division configuration, perform the following steps: 1 Write a new frequency division configuration value. 2 Write 0 to jpgeclk_loaden. 3 Write 1 to jpgeclk_loaden. This signal can be controlled by configuring PERI_CRG24 bit[9].
jpgeclk_skipcfg	JPGE clock frequency division configuration. N: N-beat clocks are disabled every 32-beat JPGE clocks. This signal can be controlled by configuring PERI_CRG24 bit[8:4]. The source working clock of the JPGE is 225 MHz. If jpgeclk_skipcfg is set to 00, the JPGE works in full-speed mode; if jpgeclk_skipcfg is set to 01, the JPGE works in speed-down mode. The actual frequency is calculated as follows: 225 x 31/32 = 218 MHz This rule applies to the configurations.

Table 3-13 describes the frequency configuration of the MDU clocks.

Table 3-13 Frequency configurations of MDU clocks

Signal	Description
mduclk_loaden	MDU clock frequency division configuration enable. To change the frequency division configuration, perform the following steps: 1 Write a new frequency division configuration value. 2 Write 0 to mduclk_loaden. 3 Write 1 to mduclk_loaden. This signal can be controlled by configuring PERI_CRG26 bit[9].
mduclk_skipcfg	MDU clock frequency division configuration. N: N-beat clocks are disabled every 32-beat MDU clocks. This signal can be controlled by configuring PERI_CRG26 bit[8:4]. The source working clock of the MDU is 99 MHz. If mduclk_skipcfg is set to 00, the MDU works in full-speed mode; if mduclk_skipcfg is set to 01, the MDU works in speed-down mode. The actual frequency is calculated as follows: 99 x 31/32 = 96 MHz This rule applies to the configurations.

Table 3-14 describes the frequency configurations of VAPU clocks.

Table 3-14 Frequency configurations of VAPU clocks

Signal	Description
vapuclk_loaden	VAPU clock frequency division configuration enable. To change the frequency division configuration, perform the following steps: 1 Write a new frequency division configuration value. 2 Write 0 to vapuclk_loaden. 3 Write 1 to vapuclk_loaden. This signal can be controlled by configuring PERI_CRG27 bit[9].
vapuclk_skipcfg	VAPU clock frequency division configuration. N: N-beat clocks are disabled every 32-beat VAPU clocks. This signal can be controlled by configuring PERI_CRG27 bit[8:4]. The source working clock of the VAPU is 225 MHz. If vapuclk_skipcfg is set to 00, the VAPU works in full-speed mode; if vapuclk_skipcfg is set to 01, the VAPU works in speed-down mode. The actual frequency is calculated as follows: 225 x 31/32 = 218 MHz This rule applies to the configurations.

Table 3-15 describes the frequency configuration of the ETH clock.

Table 3-15 Frequency configuration of the ETH clock

Signal	Description
ethcore_cksel	ETH clock source select. 00: 54 MHz 01: 27 MHz Other values: 99 MHz This signal can be controlled by configuring PERI_CRG51 bit[7:6].
ethphy_cksel	ETHPHY output clock source select. 00: 25 MHz 01: 24 MHz Other values: 27 MHz This signal can be controlled by configuring PERI_CRG51 bit[5:4].
mii_rmii_mode	ETH mode. 0: MII mode 1: RMII mode This signal can be controlled by configuring PERI_CRG51 bit[3].

Table 3-16 describes the frequency configurations of SDIO clocks.

Table 3-16 Frequency configurations of SDIO clocks

Signal	Description
sdioclk_pctrl	Polarity of the SDIO SAP clock. 0: normal phase 1: reverse phase This signal can be controlled by configuring PERI_CRG49 bit[3].
sdioclk_sel	SDIO working clock select. 0: 24 MHz 1: 50 MHz This signal can be controlled by configuring PERI_CRG49 bit[2].

Table 3-17 describes the frequency configuration of the SFC clock.

Table 3-17 Frequency configuration of the SFC clock

Signal	Description
sfc_cksel	SFC2X clock source select. The 24 MHz clock is selected by default. 0: 24 MHz clock 1: 112.5 MHz clock This signal can be controlled by configuring PERI_CRG48 bit[2].

Table 3-18 describes the frequency configuration of the NFC clock.

Table 3-18 Frequency configuration of NFC clock

Signal	Description
nfc_cksel	NFC clock source select. The 24 MHz clock is selected by default. 0: 24 MHz clock 1: 99 MHz clock This signal can be controlled by configuring PERI_CRG52 bit[2].

Table 3-19 describes the frequency configurations of SIO clock.

Table 3-19 Frequency configurations of SIO clock

Signal	Description
sio0_ckcfg[23:0]	Division clock of SIO MCLK. The configured value is calculated as follows: (MCLK/Frequency of the SIO clock source) x 2^27. The clock source frequency is 675 MHz, and the maximum value of the MCLK is 62.5 MHz. This signal can be controlled by configuring PERI_CRG34 bit[23:0].
sio_fsclk_div	Division relationship between the bit clock BCLK and sampling clock FS of SIO. 000: The FS is generated by dividing the BCLK by 16. 001: The FS is generated by dividing the BCLK by 32. 010: The FS is generated by dividing the BCLK by 48. 011: The FS is generated by dividing the BCLK by 64. 100: The FS is generated by dividing the BCLK by 128. 101: The FS is generated by dividing the BCLK by 256. Other values: The FS is generated by dividing the BCLK by 8. This signal can be controlled by configuring PERI_CRG35 bit[14:12].
sio_bclk_div	Division relationship between the main clock MCLK and bit clock BCLK of SIO. 0000: The BCLK is generated by dividing the MCLK by 1.

Signal	Description
	0001: The BCLK is generated by dividing the MCLK by 3. 0010: The BCLK is generated by dividing the MCLK by 2. 0011: The BCLK is generated by dividing the MCLK by 4. 0100: The BCLK is generated by dividing the MCLK by 6. 0101: The BCLK is generated by dividing the MCLK by 8. 0110: The BCLK is generated by dividing the MCLK by 12. 0111: The BCLK is generated by dividing the MCLK by 16. 1000: The BCLK is generated by dividing the MCLK by 24. 1001: The BCLK is generated by dividing the MCLK by 32. 1010: The BCLK is generated by dividing the MCLK by 48. 1011: The BCLK is generated by dividing the MCLK by 64. Other values: The BCLK is generated by dividing the MCLK by 8. This signal can be controlled by configuring PERI_CRG35 bit[11:8].

The sampling rate clock frequency FSCLK is specified in general; however, the values of the bit clock BCLK and main clock MCLK are variable multiples of the value of FS. The following describes how to configure the clock frequency.

The clock source for SIO decimal division is fixed at 675 MHz. In this case, the required working clock frequencies of SIO are as follows: FSCLK = 48 kHz, MCLK = 256 FSCLK = 12.288 MHz, and BCLK = 16 FSCLK = 768 kHz. The following configurations are performed:

- The MCLK is generated by dividing a 675 MHz clock by a clock divider N. The value of N is calculated as follows: N = 12.288/675. Then sio_ckcfg[23:0] is N x 2^{27}. The result is rounded off to 2443359. Therefore, the correct frequency of the CLK is obtained after sio_ckcfg is set to 0x0025_485F.
- The BCLK is generated by dividing the MCLK. The clock divider is calculated as follows: BCLK/MCLK = 16/256 = 1/16. According to the mapping in Table 3-19, set sio_bclk_div[3:0] to 0b0111 (corresponding to the clock divider 16). Then the correct frequency of the BCLK is obtained.
- FSCLK is generated by dividing the BCLK by 1/16. According to the mapping in Table 3-19, set sio_fsclk_div to 0b000 (corresponding to the frequency divider 16). Then the correct frequency of the FS CLK is obtained.

Precautions

Take the following precautions when configuring clocks:

- By default, the ARM9 working clock is in crystal oscillator mode after power-on. That is, the crystal oscillator clock input by the XIN pin is selected.
- If the frequency of the PLL is changed, the PLL can output a stable clock 0.1 ms later. The frequency of the PLL can be changed only when the system runs in slow mode.
- If the PLL output clock is not stable, the system mode cannot be switched to PLL mode. You can view the PLL lock bit to check whether the PLL is locked. The status of the PLL lock bit can be obtained by reading PERI_CRG58 bit[3:0].

3.2.4 Register Summary

Table 3-20 describes CRG registers.

Table 3-20 Summary of CRG registers (base address: 0x2003_0000)

Offset Address	Register	Description	Page
0x0000	PERI_CRG0	APLL configuration register 0	3-16
0x0004	PERI_CRG1	APLL configuration register 1	3-17
0x0008	PERI_CRG2	VPLL0 configuration register 0	3-18
0x000C	PERI_CRG3	VPLL0 configuration register 1	3-18
0x0010	PERI_CRG4	BPLL configuration register 0	3-19
0x0014	PERI_CRG5	BPLL configuration register 1	3-20
0x0020	PERI_CRG8	EPLL configuration register 0	3-21
0x0024	PERI_CRG9	EPLL configuration register 1	3-22
0x0028	PERI_CRG10	ARM9/DDR frequency mode and reset configuration register	3-23
0x002C	PERI_CRG11	VICAP clock and reset configuration register	3-24
0x0030	PERI_CRG12	Sensor output clock configuration register	3-25
0x0034	PERI_CRG13	VOU clock and reset control register	3-26
0x0038	PERI_CRG14	PWM clock and reset control register	3-27
0x0040	PERI_CRG16	VEDU clock and soft reset control register	3-27
0x0048	PERI_CRG18	VPSS clock and soft reset control register	3-28
0x0058	PERI_CRG22	TDE clock and soft reset control register	3-29
0x0060	PERI_CRG24	JPGE clock and soft reset control register	3-30
0x0068	PERI_CRG26	MDU clock and soft reset control register	3-31
0x006C	PERI_CRG27	IVE clock and soft reset control register	3-32
0x007C	PERI_CRG31	CIPHER clock and soft reset control register	3-33
0x0080	PERI_CRG32	SAR ADC control register.	3-34
0x0088	PERI_CRG34	SIO MCLK control register.	3-35
0x008C	PERI_CRG35	SIO clock and soft reset control register.	3-35
0x00B8	PERI_CRG46	USB clock and soft reset control register	3-37
0x00C0	PERI_CRG48	SFC clock and soft reset control register	3-38
0x00C4	PERI_CRG49	SDIO clock and soft reset control register	3-39

Offset Address	Register	Description	Page
0x00CC	PERI_CRG51	ETH interface clock and soft reset control register	3-39
0x00D0	PERI_CRG52	NANDC clock and soft reset control register	3-40
0x00D8	PERI_CRG54	DDRTEST clock and soft reset control register	3-41
0x00E0	PERI_CRG56	Direct memory access (DMA) clock and soft reset control register	3-42
0x00E4	PERI_CRG57	Soft reset control register for other CRG interface modules	3-42
0x00E8	PERI_CRG58	CRG status register	3-44
0x00F4	PERI_CRG61	Speed monitor control register	3-45
0x00F8	PERI_CRG62	Speed monitor status register 1	3-46

3.2.5 Register Description

PERI_CRG0

PERI_CRG0 is APLL configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0000	PERI_CRG0	0x1100_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	apll_bypass	apll_postdiv2				apll_postdiv1		apll_frac																							
Reset	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved.
[30]	RW	apll_bypass	APLL clock frequency-division bypass control. 0: no bypass 1: bypass
[29:27]	RW	apll_postdiv2	Level-2 output divider of the APLL.
[26:24]	RW	apll_postdiv1	Level-1 output divider of the APLL.
[23:0]	RW	apll_frac	Decimal divider of the APLL.

PERI_CRG1

PERI_CRG1 is APLL configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0004	PERI_CRG1	0x006C_306E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								apll_dacpd	apll_dsmpd	apll_pd	apll_foutvcopd	apll_postdivpd	apll_fout4phasepd	apll_refdiv						apll_fbdiv											
Reset	0	0	0	0	0	0	0	0	0	1	1	0	1	1	0	0	0	0	1	0	0	0	0	0	1	0	0	1	1	0	1	1

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23]	RW	apll_dacpd	APLL test signal control. 0: power down 1: normal
[22]	RW	apll_dsmpd	APLL decimal frequency-division control. 0: decimal frequency-division mode 1: integer frequency-division mode
[21]	RW	apll_pd	APLL power down control. 0: power down 1: normal
[20]	RW	apll_foutvcopd	Power down control for the APLL VCO output. 0: no output clock 1: normal output clock
[19]	RW	apll_postdivpd	Power down control for the APLL POSTDIV output. 0: no output clock 1: normal output clock
[18]	RW	apll_fout4phasepd	Power down control for the APLL FOUT output. 0: no output clock 1: normal output clock
[17:12]	RW	apll_refdiv	Divider of the APLL reference clock.
[11:0]	RW	apll_fbdiv	Integral multiplier of the APLL.

PERI_CRG2

PERI_CRG2 is VPLL0 configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0008	PERI_CRG2	0x1200_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		vpll0_bypass		vpll0_postdiv2				vpll0_postdiv1				vpll0_frac																			
Reset	0		0		0		0		1		1		0		0		0		0		0		0		0		0		0		0	

Bits	Access	Name	Description
[31]	RO	reserved	Reserved.
[30]	RW	vpll0_bypass	VPLL0 clock frequency-division bypass control. 0: no bypass 1: bypass
[29:27]	RW	vpll0_postdiv2	Level-2 output divider of VPLL0.
[26:24]	RW	vpll0_postdiv1	Level-1 output divider of VPLL0.
[23:0]	RW	vpll0_frac	Decimal divider of VPLL0.

PERI_CRG3

PERI_CRG3 is VPLL0 configuration register 1.

Offset Address	Register Name	Total Reset Value
0x000C	PERI_CRG3	0x007C_2063

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								vpll0_dacpd		vpll0_dsmpd		vpll0_pd		vpll0_foutvcopd		vpll0_postdivpd		vpll0_fout4phasepd		vpll0_refdiv				vpll0_fbdiv							
Reset	0		0		0		0		0		1		1		0		1		0		0		1		0		0		1		0	

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.

[23]	RW	vpll0_dacpd	VPLL0 test signal control. 0: power down 1: normal
[22]	RW	vpll0_dsmpd	VPLL0 decimal frequency-division control. 0: decimal frequency-division mode 1: integer frequency-division mode
[21]	RW	vpll0_pd	VPLL0 power down control. 0: power down 1: normal
[20]	RW	vpll0_foutvcopd	Power down control for the VPLL0 VCO output. 0: no output clock 1: normal output clock
[19]	RW	vpll0_postdivpd	Power down control for the VPLL0 POSTDIV output. 0: no output clock 1: normal output clock
[18]	RW	vpll0_fout4phasepd	Power down control for the VPLL0 FOUT output. 0: no output clock 1: normal output clock
[17:12]	RW	vpll0_refdiv	Divider of the VPLL0 reference clock.
[11:0]	RW	vpll0_fbdiv	Integral multiplier of VPLL0.

PERI_CRG4

PERI_CRG4 is BPLL configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0010	PERI_CRG4	0x1100_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	bpll_bypass	bpll_postdiv2				bpll_postdiv1		bpll_frac																							
Reset	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved.

Offset Address	Register Name	Total Reset Value
0x0010	PERI_CRG4	0x1100_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		bpll_bypass		bpll_postdiv2				bpll_postdiv1				bpll_frac																			
Reset	0		0		0		0		1		0		0		0		0		0		0		0		0		0		0		0	

Bits	Access	Name	Description
[30]	RW	bpll_bypass	BPLL clock frequency-division bypass control. 0: no bypass 1: bypass
[29:27]	RW	bpll_postdiv2	Level-2 output divider of BPLL.
[26:24]	RW	bpll_postdiv1	Level-1 output divider of BPLL.
[23:0]	RW	bpll_frac	Decimal divider of BPLL.

PERI_CRG5

PERI_CRG5 is BPLL configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0014	PERI_CRG5	0x006C_306E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								bpll_dacpd		bpll_dsmpd		bpll_pd		bpll_foutvcopd		bpll_postdivpd		bpll_fout4phasepd		bpll_refdiv				bpll_fbdiv							
Reset	0		0		0		0		0		1		1		1		1		0		0		1		0		0		0		1	

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23]	RW	bpll_dacpd	BPLL test signal control. 0: power down 1: normal

Offset Address	Register Name	Total Reset Value
0x0014	PERI_CRG5	0x006C_306E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								bpll_dacpd	bpll_dsmpd	bpll_pd	bpll_foutvcopd	bpll_postdivpd	bpll_fout4phasepd	bpll_refdiv						bpll_fbdiv											
Reset	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	1	1	1

Bits	Access	Name	Description
[22]	RW	bpll_dsmpd	BPLL decimal frequency-division control. 0: decimal frequency-division mode 1: integer frequency-division mode
[21]	RW	bpll_pd	BPLL power down control. 0: power down 1: normal
[20]	RW	bpll_foutvcopd	Power down control for the BPLL VCO output. 0: no output clock 1: normal output clock
[19]	RW	bpll_postdivpd	Power down control for the BPLL POSTDIV output. 0: no output clock 1: normal output clock
[18]	RW	bpll_fout4phasepd	Power down control for the BPLL FOUT output. 0: no output clock 1: normal output clock
[17:12]	RW	bpll_refdiv	Divider of the BPLL reference clock.
[11:0]	RW	bpll_fbdiv	Integral multiplier of BPLL.

PERI_CRG8

PERI_CRG8 is EPLL configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0020	PERI_CRG8	0x1B00_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		epll_bypass		epll_postdiv2				epll_postdiv1				epll_frac																			
Reset	0		0		0		0		0		0		1		0		1		1		0		0		0		0		0		0	

Bits	Access	Name	Description
[31]	RO	reserved	Reserved.
[30]	RW	epll_bypass	EPLL clock frequency-division bypass control. 0: no bypass 1: bypass
[29:27]	RW	epll_postdiv2	Level-2 output divider of the EPLL.
[26:24]	RW	epll_postdiv1	Level-1 output divider of the EPLL.
[23:0]	RW	epll_frac	Decimal divider of the EPLL.

PERI_CRG9

PERI_CRG9 is EPLL configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0024	PERI_CRG9	0x007C_40E1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								epll_dacpd		epll_dsmpd		epll_pd		epll_foutvcopd		epll_postdivpd		epll_fout4phasepd		epll_refdiv				epll_fbdiv							
Reset	0		0		0		0		0		1		1		1		1		0		0		1		0		0		1		1	

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23]	RW	epll_dacpd	EPLL test signal control. 0: power down 1: normal

[22]	RW	epll_dsmpd	EPLL decimal frequency-division control. 0: decimal frequency-division mode 1: integer frequency-division mode
[21]	RW	epll_pd	EPLL power down control. 0: power down 1: normal
[20]	RW	epll_foutvcopd	Power down control for the EPLLVCO output. 0: no output clock 1: normal output clock
[19]	RW	epll_postdivpd	Power down control for the EPLL POSTDIV output. 0: no output clock 1: normal output clock
[18]	RW	epll_fout4phasepd	Power down control for the EPLL FOUT output. 0: no output clock 1: normal output clock
[17:12]	RW	epll_refdiv	Divider of the EPLL reference clock.
[11:0]	RW	epll_fbdiv	Integral multiplier of the EPLL.

PERI_CRG10

PERI_CRG10 is an ARM9/DDR frequency mode and reset configuration register.

Offset Address	Register Name	Total Reset Value
0x0028	PERI_CRG10	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					cpuclk_loaden	cpuclk_skipcfg					cpu_srst_req	freqmode_a9_sys		reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved.

[10]	RW	cpuclk_loaden	CPU clock DFS frequency division configuration enable. To change the frequency division configuration, perform the following steps: 1 Write a new frequency division configuration value. 2 Write 0 to veduclk_loaden. 3 Write 1 to veduclk_loaden.
[9:5]	RW	cpuclk_skipcfg	CPU clock DFS frequency division configuration. N: N-beat clocks are disabled every 32-beat CPU clocks.
[4]	RW	cpu_srst_req	CPU soft reset request. This bit is valid only in slave loading mode. 0: deassert reset 1: reset
[3:0]	RO	reserved	Reserved

PERI_CRG11

PERI_CRG11 is a VICAP clock and reset configuration register.

Offset Address	Register Name	Total Reset Value
0x002C	PERI_CRG11	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7	6	5	4	3	2	1	0
Name	reserved						vi_selftest	vi_pctrl	isp_cken	isp_rst_req	vi_cken	vi_rst_req	vi1_hcken	vi_hrst_req
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved
[7]	RW	vi_selftest	VICAP self-test mode. 0: normal mode. The I/O input clock is selected. 1: 1: self-test mode. The on-chip 24 MHz test clock is selected.
[6]	RW	vi_pctrl	VI input associated clock phase control. 0: normal phase clock 1: reverse phase clock
[5]	RW	isp_cken	VI ISP clock gating. 0: disabled 1: enabled

[4]	RW	isp_rst_req	VI ISP soft reset request. 0: deassert reset 1: reset
[3]	RW	vi_cken	VI clock gating. 0: disabled 1: enabled
[2]	RW	vi_rst_req	VI soft reset request. 0: deassert reset 1: reset
[1]	RW	vi1_hcken	VI bus clock gating. 0: disabled 1: enabled
[0]	RW	vi_hrst_req	VI bus soft reset request. 0: deassert reset 1: reset

PERI_CRG12

PERI_CRG12 is a sensor output clock configuration register.

Offset Address	Register Name	Total Reset Value
0x0030	PERI_CRG12	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														sense_cksel	
Reset	1	1	1	0	0	1	0	0	0	0	0	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RW	reserved	Reserved
[2:0]	RW	sense_cksel	Sensor output clock. 000: 12 MHz 001: 24 MHz 010: 27 MHz 011: 54 MHz 100: 13.5 MHz 101: 27 MHz 110: 37.125 MHz 111: 74.25 MHz

PERI_CRG13

PERI_CRG13 is a VOU clock and reset control register.

Offset Address	Register Name	Total Reset Value
0x0034	PERI_CRG13	0x0000_0017

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				hd_sd_sel	vou_sd_cken	vou_hd_cken	vou_hcken	reserved	ddac_pd_req	reserved	vohd_out_pctrl	reserved	vo_sd_srst_req	vo_hd_srst_req	vo_hrst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11]	RW	hd_sd_sel	VOU mode. 0: SD 1: HD
[10]	RW	vou_sd_cken	VOU SD DATE clock gating. 0: disabled 1: enabled
[9]	RW	vou_hd_cken	VOU HD clock gating. 0: disabled 1: enabled
[8]	RW	vou_hcken	VOU bus clock gating. 0: disabled 1: enabled
[7]	RW	reserved	Reserved.
[6]	RW	ddac_pd_req	VOU SD DAC power-down configuration. 0: normal mode 1: power down
[5]	RW	reserved	Reserved.
[4]	RW	vohd_out_pctrl	VOU HD output associated clock phase control. 0: normal phase clock 1: reverse phase clock
[3]	RO	reserved	Reserved.
[2]	RW	vo_sd_srst_req	VO SD soft reset request. 0: deassert reset 1: reset

[1]	RW	vo_hd_srst_req	VO HD soft reset request. 0: deassert reset 1: reset
[0]	RW	vo_hrst_req	VOU bus soft reset request. 0: deassert reset 1: reset

PERI_CRG14

PERI_CRG14 is a PWM clock and reset control register.

Offset Address	Register Name	Total Reset Value
0x0038	PERI_CRG14	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														pwm_cken	pwm_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1]	RW	pwm_cken	PWM clock gating. 0: disabled 1: enabled
[0]	RW	pwm_srst_req	PWM soft reset request. 0: deassert reset 1: reset

PERI_CRG16

PERI_CRG16 is a VEDU clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0040	PERI_CRG16	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				sed_cken	reserved	vedu0clk_loaden	vedu0clk_skipcfg					reserved		vedu0_cken	vedu0_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved.
[9]	RW	veduclk_loaden	VEDU clock frequency division configuration enable. 0: disabled 1: enabled To change the frequency division configuration, perform the following steps: 1 Write a new frequency division configuration value. 2 Write 0 to veduclk_loaden. 3 Write 1 to veduclk_loaden.
[8:4]	RW	veduclk_skipcfg	VEDU clock frequency division configuration. N: N-beat clocks are disabled every 32-beat VEDU clocks.
[3:2]	RO	reserved	Reserved.
[1]	RW	vedu0_cken	VEDU clock gating. 0: disabled 1: enabled
[0]	RW	vedu_srst_req	VEDU soft reset request. 0: deassert reset 1: reset

PERI_CRG18

PERI_CRG18 is a VPSS clock and reset control register.

Offset Address	Register Name	Total Reset Value
0x0048	PERI_CRG18	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						vpsclk_loaden		vpsclk_skipcfg					reserved		vps_cken	vps_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved.
[9]	RW	vpsclk_loaden	VPSS clock frequency division configuration enable. 0: disabled 1: enabled To change the frequency division configuration, perform the following steps: 1 Write a new frequency division configuration value. 2 Write 0 to vpsclk_loaden. 3 Write 1 to vpsclk_loaden.
[8:4]	RW	vpsclk_skipcfg	VPSS clock frequency division configuration. N: N-beat clocks are disabled every 32-beat VPSS clocks.
[3:2]	RO	reserved	Reserved.
[1]	RW	vps_cken	VPSS clock gating. 0: disabled 1: enabled
[0]	RW	vps_srst_req	VPSS soft reset request. 0: deassert reset 1: reset

PERI_CRG22

PERI_CRG22 is a TDE clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0058	PERI_CRG22	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						tdeclk_loaden	tdeclk_skipcfg					reserved		tde_cken	tde_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved.
[9]	RW	tdeclk_loaden	TDE clock frequency division configuration enable. 0: disabled 1: enabled To change the frequency division configuration, perform the following steps: 1 Write a new frequency division configuration value. 2 Write 0 to tdeclk_loaden. 3 Write 1 to tdeclk_loaden.
[8:4]	RW	tdeclk_skipcfg	TDE clock frequency division configuration. N: N-beat clocks are disabled every 32-beat TDE clocks.
[3:2]	RO	reserved	Reserved.
[1]	RW	tde_cken	TDE clock gating. 0: disabled 1: enabled
[0]	RW	tde_srst_req	TDE soft reset request. 0: deassert reset 1: reset

PERI_CRG24

PERI_CRG24 is a JPGE clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0060	PERI_CRG24	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						jpgeclk_loaden		jpgeclk_skipcfg					reserved		jpge_cken	jpge_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved.
[9]	RW	jpgeclk_loaden	JPGE clock frequency division configuration enable. 0: disabled 1: enabled To change the frequency division configuration, perform the following steps: 1 Write a new frequency division configuration value. 2 Write 0 to jpgeclk_loaden. 3 Write 1 to jpgeclk_loaden.
[8:4]	RW	jpgeclk_skipcfg	JPGE clock frequency division configuration. N: N-beat clocks are disabled every 32-beat TDE clocks.
[3:2]	RO	reserved	Reserved.
[1]	RW	jpge_cken	JPGE clock gating. 0: disabled 1: enabled
[0]	RW	jpge_srst_req	JPGE soft reset request. 0: deassert reset 1: reset

PERI_CRG26

PERI_CRG26 is an MDU clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0068	PERI_CRG26	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						mduclk_loaden	mduclk_skipcfg					reserved		mdu_cken	mdu_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved.
[9]	RW	mduclk_loaden	MDU clock frequency division configuration enable. 0: disabled 1: enabled To change the frequency division configuration, perform the following steps: 1 Write a new frequency division configuration value. 2 Write 0 to mduclk_loaden. 3 Write 1 to mduclk_loaden.
[8:4]	RW	mduclk_skipcfg	MDU clock frequency division configuration. N: N-beat clocks are disabled every 32-beat MDU clocks.
[3:2]	RO	reserved	Reserved.
[1]	RW	mdu_cken	MDU clock gating. 0: disabled 1: enabled
[0]	RW	mdu_srst_req	MDU soft reset request. 0: deassert reset 1: reset

PERI_CRG27

PERI_CRG27 is a VAPU clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x006C	PERI_CRG27	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						vapuclk_loaden	vapuclk_skipcfg					reserved		vapu_cken	vapu_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved.
[9]	RW	vapuclk_loaden	VAPU clock frequency division configuration enable. 0: disabled 1: enabled To change the frequency division configuration, perform the following steps: 1 Write a new frequency division configuration value. 2 Write 0 to vapuclk_loaden. 3 Write 1 to vapuclk_loaden.
[8:4]	RW	vapuclk_skipcfg	VAPU clock frequency division configuration. N: N-beat clocks are disabled every 32-beat VAPU clocks.
[3:2]	RO	reserved	Reserved.
[1]	RW	vapu_cken	VAPU clock gating. 0: disabled 1: enabled
[0]	RW	vapu_srst_req	VAPU soft reset request. 0: deassert reset 1: reset

PERI_CRG31

PERI_CRG31 is a CIPHER clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x007C	PERI_CRG31	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														cipher_cken	cipher_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1]	RW	cipher_cken	CIPHER clock gating. 0: disabled 1: enabled
[0]	RW	cipher_srst_req	CIPHER soft reset request. 0: deassert reset 1: reset

PERI_CRG32

PERI_CRG32 is SAR ADC control register.

Offset Address	Register Name	Total Reset Value
0x0080	PERI_CRG32	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														sar_adc_cken	sar_adc_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1]	RW	sar_adc_cken	SAR ADC clock gating. 0: disabled 1: enabled

[0]	RW	sar_adc_srst_req	SAR ADC soft reset request. 0: deassert reset 1: reset

PERI_CRG34

PERI_CRG34 is SIO MCLK control register.

Offset Address	Register Name	Total Reset Value
0x0088	PERI_CRG34	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								sio_ckcfg																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:0]	RW	sio_ckcfg	Division clock of SIO MCLK. The configured value is calculated as follows: (MCLK/Frequency of the SIO clock source) x 2^27. The clock source frequency is 675 MHz, and the maximum value of the MCLK is 62.5 MHz.

PERI_CRG35

PERI_CRG35 is SIO clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x008C	PERI_CRG35	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																adac_srst_req	sio_fsclk_div			sio_bclk_div				reserved						sio_cken	sio_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15]	RW	adac_srst_req	Audio Codec soft reset request. 0: deassert reset 1: reset

[14:12]	RW	sio_fsclk_div	Division relationship between the bit clock BCLK and sampling clock FS. 000: The FS is generated by dividing the BCLK by 16. 001: The FS is generated by dividing the BCLK by 32. 010: The FS is generated by dividing the BCLK by 48. 011: The FS is generated by dividing the BCLK by 64. 100: The FS is generated by dividing the BCLK by 128. 101: The FS is generated by dividing the BCLK by 256. Other values: The FS is generated by dividing the BCLK by 8.
[11:8]	RW	sio_bclk_div	Division relationship between the main clock MCLK and bit clock BCLK. 0000: The BCLK is generated by dividing the MCLK by 1. 0001: The BCLK is generated by dividing the MCLK by 3. 0010: The BCLK is generated by dividing the MCLK by 2. 0011: The BCLK is generated by dividing the MCLK by 4. 0100: The BCLK is generated by dividing the MCLK by 6. 0101: The BCLK is generated by dividing the MCLK by 8. 0110: The BCLK is generated by dividing the MCLK by 12. 0111: The BCLK is generated by dividing the MCLK by 16. 1000: The BCLK is generated by dividing the MCLK by 24. 1001: The BCLK is generated by dividing the MCLK by 32. 1010: The BCLK is generated by dividing the MCLK by 48. 1011: The BCLK is generated by dividing the MCLK by 64. Other values: The BCLK is generated by dividing the MCLK by 8.
[7]	RW	sio_fs_rxtx_sel	Multiplexing relationship between the SIO TX FS and RX FS. 0: The RX FS is independent of the TX FS. 1: The TX FS multiplexes with the RX FS.
[6]	RW	sio_bclk_rxtx_sel	Multiplexing relationship between the SIO TX BCLK and RX BCLK. 0: The RX BCLK is independent of the TX BCLK. 1: The TX BCLK multiplexes with the RX BCLK.
[5]	RO	reserved	Reserved.
[4]	RW	sio_bclk_sel	SIO BCLK select. 0: external BCLK of the Hi3518 1: internal BCLK of the Hi3518
[3]	RW	sio_bclkout_pctrl	Polarity of SIO BCLK output. 0: normal phase 1: reverse phase

[2]	RW	sio_bclk_pctrl	SIO BCLK polarity. 0: normal phase 1: reverse phase
[1]	RW	sio_cken	SIO clock gating. 0: disabled 1: enabled
[0]	RW	sio_srst_req	SIO soft reset request. 0: deassert reset 1: reset

PERI_CRG46

PERI_CRG46 is a USB clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00B8	PERI_CRG46	0x0000_00B7

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								usb_cken	usb_ctrl_utmi1_req	usb_ctrl_utmi0_req	usb_ctrl_hub_req	usbphy_port1_treq	usbphy_port0_treq	usbphy_req	usb_ahb_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7]	RW	usb_cken	USB PHY reference clock gating. 0: disabled 1: enabled
[6]	RW	reserved	Reserved.
[5]	RW	usb_ctrl_utmi0_req	Soft reset request of USB controller port0. 0: deassert reset 1: reset
[4]	RW	usb_ctrl_hub_req	Soft reset request of the USB controller hub. 0: deassert reset 1: reset
[3]	RW	reserved	Reserved.

[2]	RW	usbphy_port0_treq	Soft reset request of USB PHY port0. 0: deassert reset 1: reset
[1]	RW	usbphy_req	Soft reset request of the USB PHY. 0: deassert reset 1: reset
[0]	RW	usb_ahb_srst_req	Soft reset request of the USB controller bus. 0: deassert reset 1: reset

PERI_CRG48

PERI_CRG48 is an SFC clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00C0	PERI_CRG48	0x0000_0002

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2	1	0
Name	reserved							sfc_cksel	sfc_cken	sfc_srst_req
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	1	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2]	RW	sfc_cksel	SFC2X clock source select. The 24 MHz clock is selected by default. 0: 24 MHz clock 1: 112.5 MHz clock
[1]	RW	sfc_cken	SFC clock gating. 0: disabled 1: enabled
[0]	RW	sfc_srst_req	SFC soft reset request. 0: deassert reset 1: reset

PERI_CRG49

PERI_CRG49 is an SDIO clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00C4	PERI_CRG49	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												sdioclk_pctrl	sdioclk_sel	sdio_cken	sdio_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:5]	RW	reserved	Reserved.
[4]	RW	sdioclk_pctrl	Polarity of the SDIO SAP clock. 0: normal phase 1: reverse phase
[3:2]	RW	sdioclk_sel	SDIO working clock select. 00: 24 MHz 01: 50 MHz 1X: reserved
[1]	RW	sdio_cken	SDIO clock gating. 0: disabled 1: enabled
[0]	RW	sdio_srst_req	SDIO soft reset request. 0: deassert reset 1: reset

PERI_CRG51

PERI_CRG51 is an ETH interface clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00CC	PERI_CRG51	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										gmac0_if_srst_req	toe_cksel	toe_hcken	toe_hrst_req	toe_cken	toe_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:6]	RW	ethcore_cksel	ETH working clock select. 00: 54 MHz clock 01: 27 MHz clock Others: 99 MHz clock
[5:4]	RW	ethphy_cksel	EHTPHY output clock select. 00: 25 MHz clock 01: 24 MHz clock Others: 27 MHz clock
[3]	RW	mii_rmii_mode	ETH mode. 0: MII mode 1: RMII mode
[2]	RW	eth_rmiick_sel	ETH RMII clock source select. 0: internal CRG clock 1: PAD input clock
[1]	RW	eth_cken	ETH clock gating. 0: disabled 1: enabled
[0]	RW	hrst_eth_s	ETH soft reset request. 0: deassert reset 1: reset

PERI_CRG52

PERI_CRG52 is a NANDC clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00D0	PERI_CRG52	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													nfc_cksel	nfc_cken	nfc_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2]	RW	nfc_cksel	NFC clock source select. The 24 MHz clock is selected by default. 0: 24 MHz clock 1: 99 MHz clock
[1]	RW	nfc_cken	NFC clock gating. 0: disabled 1: enabled
[0]	RW	nfc_srst_req	NFC soft reset request. 0: deassert reset 1: reset

PERI_CRG54

PERI_CRG54 is a DDRTEST clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00D8	PERI_CRG54	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ddrtest_cken	ddrtest_srst_req	efuse_cken	efuse_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.

[3]	RW	ddrtest_cken	DDRTEST clock gating. 0: disabled 1: enabled
[2]	RW	ddrtest_srst_req	DDRTEST soft reset request. 0: deassert reset 1: reset
[1:0]	RW	reserved	Reserved.

PERI_CRG56

PERI_CRG56 is a DMA clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00E0	PERI_CRG56	0x0000_0008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														dma_cken	dma_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1]	RW	dma_cken	DMA clock gating. 0: disabled 1: enabled
[0]	RW	dma_srst_req	DMA soft reset request. 0: deassert reset 1: reset

PERI_CRG57

PERI_CRG57 is a soft reset control register for other CRG interface modules.

Offset Address	Register Name	Total Reset Value
0x00E4	PERI_CRG57	0x0003_F000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														urat2_cken	uart1_cken	uart0_cken	ssp1_cken	ssp0_cken	ir_cken	reserved		uart2_srst_req	uart1_srst_req	uart0_srst_req	ssp1_srst_req	ssp0_srst_req	ir_srst_req	reserved	t_cap_srst_req	i2c_srst_req	test_clk_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved.
[17]	RW	urat2_cken	UART2 clock gating. 0: disabled 1: enabled
[16]	RW	uart1_cken	UART1 clock gating. 0: disabled 1: enabled
[15]	RW	uart0_cken	UART0 clock gating. 0: disabled 1: enabled
[14]	RW	ssp1_cken	SSP1 clock gating. 0: disabled 1: enabled
[13]	RW	ssp0_cken	SSP0 clock gating. 0: disabled 1: enabled
[12]	RW	ir_cken	IR clock gating. 0: disabled 1: enabled
[11:10]	RW	reserved	Reserved.
[9]	RW	uart2_srst_req	UART2 soft reset request. 0: deassert reset 1: reset
[8]	RW	uart1_srst_req	UART1 soft reset request. 0: deassert reset 1: reset

[7]	RW	uart0_srst_req	UART0 soft reset request. 0: deassert reset 1: reset
[6]	RW	ssp1_srst_req	SSP1 soft reset request. 0: deassert reset 1: reset
[5]	RW	ssp0_srst_req	SSP0 soft reset request. 0: deassert reset 1: reset
[4]	RW	ir_srst_req	IR soft reset request. 0: deassert reset 1: reset
[3]	RW	reserved	Reserved.
[2]	RW	t_cap_srst_req	t_cap soft reset request. 0: deassert reset 1: reset
[1]	RW	i2c_srst_req	I2C soft reset request. 0: deassert reset 1: reset
[0]	RW	test_clk_en	Test clock enable. 0: All test clocks are disabled. 1: All test clocks are enabled.

PERI_CRG58

PERI_CRG58 is a CRG status register.

Offset Address	Register Name	Total Reset Value
0x00E8	PERI_CRG58	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												epll_lock	bpll_lock	vpll0_lock	apll_lock
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.

[3]	RO	epll_lock	EPLL lock status. 0: unlocked 1: locked
[2]	RO	bpll_lock	BPLL lock status. 0: unlocked 1: locked
[1]	RO	vpll0_lock	VPLL0 lock status. 0: unlocked 1: locked
[0]	RO	apll_lock	APLL lock status. 0: unlocked 1: locked

PERI_CRG61

PERI_CRG61 is a speed monitor control register.

Offset Address	Register Name	Total Reset Value
0x00F4	PERI_CRG61	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													osc_en	osc_mode	osc_clk_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2]	RW	osc_en	Speed monitor enable. 0: disabled 1: enabled
[1]	RW	osc_mode	Speed monitor mode. 0: 150-step level 1: 200-step level
[0]	RW	osc_clk_en	Speed monitor clock enable. 0: disabled 1: enabled

PERI_CRG62

PERI_CRG62 is speed monitor status register 1.

Offset Address	Register Name	Total Reset Value
0x00F8	PERI_CRG62	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10	9	8	7 6 5 4	3 2 1 0
Name	reserved						osc_valid		osc _value	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0	0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved.
[9]	RO	osc_valid	Status of the SpeedMonitor. 0: invalid; 1: valid.
[8:0]	RO	osc_value	Value of the SpeedMonitor.

3.3 Interrupt System

Table 3-21describes the ARM9 interrupt sources.

Table 3-21 ARM9 interrupt sources

Interrupt Bit	Interrupt Source
0	Global software interrupt
1	WDT interrupt when periphctrl0 bit[31] is 0 COMMRX interrupt or WDT interrupt when periphctrl0 bit[31] is 1
2	RTC interrupt when periphctrl0 bit[31] is 0 COMMRX interrupt or RTC interrupt when periphctrl0 bit[31] is 1
3	Timer0/Timer1
4	Timer2/Timer3
5	UART0/UART1
6	SSP0 Note: The Hi3518C has no SSP0.
7	SSP1 Note: The Hi3518C has no SSP1.

Interrupt Bit	Interrupt Source
8	NANDC Note: The Hi3518C has no NANDC.
9	SIO
10	Temper_Cap
11	SFC
12	ETH
13	CIPHER
14	DMAC
15	USB_EHCI
16	USB_OHCI
17	VPSS
18	SDIO
19	IR/SAR_ADC Note: The Hi3518C has no IR.
20	I^2C
21	IVE
22	VICAP
23	VOU
24	VEDU
25	UART2 Note: The Hi3518C has no UART2.
26	JPGE
27	TDE
28	MDU/DDRT
29	GPIO0/GPIO1/GPIO2/GPIO11
30	GPIO3/GPIO4/GPIO5/GPIO10
31	GPIO6/GPIO7/GPIO8/GPIO9 Note: The Hi3518C has no GPIO8 and GPIO9.

3.3.1 Register Summary

Table 3-22 lists the INT registers.

Table 3-22 Summary of the INT registers (based address: 0x1014_0000)

Offset Address	Register	Description	Page
0x000	INT_IRQSTATUS	IRQ interrupt status register	3-48
0x004	INT_FIQSTATUS	FIQ interrupt status register	3-48
0x008	INT_RAWINTR	Raw interrupt status register	3-49
0x00C	INT_INTSELECT	Interrupt source select register	3-49
0x010	INT_INTENABLE	Interrupt enable register	3-50
0x014	INT_INTENCLEAR	Interrupt enable clear register	3-50
0x018	INT_SOFTINT	Software interrupt register	3-51
0x01C	INT_SOFTINTCLEAR	Software interrupt clear register	3-51
0x020	INT_PROTECTION	Protection enable register	3-52

3.3.2 Register Description

INT_IRQSTATUS

INT_IRQSTATUS is the IRQ interrupt status register.

Offset Address	Register Name	Total Reset Value
0x000	INT_IRQSTATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	irqstatus																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	irqstatus	Status of the IRQ interrupt source. 0: No interrupt is generated. 1: An IRQ interrupt is generated and sent to the processor.

INT_FIQSTATUS

INT_FIQSTATUS is the FIQ interrupt status register. The 32 bits of INT_INTENABLE map to 32 interrupt sources.

Offset Address	Register Name	Total Reset Value
0x004	INT_FIQSTATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fiqstatus																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	fiqstatus	Status of the FIQ interrupt source. 0: No interrupt is generated. 1: An FIQ interrupt is generated and sent to the processor.

INT_RAWINTR

INT_RAWINTR is the raw interrupt status register. It shows the status of raw interrupt requests and the status of the software interrupts that are generated by configuring INT_SOFTINT. The 32 bits of INT_RAWINTR map to 32 interrupt sources.

Offset Address	Register Name	Total Reset Value
0x008	INT_RAWINTR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rawinterrupt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rawinterrupt	Status of the interrupt requests of raw interrupt sources. 0: No interrupt is generated. 1: An interrupt is generated.

INT_INTSELECT

INT_INTSELECT is the interrupt source select register. It determines whether the selected interrupt sources generate IRQ interrupts or FIQ interrupts. The 32 bits of INT_INTSELECT map to 32 interrupt sources.

Offset Address	Register Name	Total Reset Value
0x00C	INT_INTSELECT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	intselect																															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	intselect	Interrupt request type of interrupt sources. 0: IRQ interrupt 1: FIQ interrupt

INT_INTENABLE

INT_INTENABLE is the interrupt enable register. It is used to enable interrupt request lines. After reset, the value of INT_INTENABLE is changed to 0x0000_0000. As a result, all interrupt sources are masked. The 32 bits of INT_INTENABLE map to 32 interrupt sources.

Offset Address	Register Name	Total Reset Value
0x010	INT_INTENABLE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	intenable																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	intenable	Returned mask status of each interrupt source when this register is read. 0: masked 1: not masked Interrupt source is enabled bit by bit when this register is written. 0: The current value of the corresponding bit is not affected. 1: The corresponding bit is set to 1 to enable the corresponding interrupt request.

INT_INTENCLEAR

INT_INTENCLEAR is the interrupt enable clear register. It is used to clear the corresponding bits of INT_INTENABLE. INT_INTENCLEAR is write-only and has no default reset value.

Offset Address	Register Name	Total Reset Value
0x014	INT_INTENCLEAR	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	intenableclear																															

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Access	Name	Description
[31:0]	WO	intenableclear	Mask of the interrupt source corresponding to INT_INTENABLE. 0: The current value of the corresponding bit of INT_INTENABLE is not affected. 1: The corresponding bit of INT_INTENABLE is cleared and the corresponding interrupt request is masked.

INT_SOFTINT

INT_SOFTINT is the software interrupt register. Through software, it controls whether to generate interrupts by the interrupt source input lines. The software interrupts can be cleared by writing INT_SOFTINTCLEAR. The clear operation is performed after the ISR is executed.

Offset Address	Register Name	Total Reset Value
0x018	INT_SOFTINT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	softint																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	softint	Generates a raw software interrupt on a specified interrupt source. 0: The current value of the corresponding bit is not affected. 1: The corresponding bit is set to 1 and a software interrupt request is generated.

INT_SOFTINTCLEAR

INT_SOFTINTCLEAR is the software interrupt clear register. It is used to clear the corresponding bit of INT_SOFTINT. INT_SOFTINTCLEAR is write-only and has no default reset value.

Offset Address	Register Name	Total Reset Value
0x01C	INT_SOFTINTCLEAR	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	softintclear																															

Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Access	Name	Description
[31:0]	WO	softintclear	Mask of the interrupt request corresponding to INT_SOFTINT. 00: The corresponding bit of INT_SOFTINT is not affected. 1: The corresponding bit of INT_SOFTINT is cleared and the corresponding interrupt request is masked.

INT_PROTECTION

INT_PROTECTION is the protection enable register It is used to enable or disable the access to the protected registers.

CAUTION

- After reset, this register is cleared and the registers of the INT can be accessed in both user mode and privileged mode.
- When the CPU cannot generate the correct protection information (HPROT), the registers of the INT can be accessed in user mode after INT_PROTECTION is reset.

Offset Address	Register Name	Total Reset Value
0x020	INT_PROTECTION	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															protection
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	protection	Register access protection enable. 0: disabled. The registers of the INT can be accessed both in user mode and privileged mode. 1: enabled. The registers of the INT can be access in privileged mode only.

3.4 System Controller

3.4.1 Overview

The system controller controls the operating mode from several aspects. To be specific, it controls the operating mode of the system, monitors the system status, manages the key functions of the system, and configures some functions of peripherals.

3.4.2 Features

The system controller has the following features:

- Controls and monitors the operating mode of the system.
- Controls the system clock and queries its status.
- Controls the system address remap and monitors its status.
- Provides general peripheral registers
- Provides write protection for key registers.
- Provides chip identification (ID) registers.

3.4.3 Function Description

Controlling the System Operating Mode

The system can work in any of the following modes:

- Normal mode

  In general, the system works in normal mode. In this mode, the system is driven by the output clock of the on-chip APLL. All modules can work properly under this clock source. Some peripherals can be driven by the output clock of VPLL0, VPLL1, or EPLL.

- Slow mode

  The slow mode is a low-speed mode. In this mode, the system is driven by the external crystal oscillator clock. Only part of on-chip peripherals (such as system controller, timer, NANDC, and SFC) work properly. Modules (such as the DDRC) that require high-speed clock cannot work under the crystal oscillator clock.

- Doze mode

  The doze mode is also a slow-speed mode, but its speed is lower than the speed of the slow mode. Only a few on-chip peripherals can work in doze mode. In this mode, the system is driven by a 46.875 kHz low-frequency clock. This clock is generated by dividing the external crystal oscillator. Except the CPU and a few modules (such as the system controller, timer, and IR), most on-chip peripherals and the memory interface cannot work in this mode.

The system controller provides a mode switching mechanism to switch the system clock source. The mode is switched by configuring three bits of the mode control register SC_CTRL [modectrl]. These bits define the operating mode to which the system is switched.

- 000: reserved
- 001: doze mode
- 010: slow mode
- 100: normal mode

- Other values: reserved

When the required system operating mode is specified by configuring the system mode control register, the system operating mode is switched to the target mode. In this case, no software intervention or command intervention is required.

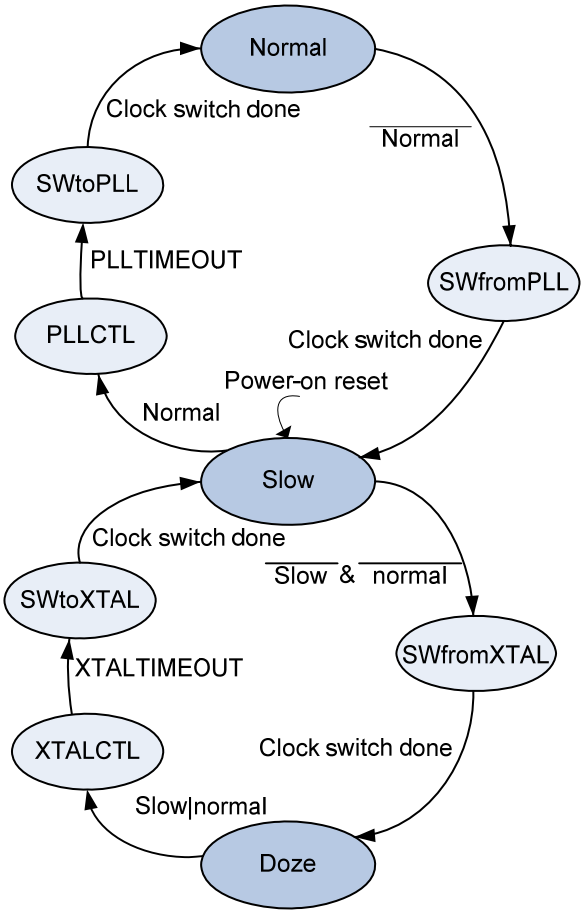
The current system status can be queried by reading SC_CTRL [modestatus]. SC_CTRL [modestatus] shows not only the preceding three main modes (normal, slow, and doze modes), but also the following intermediate status between the main modes: SWfromPLL, SWtoPLL, PLLCTL, SWfromXTAL, SWtoXTAL, and XTALCTL.

NOTE

The normal, slow, and doze modes can be switched directly. For example, if the system is in normal mode, you can switch the system to doze mode by setting SC_CTRL [modectrl] to 001. The system mode is switched to SWfromPLL, slow, and then SWfromXTAL modes before being switched to the doze mode.

Figure 3-3 shows the process of switching the system mode.

Figure 3-3 Process of switching the system mode



The operations involved in mode switching are as follows:

- When the most significant bit (MSB) of SC_CTRL [modectrl] is set to 0, the system exits the normal mode and is switched to the slow mode.
- Before being switched from the normal mode to the slow mode, the system is switched to the SWfromPLL status. This indicates that the system clock source is switched from the PLL to the crystal oscillator. After the clock switching is done, the system enters the slow mode.
- After power-on reset, the system is in slow mode. When the MSB of SC_CTRL [modectrl] is set to 1, the system enters the normal mode. During the switching to normal mode, the system is switched to the PLLCTL status to enable the ARMPLL. After a fixed wait time (the wait time depends on SC_XTALCTRL[plltime]), the system enters the SWtoPLL status to switch the clock source. After the switching is done, the system enters the normal mode.
- When the upper two bits of SC_CTRL [modectrl] are set to 0, the system is switched to the doze mode. In this case, the system is first switched to the SWfromXTAL status. This indicates that the system clock source is switched from the crystal oscillator clock to a 46.875 kHz low-frequency clock. The 46.875 kHz clock is generated by dividing the crystal oscillator clock. After the clock switching is done, the system enters the doze mode.
- When either of the upper two bits of SC_CTRL [modectrl] is set to 1, the system is switched to the slow mode. During the switching to the slow mode, the system is switched to the XTALCTL status to initialize the clock module. After a fixed wait time (the wait time depends on SC_XTALCTRL[xtaltime]), the system enters the SWtoXTAL status to switch the clock source. After the switching is done, the system enters the slow mode.

For details about the mapping between the status of the system controller and system clocks, see Table 3-6.

Soft Reset

The system controller can soft-reset the entire chip or some modules.

After the global soft reset register SC_SYSRES is configured, the system controller transmits a reset request to the on-chip reset module for setting the Hi3518.

System Address Remap Control

For details, see section 1.3 "Boot Modes."

Write Protection for Key Registers

To avoid the entire system being severely affected by the misoperation on the system controller, the system controller provides write protection for key configuration registers. The key configuration registers are as follows:

- Mode switching control register: SC_CTRL
- Control register for system global soft reset: SC_SYSRES
- PLL control register: SC_PLLCTRL
- Peripheral control register 0 and peripheral control register 1: PERIPHCTRL0 and PERIPHCTRL1

Before writing to these key registers, you must disable the write protection function by configuring SC_LOCKEN. After writes, you need to enable the write protection function by configuring SC_LOCKEN again. This ensures that these key registers are not overwritten by the software arbitrarily.

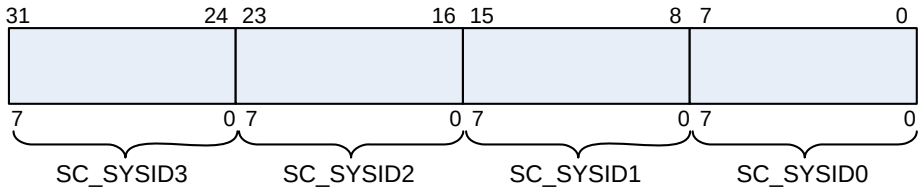
NOTE

By default, write protection is not enabled for key registers after reset. It is recommended that you enable write protection by configuring SC_LOCKEN when the system starts.

System ID Register of the Chip

The system controller provides a chip ID register SC_SYSID. This register is a virtual 32-bit read-only register. It consists of four 8-bit ID registers: SC_SYSID3, SC_SYSID2, SC_SYSID1, and SC_SYSID0. After the values of these four registers are read and combined, the value of SC_SYSID, namely, 0x3518_0100, is obtained. Figure 3-4 shows the bit allocation of chip ID registers.

Figure 3-4 Bit allocation of chip ID registers



3.4.4 Register Summary

Table 3-23 describes the registers of the system controller.

Table 3-23 Summary of the system controller registers (base address: 0x2005_0000)

Offset Address	Register	Description	Page
0x000	SC_CTRL	System control register	3-58
0x004	SC_SYSRES	System soft reset register	3-60
0x008	SC_IMCTRL	Interrupt mode control register	3-60
0x00C	SC_IMSTAT	Interrupt mode status register	3-61
0x010	SC_XTALCTRL	Crystal oscillator control register	3-62
0x014	SC_PLLCTRL	PLL control register	3-63
0x01C	PERIPHCTRL0	Peripheral control register 0	3-64
0x0020	PERIPHCTRL1	Software interrupt register	3-65
0x0038	PERIPHCTRL3	Peripheral control register 3 (MDDRC out-of-order configuration register outtodr_ctrl)	3-65

Offset Address	Register	Description	Page
0x003C	PERIPHCTRL4	Peripheral control register 4	3-67
0x0040	PERIPHCTRL5	Peripheral control register 5 (media bus timeout control register 1 for master port l)	3-68
0x0044	SC_LOCKEN	Lock register of key system control registers	3-69
0x0048	PERIPHCTRL6	Peripheral control register 6 (media bus timeout control register 2 for master port l).	3-69
0x004C	PERIPHCTRL7	Peripheral control register 7 (media bus timeout control register 3 for master port l)	3-70
0x0054	PERIPHCTRL9	Peripheral control register 9 (media bus priority configuration register for master port l)	3-71
0x0058	PERIPHCTRL10	Peripheral control register 10 (system bus timeout control register 1 for master port l)	3-72
0x005C	PERIPHCTRL11	Peripheral control register 11 (system bus timeout control register 2 for master port l)	3-73
0x0060	PERIPHCTRL12	Peripheral control register 12 (system bus priority configuration register for master port l)	3-74
0x0064	PERIPHCTRL13	Peripheral control register 13 (system bus priority configuration register for slave port l)	3-75
0x0068	PERIPHCTRL14	Peripheral control register 14 (audio CODEC control register 0)	3-75
0x006C	PERIPHCTRL15	Peripheral control register 15 (audio CODEC control register 1)	3-78
0x0070	PERIPHCTRL16	Peripheral control register 16 (audio CODEC control register 2)	3-82
0x0074	PERIPHCTRL17	Peripheral control register 17 (audio CODEC control register 3)	3-83
0x0078	PERIPHCTRL18	Peripheral control register 18 (audio CODEC control register 4)	3-85
0x007C	PERIPHCTRL19	Peripheral control register 19 (audio CODEC control register 5)	3-87
0x0080	PERIPHCTRL20	Peripheral control register 20 (USB control register 1)	3-88
0x0084	PERIPHCTRL21	Peripheral control register 21 (USB control register 2)	3-90

Offset Address	Register	Description	Page
0x008C	SYSSTAT	System status register (PLL_LOCK)	3-92
0xEE0	SCSYSID0	Chip ID register 0	3-93
0xEE4	SCSYSID1	Chip ID register 1	3-94
0xEE8	SCSYSID2	Chip ID register 2	3-94
0xEEC	SCSYSID3	Chip ID register 3	3-94

3.4.5 Register Description

SC_CTRL

SC_CTRL is a system control register. It is used to specify the operations that are performed by the system.

CAUTION

Write protection for this register can be enabled by configuring SC_LOCKEN. This register can be written only when write protection is disabled.

Offset Address	Register Name	Total Reset Value
0x000	SC_CTRL	0x0000_0212

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	timeren7ov	timeren7sel	timeren6ov	timeren6sel	timeren5ov	timeren5sel	timeren4ov	timeren4sel	wdogenov	timeren3ov	timeren3sel	timeren2ov	timeren2sel	timeren1ov	timeren1sel	timeren0ov	timeren0sel	reserved					remapstat	remapclear	reserved	modestatus			modectrl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	1	0

Bits	Access	Name	Description
[31:24]	RW	reserved	Reserved.
[23]	RW	wdogenov	Watchdog count clock select. 0: 3 MHz clock 1: bus clock
[22]	RW	timeren3ov	Count clock select of timer3. 0: 3 MHz clock. 1: bus clock

[21]	RW	reserved	Reserved.
[20]	RW	timeren2ov	Count clock select of timer2. 0: 3 MHz clock 1: bus clock
[19]	RW	reserved	Reserved.
[18]	RW	timeren1ov	Count clock select of timer1. 0: 3 MHz clock 1: bus clock
[17]	RW	reserved	Reserved.
[16]	RW	timeren0ov	Count clock select of timer0. 0: 3 MHz clock 1: bus clock
[15]	RW	reserved	Reserved.
[14:10]	-	reserved	Reserved. Reading this field returns 0 and writing to this field has no effect.
[9]	RO	remapstat	Status of address remap. 0: The address is not remapped. 1: The address is remapped. The details are as follows: NANDC or SFC is remapped to address 0.
[8]	RW	remapclear	Address remap clear. 0: keep the remap status 1: clear the remap status For details about the address mappings before and after remapping is cleared, see Table 1-1.
[7]	-	reserved	Reserved. Reading this bit returns 0 and writing to this bit has no effect.
[6:3]	RW	modestatus	Mode status. The current operating mode of the system is returned. 0x0: reserved 0x1: doze 0x2: slow 0x3: XTAL CTL 0x4: normal 0x6: PLL CTL 0x9: SW from XTAL 0xA: SW from PLL 0xB: SW to XTAL 0xE: SW to PLL Other values: reserved

[2:0]	RW	modectrl	Mode control. This field defines the operating mode to which the system controller is switched. 000: reserved 001: doze 010: slow 100: normal

SC_SYSRES

SC_SYSRES is a system soft reset register. When any value is written to this register, the system controller transmits a system soft reset request to the reset module. Then the reset module resets the system.

CAUTION

Write protection for this register can be enabled by configuring SC_LOCKEN. This register can be written only when write protection is disabled.

Offset Address	Register Name	Total Reset Value
0x004	SC_SYSRES	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	softresreq																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:0]	WO	softresreq	The system is reset when any value is written to this register.

SC_IMCTRL

SC_IMCTRL is an interrupt mode control register. It is used to control the system mode when an interrupt is generated.

Offset Address	Register Name	Total Reset Value
0x008	SC_IMCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								inmdtype	reserved			itmdctrl		itmden	

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved. Reading this field returns 0x000000 and writing to this field has no effect.
[7]	RW	inmdtype	Type of the interrupt for triggering the interrupt mode of the system. 0: fast interrupt request (FIQ) interrupt 1: FIQ interrupt or interrupt request (IRQ) interrupt
[6:4]	-	reserved	Reserved.
[3:1]	RW	itmdctrl	Operating mode of the system with the lowest speed in interrupt mode. The value obtained after the values of this register and SC_CTRL[modectrl] are ORed indicates the operating mode of the system after an interrupt is generated. The definitions of these bits are as follows: 000: sleep 001: doze 01X: slow 1XX: normal
[0]	RW	itmden	Interrupt mode enable. 0: disabled 1: enabled. When an interrupt is generated, the system enters the interrupt mode.

SC_IMSTAT

SC_IMSTAT is an interrupt mode status register. It is used to check whether the system is in interrupt mode. The system can be set to the interrupt mode forcibly by configuring this register.

CAUTION

When the interrupt service routine (ISR) ends, the interrupt mode must be cleared manually.

Offset Address	Register Name	Total Reset Value
0x00C	SC_IMSTAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															itmdstat

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved. Reading this field returns 0x00000000 and writing to this field has no effect.
[0]	RW	itmdstat	Interrupt mode status. The bit is used by software for controlling whether the system enters the interrupt mode. When the register is read: 0: The system is not in interrupt mode. 1: The system is in interrupt mode. When the register is written: 0: Software controls whether the system enters the interrupt mode. 1: Software does not control whether the system enters the interrupt mode.

SC_XTALCTRL

SC_XTALCTRL is a crystal oscillator control register. It is used to specify the stable wait time after the clock module is initialized. The stable wait time is the period when the system is switched from the XTAL CTL mode to the SW-to-XTAL mode.

Offset Address	Register Name	Total Reset Value
0x010	SC_XTALCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												xtaltime																reserved		reserved	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	-	reserved	Reserved. Reading this field returns 0x0000 and writing to this field has no effect.
[18:3]	RW	xtaltime	Wait time of crystal oscillator switching. The value of this field is used to specify the time spent on switching the system mode from XTAL CTL to SW-to-XTAL. The wait cycle can be calculated as follows: (65536 – xtaltime) x $T_{46.8\,K}$. $T_{46.8\,K}$ indicates the clock cycle of the 46.8 kHz clock.
[2]	-	reserved	Reserved. Reading this bit returns 0x0 and writing to this bit has no effect.
[1:0]	-	reserved	Reserved. Reading this field returns the written value and writing to this field has no effect.

SC_PLLCTRL

SC_PLLCTRL is a PLL control register. It is used to control whether to enable the on-chip ARMPLL through software or system mode switching. It also sets the stable time of the ARMPLL.

CAUTION

Write protection for this register can be enabled by configuring SC_LOCKEN. This register can be written only when write protection is disabled.

When the ARMPLL is enabled by switching the system mode (namely, by configuring SC_PLLCTRL[pllover]), the ARMPLL is disabled automatically if the system is not in normal mode.

The clock frequency of the APLL is controlled by PERI_CRG0 and PERI_CRG1. When the PLL frequency is changed, a stable clock can be output only after 0.5 ms. Therefore, the plltime of this register must meet this requirement.

Offset Address	Register Name	Total Reset Value
0x014	SC_PLLCTRL	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	reserved	plltime							reserved	reserved	pllover
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved. Reading this bit returns 0x0 and writing to this bit has no effect.
[27:3]	RW	plltime	Stable time of the ARMPLL. This time refers to the period from the start of the PLL to the output of a stable PLL clock. That is, the wait time of switching the system mode from PLL CTL to SW-to-PLL. The timeout is calculated as follows: 4 x (33554432 – plltime) x T_{XIN}. T_{XIN} indicates the clock cycle of the external crystal oscillator of the Hi3518.
[2]	-	reserved	Reserved. Reading this bit returns 0x0 and writing to this bit has no effect.
[1]	-	reserved	Reserved.

Offset Address	Register Name	Total Reset Value
0x014	SC_PLLCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				plltime																								reserved		reserved	pllover
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	pllover	Whether the ARMPLL is enabled is controlled by the software rather than system mode switching. **This bit must be set to 0.** 0: The ARMPLL is enabled by switching the system mode. 1: reserved

PERIPHCTRL0

PERIPHCTRL0 is peripheral control register 0.

CAUTION

Write protection for this register can be enabled by configuring SC_LOCKEN. This register can be written only when write protection is disabled.

Offset Address	Register Name	Total Reset Value
0x01C	PERIPHCTRL0	0x0022_1000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	commtx_rx_en	reserved							arm_tcm_gate_en	arm_mem_adjust							reserved	global_software_int	reserved	ddrc0_apb_gt_en	reserved											
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:23]	-	reserved	Reserved.

[22]	RW	arm_tcm_gate_en	ARM TCM dynamic clock gating enable. 0: disabled 1: enabled
[21:16]	RW	arm_mem_adjust	ARM9 memory adjustment.
[15]	-	reserved	Reserved.
[14]	RW	global_software_int	Global software interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[13]	-	reserved	Reserved.
[12]	RW	ddrc_apb_gt_en	DDRC APB clock gating. 0: disabled 1: enabled
[11:0]	-	reserved	Reserved.

PERIPHCTRL1

PERIPHCTRL1 is a software interrupt configuration register.

Offset Address	Register Name	Total Reset Value
0x0020	PERIPHCTRL1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								software_int
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	software_int	Software interrupts. 0: No interrupt is generated. 1: An interrupt is generated.

PERIPHCTRL3

PERIPHCTRL3 is peripheral control register 3 (MDDRC out-of-order configuration register outtodr_ctrl).

Offset Address	Register Name	Total Reset Value
0x0038	PERIPHCTRL3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												reserved		sys_axi		reserved								mdu_ddrt_ctrl	jpge_ctrl	tde_ctrl	vpss_ctrl	venc_ctrl	reserved	vicap_ctrl	vou_ctrl
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved.
[19:18]	RO	reserved	Reserved.
[17]	RW	ive_ctrl	Indicates whether out-of-order is allowed when the IVE subsystem accesses DDR. 0: Out-of-order is not allowed. 1: Out-of-order is allowed.
[16:8]	RO	reserved	Reserved.
[7]	RW	mdu_ddrt_ctrl	Indicates whether out-of-order is allowed when MDU or DDRT accesses DDR. 0: Out-of-order is not allowed. 1: Out-of-order is allowed.
[6]	RW	jpge_ctrl	Indicates whether out-of-order is allowed when JPGE accesses DDR. 0: Out-of-order is not allowed. 1: Out-of-order is allowed.
[5]	RW	tde_ctrl	Indicates whether out-of-order is allowed when TDE accesses DDR. 0: Out-of-order is not allowed. 1: Out-of-order is allowed.
[4]	RW	vpss_ctrl	Indicates whether out-of-order is allowed when VPSS accesses DDR. 0: Out-of-order is not allowed. 1: Out-of-order is allowed.
[3]	RW	venc_ctrl	Indicates whether out-of-order is allowed when VENC accesses DDR. 0: Out-of-order is not allowed. 1: Out-of-order is allowed.
[2]	RO	reserved	Reserved.

[1]	RW	vicap_ctrl	Indicates whether out-of-order is allowed when the VICAP accesses DDR. 0: Out-of-order is not allowed. 1: Out-of-order is allowed.
[0]	RW	vou_ctrl	Indicates whether out-of-order is allowed when the VOU accesses DDR. 0: Out-of-order is not allowed. 1: Out-of-order is allowed.

PERIPHCTRL4

PERIPHCTRL4 is peripheral control register 4.

Offset Address	Register Name	Total Reset Value
0x003C	PERIPHCTRL4	0x0000_01E0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																cbar_en	mdu_ddrt_sel	reserved						vdac_ctrl_sl	vdac_ctrl_slc	vdac_ctrl_slcd	vdac_ctrl_s	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	-	reserved	Reserved.
[16]	RW	cbar_en	cbar_en output enable. 0: disabled 1: enabled
[15]	RW	mdu_ddrt_sel	Motion detection unit (MDU) and DDR test (DDRT) function select. 0: Only the MDU is enabled. 1: Only the DDRT is enabled.
[14:9]	RO	reserved	Reserved.
[13:12]	RW	ssp_cs_sel	SSP CS select. 00: CS 0 01: CS 1 10: CS 2 11: CS 3

[8]	RW	vdac_ctrl_sl	Power-off control for the VDAC module. 0: not powered off 1: powered off
[7]	RW	vdac_ctrl_slc	Power-off control for the VDAC channel. 0: not powered off 1: powered off
[6]	RW	vdac_ctrl_slcd	Power-off control for the VDAC detection circuit. 0: not powered off 1: powered off
[5:4]	RW	vdac_ctrl_s	VDAC parameter configuration.
[3]	RO	reserved	Reserved.
[2]	RW	sdio_det_mode	Signal detection mode of the SDIO card. 0: active low 1: active high
[1]	RW	uart1_rts_ctrl	UART1 RTS output control. 0: normal output 1: reverse output
[0]	RO	reserved	Reserved.

PERIPHCTRL5

PERIPHCTRL5 is peripheral control register 5 (media bus timeout control register 1 for master port l).

Offset Address	Register Name	Total Reset Value
0x0040	PERIPHCTRL5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	count_en_media0_port1	over_value_media0_port1															count_en_media0_port0	over_value_media0_port0														

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	count_en_media0_port1	Timeout count enable for the VPPSS port. 0: disabled 1: enabled
[30:16]	RW	over_value_media0_port1	Timeout count value of the VPSS port. Count value = over_value_media0_port1 x 2
[15]	RW	count_en_media0_port0	Timeout count enable for the VENC port. 0: disabled 1: enabled
[14:0]	RW	over_value_media0_port0	Timeout count value of the VENC port. Count value = over_value_media0_port0 x 2

SC_LOCKEN

SC_LOCKEN is a register for locking key system control registers.

Offset Address	Register Name	Total Reset Value
0x0044	SC_LOCKEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	scper_lockl																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	scper_lockl	Register for locking key system control registers. The key registers include SC_CTRL, SYSSTAT, and SC_PLLCTRL. When 0x1ACC_E551 is written to SC_LOCKEN, the write permission for all registers is enabled; when any other value is written to SC_LOCKEN, the write permission is disabled. Reading this register returns the lock status rather than its written value. 0x0000_0000: The write permission is enabled (unlocked). 0x0000_0001: The write permission is disabled (locked).

PERIPHCTRL6

PERIPHCTRL6 is peripheral control register 6 (media bus timeout control register 2 for master port l).

Offset Address	Register Name	Total Reset Value
0x0048	PERIPHCTRL6	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	count_en_media0_port3	over_value_media0_port3															count_en_media0_port2	over_value_media0_port2														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	count_en_media0_port3	Timeout count enable for the JPGE port. 0: disabled 1: enabled
[30:16]	RW	over_value_media0_port3	Timeout count value of the JPGE port. Count value = over_value_media0_port3 x 2
[15]	RW	count_en_media0_port2	Timeout count enable for the TDE port. 0: disabled 1: enabled
[14:0]	RW	over_value_media0_port2	Timeout count value of the TDE port. Count value = over_value_media0_port2 x 2

PERIPHCTRL7

PERIPHCTRL7 is peripheral control register 7 (media bus timeout control register 3 for master port l).

Offset Address	Register Name	Total Reset Value
0x004C	PERIPHCTRL7	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																count_en_media0_port4	over_value_media0_port4														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15]	RW	count_en_media0_port4	Timeout count enable for the MDU port. 0: disabled 1: enabled
[14:0]	RW	over_value_media0_port4	Timeout count value of the MDU port. Count value = over_value_media0_port4 x 2

PERIPHCTRL9

PERIPHCTRL9 is peripheral control register 9 (media bus priority configuration register for master port l).

Offset Address	Register Name	Total Reset Value
0x0054	PERIPHCTRL9	0x0001_2345

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												media0_port4_pri				reserved	media0_port3_pri			reserved	media0_port2_pri			reserved	media0_port1_pri			reserved	media0_port0_pri		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1	0	1	0	0	0	1	0	1

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved.

[18:16]	RW	media0_port4_pri	MDU priority. The value 7 indicates the highest priority.
[15]	RO	reserved	Reserved.
[14:12]	RW	media0_port3_pri	JPGE priority. The value 7 indicates the highest priority.
[11]	RO	reserved	Reserved.
[10:8]	RW	media0_port2_pri	TDE priority. The value 7 indicates the highest priority.
[7]	RO	reserved	Reserved.
[6:4]	RW	media0_port1_pri	VPSS priority. The value 7 indicates the highest priority.
[3]	RO	reserved	Reserved.
[2:0]	RW	media0_port0_pri	VENC priority. The value 7 indicates the highest priority.

PERIPHCTRL10

PERIPHCTRL10 is peripheral control register 10 (system bus timeout control register 1 for master port l).

Offset Address	Register Name	Total Reset Value
0x0058	PERIPHCTRL10	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	count_en_port1	over_value_port1															count_en_port0	over_value_port0														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	count_en_port1	Timeout count enable for ARMD port. 0: disabled 1: enabled
[30:16]	RW	over_value_port1	Timeout count value of ARMD port. Count value = over_value_port1 x 2

Offset Address	Register Name	Total Reset Value
0x0058	PERIPHCTRL10	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	count_en_port1	over_value_port1															count_en_port0	over_value_port0														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15]	RW	count_en_port0	Timeout count enable for the AHB bridge port 0: disabled 1: enabled
[14:0]	RW	over_value_port0	Timeout count value of the AHB bridge port. Count value = over_value_port0 x 2

PERIPHCTRL11

PERIPHCTRL11 is peripheral control register 11 (system bus timeout control register 2 for master port l).

Offset Address	Register Name	Total Reset Value
0x005C	PERIPHCTRL11	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	count_en_port3	over_value_port3															count_en_port2	over_value_port2														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	count_en_port3	Timeout count enable for the ARMI port. 0: disabled 1: enabled

[30:16]	RW	over_value_port3	Timeout count value of the ARMI port. Count value = over_value_port3 x 2
[15]	RW	count_en_port2	Timeout count enable for the IVE port. 0: disabled 1: enabled
[14:0]	RW	over_value_port2	Timeout count value of the IVE port. Count value = over_value_port2 x 2

PERIPHCTRL12

PERIPHCTRL12 is peripheral control register 12 (system bus priority configuration register for master port l).

Offset Address	Register Name	Total Reset Value
0x0060	PERIPHCTRL12	0x0000_1234

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																reserved	mst_pri3			reserved	mst_pri2			reserved	mst_pri1			reserved	mst_pri0		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1	0	1	0	0

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved.
[14:12]	RW	mst_pri3	ARMI priority. The value 4 indicates the highest priority.
[11]	RO	reserved	Reserved.
[10:8]	RW	mst_pri2	IVE priority. The value 4 indicates the highest priority.
[7]	RO	reserved	Reserved.
[6:4]	RW	mst_pri1	Priority of ARMD. The value 4 indicates the highest priority.
[3]	RO	reserved	Reserved.
[2:0]	RW	mst_pri0	Priority of AHB bridge. The value 4 indicates the highest priority.

PERIPHCTRL13

PERIPHCTRL13 is peripheral control register 13 (system bus priority configuration register for slave port l).

Offset Address	Register Name	Total Reset Value
0x0064	PERIPHCTRL13	0x0000_1234

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												slave_priority_s5				reserved	slave_priority_s4			reserved	slave_priority_s3			reserved	slave_priority_s2			reserved	slave_priority_s1		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1	0	1	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved.
[18:15]	RO	reserved	Reserved.
[14:12]	RW	slave_priority_s4	Priority for accessing the MDDRC bus over the SYS AXI s4 port. The value 4 indicates the highest priority.
[11]	-	reserved	Reserved.
[10:8]	RW	slave_priority_s3	Priority for accessing the APB_MEDIA bus over the SYS AXI s3 port. The value 4 indicates the highest priority.
[7]	-	reserved	Reserved.
[6:4]	RW	slave_priority_s2	Priority for accessing the APB_SYS bus over the SYS AXI s2 port. The value 4 indicates the highest priority.
[3]	-	reserved	Reserved.
[2:0]	RW	slave_priority_s1	Priority for accessing the AHB of the SYS AXI s1 port. The value 4 indicates the highest priority.

PERIPHCTRL14

PERIPHCTRL14 is peripheral control register 14 (audio CODEC control register 0).

Offset Address	Register Name	Total Reset Value
0x0068	PERIPHCTRL14	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pd_adcl	pd_adcr	pd_dacl	pd_dacr	pd_micbias	pd_vref	fatartup	ana_loop	mute_dacl	mute_dacr	popfreel	popfreer	mute_adcl	mute_adcr	mclk_ana_sel	dacclk_sel	lineinl_sel	gain_micl			gainboostl	clk_timing_sel	lineinr_sel	gain_micr					gainboostr	clk_delay_sel		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	pd_adcl	Power-down control for the analog-to-digital converter left (ADCL). 0: The digital and analog parts of the ADCL work normally. 1: The digital and analog parts of the ADCL are powered down.
[30]	RW	pd_adcr	Power-down control for the analog-to-digital converter right (ADCR). 0: The digital and analog parts of the ADCR work normally. 1: The digital and analog parts of the ADCR are powered down.
[29]	RW	pd_dacl	Power-down control for the digital-to-analog converter left (DACL). 0: The digital and analog parts of the DACL work normally. 1: The digital and analog parts of the DACL are powered down.
[28]	RW	pd_dacr	Power-down control for the digital-to-analog converter right (DACR). 0: The digital and analog parts of the DACR work normally. 1: The digital and analog parts of the DACR are powered down.
[27]	RW	pd_micbias	MICBIAS power-down control signal. 0: The MICBIAS works properly. 1: The MICBIAS is powered down.
[26]	RW	pd_vref	Reference voltage power-down control signal. 0: The reference voltage is normal. 1: The reference voltage is powered down.
[25]	RW	fstarup	Reference voltage fast power-on control signal. 0: The reference voltage is powered on normally. 1: The reference voltage is powered on quickly in 0.1s.
[24]	RW	ana_loop	Analog loop control signal. 0: normal mode 1: analog loop mode

[23]	RW	mute_dacl	Mute control for the DACL. 0: The DACL works normally. 1: The DACR is muted.
[22]	RW	mute_dacr	Mute control for the DACR. 0: The DACR works normally. 1: The DACR is muted.
[21]	RW	popfreel	Pop free control for the DACL. 0: The pop free function is disabled. 1: The pop free function is enabled. The pop free function is required only in ultra-low-power mode. In this case, the capacitor at the LINEOUT end of the DACL is charged until the voltage is AVDD/2.
[20]	RW	popfreer	Pop free control for the DACR. 0: The pop free function is disabled. 1: The pop free function is enabled. The pop free function is required only in ultra-low-power mode. In this case, the capacitor at the LINEOUT end of the DACR is charged until the voltage is AVDD/2.
[19]	RW	mute_micl	LINEIN mute control for the left channel. 0: The left channel of the LINEIN works normally. 1: The left channel of the LINEIN is muted.
[18]	RW	mute_micr	LINEIN mute control for the right channel. 0: The right channel of the LINEIN works normally. 1: The right channel of the LINEIN is muted.
[17]	RW	mclk_ana_sel	MCLK phase input select. 0: MCLK normal phase input 1: MCLK reverse phase input (180º reverse)
[16]	RW	dacclk_sel	CLK edge select. 0: The phases of the DAC CLK and input CLK are the same. 1: The phases of the DAC CLK and input CLK are in reverse.
[15]	RW	lineinl_sel	LINEINL input signal select. 0: LINEINL input 1: MICP_L input

[14:10]	RW	gain_micl	Gain control for the LINEINL input end. 0x00: –16.5 dB 0x01: –15 dB 0x02: –13.5 dB ... 0x0B: 0 dB 0x0C: 1.5 dB ... 0x1F: 30 dB
[9]	RW	gainboostl	LINEINL gain boost control. 0: 0 dB 1: 26 dB
[8]	RW	clk_timing_sel	ADC CLK timing select. 0: clock timing 1 1: clock timing 2
[7]	RW	lineinr_sel	LINEINR input signal select. 0: LINEINR input 1: MICP_R input
[6:2]	RW	gain_micr	Gain control for the LINEINL input end. 0x00: –16.5 dB 0x01: –15 dB 0x02: –13.5 dB ... 0x0B: 0 dB 0x0C: 1.5 dB ... 0x1F: 30 dB
[1]	RW	gainboostr	LINEINR gain boost control. 0: 0 dB 1: 26 dB
[0]	RW	clk_delay_sel	ADC CLK delay. 0: no delay 1: delay

PERIPHCTRL15

PERIPHCTRL15 is peripheral control register 15 (audio CODEC control register 1).

Offset Address	Register Name	Total Reset Value
0x006C	PERIPHCTRL15	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dacl_rst_n	dacr_rst_n	adcl_rst_n	adcr_rst_n	dacl_en	dacr_en	adcl_en	adcr_en	i2s1_data_bits		i2s2_data_bits		dig_bypass	dig_loop	i2s1_fs_sel		i2s2_fs_sel								ibadj_adc		ibadj_dac	ibadj_ctcm	adc_adatn		adc_flstn	rst
Reset	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	1	1	0	1	1	1	1	0	0	1	1	1	0	1	0	1

Bits	Access	Name	Description
[31]	RW	dacl_rst_n	DACL reset signal. 0: valid 1: invalid
[30]	RW	dacr_rst_n	DACR reset signal. 0: valid 1: invalid
[29]	RW	adcl_rst_n	ADCL reset signal. 0: valid 1: invalid
[28]	RW	adcr_rst_n	ADCR reset signal. 0: valid 1: invalid
[27]	RW	dacl_en	DACL enable signal. 0: disabled 1: enabled
[26]	RW	dacr_en	DACR enable signal. 0: disabled 1: enabled
[25]	RW	adcl_en	ADCL enable signal. 0: disabled 1: enabled
[24]	RW	adcr_en	ADCR enable signal. 0: disabled 1: enabled

[23:22]	RW	i2s1_data_bits	I^2S1 data interface width. 00: 16 bits 01: 18 bits 10: 20 bits. 11: 24 bits
[21:20]	RW	i2s2_data_bits	I^2S2 data interface width. 00: 16 bits 01: 18 bits 10: 20 bits. 11: 24 bits
[19]	RW	dig_bypass	Bypass bit of the digital part, used for analog test mode. 0: The digital part works properly. 1: The digital part bypasses.
[18]	RW	dig_loop	Digital loop control signal. 0: valid 1: invalid
[17:13]	RW	i2s1_fs_sel	I^2S1 sample rate select. 00000: 8 kHz, 16.896 MHz mclk 00001: 16 kHz, 16.896 MHz mclk 00010: 32 kHz, 16.896 MHz mclk 00011: 64 kHz, 16.896 MHz mclk 001xx: 128 kHz, 16.896 MHz mclk 01000: 11 kHz, 16.896 MHz mclk 01001: 22 kHz, 16.896 MHz mclk 01010: 44 kHz, 16.896 MHz mclk 01011: 88 kHz, 16.896 MHz mclk 011xx: 176 kHz, 16.896 MHz mclk 10000: 12 kHz, 16.896 MHz mclk 10001: 24 kHz, 16.896 MHz mclk 10010: 48 kHz, 16.896 MHz mclk 10011: 96 kHz, 16.896 MHz mclk 101xx: 192 kHz, 16.896 MHz mclk 11000: mclk/1024 11001: mclk/512 11010: mclk/256 11011: mclk/128 111xx: mclk/64

[12:8]	RW	i2s2_fs_sel	I²S2 sample rate select. 00000: 8 kHz, 16.896 MHz mclk 00001: 16 kHz, 16.896 MHz mclk 00010: 32 kHz, 16.896 MHz mclk 00011: 64 kHz, 16.896 MHz mclk 001xx: 128 kHz, 16.896 MHz mclk 01000: 11 kHz, 16.896 MHz mclk 01001: 22 kHz, 16.896 MHz mclk 01010: 44 kHz, 16.896 MHz mclk 01011: 88 kHz, 16.896 MHz mclk 011xx: 176 kHz, 16.896 MHz mclk 10000: 12 kHz, 16.896 MHz mclk 10001: 24 kHz, 16.896 MHz mclk 10010: 48 kHz, 16.896 MHz mclk 10011: 96 kHz, 16.896 MHz mclk 101xx: 192 kHz, 16.896 MHz mclk 11000: mclk/1024 11001: mclk/512 11010: mclk/256 11011: mclk/128 111xx: mclk/64
[7:6]	RW	ibadj_adc	Bias current control signal of the ADC. 00: 3 μA 01: 5 μA (recommended) 10: 7 μA 11: 9 μA
[5]	RW	ibadj_dac	Bias current control signal of the DAC. 0: 5 μA (recommended) 1: 9 μA
[4]	WO	ibadj_ctcm	Bias current control signal of CTCM, MICBIAS, and LINEIN. 0: 5 μA (recommended) 1: 10 μA
[3:2]	RW	adc_adatn	ADC_DAC VB control. 00: R = 90% 01: R = 95% 10: R = 100% 11: R = 110%
[1]	RW	adc_flstn	Flash VREF control. 0: 0.99–2.31 V, LSB = 182 mV 1: 1.1–2.2 V, LSB = 161 mV

[0]	RW	rst	rst signal of the analog part. 0: normal mode 1: rst

PERIPHCTRL16

PERIPHCTRL16 is peripheral control register 16 (audio CODEC control register 2).

Offset Address	Register Name	Total Reset Value
0x0070	PERIPHCTRL16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	smutel	smuter	sunmutel	sunmuter	dacvu	mutel_rate		muter_rate		dacl_deemph		dacr_deemph	reserved																dacl_i2ssel	dacl_lrsel	dacr_i2ssel	dacr_lrsel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31]	RW	smutel	Soft mute control bit of the DACL. 0: Soft mute is disabled. 1: Soft mute is enabled.
[30]	RW	smuter	Soft mute control bit of the DACR. 0: Soft mute is disabled. 1: Soft mute is enabled.
[29]	RW	sunmutel	Soft unmute control bit of DACL. 0: Soft unmute is disabled. 1: Soft unmute is enabled.
[28]	RW	sunmuter	Soft unmute control bit of the DACR. 0: Soft unmute is disabled. 1: Soft unmute is enabled.
[27]	RW	dacvu	Volume update control bit of the DAC. 0: The volume is not updated. 1: The volume is updated.
[26:25]	RW	mutel_rate	Soft mute rate control bit of the DACL. 00: fs/2 01: fs/8 10: fs/32 11: fs/64

[24:23]	RW	muter_rate	Soft mute rate control bit of the DACR. 00: fs/2 01: fs/8 10: fs/32 11: fs/64
[22:21]	RW	dacl_deemph	De-emphasis control signal of the DACL. 00: none 01: 32 kHz 10: 44 kHz 11: 48 kHz
[20:19]	RW	dacr_deemph	De-emphasis control signal of the DACR. 00: none 01: 32 kHz 10: 44 kHz 11: 48 kHz
[18:4]	RW	reserved	Reserved.
[3]	RW	dacl_i2ssel	I^2S interface select. 0: I^2S1 1: I^2S2
[2]	RW	dacl_lrsel	Left and right channel data select of the DACL. 0: left channel 1: right channel
[1]	RW	dacr_i2ssel	I^2S interface select of the DACR. 0: I^2S1 1: I^2S2
[0]	RW	dacr_lrsel	Left and right channel data select of the DACR. 0: left channel 1: right channel

PERIPHCTRL17

PERIPHCTRL17 is peripheral control register 17 (audio CODEC control register 3).

Offset Address	Register Name	Total Reset Value
0x0074	PERIPHCTRL17	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dacl_mute	dacl_vol							dacr_mute	dacr_vol							dacr2dacl_en	dacr2dacl_vol							dacl2dacr_en	dacl2dacr_vol						
Reset	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0	0

Bits	Access	Name	Description
[31]	RW	dacl_mute	Mute control for the DACL. 0: normal mode 1: mute
[30:24]	RW	dacl_vol	Volume control for the DACL. 0x00: 6 dB 0x01: 5 dB 0x02: 4 dB ... 0x7E: –120 dB 0x7F: mute
[23]	RW	dacr_mute	Mute control for the DACR. 0: normal mode 1: mute
[22:16]	RW	dacr_vol	Volume control for the DACR. 0x00: 6 dB 0x01: 5 dB 0x02: 4 dB ... 0x7E: –120 dB 0x7F: mute
[15]	RW	dacr2dacl_en	Mixer control signal of dacr2dacl. 0: disabled 1: enabled

[14:8]	RW	dacr2dacl_vol	Volume control bit of dacr to dacl. 00: 36 dB 01: 35 dB 02: 34 dB ... 7E: –90 dB 7F: –91 dB
[7]	RW	dacl2dacr_en	Mixer control signal of dacl2dacr. 0: disabled 1: enabled
[6:0]	RW	dacl2dacr_vol	Volume control bit of dacl to dacr. 00: 36 dB 01: 35 dB 02: 34 dB ... 7E: –90 dB 7F: –91 dB

PERIPHCTRL18

PERIPHCTRL18 is peripheral control register 18 (audio CODEC control register 4).

Offset Address	Register Name	Total Reset Value
0x0078	PERIPHCTRL18	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	adcl_mute	adcl_vol							adcr_mute	adcr_vol							adcl_hpf_en	adcr_hpf_en	reserved										adcl_i2ssel	adcl_lrsel	adcr_i2ssel	adcr_lrsel	
Reset	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31]	RW	adcl_mute	Mute control bit of the ADCL. 0: The ADCL is unmuted. 1: The ADCL is muted.

[30:24]	RW	adcl_vol	Volume control for the ADCL. 00: 30 dB 01: 29 dB 02: 28 dB ... 7E: –96 dB 7F: –97 dB
[23]	RW	adcr_mute	Mute control bit of the ADCR. 0: The ADCR is unmuted. 1: The ADCR is muted.
[22:16]	RW	adcr_vol	Volume control for the ADCR. 00: 30 dB 01: 29 dB 02: 28 dB ... 7E: –96 dB 7F: –97 dB
[15]	RW	adcl_hpf_en	High-pass filter enable control for the ADCL. 0: disabled 1: enabled
[14]	RW	adcr_hpf_en	High-pass filter enable control for the ADCR. 0: disabled 1: enabled
[13:4]	RW	reserved	Reserved.
[3]	RW	adcl_i2ssel	I^2S interface select of the ADC (high priority). 0: I^2S1 1: I^2S2
[2]	RW	adcl_lrsel	Left and right channel data select of the DACL. 0: left channel 1: right channel
[1]	RW	adcr_i2ssel	I^2S interface select of the ADCR (low priority). 0: I^2S1 1: I^2S2
[0]	RW	adcr_lrsel	Left and right channel data select of the DACR. 0: left channel 1: right channel

PERIPHCTRL19

PERIPHCTRL19 is peripheral control register 19 (audio CODEC control register 5).

Offset Address	Register Name	Total Reset Value
0x007C	PERIPHCTRL19	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	adcl2dacl_en				adcl2dacl_vol				adcr2dacl_en				adcr2dacl_vol				adcl2dacr_en				adcl2dacr_vol				adcr2dacr_en				adcr2dacr_vol			
Reset	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0	0

Bits	Access	Name	Description
[31]	RW	adcl2dacl_en	Mixer control signal of adcl2dacl. 0: disabled 1: enabled
[30:24]	RW	adcl2dacl_vol	Volume control bit of dacl to dacl. 00: 36 dB 01: 35 dB 02: 34 dB ... 7E: –90 dB 7F: –91 dB
[23]	RW	adcr2dacl_en	Mixer control signal of adcr2dacl. 0: disabled 1: enabled
[22:16]	RW	adcr2dacl_vol	Volume control bit of dacr to dacl. 00: 36 dB 01: 35 dB 02: 34 dB ... 7E: –90 dB 7F: –91 dB
[15]	RW	adcl2dacr_en	Mixer control signal of adcl2dacr. 0: disabled 1: enabled

[14:8]	RW	adcl2dacr_vol	Volume control bit of dacl to dacr. 00: 36 dB 01: 35 dB 02: 34 dB ... 7E: –90 dB 7F: –91 dB
[7]	RW	adcr2dacr_en	Mixer control signal of adcr2dacr. 0: disabled 1: enabled
[6:0]	RW	adcr2dacr_vol	Volume control bit of dacr to dacr. 00: 36 dB 01: 35 dB 02: 34 dB ... 7E: –90 dB 7F: –91 dB

PERIPHCTRL20

PERIPHCTRL20 is a USB control register 1 (peripheral control register 20).

Offset Address	Register Name	Total Reset Value
0x0080	PERIPHCTRL20	0x0003_33A8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														usbovr_p_ctrl	usbpwr_p_ctrl	reserved	phy0_ovrcur_en	reserved	phy0_pwr_en	reserved		ss_ena_incr16_i	ss_ena_incr8_i	ss_ena_incr4_i	ss_ena_incrx_align_i	ss_autoppd_on_overcur_en_i	reserved		ulpi_bypass_en	app_start_clk_i	ohci_susp_lgcy_i	wordinterface
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0	1	1	1	0	1	0	1	0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved.
[17]	RW	usbovr_p_ctrl	Polarity for over-current protection. 0: active low 1: active high

[16]	RW	usbpwr_p_ctrl	Polarity for power enable. 0: active low 1: active high
[15]	RO	reserved	Reserved.
[14]	RW	phy0_ovrcur_en	Over-current protection enable for PHY0. 0: disabled 1: enabled
[13]	RO	reserved	Reserved.
[12]	RW	phy0_pwr_en	Power-off control for the PHY0 power supply. 0: powered off 1: enable the power output of the controller
[11:10]	RO	reserved	Reserved.
[9]	RW	ss_ena_incr16_i	AHB burst16 enable. 0: disabled 1: enabled
[8]	RW	ss_ena_incr8_i	AHB burst8 enable. 0: disabled 1: enabled
[7]	RW	ss_ena_incr4_i	AHB burst4 enable. 0: disabled 1: enabled
[6]	RW	ss_ena_incrx_align_i	Burst alignment enable. 0: disabled 1: enabled
[5]	RW	ss_autoppd_on_overcur_en_i	Port automatic power-off enable during overcurrent. 0: disabled 1: enabled
[4]	RO	reserved	Reserved (ULPI mode16_en).
[3]	RW	ulpi_bypass_en	ULPI bypass control. **This bit must be set to 1**. 0: ULPI mode 1: UTMI mode
[2]	RW	app_start_clk_i	Open host controller interface (OHCI) clock control. 0: The OHCI works properly. 1: The OHCI clock is enabled in suspend mode.
[1]	RW	ohci_susp_lgcy_i	Strap input signal when the OHCI is suspended.

[0]	RW	wordinterface	Data bit width select of the UTMI interface. 0: 8 bits 1: 16 bits

PERIPHCTRL21

PERIPHCTRL21 is USB control register 2 (peripheral control register 21).

Offset Address	Register Name	Total Reset Value
0x0084	PERIPHCTRL21	0x001D_2188

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								siddq	commononn	phy0_txhsxvtune		phy0_sleepm	phy0_loopbackenb			phy0_compdistune				phy0_sqrxtune				phy0_txfslstune				phy0_txpreemphasistune		reserved		phy0_txrisetune		phy0_txverftune			
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	0	1	0	0	0	0	1	1	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31:23]	-	reserved	Reserved.
[22]	RW	siddq	Analog power-off test enable of the PHY. 0: do not power off the analog power 1: power off the analog power The default value is 0. The bit must be set to 0 before the built-in self test (BIST).
[21]	RW	commononn	Indicates whether XO BIAS BANDGAP PLL works when the PHY is suspended. 0: clk48m_ohci output is always valid even when the PHY is suspended. 1: clk48m_ohci output is valid except when the PHY is suspended.
[20:19]	RW	phy0_txhsxvtune	Crossover voltage tune signal of DP/DM. 00: reserved 01: –15 mV 10: +15 mV 11: default

[18]	RW	phy0_sleepm	Sleep mode of port 0. 0: sleep mode 1: normal mode
[17]	RW	phy0_loopbackenb	Loopback (from D+ to D-) test enable signal of PHY0. This bit must be set to 0.
[16:14]	RW	phy0_compdistune	HOSDISCONNECT threshold level tune signal of PHY0. 000: –6% 001: –4.5% 010: –3% 100: default value 101: +1.5% 110: +3% 111: +4.5% Other values: reserved
[13:11]	RW	phy0_sqrxtune	Squelch circuit tune signal of PHY0. 000: +20% 001: +15% 010: +10% 011: +5% 100: default value 101: –5% 110: –10% 111: –15%
[10:7]	RW	phy0_txfslstune	FS LS impedance tune signal of PHY0. 0x0: +5% 0x1: +2.5% 0x3: default value 0x7: –2.5% 0xF: –5% Other values: reserved
[6]	RW	phy0_txpreemphasistune	Pre-emphasis transmit enable signal of PHY0 in HS mode. The default value is 0. 0: disabled 1: enabled
[5]	RW	reserved	Reserved.
[4]	RW	phy0_txrisetune	High-speed signal up/down time tune of PHY0. 0: default value 1: –8%

[3:0]	RW	phy0_txverftune	DC level tune signal in HS mode of PHY0. 0x0: –10% 0x1: –8.75% 0x2: –7.5% 0x3: –6.25% 0x4: –5% 0x5: –3.75% 0x6: –2.5% 0x7: –1.25% 0x8: default value 0x9: +1.25% 0xA: +2.5% 0xB: +3.7% 0xC: +5% 0xD: +6.25% 0xE: +7.5% 0xF: +8.75%

SYSSTAT

SYSSTAT is a system status register (PLL_LOCK).

Offset Address	Register Name	Total Reset Value
0x008C	SYSSTAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													arm_standbywfi	reserved	sfc_addr_mode	reserved	nf_ecc_type			nf_block_size	nf_addr_num	nf_page_size		reserved		boot_mode	reserved				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved.
[18]	RO	arm_standbywfi	Whether the ARM processor is in wait for interrupt (WFI) status. 0: non-WFI status 1: WFI status
[17]	RO	reserved	Reserved.

[16]	RO	sfc_addr_mode	Default address mode of the SFC. 0: 3-byte address mode 1: 4-byte address mode
[15]	RO	reserved	Reserved.
[14:12]	RO	nf_ecc_type	ECC mode of the NAND flash during booting. 000: non-ECC mode 001: 1-bit mode 010: 4-byte mode 011: 8-byte mode 100: 24-bit mode Other values: reserved
[11]	RO	nf_block_size	Block size of the NAND flash during booting. 0: 64 pages for the SLC component 1: 128 pages for the MLC component
[10]	RO	nf_addr_num	Number of addresses sent to the NAND flash. 0: four addresses 1: five addresses
[9:8]	RO	nf_page_size	Page size of the NAND flash during booting. 00: 512 bytes 01: 2 KB 10: 4 KB 11: 8 KB
[7:6]	RO	jtag_sel	Selected debugging mode of the chip. 00: debug ARM 01: reserved 10: debug SATA PHY 11: reserved
[5]	RO	boot_mode	Selected boot mode of the chip. 0: boot from the SPI flash 1: boot from the NAND flash
[4:0]	RO	reserved	Reserved.

SCSYSID0

SCSYSID0 is chip ID register 0.

Offset Address	Register Name	Total Reset Value
0xEE0	SCSYSID0	0x00

Bit	7	6	5	4	3	2	1	0
Name	sysid0							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	sysid0	Reading this register returns 0x00.

SCSYSID1

SCSYSID1 is chip ID register 1.

Offset Address	Register Name	Total Reset Value
0xEE4	SCSYSID1	0x01

Bit	7	6	5	4	3	2	1	0
Name	sysid1							
Reset	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[7:0]	RO	sysid1	Reading this register returns 0x01.

SCSYSID2

SCSYSID2 is chip ID register 2.

Offset Address	Register Name	Total Reset Value
0xEE8	SCSYSID2	0x18

Bit	7	6	5	4	3	2	1	0
Name	sysid2							
Reset	0	0	0	1	1	0	0	0

Bits	Access	Name	Description
[7:0]	RO	sysid2	Reading this register returns 0x18.

SCSYSID3

SCSYSID3 is chip ID register 3.

Offset Address	Register Name	Total Reset Value
0xEEC	SCSYSID3	0x35

Bit	7	6	5	4	3	2	1	0
Name	sysid3							
Reset	0	0	1	1	0	1	0	1

Bits	Access	Name	Description
[7:0]	RO	sysid3	Reading this register returns 0x35.

3.5 DMA Controller

3.5.1 Overview

DMA refers to an operating mode in which data is transferred by the hardware by means of input/output (I/O) exchange. In this mode, the DMAC directly transfers data between a memory and a peripheral, between peripherals, and between memories. This avoids the processor intervention and reduces the interrupt processing overhead of the processor. The DMA mode is used to transmit data blocks at high speed. After receiving a DMA request, the DMAC enables the master bus controller through the channel configured by the CPU and transmits the address and control signals to the memory and peripherals. The DMAC also counts the transmitted data and reports the status (that is, whether the data transfer is complete or an error occurs in the data transfer) of data transfer to the CPU as an interrupt.

3.5.2 Features

The DMAC has the following features:

- Transfers data in 8-bit, 16-bit, or 32-bit mode.
- Provides four DMA channels. Each channel can be configured to support unidirectional transfer.
- Provides eight fixed DMA channel priorities. DMA channel 0 has the highest priority; whereas channel 3 has the lowest priority. When the DMA requests from two peripherals are valid simultaneously, the channel with the higher priority starts data transfer first.
- Provides one 4x32-bit FIFO in each of DMAC channels 0 and 1 and one 16 x 32-bit FIFO in each of DMAC channels 2 and 3.
- Provides two 32-bit master bus interfaces for data transfer.
- Supports two types of DMA requests: single transfer request and burst transfer request.
- Provides 16 groups of DMA request inputs. These requests can be configured as source requests or destination requests.
- Supports the DMA requests controlled through software.
- Programs the DMA burst size.
- Configures the source address and the destination address as automatic incremental or decremental addresses during DMA transfer.
- Supports four data transfer directions:

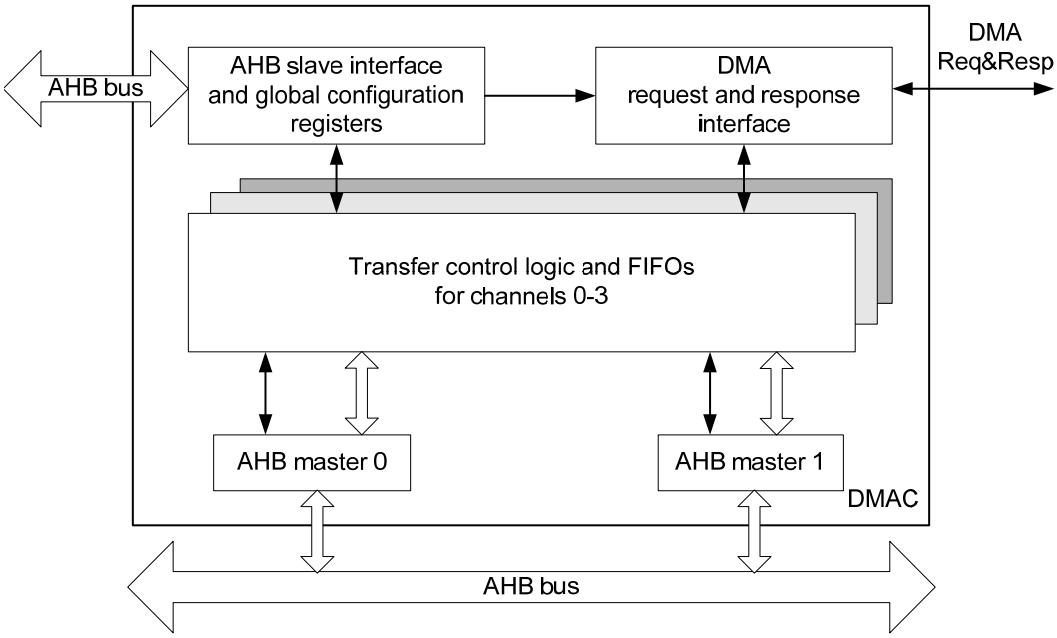
  - Memory to peripheral
  - Memory to memory
  - Peripheral to memory
  - Peripheral to peripheral
- Supports DMA transfer with the linked list.
- Supports the DMAC flow control.
- Provides a maskable interrupt output and supports the query of the statuses of the raw/masked DMA error interrupt and DMA terminal count interrupt and the status of the combination of the two interrupts.
- Controls the power consumption by disabling the DMAC and supports DMAC clock gating.

3.5.3 Function Description

Functional Block Diagram

Figure 3-5 shows the functional block diagram of the DMAC.

Figure 3-5 Functional block diagram of the DMAC



Each DMAC channel involves a group of transfer control logic and one FIFO. This group of transfer control logic perform the following operations automatically:

Step 1 Read data from the source address specified by the software.

Step 2 Buffer the data to the FIFO.

Step 3 Fetch data from the FIFO.

Step 4 Write the data to the destination address specified by the software.

----End

Workflow

The workflow of the DMAC is as follows:

Step 1 The software selects one DMAC channel for DMA transfer, configures the following items, and enables the channel:

- Source address
- Destination address
- Head pointer of the linked list
- Amount of the transferred data
- Number of source and destination peripheral request signals
- Masters used at the source and destination ends of the channel.

After the channel is enabled, the DMAC starts to check the activities of the DMA request signals from the source peripheral and destination device connected to this channel.

Step 2 The source device transmits a DMA request to the DMAC. If the source device is a memory, the DMAC considers that the DMA request is always valid by default.

Step 3 The DMAC channel responds to the DMA request of the source device. Then, the DMAC reads data from the source device and stores it in the internal FIFO of the channel.

Step 4 The destination device transmits a DMA request to the DMAC. If the destination device is a memory, the DMAC considers that the DMA request is always valid by default.

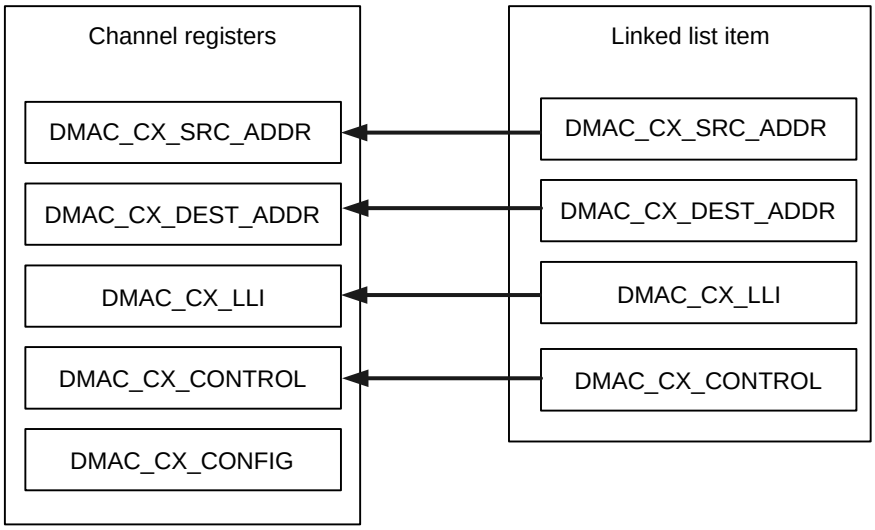
Step 5 The DMAC channel responds to the DMA request of the destination device. Then, the DMAC fetches data from the internal FIFO of the channel and writes it to the destination device.

Step 6 The steps Step 2 and Step 3 and steps Step 4 and Step 5 may be performed concurrently, because the source and destination devices may transmit DMA requests to the DMAC at the same time. When the FIFO overrun or underrun occurs on the DMA channel, the DMAC blocks the DMA requests of the source device or destination device until the FIFO is full or empty. When the DMAC interacts with the source device and destination device for several times, Step 2 to Step 5 are performed repeatedly until the specified data is transferred and a maskable terminal count interrupt is sent. If the value of DMAC_CnLLI is not 0, read linked list item (LLI) nodes by considering the register value as an address, load the obtained values to DMAC_Cn_SRC_ADDR, DMAC_Cn_DEST_ADDR, DMAC_CnLLI, and DMAC_Cn_CONTROL in sequence (see Figure 3-6), and go to Step 2. If the value of DMAC_CnLLI is 0, the current DMA transfer is stopped. In this case, the channel is disabled automatically and the transfer ends.

----End

Figure 3-6 shows how to update channel registers by using LLIs.

Figure 3-6 Updating channel registers by using the LLIs



Connections Between the DMAC and Peripherals

The peripherals initiate data transfer by transmitting DMA request signals to the DMAC.

The DMAC provides two types of DMA request signals for each peripheral:

- DMACBREQ

  Burst transfer request signal. It triggers a burst transfer and the burst size is preset.
- DMACSREQ

  Single transfer request signal. It triggers a single transfer. That is, the DMAC reads a data segment from a peripheral or writes a data segment to a peripheral.

The DMAC also provides a request clear signal DMACLR.

This signal is sent to each peripheral by the DMAC and is used to respond to the DMA request signal of each peripheral.

DMAC Request Signals

Table 3-24 describes the DMAC hardware request signals and corresponding peripheral requests.

Table 3-24 DMAC hardware request signals and corresponding peripheral requests

DMAC Hardware Request Signal No.	Peripheral Request
0	SIO receive (RX) channel
1	SIO transmit (TX) channel
2	Reserved
3	Reserved
4	Reserved

DMAC Hardware Request Signal No.	Peripheral Request
5	Reserved
6	DMA request of the UART0 RX channel
7	DMA request of the UART0 TX channel
8	DMA request of the UART1 RX channel
9	DMA request of the UART1 TX channel
10	DMA request of the UART2 RX channel
11	DMA request of the UART2 TX channel
12	DMA request of the SSP1 RX channel (reserved for the Hi3518C)
13	DMA request of the SSP1 TX (reserved for the Hi3518C)
14	DMA request of the SSP0 RX (reserved for the Hi3518C)
15	DMA request of the SSP0 TX (reserved for the Hi3518C)

The source and destination requests of each DMA channel are configured by using the software. For example, DMA request 0 is the request of the receive channel of SIO. To transmit the received data of SIO using channel 3, you must configure DMA request 0 as the source request of channel 3.

As memories do not provide DMA request signals, when a memory is used for DMA transfer, the DMAC considers that the DMA request of the memory is always valid by default. In addition, an idle cycle is inserted after each bus operation during the DMAC transfer on channel 2 or channel 3. In this way, the Master with a higher priority channel can transfer data on the bus first. Therefore, to avoid other channels waiting for the bus for a long time, it is recommended to transmit data from memory to memory using channel 2 or channel 3.

3.5.4 Operating Mode

Clock Gating

In the following cases, the DMAC and DMAC clock can be disabled using the software to reduce power consumption:

- All DMAC channels are idle and there is no DMA transfer request.
- DMAC_Cn_CONFIG [e] is set to 0 and DMAC channels are disabled.

To disable the DMAC clock, perform the following steps:

Step 1 Write 0 to DMAC_Cn_CONFIG[e] to disable DMAC channels.

Step 2 Write 0 to DMAC_CONFIG[e] to disable the DMAC.

Step 3 Write 0 to PERI_CRG56[dma_cken] to disable the bus clock gating function of the DMAC and disable the DMAC clock.

Enable the clock and the DMAC again when the DMAC is required for data transfer.

----End

Initializing the DMAC

To initialize the DMAC, perform the following steps:

Step 1 Write to DMAC_CONFIG to set the endian mode of DMAC master 1 and DMAC master 2, and write 1 to DMAC_CONFIG[e] to enable the DMAC.

Step 2 Write 1 to all the bits of DMAC_INT_ERR_CLR and DMAC_INT_TC_CLR to clear all interrupt statuses.

Step 3 Write 0 to the corresponding bits of DMAC_SYNC to set the DMA request signal groups to be synchronized.

Step 4 Configure and disable each channel in sequence. You can disable all the channels by writing 0 to DMAC_Cn_CONFIG[e] of each channel.

----End

Enabling a Channel

After the DMAC is initialized, the DMAC can transfer data only when a DMAC channel is configured and enabled. To enable a DMA channel, perform the following steps:

Step 1 Read DMAC_ENBLD_CHNS to search for free channels and select one.

Step 2 Write 1 to the corresponding bits of DMAC_INT_ERR_CLR and DMAC_INT_TC_CLR to clear the interrupt status of the selected channel.

Step 3 Configure and enable the selected channel as follows:

1. Write to DMAC_Cn_SRC_ADDR to set the access start address of the source device.
2. Write to DMAC_Cn_DEST_ADDR to set the access start address of the destination device.
3. For single-block data transfer, write 0 to DMAC_CnLLI.
4. For LLI data transfer, configure DMAC_CnLLI as the LLI header pointer.
5. Write to DMAC_Cn_CONTROL to set the master, data width, burst size, address increment, and transfer size of the source device and destination device.
6. Write to DMAC_Cn_CONFIG to set the DMA request signal, flow control mode, and interrupt mask of this channel. At this time, write 0 to DMAC_CX_CONFIG[e]. Then this channel is not enabled currently.
7. Write to DMAC_Cn_CONFIG to enable this channel. **Note:** Set the Channel Enable bit to 1 and keep other bits unchanged.

----End

Usage of DMAC_Cn_CONTROL

This register contains the control information about the DMA channels, such as the transfer size, burst size, and transfer bit width.

Before a channel is enabled, its corresponding register must be programmed using software. After the channel is enabled, the value of the register is updated when being loaded from the LLI node after a complete data block is transferred.

When a channel is active, no valid information is obtained when this register is read. This is because that after software obtains the register value, the value changes during data transfer. After the channel stops data transfer, the register can be read.

Table 3-25 describes the mapping between the value of DBSize or SBSize of DMAC_Cn_CONTROL and burst length.

Table 3-25 Mapping between the value of DBSize or SBSize and burst length

DBSize or SBSize	Burst Length
000	1
001	4
010	8
011	16
100	32
101	64
110	128
111	256

Table 3-26 describes the value of DWidth or SWidth of DMAC_Cn_CONTROL and transfer data width.

Table 3-26 Mapping between the value of DWidth or SWidth and transfer bit width

SWidth or DWidth	Transfer Bit Width
000	Byte (8 bits)
001	Half word (16 bits)
010	Word (32 bits)
011	Reserved
100	Reserved
101	Reserved
110	Reserved
111	Reserved

Note the following points when configuring DMAC_Cn_CONTROL:

- When the transfer bit width of the source device is smaller than that of the destination device, the product of the transfer bit width and transfer size of the source device must be an integral multiple of the transfer bit width of the destination device. Otherwise, data retention and data loss occur in the FIFO.
- SWidth and DWidth fields cannot be set to undefined bit widths.
- If the transfer size field is set to 0 and the DMAC is a flow controller, the DMAC does not transfer data. In this case, the programmer needs to disable the DMA channel and reprogram it.
- Do not perform common write/read tests on the DMAC_Cn_CONTROL register, because the transfer size field is different from the common register field whose written value and read value may be the same. During writes, this field serves as a control register, because it determines the number of data segments transferred by the DMAC. During reads, this field serves as a status register, because it returns the number (in the unit of the bit width of the source device) of the remaining data segments to be transferred.
- When the transfer size field is set to a value greater than the depth of the FIFO (peripheral FIFO rather than the DMAC FIFO) of the source device or destination device, the mode of DMAC source address or destination address must be set to non-incremental mode. Otherwise, the peripheral FIFO may overflow.

The bus access information is provided for the source device or destination device over the master interface signals during data transfer. Such information is related to the bits DMAC_Cn_CONTROL[prot] and DMAC_Cn_CONFIG[Lock] set by programming channel registers. Table 3-27 describes the three protection bits of the prot field of DMAC_Cn_CONTROL.

Table 3-27 Definitions of the prot field of DMAC_Cn_CONTROL

Bits	Description	Purpose
[2]	Cacheable or noncacheable	Indicates whether the access is cacheable. 0: noncacheable 1: cacheable For example, this bit can notify an advanced microcontroller bus architecture (AMBA) bridge of the following information: When finding the first burst read operation with eight digits, this bridge can initiate one 8-digit burst read operation on the destination bus directly without transmitting the read operations on the source bus to the destination bus one by one. This bit controls the output of the bus signal HPROT[3].

Bits	Description	Purpose
[1]	Bufferable or nonbufferable	Indicates whether the access is bufferable. 0: nonbufferable 1: bufferable For example, this bit is used to notify an AMBA bridge that the write operation on the source bus can be complete without waiting. That is, the operation can be performed even when the bridge does not arbitrate the operation to the destination bus and the slave device does not receive data completely. This bit controls the output of the bus signal HPROT[2].
[0]	Privileged or user	Access mode. 0: user mode 1: privileged mode This bit controls the output of the bus signal HPROT[1].

Usage of DMAC_Cn_CONFIG

Table 3-28 describes the flow controllers and transfer types corresponding to the flow_cntrl field of DMAC_Cn_CONFIG.

Table 3-28 Flow controllers and transfer types corresponding to the flow_cntrl field

Bit Value	Transfer Mode	Controller
000	Memory to memory	DMAC
001	Memory to peripheral	DMAC
010	Peripheral to memory	DMAC
011	Source device to destination device	DMAC
100	Source device to destination device	Destination device
101	Memory to peripheral	Destination device
110	Peripheral to memory	Source device
111	Source device to destination device	Source device

Processing an Interrupt

When data transfer is complete or an error occurs during data transfer, interrupts are reported to the interrupt controller. An interrupt is processed as follows:

Step 1 Read DMAC_INT_STAT to find the channel that transmits an interrupt request. When multiple channels transmit interrupt requests at the same time, the interrupt request with the highest priority is processed first.

Step 2 Read DMAC_INT_TC_STAT to query the value of the selected bit to check whether the interrupt sent by the corresponding channel is a terminal count interrupt. If the value is 1, the interrupt is a terminal count interrupt. In this case, go to Step 4; otherwise, go to Step 3.

Step 3 Read DMAC_INT_ERR_STAT to query the value of the selected bit to check whether the interrupt sent by the corresponding channel is an error interrupt. If the selected bit is 1, the interrupt is an error interrupt. In this case, go to Step 5; otherwise, end the operation.

Step 4 Process the terminal count interrupt as follows:

1. Write 1 to the selected bit of DMAC_INT_TC_CLR to clear the interrupt status of the corresponding channel.
2. Fetch or use up the data buffered in the memory. If necessary (such as creating a buffer in the memory), configure and enable the channel again.
3. End the operation.

Step 5 Process the error interrupt as follows:

1. Write 1 to the selected bit of DMAC_INT_ERR_CLR to clear the interrupt status of the corresponding channel.
2. Provide the error information. If necessary, configure and enable the channel again.
3. End the operation.

----End

3.5.5 Register Summary

Table 3-29 describes DMAC registers.

Table 3-29 Summary of the DMAC registers (base address: 0x100D_0000)

Offset Address	Register	Function Description	Page
0x000	DMAC_INT_STAT	DMAC interrupt status register	3-105
0x004	DMAC_INT_TC_STAT	DMAC terminal count interrupt status register	3-106
0x008	DMAC_INT_TC_CLR	DMAC terminal count interrupt clear register	3-106
0x00C	DMAC_INT_ERR_STAT	DMAC error interrupt status register	3-107
0x010	DMAC_INT_ERR_CLR	DMAC error interrupt clear register	3-107

Offset Address	Register	Function Description	Page
0x014	DMAC_RAW_INT_TC_STAT	DMAC raw terminal count interrupt status register	3-108
0x018	DMAC_RAW_INT_ERR_STAT	DMAC raw error interrupt status register	3-108
0x01C	DMAC_ENBLD_CHNS	DMAC channel enable status register	3-109
0x020	DMAC_SOFT_BREQ	DMA burst request register for software	3-109
0x024	DMAC_SOFT_SREQ	DMA single request register for software	3-110
0x028	DMAC_SOFT_LBREQ	DMA last burst request register for software	3-111
0x02C	DMAC_SOFT_LSREQ	DMA last single request register for software	3-111
0x030	DMAC_CONFIG	DMAC configuration register	3-112
0x034	DMAC_SYNC	DMAC request synchronization register	3-112
0x100+n x 0x20	DMAC_Cn_SRC_ADDR	DMAC source address register	3-113
0x104+n x 0x20	DMAC_Cn_DEST_ADDR	DMAC destination address register	3-114
0x108+n x 0x20	DMAC_Cn_LLI	DMAC LLI register	3-115
0x10C+n x 0x20	DMAC_Cn_CONTROL	DMAC control register	3-116
0x110+n x 0x20	DMAC_Cn_CONFIG	DMAC configuration register	3-118

3.5.6 Register Description

DMAC_INT_STAT

DMAC_INT_STAT is an interrupt status register. It shows the status of the masked interrupts. If certain bits of DMAC_INT_TC_STAT and DMAC_INT_ERR_STAT are masked at the same time, the corresponding bit of DMAC_INT_STAT1 is also masked. Each bit of DMAC_INT_STAT maps to one DMAC channel. When a bit is 1, an interrupt request is generated in the corresponding channel and the interrupt request may be an error interrupt or a terminal count interrupt.

Offset Address	Register Name	Total Reset Value
0x000	DMAC_INT_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												int_stat			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	-	reserved	Reserved.
[3:0]	RO	int_stat	Statuses of the masked interrupts of each DMA channel. Bit[3:0] map to channels 3–0. 0: No interrupt is generated. 1: An interrupt is generated. The interrupt request may be an error interrupt or a terminal count interrupt.

DMAC_INT_TC_STAT

DMAC_INT_TC_STAT is a terminal count interrupt status register. It shows the status of the masked terminal count interrupts. The corresponding mask bit is DMAC_Cn_CONFIG[itc], where n is the channel number ranging from 0 to 3. This register must work with DMAC_INT_STAT.

Offset Address	Register Name	Total Reset Value
0x004	DMAC_INT_TC_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												int_tc_stat			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	-	reserved	Reserved.
[3:0]	RO	int_tc_stat	Statuses of the masked terminal count interrupts. Bit[3:0] map to channels 3–0. 0: No terminal count interrupt is generated. 1: A terminal count interrupt is generated.

DMAC_INT_TC_CLR

DMAC_INT_TC_CLR is a terminal count interrupt clear register. It is used to clear terminal count interrupts.

Offset Address	Register Name	Total Reset Value
0x008	DMAC_INT_TC_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												int_tc_clr			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	-	reserved	Reserved.
[3:0]	WO	int_tc_clr	Terminal count interrupt clear. Bit[3:0] map to channels 3–0. 0: do not clear 1: clear

DMAC_INT_ERR_STAT

DMAC_INT_ERR_STAT is an error interrupt status register. It shows the status of the masked error interrupts. The corresponding mask bit is DMAC_Cn_CONFIG[ie]. The register must work with DMAC_INT_STAT.

Offset Address	Register Name	Total Reset Value
0x00C	DMAC_INT_ERR_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												int_err_stat			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	-	reserved	Reserved.
[3:0]	RO	int_err_stat	Statuses of masked error interrupts. Bit[3:0] map to channels 3–0. 0: No error interrupt is generated. 1: An error interrupt is generated.

DMAC_INT_ERR_CLR

DMAC_INT_ERR_CLR is an error interrupt clear register. It is used to clear error interrupts.

Offset Address	Register Name	Total Reset Value
0x010	DMAC_INT_ERR_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												int_err_clr			

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	-	reserved	Reserved.
[3:0]	WO	int_err_clr	Error interrupt clear. Bit[3:0] map to channels 3–0. 0: do not clear 1: clear

DMAC_RAW_INT_TC_STATUS

DMAC_RAW_INT_TC_STATUS is a raw terminal count interrupt status register. It shows the status of the raw terminal count interrupt of each channel.

Offset Address	Register Name	Total Reset Value
0x014	DMAC_RAW_INT_TC_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												raw_int_tc_stat			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	-	reserved	Reserved.
[3:0]	RO	raw_int_tc_stat	Statuses of the raw terminal count interrupt of each channel. Bit[3:0] map to channels 3–0. 0: No terminal count interrupt is generated. 1: A terminal count interrupt is generated.

DMAC_RAW_INT_ERR_STATUS

DMAC_RAW_INT_ERR_STATUS is a raw error interrupt status register. It shows the status of the raw error interrupt of each channel.

Offset Address	Register Name	Total Reset Value
0x018	DMAC_RAW_INT_ERR_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												raw_int_err_stat			

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	-	reserved	Reserved.
[3:0]	RO	raw_int_err_stat	Statuses of the raw error interrupt of each channel. Bit[3:0] map to channels 3–0. 0: No error interrupt is generated. 1: An error interrupt is generated.

DMAC_ENBLD_CHNS

DMAC_ENBLD_CHNS is a DMAC channel enable status register. It shows the enabled channels.

For example, if a bit of DMAC_ENBLD_CHNS is 1, the corresponding channel is enabled. The enable bit of DMAC_Cn_CONFIG of each channel determines whether the corresponding channel is enabled. When the DMA transfer over a channel is complete, the bit of DMAC_ENBLD_CHNS corresponding to the channel is cleared.

Offset Address	Register Name	Total Reset Value
0x01C	DMAC_ENBLD_CHNS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												enabled_channels			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	-	reserved	Reserved.
[3:0]	RO	enabled_channels	Channel enable. Bit[3:0] map to channels 3–0. 0: disabled 1: enabled

DMAC_SOFT_BREQ

DMAC_SOFT_BREQ is a DMA burst request register for software. It is used to control whether to generate a DMA burst request using software.

When this register is read, the device that is requesting the DMA burst transfer can be queried. This register and any peripheral each can generate a DAM request.

NOTE

It is not recommended to generate a software DMA request and a hardware DMA request at the same time.

Offset Address	Register Name	Total Reset Value
0x020	DMAC_SOFT_BREQ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																soft_breq															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	soft_breq	Controls whether to generate a DMA burst transfer request. For details about the request corresponding to each bit, see Table 3-24. When this register is written: 0: no effect 1: A DMA burst transfer request is generated. When the transfer is complete, the corresponding bit is cleared. When this register is read: 0: The peripheral corresponding to the request signal DMACBREQ[15:0] does not transmit a DMA burst request. 1: The peripheral corresponding to the request signal DMACBREQ[15:0] is requesting a DMA burst transfer.

DMAC_SOFT_SREQ

DMAC_SOFT_SREQ is a DMA single request register for software. It is used to control whether to generate a DMA single transfer request using software.

When this register is read, the device that is requesting the DMA single transfer can be queried. This register and any of the 16 DMA request input signals of the DMAC each can generate a DMA request.

NOTE

It is not recommended to generate a software DMA request and a hardware DMA request at the same time.

Offset Address	Register Name	Total Reset Value
0x024	DMAC_SOFT_SREQ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																soft_sreq															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.

[15:0]	RW	soft_sreq	Controls whether to generate a DMA burst transfer request. For details about the request corresponding to each bit, see Table 3-24. When this register is written: 0: no effect 1: A DMA single transfer request is generated. When the transfer is complete, the corresponding bit is cleared. When this register is read: 0: The peripheral corresponding to the request signal DMACSREQ[15:0] does not transmit a DMA single request. 1: The peripheral corresponding to the request signal DMACSREQ[15:0] is requesting a DMA single transfer.

DMAC_SOFT_LBREQ

DMAC_SOFT_LBREQ is a DMA last burst request register for software. It is used to control whether to generate a DMA last burst transfer request using software.

Offset Address	Register Name	Total Reset Value
0x028	DMAC_SOFT_LBREQ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																soft_lbreq															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	WO	soft_lbreq	Last burst request issued by the software. 0: no effect 1: A DMA last burst transfer request is generated. When the transfer is complete, the corresponding bit is cleared.

DMAC_SOFT_LSREQ

DMAC_SOFT_LSREQ is a DMA last single request register for software. It is used to control whether to generate a DMA last single transfer request.

Offset Address	Register Name	Total Reset Value
0x02C	DMAC_SOFT_LSREQ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																soft_lsreq															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	WO	soft_lsreq	Last single transfer request issued by the software. 0: no effect 1: A DMA last single transfer request is generated. When the transfer is complete, the corresponding bit is cleared.

DMAC_CONFIG

DMAC_CONFIG is a DMAC configuration register. It is used to configure DMAC operations. You can change the endian modes of the two master interfaces of the DMAC by writing to m1 (bit[1]) and m2 (bit[2]) of this register. After reset, the modes of the two master interfaces are set to little endian.

NOTE
Both Masters work in little endian mode.

Offset Address	Register Name	Total Reset Value
0x030	DMAC_CONFIG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													m2	m1	e
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	-	reserved	Reserved.
[2]	RW	m2	Endian mode of Master 2. 0: little endian mode 1: big endian mode
[1]	RW	m1	Endian mode of Master 1. 0: little endian mode 1: big endian mode
[0]	RW	e	DMAC enable. 0: disabled 1: enabled

DMAC_SYNC

DMAC_SYNC is a DMAC synchronization register. It is used to enable or disable the synchronization logic provided for DMA request signals.

Offset Address	Register Name	Total Reset Value
0x034	DMAC_SYNC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																dmac_sync															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	dmac_sync	Controls whether to synchronize the request signals. For details about the request corresponding to each bit, see Table 3-24. 0: enable the synchronization logic provided for the DMA request signals of the corresponding peripheral. 1: disable the synchronization logic provided for the DMA request signals of the corresponding peripheral.

NOTE

It is recommended that you disable the synchronization logic for all request signals.

DMAC_Cn_SRC_ADDR

DMAC_Cn_SRC_ADDR is a DMAC source address register. It shows the source addresses (sorted by byte) of the data to be transferred.

The offset address of the register is 0x100+n x 0x20. The value of n ranges from 0 to 3. The values 0–3 map to DMA channels 0–3.

Before a channel is enabled, its corresponding register must be programmed using software. After the channel is enabled, the register is updated in the following cases:

- The source address is incremented.
- A complete data block is transferred and then loaded from LLI nodes.

When a channel is active, no valid information is obtained when this register is read. This is because that after software obtains the register value, the value changes during data transfer. Therefore, the register is read after the channel stops data transfer. At this time, the read value is the last source address read by the DMAC.

The source and destination addresses must be aligned with the transfer widths of the source and destination devices.

Offset Address	Register Name	Total Reset Value
0x100 + n x 0x20	DMAC_Cn_SRC_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	src_addr																															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	src_addr	DMA source address.

The DMAC provides four channels. Each channel has the following five channel registers:

- DMAC_Cn_SRC_ADDR
- DMAC_Cn_DEST_ADDR
- DMAC_CnLLI
- DMAC_Cn_CONTROL
- DMAC_Cn_CONFIG

When the DMA loads LLI nodes from a memory, the DMAC updates the preceding registers except DMAC_CX_CONFIG automatically.

CAUTION

During DMA transfer, the DMAC may perform unexpected operations when the preceding channel registers are updated. Before changing the settings of a channel, you must disable the channel and then configure its relevant registers.

DMAC_Cn_DEST_ADDR

DMAC_Cn_DEST_ADDR is a destination address register. Its offset address is 0x104 + n x 0x20. The value of n ranges from 0 to 3. The values 0–3 map to DMA channels 0–3.

This register contains the destination address (sorted by byte) of the data to be transferred. Before a channel is enabled, its corresponding register must be programmed using software. After the channel is enabled, the register is updated in the following cases:

- Destination address increment.
- A complete data block is transferred and then loaded from LLI nodes.

When a channel is active, no valid information is obtained when this register is read. This is because that after software obtains the register value, the value changes during data transfer. Therefore, the register is read after the channel stops data transfer. At this time, the read value is the last destination address written by the DMAC.

Offset Address	Register Name	Total Reset Value
0x104 + n x 0x20	DMAC_Cn_DEST_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dest_addr																															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dest_addr	DMA destination address.

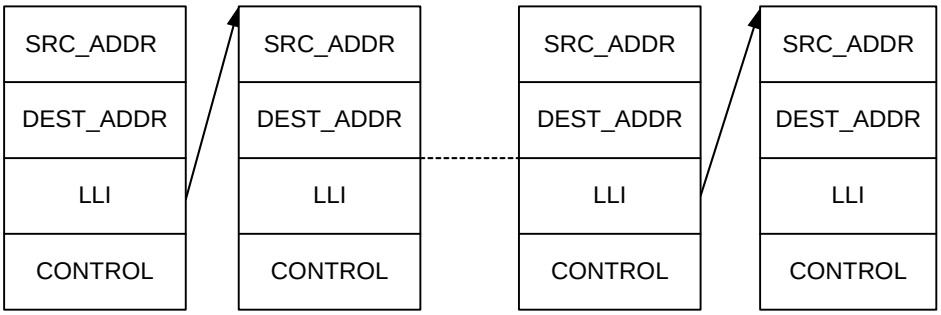
DMAC_CnLLI

DMAC_CnLLI is a DMAC LLI register. Its offset address is 0x108 + n x 0x20. The value of n ranges from 0 to 3. The values 0–3 map to DMA channels 0–3.

The data structure of a DMAC LLI node is as follows:

- Channel register DMAC_Cn_SRC_ADDR, for setting the start address of the source device
- Channel register DMAC_Cn_DEST_ADDR, for setting the start address of the destination device
- Channel register DMAC_CnLLI, for setting the address of the next node
- Channel register DMAC_Cn_CONTROL, for setting the master, data width, burst size, address increment, and transfer size of the source device and destination device

Figure 3-7 Structure of DMAC LLIs



CAUTION

The value of the LLI field must be less than or equal to 0xFFFF_FFF0. Otherwise, the address is wrapped around to 0x0000_0000 during a 4-word burst transfer. As a result, the data structure of LLI nodes cannot be stored in a continuous address area.

If the LLI field is set to 0, the current node is at the end of the linked list. In this case, the corresponding channel is disabled after the corresponding data blocks of the current node are transferred.

Offset Address	Register Name	Total Reset Value
0x108 + n x 0x20	DMAC_CnLLI	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lli																														r	lm
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RW	lli	LLI. The bit[31:2] of the next LLI node address and the address bit[1:0] are both set to 0. A linked list address must be 4-byte aligned.
[1]	RW	r	Reserved. This bit must be 0 during writes and must be masked during reads.
[0]	RW	lm	Master for loading the next LLI node. 0: Master1 1: Master2

DMAC_Cn_CONTROL

DMAC_Cn_CONTROL is a DMAC channel control register. Its offset address is 0x10C + n x 0x20. The value of n ranges from 0 to 3. The values 0–3 map to DMA channels 0–3.

Offset Address	Register Name	Total Reset Value
0x10C + n x 0x20	DMAC_Cn_CONTROL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	i	prot			di	si	d	s	dwidth				swidth				dbsize				sbsize				transfersize							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	i	Terminal count interrupt enable. This bit determines whether the current LLI node triggers a terminal count interrupt. 0: not trigger 1: trigger
[30:28]	RW	prot	HPROT[2:0] access protection signal transmitted by the Master.

[27]	RW	di	Destination address increment. 0: The destination address is not incremented 1: The destination address is incremented once after a data segment is transferred If the destination device is a peripheral, the destination address is not incremented. If the destination device is a memory, the destination address is incremented.
[26]	RW	si	Source address increment. 0: The source address is not incremented 1: The source address is incremented once after a data segment is transferred If the source device is a peripheral, the source address is not incremented. If the source device is a memory, the source address is incremented.
[25]	RW	d	Master for accessing the destination device. 0: The SIO, UART0, UART1, UART2, SSP1, and SSP0 access the destination device using Master1. 1: The SPI flash, NAND flash, and DDRC access the destination device using Master 2.
[24]	RW	s	Master for accessing the source device. 0: The SIO, UART0, UART1, UART2, SSP1, and SSP0 access the source device using Master1. 1: The SPI flash, NAND flash, and DDRC access the source device using Master2.
[23:21]	RW	dwidth	Transfer bit width of the destination device. The transfer bit width is invalid if it is greater than the bit width of the Master. The data widths of the destination and source devices can be different. The hardware automatically packs and unpacks the data. For details about the mapping between the value of DWidth and the bit width, see Table 3-26.
[20:18]	RW	swidth	Transfer bit width of the source device. The transfer bit width is invalid if it is greater than the bit width of the Master. The data widths of the destination and source devices can be different. The hardware automatically packs and unpacks the data. For details about the mapping between the value of SWidth and the bit width, see Table 3-26.

[17:15]	RW	dbsize	Burst size of the destination device. Indicates the number of data segments to be transferred by the destination device in a burst transfer, that is, the number of transferred data segments when DMACCnBREQ is valid. This value must be set to a burst size supported by the destination device. If the destination device is a memory, the value is set to the storage area size beyond the storage address boundary. For details about the mapping between the value of DBSize and the transfer size, see Table 3-25.
[14:12]	RW	sbsize	Burst size of the source device. Indicates the number of data segments to be transferred by the source device in a burst transfer, that is, the number of transferred data segments when DMACCnBREQ is valid. The value must be set to a burst size supported by the source device. If the source device is a memory, the value is set to the storage area size beyond the storage address boundary. For details about the mapping between the value of SBSize and the transfer length, see Table 3-25.
[11:0]	RW	transfersize	The DMA transfer size can be configured by writing to DMAC_Cn_CONTROL only when the DMAC is a flow controller. The transfer size indicates the number of the data segments to be transferred by the source device. When DMAC_Cn_CONTROL is read, the number of data segments transferred through the bus connected to the destination device is obtained. When a channel is active, no valid information is obtained when this register is read. This is because that after software obtains the register value, the value changes during data transfer. Therefore, the register is read after the channel is enabled and data transfer is stopped.

DMAC_Cn_CONFIG

DMAC_Cn_CONFIG is a DMAC channel configuration register. Its offset address is 0x110 + n x 0x20. The value of n ranges from 0 to 3. The values 0–3 map to DMA channels 0–3.

This register is not updated when a new LLI node is loaded.

Offset Address	Register Name	Total Reset Value
0x110 + n x 0x20	DMAC_Cn_CONFIG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													h	a	l	itc	ie	flow_cntrl		reserved		dest_peripheral				reserved		src_peripheral			e

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	-	reserved	Reserved. This bit must be 0 during writes and must be masked during reads.
[18]	RW	h	Halt bit. 0: The DMA request is allowed. 1: The subsequent DMA requests are ignored and the contents in the channel FIFO are completely transferred. This bit can disable a DMA channel without data loss by working with the Active bit and the Channel Enable bit.
[17]	RO	a	Active bit. 0: There is no data in the channel FIFO. 1: There is data in the channel FIFO. This bit can disable a DMA channel without data loss by working with the Halt bit and Channel Enable bit.
[16]	RW	l	Lock bit. 0: Disable lock transfer on the bus. 1: Enable lock transfer on the bus.
[15]	RW	itc	Terminal count interrupt mask bit. 0: Mask the terminal count interrupts of the channel. 1: Do not mask the terminal count interrupts of the channel.
[14]	RW	ie	Error interrupt mask bit. 0: Mask the error interrupts of the channel. 1: Do not mask the error interrupts of the channel.
[13:11]	RW	flow_cntrl	Flow control and transfer type field. This field is used to specify the flow controller and transfer type. The flow controller can be the DMAC, source device, or destination device. The transfer type can be memory to peripheral, peripheral to memory, peripheral to peripheral, or memory to memory. For details, see Table 3-28.
[10]	-	reserved	Reserved. This bit must be 0 during writes and must be masked during reads.
[9:6]	RW	dest_peripheral	Destination device. This field is used to select a peripheral request signal as the request signal of the DMA destination device of the channel. If the destination device for DMA transfer is a memory, this field is ignored.
[5]	-	reserved	Reserved. This bit must be 0 during writes and must be masked during reads.

[4:1]	RW	src_peripheral	Source device. This field is used to select a peripheral request signal as the request signal of the DMA source device of the channel. If the source device for DMA transfer is a memory, this field is ignored.
[0]	RW	e	Channel enable bit. The current status of a channel can be queried by reading this register or DMAC_ENBLD_CHNS. 0: disabled 1: enabled Clearing this bit can disable a channel. When this bit is cleared, the current bus transfer continues until the data transfer is complete. Then, the channel is disabled and the remaining data in the FIFO is lost. When the last LLI is transferred or an error occurs during transfer, the channel is also disabled and this bit is cleared. If you want to disable a channel without data loss, the Halt bit must be set to 1 so the subsequent DMA requests are ignored by the channel. After this, the Active bit must be polled until its value becomes 0. This indicates that there is no data in the channel FIFO. At this time, the Enable bit can be cleared. To enable a channel by setting this bit to 1, you must reinitialize the channel. If a channel is enabled by setting this bit to 1 only, unexpected results may occur.

NOTE

When a channel is disabled by writing to the Channel Enable bit, this bit can be set to 1 again only after the corresponding bit of DMAC_ENBLD_CHNS is polled to be 0. This is because the channel is not disabled immediately after the Channel Enable bit is cleared. The running delay during a bus burst operation also needs to be considered.

3.6 CIPHER

3.6.1 Overview

The CIPHER module supports data encryption and decryption using data encryption standard (DES), 3DES, or advanced encryption standard (AES) algorithm. The DES, 3DES, and AES algorithms are implemented according to FIPS46-3 and FIPS 197 standards. The DES/3DES and AES operating modes comply with FIPS-81 and NIST special 800-38a standards.

The CIPHER module can encrypt or decrypt a large amount of data effectively. In addition, it encrypts and decrypts one or more blocks at one time.

3.6.2 Features

The CIPHER module has the following features:

- Supports the AES key length of 128 bits, 192 bit, or 256 bits. If keys are configured by the key management module, the key length can be set only to 128 bits.

- Supports the DES key length of 64 bits. The values for bit 0, bit 8, bit 16, bit 24, bit 32, bit 40, bit 48, and bit 56 represent the parity check values for eight bytes respectively. The parity check values are not used during encryption or decryption.
- Supports 3-key and 2-key modes for the 3DES algorithm. If keys are configured by the key management module, only the 2-key mode is supported.
- Supports the operating modes of electronic codebook (ECB), cipher block chaining (CBC), 1-/8-/128-cipher feedback (CFB), 128-output feedback (OFB), and counter (CTR) for the AES algorithm. These operating modes comply with the NIST special 800-38a standard.
- Supports the operating modes of ECB, CBC, 1-/8-/64-CFB, and 1-/8-/64-OFB for the DES or 3DES algorithm. These operating modes comply with the FIPS-81 standard.
- Encrypts and decrypts one or more blocks at one time in ECB, CBC, CFB, OFB or CTR operating mode.
- Encrypts and decrypts one or more blocks at one time in CTR operating mode using the AES algorithm.
- Provides eight encryption/decryption keys (64 bits, 128 bits, 192 bits, or 256 bits) configured by the CPU.
- Provides eight keys (fixed at 128 bits) configured by the key management module. The master CPU cannot be read and written.
- Provides a single-block encryption/decryption channel and seven multi-block encryption/decryption channels. The single-block encryption/decryption channel can encrypt or decrypt a single block only at one time. In this case, the CPU writes data to the channel register and reads the results. For the multi-block encryption/decryption channel, the logic reads data from the DDR, and writes the encrypted or decrypted data to the DDR automatically.
- Supports weighted round robin policy for each channel. For a single-block channel, the weighted value is 1 by default; for a multi-block channel, the weighted value is configurable.
- Supports the same set of keys or different sets of keys for any channel.
- Keeps the data in the last incomplete block unprocessed when the data of the multi-block channels is not an integral multiple of encryption/decryption blocks.
- Supports data combination for multi-block channels. To be specific, if the remaining data in a linked list data block is insufficient to form an encryption/decryption block and the data block is not the last one to be processed, the remaining data is combined with the data in the next data block for encryption or decryption. This avoids data stuffing.
- Supports byte address for the multi-block encryption/decryption channel.
- Supports the multi-linked-list structure for the multi-block encryption/decryption channel and supports the combination of data from multiple linked lists. The linked list length is 20 bits. That is, the maximum data amount is 1 MB minus 1.
- Queries the interrupt status and masks and clears interrupts.
- Separately processes and controls interrupts for each channel.
- Supports multi-packet interrupts and aging interrupts.

3.6.3 Function Description

The operating modes of the DES, 3DES, and AES algorithms comply with the FIPS-81 and NIST special 800-38a standards. In the DES, 3DES, and AES algorithms, the ECB, CBC, and CFB operating modes are identical; however, the CTR (for the AES algorithm only) and OFB operating modes are slightly different.

3DES Algorithm

The 3DES algorithm supports both 3-key and 2-key operations. A 2-key operation can be regarded as a simplified 3-key operation. To be specific, key 3 is represented by key 1 in a 2-key operation.

Figure 3-8 shows the 3DES encryption of a 3-key operation and a 2-key operation.

Figure 3-8 3DES encryption of a 3-key operation and a 2-key operation

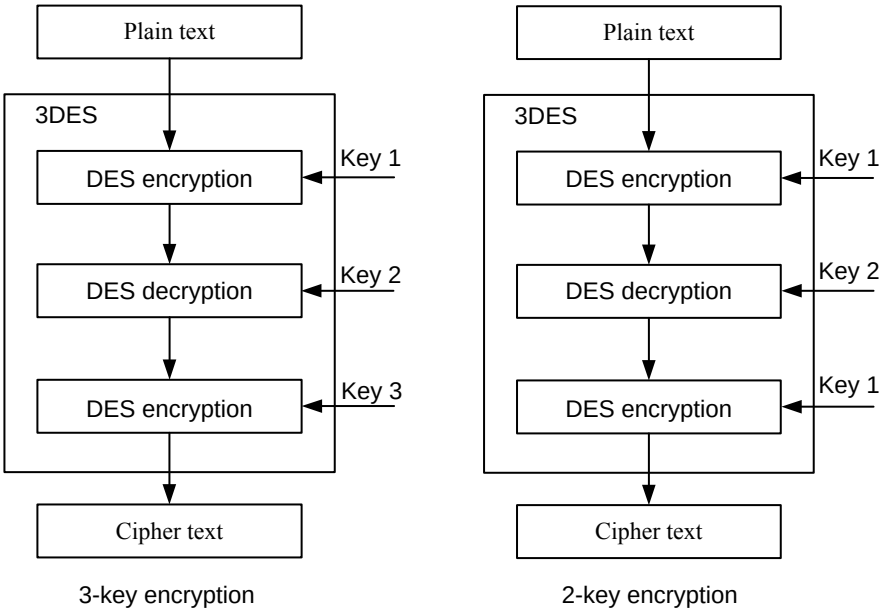
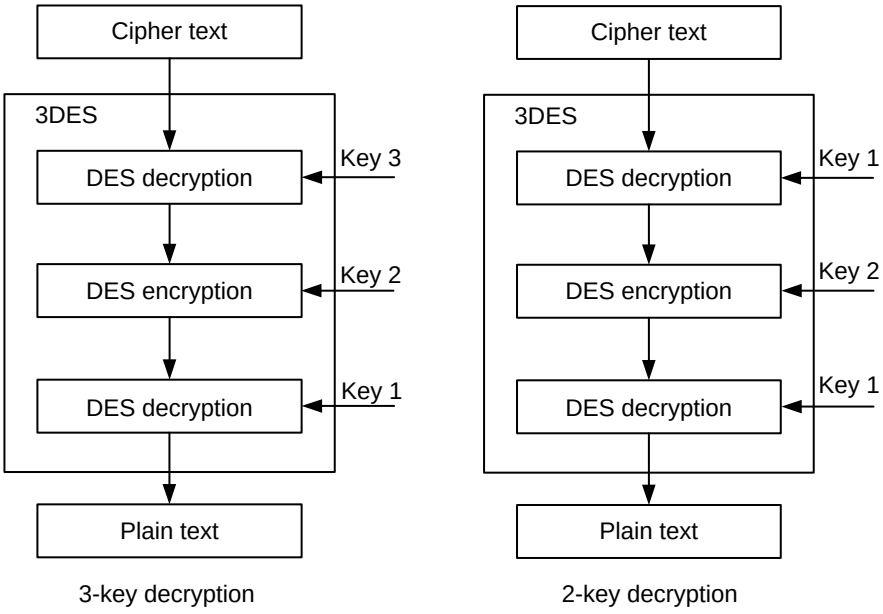


Figure 3-9 shows the 3DES decryption of a 3-key operation and a 2-key operation.

Figure 3-9 3DES decryption of a 3-key operation and a 2-key operation



ECB Mode

In ECB mode, encryption and decryption algorithms are directly applied to the block data. The operation of each block is independent. With this feature, the plain text encryption and cipher text decryption can be performed concurrently. Figure 3-10 shows the ECB mode of the AES and DES algorithms, and Figure 3-11 shows the ECB mode of the 3DES algorithm.

Figure 3-10 ECB mode of the AES and DES algorithms

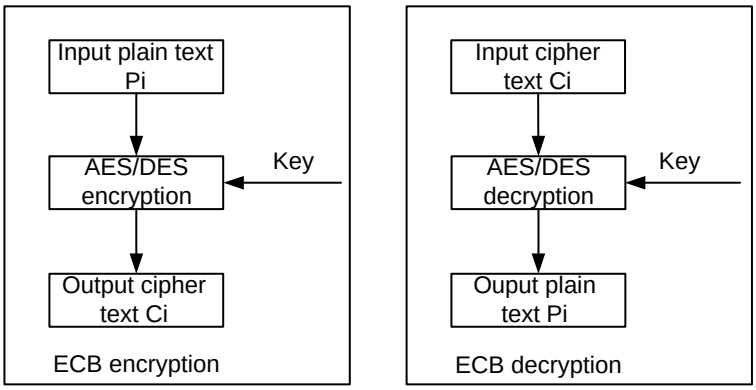
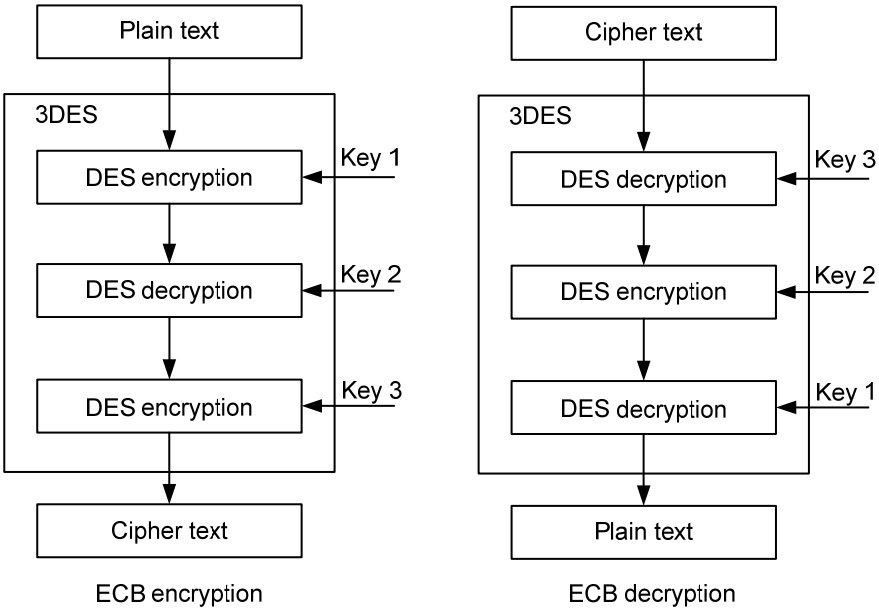


Figure 3-11 ECB mode of the 3DES algorithm



CBC Mode

In CBC mode, the encrypted input plain text block must be exclusive-ORed with the input initialization vector (IV) before being encrypted. The encryption processing of each plain text block is related to the block processing result (cipher text) of the previous plain text.

Therefore, encryption operations cannot be concurrently performed in CBC mode. The decryption operation, however, is independent of output plain text of the previous block. Therefore, decryption operations can be performed concurrently. Figure 3-12 shows the CBC mode of the AES and DES algorithms, and Figure 3-13 shows the CBC mode of the 3DES algorithm.

Figure 3-12 CBC mode of the AES and DES algorithms

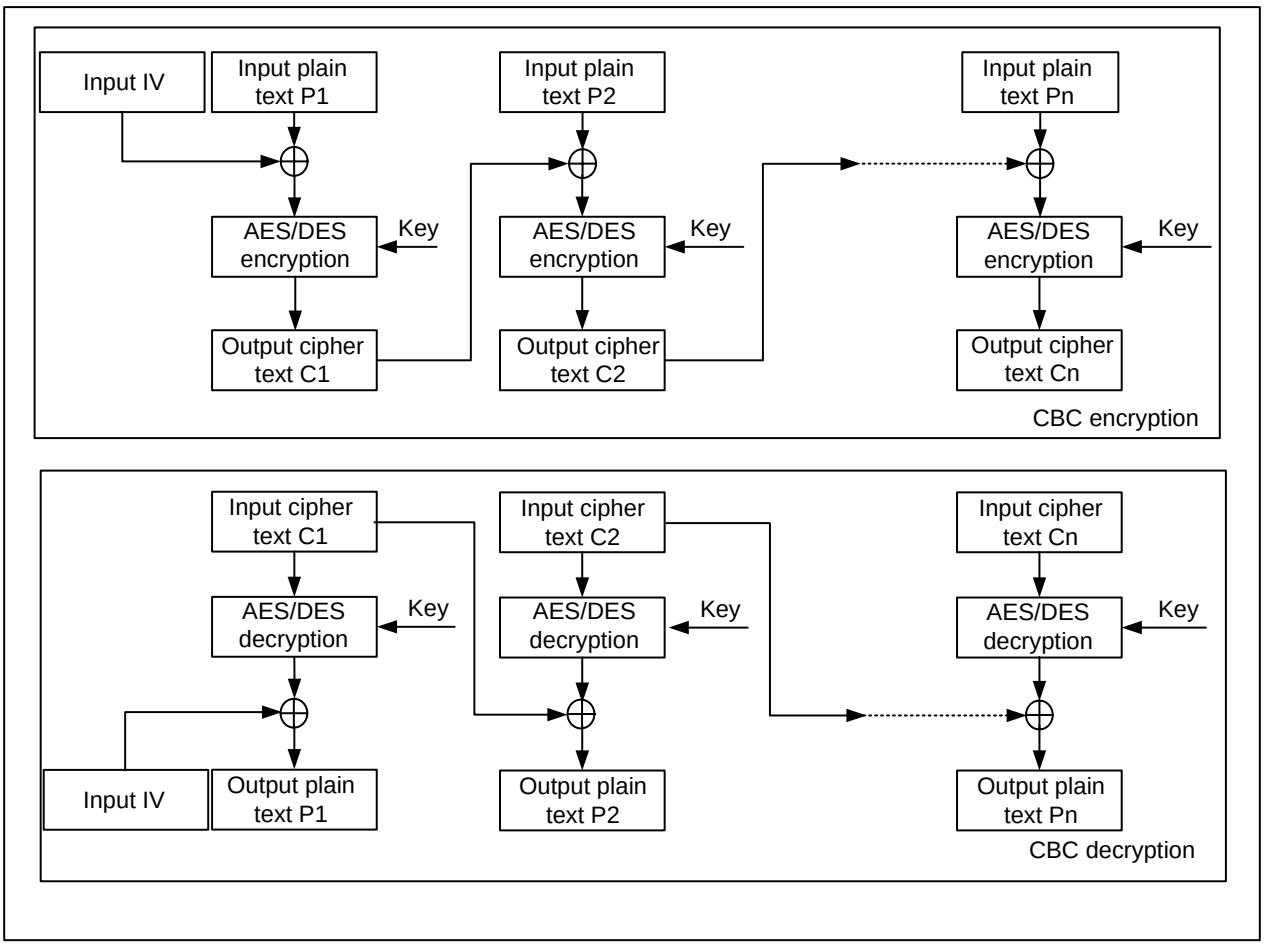
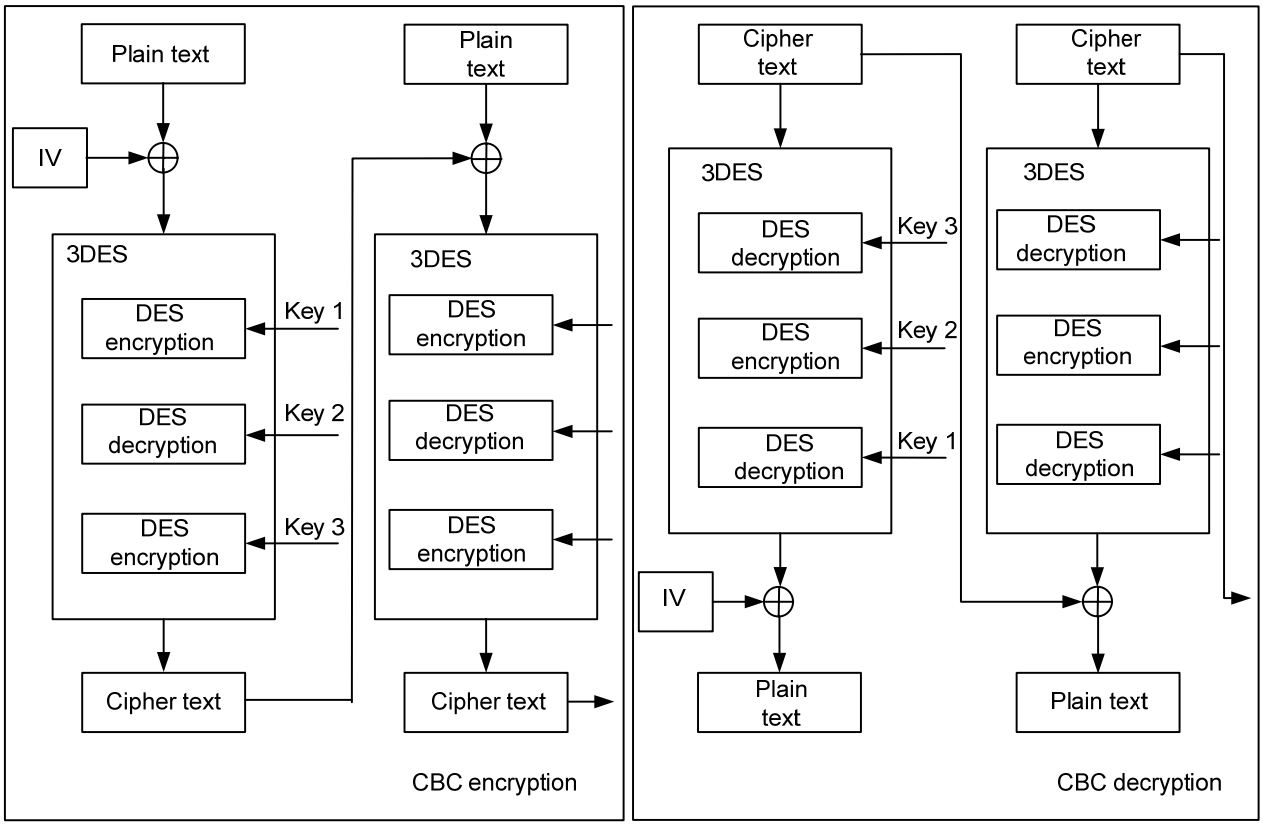


Figure 3-13 CBC mode of the 3DES algorithm



CFB Mode

The CFB mode is used to convert a block cipher into a stream cipher. This mode is implemented by selecting the operation bits of the CFB. The shift operation bits are represented by the letter s. The value of s is as follows:

- 1 bit, 8 bits, or 64 bits for the DES or 3DES algorithm
- 1 bit, 8 bits, or 128 bits for the AES algorithm

Figure 3-14 shows the s-bit CFB mode of the AES and DES algorithms, and Figure 3-15 shows the s-bit CFB mode of the 3DES algorithm.

Figure 3-14 S-bit CFB mode of the AES and DES algorithms

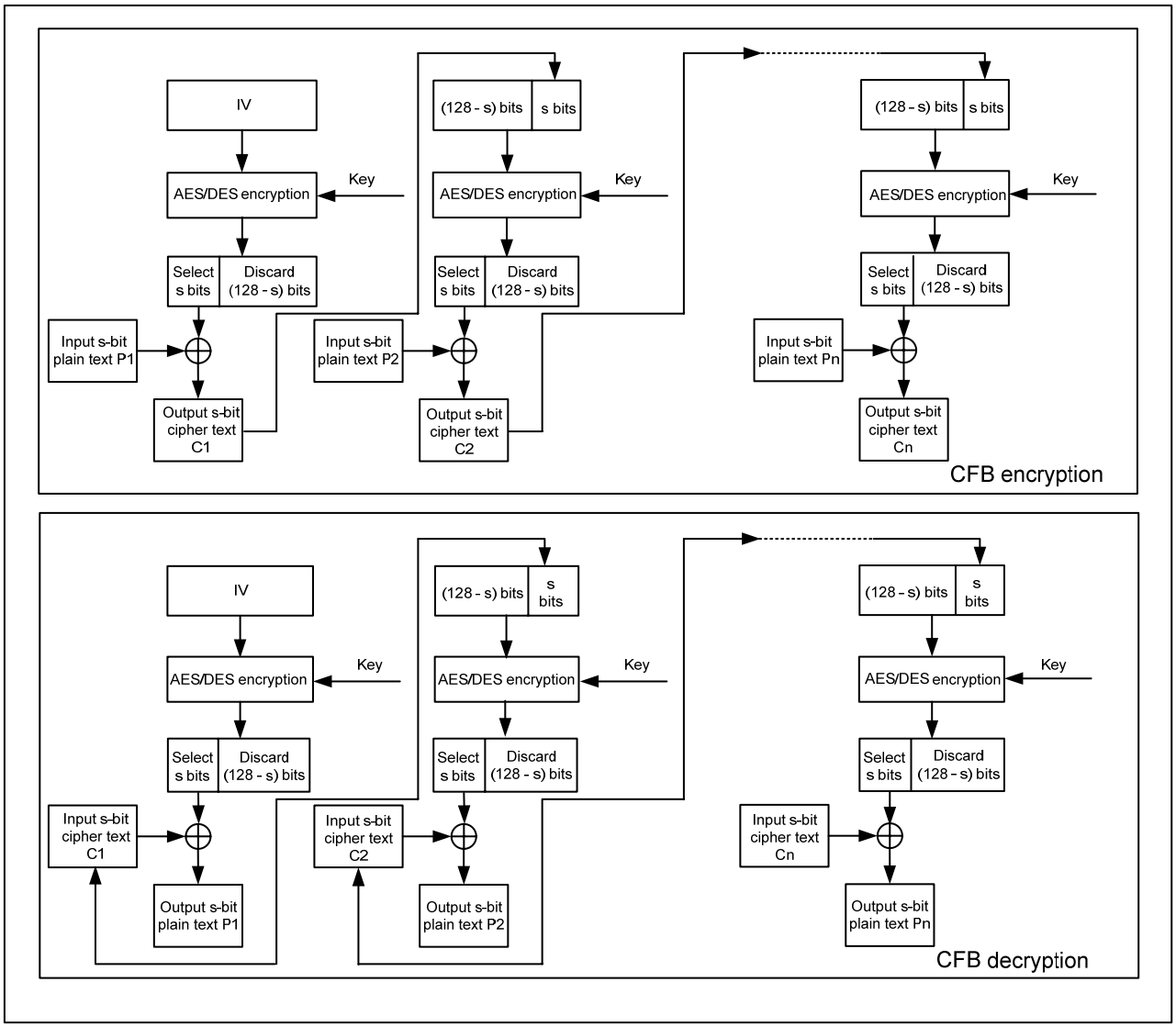
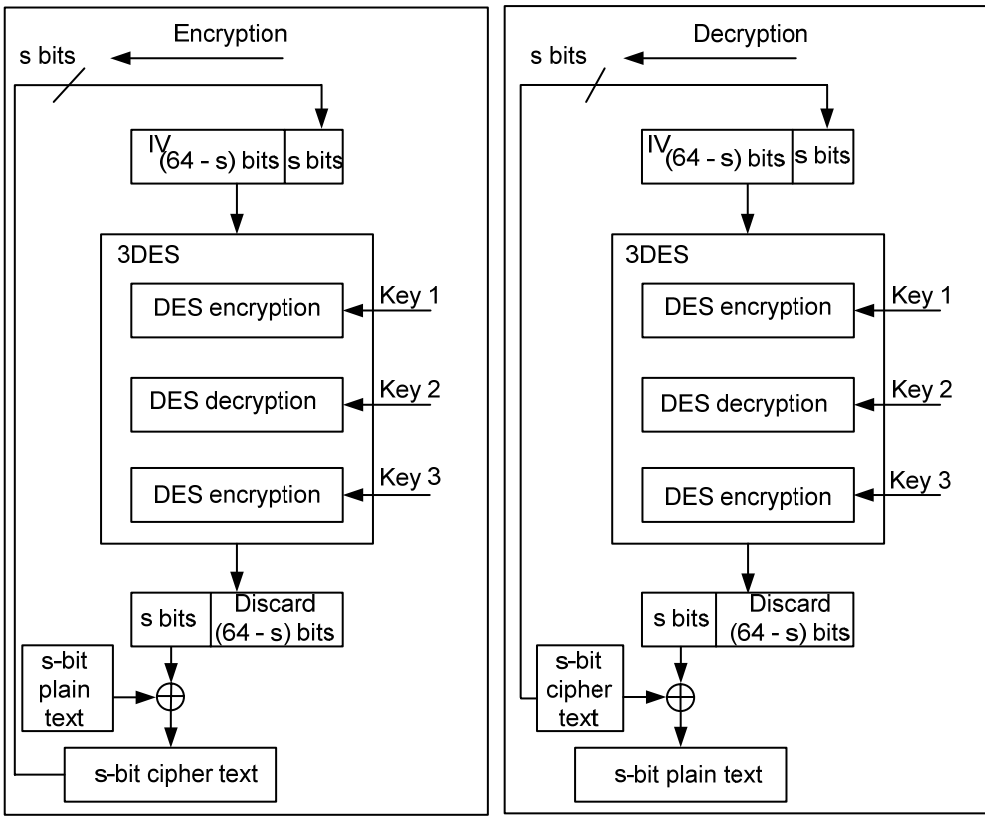


Figure 3-15 S-bit CFB mode of the 3DES algorithm



OFB Mode

In OFB mode, IVs serve as the inputs during encryption. If a same key is used, different IVs must be used to ensure operation security. The value of the s bit is as follows:

- 1 bit, 8 bits, or 64 bits for the DES or 3DES algorithm
- 128 bits for the AES algorithm

Figure 3-16 shows the OFB mode of the AES algorithm.

Figure 3-16 OFB mode of the AES algorithm

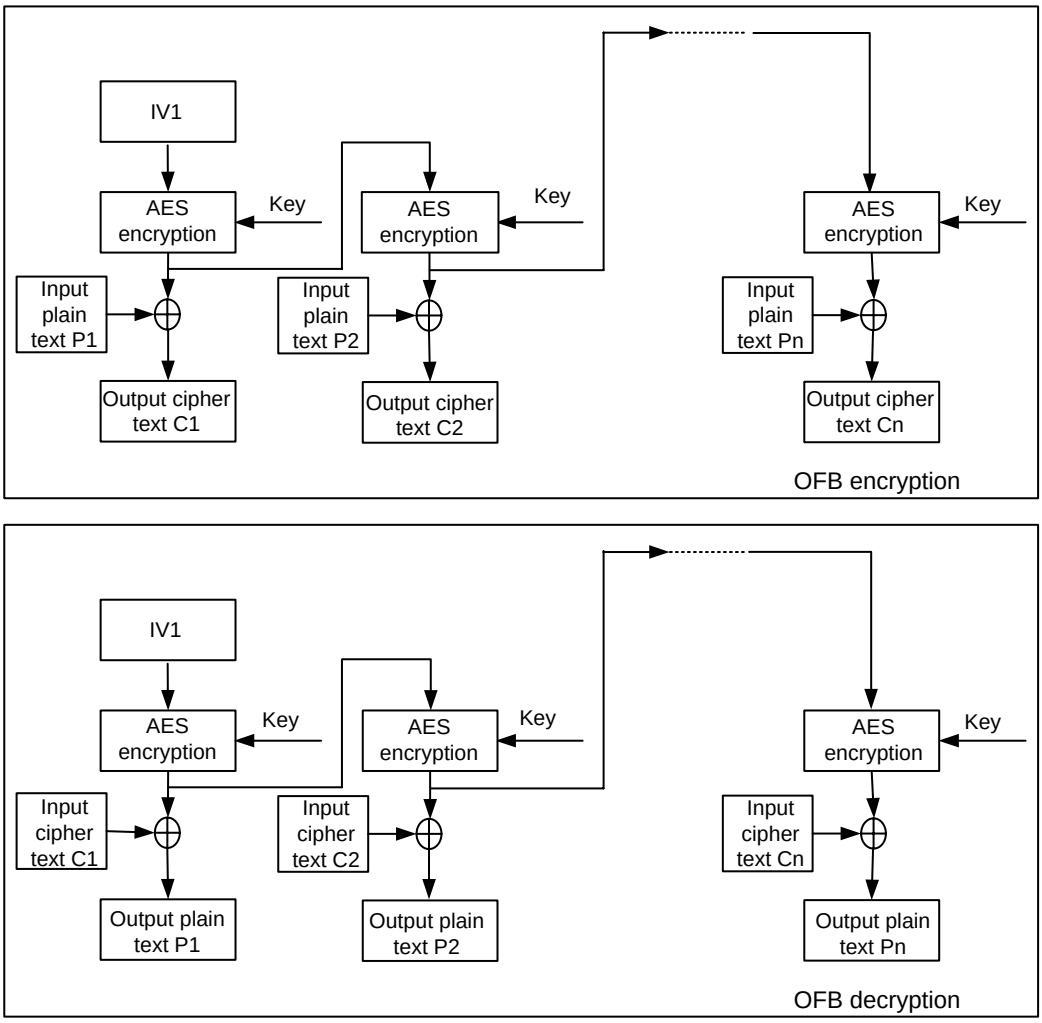


Figure 3-17 shows the s-bit OFB mode of the DES algorithm.

Figure 3-17 S-bit OFB mode of the DES algorithm

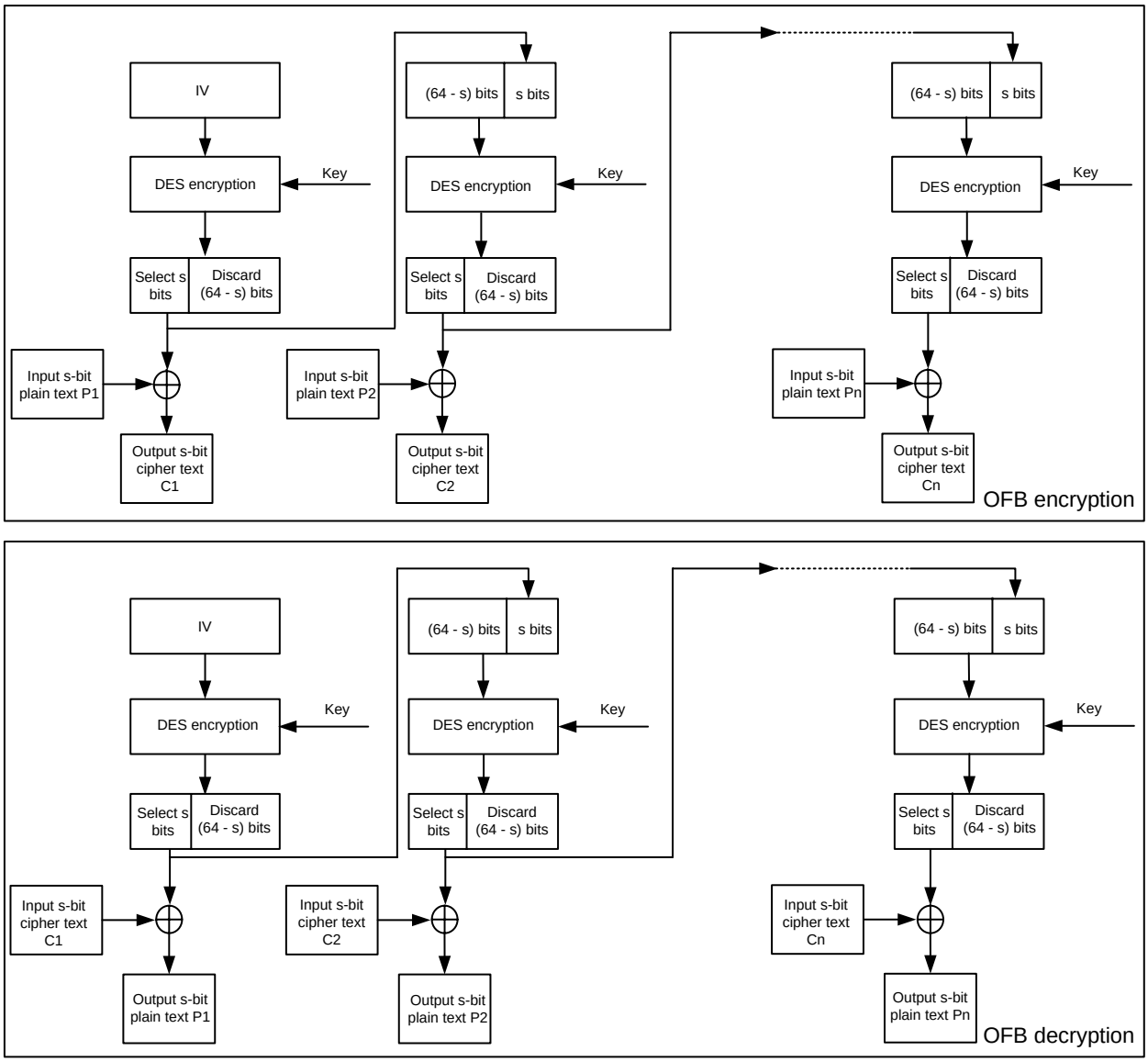
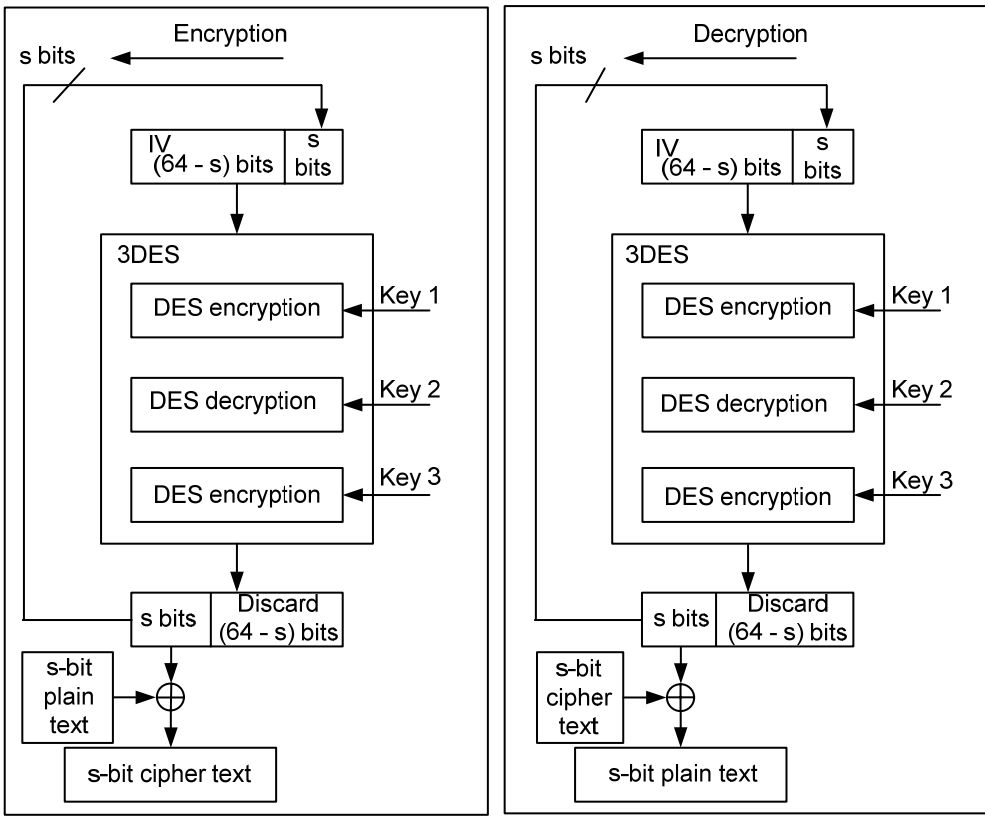


Figure 3-18 shows the s-bit OFB mode of the 3DES algorithm.

Figure 3-18 S-bit OFB mode of the 3DES algorithm



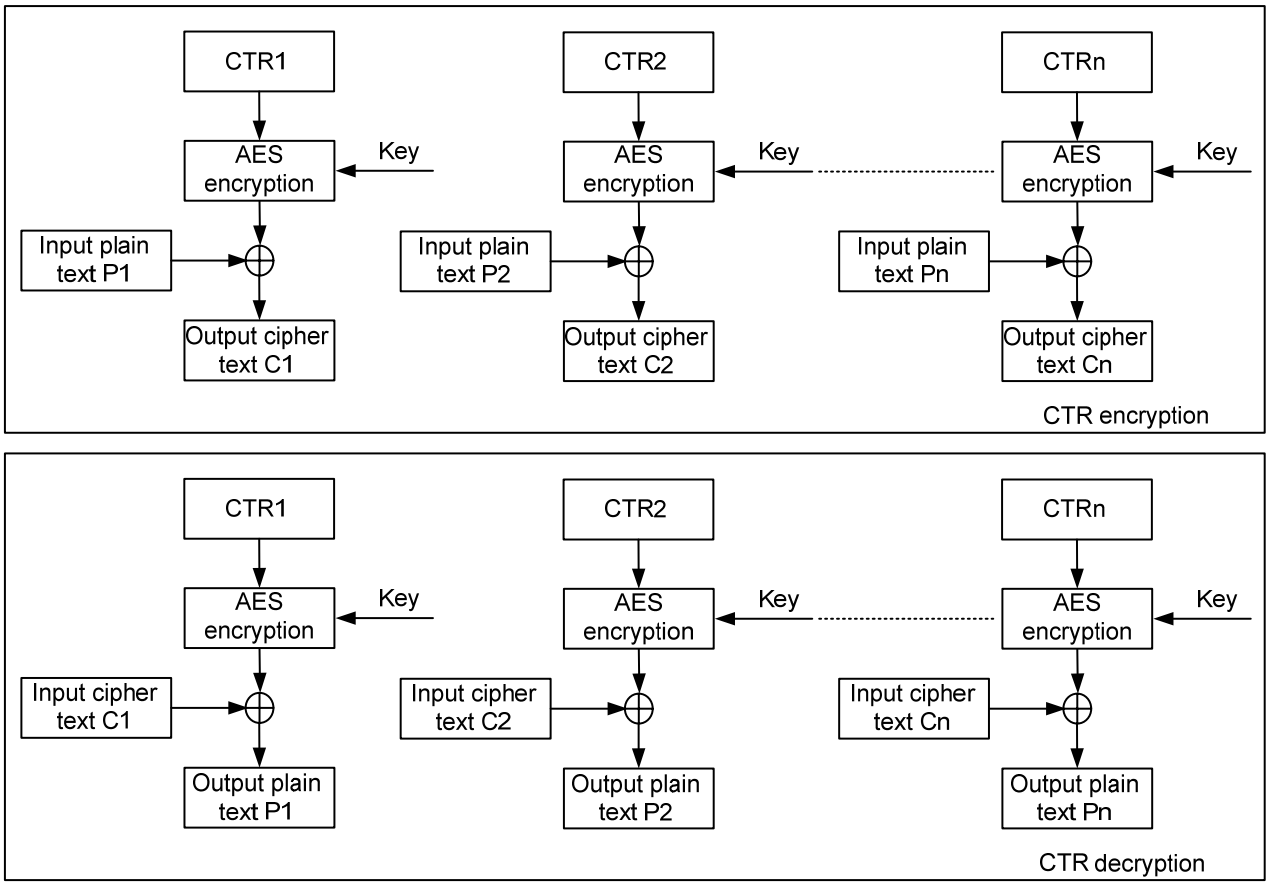
CTR Mode

In CTR mode, different data segments are input to the CIPHER module by using the AES algorithm to ensure data security. Such data can be the count value CTRn. Therefore, CTRn determines the security of the CTR mode.

NOTE
CTRn is obtained by using the accumulation count mode.

Figure 3-19 shows the CTR mode of the AES algorithm.

Figure 3-19 CTR mode of the AES algorithm



3.6.4 Operating Mode

Single-Block Operation Process of the CIPHER Module

The CIPHER module provides channel 0 as the single-block encryption/decryption channel. A single-block operation is performed as follows:

Step 1 Check whether channel 0 is busy by querying the ch0_busy field of the configuration register CHAN0_CFG of channel 0. If channel 0 is not busy, configure data inputs and write related configuration information to the registers of channel 0.

Step 2 Write to the ch0_start field of CHAN0_CFG to enable channel 0 to start encryption or decryption.

Step 3 Check whether encryption and decryption of channel 0 are complete in either of following ways:

- Query the ch0_busy field. If ch0_busy indicates that channel 0 is not busy, encryption and decryption are complete.
- Check whether the interrupt of channel 0 is generated. If the interrupt is generated, encryption and decryption are complete.

Step 4 Read the registers CHAN0_CIPHER_DOUT and CHAN0_CIPHER_IVOUT of channel 0.

----End

Multi-Block Operation Process of the CIPHER Module

The CIPHER module provides seven multi-block encryption/decryption channels. The weighted value of each channel can be set using software based on its rate. These channels automatically read data from the DDR, and write the encrypted or decrypted data to the DDR.

A multi-block operation is performed as follows:

Step 1 Initialize the channels, including setting the depth, start address, number of multi-packet interrupts, aging interrupt time of the input and output queues of each channel, and setting the control register of each channel.

Step 2 When data needs to be encrypted or decrypted, query CHANn_IBUF_CNT. If the value of this register is smaller than the value of CHANn_IBUF_NUM, add the header of the data linked list corresponding to the data to be encrypted or decrypted to the input queue, and go to Step 4; otherwise, go to step 3.

Step 3 Enable the interrupt corresponding to the input queue channel, wait for the generation of the interrupt, read CHANn_IEMPTY_CNT, write to this register to clear the interrupt, and add new data to the input queue.

Step 4 Add the linked list header of the output buffer to the output queue.

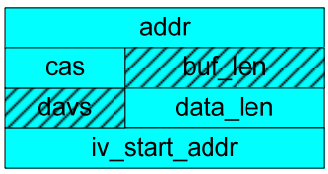
Step 5 Enable the interrupt corresponding to the output queue.

Step 6 Fetch data from the output queue, and write the number of currently received packets to CHANn_OFULL_CNT to clear the interrupt.

----End

Figure 3-20 shows the structure of the linked list header of a multi-block encryption/decryption channel.

Figure 3-20 Structure of the linked list header of a multi-block encryption/decryption channel

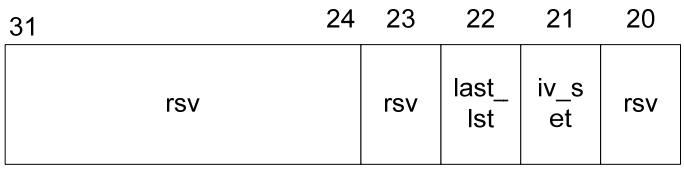


The field definitions are as follows:

- addr is the start address of the buffer pointer by the linked list header. The start address can be byte address.
- data_len is the length of the valid data pointed by the linked list header.
- cas is CIPHER control information.

Figure 3-21 shows the bits of cas.

Figure 3-21 Bits of cas



- iv_set indicates that the IV of the data pointed by the current linked list header must be replaced. iv_start_addr indicates the start address of the IV in the DDR. This address must be aligned by word.
- last_lst indicates that the data pointed by the current linked list header is the last linked list of a data block. If the logic encounters an incomplete encryption/decryption block after processing the linked list, the logic writes the incomplete block to the output buffer without performing encryption and decryption.

Clock Gating

When no encryption is required and the CIPHER module is idle, the CIPHER clock can be disabled by configuring the registers of the system controller, which reduces power consumption.

Soft Reset

The CIPHER module can be soft-reset by configuring the registers of the system controller.

3.6.5 Register Summary

Table 3-30 describes CIPHER registers.

Table 3-30 Summary of CIPHER registers (base address: 0x100C_0000)

Offset Address	Register	Description	Page
0x0000–0x000C	CHAN0_CIPHER_DOUT	CIPHER output register for channel 0 (for single-block encryption/decryption)	3-135
0x0010–0x001C	CHAN0_CIPHER_IVOUT	Operation complete IV output register of the CIPHER module	3-136
0x0020–0x008C	CHAN_CIPHER_IVOUT	IV output register for channels 1–7	3-136
0x0090–0x018C	CIPHER_KEY	CPU configuration key register of the CIPHER module	3-137
0x1000	CHAN0_CIPHER_CTRL	Encryption/decryption control register for channel 0	3-138
0x1004–0x1010	CHAN0_CIPHER_IVIN	CIPHER VI block input register for channel 0	3-141

Offset Address	Register	Description	Page
0x1014–0x1020	CHAN0_CIPHER_DIN	128-bit block input register of the CIPHER module	3-142
0x1000+n x 128	CHANn_IBUF_NUM	Input queue total depth register for channel n (n = 1–7) (linked list header count register)	3-142
0x1000+n x 128+0x4	CHANn_IBUF_CNT	Pending data buffer count register for channel n in the input queue	3-143
0x1000+n x 128+0x8	CHANn_IEMPTY_CNT	Processed data buffer count register for channel n in the input queue	3-143
0x1000+n x 128+0xC	CHANn_INT_ICNTCFG	Input queue multi-packet interrupt threshold register for channel n	3-144
0x1000+n x 128+0x10	CHANn_CIPHER_CTRL	Encryption/decryption control register for channel n	3-144
0x1000+n x 128+0x14	CHANn_SRC_LST_SADDR	Input queue start address register for channel n	3-146
0x1000+n x 128+0x18	CHANn_IAGE_TIMER	Input queue interrupt aging time configuration register for channel n	3-146
0x1000+n x 128+0x3C	CHANn_OBUF_NUM	Output queue total depth register for channel n (linked list header count register)	3-147
0x1000+n x 128+0x40	CHANn_OBUF_CNT	Pending data buffer count register for channel n in the output queue	3-147
0x1000+n x 128+0x44	CHANn_OFULL_CNT	Processed data buffer count register for channel n in the output queue	3-148
0x1000+n x 128+0x48	CHANn_INT_OCNTCFG	Output queue multi-packet interrupt threshold register for channel n	3-148
0x1000+n x 128+0x4C	CHANn_DEST_LST_SADDR	Output queue start address register for channel n	3-148
0x1000+n x 128+0x50	CHANn_OAGE_TIMER	Output queue interrupt aging time configuration register for channel n	3-149
0x1400	INT_STATUS	Interrupt status register	3-149
0x1404	INT_EN	Interrupt enable register	3-150
0x1408	INT_RAW	Raw interrupt status register	3-151
0x140C	RST_STATUS	Reset status indicator register	3-152
0x1410	CHAN0_CFG	Channel 0 configuration register	3-152

Table 3-31 describes the value range and definition of the variable in the offset addresses of CIPHER registers.

Table 3-31 Variable in the offset addresses of CIPHER registers

Variable	Value Range	Description
n	1–7	Channels 1–7 of the CIPHER module

3.6.5.2 Register Description

CHAN0_CIPHER_DOUT

CHAN0_CIPHER_DOUT is the CIPHER output register for channel 0 (for single-block encryption/decryption).

The data read from this register is the results of a single-block operation. The results of the AES algorithm are different from those of the DES or 3DES algorithm. The details are as follows:

- For the AES algorithm
  - If the 1-CFB mode is selected, the least significant bit (LSB) is valid, that is, CIPHER_DOUT bit[0] is valid.
  - If the 8-CFB mode is selected, lower eight bits are valid, that is, CIPHER_DOUT bit[7:0] is valid.
  - If the 128-CFB mode is selected, 128 bits are valid.
  - In other modes, 128 bits are valid.
- For the DES or 3DES algorithm
  - If the 1-CFB or 1-OFB mode is selected, the LSB is valid, that is, CIPHER_DOUT bit[0] is valid.
  - If the 8-CFB or 8-OFB mode is selected, lower eight bits are valid, that is, CIPHER_DOUT bit[7:0] is valid.
  - If the 64-CFB or 64-OFB mode is selected, lower 64 bits are valid, that is, CIPHER_DOUT bit[63:0] is valid.
  - In other modes, lower 64 bits are valid, that is, CIPHER_DOUT bit[63:0] is valid.

Offset Address	Register Name	Total Reset Value
0x0000–0x000C	CHAN0_CIPHER_DOUT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_cipher_dout																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	chan0_cipher_dout	128-bit block output of the CIPHER module. Each address maps to a 32-bit data segment. CIPHER_DOUT[31:0]: address 0x0000 CIPHER_DOUT[63:32]: address 0x0004 CIPHER_DOUT[95:64]: address 0x0008 CIPHER_DOUT[127:96]: address 0x000C

CHAN0_CIPHER_IVOUT

CHAN0_CIPHER_IVOUT is an operation complete IV output register of the CIPHER module.

Note the following points when reading this register:

- This register can be ignored in ECB or CTR mode.
- If a single-block operation is performed, the data of this register is the vector output of the block. The data can be used as the vector input in the next block operation for the same data packet.
  - If the AES algorithm is selected, 128 bits are valid.
  - If the DES or 3DES algorithm is selected (CIPHER_CTRL[cipher_mode] = 0b00, 0b01, or 0b11), lower 64 bits are valid, that is, CIPHER_IVOUT bit[63:0] is valid.
- If a multi-block operation is performed, the data read from this register is the output vector of the last block operation.
  - If the AES algorithm is selected, 128 bits are valid.
  - If the DES or 3DES algorithm is selected, lower 64 bits are valid, that is, CIPHER_IVOUT bit[63:0] is valid.

Offset Address	Register Name	Total Reset Value
0x0010–0x001C	CHAN0_CIPHER_IVOUT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_cipher_ivout																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	chan0_cipher_ivout	Vector output after the operation of the CIPHER module is complete. It can be ignored in ECB or CTR mode. Each address maps to a 32-bit data segment. CIPHER_DOUT[31:0]: address 0x0010 CIPHER_IVOUT[63:32]: address 0x0014 CIPHER_IVOUT[95:64]: address 0x0018 CIPHER_IVOUT[127:96]: address 0x001C

CHAN_CIPHER_IVOUT

CHAN_CIPHER_IVOUT is the IV output register for channels 1–7.

Offset Address	Register Name	Total Reset Value
0x0020–0x008C	CHAN_CIPHER_IVOUT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan_cipher_ivout																															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	chan_cipher_ivout	0x0020–0x002C: channel 1 0x0030–0x003C: channel 2 0x0040–0x004C: channel 3 0x0050–0x005C: channel 4 0x0060–0x006C: channel 5 0x0070–0x007C: channel 6 0x0080–0x008C: channel 7

CIPHER_KEY

CIPHER_KEY is a CPU configuration key register of the CIPHER module. The key is the configured value of the CPU, and the CPU can be read or written.

Note the following points when configuring this register:

- If the DES algorithm is selected, lower 64 bits are valid, that is, CIPHER_KEY[63:0] is valid.
- For the 3DES algorithm

  If a 3-key operation is performed (CIPHER_CTRL[key_length] = 0b00, 0b01, or 0b10), low 192 bits are valid.

  where

  - CIPHER_KEY bit[63:0] indicates key 1.
  - CIPHER_KEY bit[127:64] indicates key 2.
  - CIPHER_KEY bit[191:128] indicates key 3.

  If a 2-key operation is selected (CIPHER_CTRL[key_length] = 0b11), lower 128 bits are valid.

  where

  - CIPHER_KEY bit[63:0] indicates key 1.
  - CIPHER_KEY bit[127:64] indicates key 2.
- For the AES algorithm
  - If a 128-bit key operation is performed, lower 128 bits are valid, that is, CIPHER_KEY bit[127:0] is valid.
  - If a 192-bit key operation is performed, lower 192 bits are valid, that is, CIPHER_KEY bit[191:0] is valid.
  - If a 256-bit key operation is performed, 256 bits are valid.

The CIPHER module allows you to configure eight keys. Each channel can use one key, and multiple channels can share one key.

Offset Address	Register Name	Total Reset Value
0x0090–0x018C	CIPHER_KEY	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cipher_key																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cipher_key	Key input of the CIPHER module. Each address maps to a 32-bit data segment. CIPHER_KEY[31:0]: address 0x0090 CIPHER_KEY[63:32]: address 0x0094 CIPHER_KEY[95:64]: address 0x0098 CIPHER_KEY[127:96]: address 0x009C CIPHER_KEY[159: 128]: address 0x00A0 CIPHER_KEY[191:160]: address 0x00A4 CIPHER_KEY[223:192]: address 0x00A8 CIPHER_KEY[255:224]: address 0x00AC 0x0090–0x00AC: host_key0 0x00B0–0x00CC: host_key1 0x00D0–0x00EC: host_key2 0x00F0–0x010C: host_key3 0x0110–0x012C: host_key4 0x0130–0x014C: host_key5 0x0150–0x016C: host_key6 0x0170–0x018C: host_key7

CHAN0_CIPHER_CTRL

CHAN0_CIPHER_CTRL is the encryption/decryption control register for channel 0. Channel 0 is a single-block encryption/decryption channel.

Note the following points when configuring this register:

- Configure this register before configuring others registers of the CIPHER module.
- In the modes except the CFB mode of the AES algorithm, the CIPHER_CTRL[width] cannot be set to 01 or 10.
- In the modes except the CFB and OFB modes of the DES and 3DES algorithms, CIPHER_CTRL[width] cannot be set to 01 or 10.

Offset Address	Register Name	Total Reset Value
0x1000	CHAN0_CIPHER_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																key_adder				key_sel		byte_seq		reserved		key_length		ivin_sel		width		alg_sel		mode			decrypt
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	-	reserved	Reserved.
[16:14]	RW	key_adder	ID of the key used by the current channel. 000: host_key0 001: host_key1 010: host_key2 011: host_key3 100: host_key4 101: host_key5 110: host_key6 111: host_key7
[13]	RW	key_sel	Key select. 0: keys configured by the CPU 1: keys generated by the key management module
[12]	-	reserved	Reserved.
[11]	-	reserved	Reserved.
[10:9]	RW	key_length	Key length select. For the AES algorithm: 00: 128 bits 01: 192bits 10: 256 bits 11: 128 bits For the DES algorithm: 00: 3 keys 01: 3 keys 10: 3 keys 11: 2 keys
[8]	RW	ivin_sel	Input select of CIPHER_IVIN. 0: do not configure CIPHER_IVIN 1: configure CIPHER_IVIN

Offset Address	Register Name	Total Reset Value
0x1000	CHAN0_CIPHER_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																key_adder		key_sel	byte_seq	reserved	key_length		ivin_sel	width		alg_sel		mode			decrypt
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RW	width	Bit width control. For the DES or 3DES algorithm: 00: 64 bits 01: 8 bits 10: 1 bit 11: 64 bits For the AES algorithm: 00: 128 bits 01: 8 bits 10: 1 bit 11: 128 bits
[5:4]	RW	alg_sel	Algorithm select. 00: DES algorithm 01: 3DES algorithm 10: AES algorithm 11: DES algorithm
[3:1]	RW	mode	Operating mode select. For the AES algorithm: 000: ECB mode 001: CBC mode 010: CFB mode 011: OFB mode 100: CTR mode Other values: ECB mode For the DES algorithm: 000: ECB mode 001: CBC mode 010: CFB mode 011: OFB mode Other values: ECB mode

Offset Address	Register Name	Total Reset Value
0x1000	CHAN0_CIPHER_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																key_adder		key_sel	byte_seq	reserved		key_length		ivin_sel		width		alg_sel		mode		decrypt
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	decrypt	Encryption/decryption select. 0: encryption 1: decryption

CHAN0_CIPHER_IVIN

CHAN0_CIPHER_IVIN is the CIPHER VI block input register for channel 0.

Assume that channel 0 is selected for the single-block encryption/decryption and the selected mode is not ECB mode (CIPHER_CTRL[mode] = 0b001, 0b010, 0b011, or 0b100).

- If you do not want to configure the input vector (CIPHER_CTRL[ivin_sel] = 0b0), CIPHER_IVIN can be ignored.
- If you want to configure the input vector (CIPHER_CTRL[ivin_sel] = 0b1), CIPHER_IVIN needs to be configured. If the AES algorithm is selected (CIPHER_CTRL [alg_sel] = 0b10), CIPHER_IVIN bit[127:0] is valid. If the DES or 3DES algorithm is selected (CIPHER_CTRL[alg_sel] = 0b00, 0b01, or 0b11), lower 64 bits are valid, that is, CIPHER_IVIN bit[63:0] is valid.

Offset Address	Register Name	Total Reset Value
0x1004–0x1010	CHAN0_CIPHER_IVIN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_cipher_ivin																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan0_cipher_ivin	128-bit IV of the CIPHER module for channel 0 or the data input from the counter. Each address maps to a 32-bit data segment. CIPHER_IVIN[31:0]: address 0x1004 CIPHER_IVIN[63:32]: address 0x1008 CIPHER_IVIN[95:64]: address 0x100C CIPHER_IVIN[127:96]: address 0x1010

CHAN0_CIPHER_DIN

CHAN0_CIPHER_DIN is a 128-bit block input register of the CIPHER module.

Note the following points when configuring this register:

If channel 0 is selected for the single-block operation, this register needs to be configured.

- Assume that the AES algorithm (CIPHER_CTRL[alg_sel] = 0b10) is selected.
  - If the 1-CFB mode is selected, the LSB is valid, that is, CIPHER_DIN bit[0] is valid.
  - If the 8-CFB mode is selected, lower eight bits are valid, that is, CIPHER_DIN bit[7:0] is valid.
  - If the 128-CFB mode is selected, 128 bits are valid.
  - In other modes, 128 bits are valid.
- Assume that the DES or the 3DES algorithm (CIPHER_CTRL[alg_sel] = 0b00, 0b01, or 0b11) is selected.
  - If the 1-CFB or 1-OFB mode is selected, the LSB is valid, that is, CIPHER_DIN bit[0] is valid.
  - If the 8-CFB or 8-OFB mode is selected, lower eight bits are valid, that is, CIPHER_DIN bit[7:0] is valid.
  - If the 64-CFB or 64-OFB mode is selected, lower 64 bits are valid, that is, CIPHER_DIN bit[63:0] is valid.
  - In other modes, lower 64 bits are valid, that is, CIPHER_DIN bit[63:0] is valid.

Offset Address	Register Name	Total Reset Value
0x1014–0x1020	CHAN0_CIPHER_DIN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_cipher_din																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan0_cipher_din	128-bit block input of the CIPHER module for channel 0. Each address maps to a 32-bit data segment. CIPHER_DIN[31:0]: address 0x1014 CIPHER_DIN[63:32]: address 0x1018 CIPHER_DIN[95:64]: address 0x101c CIPHER_DIN[127:96]: address 0x1020

CHANn_IBUF_NUM

CHANn_IBUF_NUM is the input queue total depth register for channel n (n = 1–7). This register can be used to configure the count of linked list headers.

Offset Address	Register Name	Total Reset Value
0x1000+n x 128	CHANn_IBUF_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ibuf_num																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	ibuf_num	Input queue depth, that is, count of linked list headers configured for each channel.

CHANn_IBUF_CNT

CHANn_IBUF_CNT is the pending data buffer count register for channel n in the input queue. When this register is written by using software, the logic adds the original value of the register and the written value. After the logic processes a buffer, the value of this register is decreased by 1.

Offset Address	Register Name	Total Reset Value
0x1000+n x 128+0x4	CHANn_IBUF_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ibuf_cnt																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	ibuf_cnt	Count of buffers to be processed in the input queue.

CHANn_IEMPTY_CNT

CHANn_IEMPTY_CNT is the processed buffer count register for channel n in the input queue. When this register is written by software, the logic subtracts the written value from the original value of this register. After the logic processes a buffer, the value of this register is increased by 1.

Offset Address	Register Name	Total Reset Value
0x1000+n x 128+0x8	CHANn_IEMPTY_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																iempty_cnt																

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	iempty_cnt	Count of processed buffers in the input queue.

CHANn_INT_ICNTCFG

CHANn_INT_ICNTCFG is the input queue multi-packet interrupt threshold register for channel n. When the count of buffers in the input queue processed by the logic is above the threshold, an input queue interrupt is reported.

Offset Address	Register Name	Total Reset Value
0x1000+n x 128+0xC	CHANn_INT_ICNTCFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																int_icnt_cfg															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	int_icnt_cfg	Input queue multi-packet interrupt threshold.

CHANn_CIPHER_CTRL

CHANn_CIPHER_CTRL is the encryption/decryption control register for channel n.

Note the following points when configuring this register:

- You must configure this register before performing encryption or decryption using the channel.
- In the modes other than the CFB mode of the AES algorithm, CIPHER_CTRL[width] cannot be set to 01 or 10.
- In the modes other than the CFB and OFB modes of the DES or 3DES algorithm, CIPHER_CTRL[width] cannot be set to 01 or 10.

Offset Address	Register Name	Total Reset Value
0x1000+n x 128+0x10	CHANn_CIPHER_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	weight								reserved				key_adder				key_sel	byte_seq	ts_vld	key_length				reserved	width			alg_sel		mode		decrypt

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	-	weight	Weighted value of the current channel, in the unit of 64 bytes.
[21:17]	-	reserved	Reserved.
[16:14]	RW	key_adder	ID of the key used by the current channel. The key can be any one in the addresses 0–7.
[13]	RW	key_sel	Key select. 0: keys configured by the CPU 1: keys generated by the key management module
[12:11]	-	reserved	Reserved.
[10:9]	RW	key_length	Key length select. For the AES algorithm: 00: 128 bits 01: 192 bits 10: 256 bits 11: 128 bits For the DES algorithm: 00: 3 keys 01: 3 keys 10: 3 keys 11: 2 keys
[8]	-	reserved	Reserved.
[7:6]	RW	width	Bit width control. For the DES or 3DES algorithm: 00: 64 bits 01: 8 bits 10: 1 bit 11: 64 bits For the AES algorithm: 00: 128 bits 01: 8 bits 10: 1 bit 11: 128 bits
[5:4]	RW	alg_sel	Algorithm select. 00: DES algorithm 01: 3DES algorithm 10: AES algorithm 11: DES algorithm

[3:1]	RW	mode	Operating mode select. For the AES algorithm: 000: ECB mode 001: CBC mode 010: CFB mode 011: OFB mode 100: CTR mode Other values: ECB mode For the DES algorithm: 000: ECB mode 001: CBC mode 010: CFB mode 011: OFB mode Other values: ECB mode
[0]	RW	decrypt	Encryption/decryption select. 0: encryption 1: decryption

CHANn_SRC_LST_SADDR

CHANn_SRC_LST_SADDR is the input queue start address register for channel n. The address must be aligned by word.

Offset Address	Register Name	Total Reset Value
0x1000+n x 128+0x14	CHANn_SRC_LST_SADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	src_lst_saddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	src_lst_saddr	Start address of the input queue.

CHANn_IAGE_TIMER

CHANn_IAGE_TIMER is the input queue interrupt aging time configuration register for channel n. If an overflow occurs in the aging time counter and the count of processed buffers in the input queue is greater than 0, an input queue processing complete interrupt is reported.

Offset Address	Register Name	Total Reset Value
0x1000+n x 128+0x18	CHANn_IAGE_TIMER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																iage_timer															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	iage_timer	Aging interrupt timer.

CHANn_OBUF_NUM

CHANn_OBUF_NUM is the output queue total depth register for channel n. This register can be used to configure the count of linked list headers.

Offset Address	Register Name	Total Reset Value
0x1000+n x 128+0x3C	CHANn_OBUF_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																obuf_num															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	obuf_num	Total depth of the output queue.

CHANn_OBUF_CNT

CHANn_OBUF_CNT is the pending data buffer count register for channel n in the output queue. When this register is written by using software, the logic adds the original value of the register and the written value. After the logic processes a buffer, the value of this register is decreased by 1.

Offset Address	Register Name	Total Reset Value
0x1000+n x 128+0x40	CHANn_OBUF_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																obuf_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.

[15:0]	RW	obuf_cnt	Count of buffers to be processed in the output queue.

CHANn_OFULL_CNT

CHANn_OFULL_CNT is the processed buffer count register for channel n in the output queue. When this register is written by software, the logic subtracts the written value from the original value of this register. After the logic processes a buffer, the value of this register is increased by 1.

Offset Address	Register Name	Total Reset Value
0x1000+n x 128+0x44	CHANn_OFULL_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ofull_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	ofull_cnt	Count of processed buffers in the output queue.

CHANn_INT_OCNTCFG

CHANn_INT_OCNTCFG is the output queue multi-packet interrupt threshold register for channel n. When the count of buffers in the output queue processed by the logic is above the threshold, an output queue interrupt is reported.

Offset Address	Register Name	Total Reset Value
0x1000+n x 128+0x48	CHANn_INT_OCNTCFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																int_ocnt_cfg															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	int_ocnt_cfg	Output queue multi-packet interrupt threshold.

CHANn_DEST_LST_SADDR

CHANn_DEST_LST_SADDR is the output queue start address register for channel n. The address must be aligned by word.

Offset Address	Register Name	Total Reset Value
0x1000+n x 128+0x4C	CHANn_DEST_LST_SADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dest_lst_saddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dest_lst_saddr	Start address of the output queue.

CHANn_OAGE_TIMER

CHANn_OAGE_TIMER is the output queue interrupt aging time configuration register for channel n. If an overflow occurs in the aging time counter and the count of processed buffers in the output queue is greater than 0, an output queue processing complete interrupt is reported.

Offset Address	Register Name	Total Reset Value
0x1000+n x 128+0x50	CHANn_OAGE_TIMER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																oage_timer															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	oage_timer	Aging interrupt timer.

INT_STATUS

INT_STATUS is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0x1400	INT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ch7_ibuf_int	ch6_ibuf_int	ch5_ibuf_int	ch4_ibuf_int	ch3_ibuf_int	ch2_ibuf_int	ch1_ibuf_int	ch0_ibuf_int	ch7_obuf_int	ch6_obuf_int	ch5_obuf_int	ch4_obuf_int	ch3_obuf_int	ch2_obuf_int	ch1_obuf_int	reserved

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15]	RO	ch7_ibuf_int	Input queue data interrupt for channel 7.
[14]	RO	ch6_ibuf_int	Input queue data interrupt for channel 6.
[13]	RO	ch5_ibuf_int	Input queue data interrupt for channel 5.
[12]	RO	ch4_ibuf_int	Input queue data interrupt for channel 4.
[11]	RO	ch3_ibuf_int	Input queue data interrupt for channel 3.
[10]	RO	ch2_ibuf_int	Input queue data interrupt for channel 2.
[9]	RO	ch1_ibuf_int	Input queue data interrupt for channel 1.
[8]	RO	ch0_ibuf_int	Data processing complete interrupt for channel 0.
[7]	RO	ch7_obuf_int	Output queue data interrupt for channel 7.
[6]	RO	ch6_obuf_int	Output queue data interrupt for channel 6.
[5]	RO	ch5_obuf_int	Output queue data interrupt for channel 5.
[4]	RO	ch4_obuf_int	Output queue data interrupt for channel 4.
[3]	RO	ch3_obuf_int	Output queue data interrupt for channel 3.
[2]	RO	ch2_obuf_int	Output queue data interrupt for channel 2.
[1]	RO	ch1_obuf_int	Output queue data interrupt for channel 1.
[0]	-	reserved	Reserved.

INT_EN

INT_EN is an interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x1404	INT_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	int_en	reserved															ch7_ibuf_en	ch6_ibuf_en	ch5_ibuf_en	ch4_ibuf_en	ch3_ibuf_en	ch2_ibuf_en	ch1_ibuf_en	ch0_ibuf_en	ch7_obuf_en	ch6_obuf_en	ch5_obuf_en	ch4_obuf_en	ch3_obuf_en	ch2_obuf_en	ch1_obuf_en	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	int_en	Total interrupt enable for the CIPHER module.

[30:16]	-	reserved	Reserved.
[15]	RW	ch7_ibuf_en	Input queue data interrupt enable for channel 7.
[14]	RW	ch6_ibuf_en	Input queue data interrupt enable for channel 6.
[13]	RW	ch5_ibuf_en	Input queue data interrupt enable for channel 5.
[12]	RW	ch4_ibuf_en	Input queue data interrupt enable for channel 4.
[11]	RW	ch3_ibuf_en	Input queue data interrupt enable for channel 3.
[10]	RW	ch2_ibuf_en	Input queue data interrupt enable for channel 2.
[9]	RW	ch1_ibuf_en	Input queue data interrupt enable for channel 1.
[8]	RW	ch0_ibuf_en	Data processing complete interrupt enable for channel 0.
[7]	RW	ch7_obuf_en	Output queue data interrupt enable for channel 7.
[6]	RW	ch6_obuf_en	Output queue data interrupt enable for channel 6.
[5]	RW	ch5_obuf_en	Output queue data interrupt enable for channel 5.
[4]	RW	ch4_obuf_en	Output queue data interrupt enable for channel 4.
[3]	RW	ch3_obuf_en	Output queue data interrupt enable for channel 3.
[2]	RW	ch2_obuf_en	Output queue data interrupt enable for channel 2.
[1]	RW	ch1_obuf_en	Output queue data interrupt enable for channel 1.
[0]	-	reserved	Reserved.

INT_RAW

INT_RAW is a raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x1408	INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ch7_ibuf_raw	ch6_ibuf_raw	ch5_ibuf_raw	ch4_ibuf_raw	ch3_ibuf_raw	ch2_ibuf_raw	ch1_ibuf_raw	ch0_ibuf_raw	ch7_obuf_raw	ch6_obuf_raw	ch5_obuf_raw	ch4_obuf_raw	ch3_obuf_raw	ch2_obuf_raw	ch1_obuf_raw	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15]	RWC	ch7_ibuf_raw	Raw input queue data interrupt for channel 7.
[14]	RWC	ch6_ibuf_raw	Raw input queue data interrupt for channel 6.

[13]	RWC	ch5_ibuf_raw	Raw input queue data interrupt for channel 5.
[12]	RWC	ch4_ibuf_raw	Raw input queue data interrupt for channel 4.
[11]	RWC	ch3_ibuf_raw	Raw input queue data interrupt for channel 3.
[10]	RWC	ch2_ibuf_raw	Raw input queue data interrupt for channel 2.
[9]	RWC	ch1_ibuf_raw	Raw input queue data interrupt for channel 1.
[8]	RWC	ch0_ibuf_raw	Raw data processing complete interrupt for channel 0.
[7]	RWC	ch7_obuf_raw	Raw output queue data interrupt for channel 7.
[6]	RWC	ch6_obuf_raw	Raw output queue data interrupt for channel 6.
[5]	RWC	ch5_obuf_raw	Raw output queue data interrupt for channel 5.
[4]	RWC	ch4_obuf_raw	Raw output queue data interrupt for channel 4.
[3]	RWC	ch3_obuf_raw	Raw output queue data interrupt for channel 3.
[2]	RWC	ch2_obuf_raw	Raw output queue data interrupt for channel 2.
[1]	RWC	ch1_obuf_raw	Raw output queue data interrupt for channel 1.
[0]	-	reserved	Reserved.

RST_STATUS

RST_STATUS is a reset status indicator register.

Offset Address	Register Name	Total Reset Value
0x140C	RST_STATUS	0x0000_0001

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								rst_status
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	1

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RO	rst_status	Reset status indicator of the CIPHER module. 0: The CIPHER module is being reset. 1: The CIPHER module is working properly.

CHAN0_CFG

CHAN0_CFG is channel 0 configuration register.

Offset Address	Register Name	Total Reset Value
0x1410	CHAN0_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														ch0_busy	ch0_start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	-	reserved	Reserved.
[1]	RO	ch0_busy	Status signal of channel 0. 0: Channel 0 is idle. 1: Encryption and decryption are being performed in channel 0.
[0]	RW	ch0_start	Encryption/decryption start signal of channel 0. 0: After fetching data from the input register of channel 0, the logic sets the signal to 0. 1: The value 1 must be written to this signal when channel 0 is enabled for encryption and decryption.

3.7 Timer

3.7.1 Overview

The timer module implements the timing and counting functions. It not only serves as the system clock of the operating system, but also can be used by applications for timing and counting. The timer module has four dual-timer modules: dual-timer0 and dual-timer1. Besides the different base addresses, the four dual-timer modules provide different functions in the system applications. The details about the four dual-timer modules are as follows:

- Dual-timer0 consists of timer0 and timer1 that share a base address and an interrupt signal.
- Dual-timer1 consists of timer2 and timer3 that share a base address and an interrupt signal.

Each dual-timer module consists of two timers with the same functions.

3.7.2 Features

Each dual-timer module has the following features:

- Provides two 16-bit or 32-bit down counters. Each counter has a prescaler that supports three configurable levels.
- Provides a configurable count clock, that is, the clock can serve as the clock of the advanced peripheral bus (APB) or 3 MHz crystal oscillator clock

- Supports three count modes: free-running mode, periodic mode, and one-shot mode.
- Loads the initial value through either of the following registers: TIMERx_LOAD and TIMERx_BGLOAD
- Reads the current count value at any time
- Generates an interrupt when the count value is decreased to 0

3.7.3 Function Description

Typical Application

The timer module of the Hi3518 is designed for software. The four dual-timer modules of the Hi3518 provide different count clock configurations based on applications.

Function Principle

The timer is a 32-bit or 16-bit configurable down counter. The counter value is decremented by 1 on each rising edge of the count clock. When the count value reaches 0, the timer generates an interrupt.

The timer supports three count modes:

- Free-running mode

  The timer counts continuously. When the count value reaches 0, the timer wraps its value around to the maximum value automatically and then continues to count. When the count length is 32 bits, the maximum value is 0xFFFF_FFFF. When the count length is 16 bits, the maximum value is 0xFFFF. In free-running mode, the count value is decremented immediately from the loaded value. When the value reaches 0, the value is wrapped around to the maximum value.
- Periodic mode

  The timer counts continuously. When the count value reaches 0, the timer loads an initial value from TIMERx_BGLOAD again and then continues to count.
- One-shot mode

  The initial value is loaded to the timer. When the count value of the timer reaches 0, the timer stops counting. The timer starts to count again only when a new value is loaded and the timer is enabled.

Each timer has a prescaler that divides the frequency of the working clock of each timer by 1, 16, or 256. In this way, flexible frequencies of the count clock are provided. An initial value is loaded to the timer as follows:

- An initial value can be loaded by writing TIMERx_LOAD. When the timer works, if a value is written to TIMERx_LOAD, the timer recounts starting from this value immediately. This method is applicable to all count modes.
- The count cycle in periodic mode can be set by writing TIMERx_BGLOAD. The current count value of the timer is not affected immediately when TIMERx_BGLOAD is written. Instead, the timer continues to count until the count value reaches 0. Then the timer loads the new value of TIMERx_BGLOAD and starts to count.

3.7.4 Operating Mode

Initialization

The timer must be initialized when the system is initialized. To initialize timerX (X ranges from 0 to 3), do as follows:

Step 1 Write to TIMERx_LOAD to load an initial value to the timer.

Step 2 When the timer is required to work in periodic mode and the count cycle is different from the initial value loaded to the timer, write to TIMERx_BGLOAD to set the count cycle of the timer.

Step 3 Configure the SC_CTRL register of the system controller to set the reference clock of the clock enable signal of the timer.

Step 4 Write to TIMERx_CONTROL to set the count mode, counter length, prescaling factor, and interrupt mask of the timer, and then enable the timer to count.

----End

Interrupt Processing

The timer is used to generate interrupts periodically. Therefore, interrupt processing is a process of activating and waiting the timing interrupt. To process an interrupt, do as follows:

Step 1 Configure TIMERx_INTCLR to clear the interrupt of the timer.

Step 2 Activate the processes of waiting for the interrupt and execute the process.

Step 3 When all the processes of waiting for the interrupt are complete or the wait interrupt is in hibernate state, resume the interrupt and continue to execute the interrupted program.

----End

Clock Selection

Each timer has two optional count clocks. The following sections describe how to select a clock by taking timer0 as an example.

To select the APB clock as the count clock, do as follows:

Step 1 Set SC_CTRL[timeren0ov] to 1.

Step 2 Initialize the timer and start to count.

----End

To select the 3 MHz crystal oscillator clock as the count clock, do as follows:

Step 3 Set SC_CTRL[timeren0sel] to 0.

Step 4 Initialize the timer and start to count.

----End

3.7.5 Register Summary

The timer module consists of four timers and each timer involves a group of registers. The four groups of registers have the same features except that their base addresses and offset addresses are different. The details about their base addresses are as follows:

- Timer0 and timer1 share the base address 0x2000_0000.
- Timer2 and timer3 share the base address 0x2001_0000.

NOTE

The value of X in timerX ranges from 0 to 3.

- The registers for timer0 and timers3 are the same. In this section, timer0 registers are described as examples.
- The registers for timer0 and timer2 have the same offset address but different base addresses. The registers for timer1 and timer3 have the same offset address but different base addresses.

Table 3-32 Summary of timer registers

Offset Address of Timer0/2	Offset Address of Timer1/3	Register	Description	Page
0x000	0x020	TIMERx_LOAD	Initial count value register	3-156
0x004	0x024	TIMERx_VALUE	Current count value register	3-157
0x008	0x028	TIMERx_CONTROL	Control register	3-157
0x00C	0x02C	TIMERx_INTCLR	Interrupt clear register	3-159
0x010	0x030	TIMERx_RIS	Raw interrupt status register	3-159
0x014	0x034	TIMERx_MIS	Masked interrupt status register	3-160
0x018	0x038	TIMERx_BGLOAD	Initial count value register in periodic mode	3-160

3.7.6 Register Description

TIMERx_LOAD

TIMERx_LOAD is the initial count value register. It is used to set the initial count value of each timer. Each timer (timer0–timer3) has one such register.

NOTE

- The minimum valid value written to TIMERx_LOAD is 1.
- When the value 0 is written to TIMERx_LOAD, the dual-timer module generates an interrupt immediately.

If values are written to TIMERx_BGLOAD and TIMERx_LOAD before the rising edge of TIMCLK enabled by TIMCLKENx reaches, the count value of the next rising edge of TIMCLK is changed to the value written to TIMERx_LOAD. As the value of TIMERx_BGLOAD changes when data is written to TIMERx_LOAD, the value returned after TIMERx_BGLOAD is read is the latest value that is written to TIMERx_LOAD and TIMERx_BGLOAD. When the timer works in periodic mode and the count value decreases to 0, the initial value is loaded from TIMERx_BGLOAD to continue counting.

Offset Address	Register Name	Total Reset Value
0x000	TIMER0_LOAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	timer0_load																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	timer0_load	Initial count value of timer0

TIMERx_VALUE

TIMERx_VALUE is the current count value register. It shows the current value of the counter that is decremented. Each timer (timer0–timer3) has one such register.

After a value is written to TIMERx_LOAD, TIMERx_VALUE immediately shows the newly loaded value of the counter in the PCLK domain without waiting for the clock edge of TIMCLK enabled by TIMCLKENx.

NOTE

When a timer is in 16-bit mode, the 16 upper bits of the 32-bit TIMERx_VALUE are not set to 0 automatically. If the timer is switched from 32-bit mode to 16-bit mode and no data is written to TIMERx_LOAD, the upper 16 bits of TIMERx_VALUE may be non-zero.

Offset Address	Register Name	Total Reset Value
0x004	TIMER0_VALUE	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	timer0_value																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RO	timer0_value	Current count value of timer0 that is decremented.

TIMERx_CONTROL

TIMERx_CONTROL is the control register. Each timer (timer0–timer3) has one such register.

NOTE

When the periodic mode is selected, TIMERx_CONTROL[timermode] must be set to 1 and TIMERx_CONTROL[oneshot] must be set to 0.

Offset Address	Register Name	Total Reset Value
0x008	TIMER0_CONTROL	0x0000_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								timeren	timermode	intenable	reserved	timerpre		timersize	oneshot
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved.
[7]	RW	timeren	Timer enable. 0: disabled 1: enabled
[6]	RW	timermode	Timer count mode. 0: free-running mode 1: periodic mode
[5]	RW	intenable	Raw interrupt mask. 0: masked 1: not masked
[4]	-	reserved	Reserved.
[3:2]	RW	timerpre	Prescaling factor configuration. 00: no prescaling. That is, the clock frequency of the timer is divided by 1 01: 4-level prescaling. That is, the clock frequency of the timer is divided by 16 10: 8-level prescaling. That is, the clock frequency of the timer is divided by 256 11: undefined. If the bits are set to 11, 8-level prescaling is considered. That is, the clock frequency of the timer is divided by 256.
[1]	RW	timersize	Counter select. 0: 16-bit counter 1: 32-bit counter
[0]	RW	oneshot	Count mode select. 0: periodic mode or free-running mode 1: one-shot mode

TIMERx_INTCLR

TIMERx_INTCLR is the interrupt clear register. The interrupt status of a counter is cleared after any operation is performed on this register. Each timer (timer0–timer3) has one such register.

CAUTION

This register is a write-only register. The timer clears interrupts when any value is written to this register. In addition, no value is recorded in this register and no default reset value is defined.

Offset Address	Register Name	Total Reset Value
0x00C	TIMER0_INTCLR	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	timer0_intclr																															
Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Access	Name	Description
[31:0]	WO	timer0_intclr	Writing this register clears the output interrupt of timer0.

TIMERx_RIS

TIMERx_RIS is the raw interrupt status register. Each timer (timer0–timer3) has one such register.

Offset Address	Register Name	Total Reset Value
0x010	TIMER0_RIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															timer0ris
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved. Writing this register has no effect and reading this register returns 0.
[0]	RO	timer0ris	Raw interrupt status of timer0. 0: No interrupt is generated. 1: An interrupt is generated.

TIMERx_MIS

TIMERx_MIS is the masked interrupt status register. Each timer (timer0–timer3) has one such register.

Offset Address	Register Name	Total Reset Value
0x014	TIMER0_MIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															timer0mis
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RO	timer0mis	Masked interrupt status of timer0. 0: The interrupt is invalid. 1: The interrupt is valid.

TIMERx_BGLOAD

TIMERx_BGLOAD is the initial count value register in periodic mode. Each timer (timer0–timer3) has one such register.

The TIMERx_BGLOAD register contains the initial count value of the timer. This register is used to reload an initial count value when the count value of the timer reaches 0 in periodic mode.

In addition, this register provides another method of accessing TIMERx_LOAD. The difference is that after a value is written to TIMERx_BGLOAD, the timer does not count starting from the input value immediately.

Offset Address	Register Name	Total Reset Value
0x018	TIMER0_BGLOAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	timer0bgload																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	timer0bgload	Initial count value of timer0. Note: This register differs from TIMERx_LOAD. For details, see the descriptions of TIMERx_LOAD.

3.8 Watchdog

3.8.1 Overview

The watchdog is used to transmit a reset signal to reset the entire system within a period after an exception occurs in the system.

3.8.2 Features

The watchdog has the following features:

- Provides a 32-bit internal down counter. The count clock source is configurable.
- Supports the configurable timeout interval, namely, initial count value.
- Locks registers to avoid any modification to them.
- Supports the generation of timeout interrupts.
- Supports the generation of reset signals.
- Supports the debugging mode.

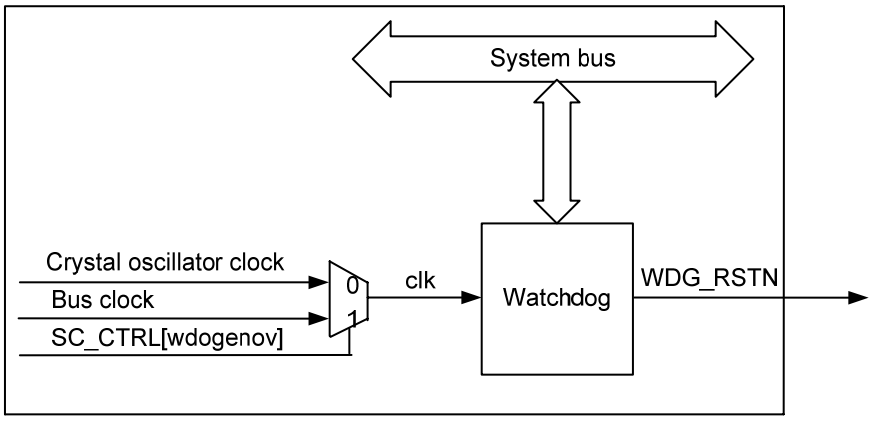
3.8.3 Function Description

Application Block Diagram

The system selects clocks for the watchdog by configuring SC_CTRL[wdogenov] and configures the parameter values of watchdog registers by using the system bus. The watchdog transmits interrupt requests to the system periodically. When the system does not respond to the interrupt requests (such as the suspend case), the watchdog transmits the WDG_RSTN reset signal to reset the system. In this way, the system running status is monitored.

Figure 3-22 shows the application block diagram of the watchdog.

Figure 3-22 Application block diagram of the watchdog



Function Principle

The watchdog works based on a 32-bit down counter. The initial value is loaded by WDG_LOAD. When the watchdog clock is enabled, the count value is decremented by 1 on the rising edge of each count clock. When the count value reaches 0, the watchdog generates an interrupt. On the next rising edge of the count clock, the counter reloads the initial value from WDG_LOAD and continues to count in decremental mode.

If the count value of the counter reaches 0 for the second time but the CPU does not clear the watchdog interrupt, the watchdog transmits the reset signal WDG_RSTN and the counter stops counting.

You can enable or disable the watchdog by configuring WDG_CONTROL as required. That is, you can control the watchdog whether to generate interrupts and reset signals.

- When the interrupt generation function is disabled, the watchdog counter stops counting.
- When the interrupt generation function is enabled again, the watchdog counter counts starting from the preset value of WDG_LOAD instead of the last count value. Before an interrupt is generated, the initial value can be reloaded.

The count clock of the watchdog can be a crystal oscillator clock or a bus clock so different count time ranges are available.

By configuring WDG_LOCK, you can disable the operation of writing to the internal registers of the watchdog.

- Writing 0x1ACC_E551 to WDG_LOCK to enable the write permission for all the registers of the watchdog.
- Writing any other values to WDG_LOCK to disable the write permission for all the registers of the watchdog except WDG_LOCK.

This feature avoids modifications to the watchdog registers by software. Therefore, the watchdog operation is not terminated by mistake by software when an exception occurs.

In debugging mode, the watchdog is disabled automatically to avoid the intervention to the normal debugging.

3.8.4 Operating Mode

Configuring the Frequency of the Count Clock

The system supports two types of watchdog count clocks: 3 MHz crystal oscillator clock and bus clock. The two clocks are selected by configuring SC_CTRL[wdogenov].

The count time T_{WDG} of the watchdog is calculated as follows:

$$T_{WDG} = Value_{WDG\_LOAD} \times \left(\frac{1}{f_{clk}} \right)$$

NOTE

The definition of each parameter in the preceding formula is as follows:

- T_{WDG} indicates the count time of the watchdog.
- $Value_{WDG\_LOAD}$ indicates the initial count value of the watchdog.
- f_{clk} indicates the frequency of the watchdog count clock.

The ranges of the count time of the watchdog under different clocks are as follows:

- When a 3 MHz crystal oscillator clock is selected, the count time ranges from 0s to 1400s.
- When a bus clock (such as a 100 MHz clock) is selected, the count time ranges from 0s to 42s.

Initializing the System

The watchdog counter stops counting after the system power-on reset. Before the system is initialized, the watchdog must be initialized and enabled. To initialize the watchdog, perform the following steps:

Step 1 Write to WDG_LOAD to set the initial count value.

Step 2 Write to WDG_CONTROL to enable the interrupt mask function and start the watchdog counter.

Step 3 Write to WDG_LOCK to lock the watchdog to avoid the watchdog settings being modified by the software by mistake.

----End

Processing an Interrupt

After an interrupt is received from the watchdog, the interrupt must be cleared in time and the initial count value must be reloaded to the watchdog to restart counting. A watchdog interrupt is processed as follows:

Step 1 Write 0x1ACC_E551 to WDG_LOCK to unlock the watchdog.

Step 2 Write to WDG_INTCLR to clear the watchdog interrupt and load the initial count value to the watchdog to restart counting.

Step 3 Write any other values rather than 0x1ACC_E551 to WDG_LOCK to lock the watchdog.

----End

Disabling the Watchdog

You can control the status of the watchdog by writing 0 or 1 to WDG_CONTROL[inten].

- 0: disabled
- 1: enabled

3.8.5 WatchDogRegister Summary

Table 3-33 describes watchdog registers.

Table 3-33 Summary of watchdog registers (base address: 0x2004_0000)

Offset Address	Register	Description	Page
0x0000	WDG_LOAD	Initial count value register	3-164
0x0004	WDG_VALUE	Current count value register	3-164
0x0008	WDG_CONTROL	Control register	3-165

0x000C	WDG_INTCLR	Interrupt clear register	3-165
0x0010	WDG_RIS	Raw interrupt register	3-166
0x0014	WDG_MIS	Masked interrupt status register	3-166
0x0018–0x0BFC	RESERVED	Reserved	-
0x0C00	WDG_LOCK	Lock register	3-166

3.8.6 Register Description

WDG_LOAD

WDG_LOAD is an initial count value register. It is used to configure the initial count value of the internal counter of the watchdog.

Offset Address	Register Name	Total Reset Value
0x0000	WDG_LOAD	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdg_load																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RW	wdg_load	Initial count value of the watchdog counter.

WDG_VALUE

WDG_VALUE is a current count value register It is used to read the current count value of the internal counter of the watchdog.

Offset Address	Register Name	Total Reset Value
0x0004	WDG_VALUE	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdogvalue																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RO	wdogvalue	Current count value of the watchdog counter.

WDG_CONTROL

WDG_CONTROL is a control register. It is used to enable or disable the watchdog and control the interrupt and reset functions of the watchdog.

Offset Address	Register Name	Total Reset Value
0x0008	WDG_CONTROL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														resen	inten
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	-	reserved	Reserved.
[1]	RW	resen	Output enable of the watchdog reset signal. 0: disabled 1: enabled
[0]	RW	inten	Output enable of the watchdog interrupt signal. 0: The counter stops counting, the current count value remains unchanged, and the watchdog is disabled. 1: The counter, interrupt and watchdog are enabled.

WDG_INTCLR

WDG_INTCLR is an interrupt clear register. It is used to clear watchdog interrupts so the watchdog can reload an initial value for counting. This register is write-only. When a value is written to this register, the watchdog interrupts are cleared. No written value is recorded in this register and no default reset value is defined.

Offset Address	Register Name	Total Reset Value
0x000C	WDG_INTCLR	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdg_intclr																															
Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Access	Name	Description
[31:0]	WO	wdg_intclr	Writing any value to this register clears the watchdog interrupts and enables the watchdog to reload an initial count value from WDG_LOAD to restart counting.

WDG_RIS

WDG_RIS is a raw interrupt status register. It shows the raw interrupt status of the watchdog.

Offset Address	Register Name	Total Reset Value
0x0010	WDG_RIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															wdogris
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RO	wdogris	Status of the raw interrupts of the watchdog. When the count value reaches 0, this bit is set to 1. 0: No interrupt is generated. 1: An interrupt is generated.

WDG_MIS

WDG_MIS is a masked interrupt status register. It shows the masked interrupt status of the watchdog.

Offset Address	Register Name	Total Reset Value
0x0014	WDG_MIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															wdogmis
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RO	wdogmis	Status of the masked interrupts of the watchdog. 0: No interrupt is generated or the interrupt is masked. 1: An interrupt is generated.

WDG_LOCK

WDG_LOCK is a lock register. It is used to control the write and read permissions for the watchdog registers.

Offset Address	Register Name	Total Reset Value
0x0C00	WDG_LOCK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdg_lock																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wdg_lock	Writing 0x1ACC_E551 to this register enables the write permission for all the registers. Writing other values disables the write permission for all the registers. When this register is read, the lock status rather than the written value of this register is returned. 0x0000_0000: The write permission is available (unlocked). 0x0000_0001: The write permission is unavailable (locked).

3.9 RTC

3.9.1 Overview

The RTC is used to display the time in real time and periodically generate alarms.

3.9.2 Features

The RTC has the following features:

- Provides a 40-bit up counter. Of the 40 bits, 16 bits are for counting days, five bits are for counting hours, six bits are for counting minutes, six bits are for counting seconds, and the other seven bits are for counting 10 ms.
- Provides a 100 Hz count clock.
- Allows you to configure the initial count value.
- Allows you to configure the match value.
- Supports the timeout interrupt.
- Supports soft reset.
- Automatically corrects the counting frequency based on the measured temperature.
- Provides the junction temperature of the position where the RTC is located.

3.9.3 Function Description

The RTC has a 40-bit up counter for counting days, hours, minutes, seconds, and 10 ms. The initial values are loaded from RTC_LR_10MS, RTC_LR_S, RTC_LR_M, RTC_LR_H, RTC_LR_D_L, and RTC_LR_D_H. This section assumes that the counter is divided into the day counter, hour counter, minute counter, second counter, and 10 ms counter. When the count value is equal to the values of RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H,

RTC_MR_D_L, and RTC_MR_D_H, the RTC generates an interrupt. Then, the counter continues to count in incremental mode on the rising edge of the next count clock.

By configuring RTC_IMSC, you can allow or forbid the RTC to generate interrupts. Note the following two cases:

- When the function of generating interrupts is disabled, the RTC counter continues to count in incremental mode and no interrupts are generated. RTC_MSC_INT shows the status of masked interrupts and RTC_RAW_INT shows the status of raw interrupts.
- When the function of generating interrupts is enabled, the RTC counter still counts in incremental mode. When the count value is equal to the values of RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, and RTC_MR_D_H, the RTC generates an interrupt.

The RTC uses a 100 Hz count clock and a 16-bit day counter. The value of the day counter can be used to reckon the specific year, month, and day.

3.9.4 Operating Mode

3.9.4.1 Count Clock Frequency

The RTC uses a 100 Hz count clock. The maximum RTC count time (T_{RTC}) is calculated as follows:

$T_{RTC} = 2^{16} = 65536$ days

3.9.4.2 Soft Reset

The RTC can be separately soft-reset by configuring RTC_POR_N. After soft reset, the value of each RTC configuration register is restored to its default value. Therefore, these registers must be initialized again.

To soft-reset the RTC, perform the following steps:

Step 1 Write 0 to RTC_POR_N.

Step 2 Wait 30 ms.

----End

3.9.4.3 Initializing the RTC

The system needs to initialize the RTC when the RTC is powered on for the first time. The initialization process is as follows:

Step 1 Configure RTC_POR_N to reset the RTC.

Step 2 Wait 30 ms.

Step 3 Configure RTC_IMSC to set the interrupt mask bit of the RTC.

Step 4 Configure RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, and RTC_MR_D_H to set the RTC match value.

Step 5 Configure RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, and RTC_MR_D_H to set the initial count value of the RTC.

Step 6 Set RTC_LORD to 1 to load the initial count value to the RTC counter.

Based on the 100 Hz count clock, the RTC counts starting from the values of RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, and RTC_MR_D_H. When the count value is equal to the values of RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, and RTC_MR_D_H, the RTC determines whether to generate an interrupt based on the settings of RTC_IMSC.

----End

3.9.4.4 Handling Interrupts

If the system receives an interrupt from the RTC, the configured time is reached. Then user-defined operations can be performed. The RTC counter, however, still counts in incremental mode. To clear an RTC interrupt, set RTC_INT_CLR to 1. To continue to configure time, write a new match value to RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, and RTC_MR_D_H.

3.9.4.5 Accessing RTC Registers

Internal RTC registers are located in the RTC module, not on the APB. The RTC registers on the APB are used only for accessing internal RTC registers.

To write to internal RTC registers, perform the following steps:

Step 1 Configure SPI_CLK_DIV.

This example assumes that the APB clock is 120 MHz and the expected SPI clock is 12 MHz. The configured value of SPI_CLK_DIV is calculated as follows: (120/12)/2 – 1 = 4 = 0x04. If you have configured SPI_CLK_DIV and do not want to change the SPI clock frequency, skip this step.

Step 2 Read SPI_RW bit[31] until it is 0.

Step 3 Configure SPI_RW.

The internal offset address for RTC_MR_10MS is 0x06. If you want to write 0x10 to RTC_MR_10MS, write 0x01060010 to SPI_RW. That is, spi_start is 1, spi_rw is 0, spi_add is 0x06, and spi_wdata is 0x10.

----End

To read internal RTC registers, perform the following steps:

Step 1 Configure SPI_CLK_DIV.

This step assumes that the APB clock is 120 MHz and the expected SPI clock is 12 MHz. The configured value of SPI_CLK_DIV is calculated as follows: (120/12)/2 – 1 = 4 = 0x04. If you have configured SPI_CLK_DIV and do not want to change the SPI clock frequency, skip this step.

Step 2 Read SPI_RW bit[31] until it is 0.

Step 3 Configure SPI_RW.

The internal offset address for RTC_MR_10MS is 0x06. If you want to read SPI_RW, write 0x01860000 to SPI_RW. That is, spi_start is 1, spi_rw is 0, and spi_add is 0x06.

Step 4 Read SPI_RW bit[31] until it is 0. SPI_RW [15:8] is the value that is returned after RTC_MR_10MS is read.

----End

3.9.4.6 Automatically Correcting the Counting Frequency Based on the Temperature

The crystal output frequency changes when the temperature changes. The relationship between the temperature and the output frequency of a specific crystal is defined by configuring registers during RTC initialization. The temperature is measured and the temperature calculated by using the correction algorithm is written at intervals (such as 1 minute). This ensures that the RTC generates a 100 Hz clock for counting. When the RTC correction algorithm is used, the temperature can be the value of the internal t_sensor or the externally measured temperature. When the temperature obtained by the internal t_sensor is selected, you need only to set a temperature update period for the t_sensor such as 1 minute, 4 minutes, 8 minutes, or 16 minutes without system intervention. When the temperature obtained by the internal t_sensor is selected, the system reads the internal chip temperature from the internal t_sensor at an interval of 1 minute, 4 minutes, 8 minutes, or 16 minutes. The ambient temperature that is equal to the read temperature minus the experience deviation is written to the OUTSIDE_TEMP register. When the externally measured temperature is selected, you can use the successive approximation register analog-to-digital converter (SAR ADC) and temperature-sensitive resistors or you can use only the external temperature sensor DS1820 or DS18B20. In this case, the system must measure the temperature and write the value to the external temperature register in a period. As the temperature update period allowed by the RTC is 1 minute, 4 minute, 8 minutes, or 16 minutes, you are advised to set the temperature measurement period to 1 minute, 4 minute, 8 minutes, or 16 minutes.

The following takes the external temperature sensor DS1820 as an example. To correct the counting frequency based on the temperature, perform the following steps:

Step 1 Set TEMP_SEL bit[1] to 0 and TEMP_SEL bit[0] to 1 to select an external temperature mode.

Step 2 Set RTC_SAR_CTRL[1:0] to 0 to set the temperature update period to 1 minute.

Step 3 Set INT_MASK to 0 to enable the temperature sensor measurement interrupt.

Step 4 Set CONVER_T to 1 to start the temperature measurement sensor.

Step 5 Wait until the temperature sensor measurement completion interrupt is generated.

Step 6 Set INT_CLEAR to 1 to clear the interrupt.

Step 7 Read T_VALUE and convert the temperature code words into the temperature code words supported by the t_sensor, and write the converted code words to OUTSIDE_TEMP.

Step 8 Wait 1 minute and repeat Step 4 to Step 8.

----End

3.9.5 Register Summary

Table 3-34 describes RTC APB registers.

Table 3-34 Summary of RTC APB registers (base address: 0x2006_0000)

Offset Address	Register	Description	Page
0x0000	SPI_CLK_DIV	SPI clock ratio register	3-175
0x0004	SPI_RW	SPI read/write register	3-176
0x0080	CONVER_T	Temperature sensor measurement control register	3-177
0x0084	CRC_EN	Temperature sensor measurement CRC check enable register	3-177
0x0088	INT_MASK	Temperature sensor measurement interrupt mask register	3-178
0x008C	INT_CLEAR	Temperature sensor measurement interrupt clear register	3-178
0x0090	BUSY	Temperature sensor measurement status register	3-179
0x0094	INT_RAW	Raw temperature sensor measurement interrupt status register	3-179
0x0098	INT_TCAP	Temperature sensor measurement interrupt status register	3-180
0x009C	T_VALUE	Temperature sensor measurement value register	3-180
0x00A0	FILTER_NUM	Filter glitch width configuration register	3-181

Table 3-35 describes the internal RTC registers.

Table 3-35 Summary of internal RTC registers (base address: 0x00)

Offset Address	Register	Description	Page
0x00	RTC_10MS_COUNT	Count value register for the RTC 10 ms counter	3-181
0x01	RTC_S_COUNT	Count value register for the RTC second counter	3-182
0x02	RTC_M_COUNT	Count value register for the RTC minute counter	3-182
0x03	RTC_H_COUNT	Count value register for the RTC hour counter	3-183
0x04	RTC_D_COUNT_L	Lower-8-bit count value register for the RTC day counter	3-183

Offset Address	Register	Description	Page
0x05	RTC_D_COUNT_H	Upper-8-bit count value register for the RTC day counter	3-184
0x06	RTC_MR_10MS	Match value register for the RTC 10 ms counter	3-184
0x07	RTC_MR_S	Match value register for the RTC second counter	3-185
0x08	RTC_MR_M	Match value register for the RTC minute counter	3-185
0x09	RTC_MR_H	Match value register for the RTC hour counter	3-186
0x0A	RTC_MR_D_L	Lower-8-bit match value register for the RTC day counter	3-186
0x0B	RTC_MR_D_H	Upper-8-bit match value register for the RTC day counter	3-187
0x0C	RTC_LR_10MS	Configured value register for the RTC 10 ms counter	3-187
0x0D	RTC_LR_S	Configured value register for the RTC second counter	3-188
0x0E	RTC_LR_M	Configured value register for the RTC minute counter	3-188
0x0F	RTC_LR_H	Configured value register for the RTC hour counter	3-189
0x10	RTC_LR_D_L	Lower-8-bit configured value register for the RTC day counter	3-189
0x11	RTC_LR_D_H	Upper-8-bit configured value register for the RTC day counter	3-190
0x12	RTC_LORD	RTC configured value loading enable register	3-190
0x13	RTC_IMSC	RTC interrupt enable register	3-191
0x14	RTC_INT_CLR	RTC interrupt clear register	3-191
0x15	RTC_MSC_INT	RTC mask interrupt status register.	3-192
0x16	RTC_RAW_INT	RTC raw interrupt status register	3-192
0x17	RTC_CLK	RTC output clock select register	3-193
0x18	RTC_POR_N	RTC reset control register	3-193
0x1A	RTC_SAR_CTRL	RTC internal t_sensor control register	3-194

Offset Address	Register	Description	Page
0x1C	TOT_OFFSET_L	Lower-8-bit corrected tot_offset register when the correction algorithm is used	3-195
0x1D	TOT_OFFSET_H	Upper-1-bit corrected tot_offset register when the correction algorithm is used	3-195
0x1E	TEMP_OFFSET	Temperature code word offset register corresponding to the correction input lookup table (LUT)	3-196
0x1F	OUTSIDE_TEMP	External ambient temperature register	3-196
0x20	DIE_TEMP	RTC internal t_sensor temperature register	3-196
0x21	TEMP_SEL	Correction algorithm input temperature source select register	3-197
0x22	LUT1	Temperature correction algorithm LUT1 register	3-198
0x23	LUT2	Temperature correction algorithm LUT2 register	3-198
0x24	LUT3	Temperature correction algorithm LUT3 register	3-199
0x25	LUT4	Temperature correction algorithm LUT4 register	3-199
0x26	LUT5	Temperature correction algorithm LUT5 register	3-199
0x27	LUT6	Temperature correction algorithm LUT6 register	3-200
0x28	LUT7	Temperature correction algorithm LUT7 register	3-200
0x29	LUT8	Temperature correction algorithm LUT8 register	3-200
0x2A	LUT9	Temperature correction algorithm LUT9 register	3-201
0x2B	LUT10	Temperature correction algorithm LUT10 register	3-201
0x2C	LUT11	Temperature correction algorithm LUT11 register	3-201
0x2D	LUT12	Temperature correction algorithm LUT12 register	3-202
0x2E	LUT13	Temperature correction algorithm LUT13 register	3-202

Offset Address	Register	Description	Page
0x2F	LUT14	Temperature correction algorithm LUT14 register	3-202
0x30	LUT15	Temperature correction algorithm LUT15 register	3-203
0x31	LUT16	Temperature correction algorithm LUT16 register	3-203
0x32	LUT17	Temperature correction algorithm LUT17 register	3-203
0x33	LUT18	Temperature correction algorithm LUT18 register	3-204
0x34	LUT19	Temperature correction algorithm LUT19 register	3-204
0x35	LUT20	Temperature correction algorithm LUT20 register	3-204
0x36	LUT21	Temperature correction algorithm LUT21 register	3-205
0x37	LUT22	Temperature correction algorithm LUT22 register	3-205
0x38	LUT23	Temperature correction algorithm LUT23 register	3-205
0x39	LUT24	Temperature correction algorithm LUT24 register	3-206
0x3A	LUT25	Temperature correction algorithm LUT25 register	3-206
0x3B	LUT26	Temperature correction algorithm LUT26 register	3-206
0x3C	LUT27	Temperature correction algorithm LUT27 register	3-207
0x3D	LUT28	Temperature correction algorithm LUT28 register	3-207
0x3E	LUT29	Temperature correction algorithm LUT29 register	3-207
0x3F	LUT30	Temperature correction algorithm LUT30 register	3-208
0x40	LUT31	Temperature correction algorithm LUT31 register	3-208
0x41	LUT32	Temperature correction algorithm LUT32 register	3-208

Offset Address	Register	Description	Page
0x42	LUT33	Temperature correction algorithm LUT33 register	3-209
0x43	LUT34	Temperature correction algorithm LUT34 register	3-209
0x44	LUT35	Temperature correction algorithm LUT35 register	3-209
0x45	LUT36	Temperature correction algorithm LUT36 register	3-210
0x46	LUT37	Temperature correction algorithm LUT37 register	3-210
0x47	LUT38	Temperature correction algorithm LUT38 register	3-210
0x48	LUT39	Temperature correction algorithm LUT39 register	3-211
0x49	LUT40	Temperature correction algorithm LUT40 register	3-211
0x4A	LUT41	Temperature correction algorithm LUT41 register	3-211
0x4B	LUT42	Temperature correction algorithm LUT42 register	3-212
0x4C	LUT43	Temperature correction algorithm LUT43 register	3-212
0x4D	LUT44	Temperature correction algorithm LUT44 register	3-212
0x4E	LUT45	Temperature correction algorithm LUT45 register	3-213
0x4F	LUT46	Temperature correction algorithm LUT46 register	3-213
0x50	LUT47	Temperature correction algorithm LUT47 register	3-213

3.9.6 APB Register Description

SPI_CLK_DIV

SPI_CLK_DIV is the SPI clock ratio register.

Offset Address	Register Name	Total Reset Value
0x0000	SPI_CLK_DIV	0x0000_003B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								spi_clk_div							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	1

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved.
[7:0]	RW	spi_clk_div	SPI clock ratio. The SPI clock frequency cannot be higher than 20 MHz. The value 12 MHz is recommended. The field value ranges from 1 to 255. The value of spi_clk_div is used to define the SPI RX and RX bit rates. The formula is as follows: FSPICLK = FAPBCLK/2 x (spi_clk_div + 1)FAPBCLK is the APB clock frequency. If the APB clock is 120 MHz and the expected SPI clock is 12 MHz, the configured value of spi_clk_div is calculated as follows: (120/12)/2 –1 = 4

SPI_RW

SPI_RW is the SPI read/write register.

Offset Address	Register Name	Total Reset Value
0x0004	SPI_RW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	spi_busy	reserved						spi_start	spi_rw	spi_add							spi_rdata								spi_wdata							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	spi_busy	SPI read/write status indicator. 0: The SPI is idle, and a new read/write operation can be initiated over the SPI. 1: A read/write operation is being performed over the SPI, and no new operation is allowed.
[30:25]	-	reserved	Reserved.
[24]	W1_PULSE	spi_start	SPI read/write start. Writing 1 automatically clears this field. Writing has no effect when spi_busy is 1. That is, no new SPI operation is started before the previous read/write operation is complete. If a start request is sent, hardware ignores this request.

[23]	RW	spi_rw	SPI operation type. 0: write 1: read
[22:16]	RW	spi_add	SPI operation address. The address range is 0–127.
[15:8]	RO	spi_rdata	Data read from the SPI.
[7:0]	RW	spi_wdata	Data to be written to the SPI.

CONVER_T

CONVER_T is the temperature sensor measurement control register.

Offset Address	Register Name	Total Reset Value
0x0080	CONVER_T	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															conver_t
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	conver_t	Temperature sensor measurement start. This field must be set to 1. 1: starts. Hardware automatically sets this field to 0 when the interrupt is cleared.

CRC_EN

CRC_EN is the temperature sensor measurement CRC check enable register.

Offset Address	Register Name	Total Reset Value
0x0084	CRC_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															crc_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	crc_en	Temperature sensor measurement CRC check enable. 0: disabled 1: enabled

INT_MASK

INT_MASK is the temperature sensor measurement interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x0088	INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															int_mask
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	int_mask	Temperature sensor measurement interrupt mask. 0: not masked 1: masked

INT_CLEAR

INT_CLEAR is the temperature sensor measurement interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x008C	INT_CLEAR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															int_clear
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	int_clear	Temperature sensor measurement interrupt clear. Writing 1 clears the interrupt. Hardware automatically sets this field to 0 after the interrupt is cleared.

BUSY

BUSY is the temperature sensor measurement status register.

Offset Address	Register Name	Total Reset Value
0x0090	BUSY	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															busy
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RO	busy	Temperature sensor measurement status. 0: ready 1: busy

INT_RAW

INT_RAW is the raw temperature sensor measurement interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0094	INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														int_err	get_tmprt_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	-	reserved	Reserved.
[1]	RO	int_err	Error interrupt.
[0]	RO	get_tmprt_int	Temperature measurement completion interrupt.

INT_TCAP

INT_TCAP is the temperature sensor measurement interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0098	INT_TCAP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															int_tcap
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RO	int_tcap	Masked interrupt status. 0: No interrupt is generated. 1: An interrupt is generated.

T_VALUE

T_VALUE is the temperature sensor measurement value register.

Offset Address	Register Name	Total Reset Value
0x009C	T_VALUE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				t_value											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	-	reserved	Reserved.
[11:0]	RO	t_value	Temperature measured by the sensor.

FILTER_NUM

FILTER_NUM is the filter glitch width configuration register.

Offset Address	Register Name	Total Reset Value
0x00A0	FILTER_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												filter_num			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	-	reserved	Reserved.
[3:0]	RW	filter_num	Filter glitch width for inputs. The glitch with the width of (N + 1) APB clocks is filtered.

3.9.7 Internal Register Description

RTC_10MS_COUNT

RTC_10MS_COUNT is the count value register for the RTC 10 ms counter.

Offset Address	Register Name	Total Reset Value
0x00	RTC_10MS_COUNT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved	rtc_10ms_count						
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7]	-	reserved	Reserved.
[6:0]	RO	rtc_10ms_count	RTC 10 ms counter value. It indicates the currently counted time. Its unit is 10 ms. The value range is 0–99.

RTC_S_COUNT

RTC_S_COUNT is the count value register for the RTC second counter.

Offset Address	Register Name	Total Reset Value
0x01	RTC_S_COUNT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved		rtc_s_count					
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	-	reserved	Reserved.
[5:0]	RO	rtc_s_count	RTC second counter value. It indicates the currently counted seconds. The value range is 0–59.

RTC_M_COUNT

RTC_M_COUNT is the count value register for the RTC minute counter.

Offset Address	Register Name	Total Reset Value
0x02	RTC_M_COUNT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved		rtc_m_count					
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	-	reserved	Reserved.
[5:0]	RO	rtc_m_count	RTC minute counter value. It indicates the currently counted minutes. The value range is 0–59.

RTC_H_COUNT

RTC_H_COUNT is the count value register for the RTC hour counter.

Offset Address	Register Name	Total Reset Value
0x03	RTC_H_COUNT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved			rtc_h_count				
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:5]	-	reserved	Reserved.
[4:0]	RO	rtc_h_count	RTC hour counter value. It indicates the currently counted hours. The value range is 0–23.

RTC_D_COUNT_L

RTC_D_COUNT_L is the lower-8-bit count value register for the RTC day counter.

Offset Address	Register Name	Total Reset Value
0x04	RTC_D_COUNT_L	0x00

Bit	7	6	5	4	3	2	1	0
Name	rtc_d_count_l							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	rtc_d_count_l	Lower eight bits of the RTC day counter value. This field works with RTC_D_COUNT_H to indicate the currently counted days. The day range is 0–65535.

RTC_D_COUNT_H

RTC_D_COUNT_H is the upper-8-bit count value register for the RTC day counter.

Offset Address	Register Name	Total Reset Value
0x05	RTC_D_COUNT_H	0x00

Bit	7	6	5	4	3	2	1	0
Name	rtc_d_count_h							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	rtc_d_count_h	Upper eight bits of the RTC day counter value. This field works with RTC_D_COUNT_L to indicate the currently counted day. The day range is 0–65535.

RTC_MR_10MS

RTC_MR_10MS is the match value register for the RTC 10 ms counter.

Offset Address	Register Name	Total Reset Value
0x06	RTC_MR_10MS	0x7F

Bit	7	6	5	4	3	2	1	0
Name	reserved	rtc_mr_10ms						
Reset	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[7]	RW	reserved	Reserved.
[6:0]	RW	rtc_mr_10ms	Match value of the RTC 10 ms counter. The value range is 0–99.

RTC_MR_S

RTC_MR_S is the match value register for the RTC second counter.

Offset Address	Register Name	Total Reset Value
0x07	RTC_MR_S	0x3F

Bit	7	6	5	4	3	2	1	0
Name	reserved		rtc_mr_s					
Reset	0	0	1	1	1	1	1	1

Bits	Access	Name	Description
[7:6]	RW	reserved	Reserved.
[5:0]	RW	rtc_mr_s	Match value of the RTC second counter. The value range is 0–59.

RTC_MR_M

RTC_MR_M is the match value register for the RTC minute counter.

Offset Address	Register Name	Total Reset Value
0x08	RTC_MR_M	0x3F

Bit	7	6	5	4	3	2	1	0
Name	reserved		rtc_mr_m					
Reset	0	0	1	1	1	1	1	1

Bits	Access	Name	Description
[7:6]	RW	reserved	Reserved.
[5:0]	RW	rtc_mr_m	Match value of the RTC minute counter. The value range is 0–59.

RTC_MR_H

RTC_MR_H is the match value register for the RTC hour counter.

Offset Address	Register Name	Total Reset Value
0x09	RTC_MR_H	0x1F

Bit	7	6	5	4	3	2	1	0
Name	reserved			rtc_mr_h				
Reset	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[7:5]	RW	reserved	Reserved.
[4:0]	RW	rtc_mr_h	Match value of the RTC hour counter. The value range is 0–23.

RTC_MR_D_L

RTC_MR_D_L is the lower-8-bit match value register for the RTC day counter.

Offset Address	Register Name	Total Reset Value
0x0A	RTC_MR_D_L	0xFF

Bit	7	6	5	4	3	2	1	0
Name	rtc_mr_d_l							
Reset	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[7:0]	RW	rtc_mr_d_l	Lower eight bits of the match value of the RTC day counter. This field works with RTC_MR_D_H to indicate the matched day. The day range is 0–65535.

RTC_MR_D_H

RTC_MR_D_H is the upper-8-bit match value register for the RTC day counter.

Offset Address	Register Name	Total Reset Value
0x0B	RTC_MR_D_H	0xFF

Bit	7	6	5	4	3	2	1	0
Name	rtc_mr_d_h							
Reset	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[7:0]	RW	rtc_mr_d_h	Upper eight bits of the match value of the RTC day counter. This field works with RTC_MR_D_L to indicate the matched day. The day range is 0–65535.

RTC_LR_10MS

RTC_LR_10MS is the configured value register for the RTC 10 ms counter.

Offset Address	Register Name	Total Reset Value
0x0C	RTC_LR_10MS	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved	rtc_lr_10ms						
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7]	RW	reserved	Reserved.
[6:0]	RW	rtc_lr_10ms	Configured value of the RTC 10 ms counter. The value range is 0–99.

RTC_LR_S

RTC_LR_S is the configured value register for the RTC second counter.

Offset Address	Register Name	Total Reset Value
0x0D	RTC_LR_S	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved		rtc_lr_s					
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RW	reserved	Reserved.
[5:0]	RW	rtc_lr_s	Configured value of the RTC second counter. The value range is 0–59.

RTC_LR_M

RTC_LR_M is the configured value register for the RTC minute counter.

Offset Address	Register Name	Total Reset Value
0x0E	RTC_LR_M	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved		rtc_lr_m					
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RW	reserved	Reserved.
[5:0]	RW	rtc_lr_m	Configured value of the RTC minute counter. The value range is 0–59.

RTC_LR_H

RTC_LR_H is the configured value register for the RTC hour counter.

Offset Address	Register Name	Total Reset Value
0x0F	RTC_LR_H	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved			rtc_lr_h				
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:5]	RW	reserved	Reserved.
[4:0]	RW	rtc_lr_h	Configured value of the RTC hour counter. The value range is 0–23.

RTC_LR_D_L

RTC_LR_D_L is the lower-8-bit configured value register for the RTC day counter.

Offset Address	Register Name	Total Reset Value
0x10	RTC_LR_D_L	0x00

Bit	7	6	5	4	3	2	1	0
Name	rtc_lr_d_l							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	rtc_lr_d_l	Lower eight bits of the configured value of the RTC day counter. This field works with RTC_LR_D_H to indicate the configured day. The day range is 0–255.

RTC_LR_D_H

RTC_LR_D_H is the upper-8-bit configured value register for the RTC day counter.

Offset Address	Register Name	Total Reset Value
0x11	RTC_LR_D_H	0x00

Bit	7	6	5	4	3	2	1	0
Name	rtc_lr_d_h							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	rtc_lr_d_h	Upper eight bits of the configured value of the RTC day counter. This field works with RTC_LR_D_L to indicate the configured day. The day range is 0–255.

RTC_LORD

RTC_LORD is the RTC configured value loading enable register.

Offset Address	Register Name	Total Reset Value
0x12	RTC_LORD	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved							rtc_load
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:1]	-	reserved	Reserved.
[0]	RW	rtc_load	RTC configured value loading enable. When the field is enabled, the RTC configured value will be loaded to the RTC accumulator. If software writes 1 to load the configured value, hardware will automatically set this field to 0 after successful loading.

RTC_IMSC

RTC_IMSC is the RTC interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x13	RTC_IMSC	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved							rtc_imsc
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:1]	-	reserved	Reserved.
[0]	RW	rtc_imsc	RTC timing interrupt enable. 0: disabled 1: enabled

RTC_INT_CLR

RTC_INT_CLR is the RTC interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x14	RTC_INT_CLR	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved							rtc_int_clr
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:1]	-	reserved	Reserved.
[0]	RW	rtc_int_clr	RTC timing interrupt clear. If software writes 1 to clear the interrupt, hardware will automatically set this field to 0 after the interrupt is successfully cleared.

RTC_MSC_INT

RTC_MSC_INT is the RTC mask interrupt status register.

Offset Address	Register Name	Total Reset Value
0x15	RTC_MSC_INT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved							mask_int
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:1]	-	reserved	Reserved.
[0]	RO	mask_int	Mask interrupt status.

RTC_RAW_INT

RTC_RAW_INT is the RTC raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x16	RTC_RAW_INT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved							raw_int
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:1]	-	reserved	Reserved.
[0]	RO	raw_int	Raw interrupt status.

RTC_CLK

RTC_CLK is the RTC output clock select register.

Offset Address	Register Name	Total Reset Value
0x17	RTC_CLK	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved						clk_out_sel	
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:2]	-	reserved	Reserved.
[1:0]	RW	clk_out_sel	Output test clock of the RTC. 00: output crystal oscillator clock 01: output corrected 100 Hz clock 1X: output 1 Hz clock

RTC_POR_N

RTC_POR_N is the RTC reset control register.

Offset Address	Register Name	Total Reset Value
0x18	RTC_POR_N	0x01

Bit	7	6	5	4	3	2	1	0
Name	reserved							rtc_por_n
Reset	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[7:1]	-	reserved	Reserved.
[0]	RW	rtc_por_n	RTC reset. This field is automatically set to 1 after the RTC is successfully reset. 0: reset

RTC_SAR_CTRL

RTC_SAR_CTRL is the RTC internal t_sensor control register.

Offset Address	Register Name	Total Reset Value
0x1A	RTC_SAR_CTRL	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved						sample_time	
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:2]	RW	reserved	Reserved.
[1:0]	RW	sample_time	Temperature update period 00: 1 minute 01: 4 minutes 10: 8 minutes 11: 16 minutes

TOT_OFFSET_L

TOT_OFFSET_L is the lower-8-bit corrected tot_offset register when the correction algorithm is used.

Offset Address	Register Name	Total Reset Value
0x1C	TOT_OFFSET_L	0x00

Bit	7	6	5	4	3	2	1	0
Name	tot_offset_l							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	tot_offset_l	Corrected tot_offset by using the correction algorithm. The value is expressed by complement codes –256 to +255. That is, tot_offset is 1990 + (–256 to +255) in the correction algorithm. This field value is the lower seven bits of tot_offset.

TOT_OFFSET_H

TOT_OFFSET_H is the upper-1-bit corrected tot_offset register when the correction algorithm is used.

Offset Address	Register Name	Total Reset Value
0x1D	TOT_OFFSET_H	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved							tot_offset_h
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:1]	-	reserved	Reserved.
[0]	RW	tot_offset_h	Corrected tot_offset by using the correction algorithm. The value is expressed by complement codes –256 to +255. That is, tot_offset is 1990 + (–256 to +255) in the correction algorithm. This field value is the upper one bit of tot_offset.

TEMP_OFFSET

TEMP_OFFSET is the temperature code word offset register corresponding to the correction input LUT.

Offset Address	Register Name	Total Reset Value
0x1E	TEMP_OFFSET	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved		temp_offset					
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	-	reserved	Reserved.
[5:0]	RW	temp_offset	Offset of the temperature code words that are input to the correction LUT. The value is expressed by the complement code and the value ranges from –32 to +31.

OUTSIDE_TEMP

OUTSIDE_TEMP is the external ambient temperature register.

Offset Address	Register Name	Total Reset Value
0x1F	OUTSIDE_TEMP	0x00

Bit	7	6	5	4	3	2	1	0
Name	outside_temp							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	outside_temp	Ambient temperature. The code word indicates –40°C to +140°C.

DIE_TEMP

DIE_TEMP is the RTC internal t_sensor temperature register.

Offset Address	Register Name	Total Reset Value
0x20	DIE_TEMP	0x00

Bit	7	6	5	4	3	2	1	0
Name	die_temp							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	die_temp	Internal chip temperature provided by the t_sensor in the RTC. The code word indicates –40°C to +140°C.

TEMP_SEL

TEMP_SEL is the correction algorithm input temperature source select register.

Offset Address	Register Name	Total Reset Value
0x21	TEMP_SEL	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved						fix_mode	temp_sel
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:2]	RW	reserved	Reserved.
[1]	RW	fix_mode	Correction algorithm input temperature source select. This field works with temp_sel. For details, see descriptions of the temp_sel field.

[0]	RW	temp_sel	Correction algorithm input temperature source select. This field parameter works with fix_mode. When the chip is powered on, the value meanings for {fix_mode, temp_sel} are as follows: 00: The correction circuit temperature is read from the DIE_TEMP register. 01: The correction circuit temperature is read from the OUTSIDE_TEMP register. 1X: The correction circuit temperature is read from the OUTSIDE_TEMP register. When the chip is powered off, the value meanings for {fix_mode, temp_sel} are as follows: 0X: The correction circuit temperature is read from the DIE_TEMP register. 1X: The correction circuit temperature is read from the OUTSIDE_TEMP register.

LUT1

LUT1 is the temperature correction algorithm LUT1 register.

Offset Address	Register Name	Total Reset Value
0x22	LUT1	0xAC

Bit	7	6	5	4	3	2	1	0
Name	lut1							
Reset	1	0	1	0	1	1	0	0

Bits	Access	Name	Description
[7:0]	RW	lut1	Temperature correction algorithm LUT1.

LUT2

LUT2 is the temperature correction algorithm LUT2 register.

Offset Address	Register Name	Total Reset Value
0x23	LUT2	0xB4

Bit	7	6	5	4	3	2	1	0
Name	lut2							
Reset	1	0	1	1	0	1	0	0

Bits	Access	Name	Description
[7:0]	RW	lut2	Temperature correction algorithm LUT2.

LUT3

LUT3 is the temperature correction algorithm LUT3 register.

Offset Address	Register Name	Total Reset Value
0x24	LUT3	0xBB

Bit	7	6	5	4	3	2	1	0
Name	lut3							
Reset	1	0	1	1	1	0	1	1

Bits	Access	Name	Description
[7:0]	RW	lut3	Temperature correction algorithm LUT3.

LUT4

LUT4 is the temperature correction algorithm LUT4 register.

Offset Address	Register Name	Total Reset Value
0x25	LUT4	0xC2

Bit	7	6	5	4	3	2	1	0
Name	lut4							
Reset	1	1	0	0	0	0	1	0

Bits	Access	Name	Description
[7:0]	RW	lut4	Temperature correction algorithm LUT4.

LUT5

LUT5 is the temperature correction algorithm LUT5 register.

Offset Address	Register Name	Total Reset Value
0x26	LUT5	0xC8

Bit	7	6	5	4	3	2	1	0
Name	lut5							
Reset	1	1	0	0	1	0	0	0

Bits	Access	Name	Description
[7:0]	RW	lut5	Temperature correction algorithm LUT5.

LUT6

LUT6 is the temperature correction algorithm LUT6 register.

Offset Address	Register Name	Total Reset Value
0x27	LUT6	0xCF

Bit	7	6	5	4	3	2	1	0
Name	lut6							
Reset	1	1	0	0	1	1	1	1

Bits	Access	Name	Description
[7:0]	RW	lut6	Temperature correction algorithm LUT6.

LUT7

LUT7 is the temperature correction algorithm LUT7 register.

Offset Address	Register Name	Total Reset Value
0x28	LUT7	0xD5

Bit	7	6	5	4	3	2	1	0
Name	lut7							
Reset	1	1	0	1	0	1	0	1

Bits	Access	Name	Description
[7:0]	RW	lut7	Temperature correction algorithm LUT7.

LUT8

LUT8 is the temperature correction algorithm LUT8 register.

Offset Address	Register Name	Total Reset Value
0x29	LUT8	0xDC

Bit	7	6	5	4	3	2	1	0
Name	lut8							
Reset	1	1	0	1	1	1	0	0

Bits	Access	Name	Description
[7:0]	RW	lut8	Temperature correction algorithm LUT8.

LUT9

LUT9 is the temperature correction algorithm LUT9 register.

Offset Address	Register Name	Total Reset Value
0x2A	LUT9	0xE2

Bit	7	6	5	4	3	2	1	0
Name	lut9							
Reset	1	1	1	0	0	0	1	0

Bits	Access	Name	Description
[7:0]	RW	lut9	Temperature correction algorithm LUT9.

LUT10

LUT10 is the temperature correction algorithm LUT10 register.

Offset Address	Register Name	Total Reset Value
0x2B	LUT10	0xE8

Bit	7	6	5	4	3	2	1	0
Name	lut10							
Reset	1	1	1	0	1	0	0	0

Bits	Access	Name	Description
[7:0]	RW	lut10	Temperature correction algorithm LUT10.

LUT11

LUT11 is the temperature correction algorithm LUT11 register.

Offset Address	Register Name	Total Reset Value
0x2C	LUT11	0xEE

Bit	7	6	5	4	3	2	1	0
Name	lut11							
Reset	1	1	1	0	1	1	1	0

Bits	Access	Name	Description
[7:0]	RW	lut11	Temperature correction algorithm LUT11.

LUT12

LUT12 is the temperature correction algorithm LUT12 register.

Offset Address	Register Name	Total Reset Value
0x2D	LUT12	0xF3

Bit	7	6	5	4	3	2	1	0
Name	lut12							
Reset	1	1	1	1	0	1	1	1

Bits	Access	Name	Description
[7:0]	RW	lut12	Temperature correction algorithm LUT12.

LUT13

LUT13 is the temperature correction algorithm LUT13 register.

Offset Address	Register Name	Total Reset Value
0x2E	LUT13	0xF9

Bit	7	6	5	4	3	2	1	0
Name	lut13							
Reset	1	1	1	1	1	0	0	1

Bits	Access	Name	Description
[7:0]	RW	lut13	Temperature correction algorithm LUT13.

LUT14

LUT14 is the temperature correction algorithm LUT14 register.

Offset Address	Register Name	Total Reset Value
0x2F	LUT14	0xFE

Bit	7	6	5	4	3	2	1	0
Name	lut14							
Reset	1	1	1	1	1	1	1	0

Bits	Access	Name	Description
[7:0]	RW	lut14	Temperature correction algorithm LUT14.

LUT15

LUT15 is the temperature correction algorithm LUT15 register.

Offset Address	Register Name	Total Reset Value
0x30	LUT15	0x03

Bit	7	6	5	4	3	2	1	0
Name	lut15							
Reset	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[7:0]	RW	lut15	Temperature correction algorithm LUT15.

LUT16

LUT16 is the temperature correction algorithm LUT16 register.

Offset Address	Register Name	Total Reset Value
0x31	LUT16	0x08

Bit	7	6	5	4	3	2	1	0
Name	lut16							
Reset	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[7:0]	RW	lut16	Temperature correction algorithm LUT16.

LUT17

LUT17 is the temperature correction algorithm LUT17 register.

Offset Address	Register Name	Total Reset Value
0x32	LUT17	0x0D

Bit	7	6	5	4	3	2	1	0
Name	lut17							
Reset	0	0	0	0	1	1	0	1

Bits	Access	Name	Description
[7:0]	RW	lut17	Temperature correction algorithm LUT17.

LUT18

LUT18 is the temperature correction algorithm LUT18 register.

Offset Address	Register Name	Total Reset Value
0x33	LUT18	0x12

Bit	7	6	5	4	3	2	1	0
Name	lut18							
Reset	0	0	0	1	0	0	1	0

Bits	Access	Name	Description
[7:0]	RW	lut18	Temperature correction algorithm LUT18.

LUT19

LUT19 is the temperature correction algorithm LUT19 register.

Offset Address	Register Name	Total Reset Value
0x34	LUT19	0x17

Bit	7	6	5	4	3	2	1	0
Name	lut19							
Reset	0	0	0	1	0	1	1	1

Bits	Access	Name	Description
[7:0]	RW	lut19	Temperature correction algorithm LUT19.

LUT20

LUT20 is the temperature correction algorithm LUT20 register.

Offset Address	Register Name	Total Reset Value
0x35	LUT20	0x1B

Bit	7	6	5	4	3	2	1	0
Name	lut20							
Reset	0	0	0	1	1	0	1	1

Bits	Access	Name	Description
[7:0]	RW	lut20	Temperature correction algorithm LUT20.

LUT21

LUT21 is the temperature correction algorithm LUT21 register.

Offset Address	Register Name	Total Reset Value
0x36	LUT21	0x1F

Bit	7	6	5	4	3	2	1	0
Name	lut21							
Reset	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[7:0]	RW	lut21	Temperature correction algorithm LUT21.

LUT22

LUT22 is the temperature correction algorithm LUT22 register.

Offset Address	Register Name	Total Reset Value
0x37	LUT22	0x23

Bit	7	6	5	4	3	2	1	0
Name	lut22							
Reset	0	0	1	0	0	0	1	1

Bits	Access	Name	Description
[7:0]	RW	lut22	Temperature correction algorithm LUT22.

LUT23

LUT23 is the temperature correction algorithm LUT23 register.

Offset Address	Register Name	Total Reset Value
0x38	LUT23	0x27

Bit	7	6	5	4	3	2	1	0
Name	lut23							
Reset	0	0	1	0	0	1	1	1

Bits	Access	Name	Description
[7:0]	RW	lut23	Temperature correction algorithm LUT23.

LUT24

LUT24 is the temperature correction algorithm LUT24 register.

Offset Address	Register Name	Total Reset Value
0x39	LUT24	0x2B

Bit	7	6	5	4	3	2	1	0
Name	lut24							
Reset	0	0	1	0	1	0	1	1

Bits	Access	Name	Description
[7:0]	RW	lut24	Temperature correction algorithm LUT24.

LUT25

LUT25 is the temperature correction algorithm LUT25 register.

Offset Address	Register Name	Total Reset Value
0x3A	LUT25	0x2E

Bit	7	6	5	4	3	2	1	0
Name	lut25							
Reset	0	0	1	0	1	1	1	0

Bits	Access	Name	Description
[7:0]	RW	lut25	Temperature correction algorithm LUT25.

LUT26

LUT26 is the temperature correction algorithm LUT26 register.

Offset Address	Register Name	Total Reset Value
0x3B	LUT26	0x32

Bit	7	6	5	4	3	2	1	0
Name	lut26							
Reset	0	0	1	1	0	0	1	0

Bits	Access	Name	Description
[7:0]	RW	lut26	Temperature correction algorithm LUT26.

LUT27

LUT27 is the temperature correction algorithm LUT27 register.

Offset Address	Register Name	Total Reset Value
0x3C	LUT27	0x35

Bit	7	6	5	4	3	2	1	0
Name	lut27							
Reset	0	0	1	1	0	1	0	1

Bits	Access	Name	Description
[7:0]	RW	lut27	Temperature correction algorithm LUT27.

LUT28

LUT28 is the temperature correction algorithm LUT28 register.

Offset Address	Register Name	Total Reset Value
0x3D	LUT28	0x38

Bit	7	6	5	4	3	2	1	0
Name	lut28							
Reset	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[7:0]	RW	lut28	Temperature correction algorithm LUT28.

LUT29

LUT29 is the temperature correction algorithm LUT29 register.

Offset Address	Register Name	Total Reset Value
0x3E	LUT29	0x3B

Bit	7	6	5	4	3	2	1	0
Name	lut29							
Reset	0	0	1	1	1	0	1	1

Bits	Access	Name	Description
[7:0]	RW	lut29	Temperature correction algorithm LUT29.

LUT30

LUT30 is the temperature correction algorithm LUT30 register.

Offset Address	Register Name	Total Reset Value
0x3F	LUT30	0x3E

Bit	7	6	5	4	3	2	1	0
Name	lut30							
Reset	0	0	1	1	1	1	1	0

Bits	Access	Name	Description
[7:0]	RW	lut30	Temperature correction algorithm LUT30.

LUT31

LUT31 is the temperature correction algorithm LUT31 register.

Offset Address	Register Name	Total Reset Value
0x40	LUT31	0x41

Bit	7	6	5	4	3	2	1	0
Name	lut31							
Reset	0	1	0	0	0	0	0	1

Bits	Access	Name	Description
[7:0]	RW	lut31	Temperature correction algorithm LUT31.

LUT32

LUT32 is the temperature correction algorithm LUT32 register.

Offset Address	Register Name	Total Reset Value
0x41	LUT32	0x43

Bit	7	6	5	4	3	2	1	0
Name	lut32							
Reset	0	1	0	0	0	0	1	1

Bits	Access	Name	Description
[7:0]	RW	lut32	Temperature correction algorithm LUT32.

LUT33

LUT33 is the temperature correction algorithm LUT33 register.

Offset Address	Register Name	Total Reset Value
0x42	LUT33	0x45

Bit	7	6	5	4	3	2	1	0
Name	lut33							
Reset	0	1	0	0	0	1	0	1

Bits	Access	Name	Description
[7:0]	RW	lut33	Temperature correction algorithm LUT33.

LUT34

LUT34 is the temperature correction algorithm LUT34 register.

Offset Address	Register Name	Total Reset Value
0x43	LUT34	0x48

Bit	7	6	5	4	3	2	1	0
Name	lut34							
Reset	0	1	0	0	1	0	0	0

Bits	Access	Name	Description
[7:0]	RW	lut34	Temperature correction algorithm LUT34.

LUT35

LUT35 is the temperature correction algorithm LUT35 register.

Offset Address	Register Name	Total Reset Value
0x44	LUT35	0x4A

Bit	7	6	5	4	3	2	1	0
Name	lut35							
Reset	0	1	0	0	1	0	1	0

Bits	Access	Name	Description
[7:0]	RW	lut35	Temperature correction algorithm LUT35.

LUT36

LUT36 is the temperature correction algorithm LUT36 register.

Offset Address	Register Name	Total Reset Value
0x45	LUT36	0x4B

Bit	7	6	5	4	3	2	1	0
Name	lut36							
Reset	0	1	0	0	1	0	1	1

Bits	Access	Name	Description
[7:0]	RW	lut36	Temperature correction algorithm LUT36.

LUT37

LUT37 is the temperature correction algorithm LUT37 register.

Offset Address	Register Name	Total Reset Value
0x46	LUT37	0x4D

Bit	7	6	5	4	3	2	1	0
Name	lut37							
Reset	0	1	0	0	1	1	0	1

Bits	Access	Name	Description
[7:0]	RW	lut37	Temperature correction algorithm LUT37.

LUT38

LUT38 is the temperature correction algorithm LUT38 register.

Offset Address	Register Name	Total Reset Value
0x47	LUT38	0x4F

Bit	7	6	5	4	3	2	1	0
Name	lut38							
Reset	0	1	0	0	1	1	1	1

Bits	Access	Name	Description
[7:0]	RW	lut38	Temperature correction algorithm LUT38.

LUT39

LUT39 is the temperature correction algorithm LUT39 register.

Offset Address	Register Name	Total Reset Value
0x48	LUT39	0x50

Bit	7	6	5	4	3	2	1	0
Name	lut39							
Reset	0	1	0	1	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	lut39	Temperature correction algorithm LUT39.

LUT40

LUT40 is the temperature correction algorithm LUT40 register.

Offset Address	Register Name	Total Reset Value
0x49	LUT40	0x51

Bit	7	6	5	4	3	2	1	0
Name	lut40							
Reset	0	1	0	1	0	0	0	1

Bits	Access	Name	Description
[7:0]	RW	lut40	Temperature correction algorithm LUT40.

LUT41

LUT41 is the temperature correction algorithm LUT41 register.

Offset Address	Register Name	Total Reset Value
0x4A	LUT41	0x52

Bit	7	6	5	4	3	2	1	0
Name	lut41							
Reset	0	1	0	1	0	0	1	0

Bits	Access	Name	Description
[7:0]	RW	lut41	Temperature correction algorithm LUT41.

LUT42

LUT42 is the temperature correction algorithm LUT42 register.

Offset Address	Register Name	Total Reset Value
0x4B	LUT42	0x53

Bit	7	6	5	4	3	2	1	0
Name	lut42							
Reset	0	1	0	1	0	0	1	1

Bits	Access	Name	Description
[7:0]	RW	lut42	Temperature correction algorithm LUT42.

LUT43

LUT43 is the temperature correction algorithm LUT43 register.

Offset Address	Register Name	Total Reset Value
0x4C	LUT43	0x54

Bit	7	6	5	4	3	2	1	0
Name	lut43							
Reset	0	1	0	1	0	1	0	0

Bits	Access	Name	Description
[7:0]	RW	lut43	Temperature correction algorithm LUT43.

LUT44

LUT44 is the temperature correction algorithm LUT44 register.

Offset Address	Register Name	Total Reset Value
0x4D	LUT44	0x54

Bit	7	6	5	4	3	2	1	0
Name	lut44							
Reset	0	1	0	1	0	1	0	0

Bits	Access	Name	Description
[7:0]	RW	lut44	Temperature correction algorithm LUT44.

LUT45

LUT45 is the temperature correction algorithm LUT45 register.

Offset Address	Register Name	Total Reset Value
0x4E	LUT45	0x55

Bit	7	6	5	4	3	2	1	0
Name	lut45							
Reset	0	1	0	1	0	1	0	1

Bits	Access	Name	Description
[7:0]	RW	lut45	Temperature correction algorithm LUT45.

LUT46

LUT46 is the temperature correction algorithm LUT46 register.

Offset Address	Register Name	Total Reset Value
0x4F	LUT46	0x55

Bit	7	6	5	4	3	2	1	0
Name	lut46							
Reset	0	1	0	1	0	1	0	1

Bits	Access	Name	Description
[7:0]	RW	lut46	Temperature correction algorithm LUT46.

LUT47

LUT47 is the temperature correction algorithm LUT47 register.

Offset Address	Register Name	Total Reset Value
0x50	LUT47	0x55

Bit	7	6	5	4	3	2	1	0
Name	lut47							
Reset	0	1	0	1	0	1	0	1

Bits	Access	Name	Description
[7:0]	RW	lut47	Temperature correction algorithm LUT47.

3.10 Power Management and Low-Power Mode Control

3.10.1 Overview

In low-power mode, the power consumption of the chip is reduced effectively. The Hi3518 reduces its power consumption in the following low-power control modes:

- System operating mode control

  In all operating modes except the normal mode, the power consumption is reduced to some extent. You can select different operating modes according to the actual power consumption and function requirements.
- Clock gating and clock frequency adjustment

  The clock disabling function is used to disable unnecessary clocks to reduce the power consumption of the chip. In addition, the frequency of the system working clock can be adjusted. That is, when the function requirement is met, you can adjust the clock frequency to reduce the power consumption of the chip.
- Module low-power control

  When a module is idle, it can be disabled or switched to low-power mode to reduce the power consumption.
- DDR low-power control

  The power consumption of the DDRC and related pins can be controlled dynamically. You can enable this function to reduce the power consumption of the chip. You can also enable the self-refresh function of the DDR to reduce the power consumption of the entire product.

3.10.2 Operating Modes of the System

The system provides two operating modes.

- Normal operating mode: This mode maps to the normal running mode of the system.

  When the system works in normal mode, you can control the clock frequency and set the modules and DDR to low-power mode to reduce the power consumption.
- Standby operating mode: This mode maps to the slow and doze running modes of the system.
  - In standby mode, the system works at the clock with low frequency, and the clocks of most idle modules are disabled. Therefore, the power consumption is low.
  - When the system works in slow or doze mode, you can power off the power supplies of idle modules to reduce the power consumption.

  The mode can be switched by configuring the system controller. For details, see section 3.4 "System Controller."

3.10.3 Clock Gating and Clock Frequency Adjustment

The system supports clock gating of each module. When a module is idle, its clock can be disabled to reduce the power consumption of the chip. For details about the process, see the description in the section of "clock gating" of each module.

In normal mode, the system can adjust its working frequency to reduce the power consumption of the chip. To adjust the system working frequency, perform the following steps:

- Disable the service module to prevent it from accessing the DDR.
- Enable the system to run in the off-chip memory.

When DDRC_SREFCTRL[sr_seq] is set to a valid value, the DDRC forces the DDRn SDRAM to enter the self-refresh mode.

Step 1 Set the value of SC_PLLCTRL[27:3] to the stable time of the PLL.

Step 2 Configure PERI_CRG0 and PERI_CRG1 to control the clock divider of the PLL

Step 3 Wait a moment and configure DDRC_SREFCTRL to enable the DDRC to exit the self-refresh mode based on the configuration requirements of the DDRC.

Step 4 The program starts to run in the DDR.

----End

The working frequencies of some modules can also be adjusted separately. This reduces the power consumption of the system further. For details about the clock source of each module, see section 3.2.3 "Clock Configuration."

3.10.4 Module Low-Power Control

Most modules including USB 2.0 host, Video DAC, and PLL modules support low-power operating modes. For details, see the descriptions of the system controller, VDP, and clocks.

- Low-power control for the USB host module:
  - Disable the USB 2.0 host clock by setting PERI_CRG46 bit[7] to 0.
  - Powered off the USB PHY by setting PERIPHCTRL21 bit[22] to 1.
- The audio CODEC can control the power consumption of each channel. When the corresponding bit of PERIPHCTRL14 bit[31:26] is set to 1, the channel power is turned off. Then the audio DAC works in low-power mode.
- When the video DAC is not used, you can:
  - Power off the detection circuit of the video DAC by setting PERIPHCTRL4 bit[6] to 1.
  - Power off the video DAC channel by setting PERIPHCTRL4 bit[7] to 1.
  - Power off the video DAC by setting PERIPHCTRL4 bit[8] to 1.
- The PLL also supports the low-power mode. If the PLL is not used, it can be disabled to switch the system to low-power mode.
  - If the APLL is not used, you can set PERI_CRG1[apll_pd] to 0 to disable it. Then the APLL enters the low-power mode.
  - If VPLL0 is not used, you can set PERI_CRG3[vpll0_pd] to 0 to disable it. Then VPLL0 enters the low-power mode.
  - If BPLL is not used, you can set PERI_CRG5 bit[21] to 0 to disable it. Then BPLL enters the low-power mode.
  - If the EPLL is not used, you can set PERI_CRG9 bit[21] to 0 to disable it. Then the EPLL enters the low-power mode.

3.10.5 DDR Low-Power Control

For details about the low-power control mode of the DDRC, see the description of "Configuring the Low-Power Mode" in section 4.1.4 "Operating Mode."

3.11 Processor Subsystem

The ARM926EJ-S processor has the following features:

- Uses the 32-bit ARM v5TEJ and 5-stage pipeline to be compatible with the 32-bit ARM and the 16-bit Thumb instruction sets.
- Supports the embedded enhanced DSP instructions.
- Supports Java.
- Provides the independent 16 KB instruction cache, 16 KB data cache, and 4-way set associative cache. The cache line size is 32 bytes. The data cache supports configurable write-back and write-through operations.
- Provides the caches that support configurable pseudo-random or round-robin replacement algorithm.
- Provides independent instructions and data bus interfaces.
- The ratio of the operating frequency of the bus clock to that of system clock of the ARM926EJ-S can be set to 1:2. The two clocks have the same phase.
- Includes an MMU that supports multiple open operating systems, such as VxWorks, Linux, WindowCE, and PalmOS.
- Provides an independent 2-KB ITCM.
- Uses the little endian mode.
- Supports FIQs and IRQs.
- Supports the JTAG debugging interface.
- Supports dynamic and static power management.
- Supports a maximum of 440 MHz working frequency.

Contents

Figures

Tables

4 Memory Interfaces

4.1 DDRC

4.1.1 Overview

The DDR2/DDR3 SDRAM controller (DDRC) controls the access to the DDR2 SDRAM or DDR3 SDRAM. In the following sections, DDR2/DDR3 SDRAM is expressed as DDRn SDRAM.

NOTE

The Hi3518 provides one DDRC that supports 16-bit DDRs.

4.1.2 Features

The DDRC has the following features:

- Provides one DDRn SDRAM CS space and supports 16-bit data bus and at most 14-bit address bus.
- Supports a maximum of 2 Gbit in 16-bit mode.
- Supports the 440 MHz DDRn SDRAM bus.
- Supports various low-power modes for the DDRn SDRAM including power down and self refresh.
- Supports burst4 and burst8 transfer modes for the DDR2 SDRAM and burst8 transfer mode for the DDR3 SDRAM.

4.1.3 Function Description

4.1.3.1 Application Block Diagram

By using the DDRC, the master devices such as the CPU of the system-on-chip (SoC) can access the external DDRn SDRAM. After the timing parameter registers of the DDRC are configured by using the CPU, the DDRC supports the DDR2 SDRAM and DDR3 SDRAM complying with the JEDEC (JESD79) standard. Table 4-1 lists the mainstream DDR2 SDRAMs supported by the DDRC. The descriptions in Table 4-1 are based on the working frequencies of DDR2 SDRAMs. The restrictions such as the capacity are not taken into account.

Table 4-1 DDR2 SDRAMs supported by the DDRC

Vendor	200 MHz	333 MHz	400 MHz
JESD79 (DDR2 Standard)	DDR2-400 DDR2-533 DDR2-667 DDR2-800	DDR2-667 DDR2-800	DDR2-800
Micron	-5E DDR2-400 -37E DDR2-533 -3 DDR2-667 -3E DDR2-667 -25 DDR2-800 -25E DDR2-800	-3 DDR2-667 -3E DDR2-667 -25 DDR2-800 -25E DDR2-800	-25 DDR2-800 -25E DDR2-800
ELPIDA	-4A DDR2-400 -5C DDR2-533 -6E DDR2-667 -6C DDR2-667 -8E DDR2-800	-6E DDR2-667 -6C DDR2-667 -8E DDR2-800	-8E DDR2-800
Hynix	-E3 DDR2-400 -C4 DDR2-533 -Y4 DDR2-667 -Y5 DDR2-667 -S5 DDR2-800 -S6 DDR2-800	-Y4 DDR2-667 -Y5 DDR2-667 -S5 DDR2-800 -S6 DDR2-800	-S5 DDR2-800 -S6 DDR2-800
Samsung	-CC DDR2-400 -D5 DDR2-533 -E6 DDR2-667 -E7 DDR2-800	-E6 DDR2-667 -E7 DDR2-800	-E7 DDR2-800

NOTE

- The DDRC supports the SDRAMs complying with the JESD79 standard. In different operating modes, the DDRC supports only the SDRAMs whose frequencies are higher than or equal to its working frequency. You can refer to this feature to select the SDRAMs provided by other vendors.
- You need to select DDR2 SDRAMs provided by each vendor according to their working frequencies. In practice, the DDR2 SDRAMs with the same working frequency may differ from each other in capacity or bit width. A DDR2 SDRAM is supported by the DDRC as long as its working frequency is listed in Table 4-1. The capacity and bit width of a DDR2 SDRAM are selected based on the actual application scenario of the chip.

Table 4-2 lists the DDR3 SDRAMs supported by the DDRC.

Table 4-2 DDR3 SDRAMs supported by the DDRC

Vendor	400 MHz	533 MHz	800 MHz
JESD79 (DDR3 Standard)	DDR3-800 DDR3-1066 DDR3-1333	None	None

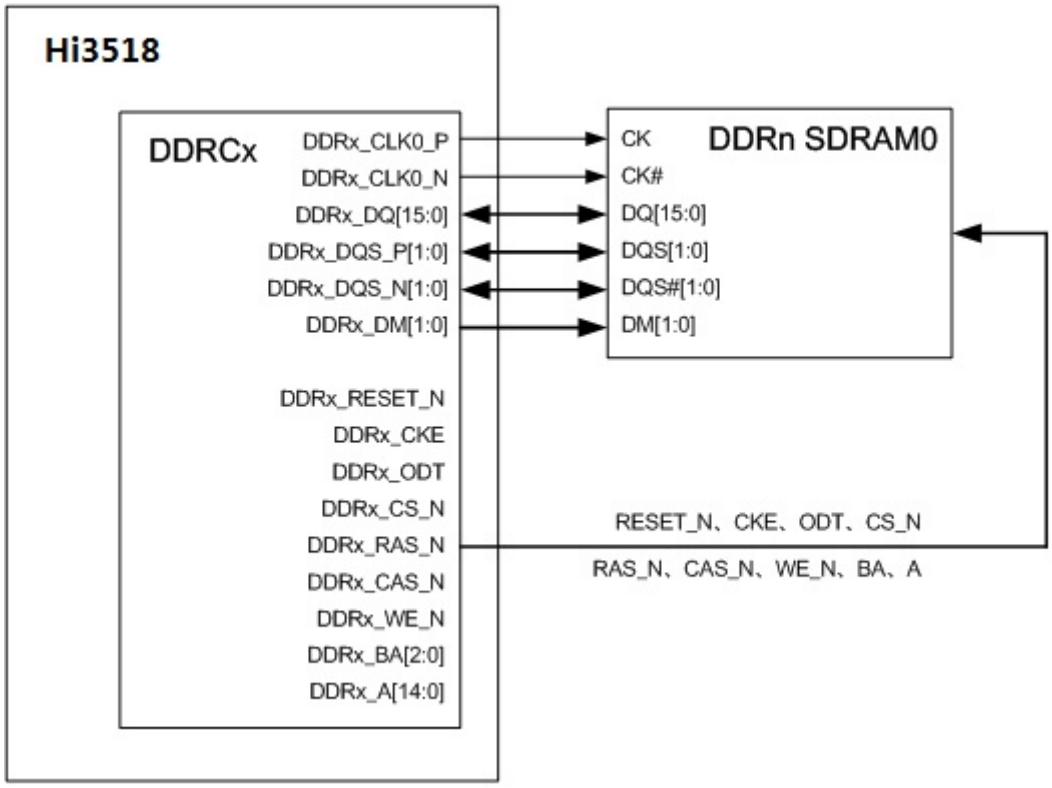
NOTE

If the working frequency of the DDRC is 400 MHz, the frequencies of all the DDR3s can be decreased to 400 MHz.

The supported memory types are based on the JEDEC standard.

The DDRC supports 16-bit interconnection modes. In 16-bit mode, the DDRC connects to one 16-bit or two 8-bit DDRn SDRAMs. The following is an example using one 16-bit DDRn SDRAMs. Figure 4-1 shows the diagram of connecting a DDRC to two 16-bit DDRn SDRAMs.

Figure 4-1 Diagram of connecting a DDRC to one DDRn SDRAMs in 32-bit mode



Description:
The letter *x* in DDRCx or DDRx indicates the DDR controller ID and its value is 0 or 1.
DDRn SDRAMx is a 16-bit memory.
The command control signals of the DDRC include DDRx_CKE, DDRx_RESET_N, DDRx_ODT, DDRx_CS_N, DDRx_RAS_N, DDRx_CAS_N, DDRx_WE_N, DDRx_BA[2:0] and DDRx_A[13:0]. These signals connect to the command control signals of the DDRn SDRAM. That is, the command control bus of the DDRC is connected in one-driven-one mode.
If the capacity of a DDR2 SDRAM is smaller than 1 Gbit, the output address signal DDRx_BA[2] of the

DDRC is floated.
DDRx_RESET_N is floated in DDR2 mode.

4.1.3.2 Function Principle

As the timings of the DDRC interface comply with the JESD79 standard, the DDRC can access the data of the DDRn SDRAM and control the status of the DDRn SDRAM by transmitting the command words of the DDRn SDRAM. The DDRC can also read and write the DDRn SDRAM, automatically refresh the DDRn SDRAM, and control the power consumption of the DDRn SDRAM.

Command Truth Value Table

The DDRC can read, write, and control the command words of the DDRn SDRAM. Table 4-3 lists the command truth values of the DDRC.

Table 4-3 Command truth values of the DDRC

FUNCTION	DDRn_CKE	DDRn_CSN	DDRn_RASN	DDRn_CASN	DDRn_WEN	DDRn_ADR			DDRn_BA
						11	AP(10)	9:0	
DESELECT	H	H	X	X	X	X	X	X	X
ACTIVE	H	L	L	H	H	V	V	V	V
READ	H	L	H	L	H	V	V	V	V
WRITE	H	L	H	L	L	V	V	V	V
PRECHARGE	H	L	L	H	L	X	L	X	V
PRECHARGE ALL	H	L	L	H	L	X	H	X	X
AUTO REFRESH	H	L	L	L	H	X	X	X	X
SELF REFRESH	L	L	L	L	H	X	X	X	X
MODE REGISTER SET	H	L	L	L	L	V	V	V	V
ZQCL	H	L	H	H	L	X	H	X	X
ZQCS	H	L	H	H	L	X	L	X	X

NOTE

- H: high level; L: low level; V: valid; X: ignored.
- ZQ calibration long (ZQCL): start a ZQ calibration on the DDR3 SDRAM when it is initialized during power on.

- ZQ calibration short (ZQCS): start a calibration on the DDR3 SDRAM when its ambient environment is changed.

Auto Refresh

When DDRC_TIMING2[taref] is set to a non-zero value, the DDRC refreshes the DDRn SDRAM by generating a periodic auto refresh command automatically At normal temperature, the DDR2 SDRAM must be auto-refreshed for 8192 times within 64 ms. That is, the auto-refresh cycle is 7.8 µs. The relationship between the configured value (Taref) of DDRC_TIMING2 [taref] and the auto-refresh cycle T (T = 7.8 µs or 3.9 µs) is as follows:

Taref ≤ T/(16 x DDR clock cycle)

When DDRC_TIMING2[taref] is configured, the internal counter of the DDRC loads the taref value automatically and then counts in decremental mode. When the count value reaches 0, the DDRC initiates an auto-refresh operation and the counter reloads the taref value to count.

Low-Power Management

The DDRC supports two types of low-power management: common low-power mode and auto-refresh low-power mode.

When the system is idle (the DDR is not read or written over the DDRC bus interface for a period), the DDRn SDRAM enters the common low-power mode automatically.

When the system needs to be switched to the standby mode, you can force the DDRn SDRAM to enter the self-refresh low-power mode by configuring DDRC_SREFCTRL[sr_req]. In this mode, the power consumption of the DDRn SDRAM is minimized, but the data in the DDRn SDRAM is retained. In this case, the system cannot access the DDRn SDRAM.

Arbitration Mechanism

The DDRC uses the priority scheduling algorithm. That is, the DDRC adds priority attributes to bus commands by configuring DDRC_QOS[pri], and schedules the commands based on the priority attributes. In this way, the DDR2 SDRAM is accessed in a high-effective manner. The DDRC can also add delay attributes to bus commands by configuring DDRC_QOS[qos_en] and DDRC_QOSx[qos], and ensure delay response to the commands based on the delay priority scheduling algorithm. The DDRC adds the traffic control attributes to bus interfaces by configuring DDRC_FLUX[flux_port_en] and DDRC_FLUX[flux]. When the delay time is not consumed, traffic of each bus interface is allocated to ensure that the bandwidth of each interface when the DDRC is accessed in busy hours.

Address Mapping Mode

The DDRC can convert the access address of the system bus into that of the DDRn SDRAM. By configuring DDRC_RNKCFG[mem_map], DDRC_RNKCFG[mem_row], and DDRC_RNKCFG[mem_col], the DDRC converts the system bus address into the address of the DDRn SDRAM based on the address mapping algorithm.

The following example describes the mapping algorithm of the system bus address and the address of the DDRn SDRAM. Assume that the system bus address is BUSADR[28:0], the valid address is BUSADR[m – 1:0], and the address of the DDRn SDRAM is DDRADR[13:0]. When DDRADR[13:0] serves as the row address, its valid address is DDRROW[x – 1:0]; when it serves as the column address, its valid address is DDRCOL[y –

1:0]. In addition, the bank address of the DDR is DDRBA[z – 1:0] and the width of the storage data bus of the DDRC is DW. In this case, the address mappings are as follows:

- When DDRC_RNKCFG[mem_map] is set to 2b00, the mapping mode of the row-bank-column (RBC) is as follows:

  BUSADR[m – 1: 0] = {DDRROW[x – 1: 0], DDRBA[z – 1:0], DDRCOL[y – 1:0], DW{b0}}

- When DDRC_RNKCFG[mem_map] is set to 2b01, the mapping mode of the RBC is as follows:

  BUSADR[m – 1:0] = {DDR_BA[z – 1:0], DDRROW[x – 1:0], DDRCOL[y – 1:0], DW{b0}}

In the preceding expressions, the condition of the equation m = x + y + z + DW is true.

When the DDRC is in 16-bit mode, the value of DW is 1.

Table 4-4 describes the mapping of the system bus address and the DDRn SDRAM address when DDRC_RNKCFG[mem_map] is set to 2b00 and A10 acts as the AP function bit of the DDR.

To be specific, Table 4-4 describes the address mapping in RBC mode. That is, the address is mapped in RBC mode based on the preceding expressions.

Table 4-4 DDRC address mapping in 16-bit mode

Memory Type	**Row Address Width**	**Column Address Width**	**DDR BA**			**Row Address or Column Address**	**DDR ADR**						
Mbitxbw			**2**	**1**	**0**		**13**	**12**	**11**	**10/AP**	**9**	**8**	**[7:0]**
256 Mbits 4 banks													
16x16	13	9	None	11	10	Row address	None	24	23	22	21	20	[19:12]
						Column address	None	None	None	AP	None	9	[8:1]
512 Mbits 4 banks													
32x16	13	10	None	12	11	Row address	None	25	24	23	22	21	[20:13]
						Column address	None	None	None	AP	10	9	[8:1]
1024 Mbits 8 bank													

Memory Type	Row Address Width	Column Address Width	DDR BA			Row Address or Column Address	DDR ADR						
Mbitxbw			2	1	0		13	12	11	10/AP	9	8	[7:0]
64x16	13	10	13	12	11	Row address	None	26	25	24	23	22	[21:14]
						Column address	None	None	None	AP	10	9	[8:1]
2048 Mbits 8 bank													
128x16	14	10	13	12	11	Row address	27	26	25	24	23	22	[21:14]
						Column address	None	None	None	AP	10	9	[8:1]

4.1.4 Operating Mode

4.1.4.1 Clock Gating

After the system enters the low-power mode, the working clock of the DDRC can be disabled. Before the system restores to the normal mode, the working clock of the DDRC must be enabled.

To disable the working clock after the DDRC enters the low-power mode, perform the following steps:

1. Enable the system to run in the flash memory or the TCM.
2. Set DDRC_SREFCTRL[sr_req] to 1 to request to enter the self-refresh mode.
3. Query DDRC_STATUS[in_sr] until its value is 1. It indicates that the DDRC enters the low-power mode.
4. Disable the DDR clock by setting DDRC_PUB_DSGCR [ckoe] to 0x0.
5. Disable the DDRC clock.
6. Enter the low-power mode.

----End

To enable the working clock after the DDRC exits the low-power mode, perform the following steps:

1. Enable the DDRC clock when the system runs in normal mode.

2. Set DDRC_CONFIG1 to 0x0040_0785, and enable the DDR clock by setting DDRC_PUB_DSGCR [ckoe] to 0x1.
3. Set DDRC_PUB_PIR to 0x0000_000F.
4. Wait 20 μs until the DLL is locked and impedance calibration is complete.
5. Set DDRC_SREFCTRL[sr_req] to 0 to request to exit the self-refresh mode.
6. Query DDRC_STATUS[in_sr] until its value is 0. It indicates that the DDRC exits the low-power mode.
7. The system accesses the DDR properly.

----End

4.1.4.2 Soft Reset

The DDRC does not support separate soft reset. It can be reset only by a global soft reset. After reset, the DDRn SDRAM must be reinitialized according to the following initialization processes.

4.1.4.3 Initializing the DDR2 SDRAM

After power-on, the system can access the DDR2 SDRAM only when the DDR2 SDRAM is initialized. Before initializing the DDR2 SDRAM, note the following:

- Power on the DDR2 SDRAM according to the JEDEC standard. That is, you must power on VDD, VDDQ, VREF, and VTT in sequence.
- Initialize the DDR2 SDRAM after the system runs in normal mode.

In DDRC 16-bit mode, this section assumes that the memory consists of two 1 Gbit DDR2 SDRAMs (each with 8-bit bus width). To initialize the DDR2 SDRAM, perform the following steps:

1. Wait more than 200 μs.
2. Set DDRC_CONFIG0 to 0x8000_0500. This indicates that the DDRC mode is set to 16-bit DDR2 SDRAM mode, and DDRC_CONFIG0[pd_en] is set to 0 to disable the power-down mode. Set DDRC_CONFIG1 to 0x0000_0785. This indicates that DDRC_CONFIG1DDRC_CONFIG1[read_mode] and DDRC_CONFIG1DDRC_CONFIG1[ecc_en] are set to 0x0, and DDRC_CONFIG1DDRC_CONFIG1[wr_rcv_mode], DDRC_CONFIG1DDRC_CONFIG1[clkratio], and DDRC_CONFIG1DDRC_CONFIG1[zqc_en] are set to 0x1.

   NOTE
   - The low-power mode is disabled by default after power-on reset. During initialization, the functions of automatically entering the low-power mode and disabling clocks must be disabled. In normal mode, you are advised to enable the low-power control function to reduce power consumption.
   - DDRC_CONFIG1[wr_rcv_mode] must be set to 1. Otherwise, the chip bus may be suspended.
3. Set DDRC_TIMING2 bit[31:11], and set DDRC_TIMING2[taref] is set to 0x000 to disable the auto-refresh function.
4. Set DDRC_RNKCFG0 to DDRC_RNKCFG3 to 0x0000_0132, mapping mode of the bus address to R-B-C-DW, AP to A10, column address width to 10, and row address width to 14.

5. Set DDRC_TIMING0, DDRC_TIMING1, and DDRC_TIMING3 based on the working frequency and requirements of the DDR2 SDRAM.
6. Set DDRC_BASEADDR to 0x8000_0000.
7. Configure DDRC_QOSCFG0, and DDRC_QOS (DDRC_RDQOS0 to DDRC_RDQOS15) as required. You can also set these registers to default values.
8. Set DDRC_ODTCFG[wodt0] to 0x1 and DDRC_ODTCFG[rodt0] to 0x0.
9. Set DDRC_DTRCTRL[train_mode] and DDRC_DTRCTRL[train_en] to 0 to enable the synopys training mode.
10. Set DDRC_SREFCTRL to 0x0 to exit the self-refresh mode.
11. Query DRC_STATUS[in_sr] until it is 0 or the software waits more than 1 μs.
12. Set DDRC_PUB_PIR to 0x8000_0000 to perform initialization in PHY bypass mode after power-on.
13. Wait 500 ns, and query DDRC_PUB_PGSR [idone] until it is 1.
14. Configure the DDR PHY control registers DDRC_PUB_PGCR and DDRC_PUB_DSGCR as required, and set DDRC_PUB_DXNGCR (blanes = 0) and DDRC_PUB_DXNGCR (blanes = 1) to 0x0000_0E81.
15. Configure the DDR PHY time parameters registers DDRC_PUB_PTR0, DDRC_PUB_PTR1, DDRC_PUB_PTR2, DDRC_PUB_DTPR0, DDRC_PUB_DTPR1, and DDRC_PUB_DTPR2 based on the working frequency of the DDR2 SDRAM.
16. Based on the working frequency and requirements of the DDR2 SDRAM, configure the DDRC_PUB_MR0, DDRC_PUB_MR1, DDRC_PUB_MR2, and DDRC_PUB_MR3 registers to set the column address signal (CAS) latency, write recovery latency, burst length, output drive impedance, and input ODT impedance of the DDR2 SDRAM.

    NOTE

    - The values of the CAS latency and DDRC_TIMING1[cl] must be the same.
    - DDRC_PUB_MR0, DDRC_PUB_MR1, DDRC_PUB_MR2, and DDRC_PUB_MR3 are mode register MRS, extended mode register (EMRS1), extended mode register 2 (EMRS2), and extended mode register 3 (EMRS3) respectively. When configuring these registers, you need to configure only A15–A0 bits (actual valid bits are A13–A0) of the mode register described in the DDR2 SDRAM user manual. The upper three bits A18–A16 of the mode register indicate the bank address and do not need to be configured. Note that the bank address for some DDRn SDRAMs corresponds to bits A17−A15.
17. Set DDRC_PUB_PIR to 0x0000_00FF to start PHY utility block (PUB) initialization. This indicates that the fields DDRC_PUB_PIR[init], DDRC_PUB_PIR[dllsrst], DDRC_PUB_PIR[dlllock], DDRC_PUB_PIR[zcal], DDRC_PUB_PIR[itmsrst], DDRC_PUB_PIR[dramrst], DDRC_PUB_PIR[draminit], and DDRC_PUB_PIR[qstrn] are set to 1.
18. Wait 500 ns and query DDRC_PUB_PGSR[idone] until it is 1.
19. Configure DDRC_TIMING2[taref] based on the working frequency and requirements of the DDR2 SDRAM, and enable the auto-refresh function.

----End

After the preceding steps are complete, the DDR2 SDRAM works properly.

4.1.4.4 Initializing the DDR3 SDRAM

After power on, the system can access the DDR3 SDRAM only when the DDR3 SDRAM is initialized. Before initializing the DDR3 SDRAM, note the following:

- Power on the DDR3 SDRAM by following the JEDEC standard. That is, you must power on VDD, VDDQ, VREF, and VTT in sequence.
- Initialize the DDR3 SDRAM after the system runs in normal mode.

In DDRC 16-bit mode, this section assumes that the memory consists of two 1 Gbit DDR3 SDRAMs (each with 8-bit bus bit width). To initialize the DDR3 SDRAM, perform the following steps:

1. Wait more than 200 μs.
2. Set DDRC_CONFIG0 to 0x8000_0600. This indicates that the DDRC mode is set to 16-bit DDR3 SDRAM mode, and DDRC_CONFIG0[pd_en] is set to 0x0 to disable the power-down mode. Set DDRC_CONFIG1 to 0x0000_0785. This indicates that DDRC_CONFIG1[read_mode] and DDRC_CONFIG1[ecc_en] are set to 0x0, and DDRC_CONFIG1[wr_rcv_mode], DDRC_CONFIG1[clkratio], and DDRC_CONFIG1[zqc_en] are set to 0x1.

   NOTE
   - The low-power mode is disabled by default after power-on reset. During initialization, the functions of automatically entering the low-power mode and disabling clocks must be disabled. In normal mode, you are advised to enable the low-power control function to reduce power consumption.
   - DDRC_CONFIG1[wr_rcv_mode] must be set to 1. Otherwise, the chip bus may be suspended.
3. Set DDRC_TIMING2 bit[31:11] based on the working frequency and requirements of the DDR3 SDRAM, and set DDRC_TIMING2[taref] to 0x000 to disable the auto-refresh function.
4. Set DDRC_CTRL to 0x0001 to enable the DDR3 SDRAM to exit the reset status.

   NOTE
   - The DDR3 SDRAM exits the reset status during global reset after power-on or during reset deassertion. The DDR PHY is in PUB mode after reset by default. In this case, the DDR PHY controls the DDR3 SDRAM, including resetting, reading, or writing to the DDR3. When the DDR PHY is reset, the signal ram_rst_n for setting the DDR3 SDRAM is high by default.
   - Set DDRC_CTRL to 0x0001 to prevent the DDRC reset signal from being transmitted to the DDR3 SDRAM when the DDR PHY exits the PUB mode.
5. Set DDRC_CONFIG0 to 0x8C34_0600.

   Set DDRC_RNKCFG0 to DDRC_RNKCFG3 to 0x0000_0132, mapping mode of the bus address to R-B-C-DW, AP to A10, column address width to 10, and row address width to 14.
6. Set DDRC_TIMING0, DDRC_TIMING1, and DDRC_TIMING3 based on the working frequency and requirements of the DDR3 SDRAM.
7. Set DDRC_BASEADDR to 0x8000_0000.
8. Configure DDRC_QOSCFG0, and DDRC_QOS (DDRC_RDQOS0 to DDRC_RDQOS15) as required. You can also set these registers to default values.
9. Set DDRC_ODTCFG[wodt0] to 0x1 and DDRC_ODTCFG[rodt0] to 0x0.
10. Set DDRC_DTRCTRL[train_mode] and DDRC_DTRCTRL[train_en] to 0 to enable the synopys training mode.

11. Set DDRC_SREFCTRL to 0x0 to exit the self-refresh mode.
12. Query DRC_STATUS[in_sr] until it is 0 or the software waits more than 1 μs.
13. Set DDRC_PUB_PIR to 0x8000_0000 to perform initialization in PHY bypass mode after power-on.
14. Wait 500 ns, and query DDRC_PUB_PGSR [idone] until it is 1.
15. Configure the DDR PHY control registers DDRC_PUB_PGCR and DDRC_PUB_DSGCR as required, and set DDRC_PUB_DXNGCR (blanes = 0) and DDRC_PUB_DXNGCR (blanes = 1) to 0x0000_0E81.
16. Configure the DDR PHY time parameters registers DDRC_PUB_PTR0, DDRC_PUB_PTR1, DDRC_PUB_PTR2, DDRC_PUB_DTPR0, DDRC_PUB_DTPR1, and DDRC_PUB_DTPR2 based on the working frequency of the DDR3 SDRAM.
17. Based on the working frequency and requirements of the DDR3 SDRAM, configure the DDRC_PUB_MR0, DDRC_PUB_MR1, DDRC_PUB_MR2, and DDRC_PUB_MR3 registers to set the CAS latency, CAS write latency, write recovery latency, burst length, output drive impedance, and input ODT impedance of the DDR3 SDRAM.

    NOTE

    - The values of the CAS latency and DDRC_TIMING1[cl] must be the same.
    - The values of the CAS write latency and DDRC_TIMING1[wl] must be the same.
    - DDRC_PUB_MR0, DDRC_PUB_MR1, DDRC_PUB_MR2, and DDRC_PUB_MR3 are mode register MRS, extended mode register (EMRS1), extended mode register 2 (EMRS2), and extended mode register 3 (EMRS3) respectively. When configuring these registers, you need to configure only A15–A0 bits (actual valid bits are A13–A0) of the mode register described in the DDR3 SDRAM user manual. The upper three bits A18–A16 of the mode register indicate the bank address and do not need to be configured. Note that the bank address for some DDRn SDRAMs corresponds to bits A17−A15.
18. Set DDRC_PUB_PIR to 0x0000_00FF to start PUB initialization. This indicates that fields [init], [dllsrst], [dlllock], [zcal], [itmsrst], [dramrst], [draminit], and [qstrn] are set to 1.
19. Wait 500 ns and query DDRC_PUB_PGSR[idone] until it is 1.
20. Configure DDRC_TIMING2 [taref], and enable the auto-refresh function.

----End

After the preceding steps are complete, the DDR3 SDRAM works properly.

4.1.4.5 Low-Power Configuration

The DDRC supports two types of low-power modes for the DDRn SDRAM: DDRn SDRAM power-down mode and DDRn SDRAM self-refresh mode.

When DDRC_CONFIG0[pd_en] and DDRC_CONFIG0[pd_prd] are set to valid values, the DDRC automatically forces the DDRn SDRAM to enter the low-power mode if the system is idle. When DDRC_CONFIG0[pd_en] is set to 1 and the DDRC does not access the DDRn SDRAM withinDDRC_CONFIG0[pd_prd] bus clock cycles, the DDRC forces the DDRn SDRAM to enter the low-power mode.

When DDRC_SREFCTRL[sr_seq] is set to a valid value, the DDRC forces the DDRn SDRAM to enter the self-refresh mode. When DDRC_SREFCTRL[sr_req] is set to 1, the DDRC forces the DDRn SDRAM to enter the self-refresh mode without responding to the bus requests after completing the current access operation.

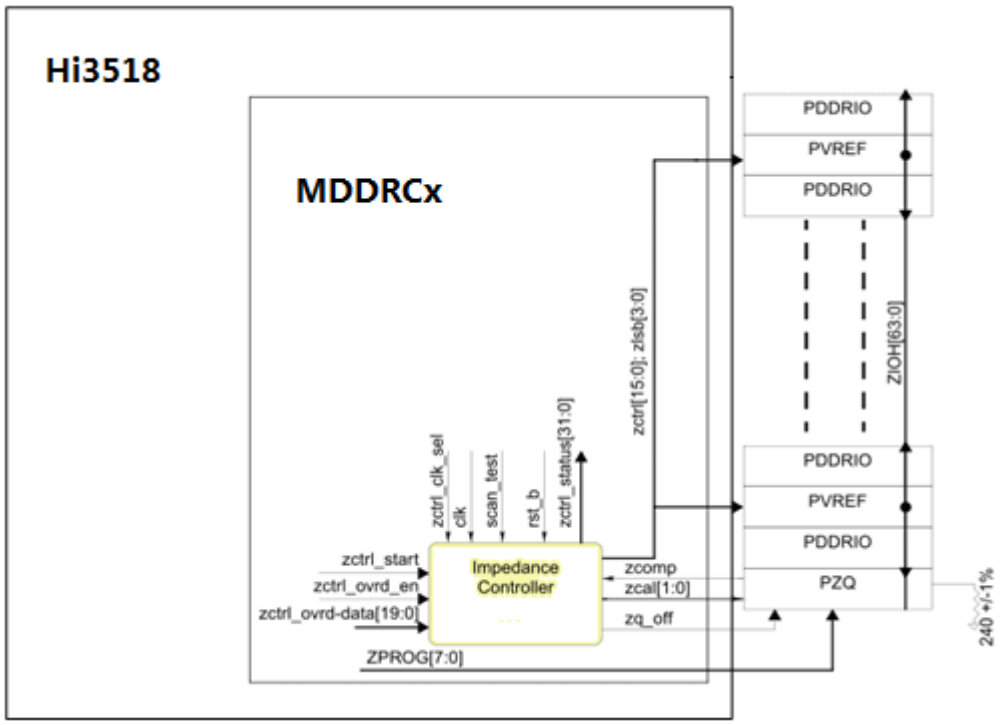
4.1.4.6 DDR I/Os Impedance Configuration

When the DDRn SDRAM is used, DDRC automatically calibrates the TX impedance and RX impedance of the DDR IOs.

You can enable the automatic calibration function by configuring DDRC_PUB_PIR [zcal]. Automatic calibration is enabled by default. To configure the automatic calibration function, set DDRC_PUB_ZQ_CTRL0 [zden] to 1'b1 and configure DDRC_PUB_ZQ_CTRL0 [zdata] as required.

To implement the calibration function, 2% reference resistors need to be connected to chip I/Os. Figure 4-2 shows how the reference resistors are connected.

Figure 4-2 Diagram of connecting the reference resistors to the DDR I/Os



NOTE

- The letter x in DDRx indicates the DDR controller ID and its value is 0 or 1.
- You are advised to select a 1% 240 Ω resistor as the DDR I/O reference resistor.
- You are advised to select a 240 Ω RX resister in DDR3 mode and a 300 Ω RX resister in DDR2 mode.

4.1.5 Register Summary

Table 4-5 describes the value ranges and meanings of the variables in the offset addresses for registers.

Table 4-5 Variables in the offset addresses for registers

Variable	Value Range	Description
blanes	0–1	Number of byte lanes supported by the DDRC
id0	0–15	Number of registers supported by the DDRC
ports	0–2	Number of AXI ports

Table 4-6 describes the DDRC registers.

Table 4-6 Summary of the DDRC registers (base address: 0x2011_0000)

Offset Address	Register	Description	Page
0x000	DDRC_STATUS	DDRC status register	4-16
0x004	DDRC_SREFCTRL	DDRC self-refresh control register	4-17
0x008	DDRC_INITCTRL	DDRC initialization control register	4-17
0x010	DDRC_CTRL	DDRC control register	4-18
0x014	DDRC_EMRS01	DDRC mode configuration register	4-18
0x018	DDRC_EMRS23	DDRC extended mode configuration register	4-19
0x01C	DDRC_CONFIG0	DDRC function configuration register 0	4-20
0x020	DDRC_CONFIG1	DDRC function configuration register 1	4-21
0x024	DDRC_CMDCFG	DDRC command configuration register	4-24
0x028	DDRC_CMDEXE	DDRC software configuration command start register	4-25
0x02C	DDRC_RNKCFG	DDR feature configuration register	4-25
0x040	DDRC_BASEADDR	DDR space base address configuration register	4-27
0x050	DDRC_TIMING0	DDR timing parameter register 0	4-27
0x054	DDRC_TIMING1	DDR timing parameter register 1	4-28
0x058	DDRC_TIMING2	DDR timing parameter register 2	4-29
0x05C	DDRC_TIMING3	DDR timing parameter register 3	4-30
0x060	DDRC_TIMING4	DDR timing parameter register 4	4-31
0x0A0	DDRC_DTRADDR	DDRC gating training address configuration register	4-32
0x0A4	DDRC_DTRDATA0	DDRC gating training data configuration register 0	4-32

Offset Address	Register	Description	Page
0x0A8	DDRC_DTRDATA1	DDRC gating training data configuration register 1	4-33
0x0AC	DDRC_DTRCTRL	DDRC gating training control register	4-33
0x0B0	DDRC_DTRPRD	DDRC gating track period configuration register	4-35
0x0B4	DDRC_DTRGATE	DDRC gating phase position register	4-35
0x0C4	DDRC_DTRLAT	DDRC gating period position register	4-36
0x0D4	DDRC_DTRSTATUS	DDRC gating status register	4-36
0x0F0	DDRC_AXISTATUS	DDRC interface status register	4-37
0x0F4	DDRC_ODTCFG	DDR ODT feature configuration register	4-38
0x100	DDRC_QOSCFG0	DDRC QoS algorithm configuration register 0	4-39
0x150+0x4 x id0	DDRC_QOS	DDRC command priority configuration register	4-39
0x200+0x4 x ports	DDRC_FLUX	DDRC AXI port bandwidth traffic control configuration register	4-40
0x240	DDRC_TEST0	DDRC test status register	4-41
0x244	DDRC_TEST1	DDRC test status register	4-42
0x248	DDRC_TEST2	DDRC test status register	4-42
0x24C	DDRC_TEST3	DDRC test status register	4-43
0x250	DDRC_TEST4	DDRC test status register	4-43
0x260	DDRC_TEST7	DDRC performance measurement control register	4-43
0x264	DDRC_TEST8	DDRC write command count register	4-44
0x268	DDRC_TEST9	DDRC read command count register	4-45
0x26C	DDRC_TEST10	DDRC DMC wait command count register	4-45
0x280	DDRC_TEST12	DDRC test status register	4-46
0x284	DDRC_TEST13	DDRC reorder test status register 1	4-46
0x288	DDRC_TEST14	DDRC reorder test status register 2	4-46
0x28C	DDRC_TEST15	DDRC reorder test status register 3	4-47

Table 4-7 describes the DDR PHY registers.

Table 4-7 Summary of the DDR PHY registers (base address: 0x2012_0000)

Offset Address	Register	Description	Page
0x404	DDRC_PUB_PIR	PHY initialization register	4-47
0x408	DDRC_PUB_PGCR	PHY general configuration	4-49
0x40C	DDRC_PUB_PGSR	PHY general configuration	4-52
0x410	DDRC_PUB_DLLGCR	DLL general control register	4-53
0x414	DDRC_PUB_ACDLLCR	AC DLL control register	4-56
0x418	DDRC_PUB_PTR0	PHY timing register 0	4-58
0x41C	DDRC_PUB_PTR1	PHY timing register 1	4-59
0x420	DDRC_PUB_PTR2	PHY timing register 2	4-59
0x424	DDRC_PUB_ACIOCR	AC I/O configuration	4-60
0x428	DDRC_PUB_DXCCR	DATX8 common configuration register	4-62
0x42C	DDRC_PUB_DSGCR	DDR system general configuration register	4-63
0x430	DDRC_PUB_DCR	DRAM configuration register	4-66
0x434	DDRC_PUB_DTPR0	DRAM Timing parameters register 0	4-67
0x438	DDRC_PUB_DTPR1	DRAM Timing parameters register 1	4-69
0x43C	DDRC_PUB_DTPR2	DRAM Timing parameters register 2	4-71
0x440	DDRC_PUB_MR0	Mode register 0	4-72
0x444	DDRC_PUB_MR1	Mode register 1	4-72
0x448	DDRC_PUB_MR2	Mode register 2	4-73
0x44C	DDRC_PUB_MR3	Mode register 3	4-73
0x450	DDRC_PUB_ODTCR	ODT configuration register	4-74
0x454	DDRC_PUB_DTAR	Data training address register	4-74
0x458	DDRC_PUB_DTDR0	Data training data register 0	4-75
0x45C	DDRC_PUB_DTDR1	Data training data register 1	4-76

Offset Address	Register	Description	Page
0x580	DDRC_PUB_ZQ_CTRL0	Pub DDR PHY I/O compensation configuration register 0	4-77
0x584	DDRC_PUB_ZQ_CTRL1	Pub DDR PHY I/O compensation configuration register 1	4-77
0x588	DDRC_PUB_ZQ_STATUS0	DDR PHY I/O compensation status register 0	4-77
0x58C	DDRC_PUB_ZQ_STATUS1	DDR PHY I/O compensation status register 1	4-78
0x5C0 + 0x40 x blanes	DDRC_PUB_DXNGCR	DATX8 general configuration register	4-78
0x5C4 + 0x40 x blanes	DDRC_PUB_DXNGSR0	DATX8 general status register 0	4-81
0x5C8 + 0x40 x blanes	DDRC_PUB_DXNGSR1	DATX8 general status register 1	4-82
0x5CC + 0x40xblanes	DDRC_PUB_DXNDLLCR	DATX8 DLL control register	4-83
0x5D0 + 0x40 x blanes	DDRC_PUB_DXNDQTR	DATX8 DQ timing register	4-85
0x5D4 + 0x40 x blanes	DDRC_PUB_DXNDQSTR	DATX8 DQS timing register	4-86

4.1.6 Register Description

DDRC_STATUS

DDRC_STATUS is a DDRC status register.

Offset Address	Register Name	Total Reset Value
0x000	DDRC_STATUS	0x0000_0005

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												in_init	in_sr	reserved	busy
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.

[3]	RO	in_init	Initialization status of a controller. 0: normal 1: initializing
[2]	RO	in_sr	Self-refresh status of a controller. 0: normal 1: self refreshing
[1]	RO	reserved	Reserved.
[0]	RO	busy	Busy status of a controller. 0: idle 1: A command is being processed.

DDRC_SREFCTRL

DDRC_SREFCTRL is a DDRC self-refresh control register.

Offset Address	Register Name	Total Reset Value
0x004	DDRC_SREFCTRL	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															sr_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	sr_req	SDRAM self-refresh request. 0: exit the self-refresh status 1: enter the self-refresh status

DDRC_INITCTRL

DDRC_INITCTRL is a DDRC initialization control register.

Offset Address	Register Name	Total Reset Value
0x008	DDRC_INITCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															init_req

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	init_req	Initialization enable. 0: Initialization is complete or initialization is performed properly. 1: The SDRAM starts to be initialized.

DDRC_CTRL

DDRC_CTRL is a DDRC control register.

Offset Address	Register Name	Total Reset Value
0x010	DDRC_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															ddr_rst_n
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	ddr_rst_n	DDR3 SDRAM reset. 0: valid 1: invalid Note: This bit is valid only for the DDR3 SDRAM and is set to 1 by default.

DDRC_EMRS01

DDRC_EMRS01 is a DDR mode configuration register.

Offset Address	Register Name	Total Reset Value
0x014	DDRC_EMRS01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	emrs1																mrs															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	emrs1	DDRn SDRAM extended mode register 1. This field corresponds to valid bits 13−0 of mode register 1 (MR1) in the DDRn SDRAM user manual. MR1 bit[15:14] for most DDRs are not used. DDRC_EMRS01 bit[31:30] must be set to 0b00. For details about MR1, see the DDRn SDRAM user manual.
[15:0]	RW	mrs	DDRn SDRAM mode register. This field corresponds to valid bits 13−0 of mode register 0 (MR0) in the DDRn SDRAM user manual. MR0 bit[15:14] for most DDRs are not used. DDRC_EMRS01 bit[15:14] must be set to 0b00. For details about MR0, see the DDRn SDRAM user manual.

DDRC_EMRS23

DDRC_EMRS23 is a DDR extended mode configuration register.

Offset Address	Register Name	Total Reset Value
0x018	DDRC_EMRS23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	emrs3																emrs2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	emrs3	DDRn SDRAM extended mode register 3. This field corresponds to valid bits 13−0 of mode register 3 (MR3) in the DDRn SDRAM user manual. MR3 bit[15:14] for most DDRs are not used. DDRC_EMRS23 bit[31:30] must be set to 0b00. For details about MR3, see the DDRn SDRAM user manual.
[15:0]	RW	emrs2	DDRn SDRAM extended mode register 2. This field corresponds to valid bits 13−0 of mode register 2 (MR2) in the DDRn SDRAM user manual. MR2 bit[15:14] for most DDRs are not used. DDRC_EMRS23 bit[15:14] must be set to 0b00. For details about MR2, see the DDRn SDRAM user manual.

DDRC_CONFIG0

DDRC_CONFIG0 is DDRC function configuration register 0.

Offset Address	Register Name	Total Reset Value
0x01C	DDRC_CONFIG0	0x2000_0510

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	init_arefnum				pd_prd								rcv_pdr	sr_cc	pd_cc	pd_en	reserved			rank	reserved		dram_type		reserved		mem_width		reserved		brst_a12	brstlen
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	init_arefnum	Number of auto-refresh operations when the DDRn SDRAM is being initialized. 0x0–0x2: two 0x3–0xF: n.
[27:20]	RW	pd_prd	Power down cycle of the SDRAM. When the DDRC does not receive any command in pd_prd consecutive cycles, it forces the DDRn SDRAM to enter the low-power mode; when a command is received, the DDRC forces the DDRn SDRAM to exit the low-power mode. 0x00: 1 clock cycle 0x01–0xFF: n clock cycles **Note: This parameter is valid only when pd_en is 1.**
[19]	RW	rcv_pdr	DDR receive I/O dynamic power-down control enable. The DDRC disables the receive buffer of the DDR data I/O in the non-read status when it is enabled. 0: disabled 1: enabled
[18]	RW	sr_cc	DDRn SDRAM clock control in self-refresh mode. 0: The DDRn SDRAM clock is enabled. 1: The DDRn SDRAM clock is disabled.
[17]	RW	pd_cc	DDRn SDRAM clock control in power-down mode. 0: The DDRn SDRAM clock is enabled. 1: The DDRn SDRAM clock is disabled. **Note: This parameter is valid only when the LPDDR SDRAM or LPDDR2 SDRAM is connected.**
[16]	RW	pd_en	Automatic low-power enable of the DDRn SDRAM. 0: disabled 1: enabled
[15:14]	RW	reserved	Reserved.

[13:12]	RW	rank	Rank configuration of the DDRC. 00: 1 rank Other values: reserved
[11]	RW	reserved	Reserved.
[10:8]	RW	dram_type	External memory type. 101: DDR2 110: DDR3 Other values: reserved
[7:6]	RW	reserved	Reserved.
[5:4]	RW	mem_width	Bit width of the storage data bus. 00: 16 bits 01: 32 bits Other values: reserved
[3:2]	RW	reserved	Reserved.
[1]	RW	brst_a12	DDR3 SDRAM A12 command enable. 0: disabled 1: enabled **Note: The recommended value is 0.**
[0]	RW	brstlen	Burst length of the DDRC. 0: burst4 1: burst8 When the ratio of the frequency of the DDRC to the frequency of the PHY is 1:1, the burst length of the DDR2 SDRAM can be set to burst 4 or burst 8. The burst length of the DDR3 SDRAM can only be set to burst 8. When the ratio of the frequency of the DDRC to the frequency of the PHY is 1:2, the burst length of the DDR2 SDRAM and the DDR3 SDRAM can only be set to burst 4

DDRC_CONFIG1

DDRC_CONFIG1 is DDRC function configuration register 1.

Offset Address	Register Name	Total Reset Value
0x020	DDRC_CONFIG1	0x0000_A380

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sref_arefnum				reserved					sref_zqc_en	reserved	clk_switch	reserved				odis_ddrio	pd_ac	pd_pst_opn		pd_pre_cls		reorder_en	auto_pre_en	wr_rcv_mode	exclu_en	lock_en	aref_mode	wrlvl_en	dual_ch	read_mode		clkratio		ecc_en	zqc_en

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	1	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	sref_arefnum	Number of times of auto refresh operations after DDRn SDRAM exits auto refresh in DFS process. 0x0–0x1: once 0x2–0xF: n times **Note: This field is valid only when train_en is 1. When train_en is 0, DDRn SDRAM exits self refresh and DDRC does not perform auto refresh operation.**
[27:23]	RW	reserved	Reserved.
[22]	RW	sref_zqc_en	ZQ calibration long enable when the DDR exits the self-refresh state. 0: disabled 1: enabled **Note: This bit is valid for the DDR3 or LPDDR2 mode.If the DDR is in the self-refresh state for a long time, set this bit to 1.**
[21]	RW	reserved	Reserved.
[20]	RW	clk_switch	DDRC low-power clock switch control. This field determines whether to perform back pressure on AXI port command when DDRC enters the low-power status (DDR self refresh). 0: not perform back pressure on the command and return the error response. 1: perform back pressure on the command and run the original command when the clock is switched.
[19:18]	RW	reserved	Reserved.
[17]	RW	odis_ddrio	Output disable configuration of the DDR command and data I/O. 0: enable the pin output 1: disable the pin output **Note: This is a static configuration. When DDR enters the self–refresh mode, set DDR to 1 to disable the DDR command and data I/O output. Before DDR exits the self–refresh mode, set DDR to 0 to enable the DDR command and data I/O output.**
[16]	RW	pd_ac	SDRAM address command status enable control in power-down mode. 0: enable the pin output 1: disable the pin output **Note: When pd_en is enabled, pd_ac is valid. The control pins exclude CKE, ODT, CSN, and RESET_N.**

[15:14]	RW	pd_pst_opn	SDRAM address/command pin delay before the power-down mode is exited. 00: 0 cycles 01: 1 cycle 10: 2 cycles 11: 3cycles **Note: When pd_en is enabled, pd_pst_opn is valid. The control pins exclude CKE and RESET_N.**
[13:12]	RW	pd_pre_cls	SDRAM address/command disable delay after the power-down mode is entered. 00: 0 cycles 01: 1 cycle 10: 2 cycles 11: 3 cycles **Note: When pd_en is enabled, pd_pre_cls is valid. The control pins exclude CKE and RESET_N.**
[11]	RW	reserved	Reserved.
[10]	RW	auto_pre_en	Auto precharge enable. 0: disabled 1: enabled
[9]	RW	wr_rcv_mode	Mode of receiving the write command over the DDRC AXI port. 0: The write command is received directly. 1: The write command is received only after the expected data to be written arrives.
[8]	RW	exclu_en	Exclusive command enable. 0: disabled 1: enabled
[7]	RW	lock_en	WRAP command lock enable. 0: disabled 1: enabled
[6]	RW	aref_mode	Auto-refresh mode select. 0: An auto-refresh operation is performed every one tREFI period. 1: Eight auto-refresh operations are performed every nine tREFI periods.
[5]	RW	wrlvl_en	Auto-control enable of the DDR3 write level hardware. 0: disabled 1: enabled
[4]	RW	reserved	Reserved. **This field must be set to 0.**

[3]	RW	read_mode	Read mode select of the DDRC. 0: associated read mode 1: delay read mode The associated read mode is a mode in which the DDRC samples data based on the data valid signal from the PHY. The delay read mode is a mode in which the DDRC samples the data from the PHY after the internal delay of the DDRC. **Note: This bit must be set to 0 when DDRC_DTRCTRL[train_mode] is set to 0.**
[2]	RW	clkratio	Operating mode of the DDRC. When the frequency ratio of DDRC to PHY is 1:1, this bit is set to 0. When the frequency ratio of DDRC to PHY is 1:2, this bit is set to 1.
[1]	RW	ecc_en	ECC enable of the DDRC 0: disabled 1: enabled
[0]	RW	zqc_en	DDR3 SDRAM ZQ enable. 0: disabled 1: enabled **Note: This bit is valid for the DDR3 SDRAM only and is set to 1 by default.**

DDRC_CMDCFG

DDRC_CMDCFG is a DDRC command configuration register.

Offset Address	Register Name	Total Reset Value
0x024	DDRC_CMDCFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cmd_mrs																cmd_ba								cmd_rank				reserved			cmd_type
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	cmd_mrs	Value of the DDR mode register when the load mode register (LMR) command is configured.
[15:8]	RW	cmd_ba	Value of the DDR BA when the LMR command is configured.

[7:4]	RW	cmd_rank	Rank for running commands. 0: The configuration command is executed. 1: The configuration command is not executed. Each bit controls a rank. **Note: As the Hi3518 only has rank0, cmd_rank must be set to 0x0 or 0x1.**
[3:2]	RW	reserved	Reserved.
[1:0]	RW	cmd_type	DDR command configuration. 00: enter the deep power-down mode 01: exit the deep power-down mode 10: LMR command 11: ZQCL

DDRC_CMDEXE

DDRC_CMDEXE is a DDRC software configuration command start register.

Offset Address	Register Name	Total Reset Value
0x028	DDRC_CMDEXE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															cmd_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	cmd_req	Request of executing the configuration command of the DDRC. 0: The command is not executed or the parameter is cleared automatically after the command is executed. 1: The command is requested to be executed.

DDRC_RNKCFG

DDRC_RNKCFG is a DDR feature configuration register.

Offset Address	Register Name	Total Reset Value
0x02C	DDRC_RNKCFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		mem_map		reserved			mem_bank	reserved		mem_row			reserved		mem_col	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved.
[13:12]	RW	mem_map	Address translation mode of the SDRAM. 00: {Rank, Row, Ba, Col, DW} = AXI_Address 01: {Rank, Ba, Row, Col, DW} = AXI_Address Other values: reserved
[11:9]	RW	reserved	Reserved.
[8]	RW	mem_bank	Number of banks of a single SDRAM. 0: 4 banks 1: 8 banks If there are multiple ranks, the ranks in the same channel can have different configurations. In dual-channel mode, the dual channels must have the same configuration.
[7]	RW	reserved	Reserved.
[6:4]	RW	mem_row	Bit width of the row address of a single SDRAM. 000: 11 bits 001: 12 bits 010: 13 bits 011: 14 bits 100: 15 bits 101: 16 bits Other values: reserved
[3]	RW	reserved	Reserved.
[2:0]	RW	mem_col	Bit width of the column address of a single SDRAM. 000: 8 bits 001: 9 bits 010: 10 bits 011: 11 bits 100: 12 bits Other values: reserved

DDRC_BASEADDR

DDRC_BASEADDR is a DDR space base address configuration register.

Offset Address	Register Name	Total Reset Value
0x040	DDRC_BASEADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mem_base_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	mem_base_addr	Configuration of the start base address of the DDR in the system.

DDRC_TIMING0

DDRC_TIMING0 is DDR timing parameter register 0.

Offset Address	Register Name	Total Reset Value
0x050	DDRC_TIMING0	0xFFFF_3F1F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tmrd				trrd				trp				trcd				reserved				trc				reserved				tras			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[31:28]	RW	tmrd	Count of wait cycles of LMR command. 0x0–0x1: 1 clock cycle 0x2–0xF: n clock cycles
[27:24]	RW	trrd	Number of wait cycles of the ACT bank A to ACT bank B command. 0x0–0x1: 1 clock cycle 0x2–0xF: n clock cycles
[23:20]	RW	trp	Count of wait cycles for disabling commands (PRE period). 0x0–0x1: 1 clock cycle 0x2–0xF: n clock cycles
[19:16]	RW	trcd	Number of wait cycles from the ACT bank command to the read or write bank command. 0x0–0x3: 3 clock cycles 0x4–0xF: n clock cycles
[15:14]	RW	reserved	Reserved.

[13:8]	RW	trc	Number of wait cycles from an ACT bank command to the next ACT bank command. 0x00–0x01: 1 clock cycle 0x02–0x3F: n clock cycles
[7:5]	RW	reserved	Reserved.
[4:0]	RW	tras	Number of wait cycles from ACT to PRE. 0x00–0x01: 1 clock cycle 0x02–0x0F: n clock cycles

DDRC_TIMING1

DDRC_TIMING1 is DDR timing parameter register 1.

Offset Address	Register Name	Total Reset Value
0x054	DDRC_TIMING1	0xFF01_45FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tsre								trdlat				trtw				twl				tcl				trfc							
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:24]	RW	tsre	Number of wait cycles from the self-refresh exit command to the read command. 0x0: 1 clock cycle 0x01–0xFF: n x 2 clock cycles When the DDR3 SDRAM is used, the value is set to tXSDLL.
[23:20]	RW	trdlat	Inherent delay of the DDR PHY. 0x0–0xF: n + 1 clock cycles When the Dophin PHY is used, the value is set to 0x5. This field is valid when read_mode is 1 (delay read mode).
[19:16]	RW	trtw	Delay from the last read data segment to the first written data segment. 0x0–0x1: 1 clock cycle 0x2-0xF: n + 1 clock cycles
[15:12]	RW	twl	Number of wait cycles from the write command to the write data. 0x0–0x1: 1 clock cycle 0x2–0xF: n clock cycles For example, 0x3 indicates 3 clock cycles. **Note: In DDR2 mode, twl is set to (tcl – 1) and the equation of twl – taond ≥ 1 must be true.** **Note: The time parameter value is calculated based on the**

			DDR SRAM clock cycle.
[11:8]	RW	tcl	DDR CL from the read command to the read data. 0x0–0x1: 1 clock cycle 0x2–0xF: n clock cycles **Note: The time parameter value is calculated based on the DDR SRAM clock cycle.**
[7:0]	RW	trfc	Number of wait cycles of the AREF period or AREF to the ACT command. The register can be set to the maximum value max{trfc, tzqcs}. 0x00–0x01: 1 clock cycle 0x02–0xFF: n clock cycles

DDRC_TIMING2

DDRC_TIMING2 is DDR timing parameter register 2.

Offset Address	Register Name	Total Reset Value
0x058	DDRC_TIMING2	0xF3F3_F000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tcke				twtr				twr				reserved				tfaw				reserved				taref							
Reset	1	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	tcke	Minimum cycle of maintaining the low-power mode. 0x0–0x1: 1 clock cycle 0x2–0xF: n clock cycles The value needs to be set to the maximum value among tCKESR, tCKSRE, tCKSRX, and tCKE. When the Dophin DDR PHY is used, the value of this register needs to be set to max{tCKSRx, tCKE} + 3.
[27:24]	RW	twtr	Number of wait cycles of the last write-to-read command. 0x0–0x1: 1 clock cycle 0x2–0xF: n clock cycles For example, 0x3 indicates 3 clock cycles.

[23:20]	RW	twr	Number of wait cycles of write recovery. 0x0–0x1: 1 clock cycle 0x2–0xF: n clock cycles **Note: When DFS is required, tWR must be set to the maximum frequency in the DFS and cannot be changed with the frequency of the DDR.**
[19:18]	RW	reserved	Reserved.
[17:12]	RW	tfaw	Number of clock cycles of four consecutive activation commands. 0x00-0x3F: n clock cycles For example, 0x14 indicates 20 clock cycles.
[11]	RW	reserved	Reserved.
[10:0]	RW	taref	Number of auto-refresh cycles. 0x000: forbidden 0x001–0x7FF: The auto-refresh cycle of the SDRAM is 16 x n clock cycles. For example, 0x008 indicates 128 clock cycles. The configuration interval is calculated as follows: Configuration interval = tREFI/16/Tclk. tREFI is 7800 ns, and Tclk is two times of the running cycle when the SDRAM is used. When DDRC_CONFIG1[aref_mode] is 1, the interval of DDRC_TIMING2 must be set to 8 x tREFI.

DDRC_TIMING3

DDRC_TIMING3 is DDR timing parameter register 3.

Offset Address	Register Name	Total Reset Value
0x05C	DDRC_TIMING3	0xFFDF_F0F2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tzq_prd												tzqinit								taond				txard				trtp			
Reset	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	0	0	0	0	1	1	1	1	0	0	1	0

Bits	Access	Name	Description
[31:22]	RW	tzq_prd	Number of ZQCS command cycles. 0x000: The ZQCS command is forbidden. 0x001–0x3FF: n x 128 AREF cycles. The number of ZQCS command cycles is n x 128 taref clock cycles.
[21:12]	RW	tzqinit	Number of delay cycles during ZQ initialization. 0x0–0x1FF: n + 1 clock cycles The value needs to be set to the maximum value between tZQINIT

			and tDLLK.
[11:8]	RW	taond	Count of ODT enable/disable cycles. In DDR2 mode (taond/taofd): 0x0: 2/2.5 0x1: 3/3.5 0x2: 4/4.5 0x3: 5/5.5 Other values: reserved In DDR3 mode, the value is set to (tWL – 1). **Note: The time parameter value is calculated based on the DDR SRAM clock cycle.**
[7:4]	RW	txard	Number of wait cycles of exiting the DDR low-power mode. 0x0–0xF: n clock cycles. The letter *n* indicates the corresponding decimal value. For example, 0x7 indicates 7 clock cycles. The value is set to the maximum value among tXP, tXARD, tXARDS, and tXS. In DDR3 mode, when the register is set to tXS, txard only needs to be set to an equivalent clock cycle of 10 ns.
[3:0]	RW	trtp	Wait delay from the read command to the disable command. 000–010: 2 clock cycles 011–111: n clock cycles Trtp is calculated as follows: AL + BL/2 + Max(trtp, 2) – 2

DDRC_TIMING4

DDRC_TIMING4 is DDR timing parameter register 4.

Offset Address	Register Name	Total Reset Value
0x060	DDRC_TIMING4	0x000F_2028

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												twlo				reserved				twldqsen				reserved				twlmrd			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	0	0	0	0	0	0	0	1	0	1	0	0	0

Bits	Access	Name	Description
[31:20]	RW	reserved	Reserved.

[19:16]	RW	twlo	DDR3 write level status delay. 0x0–0x1: 1 clock cycle 0x2–0xF: n clock cycles The parameter is equal to twlo+twloe defined in the DDR3 protocol.
[15:14]	RW	reserved	Reserved.
[13:8]	RW	twldqsen	DDR3 write level start delay. 0x0–0x1: 1 clock cycle 0x02-0x3F: n clock cycles
[7:6]	RW	reserved	Reserved.
[5:0]	RW	twlmrd	Valid delay of the initial DQS of DDR3 write level. 0x0–0x1: 1 clock cycle 0x02-0x3F: n clock cycles

DDRC_DTRADDR

DDRC_DTRADDR is a DDRC gating training address configuration register.

Offset Address	Register Name	Total Reset Value
0x0A0	DDRC_DTRADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	train_row																train_bank				train_col											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	train_row	Row address of the DDRn SDRAM used in the gating position training. When the row address is less than 16 bits, the upper bits are stuffed with 0s.
[15:13]	RW	train_bank	Bank address of the DDRn SDRAM used in the gating position training. When the bank address is less than three bits, the upper bits are stuffed with 0s.
[12:0]	RW	train_col	Column address of the DDRn SDRAM used in the gating position training. When the column address is less than 13 bits, the upper bits are stuffed with 0s.

DDRC_DTRDATA0

DDRC_DTRDATA0 is DDRC gating training data configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0A4	DDRC_DTRDATA0	0xE11E_D22D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dtr_byte3								dtr_byte2								dtr_byte1								dtr_byte0							
Reset	1	1	1	0	0	0	0	1	0	0	0	1	1	1	1	0	1	1	0	1	0	0	1	0	0	0	1	0	1	1	0	1

Bits	Access	Name	Description
[31:24]	RW	dtr_byte3	Gating training data configuration 0 of the DDRC. When the DDRC performs training, data must be transferred in DDR BL8 mode in each read or write operation. **Note: The data configured for each byte (data for the upper four bits and lower four bits) must be different.**
[23:16]	RW	dtr_byte2	Gating training data configuration of the DDRC.
[15:8]	RW	dtr_byte1	Gating training data configuration of the DDRC.
[7:0]	RW	dtr_byte0	Gating training data configuration of the DDRC.

DDRC_DTRDATA1

DDRC_DTRDATA1 is DDRC gating training data configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0A8	DDRC_DTRDATA1	0xC33C_B44B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dtr_byte7								dtr_byte6								dtr_byte5								dtr_byte4							
Reset	1	1	0	0	0	0	1	1	0	0	1	1	1	1	0	0	1	0	1	1	0	1	0	0	0	1	0	0	1	0	1	1

Bits	Access	Name	Description
[31:24]	RW	dtr_byte7	Gating training data configuration 1 of the DDRC. When the DDRC performs training, data must be transferred in DDR BL8 mode in each read or write operation. **Note: The data configured for each byte (data for the upper four bits and lower four bits) must be different.**
[23:16]	RW	dtr_byte6	Gating training data configuration of the DDRC.
[15:8]	RW	dtr_byte5	Gating training data configuration of the DDRC.
[7:0]	RW	dtr_byte4	Gating training data configuration of the DDRC.

DDRC_DTRCTRL

DDRC_DTRCTRL is a DDRC gating training control register.

Offset Address	Register Name	Total Reset Value
0x0AC	DDRC_DTRCTRL	0x0000_0401

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dt_byte								reserved				train_start_pos				reserved		train_rank		rensel			train_mode	reserved		dt_limit		reserved		track_en	train_en	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:24]	RW	dt_byte	Byte training enable. 0: disabled 1: enabled [24]: DDRC byte0 training enable … [31]: DDRC byte7 training enable
[23:20]	RW	reserved	Reserved.
[19:16]	RW	train_start_pos	Start position of the gating training. 0x0-0x5: n clock cycles Other values: reserved
[15:14]	RW	reserved	Reserved.
[13:12]	RW	train_rank	Number of ranks in the gating training. 0x0–0x3: n + 1 ranks **Note: As the Hi3518 has only one rank, train_rank can be set only to 0.**
[11:9]	RW	rensel	Read enable delay cycle. 000–011: n + 1 clock cycles Other values: reserved
[8]	RW	train_mode	Gating training mode. 0: Dophin training mode 1: common training mode
[7:6]	RW	reserved	Reserved.
[5:4]	RW	dt_limit	DQS gating shift control. 00: shift 0° 01: shift 90° 10: shift 180° 11: shift 270°
[3]	RW	reserved	Reserved.

[2]	RW	track_en	Auto-refresh enable for the gating position. 0: disabled 1: enabled **Note: A read operation is required between two training operations and the continuous length of the accessed data must be greater than DDR burst 8.**
[1]	RW	train_en	Gating position training enable. 0: disabled 1: enabled
[0]	RW	reserved	Reserved.

DDRC_DTRPRD

DDRC_DTRPRD is a DDRC gating track period configuration register.

Offset Address	Register Name	Total Reset Value
0x0B0	DDRC_DTRPRD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												track_prd																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved.
[19:0]	RW	track_prd	Auto-update period configuration of the DQS gating. The DDRC tracks the gating position in the configured period. 0x0: 1 AREF period 0x1–0x7FF: n + 1 AREF periods

DDRC_DTRGATE

DDRC_DTRGATE is a DDRC gating phase position register.

Offset Address	Register Name	Total Reset Value
0x0B4	DDRC_DTRGATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																gate_sel															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.

			Note: This register cannot be read continuously.
[15:0]	RW	gate_sel	Gating phase position of the DDRC. 00: 0° 01: 90° 10: 180° 11: 270° [2 x (N + 1) – 1:2 x N]: gating phase of DDRC byteN N = 0–7

DDRC_DTRLAT

DDRC_DTRLAT is a DDRC gating period position register.

Offset Address	Register Name	Total Reset Value
0x0C4	DDRC_DTRLAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sys_lat																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sys_lat	Number of gating delay cycles of the DDRC. 0x0–0x5: n clock cycles Other values: reserved [4 x (N + 1) – 1:4 x N]: gating phase of DDRC ByteN. N = 0–7 **Note: This register cannot be read or written continuously.**

DDRC_DTRSTATUS

DDRC_DTRSTATUS is a DDRC gating status register.

Offset Address	Register Name	Total Reset Value
0x0D4	DDRC_DTRSTATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dtr_st																dtr_ok								dtr_err							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	dtr_st	Phase shift status of the byte gating position. 00: shift 0°

			01: shift 90° 10: shift 180° 11: shift 270° bit[31:30] to bit[17:16]: Each two bits correspond to DDRC byte7 to DDRC byte0 respectively.
[15:8]	RO	dtr_ok	Gating training status. 0: training error 1: no training error bit[15] to bit[8]: Each bit corresponds to DDRC byte7 to DDRC byte0 respectively.
[7:0]	RO	dtr_err	Auto tracking error status of the gating position. 0: no tracking error 1: tracking error bit[7] to bit[0]: Each bit corresponds to DDRC byte7 to DDRC byte0 respectively.

DDRC_AXISTATUS

DDRC_AXISTATUS is a DDRC interface status register.

Offset Address	Register Name	Total Reset Value
0x0F0	DDRC_AXISTATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								axi_st7	axi_st6	axi_st5	axi_st4	axi_st3	axi_st2	axi_st1	axi_st0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7]	RO	axi_st7	Status of DDRC bus interface 7. 0: idle 1: A command is being executed.
[6]	RO	axi_st6	Status of DDRC bus interface 6. 0: idle 1: A command is being executed.
[5]	RO	axi_st5	Status of DDRC bus interface 5. 0: idle 1: A command is being executed.

[4]	RO	axi_st4	Status of DDRC bus interface 4. 0: idle 1: A command is being executed.
[3]	RO	axi_st3	Status of DDRC bus interface 3. 0: idle 1: A command is being executed.
[2]	RO	axi_st2	Status of DDRC bus interface 2. 0: idle 1: A command is being executed.
[1]	RO	axi_st1	Status of DDRC bus interface 1. 0: idle 1: A command is being executed.
[0]	RO	axi_st0	Status of DDRC bus interface 0. 0: idle 1: A command is being executed.

DDRC_ODTCFG

DDRC_ODTCFG is a DDR ODT feature configuration register.

Offset Address	Register Name	Total Reset Value
0x0F4	DDRC_ODTCFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															rodt0	reserved															wodt0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RW	reserved	Reserved. This field must be fixed at 0.
[16]	RW	rodt0	Read ODT configuration of rank0. 0: disabled 1: enabled
[15:1]	RW	reserved	Reserved. This field must be fixed at 0.
[0]	RW	wodt0	Write ODT configuration of rank1. 0: disabled 1: enabled

DDRC_QOSCFG0

DDRC_QOSCFG0 is DDRC QoS algorithm configuration register 0.

Offset Address	Register Name	Total Reset Value
0x100	DDRC_QOSCFG0	0x0000_000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									idmap_mode	id_order_ctl	order_en	dmc_fifo_lvl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:7]	RW	reserved	Reserved.
[6]	RW	idmap_mode	ID mapping mode. 0: The id_map mapping mode configured by the register is used by default. 1: The QoS mapping mode is used. The AXI port configures this mode in associated mode by running read/write commands. This mapping mode is valid only when its macro definition is enabled in the RTL code. **This field must be 1.**
[5]	RW	id_order_ctl	Out-of –order execution enable of the specified ID. 0: disabled 1: enabled The DDRC does not ensure the order when conflict occurs between the DDR row addresses of the read/write commands with the specified ID and other IDs. Master ensures the consistency of the data.
[4]	RW	order_en	Execution order enable for the commands with the same priority. 0: disabled 1: enabled
[3:0]	RW	dmc_fifo_lvl	Depth of the command register FIFO in the DMC. 0x0–0xF: n + 1 command depths **Note: The maximum depth of the command register FIFO in the Hi3518 is 0xB, but it is recommended to set the depth to 0x7**.

DDRC_QOS

DDRC_QOS is a DDRC command priority configuration register.

Offset Address	Register Name	Total Reset Value
0x150+0x4 x id0 id0(0–15)	DDRC_QOS	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				rd_pri_apt				rd_age_prd				reserved			rd_qos_en	reserved				rd_qos								reserved		rd_pri	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:28]	RW	reserved	Reserved.
[27:24]	RW	pri_apt	Command priority adaptation configuration. 0x0: disabled 0x1−0xF: n x 16 clock cycles
[23:20]	RW	age_prd	Command aging cycle configuration. 0x0: disabled 0x1−0xF: n x 16 clock cycles
[19:17]	RW	reserved	Reserved.
[16]	RW	qos_en	Command QoS enable (timeout). 0: disabled 1: enabled
[15:14]	RW	reserved	Reserved.
[13:4]	RW	qos	Command QoS configuration (timeout). 0x1−0x3FF: n clock cycles Other values: reserved **Note: The used timeout is an integral multiple of 16. The lower four bits of rd_qos is ignored.**
[3]	RW	reserved	Reserved.
[2:0]	RW	pri	Command priority configuration. 000: highest priority 001: higher priority … 111: lowest priority

DDRC_FLUX

DDRC_FLUX is a DDRC AXI port bandwidth traffic control configuration register.

Offset Address	Register Name	Total Reset Value
0x200+0x4 x ports ports(0–5)	DDRC_FLUX	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										flux_port_en	flux_ovfl	reserved				flux_lvl				reserved				flux							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RW	reserved	Reserved.
[21]	RW	flux_port_en	AXI port DDRC traffic count enable. 0: disabled 1: enabled
[20]	RW	flux_ovfl	AXI port traffic overflow allow enable. 0: disabled 1: enabled When this bit is set to 1, the traffic of the AXI port exceeds the bandwidth limit, and no request is raised over the AXI ports without overflow, the bandwidth of the AXI port can exceed the configured value.
[19:17]	RW	reserved	Reserved.
[16:12]	RW	flux_lvl	AXI port traffic overflow allow threshold. 0x0–0xC: DMC threshold for allowing traffic overflow Other values: reserved When flux_ovfl is set to 1, this traffic overflow over the AXI port is allowed if the traffic of the AXI port is greater than the configured bandwidth of flux and the number of the commands to be processed in DMC is less than the configured threshold.
[11:10]	RW	reserved	Reserved.
[9:0]	RW	flux	Bandwidth configuration of the AXI port. 0x0–0x3FF: ratio of the maximum DDR bandwidth to the total bandwidth accessed by the AXI port. The total bandwidth is 1024. The configured value is calculated as follows: ratio of the required bandwidth to the total bandwidth x1024. For example, if 20% of bandwidth is required for this AXI port, configure flux to 0xCD.

DDRC_TEST0

DDRC_TEST0 is a DDRC test status register.

Offset Address	Register Name	Total Reset Value
0x240	DDRC_TEST0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dmc_ct																dmc_cv															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	dmc_ct	DDRC command type.
[15:0]	RO	dmc_cv	Commands that are being processed by the DDRC.

DDRC_TEST1

DDRC_TEST1 is a DDRC test status register.

Offset Address	Register Name	Total Reset Value
0x244	DDRC_TEST1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								dt_num				reserved	byte_sel		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved.
[8:4]	RW	dt_num	Cycle n select, data read from the training module (n = 0–23).
[3]	RW	reserved	Reserved.
[2:0]	RW	byte_sel	Channel select of the returned data. 0x0–0x7: channel n select

DDRC_TEST2

DDRC_TEST2 is a DDRC test status register.

Offset Address	Register Name	Total Reset Value
0x248	DDRC_TEST2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	data_h																															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	data_h	Upper 32 bits of the training data.

DDRC_TEST3

DDRC_TEST3 is a DDRC test status register.

Offset Address	Register Name	Total Reset Value
0x24C	DDRC_TEST3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	data_l																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	data_l	Lower 32 bits of the training data.

DDRC_TEST4

DDRC_TEST4 is a DDRC test status register.

Offset Address	Register Name	Total Reset Value
0x250	DDRC_TEST4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dt_ok_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	dt_ok_cnt	Number of times of correct training data. 0x0–0xF: n + 1 [3 x (N + 1) – 1:3 x N]: number of times of correct byteN

DDRC_TEST7

DDRC_TEST7 is a DDRC performance measurement control register.

Offset Address	Register Name	Total Reset Value
0x260	DDRC_TEST7	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	perf_mode	perf_en	perf_ch		perf_prd																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	perf_mode	Performance measurement mode. 0: continuous trigger mode. The performance counter counts continuously. No data overflow occurs within 1s = (533 MHz). 1: single trigger mode. When the performance counter reaches the maximum value, the count value is retained but counting is stopped. **Note: When an overflow occurs, the count values wrap.**
[30]	RW	perf_en	Performance measurement enable. 0: disabled 1: enabled **Note: When perf_mode is 0 and this bit is enabled, performance measurement register starts cyclic counting. When perf_mode is 1, this bit is cleared after counting is complete once.**
[29:28]	RW	perf_ch	Read and write count channel. 00: disabled 01: channel 0 10: channel 1 11: channel 0 and channel 1 **Note: This register limits the number of read/write command count channels of DDRC_TEST8 and DDRC_TEST9.**
[27:0]	RW	perf_prd	Performance measurement cycle. 0x0–0xFFFFFFF: count cycles The actual count cycle is calculated as follows: perf_prd x 4 xtclk. Where tclk is the bus clock cycle of the DDRC. **Note: This configuration is valid only when perf_mode is 1. When perf_mode is set to 0 to select the continuous count mode, the performance counters keep on counting.**

DDRC_TEST8

DDRC_TEST8 is a DDRC write command count register.

Offset Address	Register Name	Total Reset Value
0x264	DDRC_TEST8	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wr_num																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RWC	wr_num	Count of write commands in the count period. This register is written to clear. Wrap cycle counting is supported.

DDRC_TEST9

DDRC_TEST9 is a DDRC read command count register.

Offset Address	Register Name	Total Reset Value
0x268	DDRC_TEST9	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rd_num																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RWC	rd_num	Count of read commands in the count period. This register is written to clear. Wrap cycle counting is supported.

DDRC_TEST10

DDRC_TEST10 is a DDRC DMC wait command count register.

Offset Address	Register Name	Total Reset Value
0x26C	DDRC_TEST10	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dmc_cmd_num																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RWC	dmc_cmd_num	Count of DMC wait commands of the DDRC in the count period. This register is written to clear. Wrap cycle counting is supported.

			Note: As the register width is limited and data overflow needs to be avoided within 1s under the 533 MHz clock, the displayed count value of this register is the actual count value divided by 2.

DDRC_TEST12

DDRC_TEST12 is a DDRC test status register.

Offset Address	Register Name	Total Reset Value
0x280	DDRC_TEST12	0x0000_0FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wfifo_f																wfifo_e															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	wfifo_f	Write FIFO full status.
[15:0]	RO	wfifo_e	Write FIFO empty status. **Note: Only the 12-bit reset value is 0xFFF for the Hi3518.**

DDRC_TEST13

DDRC_TEST13 is DDRC reorder test status register 1.

Offset Address	Register Name	Total Reset Value
0x284	DDRC_TEST13	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ddrexec_reorder															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RO	ddrexec_reorder	DDREXEC reorder status.

DDRC_TEST14

DDRC_TEST14 is DDRC reorder test status register 2.

Offset Address	Register Name	Total Reset Value
0x288	DDRC_TEST14	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ddrexec_reorder_req																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RO	ddrexec_reorder_req	DDREXEC reorder request status.

DDRC_TEST15

DDRC_TEST15 is DDRC reorder test status register 3.

Offset Address	Register Name	Total Reset Value
0x28C	DDRC_TEST15	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ddrexec_reorder_gnt																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RO	ddrexec_reorder_gnt	DDREXEC reorder arbitration status.

DDRC_PUB_PIR

DDRC_PUB_PIR is a PHY initialization register.

Offset Address	Register Name	Total Reset Value
0x404	DDRC_PUB_PIR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	initbyp	zcalbyp	lockbyp	clrsr	reserved								ctldinit	dllbyp	icpc	reserved								eyetrn	qstrn	draminit	dramrst	itmsrst	zcal	dlllock	dllsrst	init	

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	initbyp	Initialization bypass. If this bit is set, all running initialization routines including PHY initialization, DRAM initialization, and PHY training are bypassed or stopped. Initialization may be manually triggered by using INIT and the other relevant bits of the PIR register. This bit is self-cleared.
[30]	RW	zcalbyp	Impedance calibration bypass. If this bit is set, impedance calibration of all ZQ control blocks that are automatically triggered after reset are bypassed or stopped. Impedance calibration may be manually triggered by using INIT and ZCAL bits of the PIR register. This bit is self-cleared.
[29]	RW	lockbyp	DLL lock bypass. If this bit is set, the waiting of DLLs to lock is bypassed or stopped. DLL lock wait is automatically triggered after reset. DLL lock wait may be manually triggered by using INIT and DLLLOCK bits of the PIR register. This bit is self-cleared.
[28]	RW	clrsr	Status clear. A write of '1' to this bit will clear (reset to '0') all status registers, including PGSR and DXnGSR. The clear status register bit is self-cleared. This bit is primarily for debugging and is typically not needed during normal functional operation. When PGSR.IDONE is 1, it can be used to manually clear the PGSR status bits, although starting a new initialization process will automatically clear the PGSR status bits. It can also be used to manually clear the DXnGSR status bits, although starting a new data training process will automatically clear the DXnGSR status bits.
[27:19]	RW	reserved	reserved
[18]	RW	ctldinit	Controller DRAM initialization. If this bit is set, this DRAM initialization will be performed by the controller. If this bit is not set, this DRAM initialization will be performed by using the built-in initialization sequence or by using software over the configuration port.
[17]	RW	dllbyp	DLL bypass. If this bit is set to 1, all PHY DLLs enter the bypass mode. A bypassed DLL is also powered down (disabled).
[16]	RW	icpc	Initialization complete pin configuration. 0: This bit is asserted after PHY initialization (DLL locking and impedance calibration) is complete. 1: This bit is asserted after PHY initialization and the triggered PUB initialization (DRAM initialization, data training, or initialization trigger with no selected initialization) are complete.

[15:9]	RW	reserved	Reserved.
[8]	RW	eyetrn	Execute read data eye training by PUB. 0: disabled 1: enabled This function is not support by this version.
[7]	RW	qstrn	Execute read DQS training by PUB. 0: disabled 1: enabled
[6]	RW	draminit	DRAM initialization for executing the DRAM initialization sequence. 0: disabled 1: enabled
[5]	RW	dramrst	DRAM reset (valid only for DDR3). 0: disabled 1: enabled
[4]	RW	itmsrst	ITM soft reset. 0: disabled 1: enabled
[3]	RW	zcal	PHY impedance calibration. 0: disabled 1: enabled
[2]	RW	dlllock	DLL lock for waiting for the PHY DLLs to lock. 0: disabled 1: enabled
[1]	RW	dllsrst	DLL soft reset. All PHY DLLs are soft-reset by driving the DLL soft reset pin. 0: disabled 1: enabled
[0]	RW	init	Initialization trigger (self-cleared). 0: No operation is performed. 1: The DDR system initialization is triggered.

DDRC_PUB_PGCR

DDRC_PUB_PGCR is a PHY general configuration register.

Offset Address	Register Name	Total Reset Value
0x408	DDRC_PUB_PGCR	0x0184_2E04

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lbmode	lbgdqs	lbdqss	rfshdt				pddisdx	zcksel			ranken				ioddrm	iolb	ckinv	ckdv		cken				dtosel				dftlmt		dftcmp	dqscfg	itmdmd
Reset	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0	0	0	0	1	0	1	1	1	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31]	RW	lbmode	Loopback mode. If this bit is set, the PHY/PUB is in loopback mode.
[30]	RW	lbgdqs	Loopback DQS gating. This bit is used to select the DQS gating mode (including BIST loopback mode) that should be used when the PHY is in loopback mode. 0: DQS gate training will be triggered on the PUB. 1: DQS gate is manually set by using software.
[29]	RW	lbdqss	Loopback DQS shift. This bit is used to select how the read DQS is shifted during loopback to ensure that the read DQS is centered into the read data eye. 0: PUB sets the read DQS delay to 0, and the DQS is already shifted 90º by a write path. 1: The read DQS shift is manually set by using software.
[28:25]	RW	rfshdt	Refresh during training. A non-zero value specifies that a burst of refreshes equal to the number specified in this field should be sent to the SDRAM after training of each rank except the last rank.
[24]	RW	pddisdx	Power down disabled byte. If this bit is set, the DLL and I/Os of a disabled byte should be powered down.
[23:22]	RW	zcksel	Impedance clock divider select. This bit is used to select the divide ratio for the clock used by the impedance control logic relative to the clock used by the memory controller and SDRAM. 00: divide by 2 01: divide by 8 10: divide by 32 11: divide by 64

[21:18]	RW	ranken	Rank enable. This field specifies the ranks that are enabled for data training. Bit 0 controls rank 0, bit 1 controls rank 1, bit 2 controls rank 2, and bit 3 controls rank 3. Setting a bit to 1 enables the corresponding rank, and setting a bit to 0 disables the corresponding rank. **Note: The actual reset value is calculated based on the configured number of ranks. The Hi3518 supports only one rank.**
[17:16]	RW	ioddrm	I/O DDR mode (D3F I/O only). This field is used to select the DDR mode for the I/Os.
[15]	RW	iolb	I/O loopback select. This bit is used to select where the signal loopback occurs inside the I/O. 0: Loopback is after output buffer, and output enable must be asserted 1: Loopback is before output buffer, and output enable is ignored.
[14]	RW	ckinv	CK invert. If this bit is set, CK/CK# must be inverted. Otherwise, CK/CK# toggles with normal polarity.
[13:12]	RW	ckdv	CK disable value. The static value that must be driven on CK/CK# pair(s) when the pair(s) is disabled. CKDV[0] specifies the value for CK and CKDV[1] specifies the value for CK#.
[11:9]	RW	cken	CK enable. This field controls whether the CK going to the SDRAM is enabled (toggling) or disabled (static value defined by CKDV). One bit corresponds to each of the three CK pairs.
[8:5]	RW	dtosel	DLL test signal output select. 0000: test signal of DX DLL0 0001: test signal of DX DLL1 0010: test signal of DX DLL2 0011: test signal of DX DLL3 1001: test signal of the AC DLL 1111: test signal of DDR PHYB Other values: reserved

[4:3]	RW	dftlmt	DQS drift limit. This field specifies the expected limit of drift on read data strobes. A drift of this value or greater is reported as a drift error through the host port error flag. 00: no limit (no error is reported) 01: 90° drift 10: 180° drift 11: 270° or more drift Note: Although a value is reported through the error flag, this is not an error and no action is required. It only indicates that the drift is greater than expected value.
[2]	RW	dftcmp	DQS drift compensation enable. 0: disabled 1: enabled Drift compensation is enabled by default. **Note: Drift compensation must be disabled for LPDDR2.**
[1]	RW	dqscfg	DQS gating configuration. This bit is used to select one of the two DQS gating schemes. 0: DQS gating is shut off by using the rising edge of DQS_b (active window mode) 1: DQS gating blankets the whole burst (passive window mode). Note: Passive window must be used for LPDDR2.
[0]	RW	itmdmd	ITM DDR mode. This bit is used to select whether ITMS uses DQS and DQS# or it only uses DQS. 0: ITMS uses DQS and DQS#. 1: ITMS uses only DQS. **Note: The valid value for DDR is 1.**

DDRC_PUB_PGSR

DDRC_PUB_PGSR is a PHY general status register.

Offset Address	Register Name	Total Reset Value
0x40C	DDRC_PUB_PGSR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tq	reserved																							dfterr	dtierr	dterr	dtdone	didone	zcdone	dldone	idone

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	tq	Temperature output (only for LPDDR). This bit is connected to the DRAM TQ pin that is defined to high when the LPDDR device temperature is greater than or equal to 85ºC. Otherwise, this bit is low.
[30:8]	RO	reserved	Reserved.
[7]	RO	dfterr	DQS drift error. If this bit is set, at least one of the read data strobes has drifted by more than or equal to the drift limit configured in the PHY general configuration register (PGCR).
[6]	RO	dtierr	Data training intermittent error. If this bit is set, there is an intermittent error during data training. For example, a pass is followed by a failure and then another pass.
[5]	RO	dterr	Data training error. If this bit is set, a valid DQS gating window cannot be found during data training.
[4]	RO	dtdone	Data training done. If this bit is set, the PHY has finished data training.
[3]	RO	didone	DRAM initialization done. If this bit is set, DRAM initialization is complete.
[2]	RO	zcdone	Impedance calibration done. If this bit is set, impedance calibration is complete.
[1]	RO	dldone	DLL lock done. If this bit is set, DLL locking is complete.
[0]	RO	idone	Initialization done. If this bit is set, DDR system initialization is complete. This bit is set after all the selected initialization routines in PIR register are complete.

DDRC_PUB_DLLGCR

DDRC_PUB_DLLGCR is a DLL general control register.

Offset Address	Register Name	Total Reset Value
0x410	DDRC_PUB_DLLGCR	0x0373_7000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dllrsvd2		lockdet	dllrsvd1	sbias								mbias								testsw	atc		dtc			testen	ipump			dres	
Reset	0	0	0	0	0	0	1	1	0	1	1	1	0	0	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RW	dllrsvd2	DLL reserved control. This bit is connected to the DLL control bus and is reserved for future use.
[29]	RW	lockdet	Master lock detector enable. Note: This field is only valid for a few processes and is reserved for other processes.
[28]	RW	dllrsvd1	DLL reserved control. This bit is connected to the DLL control bus and is reserved for future use.
[27:20]	RW	sbias	Slave bias trim. This field is used to trim the bias for the slave DLL. Note: If DWC_DDR3PHY_DLL_TYPEA Verilog macro is defined, the default value for this field is 0x00.
[19:12]	RW	mbias	Master bias trim. This field is used to trim the bias for the master DLL. Note: If DWC_DDR3PHY_DLL_TYPEA Verilog macro is defined, the default value for this field is 0x00.
[11]	RW	testsw	Test switch. This bit is used to select the test signals of either the master DLL ('0') or the slave DLL ('1').
[10:9]	RW	atc	Analog test control. This field is used to select the analog signal to be output on the DLL analog test output (test_out_a) when TESTEN is high (output is Vss when TESTEN is low). The test output either comes from the master DLL or the slave DLL, depending on the setting of the test switch (TESTSW). Both master DLL and slave DLL outputs are similar to analog test signals. 00: filter output (Vc) 01: replica bias output for NMOS (Vbn) 10: replica bias output for PMOS (Vbp) 11: Vdd 00

[8:6]	RW	dtc	Digital test control. This field is used to select the digital signal to be output on the DLL digital test output (test_out_d[1]) when TESTEN is high (output is '0' when TESTEN is low). The following are valid settings for the master DLL (such as when TESTSW is '0'): 000: 0º output clock (clk_0) 001: 90º output clock (clk_90) 010: 180º output clock (clk_180) 011: 270º output clock (clk_270) 100: 360º internal clock (clk_360_int) 101: speed-up pulse (spdup) 110: slow-down pulse (slwdn) 111: 0º MCTL logic clock (cclk_0) The following are valid settings for the slave DLL (such as when TESTSW is '1'): 000: input DQS strobe (dqs) 001: input clock reference (clk_90_in) 010: internal feedback clock (clk_0_out) 011: 90º output DQS_b strobe (dqsb_90) 100: 90º output DQS strobe (dqs_90) 101: speed-up pulse (spdup) 110: slow-down pulse (slwdn) 111: auto-lock enable signal
[5]	RW	testen	Test enable. This bit is used to enable digital and analog test outputs selected by the DTC and ATC respectively.
[4:2]	RW	ipump	Charge pump current trim This field is used to trim charge pump current. 000: maximum current 111: minimum current
[1:0]	RW	dres	Delta resistor trim. This field is used to trim reference current versus resistor value variation: 00: Rnom 01: Rnom − 20% 1x: Rnom + 20% **Note: This field is reserved for a few processes and is not used by the DLL.**

DDRC_PUB_ACDLLCR

DDRC_PUB_ACDLLCR is an AC DLL control register.

Offset Address	Register Name	Total Reset Value
0x414	DDRC_PUB_ACDLLCR	0x4000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dlldis	dllsrst	reserved										sdlbmode	atesten	sdphase				sstart		mfwdly				mfbdly				sfwdly				sfbdly			
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	dlldis	DLL disable. A disabled DLL is bypassed. The default value 0 indicates that the DLL is enabled.
[30]	RW	dllsrst	DLL soft reset. The AC DLL is soft-reset by driving the DLL soft reset pin.
[29:20]	RW	reserved	Reserved.
[19]	RW	sdlbmode	Slave DLL loopback mode. If this bit is set, the slave DLL is put in loopback mode in which there is no 90º phase shift on read DQS/DQS#. This bit must be set when the byte PHYs are operated in loopback mode such as during BIST loopback.
[18]	RW	atesten	Analog test enable. This bit is used to enable the analog test signal to be output on the DLL analog test output (test_out_a). The DLL analog test output is tristated when this bit is 0.

[17:14]	RW	sdphase	Slave DLL phase trim. This field is used to select the phase difference between the input clock and the corresponding output clock of the slave DLL. 0000: 90 0001: 72 0010: 54 0011: 36 0100: 108 0101: 90 0110: 72 0111: 54 1000: 126 1001: 108 1010: 90 1011: 72 1100: 144 1101: 126 1110: 108 1111: 90
[13:12]	RW	sstart	Slave auto startup. This field is used to control how the slave DLL starts up relative to the master DLL locking. 0X: Slave DLL automatically starts up once the master DLL is locked. 10: The automatic startup of the slave DLL is disabled, and the phase detector is disabled. 11: The automatic startup of the slave DLL is disabled, and the phase detector is enabled.
[11:9]	RW	mfwdly	Master feed-forward delay trim. This field is used to trim the delay in the master DLL feed-forward path. 000: minimum delay 111: maximum delay
[8:6]	RW	mfbdly	Master feedback delay trim. This field is used to trim the delay in the master DLL feedback path. 000: minimum delay 111: maximum delay

[5:3]	RW	sfwdly	Slave feed-forward delay trim. This field is used to trim the delay in the slave DLL feed-forward path. 000: minimum delay 111: maximum delay
[2:0]	RW	sfbdly	Slave feedback delay trim. This field is used to trim the delay in the slave DLL feedback path. 000: minimum delay 111: maximum delay

DDRC_PUB_PTR0

DDRC_PUB_PTR0 is PHY timing register 0.

Offset Address	Register Name	Total Reset Value
0x418	DDRC_PUB_PTR0	0x0022_AF9B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												titmsrst				tdlllock												tdllsrst			
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	0	1	0	1	1	1	1	1	0	0	1	1	0	1	1

Bits	Access	Name	Description
[31:22]	RW	reserved	Reserved
[21:18]	RW	titmsrst	ITM soft reset time. This field defines the number of controller clock cycles during which the ITM soft reset pin must remain asserted when soft reset is performed on ITMs. The number must correspond to a value that is greater than or equal to eight controller clock cycles. The default value corresponds to eight controller clock cycles.
[17:6]	RW	tdlllock	DLL lock time. The field defines the number of clock cycles for the DLL to stabilize and lock the number of clock cycles from when the DLL reset pin is deasserted to when the DLL has locked and is ready for use. For details, see the PHY data book for the DLL lock time. The default value corresponds to 5.12 µs at 533 MHz.
[5:0]	RW	tdllsrst	DLL soft reset time. The field defines the number of controller clock cycles during which the DLL soft reset pin must remain asserted when the soft reset is triggered through the PHY initialization register (PIR). The number must correspond to a value that is greater than or equal to 50 ns or eight controller clock cycles, whichever is greater. The default value corresponds to 50 ns at 533 MHz.

DDRC_PUB_PTR1

DDRC_PUB_PTR1 is PHY timing register 1.

Offset Address	Register Name	Total Reset Value
0x41C	DDRC_PUB_PTR1	0x0604_111D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tdinit1								tdinit0															
Reset	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	0	0	1	1	1	0	1

Bits	Access	Name	Description
[31:27]	RW	reserved	Reserved
[26:19]	RW	tdinit1	DRAM initialization time 1. The DRAM initialization time corresponding to the following: DDR3: CKE high time to first command (tRFC +10 ns or 5 tCK, whichever value is larger) DDR2: CKE high time to first command (400 ns) DDR: CKE high time to first command (400 ns or 1 tCK) LPDDR2: CKE low time with power and clock stable (100 ns) The default value corresponds to DDR3 360 ns at 533MHz.
[18:0]	RW	tdinit0	DRAM initialization time 0. The DRAM initialization time corresponding to the following: DDR3: CKE low time with power and clock stable (500 µs) DDR2: CKE low time with power and clock stable (200 µs) DDR: CKE low time with power and clock stable (200 µs) LPDDR: CKE high time to first command (200 µs) LPDDR2: CKE high time to first command (200 µs) The default value corresponds to DDR3 500 µs at 533MHz.

DDRC_PUB_PTR2

DDRC_PUB_PTR2 is PHY timing register 2.

Offset Address	Register Name	Total Reset Value
0x420	DDRC_PUB_PTR2	0x042D_A072

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tdinit3								tdinit2															
Reset	0	0	0	0	0	1	0	0	0	0	1	0	1	1	0	1	1	0	1	0	0	0	0	0	0	1	1	1	0	0	1	0

Bits	Access	Name	Description
[31:27]	RW	reserved	Reserved

[26:17]	RW	tdinit3	DRAM initialization time 3. The DRAM initialization time corresponding to the following: LPDDR2: time from ZQ initialization command to first command (1 μs) The default value corresponds to the LPDDR2 1 μs at 533MHz.
[16:0]	RW	tdinit2	DRAM initialization time 2. The DRAM initialization time corresponding to the following: DDR3: reset low time (200 μs on power-on or 100 ns after power-on) LPDDR2: time from reset command to end of auto initialization (1 μs + 10 μs = 11 μs) The default value corresponds to DDR3 200 μs at 533MHz.

DDRC_PUB_ACIOCR

DDRC_PUB_ACIOCR is an AC I/O configuration register.

Offset Address	Register Name	Total Reset Value
0x424	DDRC_PUB_ACIOCR	0x3040_0812

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	acsr		rstiom	rstpdr	rstpdd	rstodt	rankpdr				cspdd				rankodt				ckpdr		ckpdd				ckodt			acpdr	acpdd		acodt		acoe		aciom	
Reset	0	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1	0

Bits	Access	Name	Description
[31:30]	RO	acsr	Address/Command slew rate. **Note: The Hi3518 does not support the configuration.**
[29]	RW	rstiom	SDRAM reset I/O mode. This bit is used to select SSTL mode (when set to 0) or CMOS mode (when set to 1) of the I/O for SDRAM reset.
[28]	RW	rstpdr	SDRAM reset power down receiver. If this bit is set, the input receiver on the I/O is powered down for the SDRAM RST# pin.
[27]	RW	rstpdd	SDRAM reset power down driver. If this bit is set, the output driver on the I/O is powered down for the SDRAM RST# pin.
[26]	RW	rstodt	SDRAM reset on-die termination. If this bit is set, the on-die termination on the I/O is enabled for the SDRAM RST# pin.

[25:22]	RW	rankpdr	Rank power down receiver. If this field is set, the input receiver on the I/O is powered down for CKE[3:0], ODT[3:0], and CS#[3:0] pins. RANKPDR[0] controls the power down for CKE[0], ODT[0], and CS#[0]; RANKPDR[1] controls the power down for CKE[1], ODT[1], and CS#[1], and so on. Note: The actual reset value is calculated based on the configured number of ranks. For the Hi3518, each PUB supports one rank.
[21:18]	RW	cspdd	CS# power down driver. If this field is set, the output driver on the I/O is powered down for CS#[3:0] pins. PDD[0] controls the power down for CS#[0], PDD[1] controls the power down for CS#[1], and so on. The power down for the CKE and ODT drivers is controlled by the DSGCR register. **Note: The actual reset value is calculated based on the configured number of ranks. For the Hi3518, each PUB supports one rank.**
[17:14]	RW	rankodt	Rank on-die termination. If this field is set, the on-die termination on the I/O is enabled for CKE[3:0], ODT[3:0], and CS#[3:0] pins. RANKODT[0] controls the on-die termination for CKE[0], ODT[0], and CS#[0]; RANKODT[1] controls the on-die termination for CKE[1], ODT[1], and CS#[1], and so on. Note: The actual reset value is calculated based on the configured number of ranks. For the Hi3518, each PUB supports one rank.
[13:11]	RW	ckpdr	CK power down receiver. If this field is set, the input receiver on the I/O is powered down for CK[0], CK[1], and CK[2] pins respectively. Note: The actual reset value is calculated based on the configured number of DDRCKs. For the Hi3518, each PUB supports one DDRCK.
[10:8]	RW	ckpdd	CK power down driver. If this field is set, the output driver on the I/O is powered down for CK[0], CK[1], and CK[2] pins respectively. Note: The actual reset value is calculated based on the configured number of DDRCKs. For the Hi3518, each PUB supports one DDRCK.
[7:5]	RW	ckodt	CK on-die termination. If this field is set, the on-die termination on the I/O is enabled for CK[0], CK[1], and CK[2] pins respectively. Note: The actual reset value is calculated based on the configured number of DDRCKs. For the Hi3518, each PUB supports one DDRCK.

[4]	RW	acpdr	AC power down receiver. If this bit is set, the input receiver on the I/O is powered down for RAS#, CAS#, WE#, BA[2:0], and A[15:0] pins, as well as the optional DIMM PAR_IN pin and LPDDR TPD pin.
[3]	RW	acpdd	AC power down driver. If this bit is set, the output driver on the I/O is powered down for RAS#, CAS#, WE#, BA[2:0], and A[15:0] pins, as well as the optional DIMM PAR_IN pin and LPDDR TPD pin.
[2]	RW	acodt	Address/Command on-die termination. If this bit is set, the on-die termination on the I/O is enabled for RAS#, CAS#, WE#, BA[2:0], and A[15:0] pins, as well as the optional DIMM PAR_IN pin and LPDDR TPD pin.
[1]	RW	acoe	Address/Command output enable. If this bit is set, the output driver on the I/O is enabled for all address and command pins, as well as the optional DIMM PAR_IN pin and LPDDR TPD pin.
[0]	RW	aciom	Address/Command I/O mode. This bit is used to select the SSTL mode (when set to 0) or CMOS mode (when set to 1) of the I/O for all address and command pins, as well as the optional DIMM PAR_IN pin and LPDDR TPD pin.

DDRC_PUB_DXCCR

DDRC_PUB_DXCCR is a DATX8 common configuration register.

Offset Address	Register Name	Total Reset Value
0x428	DDRC_PUB_DXCCR	0x0000_0800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		dxsr		dqsnres				dqsres				dxpdr	dxpdd	dxiom	dxodt
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RW	reserved	reserved
[13:12]	RW	dxsr	Data slew rate (only for D3F I/O). This field is used to select the slew rate of the I/O for DQ, DM, and DQS/DQS# pins of all DATX8 macros. **Note: The Hi3518 does not support the configuration.**

[11:8]	RW	dqsnres	DQS# resistor. This field is used to select the on-die pull-up/pull-down resistor for DQS# pins. This field has the same encoding as DQSRES. Note: A DQS# resistor must be connected for LPDDR2.
[7:4]	RW	dqsres	DQS resistor. This field is used to select the on-die pull-down/pull-up resistor for DQS pins. DQSRES[3] selects pull-down (when set to 0) or pull-up (when set to 1). DQSRES[2:0] selects the resistor value as follows: 000: open. The on-die resistor is disconnected. 001: 688 ohms 010: 611 ohms 011: 550 ohms 100: 500 ohms 101: 458 ohms 110: 393 ohms 111: 344 ohms Note: A DQS resistor must be connected for LPDDR2.
[3]	RW	dxpdr	Data power down receiver. If this bit is set, the input receiver on I/O is powered down for DQ, DM, and DQS/DQS# pins of all DATX8 macros. This bit is ORed with the PDR configuration bit of the individual DATX8(DXnGCR).
[2]	RW	dxpdd	Data power down driver. If this bit is set, the output driver on I/O is powered down for DQ, DM, and DQS/DQS# pins of all DATX8 macros. This bit is ORed with the PDD configuration bit of the individual DATX8(DXnGCR).
[1]	RW	dxiom	Data on-die termination. If this bit is set, the on-die termination on the I/O is enabled for DQ, DM, and DQS/DQS# pins of all DATX8 macros. This bit is ORed with the ODT configuration bit of the individual DATX8 (DXnGCR)
[0]	RW	dxodt	Data on-die termination. If this bit is set, the on-die termination on the I/O is enabled for DQ, DM, and DQS/DQS# pins of all DATX8 macros. This bit is ORed with the ODT configuration bit of the individual DATX8 (DXnGCR)

DDRC_PUB_DSGCR

DDRC_PUB_DSGCR is a DDR system general configuration register.

Offset Address	Register Name	Total Reset Value
0x42C	DDRC_PUB_DSGCR	0xFA00_001F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ckeoe	rstoe	odtoe	ckoe	tpdoe	tpdpd	nl2oe	nl2pd	odtpdd				ckepdd				reserved				dqsge				dqsgx				lpdllpd	lpiopd	zuen	bdisen	puren
Reset	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[31]	RW	ckeoe	SDRAM CKE output enable. If this bit is set, the output driver on the I/O is enabled for the SDRAM CKE pin.
[30]	RW	rstoe	SDRAM reset output enable. If this bit is set, the output driver on the I/O is enabled for the SDRAM RST# pin.
[29]	RW	odtoe	SDRAM ODT output enable. If this bit is set, the output driver on the I/O is enabled for the SDRAM ODT pin.
[28]	RW	ckoe	SDRAM CK output enable. If this bit is set, the output driver on the I/O is enabled for SDRAM CK/CK# pins.
[27]	RW	tpdoe	SDRAM TPD output enable (only for LPDDR). If this bit is set, the output driver on the I/O is enabled for the SDRAM TPD pin.
[26]	RW	tpdpd	SDRAM TPD power down driver (only for LPDDR). If this bit is set, the output driver on the I/O is powered down for SDRAM TPD pin. Note that the power down of the receiver on the I/O for SDRAM TPD pin is controlled by ACIOCR[ACPDR] register bit.
[25]	RW	nl2oe	Non-LPDDR2 output enable. If this bit is set, the output driver on the I/O is enabled for non-LPDDR2 (ODT, RAS#, CAS#, WE#, and BA) pins. This may be used when a chip designed for both LPDDR2 and other DDR modes is being used in LPDDR2 mode. For these pins, the I/O output enable signal (OE) is an AND of this bit and the respective output enable bit in the ACIOCR or DSGCR register.
[24]	RW	nl2pd	Non-LPDDR2 power down. If this bit is set, the output driver and the input receiver on the I/O are powered down for non-LPDDR2 (ODT, RAS#, CAS#, WE#, and BA) pins. This may be used when a chip designed for both LPDDR2 and other DDR modes is being used in LPDDR2 mode. For these pins, the I/O power down signal (PDD or PDR) is an OR of this bit and the respective power-down bit in the ACIOCR register.

[23:20]	RW	odtpdd	ODT power down driver. If this field is set, the output driver on the I/O is powered down for ODT[3:0] pins. ODTPDD[0] controls the power down for ODT[0], ODTPDD[1] controls the power down for ODT[1], and so on. Note: The actual reset value is calculated based on the configured number of ranks. For the Hi3518, each PUB supports one rank.
[19:16]	RW	ckepdd	CKE power down driver. If this field is set, the output driver on the I/O is powered down for CKE[3:0] pins. CKEPDD[0] controls the power down for CKE[0], CKEPDD[1] controls the power down for CKE[1], and so on. Note: The actual reset value is calculated based on the configured number of ranks. For the Hi3518, each PUB supports one rank.
[15:11]	RW	reserved	Reserved
[10:8]	RW	dqsge	DQS gate early. This field specifies the number of clock cycles during which the DQS gating must be enabled earlier than its normal position. This field is applicable only when the PDQSR I/O cell and passive DQS gating are used and there is no drift compensation. This field is recommended to be set to zero for all DDR types other than LPDDR2. For LPDDR2, this field is set to (tDQSCKmax − tDQSCK) divided by clock cycle and rounded up.
[7:5]	RW	dqsgx	DQS gate extension. This field specifies the number of clock cycles during which the DQS gating must be extended beyond the normal burst length width. This field is applicable only when the PDQSR I/O cell and passive DQS gating are used and there is no drift compensation. This field is recommended to be set to zero for all DDR types other than LPDDR2. For LPDDR2, this field is set to (tDQSCKmax − tDQSCK) divided by clock cycle and rounded up.
[4]	RW	lpdllpd	Low-power DLL power down. If this bit is set, the PHY must respond to the DFI low-power opportunity request and power down the DLL of the byte when the wakeup time request satisfies the DLL lock time.
[3]	RW	lpiopd	Low-power I/O power down. If this bit is set, it specifies that the PHY should respond to the DFI low-power opportunity request and power down the I/Os of the byte.
[2]	RW	zuen	Impedance update enable. If this bit is set, the PHY must perform impedance calibration (update) whenever there is a controller initiated DFI update request. Otherwise the PHY will ignore an update request from the controller.

[1]	RW	bdisen	Byte disable enable. If this bit is set, the PHY must respond to the DFI byte disable request. Otherwise the byte disable from the DFI is ignored, and therefore bytes can be disabled only by using the DXnGCR register.
[0]	RW	puren	PHY update request enable. If this bit is set, the PHY must issue a PHY-initiated DFI update request when there is DQS drift of more than 3/4 of a clock cycle within one continuous (back-to-back) read burst. The PHY issues PHY-initiated update requests and the controller must respond by default. Otherwise, the PHY may return erroneous values. The option to disable it is provided only for silicon evaluation and testing.

DDRC_PUB_DCR

DDRC_PUB_DCR is a DRAM configuration register.

Offset Address	Register Name	Total Reset Value
0x430	DDRC_PUB_DCR	0x0000_000B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tpd	rdimm	udimm	ddr2t	nosra	reserved																	ddrtype		mprdq	pdq					ddr8bnk	ddrmd		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1

Bits	Access	Name	Description
[31]	RW	tpd	Test power down (only for LPDDR). **Note: The Hi3518 does not support this function.**
[30]	RW	rdimm	Registered DIMM. **Note: The Hi3518 does not support this function.**
[29]	RW	udimm	Unbuffered DIMM address mirroring. **Note: The Hi3518 does not support this function.**
[28]	RW	ddr2t	DDR 2T timing. **Note: The Hi3518 does not support this function.**
[27]	RW	nosra	No simultaneous rank access. **Note: The Hi3518 does not support this function.**
[26:10]	RW	reserved	Reserved.

[9:8]	RW	ddrtype	DDR type. This field is used to select the DDR type for the specified DDR mode. The following are valid values for LPDDR2: 00: LPDDR2-S4 01: LPDDR2-S2 10: LPDDR2-NVM 11: reserved **Note: You do not need to configure this field.**
[7]	RW	mprdq	Multi-purpose register (MPR) DQ (only for DDR3). This field specifies the value that is driven on non-primary DQ pins during MPR reads. 0: The primary DQ drives out the data from MPR (0-1-0-1); non-primary DQs drive '0'. 1: The primary DQ and non-primary DQs all drive the same data from MPR (0-1-0-1).
[6:4]	RW	pdq	Primary DQ (only for DDR3). This field specifies the DQ pin in a byte that is designated as a primary pin for multi-purpose register (MPR) reads. The valid values 0−7 correspond to DQ[0] to DQ[7] respectively.
[3]	RW	ddr8bnk	DDR 8-bank. If this bit is set, the SDRAM used has eight banks. For tRPA, tRP+1 and tFAW are used for 8-bank DRAMs; for other tRPA, tRP but no tFAW is used. Note that a setting of 1 for DRAMs that have less than 8 banks still results in correct functionality but less tighter DRAM command spacing for the parameters described here.
[2:0]	RW	ddrmd	SDRAM DDR mode. 000: LPDDR (mobile DDR) 001: DDR 010: DDR2 011: DDR3 100: LPDDR2 (mobile DDR2) 101–111: reserved

DDRC_PUB_DTPR0

DDRC_PUB_DTPR0 is DRAM timing parameters register 0.

Offset Address	Register Name	Total Reset Value
0x434	DDRC_PUB_DTPR0	0x3092_666E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tccd	trc							trrd				tras				trcd				trp				twtr				trtp			tmrd
Reset	0	0	1	1	0	0	0	0	1	0	0	1	0	0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	1	1	1	0

Bits	Access	Name	Description
[31]	RW	tccd	Read to read and write to write command delay. 0: BL/2 for DDR2 and 4 for DDR3 1: BL/2 + 1 for DDR2 and 5 for DDR3
[30:25]	RW	trc	Activate to activate command delay (same bank). The valid value ranges from 2 to 42.
[24:21]	RW	trrd	Activate to activate command delay (different banks). The valid value ranges from 1 to 8.
[20:16]	RW	tras	Activate to precharge command delay. The valid value ranges from 2 to 31.
[15:12]	RW	trcd	Activate to read or write delay. The minimum time from when an activate command is issued to when a read or write to the activated row can be issued. The valid value range from 2 to 11.
[11:8]	RW	trp	Precharge command period. This field indicates the minimum time between a precharge command and any other command. **Note that the controller automatically derives tRPA for 8-bank DDR2 devices by adding 1 to tRP**. **The valid value ranges from 2 to 11.**
[7:5]	RW	twtr	Internal write to read command delay. The valid value ranges from 1 to 6.
[4:2]	RW	trtp	Internal read to precharge command delay. The valid value ranges from 2 to 6. Note that even though RTP does not apply to JEDEC DDR devices, this parameter must still be set to a minimum value of 2 for DDR because the controller always uses the following DDR2 equation to calculate the read to precharge timing (which is BL/2 for JEDEC DDR): AL + BL/2 + max(RTP, 2) – 2

[1:0]	RW	tmrd	Load mode cycle time. This field indicates the minimum time between a load mode register command and any other command. For DDR3, this field indicates the minimum time between two load mode register commands. The valid value for DDR2 ranges from 2 to 3. For DDR3, the value used for tMRD is 4 plus the value programmed in these bits. 00: 4 01: 5 10: 6 11: 7

DDRC_PUB_DTPR1

DDRC_PUB_DTPR1 is DRAM timing parameters register 1.

Offset Address	Register Name	Total Reset Value
0x438	DDRC_PUB_DTPR1	0x0983_0090

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				tdqsckmax				tdqsck				trfc				reserved				trtodt		tmod		tfaw				trtw		taondtaofd	
Reset	0	0	0	0	1	0	0	1	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:30]	RW	reserved	Reserved
[29:27]	RW	tdqsckmax	Maximum DQS output access time from CK/CK# (LPDDR2 only). This value is used for implementing read-to-write spacing. The valid value ranges from 1 to 7.
[26:24]	RW	tdqsck	DQS output access time from CK/CK# (only for LPDDR2). This value is used for calculating the read latency. The valid value ranges from 1 to 7. This value is derived from the corresponding parameter in the SDRAM data sheet divided by the clock cycle time without rounding up. The fractional remainder is automatically adjusted for by data training in quarter clock cycle units. If data training is not performed, this fractional remainder must be converted into quarter clock cycle units and the gating registers (DXnDQSTR) are adjusted accordingly.

[23:16]	RW	trfc	Refresh-to-refresh. This field indicates the minimum time between two refresh commands or between a refresh and an active command. The value unit is clock cycle. The value is derived from the minimum refresh interval from the data sheet, tRFC(min), divided by the clock cycle time. The default number of clock cycles is the greatest value in tRFC(min) defined in the JEDEC protocol.
[15:12]	RW	reserved	Reserved
[11]	RW	trtodt	Read to ODT delay (only for DDR3). This field specifies whether ODT can be enabled immediately after the read postamble or one clock delay has been added. 0: ODT may be turned on immediately after read postamble. 1: ODT may not be turned on until one clock after the read postamble. If tRTODT is set to 1 and ODT is enabled, the read-to-write latency increases by 1.
[10:9]	RW	tmod	Load mode update delay (only for DDR3). This field indicates the minimum time between a load mode register command and a non-load mode register command. 00: 12 01: 13 10: 14 11: 15
[8:3]	RW	tfaw	4-bank activate period. No more than 4-bank activate commands may be issued in a specified tFAW period. This field applies only to 8-bank devices. The valid value ranges from 2 to 31.
[2]	RW	trtw	Read to write command delay. 0: standard bus turn around delay 1: add 1 clock to standard bus turn around delay This parameter allows the user to increase the delay between issuing write commands to the SDRAM when preceded by read commands. This provides an option to increase bus turn-around margin for high-frequency systems.

[1:0]	RW	taondtaofd	ODT turn-on/turn-off delays (only for DDR2). The delay unit is clock cycle. 00: 2/2.5 01: 3/3.5 10: 4/4.5 11: 5/5.5 Most DDR2 devices use the fixed value 2/2.5. For non-standard SDRAMs, the user must ensure that the operational write latency is always greater than or equal to the ODT turn-on delay. For example, if the CAS latency, CAS additive latency, and write latency for a DDR2 SDRAM is 3, 0, and 2 respectively, the 2/2.5 but not 3/3.5 or larger can be used.

DDRC_PUB_DTPR2

DDRC_PUB_DTPR2 is DRAM timing parameters register 2.

Offset Address	Register Name	Total Reset Value
0x43C	DDRC_PUB_DTPR2	0x1001_A0C8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				tdllk												tcke				txp				txs							
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0	1	1	0	0	1	0	0	0

Bits	Access	Name	Description
[31:29]	RW	reserved	Reserved.
[28:19]	RW	tdllk	DLL locking time. The valid value ranges from 2 to 1023.
[18:15]	RW	tcke	CKE minimum pulse width. This field also specifies the minimum time during which the SDRAM must remain in power-down or self-refresh mode. For DDR3, this parameter must be set to the value of tCKESR that is usually greater than the value of tCKE. The valid value ranges from 2 to 15.
[14:10]	RW	txp	Power down exit delay. This field indicates the minimum time between a power down exit command and any other command. This parameter must be set to the maximum value among the various minimum power down exit delay parameters specified in the SDRAM data sheet, for example, max(tXP, tXARD, tXARDS) for DDR2 and max(tXP, tXPDLL) for DDR3. The valid value ranges from 2 to 31.

[9:0]	RW	txs	Self refresh exit delay. This field indicates the minimum time between a self refresh exit command and any other command. This parameter must be set to the maximum value among the various minimum self refresh exit delay parameters specified in the SDRAM data sheet, for example, max(tXSNR, tXSRD) for DDR2 and max(tXS, tXSDLL) for DDR3. The valid value ranges from 2 to 1023.

DDRC_PUB_MR0

DDRC_PUB_MR0 is mode register 0.

Offset Address	Register Name	Total Reset Value
0x440	DDRC_PUB_MR0	0x0000_0A52

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																mr0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	1	0	0	1	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved
[15:0]	RW	mr0	SDRAM mode register 0 (MR0). This field corresponds to valid bits 13−0 of mode register 0 (MR0) in the DDRn SDRAM user manual. DDRC_PUB_MR0 bit[15:14] must be set to 0b00. **Note: For details about MR0, see the DDRn SDRAM user manual**.

DDRC_PUB_MR1

DDRC_PUB_MR1 is mode register 1.

Offset Address	Register Name	Total Reset Value
0x444	DDRC_PUB_MR1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																mr1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved
[15:0]	RW	mr1	SDRAM extended mode register 1 (EMR1). This field corresponds to valid bits 13−0 of mode register 1 (MR1) in the DDRn SDRAM user manual. DDRC_PUB_MR1 bit[15:14]

			must be set to 0b00. **Note: For details about MR1, see the DDRn SDRAM user manual**.

DDRC_PUB_MR2

DDRC_PUB_MR2 is mode register 2.

Offset Address	Register Name	Total Reset Value
0x448	DDRC_PUB_MR2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																mr2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved
[15:0]	RW	mr2	This field corresponds to valid bits 13−0 of mode register 2 (MR2) in the DDRn SDRAM user manual. DDRC_PUB_MR2 bit[15:14] must be set to 0b00. **Note: For details about MR2, see the DDRn SDRAM user manual**.

DDRC_PUB_MR3

DDRC_PUB_MR3 is mode register 3.

Offset Address	Register Name	Total Reset Value
0x44C	DDRC_PUB_MR3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																mr3															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved
[15:0]	RW	mr3	SDRAM extended mode register 3 (EMR3) This field corresponds to valid bits 13−0 of mode register 1 (MR1) in the DDRn SDRAM user manual. DDRC_PUB_MR3 bit[15:14] must be set to 0b00. **Note: For details about MR3, see the DDRn SDRAM user manual**.

DDRC_PUB_ODTCR

DDRC_PUB_ODTCR is an ODT configuration register.

Offset Address	Register Name	Total Reset Value
0x450	DDRC_PUB_ODTCR	0x0001_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	wrodt3	wrodt2	wrodt1	wrodt0	rdodt3	rdodt2	rdodt1	rdodt0
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RW	wrodt3	Write ODT: rank select. The description is the same as wodt0. Note: The actual reset value is calculated based on the configured number of ranks. The Hi3518 does not support the configuration.
[27:24]	RW	wrodt2	Write ODT: rank select. The description is the same as wodt0. Note: The actual reset value is calculated based on the configured number of ranks. The Hi3518 does not support the configuration.
[23:20]	RW	wrodt1	Write ODT: rank select. The description is the same as wodt0.
[19:16]	RW	wrodt0	Write ODT: specifies whether ODT should be enabled ('1') or disabled ('0') on each of at most four ranks when a write command is sent to rank n. WRODT0, WRODT1, WRODT2, and WRODT3 specify ODT settings when a write is to rank 0, rank 1, rank 2, and rank 3 respectively. The four bits of each field each represent a rank, the LSB being rank 0 and the MSB being rank 3. The ODT is enabled only on the rank that is being written to by default.
[15:12]	RW	rdodt3	Read ODT: rank select. The description is the same as rodt0. Note: The actual reset value is calculated based on the configured number of ranks. The Hi3518 does not support the configuration.
[11:8]	RW	rdodt2	Read ODT: rank select. The description is the same as rodt0. Note: The actual reset value is calculated based on the configured number of ranks. The Hi3518 does not support the configuration.
[7:4]	RW	rdodt1	Read ODT: rank select. The description is the same as rodt0.
[3:0]	RW	rdodt0	Read ODT: specifies whether ODT should be enabled ('1') or disabled ('0') on each of at most four ranks when a read command is sent to rank n. RDODT0, RDODT1, RDODT2, and RDODT3 specify ODT settings when a read is to rank 0, rank 1, rank 2, and rank 3 respectively. The four bits of each field each represent a rank, the LSB being rank 0 and the MSB being rank 3. The ODT is disabled during reads by default.

DDRC_PUB_DTAR

DDRC_PUB_DTAR is a data training address register.

Offset Address	Register Name	Total Reset Value
0x454	DDRC_PUB_DTAR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dtmpr	dtbank			dtrow																dtcol											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	dtmpr	Data training using MPR (only for DDR3). If this bit is set, the SDRAM multi-purpose register (MPR) should be used during data training. Otherwise, data training is performed by first writing to some locations in the SDRAM and then reading them back.
[30:28]	RW	dtbank	Data training bank address. This field is used to select the SDRAM bank address to be used during data training.
[27:12]	RW	dtrow	Data training row address. This field is used to select the SDRAM row address to be used during data training.
[11:0]	RW	dtcol	Data training column address. This field is used to select the SDRAM column address to be used during data training. The lower four bits of this address must always be "0000".

DDRC_PUB_DTDR0

DDRC_PUB_DTDR0 is data training data register 0.

Offset Address	Register Name	Total Reset Value
0x458	DDRC_PUB_DTDR0	0xDD22_EE11

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dtbyte3								dtbyte2								dtbyte1								dtbyte0							
Reset	1	1	0	1	1	1	0	1	0	0	1	0	0	0	1	0	1	1	1	0	1	1	1	0	0	0	0	1	0	0	0	1

Bits	Access	Name	Description
[31:24]	RW	dtbyte3	Data training data. This field indicates the fourth byte of data used during data training. The same data byte is used for each byte lane. The default sequence is a walking 1 while data toggling every data cycle.
[23:16]	RW	dtbyte2	Data training data. This field indicates the third byte of data used during data training.

			This same data byte is used for each byte lane. The default sequence is a walking 1 while data toggling every data cycle.
[15:8]	RW	dtbyte1	Data training data. This field indicates the second byte of data used during data training. This same data byte is used for each byte lane. The default sequence is a walking 1 while data toggling every data cycle.
[7:0]	RW	dtbyte0	Data training data. This field indicates the first byte of data used during data training. This same data byte is used for each byte lane. The default sequence is a walking 1 while data toggling every data cycle.

DDRC_PUB_DTDR1

DDRC_PUB_DTDR1 is data training data register 1.

Offset Address	Register Name	Total Reset Value
0x45C	DDRC_PUB_DTDR1	0x7788_BB44

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dtbyte7								dtbyte6								dtbyte5								dtbyte4							
Reset	0	1	1	1	0	1	1	1	1	0	0	0	1	0	0	0	1	0	1	1	1	0	1	1	0	1	0	0	0	1	0	0

Bits	Access	Name	Description
[31:24]	RW	dtbyte7	Data training data. This field indicates the eighth byte of data used during data training. This same data byte is used for each byte lane. The default sequence is a walking 1 while data toggling every data cycle.
[23:16]	RW	dtbyte6	Data training data. This field indicates the seventh byte of data used during data training. This same data byte is used for each byte lane. The default sequence is a walking 1 while data toggling every data cycle.
[15:8]	RW	dtbyte5	Data training data. This field indicates the sixth byte of data used during data training. This same data byte is used for each byte lane. The default sequence is a walking 1 while data toggling every data cycle.
[7:0]	RW	dtbyte4	Data training data. This field indicates the fifth byte of data used during data training. This same data byte is used for each byte lane. The default sequence is a walking 1 while data toggling every data cycle.

DDRC_PUB_ZQ_CTRL0

DDRC_PUB_ZQ_CTRL0 is PUB DDR PHY I/O compensation configuration register 0.

Offset Address	Register Name	Total Reset Value
0x580	DDRC_PUB_ZQ_CTRL0	0x0000_014A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	zqpd		zcal		zcalbyp		zden		zdata																							
Reset	0		0		0		0		0		0		0		0		0		0		0		0		0		1		0		1	
Reset	0		0		0		0		0		0		0		0		0		0		0		0		1		0		0		1	
Reset	0		0		0		0		0		0		0		0		0		0		0		0		0		1		0		1	
Reset	0		0		0		0		0		0		0		0		0		0		0		0		1		0		0		1	

Bits	Access	Name	Description
[31]	RW	zqpd	ZQ power down. 0: normal mode 1: The ZQ PAD power supply is shut down to implement low-power control.
[30]	RW	zcal	Impedance calibration enable. Writing 1 enables the impedance auto-calibration logic. This field is automatically cleared after calibration.
[29]	RW	zcalbyp	Impedance compensation bypass mode. 0: automatic 1: ZQ auto-calibration is disabled. Calibration can be manually enabled.
[28]	RW	zden	Impedance compensation mode. 0: auto-compensation mode 1: customer-specific mode
[27:0]	RW	zdata	Impedance calibration configuration. zdata[27:20]: reserved zdata[19:15]: ODT pull-up impedance zdata[14:10]: ODT pull-down impedance zdata[9:5]: output pull-up impedance zdata[4:0]: output pull-down impedance

DDRC_PUB_ZQ_CTRL1

DDRC_PUB_ZQ_CTRL1 is PUB DDR PHY I/O compensation configuration register 1.

Offset Address	Register Name	Total Reset Value
0x584	DDRC_PUB_ZQ_CTRL1	0x0000_007B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								zprog_odt				zprog_drv			

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	1

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.
[7:4]	RW	zprog_odt	I/O matched impedance divide ratio select.
[3:0]	RW	zprog_drv	I/O drive impedance divide ratio select.

DDRC_PUB_ZQ_STATUS0

DDRC_PUB_ZQ_STATUS0 is DDR PHY I/O compensation status register 0.

Offset Address	Register Name	Total Reset Value
0x588	DDRC_PUB_ZQ_STATUS0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	zdone	zerr	reserved		zctrl																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	zdone	Impedance calibration completion indicator. 0: Impedance calibration does not start or impedance is being calibrated. 1: Impedance calibration is complete.
[30]	RO	zerr	Impedance calibration error indicator. 0: normal 1: error
[29:28]	RO	reserved	Reserved.
[27:0]	RO	zctrl	Impedance calibration configuration. zctrl[27:20]: reserved zctrl[19:15]: ODT pull-up impedance zctrl[14:10]: ODT pull-down impedance zctrl[9:5]: output pull-up impedance zctrl[4:0]: output pull-down impedance

DDRC_PUB_ZQ_STATUS1

DDRC_PUB_ZQ_STATUS1 is DDR PHY I/O compensation status register 1.

Offset Address	Register Name	Total Reset Value
0x58C	DDRC_PUB_ZQ_STATUS1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								opu		opd		zpu		zpd	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:6]	RO	opu	ODT impedance pull-up calibration status. 00: Impedance calibration is complete and no error occurs. 01: An overflow error occurs. 10: An underflow error occurs. 11: Calibration is in progress.
[5:4]	RO	opd	ODT impedance pull-down calibration status. 00: Impedance calibration is complete and no error occurs. 01: An overflow error occurs. 10: An underflow error occurs. 11: Calibration is in progress.
[3:2]	RO	zpu	Output impedance pull-up calibration status. 00: Impedance calibration is complete and no error occurs. 01: An overflow error occurs. 10: An underflow error occurs. 11: Calibration is in progress.
[1:0]	RO	zpd	Output impedance pull-down calibration status. 00: Impedance calibration is complete and no error occurs. 01: An overflow error occurs. 10: An underflow error occurs. 11: Calibration is in progress.

DDRC_PUB_DXNGCR

DDRC_PUB_DXNGCR is a DATX8 general configuration register.

Offset Address	Register Name	Total Reset Value
0x5C0 + 0x40 x blanes blanes(0−1)	DDRC_PUB_DXNGCR	0x0000_0E81

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		rttoal	rttoh		dqrtt	dqsrtt	dsen		dqsrpd	dxpdr	dxpdd	dxiom	dqodt	dqsodt	dxen
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:14]	RW	reserved	Reserved
[13]	RW	rttoal	RTT on additive latency. This bit indicates the time when the ODT control of DQ/DQS SSTL I/Os is set to the value in DQODT/DQSODT during read cycles. 0: ODT control is set to DQSODT/DQODT almost two cycles before read data preamble 1: ODT control is set to DQSODT/DQODT almost one cycle before read data preamble
[12:11]	RW	rttoh	RTT output hold. This field indicates the number of clock cycles (from 0 to 3) after the read data postamble during which ODT control should retain DQSODT for DQS or DQODT for DQ/DM before it is disabled (setting it to '0') when dynamic ODT control is used. ODT is disabled almost RTTOH clock cycles after the read postamble.
[10]	RW	dqrtt	DQ dynamic RTT control. If this bit is set, the ODT control of DQ/DM SSTL I/Os is dynamically controlled by setting it to the value in DQODT during reads and disabling it (setting it to '0') during any other cycle. If this bit is not set, the ODT control of DQ SSTL I/Os is always set to the value in DQODT.
[9]	RW	dqsrtt	DQS dynamic RTT control. If this bit is set, the ODT control of DQS SSTL I/Os is dynamically controlled by setting it to the value in DQSODT during reads and disabling it (setting it to '0') during any other cycle. If this bit is not set, the ODT control of DQS SSTL I/Os is always set to the value in DQSODT field.

[8:7]	RW	dsen	Write DQS enable. This field is used to control whether the write DQS going to the SDRAM is enabled (toggling) or disabled (static value) and whether the DQS is inverted. DQS# is always the inversion of DQS. These values are valid only when DQS/DQS# output enable is on; otherwise, the DQS/DQS# is tristated. 00: DQS disabled (driven to constant 0) 01: DQS toggling with inverted polarity 10: DQS toggling with normal polarity (This should be the default setting) 11: DQS disabled (driven to constant 1)
[6]	RW	dqsrpd	DQSR power down. If this bit is set, the PDQSR cell is powered down.
[5]	RW	dxpdr	Data power down receiver. If this bit is set, the input receiver on I/O is powered down for DQ, DM, and DQS/DQS# pins of the byte.
[4]	RW	dxpdd	Data power down driver. If this bit is set, the output driver on I/O is powered down for DQ, DM, and DQS/DQS# pins of the byte.
[3]	RW	dxiom	Data I/O mode. This bit is used to select the SSTL mode (when set to 0) or CMOS mode (when set to 1) of the I/O for DQ, DM, and DQS/DQS# pins of the byte.
[2]	RW	dqodt	Data on-die termination. If this bit is set, the on-die termination on the I/O is enabled for DQ and DM pins of the byte.
[1]	RW	dqsodt	DQS on-die termination. If this bit is set, the on-die termination on the I/O is enabled for DQS/DQS# pin of the byte.
[0]	RW	dxen	Data byte enable. If this bit is set, the DATX8 and SSTL I/Os used on the data byte are enabled. Setting this bit to '0' disables the byte. For example, the byte SSTL I/Os enter the power-down mode and the DLL in the DATX8 enters the bypass mode.

DDRC_PUB_DXNGSR0

DDRC_PUB_DXNGSR0 is DATX8 general status register 0.

Offset Address	Register Name	Total Reset Value
0x5C4 + 0x40 x blanes blanes(0−1)	DDRC_PUB_DXNGSR0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								dtpass											reserved	dtierr				dterr				dtdone			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:13]	RO	dtpass	Data training pass count. **This field indicates the number of passing configurations during DQS gate training. Bits [2:0] are for rank 0, bits [5:3] for rank 1, and so on.**
[12]	RO	reserved	Reserved
[11:8]	RO	dtierr	Data training intermittent error. If this field is set, there is an intermittent error during data training of the byte. For example, a pass is followed by a failure and then another pass. Bit [0] is for rank 0, bit 1 for rank 1, and so on.
[7:4]	RO	dterr	Data training error. If this field is set, a valid DQS gating window cannot be found during data training of the byte. Bit [0] is for rank 0, bit 1 for rank 1, and so on.
[3:0]	RO	dtdone	Data training done. If this field is set, the byte has finished data training. Bit [0] is for rank 0, bit 1 for rank 1, and so on.

DDRC_PUB_DXNGSR1

DDRC_PUB_DXNGSR1 is DATX8 general status register 1.

Offset Address	Register Name	Total Reset Value
0x5C8 + 0x40 x blanes blanes(0−1)	DDRC_PUB_DXNGSR1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				dqsdft								dfterr			

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:4]	RO	dqsdft	DQS drift. This field is used to report the drift on the read data strobe of the data byte. 00: no drift 01: 90° drift 10: 180° drift 11: 270° drift or more **Bits [1:0] are for rank 0, bits [3:2] for rank 1, and so on.**
[3:0]	RO	dfterr	DQS drift error. If this field is set, the byte read data strobe has drifted by more than or equal to the drift limit configured in the PHY general configuration register (PGCR). Bit [0] is for rank 0, bit 1 for rank 1, and so on.

DDRC_PUB_DXNDLLCR

DDRC_PUB_DXNDLLCR is a DATX8 DLL control register.

Offset Address	Register Name	Total Reset Value
0x5CC + 0x40 x blanes blanes(0−1)	DDRC_PUB_DXNDLLCR	0x4000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dlldis	dllsrst	reserved										sdlbmode	atesten	sdphase				sstart		mfwdly				mfbdly				sfwdly				sfbdly			
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	dlldis	DLL disable. A disabled DLL is bypassed. The default value 0 indicates that the DLL is enabled.
[30]	RW	dllsrst	DLL soft reset. This bit is used to soft-reset the byte DLL by driving the DLL soft reset pin.
[29:20]	RW	reserved	Reserved.

[19]	RW	sdlbmode	Slave DLL loopback mode. If this bit is set, the slave DLL enters the loopback mode in which there is no 90º phase shift on read DQS/DQS#. This bit must be set when the byte PHYs are operated in loopback mode such as during BIST loopback. This bit applies only to the PHYs that have this feature. For details, see the PHY data book.
[18]	RW	atesten	Analog test enable. This bit is used to enable the analog test signal to be output on the DLL analog test output (test_out_a). The DLL analog test output is tristated when this bit is 0.
[17:14]	RW	sdphase	Slave DLL phase trim. This field is used to select the phase difference between the input clock and the corresponding output clock of the slave DLL. 0000: 90 0001: 72 0010: 54 0011: 36 0100: 108 0101: 90 0110: 72 0111: 54 1000: 126 1001: 108 1010: 90 1011: 72 1100: 144 1101: 126 1110: 108 1111: 90
[13:12]	RW	sstart	Slave auto startup. This field is used to control how the slave DLL starts up relative to the master DLL locking: 0X: Slave DLL automatically starts up once the master DLL is locked. 10: The automatic startup of the slave DLL is disabled, and the phase detector is disabled. 11: The automatic startup of the slave DLL is disabled, and the phase detector is enabled.
[11:9]	RW	mfwdly	Master feed-forward delay trim. This field is used to trim the delay in the master DLL feed-forward path. 000: minimum delay 111: maximum delay

[8:6]	RW	mfbdly	Master feedback delay trim. This field is used to trim the delay in the master DLL feedback path. 000: minimum delay 111: maximum delay
[5:3]	RW	sfwdly	Slave feed-forward delay trim. This field is used to trim the delay in the slave DLL feed-forward path. 000: minimum delay 111: maximum delay
[2:0]	RW	sfbdly	Slave feed-back delay trim. This field is used to trim the delay in the slave DLL feedback path. 000: minimum delay 111: maximum delay

DDRC_PUB_DXNDQTR

DDRC_PUB_DXNDQTR is a DATX8 DQ timing register.

Offset Address	Register Name	Total Reset Value
0x5D0 + 0x40 x blanes blanes(0−1)	DDRC_PUB_DXNDQTR	0xFFFF_FFFF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dqdly7	dqdly6	dqdly5	dqdly4	dqdly3	dqdly2	dqdly1	dqdly0
Reset	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:28]	RW	dqdly7	DQ7 delay. The description is the same as DQ0 delay.
[27:24]	RW	dqdly6	DQ6 delay. The description is the same as DQ0 delay.
[23:20]	RW	dqdly5	DQ5 delay. The description is the same as DQ0 delay.
[19:16]	RW	dqdly4	DQ4 delay. The description is the same as DQ0 delay.
[15:12]	RW	dqdly3	DQ3 delay. The description is the same as DQ0 delay.
[11:8]	RW	dqdly2	DQ2 delay. The description is the same as DQ0 delay.

[7:4]	RW	dqdly1	DQ1 delay. The description is the same as DQ0 delay.
[3:0]	RW	dqdly0	DQ0 delay. This field is used to adjust the delay of the data relative to the nominal delay that matches the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. DQDLY0 controls the delay of data bit [0], DQDLY1 controls data bit [1], and so on. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the upper two bits control the delay for the data clocked by DQS_b. The following are valid settings for each 2-bit control field: 00: nominal delay 01: nominal delay + 1 step 10: nominal delay + 2 steps 11: nominal delay + 3 steps Note: The step size can be queried in the data books of compatible DWC DDR PHYs.

DDRC_PUB_DXNDQSTR

DDRC_PUB_DXNDQSTR is a DATX8 DQS timing register.

Offset Address	Register Name	Total Reset Value
0x5D4 + 0x40 x blanes blanes(0−1)	DDRC_PUB_DXNDQSTR	0x3DB0_1000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		dmdly				dqsndly		dqsdly				r3dgps		r2dgps		r1dgps		r0dgps		r3dgsl		r2dgsl		r1dgsl		r0dgsl					
Reset	0	0	1	1	1	1	0	1	1	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RW	reserved	Reserved

[29:26]	RW	dmdly	DM delay. This field is used to adjust the delay of the data mask relative to the nominal delay that matches the delay of the data strobes through the slave DLL and clock tree. The lower two bits of the DQMDLY controls the delay for the data clocked by DQS, while the upper two bits control the delay for the data clocked by DQS_b. The following are valid settings for each 2-bit control field: 00: nominal delay 01: nominal delay + 1 step 10: nominal delay + 2 steps 11: nominal delay + 3 steps Note: The step size can be queried in the data books of compatible DWC DDR PHYs.
[25:23]	RW	dqsndly	DQS# delay. This field is used to adjust the delay of the data strobes relative to the nominal delay that matches the delay of the data bit through the slave DLL and clock tree. DQSDLY controls the delay on DQS strobe and DQSNDLY controls the delay on DQS#. 000: nominal delay − 3 steps 001: nominal delay − 2 steps 010: nominal delay − 1 step 011: nominal delay 100: nominal delay + 1 step 101: nominal delay + 2 steps 110: nominal delay + 3 steps 111: nominal delay + 4 steps Note: The step size can be queried in the data books of compatible DWC DDR PHYs.
[22:20]	RW	dqsdly	DQS. This field is used to adjust the delay of the data strobes relative to the nominal delay that matches the delay of the data bit through the slave DLL and clock tree. DQSDLY controls the delay on DQS strobe and DQSNDLY controls the delay on DQS#. 000: nominal delay − 3 steps 001: nominal delay − 2 steps 010: nominal delay − 1 step 011: nominal delay 100: nominal delay + 1 step 101: nominal delay + 2 steps 110: nominal delay + 3 steps 111: nominal delay + 4 steps **Note: The step size can be queried in the data books of compatible DWC DDR PHYs.**

[19:18]	RW	r3dgps	Rank 3 DQS gating phase select. The description is the same as r0dgps. **Note: The actual reset value is calculated based on the configured number of ranks. The Hi3518 does not support the configuration.**
[17:16]	RW	r2dgps	Rank 2 DQS gating phase select. The description is the same as r0dgps. **Note: The actual reset value is calculated based on the configured number of ranks. The Hi3518 does not support the configuration.**
[15:14]	RW	r1dgps	Rank 1 DQS gating phase select. The description is the same as r0dgps. The Hi3518 does not support the configuration.
[13:12]	RW	r0dgps	Rank 0 DQS gating phase select. This field is used to select the clock used to enable the data strobes during read, so that the value of the data strobes before and after the preamble/postamble are filtered out. The RnDGPS fields are initially set by the PUBL during automatic DQS data training and subsequently updated during data strobe drift compensation. However, these values can be overwritten by a direct write to this register, and the automatic update during DQS drift compensation can be disabled using the PHY general configuration register (PGCR). Every two bits of this register control the DQS gating for each of at most four ranks. R0DGPS controls the DQS gating for rank 0, R1DGPS controls rank 1, and so on. The following are valid values for each 2-bit RnDGPS field: 00: 90° clock (clk90) 01: 180° clock (clk180) 10: 270° clock (clk270) 11: 360° clock (clk0)
[11:9]	RW	r3dgsl	Rank 3 DQS gating system latency. The description is the same as r0dgsl. **Note: The actual reset value is calculated based on the configured number of ranks. The Hi3518 does not support the configuration.**
[8:6]	RW	r2dgsl	Rank 2 DQS gating system latency. The description is the same as r0dgsl. **Note: The actual reset value is calculated based on the configured number of ranks. The Hi3518 does not support the configuration.**
[5:3]	RW	r1dgsl	Rank 1 DQS gating system latency. The description is the same as r0dgsl.

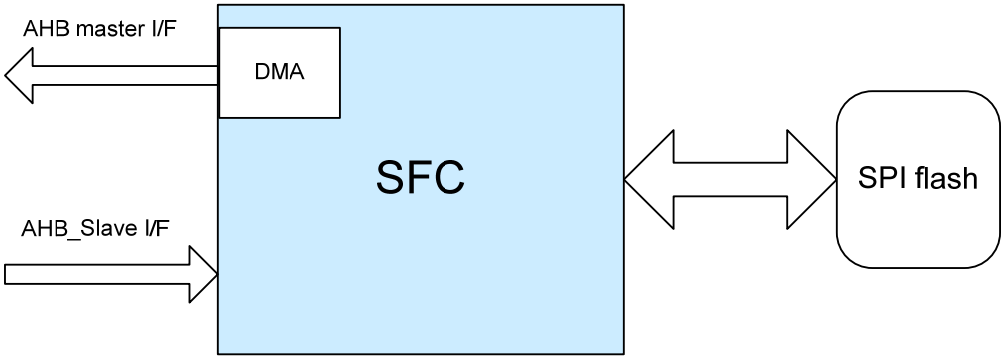
[2:0]	RW	r0dgsl	Rank 0 DQS gating system latency. This field is used to increase the number of clock cycles required for obtaining valid DDR read data. At most five extra clock cycles are supported. This is used to compensate for board delays and other system delays. The value 000 indicates power-on by default (for example, no extra clock cycles are required). The SL fields are initially set by the PUBL during automatic DQS data training but these values can be overwritten by a direct write to this register. Every three bits of this register control the latency of each of at most four ranks. R0DGSL controls the latency of rank 0, R1DGSL controls rank 1, and so on. 000: no extra clock cycles 001: 1 extra clock cycle 010: 2 extra clock cycles 011: 3 extra clock cycles 100: 4 extra clock cycles 101: 5 extra clock cycles 110: reserved 111: reserved

4.2 SPI Flash Controller

4.2.1 Overview

The serial peripheral interface flash controller (SFC) is a SPI flash controller. The SFC provides an AHB slave interface on the service side to control access to the SPI flash through the AHB channel and provides an AHB master interface to read and write to the SPI flash in direct memory access (DMA) mode.

Figure 4-3 SFC application block diagram



4.2.2 Features

4.2.2.1 AHB Slave Interface

The AHB slave interface has the following features:

- Provides an AHB slave interface to allow users to access an internal configuration register or the SPI flash memory based on the selected signal.
- Supports the advanced microcontroller bus architecture 2.0 (AMBA 2.0) protocol.
- Supports the little endian mode.

4.2.2.2 AHB Master Interface

The AHB master interface has the following features:

- Provides an AHB master interface for transferring data between the memory and flash memory in DMA mode.
- Supports the AMBA2.0 protocol.
- Supports only the little endian mode.
- Provides the transfer modes such as Single, INCR4, INCR8, and INCR16.
- Does not support early termination.
- Supports lock transfer.

4.2.2.3 Memory Interface

The memory interface has the following features:

- Supports only one CS. Supports a maximum of 128 Mbits (in 3-byte address mode) or 8 Gbits (in 4-byte address mode) storage space. In addition, the SPI flash can be mapped to the system address space. The mapping base address can be configured. The mapping system space must be within the space of 0x58000000–0x5BFFFFFF.
- Supports address aliasing. Address 0 can be mapped to the SPI flash by address aliasing after power-on to boot the chip from the SPI flash.
- Supports the standard SPI, dual input/dual-output SPI, quad-output/qual-input SPI, dual I/O SPI, quad-I/O SPI, full DIO SPI, and full QIO SPI. After power-on, the standard SPI is selected by default. You can change the interface type by configuring the corresponding registers.
- Supports two flash address modes: 3-byte address mode and 4-byte address mode. You can set the default address mode by pulling up or down the SFC_ADDR_MODE pin (multiplexed with the SFC_CLK pin), and switch the address mode by configuring registers. The 3-byte address mode supports a maximum capacity of 128 Mbits. The 4-byte address mode supports a maximum capacity of 8 Gbits.
- Supports read/write operations by means of bus, register programming, or DMA.
- Supports various write protection operations.

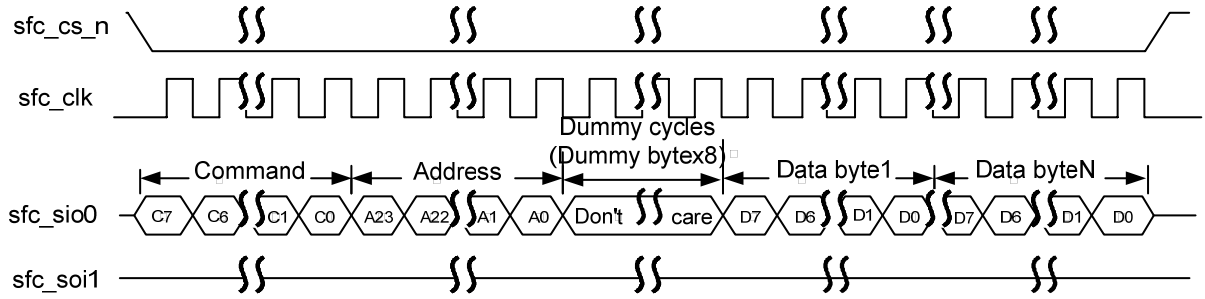
4.2.3 Function Description

4.2.3.1 Interface Mode Timing

Standard SPI

In standard SPI interface mode, a 1-bit data input line and a 1-bit data output line are supported. Figure 4-27 and Figure 4-28 show the timings of the standard SPI interface.

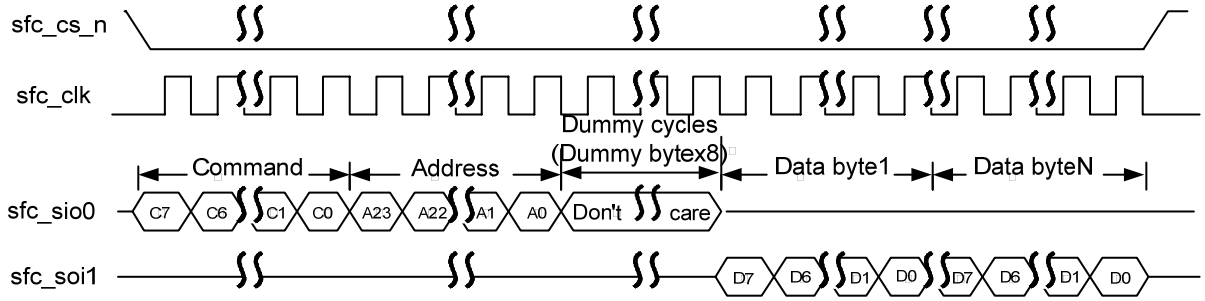
Figure 4-27 Timing of the standard SPI interface (write)



NOTE

- The opcode bytes, address bytes, and dummy bytes are output in unit of a single bit in serial mode through the sfc_sio0 line.
- The data bytes are output in unit of a single bit in serial mode through the sfc_soi0 line.

Figure 4-28 Timing of the standard SPI interface (read)



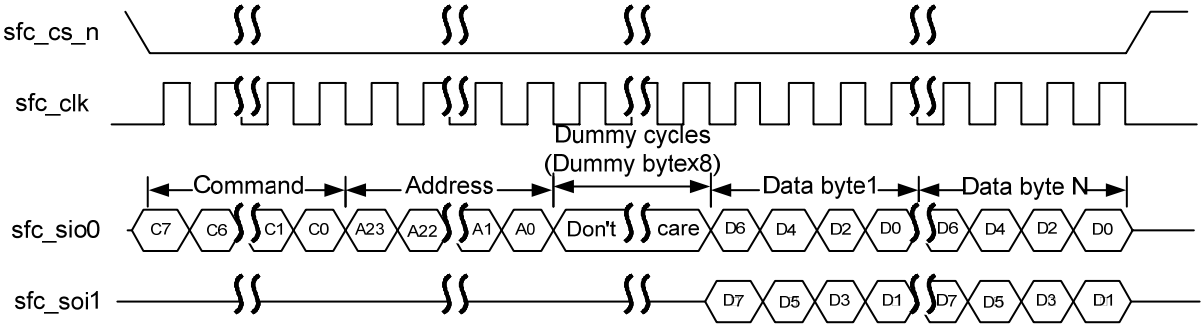
NOTE

- The opcode bytes, address bytes, and dummy bytes are output in unit of a single bit in serial mode through the sfc_sio0 line.
- The data bytes are output in unit of a single bit in serial mode through the sfc_soi1 line.

Dual Input/Dual Output SPI

In dual input/dual output SPI mode, 2-bit bidirectional data lines are supported. Figure 4-30 shows the timing in dual input/dual output SPI mode.

Figure 4-30 Timing of the dual input/dual output SPI interface



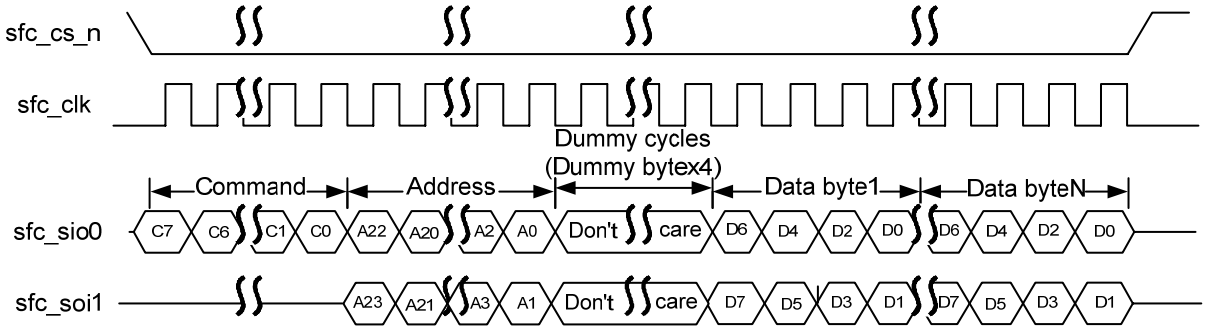
NOTE

- The opcode bytes, address bytes, and dummy bytes are output in unit of a single bit in serial mode through the sfc_sio0 line.
- The data bytes are output (write) and input (read) in unit of dual bits through the sfc_sio0 or sfc_soi1 line.

Dual I/O SPI

In dual I/O SPI interface mode, 2-bit bidirectional data lines are supported. Figure 4-31 shows the timing in dual I/O SPI interface mode.

Figure 4-31 Timing of the dual I/O SPI interface



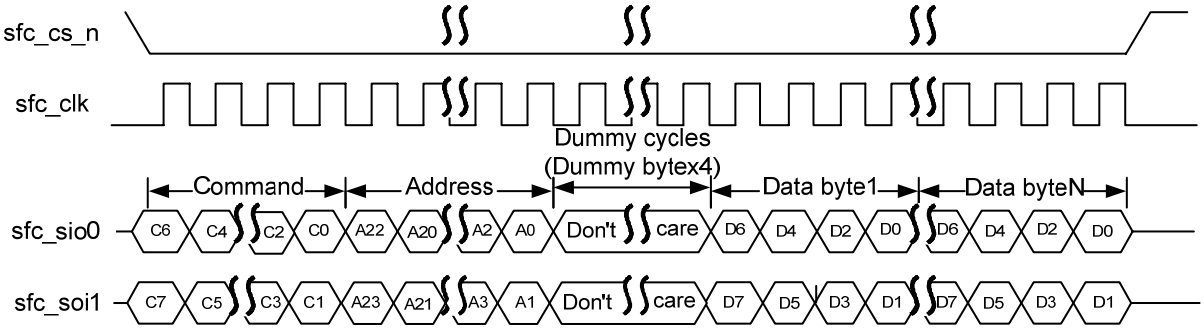
NOTE

- The opcode bytes are output in unit of a single bit in serial mode through the sfc_sio0 line. The address bytes and dummy bytes are output in unit of dual bits through the sfc_sio0 or sfc_soi1 line.
- The data bytes are output (write) or input (read) in unit of dual bits through the sfc_sio0 or sfc_soi1 line.

Full Dual I/O SPI

In full dual I/O SPI mode, 2-bit bidirectional data lines are supported. Figure 4-32 shows the timing in full dual I/O SPI mode.

Figure 4-32 Timing of the full dual−I/O SPI interface



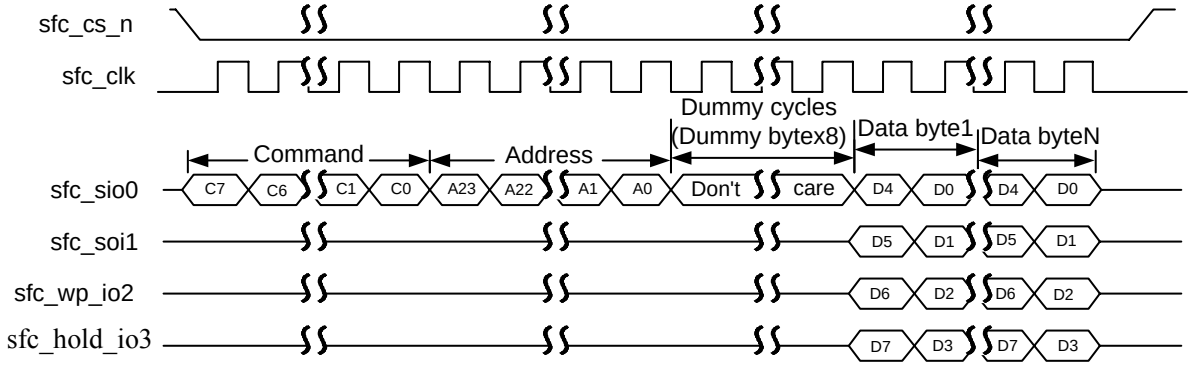
NOTE

- The opcode bytes, address bytes, and dummy bytes are output in unit of dual bits through thesfc_sio0 or sfc_soi1 line.
- The data bytes are output (write) or input (read) in unit of dual bits through the sfc_sio0, sfc_soi1, sfc_wp, or sfc_hold line.

Quad Input/Quad Output SPI

In quad input/quad output SPI mode, 4-bit bidirectional data lines are used. Figure 4-33 shows the timing in quad input/quad output SPI mode.

Figure 4-33 Timing of the quad input/quad output SPI interface



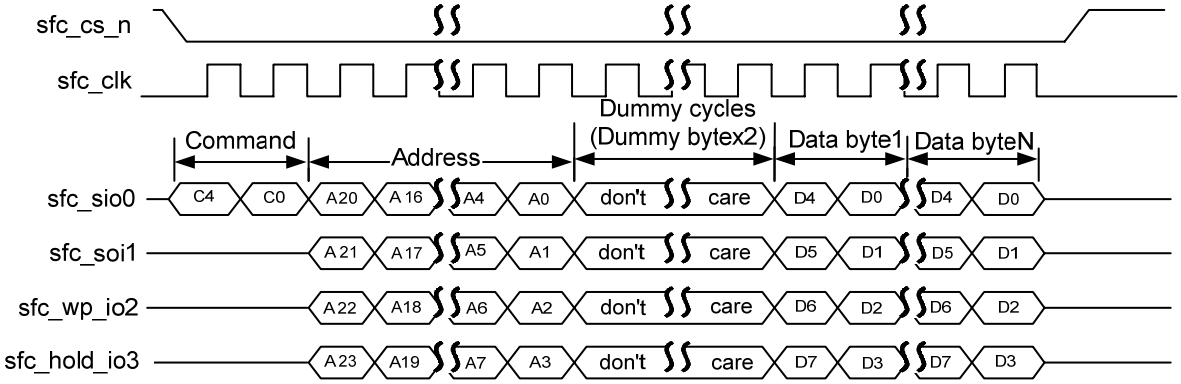
NOTE

- The opcode bytes, address bytes, and dummy bytes are output in unit of a single bit in serial mode through the sfc_sio0 line.
- The data bytes are output (write) and input (read) in unit of quad bits through the sfc_sio0, sfc_soi1, sfc_wp, or sfc_hold line.

Quad I/O SPI

In quad I/O SPI interface mode, 4-bit bidirectional data lines are used. Figure 4-34 shows the timing in quad I/O SPI interface mode.

Figure 4-34 Timing of the quad I/O SPI interface



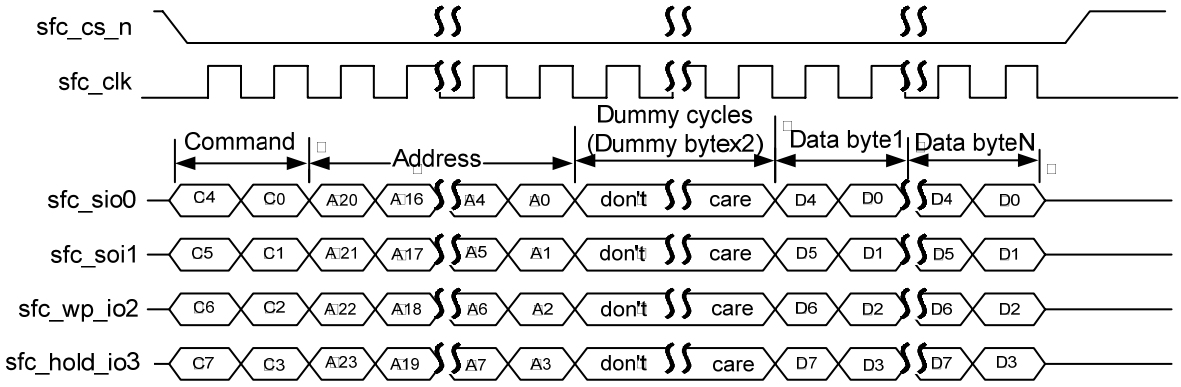
NOTE

- The opcode bytes are output in unit of a single bit in serial mode through the sfc_sio0 line. The address bytes and dummy bytes are output in unit of quad bits through the sfc_sio0, sfc_soi1, or sfc_wp, or sfc_hold line.
- The data bytes are output (write) or input (read) in unit of quad bits through the sfc_sio0, sfc_soi1, sfc_wp, or sfc_hold line.

Full Quad SPI

In full quad SPI interface mode, 4-bit bidirectional data lines are supported. Figure 4-35 shows the timing in full quad SPI interface mode.

Figure 4-35 Timing of the full quad SPI interface



NOTE

- The opcode bytes, address bytes, and dummy bytes are output in unit of quad bits through the sfc_sio0, sfc_soi1, sfc_wp, or sfc_hold line.
- The data bytes are output (write) and input (read) in unit of quad bits through the sfc_sio0, sfc_soi1, sfc_wp, or sfc_hold line.

4.2.3.2 Reading or Writing to the SPI Flash

The SPI flash can be read and written in the following ways:

- Send commands such as **SPI Flash Program** and **Read** based on register configurations to write to and read the SPI flash.

  This method requires the CPU to directly control the SPI flash commands and parameters to be sent.
- The CPU reads and writes to the SPI flash over the AHB slave interface in a similar way as the CPU reads and writes to a common memory.

  The SFC automatically maps the AHB bus read/write timing to an SPI flash read/write command.
- Data is transferred between the SPI flash and the memory in DMA mode.

4.2.3.3 Other Operations

Other operations on the SPI flash such as erase and device ID read can be implemented only by using registers.

4.2.3.4 Switching the Flash Address Mode

The SFC module supports 3-byte and 4-byte flash address modes. You can set the default address mode by pulling up or down the SFC_ADDR_MODE, and dynamically switch the address mode by configuring registers after the chip boots.
To set the default address mode when the chip boots, do as follows:

- Pull down the SFC_ADDR_MODE pin (multiplexed with the SFC_CLK pin) to set the default address mode to 3-byte address mode.
- Pull up the SFC_ADDR_MODE pin (multiplexed with the SFC_CLK pin) to set the default address mode to 4-byte address mode.

To switch the SPI flash address mode, perform the following steps:

1. Before switching between flash address modes, ensure that the operations on the SPI flash are complete.
2. Send specific commands to configure the SPI flash to enter the 4-byte mode by using registers based on SPI flash requirements.
3. Set the SFC flash address mode to 4-byte (GLOBAL_CONFIG[flash_addr_mode]).

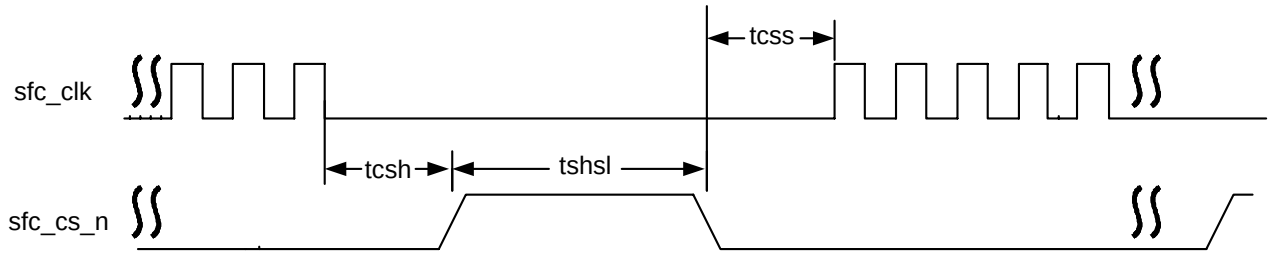
----End

For details about the commands for switching between SPI flash address modes, see the SPI flash manual.

4.2.3.5 Timing Description

Figure 4-36 describes timings and related parameters.

Figure 4-36 SPI output timing



NOTE

- tcsh: CS setup time
- tcss: CS hold time
- tshsl: CS deselect time

4.2.4 Working Process

4.2.4.1 Initialization

The initialization is implemented as follows:

1. Configure the timing register if the timing parameter needs to be configured.
2. For details about the flash 4-bye address mode, see section 4.3.3.4 "Switching the Flash Address Mode."
3. Configure the bus operation direction register.
   1. Configure BUS_FLASH_SIZE based on the size of the flash memory. You can obtain the size by sending the **Read ID** command to the flash memory to get the device models.
   2. Configure BUS_BASE_ADDR and BUS_ALIAS_ADDR based on the situation the flash memory is mapped to the system address space. The mapping address space must be within the address space that the system bus allocates to SFC_MEM.
   3. For some devices, the Hi3716M needs to send special instructions before reading and writing devices (flash memory) in non standard SPI timing mode.
   4. Configure the instructions and parameters of the bus read and write operations.

      Configure BUS_CONFIG1 or BUS_CONFIG2.
   5. Enable the bus write function if necessary. The bus write function is disabled by default.

      Configure BUS_CONFIG1[wr_enable] as 1.

NOTE

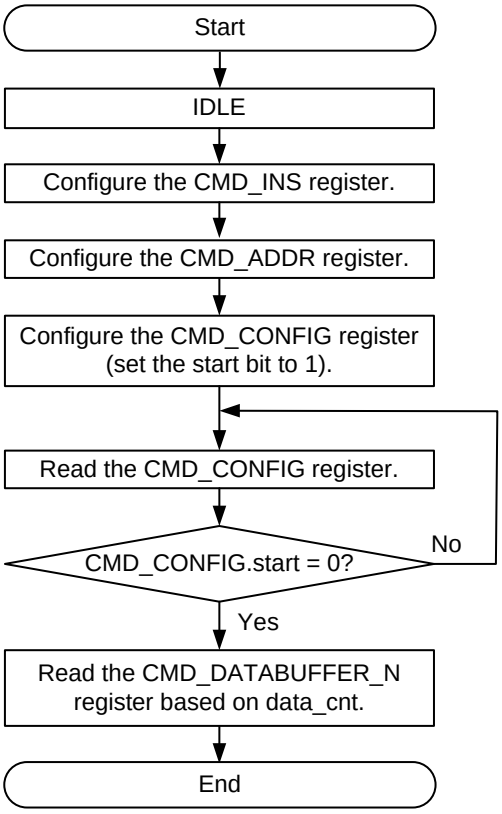
- The SPI flash does not need to be initialized for operations on the SPI flash by using registers. Registers must be reconfigured before each operation.
- This initialization process is only for reference. You are advised to adjust the initialization process based on device difference.

----End

4.2.4.2 Process of Reading the Flash Memory

Figure 4-37 shows the process of reading the flash memory by using related registers in query mode.

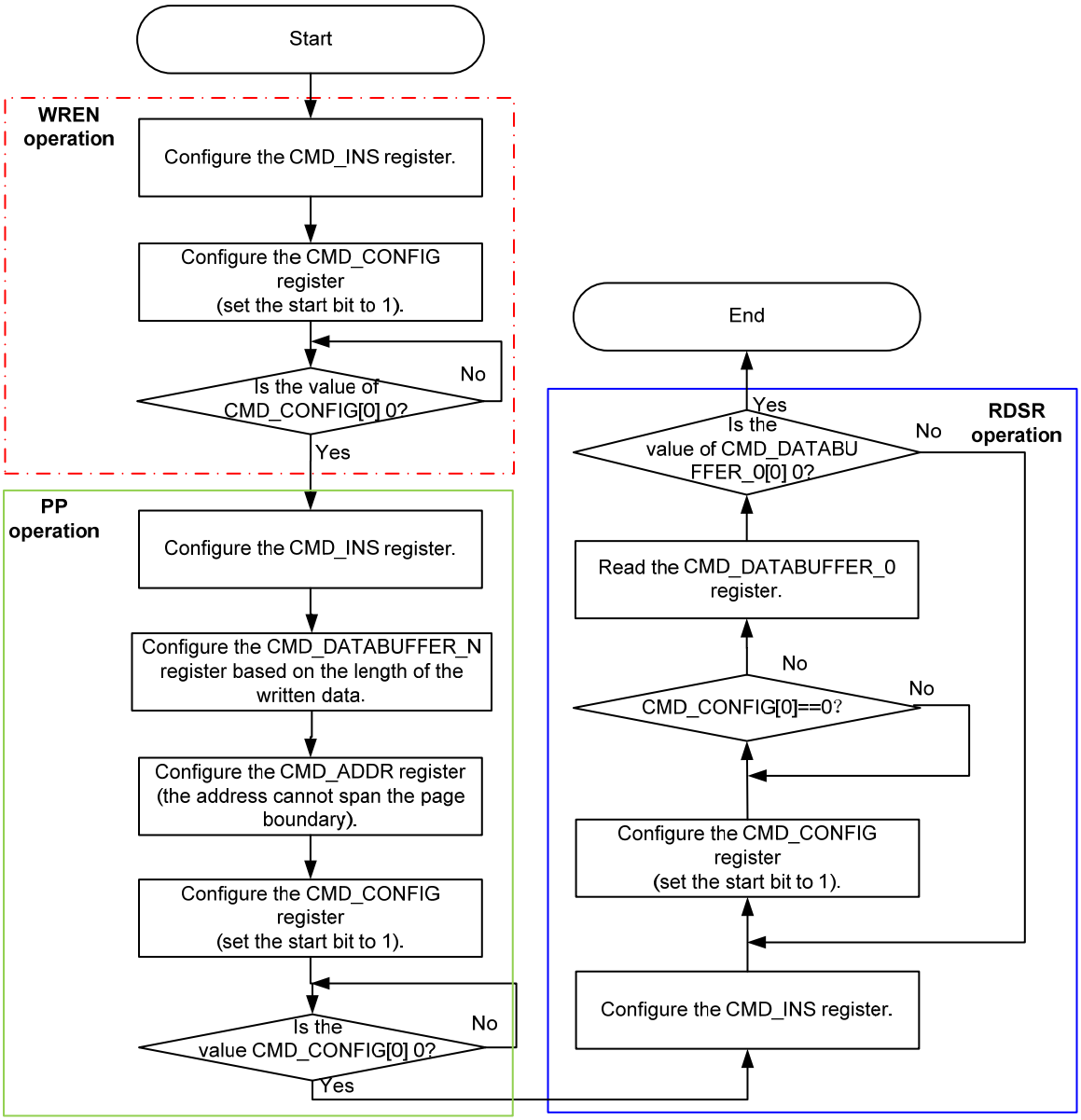
Figure 4-37 Process of reading the flash memory by using related registers in query mode



4.2.4.3 Process of Writing to the Flash Memory

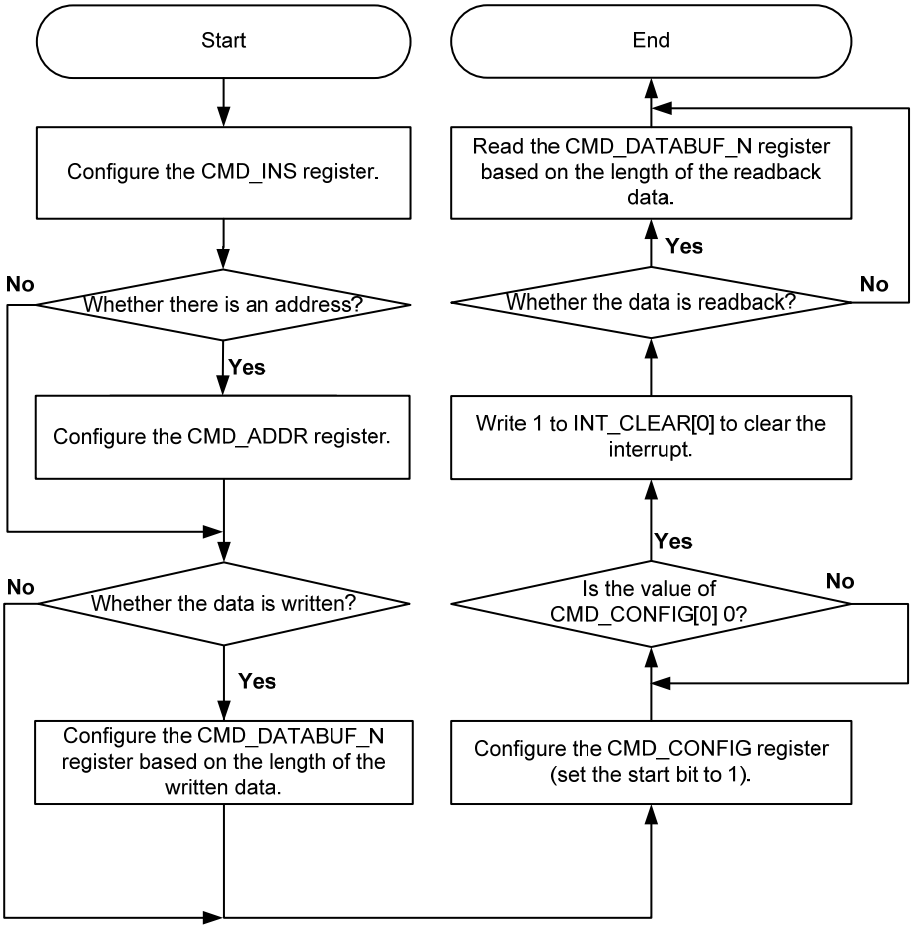
Figure 4-38 shows the process of writing to the flash memory by using related registers in interrupt mode.

Figure 4-38 Process of writing to the flash memory by using related registers in interrupt mode



4.2.4.4 Other Operations in Register Mode

Figure 4-39 Process of other operations



4.2.4.5 Process of Reading and Writing the Flash Memory Directly over the AHB Bus

After the SFC module is power-on reset, it is set to standard SPI timing mode by default. The flash memory can be directly read and written without additional configurations.

By default, writing to the flash memory over the AHB bus is forbidden. To enable the bus write operation, set BUS_CONFIG1[wr_enable] to 1.

For details about the read and write configuration of the bus, see section 4.3.4.1 "Initialization."

4.2.4.6 Process of Reading and Writing the Flash Memory in DMA Mode

The process of reading and writing the flash memory in DMA mode is as follows:

1. If you need to adjust the timing configurations of the bus operation mode, see section 4.3.4.1 "Initialization."

2. Configure the memory start address, flash memory start address (flash memory offset address), and data length.
3. Configure the read and write directions.
4. Enabled the DMA operation (set BUS_DMA_CTRL [start] to 1).
5. Wait for the dma_done interrupt or poll BUS_DMA_CTRL [start] until it is changed to 0.

NOTE

- The DMA operation and flash memory register command operation can be performed simultaneously.
- The flash memory can be directly accessed over the AHB slave interface during the DMA operation, but the configurations related to bus operation cannot be changed.

----End

4.2.5 Register Summary

Table 4-14 describes the SFC registers.

Table 4-14 Summary of SFC registers (base address: 0x1001_0000)

Offset Address	Register	Description	Page
0x0100	GLOBAL_CONFIG	Global configuration register	4-101
0x0110	TIMING	Timing configuration register	4-102
0x0120	INT_RAW_STATUS	Interrupt raw status register	4-102
0x0124	INT_STATUS	Masked interrupt status register	4-103
0x0128	INT_MASK	Interrupt mask register	4-104
0x012C	INT_CLEAR	Interrupt clear register	4-104
0x01F8	VERSION	Version register	4-105
0x01FC	VERSION_SEL	Version selection register	4-105
0x0200	BUS_CONFIG1	Bus operation configuration register 1	4-106
0x0204	BUS_CONFIG2	Bus configuration register 2	4-108
0x0210	BUS_FLASH_SIZE	Bus operation mapping size register	4-108
0x0218	BUS_BASE_ADDR	Bus mapping base address register	4-109
0x021C	BUS_ALIAS_ADDR	Bus mapping alias mapping base address register	4-109
0x0240	BUS_DMA_CTRL	DMA operation control register	4-110
0x0244	BUS_DMA_MEM_SADDR	DMA DDR start address register	4-110
0x0248	BUS_DMA_FLASH_SADDR	DMA operation Flash start address register	4-111

0x024C	BUS_DMA_LEN	DMA operation transfer data length register	4-111
0x0250	BUS_DMA_AHB_CTRL	DMA operation AHB burst control register	4-111
0x0300	CMD_CONFIG	Command operation configuration register	4-112
0x0308	CMD_INS	Command operation instruction register	4-113
0x030C	CMD_ADDR	Command operation address register	4-114
0x0400 + 4xN	CMD_DATABUF_N	Command operation data buffer register N (N = 0−15)	4-114

4.2.6 Register Description

GLOBAL_CONFIG

GLOBAL_CONFIG is a global configuration register.

Offset Address	Register Name	Total Reset Value
0x0100	GLOBAL_CONFIG	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	reserved							reserved	flash_addr_mode	wp_en	mode
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved.
[4:3]	RW	reserved	Reserved. This bit must be set to 0.
[2]	RW	flash_addr_mode	SPI address mode 0: 3-byte address mode (default) 1: 4-byte address mode The write operation is invalid when CMD.start is 1.
[1]	RW	wp_en	Enable hardware write protection. The WP pin is forcibly pulled down when the bit is set to 1. 0: disabled 1: enabled

[0]	RW	mode	SPI mode configuration 0: mode 0 1: mode 3

TIMING

TIMNG is a timing configuration register.

Offset Address	Register Name	Total Reset Value
0x0110	TIMING	0x0000_660F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																	tcsh			reserved	tcss			reserved				tshsl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved.
[14:12]	RW	tcsh	Set the CS hold time 000–111: n + 1 clock cycles (n = 0, 1, 2, …, or 7)
[11]	RW	reserved	Reserved.
[10:8]	RW	tcss	Set the setup time of the CS. 000–111: n + 1 clock cycles (n = 0, 1, 2, …, or 7)
[7:4]	RO	reserved	Reserved
[3:0]	RW	tshsl	Indicates the deselect time of the CS. It is equal to the interval between two flash operations. 0000–1111: n + 2 clock cycles. (n = 0, 1, 2, …, or 15)

INT_RAW_STATUS

INT_RAW_STATUS is an interrupt raw status register.

Offset Address	Register Name	Total Reset Value
0x0120	INT_RAW_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														dma_done_int_raw_status	cmd_op_end_raw_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1]	RO	dma_done_int_raw_status	Raw status of DMA operation done interrupt (not masked) 0: The operation is not complete. 1: The operation is complete.
[0]	RO	cmd_op_end_raw_status	Raw interrupt status of instruction operation end (not masked). 0: The operation is not complete. 1: The operation is complete.

INT_STATUS

INT_STATUS is a masked interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0124	INT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														dma_done_int_status	cmd_op_end_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.

[1]	RO	dma_done_int_status	Raw status of DMA operation done interrupt (masked) 0: The operation is not complete. 1: The operation is complete.
[0]	RO	cmd_op_end_status	Interrupt status of instruction operation end (masked) 0: The operation is not complete. 1: The operation is complete.

INT_MASK

INT_MASK is an interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x0128	INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														dma_done_int_mask	cmd_op_end_int_mask
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1]	RW	dma_done_int_mask	DMA operation done interrupt mask bit 0: masked 1: not masked
[0]	RW	cmd_op_end_int_mask	Instruction operation end interrupt mask bit 0: masked 1: not masked

INT_CLEAR

INT_CLEAR is an interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x012C	INT_CLEAR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														dma_done_int_clr	cmd_op_end_int_clr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1]	WO	dma_done_int_clr	DMA done interrupt clear bit. Writing 1 to this bit clears dma_done_status and dma_done_raw_status. 0: not cleared 1: cleared After a clear operation is complete, this bit returns 0 automatically.
[0]	WO	cmd_op_end_int_clr	Instruction operation end interrupt clear bit. Writing 1 to this bit clears cmd_op_end_status and cmd_op_end_raw_status. 0: not cleared 1: cleared After a clear operation is complete, this bit returns 0 automatically.

VERSION

VERSION is a version register.

Offset Address	Register Name	Total Reset Value
0x01F8	VERSION	0x0000_0350

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VERSION																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	1	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	VERSION	SFC version number

VERSION_SEL

VERSION_SEL is a version selection register.

Offset Address	Register Name	Total Reset Value
0x01FC	VERSION_SEL	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															version_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RO	version_sel	New and earlier version register group indication signal 0: earlier version register group 1: new version register group

BUS_CONFIG1

BUS_CONFIG1 is the bus operation configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0200	BUS_CONFIG1	0x8080_0300

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rd_enable	wr_enable	wr_ins								wr_dummy_bytes		wr_mem_if_type				rd_ins								rd_prefetch_cnt				rd_dummy_bytes			rd_mem_if_type
Reset	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	rd_enable	Bus read control. The value 0 is returned when the bus reads data. 0: disabled 1: enabled
[30]	RW	wr_enable	Bus write control. Ignore the bus write operation. 0: disabled 1: enabled
[29:22]	RW	wr_ins	Write instruction

[21:19]	RW	wr_dummy_bytes	Dummy byte of the bus write operation 0: no dummy byte 1: 1 byte 2: 2 bytes ... 7: 7 bytes
[18:16]	RW	wr_mem_if_type	Bus write operation specifies the type of the connected SPI flash interface. 000: standard SPI interface type 001: dual-Input/dual-Output SPI 010: dual-I/O SPI 011: full DIO SPI 100: reserved 101: quad-Input/Dual-Output SPI 110: quad-I/O SPI 111: full QIO SPI
[15:8]	RW	rd_ins	Read instruction
[7:6]	RW	rd_prefetch_cnt	Clock cycle for prefetching data when the flash memory is accessed at a variable data length through the bus. 00: not prefetched (default) 01: prefetch the data in one clock cycle 10: prefetch the data in two clock cycles 11: prefetch the data in three clock cycles
[5:3]	RW	rd_dummy_bytes	Dummy byte of the bus read operation 0: no dummy byte 1: 1 byte 2: 2 bytes ... 7: 7 bytes
[2:0]	RW	rd_mem_if_type	Bus read operation specifies the type of the connected SPI flash interface. 000: standard SPI interface type 001: dual-Input/Dual-Output SPI 010: dual-I/O SPI 011: full DIO SPI 100: reserved 101: quad-Input/Dual-Output SPI 110: quad-I/O SPI 111: full QIO SPI

BUS_CONFIG2

BUS_CONFIG2 is the bus configuration register 2.

Offset Address	Register Name	Total Reset Value
0x0204	BUS_CONFIG2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2:0]	RW	reserved	Reserved. The value 0 must be written to this bit.

BUS_FLASH_SIZE

BUS_FLASH_SIZE is a bus mapping size register.

Offset Address	Register Name	Total Reset Value
0x0210	BUS_FLASH_SIZE	0x0000_0909

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				flash_size_cs1				reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:8]	RW	flash_size_cs1	Capacity of the SPI flash connected to CS 1. 0000: 0000: No SPI flash is connected. 0001: 512 kbits 0010: 1 Mbit 0011: 2 Mbits 0100: 4 Mbits 0101: 8 Mbits 0110: 16 Mbits 0111: 32 Mbits 1000: 64 Mbits 1001: 128 Mbits (default) 1010: 256 Mbits

			1011: 512 Mbits 1100: 1 Gbit 1101: 2 Gbits 1110: 4 Gbits 1111: 8 Gbits
[7:0]	RW	reserved	Reserved

BUS_BASE_ADDR

Bus mapping base address register is a bus mapping base address register.

Offset Address	Register Name	Total Reset Value
0x0218	BUS_BASE_ADDR	0x5800_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bus_base_addr_high																reserved															
Reset	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	bus_base_addr_high	The flash memory is mapped to the system space address.
[15:0]	RO	reserved	Reserved.

BUS_ALIAS_ADDR

BUS_ALIAS_ADDR is a bus alias base address register.

Offset Address	Register Name	Total Reset Value
0x021C	BUS_ALIAS_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flash_alias_addr																reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	flash_alias_addr	The flash memory is mapped to the second base address of the system space.
[15:0]	RO	reserved	Reserved.

BUS_DMA_CTRL

BUS_DMA_CTRL is a DMA control register.

Offset Address	Register Name	Total Reset Value
0x0240	BUS_DMA_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														rw	start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved.
[4]	RW	reserved	Reserved. The value 1 is always written to this bit.
[3:2]	RO	reserved	Reserved.
[1]	RW	rw	DMA read and write indication. 0: write operation (write data to the flash memory) 1: read operation (read data from the flash memory)
[0]	RW	start	DMA transfer enable control 0: no operation or the operation is complete. 1: Writing 1 to this bit to enable the DMA operation. Read 1 from this bit indicates the DMA is operating. The value 0 is automatically returned after the DMA operation is complete.

BUS_DMA_MEM_SADDR

BUS_DMA_MEM_SADDR is DMA DDR start address register.

Offset Address	Register Name	Total Reset Value
0x0244	BUS_DMA_MEM_SADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_mem_saddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dma_mem_saddr	DMA DDR start address. The start address must be 4-byte aligned.

BUS_DMA_FLASH_SADDR

BUS_DMA_MEM_SADDR is a DMA flash start address register.

Offset Address	Register Name	Total Reset Value
0x0248	BUS_DMA_FLASH_SADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_flash_saddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dma_flash_saddr	DMA flash start address.

BUS_DMA_LEN

BUS_DMA_LEN is a DMA transfer data length register.

Offset Address	Register Name	Total Reset Value
0x024C	BUS_DMA_LEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		dma_len																													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RW	reserved	Reserved.
[29:0]	RW	dma_len	DMA data transfer length.

BUS_DMA_AHB_CTRL

BUS_DMA_AHB_CTRL is a DMA AHB burst control register.

Offset Address	Register Name	Total Reset Value
0x0250	BUS_DMA_AHB_CTRL	0x0000_0007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													incr16_en	incr8_en	incr4_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Access	Name	Description
[31:3]	RW	reserved	Reserved.
[2]	RW	incr16_en	INC16 burst type enable. 0: disabled 1: enabled
[1]	RW	incr8_en	INC8 burst type enable. 0: disabled. 1: enabled
[0]	RW	incr4_en	INC4 burst type enable. 0: disabled. 1: enabled

CMD_CONFIG

CMD_CONFIG is a command configuration register.

Offset Address	Register Name	Total Reset Value
0x0300	CMD_CONFIG	0x0000_7E00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												mem_if_type			reserved	data_cnt							rw	data_en	dummy_byte_cnt			addr_en	reserved		start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved.

[19:17]	RW	mem_if_type	Specifies the type of the SPI flash interface in register command operation mode. 000: standard SPI interface type 001: dual-Input/Dual-Output SPI 010: dual-I/O SPI 011: full DIO SPI 100: reserved 101: quad-Input/Dual-Output SPI 110: quad-I/O SPI 111: full QIO SPI
[16:15]	RW	reserved	Reserved. The value 0 must be written to this bit.
[14:9]	RW	data_cnt	The length of the read and written data is N+1 bytes.
[8]	RW	rw	Indicates that the data is read or written when that data_en is 1. 0: write. Data is written to the flash memory. 1: read. Data is read from the flash memory.
[7]	RW	data_en	Indicates whether there is data in this operation. 0: no data 1: there is data.
[6:4]	RW	dummy_byte_cnt	Dummy byte in register command operation mode. 0: no dummy byte 1: 1 byte 2: 2 bytes ... 7: 7 bytes
[3]	RW	addr_en	Indicates whether there is an address for the current operation. 0: 0: There is no address 1: There is an address.
[2]	RO	reserved	Reserved.
[1]	RW	reserved	The value 1 is always written to this bit.
[0]	RW	start	Instruction operation start. 0: The operation is complete. 1: The operation starts. After the operation is complete, the bit returns 0 automatically.

CMD_INS

CMD_INS is a command instruction register.

Offset Address	Register Name	Total Reset Value
0x0308	CMD_INS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								REG_INS							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:0]	RW	REG_INS	Instruction code in the mode that the register accesses the flash memory.

CMD_ADDR

CMD_ADDR is a command address register.

Offset Address	Register Name	Total Reset Value
0x030C	CMD_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								cmd_addr							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:0]	RW	cmd_addr	Operation address in the mode that the register accesses the flash memory.

CMD_DATABUF_N

CMD_DATABUF_N is a command data buffer register.

Offset Address	Register Name	Total Reset Value
0x0400 + 4xN (N = 0−15)	CMD_DATABUF_N	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cmd_databuf_n																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cmd_databuf_n	Data buffer N in the mode that the register accesses the flash memory. Register offset address 0x400+4Xn. The variable *N* can be set to 0 to 15.

4.3 NAND Flash Controller

4.3.1 Overview

The NAND flash controller (NANDC) provides memory controller interfaces. These interfaces enable the Hi3518 to connect to external NAND flash memories to access data.

4.3.2 Features

The NANDC has the following features:

- Provides 2 KB (2048 + 320 bytes) on-chip buffer for improving the read speed.
- Supports two CSs and two ready/busy signals and allows two NAND flash memories to share one ready/busy signal.
- Supports NAND flash interfaces with 8-bit data bus.
- Allows the chip to boot from the NAND flash corresponding to CS 0 and supports the NAND flash memory with the page size of 2 KB, 4 KB, or 8 KB.
- Enables or disables error correcting code (ECC) check and error correction. 1-bit/512 bytes, 4-bit/512 bytes, and 24-bit/1024 bytes ECC check and error correction are supported.
- Reports read/write interrupts, erase interrupts, programming complete interrupts, and ECC check error interrupts.
- Reads/writes data with variable lengths.
- Flexibly configures the commands issued by the controller to support various NAND flash command operations including cache read and write.
- Supports interruption in the process of reading and writing the NAND flash to release the shared bus.
- Operates two NAND flash memories in an alternate manner to improve efficiency.
- Supports write protection for the NAND flash and configurable write-protection addresses.

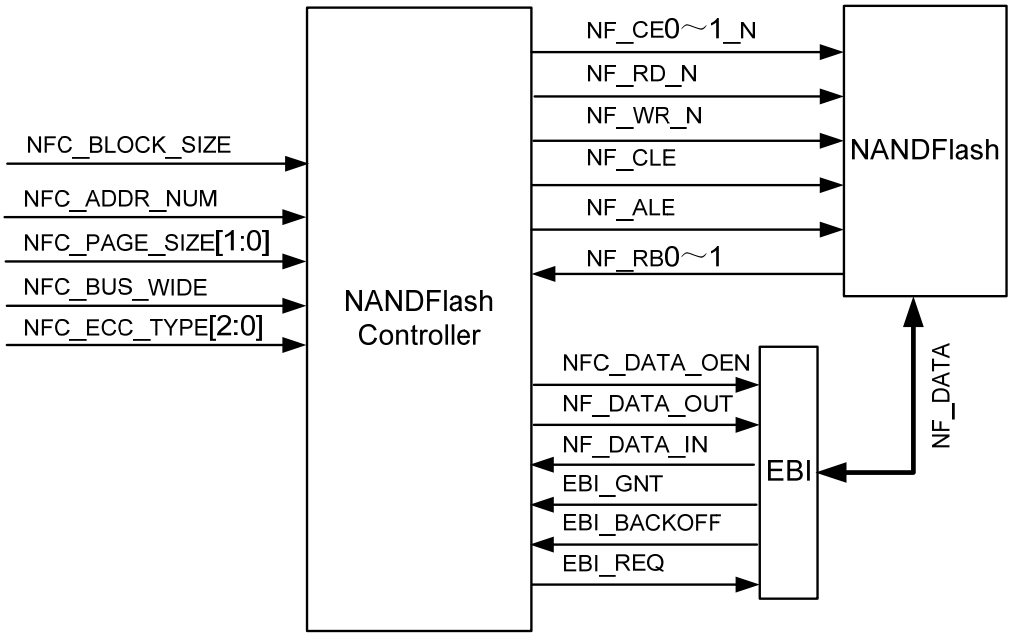
- Supports the lock and lock-down modes and the enabling and disabling of flash lock and flash global lock. By default, flash lock and flash global lock are enabled. The NANDC always reports operation error interrupts if the locked addresses are written.
- Reads NAND flash data in enhanced data out (EDO) mode.

4.3.3 Function Description

4.3.3.1 Block Diagram of NANDC Interfaces

The chip provides two CS signals and two ready/busy signals, so it can connect to NAND flash memories conveniently. If only one ready/busy signal is used, NF_RB0 is required. Figure 4-34 shows the block diagram of NANDC interfaces.

Figure 4-34 Block diagram of NANDC interfaces



4.3.3.2 Function Principle

The data is generally stored in the NAND flash by blocks and pages. Each block consists of several pages. Before writing data to the NAND flash, you must erase it by blocks. Then, you can read/write the NAND flash by pages.

The commands for operating the NAND flash vary according to vendors. That is, the specific commands are subject to component manuals.

A typical read operation is performed as follows:

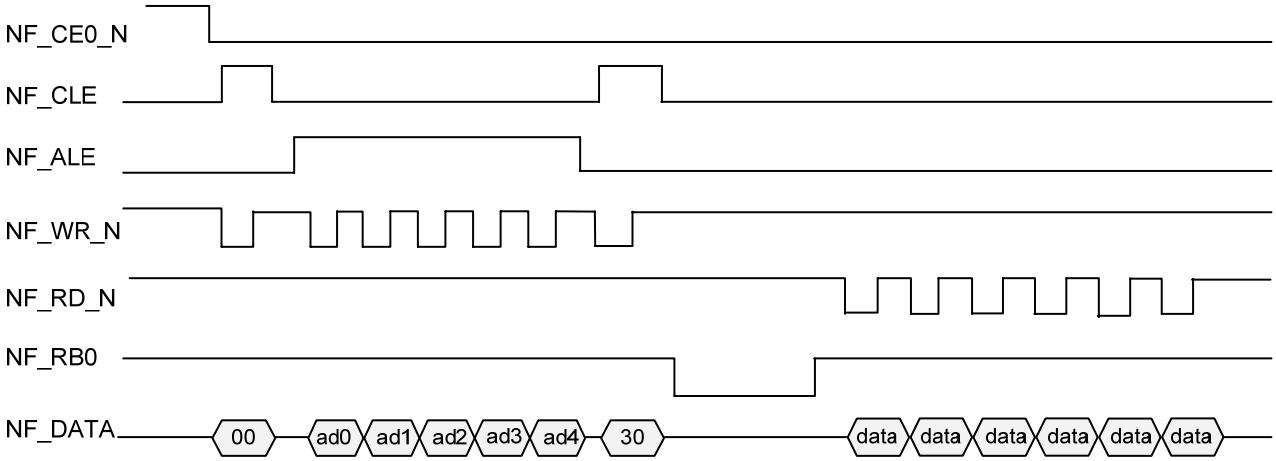
1. Transmit the read command 0x00 to the NAND flash.
2. Transmit the read start address. The start address consists of the internal page address, page address, and block address. For details, see the NAND flash manuals provided by relevant vendors.

3. Transmit the read acknowledgement command 0x30. The NAND flash pulls the RB signal low. This indicates that the NAND flash is being read. About 25 μs later, the RB signal becomes high. This indicates that data of the NAND flash is ready.
4. The CPU reads data from the NAND flash through the NF_RD_N signal.

----End

Figure 4-35 shows the typical timing when the NANDC reads the data of a page size from the NAND flash.

Figure 4-35 Typical timing when the NANDC reads the data of a page size from the NAND flash



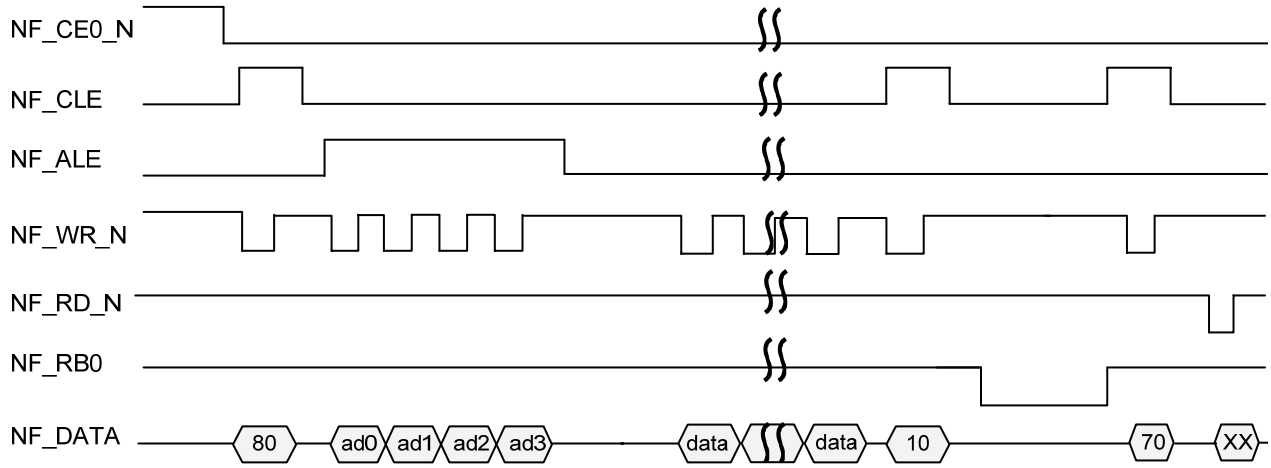
A typical programming operation (writing data) is performed as follows:

1. Transmit the programming command 0x80 to the NAND flash.
2. Transmit the start address from which data is written. The start address consists of the internal page address, page address, and block address. For details, see the NAND flash manuals provided by relevant vendors.
3. Write data to the internal buffer of the NAND flash.
4. The CPU sends the programming acknowledgement command 0x10. In this case, the NAND flash pulls the RB signal low. This indicates that the NAND flash is being programmed. About 200 ms later, the RB signal becomes high. This indicates that the programming operation is complete.
5. The CPU transmits the read status command 0x70 to read the status data that indicates whether the programming operation is successful.

----End

Figure 4-36 shows the timing when NANDC starts programming.

Figure 4-36 Timing when the NANDC starts programming



4.3.3.3 Operating Mode

Mapping Mode of the NAND Flash

When the Hi3518 boots, you need to select the NAND flash type by setting the pull-up or pull-down modes of the pins NF_BOOT_PIN0 (multiplexed with the NF_REN pin), NF_BOOT_PIN1 (multiplexed with the NF_CLE pin), NF_BOOT_PIN2 (multiplexed with the NF_ALE pin), NF_BOOT_PIN3 (multiplexed with the NF_WEN pin), and NF_BOOT_PIN4 (multiplexed with the SPI0_CSN pin). Note that you must set the pull-up or pull-down modes of pins properly no matter whether the system boots from the NAND flash. Otherwise, the system fails to boot.

Table 4-9 describes the mapping modes of pins.

Table 4-8 Mapping modes of pins

{NF_BOOT_PIN4, NF_BOOT_PIN3, NF_BOOT_PIN2, NF_BOOT_PIN1, NF_BOOT_PIN0}	Page Size	ecc_type	block_size	addr_num	bus_wide	Remarks
00000	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
00001	01	001	0	1	0	2 KB page size 1-bit ECC 64 pages/block 5 addresses
00010	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
00011	01	010	0	1	0	2 KB pages size 4-bit ECC 64 pages/block 5 addresses
00100	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

00101	01	100	0	1	0	2 KB pages size 24-bit ECC 64 pages/blocks 5 addresses
00110	01	001	0	0	0	2 KB pages size 1-bit ECC 64 pages/blocks 4 addresses
00111	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
01000	10	010	1	1	0	4 KB pages size 4-bit ECC 128 pages/blocks 4 addresses
01001	10	010	0	1	0	4 KB pages size 4-bit ECC 64 pages/blocks 4 addresses
01010	01	010	0	0	0	2 KB pages size 4-bit ECC 64 pages/blocks 4 addresses
01011	10	100	1	1	0	4 KB pages size 24-bit ECC 128 pages/blocks 4 addresses
01100	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
01101	11	100	1	1	0	8 KB pages size 24-bit ECC 128 pages/blocks 4 addresses
01110	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
01111	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
10000	11	100	0	1	0	8 KB pages size 24-bit ECC 64 pages/blocks

						4 addresses
10001	10	100	0	1	0	4 KB pages size 24-bit ECC 64 pages/blocks 4 addresses
10010	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
10011	10	001	0	1	0	4 KB pages size 1-bit ECC 64 pages/blocks 4 addresses
10100	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
10101	01	010	1	1	0	2 KB pages size 4-bit ECC 128 pages/blocks 4 addresses
10110	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
10111	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
11000	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
11001	01	100	1	1	0	2 KB pages size 24-bit ECC 128 pages/blocks 4 addresses
11010	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
11011	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
11100	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
11101	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
11110	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
11111	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Clock Gating

When the NAND flash is not used, you can disable the working clock of the NANDC. To disable the clock, perform the following steps:

1. Read NFC_STATUS[nfc_ready] of the NANDC.

2. If NFC_STATUS[nfc_ready] is 1 and the NAND flash is not read and written by the software, go to step 3; otherwise, go to step 1.
3. Write 0 to PERI_CRG52[nfc_cken] to disable the clock.

----End

Soft Reset

After the NANDC is enabled by writing data to NFC_OP, if NFC_STATUS[nfc_ready] is changed to 0 and cannot be changed to 1 for a long period, the NANDC is abnormal and a soft reset operation is required. The maximum duration depends on the NAND flash. For the SLC flash, it is less than 4 ms; for the MLC, it is less than 11 ms.

The NANDC can be soft-reset by writing 1 to PERI_CRG52[nfc_srst_req]. After reset, each configuration register is restored to its default value. Therefore, these registers must be reinitialized. In addition, a reset command must be sent to the NAND flash after soft reset (if the NAND flash supports reset) to ensure its reliability.

NOTE

The NANDC supports the lock function. If this function is enabled, it can be disabled until a hard reset is performed.

Boot Configuration Pins

The NANDC supports the NAND boot function and the memory with the page size of 2 KB, 4KB, or 8 KB. The NANDC can boot from the NAND flash corresponding only to CS 0.

After reset, the boot mode of the NANDC depends on the levels of the NANDC boot configuration pins. When the NANDC is reset, the levels of the boot configuration pins are sampled. After sampling, the operating status of the NANDC is not affected by the levels. Table 4-9 shows the boot configuration pins.

Table 4-9 Boot configuration pins

Register	I/O	Description
NFC_ADDR_NUM	I	Number of addresses sent to the NAND flash by the NANDC during booting. 0: 4 address cycles 1: 5 address cycles.
NFC_PAGE_SIZE	I	Page size of the NAND flash during booting. 01: 2 KB 10: 4 KB 11: 8 KB Other values: reserved
NFC_BUS_WIDE	I	Bus width of the NAND flash during booting. 0: 8 bits 1: 16 bits
NFC_ECC_TYPE[2:0]	I	ECC mode during booting.

		000: disabled 001: 1-bit mode 010: 4-bit mode 100: 24-bit mode Other values: reserved
NFC_BLOCK_SIZE	I	Block size of the NAND flash during booting. 0: 64 pages 1: 128 pages

Boot Mode

By default, the NANDC is in boot mode and the NANDC can be booted only from CS 0 corresponding to the NAND flash.

In boot mode:

- Data stored in the 1 MB address can be read by the CPU.
- Bad blocks can be automatically detected and skipped.
- When the NANDC boots from the NAND flash, the NANDC automatically sends a command to read the corresponding page of the NAND flash based on the addresses read by the CPU and then returns the corresponding data.
- Data cannot be written to the internal buffer through the CPU.
- The boot configuration pins must be configured properly according to the models of the connected NAND flash.

Normal Mode

The NANDC is switched to the normal mode when NFC_CON [op_mode] is set to 1. In this mode, the CPU can erase, program, and read the NAND flash. The NANDC is switched to the quick ECC error correction clock when PERI_CRG52[nfc_clk_sel] is set to 1.

Setting the Address of the NAND Flash

The NANDC does not translate addresses. According to the number of addresses configured by the command configuration register, the NANDC sends the values of lower-bit and upper-bit address registers to the NAND flash directly. Therefore, the software needs to translate the address of the CPU into the address of the NAND flash and write the translated address to the address register. For details about the address configuration requirements on each flash memory, see the user manuals of the corresponding NAND flash.

Table 4-10 describes the requirements on the addresses of Samsung K9F2G08U0M memory. Its capacity is 256 MB x 8 bits and its page size is 2 KB. A0 to A11 indicate the internal page addresses (column addresses) and A12 to A27 indicate the page addresses (row addresses).

Table 4-10 Addresses of the K9F2G08U0M

Cycle	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
First cycle	A0	A1	A2	A3	A4	A5	A6	A7

Second cycle	A8	A9	A10	A11	0	0	0	0
Third cycle	A12	A13	A14	A15	A16	A17	A18	A19
Fourth cycle	A20	A21	A22	A23	A24	A25	A26	A27

Table 4-11 describes the requirements on the addresses of Samsung K9GAG08X0M memory. Its capacity is 2 GB x 8 bits and its page size is 4 KB. A0 to A12 indicate the internal page addresses (column addresses) and A13 to A31 indicate the page addresses (row addresses).

Table 4-11 Addresses of the K9GAG08X0M

Cycle	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
First Cycle	A0	A1	A2	A3	A4	A5	A6	A7
Second Cycle	A8	A9	A10	A11	A12	0	0	0
Third cycle	A13	A14	A15	A16	A17	A18	A19	A20
Fourth cycle	A21	A22	A23	A24	A25	A26	A27	A28
Fifth cycle	A29	A30	A31	0	0	0	0	0

Address Mapping

In normal mode, the address mapping of the NANDC is as follows:

- The base address of the internal buffer of the NANDC is 0x5000_0000.
- The base address of the internal register area of the NANDC is 0x1000_0000.

Operation Commands

The NAND flash memories provide certain advanced commands. Table 4-12 shows the common commands for operating NAND flash memories.

Table 4-12 Common commands for operating the NAND flash

Description	First Cycle	Second Cycle	Remarks
Read	00H	30H	None
Programming	80H	10H	None
Block erase	60H	D0H	None

Read ID	90H	None	None
Read status	70H	None	None
Reset	FFH	None	None

4.3.4 Data Storage Structure

The size of the internal buffer of the NANDC is (2048 + 320) bytes. This section describes the storage structures of the data in the NANDC buffer. The data is read from or written to the NAND flash.

4.3.4.1 1-Bit ECC Mode

2 KB (2048 + 64 Bytes) Page Size

2048-byte valid data is stored in the buffer ranging from 0x000 to 0x7FF; 64-byte spare data is stored in the buffer ranging from 0x800 to 0x83F.

The data structures of the driver, NANDC buffer, and NAND flash are the same, as shown in Figure 4-37.

Figure 4-37 Data storage structure of the NAND flash with the page size of 2 KB (2048 + 64 bytes) in 1-bit ECC mode

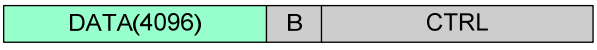
B: indicates bad block, 2 bytes
CTRL: indicates the control area for the software, 42 bytes

DECC: indicates the ECC code in the data area, 12 bytes
SECC: indicates the bad block flag and ECC code in the CTRL area, 8 bytes. (Starting from the bad block flag, each 16-byte data is used to calculate a 2-byte check code. During calculation, the position data of DECC and SECC is masked as 0.)

4 KB (4096 Bytes +56 Bytes) Page Size

Figure 4-38 shows the (4096 + 56)-byte data structure of the driver.

Figure 4-38 (4096 + 56)-byte data structure of the driver in 1-bit ECC mode

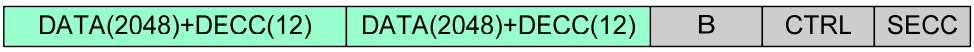


B: indicates bad block, 2 bytes

CTRL: indicates the control area for the software, 54 bytes

In the NAND flash, data is stored in (2048 + 12)-byte ECC code alternate mode (4096 + 24 bytes in total), as shown in Figure 4-39.

Figure 4-39 Data structure of the NAND flash in 1-bit ECC mode



B: indicates bad block, 2 bytes

CTRL: indicates the control area for

the software, 54 bytes

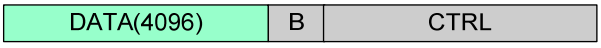
SECC: indicates the bad block flag and ECC code in the CTRL area, 8 bytes. (Starting from the bad block flag, each 16-byte data is used to calculate a 2-byte check code. During calculation, the position data of SECC is masked as 0.)

4.3.4.2 4-Bit ECC Mode

4 KB (4096 + 128 Bytes) Page Size

For the device with 4 KB page size, the available spare area for the software is 46 bytes. Figure 4-40 shows the (4096 + 128)-byte data structure of the driver.

Figure 4-40 (4096 + 48)-byte data structure of the driver in 4-bit ECC mode

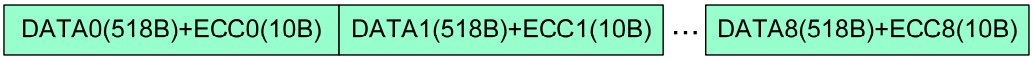


B: indicates bad block, 2 bytes

CTRL: indicates the control area for the software, 46 bytes

Figure 4-41 shows the structure of the data written to the NAND flash. The valid data of the software is divided into eight 518-byte data blocks. Each data block is used to calculate the ECC code once. The data written to the NAND flash is automatically stored in alternate mode of 518-byte data + 10-byte ECC code. In general, the data is stored in eight groups.

Figure 4-41 (4096 + 128)-byte data structure of the NAND flash in 4-bit ECC mode

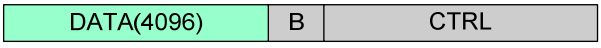


4.3.4.3 24-Bit ECC Mode

4 KB Page Size

Figure 4-42 shows the (4096 + 32)-byte data structure of the driver when the page size is 4 KB.

Figure 4-42 (4096 + 32)-byte data structure of the driver in 24-bit ECC mode

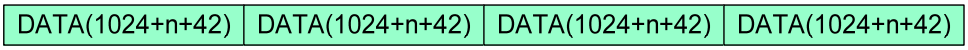


B: indicates bad block, 2 bytes

CTRL: indicates the control area for the software, 30 bytes (when *n* is set to 8)

When data is written to the NAND flash, the data is divided into four (1024 + n)-byte data blocks (*n* can be set to 4 or 8). Each data block is used to calculate a 42-byte ECC code. Then the data blocks and ECC code are stored alternately. The total size of the data and code is 4096 + 200 bytes, as shown in Figure 4-43.

Figure 4-43 (4096 + 200)-byte data structure of the NAND flash in 24-bit ECC mode (n = 8)



In boot mode, the value of *n* is 8 bytes by default.

8 KB Page Size

Figure 4-44 shows the (8192 + 32)-byte data structure of the driver when the page size is 8 KB.

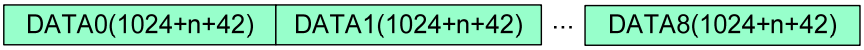
Figure 4-44 (8192 + 32)-byte data structure of the driver in 24-bit ECC mode

B: indicates bad block, 2 bytes

CTRL: indicates the control area for the software, 30 bytes (when *n* is set to 4)

When data is written to the NAND flash, the data is divided into eight (1024 + n)-byte data blocks (*n* is 4 or 8). Each data block is used to calculate a 42-byte ECC code. Then the data blocks and ECC code are stored alternately, as shown in Figure 4-45.

Figure 4-45 (8192 + 368)-byte data structure of the NAND flash in 24-bit ECC mode (n = 4)



In boot mode, the value of *n* is 8 bytes by default.

4.3.5 Software Operations

4.3.5.1 Initialization

To initialize the NAND Flash perform the following steps:

1. Write 1 to NFC_CON[op_mode] to enter the normal mode, set NFC_CON[bus_width] and NFC_CON[page_size] based on the page size and bit width of the interconnected component and set NFC_CON[rb_sel] based on the number of CSs and the number of ready_busy signals of the interconnected component, write NFC_CON[ecc_type] to set the check and error correction modes.
2. Write to NFC_PWIDTH based on the timing requirements of the connected component.
3. In query mode, write the interrupt enable register NFC_INTEN to mask all the interrupts; in interrupt mode, enable only the op_done interrupt and mask other interrupts.

----End

4.3.5.2 Erasing Data in the NAND Flash

To erase data in the NAND flash perform the following steps:

1. Write the programming page address to NFC_ADDRL and NFC_ADDRH and write the erase command 0x0070_D060 to NFC_CMD.
2. Write 0x369 to NFC_OP and enable the NANDC to erase the NAND flash. Assume that the NAND flash chip needs three addresses and the operation is performed on CS 0.
3. In query mode, check whether NFC_STATUS[nfc_ready] is 1. If the value is 1, go to step 4; otherwise, continue the query. In interrupt mode, check whether NFC_INTS[op_done] is 1. If the value is 1, go to step 4.
4. Read NFC_STATUS[nf_status] to check whether the erase operation is successful.

----End

4.3.5.3 Writing Data to the NAND Flash in DMA Mode

To write data to the NAND Flash in DMA mode, perform the following steps:

1. Set the parameters of NFC_CON such as page size, ecc_type, and bus_wide based on the type of the interconnected component. If the error correction type is 24-bit ECC check, configure NFC_OP_PARA[ext_len].
2. The CPU configures NFC_BADDR_D, and NFC_BADDR_OOB. The CPU also needs to configure NFC_DMA_LEN if it is in ECC0 mode.
3. The CPU writes to NFC_DMA_CTRL and enables the NANDC to write to the NAND flash.
4. The CPU waits until the NANDC transmits a DMA transfer done interrupt.

----End

4.3.5.4 Reading the NAND Flash in DMA Mode

To read data to the NAND Flash in DMA mode, perform the following steps:

1. Set the parameters of NFC_CON such as page size, ecc_type, and bus_wide based on the type of the interconnected component. If the error correction type is 24-bit ECC check, configure NFC_OP_PARA[ext_len].
2. The CPU configures NFC_BADDR_D, NFC_DMA_LEN, NFC_RD_LOGIC_ADDR, and NFC_RD_LOGIC_LEN.
3. The CPU writes to NFC_DMA_CTRL and enables the NANDC to read the NAND flash.
4. The CPU waits until the NANDC transmits a DMA transfer done interrupt.

----End

4.3.6 Precautions

Take the following precautions:

- The operation commands supported by the NAND flash memories vary according to vendors. Therefore, the command register NFC_CMD must be configured properly according to memory manuals. In addition, the number of address cycles required by the NAND flash memories of different capacities is different. You need to configure the address_cycles field of NFC_OP according to memory manuals. Furthermore, the timings supported by memories are different. Therefore, the read/write pulse width

register NFC_PWIDTH and operation interval register NFC_OPIDLE must be configured properly according to memory manuals.

- After configuring related registers and buffer, write to the NFC_OP register to enable the NANDC to read and write to the flash memory. After that, do not write to related registers; otherwise, the NANDC or flash memory may be abnormal.
- After enabling the NAND flash to be read and written by writing to NFC_OP, do not read and write the buffer of the NANDC when the flag NFC_STATUS[nfc_ready] is 0. Otherwise, error data may be returned.

4.3.7 Register Summary

Table 4-13 describes the NANDC registers.

Table 4-13 Summary of NANDC registers (base address; 0x1000_0000)

Offset Address	Register	Description	Page
0x00	NFC_CON	NANDC configuration register	4-129
0x04	NFC_PWIDTH	Read/write pulse width configuration register	4-131
0x08	NFC_OPIDLE	Operation interval configuration register	4-131
0x0C	NFC_CMD	Command word configuration register	4-132
0x10	NFC_ADDRL	Lower-bit address configuration register	4-132
0x14	NFC_ADDRH	Upper-bit address configuration register	4-133
0x18	NFC_DATA_NUM	Read/written data count configuration register	4-133
0x1C	NFC_OP	Operation register	4-134
0x20	NFC_STATUS	Status register	4-135
0x24	NFC_INTEN	Interrupt enable register	4-136
0x28	NFC_INTS	Interrupt status register	4-137
0x2C	NFC_INTCLR	Interrupt clear register	4-138
0x30	NFC_LOCK	Lock address configuration register	4-139
0x34	NFC_LOCK_SA0	Lock start address 0 configuration register	4-140
0x38	NFC_LOCK_SA1	Lock start address 1 configuration register	4-141
0x3C	NFC_LOCK_SA2	Lock start address 2 configuration register	4-141
0x40	NFC_LOCK_SA3	Lock start address 3 configuration register	4-142
0x44	NFC_LOCK_EA0	Lock end address 0 configuration register	4-142
0x48	NFC_LOCK_EA1	Lock end address 1 configuration register	4-143
0x4C	NFC_LOCK_EA2	Lock end address 2 configuration register	4-144

0x50	NFC_LOCK_EA3	Lock end address 3 configuration register	4-144
0x54	NFC_EXPCMD	Extended page command register	4-145
0x58	NFC_EXBCMD	Extended block command register	4-145
0x5C	NFC_ECC_TEST	ECC test register	4-146
0x60	NFC_DMA_CTRL	DMA control register	4-146
0x64	NFC_BADDR_D	Base address register of the data transfer area.	4-148
0x68	NFC_BADDR_OOB	Base address register of the out-of-band (OOB) area.	4-148
0x6C	NFC_DMA_LEN	Transfer length register.	4-149
0x70	NFC_OP_PARA	Operation parameter register	4-149
0x74	NFC_VERSION	Controller version register	4-151
0x78	NFC_BUF_BADDR	Base address register of the NANDC buffer	4-151
0x7C	NFC_RD_LOGIC_ADDR	Logic address register for reading the NAND flash in DMA mode	4-152
0x80	NFC_RD_LOGIC_LEN	Logic length register for reading the NAND flash in DMA mode	4-153
0x90	NFC_FIFO_EMPTY	Internal FIFO status register	4-153
0x94	NFC_BOOT_SET	Boot parameter configuration register	4-153
0x98	NF_STATUS	NAND flash status register	4-154

4.3.8 Register Description

NFC_CON

NFC_CON is a NANDC configuration register.

Offset Address	Register Name	Total Reset Value
0x00	NFC_CON	0x0000_0182

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				edo_en	ecc_type			rb_sel	cs_ctrl	reserved		bus_width	pagesize		op_mode

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:12]	-	reserved	Reserved.
[11]	RW	edo_en	NAND flash data read enable in EDO mode. 0: normal mode 1: EDO mode This function must be used according to the requirements of specific memories.
[10:8]	RW	ecc_type	ECC mode select. 000: non-ECC mode 001: 1-bit mode 010: 4-bit mode 011: reserved 100: 24-bit mode for 1 KB 101–111: reserved The reset value depends on the NFC_ECC_TYPE pin.
[7]	RW	rb_sel	This field is valid when multiple external NAND flash memories (multiple CSs) are connected. 0: The NAND flash memories share a ready/busy signal. 1: The NAND flash memories use their own ready/busy signals. When only one NAND flash is connected, only CS0 and ready/busy 0 are used.
[6]	RW	cs_ctrl	CS control. 0: When the NAND flash is busy, the CS signal is fixed at 0. 1: When the NAND flash is busy, the CS signal is set to 1. This mode maps to the "cs do not care" mode of the NAND flash.
[5:4]	-	reserved	Reserved.
[3]	RW	bus_width	Data line width of the NAND flash. 0: 8 bits. 1: 16 bits The reset value depends on the NFC_BUS_WIDE pin.
[2:1]	RW	pagesize	Page size of the NAND flash. 01: 2 KB 10: 4 KB 11: 8 KB Other values: reserved The reset value depends on the NFC_PAGE_SIZE pin.

[0]	RW	op_mode	Operating mode of the NANDC. 0: boot mode 1: normal mode

NFC_PWIDTH

NFC_PWIDTH is a read/write pulse width configuration register.

Offset Address	Register Name	Total Reset Value
0x04	NFC_PWIDTH	0x0000_0333

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				rw_hcnt				r_lcnt				w_lcnt			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0	1	1

Bits	Access	Name	Description
[31:12]	-	reserved	Reserved.
[11:8]	RW	rw_hcnt	High-level width of the read/write signal of the NAND flash. 0x0–0xF: 1–16 clock cycles.
[7:4]	RW	r_lcnt	Low-level width of the read signal of the NAND flash. 0x0–0xF: 1–16 clock cycles.
[3:0]	RW	w_lcnt	Low-level width of the write signal of the NAND flash. 0x0–0xF: 1–16 clock cycles.

NFC_OPIDLE

NFC_OPIDLE is an operation interval configuration register.

Offset Address	Register Name	Total Reset Value
0x08	NFC_OPIDLE	0x00FF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								frb_wait				cmd1_wait				addr_wait				write_data_wait				cmd2_wait				frb_idle			
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.

[23:20]	RW	frb_wait	When a number of cycles are delayed after a read/write command is sent, the ready signal is detected to check whether it becomes high. The number of delay cycles is frb_wait x 8.
[19:16]	RW	cmd1_wait	Number of wait cycles after command 1 is sent. 0x0–0xF: 1–16 clock cycles.
[15:12]	RW	addr_wait	Number of wait cycles after the address is sent. 0x0–0xF: 1–16 clock cycles.
[11:8]	RW	write_data_wait	Number of wait cycles after data is written. 0x0–0xF: 1–16 clock cycles.
[7:4]	RW	cmd2_wait	Number of wait cycles after command 2 is sent. 0x0–0xF: 1–16 clock cycles.
[3:0]	RW	frb_idle	A read signal can be sent only when a number of cycles are delayed after the ready signal of the NAND flash becomes high. The number of delay cycles is frb_idle x 8.

NFC_CMD

NFC_CMD is a command word configuration register.

Offset Address	Register Name	Total Reset Value
0x0C	NFC_CMD	0x0070_3000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								read_status_cmd								cmd2								cmd1							
Reset	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:16]	RW	read_status_cmd	Read status command word.
[15:8]	RW	cmd2	Command 2 that is sent to the NAND flash by the NANDC.
[7:0]	RW	cmd1	Command 1 that is sent to the NAND flash by the NANDC.

NFC_ADDRL

NFC_ADDRL is a lower-bit address configuration register.

Offset Address	Register Name	Total Reset Value
0x10	NFC_ADDRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	addr_l																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	addr_l	Lower 32-bit address of the NAND flash.

NFC_ADDRH

NFC_ADDRH is an upper-bit address configuration register.

Offset Address	Register Name	Total Reset Value
0x14	NFC_ADDRH	0x0000_00000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																addr_h															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	addr_h	Upper 16-bit address of the NAND flash.

NFC_DATA_NUM

NFC_DATA_NUM is a read/written data count configuration register.

Offset Address	Register Name	Total Reset Value
0x18	NFC_DATA_NUM	0x0000_0840

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				nfc_data_num											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	-	reserved	Reserved.
[11:0]	RW	nfc_data_num	Number of data segments that are read and written randomly by the NANDC. The maximum value is 2368 bytes. **Note: This field is valid only when ecc_type is 00.**

NFC_OP

NFC_OP is an operation register.

Offset Address	Register Name	Total Reset Value
0x1C	NFC_OP	0x0000_0A6E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				address_cycles				nf_cs				cmd1_en	addr_en	write_data_en	cmd2_en	wait_ready_en	read_data_en	read_status_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	1	0	1	1	1	0

Bits	Access	Name	Description
[31:12]	-	reserved	Reserved.
[11:9]	RW	address_cycles	Number of address cycles sent to the NAND flash.
[8:7]	RW	nf_cs	NAND flash CS signal select. 00: CS 0 01: CS 1 Other values: reserved
[6]	RW	cmd1_en	Command 1 transmit enable. 0: disabled 1: enabled
[5]	RW	addr_en	NAND flash address write enable. 0: disabled 1: enabled
[4]	RW	write_data_en	NAND flash data write enable. 0: disabled 1: enabled **Note: read_data_en and write_data_en cannot be 1 at the same time.**
[3]	RW	cmd2_en	Command 2 transmit enable. 0: disabled 1: enabled
[2]	RW	wait_ready_en	Wait ready/busy high enable. 0: disabled 1: enabled

[1]	RW	read_data_en	NAND flash data read enable by starting to read the state machine. 0: disabled 1: enabled **Note: read_data_en and write_data_en cannot be 1 at the same time.**
[0]	RW	read_status_en	When this bit is 1, the command 0x70 for reading the status is sent to the NAND flash and the status data is read from the NAND flash. After that, the returned data is written to the NFC_STATUS field of the NANDC status register instead of the internal buffer. After the NAND flash is erased and programmed, the results need to be read to check whether the operations are successful. If this bit is enabled, the operations such as erasing and programming can be performed at a time, and the data indicating whether the operation is successful can be returned from the NAND flash. In this way, the CPU intervention is reduced. **Note: When read_data_en is 1, this bit is invalid.**

NFC_STATUS

NFC_STATUS is a status register.

Offset Address	Register Name	Total Reset Value
0x20	NFC_STATUS	0x0000_001F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				nf_status								reserved			nf1_ready	nf0_ready	nfc_ready
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved.
[12:5]	RO	nf_status	Status data read from the NAND flash. This field is valid only when both NFC_OP[read_status] and NFC_STATUS[nfc_ready] are 1.
[4:3]	-	reserved	Reserved.
[2]	RO	nf1_ready	Status of the ready/busy signal of the NAND flash corresponding to CS 1. This bit is valid when multiple flash memories are connected and they use their own ready_busy signals. This is because multiple NAND flash memories share a ready/busy signal by default. The reset value of the bit is 0.
[1]	RO	nf0_ready	Status of the ready/busy signal of the NAND flash corresponding

			to CS 0. This bit is valid when multiple flash memories are connected and they use their own ready_busy signals. This is because multiple NAND flash memories share a ready/busy signal by default. The reset value of the bit is 0.
[0]	RO	nfc_ready	Status of the ready/busy signal of the NANDC. 0: The NANDC is working. 1: The operation is complete and the next command can be received. When NFC_OP is written to start a NANDC operation, the bit is cleared automatically.

NFC_INTEN

NFC_INTEN is an interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x24	NFC_INTEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							wr_lock_en	ahb_op_en	err_invalid	err_valid	reserved		cs1_done_en	cs0_done_en	op_done_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	-	reserved	Reserved.
[8]	RW	wr_lock_en	Lock address write error interrupt enable. 0: disabled 1: enabled
[7]	RW	ahb_op_en	CPU read/write NANDC buffer error interrupt enable when the NANDC is reading/writing data from/to the NAND flash. 0: disabled 1: enabled
[6]	RW	err_invalid	Uncorrectable error interrupt.
[5]	RW	err_valid	Correctable error interrupt.
[4:3]	-	reserved	Reserved.
[2]	RW	cs1_done_en	CS 1 ready/busy signal going high interrupt enable. 0: disabled 1: enabled

[1]	RW	cs0_done_en	CS 0 ready/busy signal going high interrupt enable. 0: disabled 1: enabled
[0]	RW	op_done_en	Current operation done enable of the NANDC. 0: disabled 1: enabled

NFC_INTS

NFC_INTS is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0x28	NFC_INTS	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							wr_lock_en	ahb_op_en	err_invalid	err_vavid	reserved		cs1_done	cs0_done	op_done
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:9]	-	reserved	Reserved.
[8]	RO	wr_lock_en	Interrupt generated when the lock address is written. 0: No interrupt is generated. 1: An interrupt is generated.
[7]	RO	ahb_op_en	Interrupt generated when the CPU reads and writes the NANDC buffer in the process of reading/writing data from/to the NAND flash by the NANDC. 0: No interrupt is generated. 1: An interrupt is generated.
[6]	RO	err_invalid	Uncorrectable error interrupt. 0: No interrupt is generated. 1: An interrupt is generated. In 1-bit ECC mode, if errors occur in two or more bits in the checked 512-byte data, an interrupt is generated. In 4-bit ECC mode, if errors occur in five or more bits in the checked 512-byte data, an interrupt is generated. In 8-bit ECC mode, if errors occur in eight or more bits in the checked 512-byte data, an interrupt is generated.

[5]	RO	err_vavid	Correctable error interrupt. 0: No interrupt is generated. 1: An interrupt is generated. In 1-bit ECC mode, if an error occurs in one bit in the checked 512-byte data, an interrupt is generated. In 4-bit ECC mode, if errors occur in one to four bits in the checked 512-byte data, an interrupt is generated. In 8-bit ECC mode, if errors occur in one to eight bits of the checked 512-byte data, an interrupt is generated.
[4:3]	-	reserved	Reserved.
[2]	RO	cs1_done	CS 1 ready/busy signal going high interrupt. 0: No interrupt is generated. 1: An interrupt is generated. This bit is valid when two flash memories are connected and the two flash memories use their own ready/busy signals. Otherwise, the bit is fixed at 0.
[1]	RO	cs0_done	CS 0 ready/busy signal going high interrupt. 0: No interrupt is generated. 1: An interrupt is generated. This bit is valid when two flash memories are connected and the two flash memories use their own ready/busy signals. Otherwise, the bit is fixed at 0.
[0]	RO	op_done	Current operation done interrupt of the NANDC. 0: No interrupt is generated. 1: An interrupt is generated. After NFC_OP is written, the bit is automatically cleared.

NFC_INTCLR

NFC_INTCLR is an interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x2C	NFC_INTCLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							wr_lock_en	ahb_op_en	r_5bit_err_clr	r_4bit_err_clr	reserved			cs1_done_clr	cs0_done_clr	op_done_clr

Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	-	reserved	Reserved.
[8]	WO	wr_lock_en	wr_lock_en interrupt clear. 0: not cleared 1: cleared
[7]	WO	ahb_op_en	ahb_op_en interrupt clear. 0: not cleared 1: cleared
[6]	WO	r_5bit_err_clr	r_5bit_err interrupt clear. 0: not cleared 1: cleared
[5]	WO	r_4bit_err_clr	r_4bit_err interrupt clear. 0: not cleared 1: cleared
[4:3]	-	reserved	Reserved.
[2]	WO	cs1_done_clr	cs1_done interrupt clear. 0: not cleared 1: cleared
[1]	WO	cs0_done_clr	cs0_done interrupt clear. 0: not cleared 1: cleared
[0]	WO	op_done_clr	op_done interrupt clear. 0: not cleared 1: cleared

NFC_LOCK

NFC_LOCK is a lock address configuration register.

Offset Address	Register Name	Total Reset Value
0x30	NFC_LOCK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												lock_excmd_en	lock_en	global_lock_en	lock_down

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	-	reserved	Reserved.
[3]	RW	lock_excmd_en	Protection address write-protection enable according to the extended write command (new commands may be added to new memories). 0: disabled 1: enabled
[2]	RW	lock_en	Flash lock enable. When this control bit is 1, if the erased or programmed address is between the start lock address and the end lock address, the erasing and programming operations are invalid. 0: disabled 1: enabled
[1]	RW	global_lock_en	Flash global lock enable. When this bit is 1, the NAND flash cannot be erased or programmed. 0: disabled 1: enabled
[0]	RW	lock_down	NAND flash lock mode. 0: lock mode 1: lock-down mode. After the value 1 is written, this bit cannot be written. In addition, this bit can be cleared only when a hard reset is performed.

NFC_LOCK_SA0

NFC_LOCK_SA0 is lock start address 0 configuration register.

Offset Address	Register Name	Total Reset Value
0x34	NFC_LOCK_SA0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												flash_lock_cs	flash_lock_addr0																		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	-	reserved	Reserved.

[20:19]	RW	flash_lock_cs	NAND flash lock CS. 00: CS 0 01: CS 1 Other values: reserved
[18:0]	RW	flash_lock_addr0	Lock start address 0. The LSB maps to the fifth row address of the NAND flash.

NFC_LOCK_SA1

NFC_LOCK_SA1 is lock start address 1 configuration register.

Offset Address	Register Name	Total Reset Value
0x38	NFC_LOCK_SA1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												flash_lock_cs	flash_lock_addr1																		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	-	reserved	Reserved.
[20:19]	RW	flash_lock_cs	NAND flash lock CS. 00: CS 0 01: CS 1 Other values: reserved
[18:0]	RW	flash_lock_addr1	Lock start address 1. The LSB maps to the fifth row address of the NAND flash.

NFC_LOCK_SA2

NFC_LOCK_SA2 is lock start address 2 configuration register.

Offset Address	Register Name	Total Reset Value
0x3C	NFC_LOCK_SA2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												flash_lock_cs	flash_lock_addr2																		

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	-	reserved	Reserved.
[20:19]	RW	flash_lock_cs	NAND flash lock CS. 00: CS 0 01: CS 1 Other values: reserved
[18:0]	RW	flash_lock_addr2	Lock start address 2. The LSB maps to the fifth row address of the NAND flash.

NFC_LOCK_SA3

NFC_LOCK_SA3 is lock start address 3 configuration register.

Offset Address	Register Name	Total Reset Value
0x40	NFC_LOCK_SA3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												flash_lock_cs	flash_lock_addr3																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	-	reserved	Reserved.
[20:19]	RW	flash_lock_cs	NAND flash lock CS. 00: CS 0 01: CS 1 Other values: reserved
[18:0]	RW	flash_lock_addr3	Lock start address 3. The LSB maps to the fifth row address of the NAND flash.

NFC_LOCK_EA0

NFC_LOCK_EA0 is lock end address 0 configuration register.

Offset Address	Register Name	Total Reset Value
0x44	NFC_LOCK_EA0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												flash_lock_cs				flash_lock_eaddr0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	-	reserved	Reserved.
[20:19]	RW	flash_lock_cs	NAND flash lock CS. 00: CS 0 01: CS 1 Other values: reserved
[18:0]	RW	flash_lock_eaddr0	Lock end address 0. The LSB maps to the fifth row address of the NAND flash.

NFC_LOCK_EA1

NFC_LOCK_EA1 is lock end address 1 configuration register.

Offset Address	Register Name	Total Reset Value
0x48	NFC_LOCK_EA1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												flash_lock_cs				flash_lock_eaddr1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	-	reserved	Reserved.
[20:19]	RW	flash_lock_cs	NAND flash lock CS. 00: CS 0 01: CS 1 Other values: reserved
[18:0]	RW	flash_lock_eaddr1	Lock end address 1. The LSB maps to the fifth row address of the NAND flash.

NFC_LOCK_EA2

NFC_LOCK_EA2 is lock end address 2 configuration register.

Offset Address	Register Name	Total Reset Value
0x4C	NFC_LOCK_EA2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												flash_lock_cs	flash_lock_eaddr2																		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	-	reserved	Reserved.
[20:19]	RW	flash_lock_cs	NAND flash lock CS. 00: CS 0 01: CS 1 Other values: reserved
[18:0]	RW	flash_lock_eaddr2	Lock end address 2. The LSB maps to the fifth row address of the NAND flash.

NFC_LOCK_EA3

NFC_LOCK_EA3 is lock end address 3 configuration register.

Offset Address	Register Name	Total Reset Value
0x50	NFC_LOCK_EA3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												flash_lock_cs	flash_lock_eaddr3																		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	-	reserved	Reserved.

[20:19]	RW	flash_lock_cs	NAND flash lock CS. 00: CS 0 01: CS 1 Other values: reserved
[18:0]	RW	flash_lock_eaddr3	Lock end address 3. The LSB maps to the fifth row address of the NAND flash.

NFC_EXPCMD

NFC_EXPCMD is an extended page command register.

Offset Address	Register Name	Total Reset Value
0x54	NFC_EXPCMD	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	ex_pcmd3		ex_pcmd2		ex_pcmd1		ex_pcmd0	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	ex_pcmd3	Extended page write command 3 of the NAND flash.
[23:16]	RW	ex_pcmd2	Extended page write command 2 of the NAND flash.
[15:8]	RW	ex_pcmd1	Extended page write command 1 of the NAND flash.
[7:0]	RW	ex_pcmd0	Extended page write command 0 of the NAND flash.

NFC_EXBCMD

NFC_EXBCMD is an extended block command register.

Offset Address	Register Name	Total Reset Value
0x58	NFC_EXBCMD	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				ex_bcmd1		ex_bcmd0	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:8]	RW	ex_bcmd1	Extended block write command 1 of the NAND flash.
[7:0]	RW	ex_bcmd0	Extended block write command 0 of the NAND flash.

NFC_ECC_TEST

NFC_ECC_TEST is an ECC test register.

Offset Address	Register Name	Total Reset Value
0x5C	NFC_ECC_TEST	0x0000_0021

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													ecc_mask	dec_only	enc_only
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1

Bits	Access	Name	Description
[31:3]	-	reserved	Reserved.
[2]	RW	ecc_mask	ECC function mask. 0: Whether the ECC check and correction are performed depends on the value of ecc_type. 1: The ECC check and correction are forbidden. The structure of the data read from or written to the NAND flash is still converted based on the format of ecc_type.
[1]	RW	dec_only	Decoding only enable. When 1 is written to this bit, ECC decoding is enabled, but the NAND flash is not read or written. When the bit is read, the value 0 is returned.
[0]	RW	enc_only	Encoding only enable. When 1 is written to this bit, ECC encoding is enabled, but the NAND flash is not read or written. When this bit is read, the return value 1 indicates that ECC encoding and decoding are complete and the value 0 indicates that ECC encoding and decoding are in progress.

NFC_DMA_CTRL

NFC_DMA_CTRL is a DMA control register.

Offset Address	Register Name	Total Reset Value
0x60	NFC_DMA_CTRL	0x0000_0070

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				wr_cmd_disable	rw_nf_disable	dma_nf_cs		dma_addr_num	burst16_en	burst8_en	burst4_en	reserved			dma_wr_en	dma_start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0

Bits	Access	Name	Description
[31:12]	-	reserved	Reserved.
[11]	RW	wr_cmd_disable	Whether the NANDC initiates a complete timing for reading/writing to the NAND flash. 0: The NANDC initiates a complete timing for reading/writing to the NAND flash. 1: The NANDC initiates a timing for reading/writing to data rather than a command. That is, the NANDC initiates CS signals and read/write pulse signals for reading/writing data rather than the CLE and ALE signals.
[10]	RW	rw_nf_disable	Whether the DMA operation and the read/write operation are performed at the same time. 0: The DMA operation and the read/write operation on the NAND flash are performed at the same time. 1: Data is transferred between the buffer and the DDR, but the NAND flash is not read or written.
[9:8]	RW	dma_nf_cs	NAND flash CS select for operating the DMA. 00: CS 0 01: CS 1 Other values: reserved
[7]	RW	dma_addr_num	Number of addresses. 0: 5 addresses 1: 4 addresses
[6]	RW	burst16_en	Burst 16 enable. 0: disabled 1: enabled
[5]	RW	burst8_en	Burst 8 enable. 0: disabled 1: enabled

[4]	RW	burst4_en	Burst 4 enable. 0: disabled 1: enabled
[3]	RW	oob_area_en	OOB area write enable. This bit is valid only in 1-bit ECC mode. 0: disabled 1: enabled
[2]	RW	data_area_en	Data area write enable. This bit is valid only in 1-bit ECC mode. 0: disabled 1: enabled
[1]	RW	dma_wr_en	DMA read/write enable. 0: read 1: write
[0]	RW	dma_start	DMA operation enable. When the value 1 is written to this bit, the DMA operations are enabled. The bit retains 1 until the DMA operations are complete. Writing 0 to this bit has no effect. If the value 0 is returned after this bit is read, the DMA operations are complete.

NFC_BADDR_D

NFC_BADDR_D is a base address register of the data transfer area in DMA mode.

Offset Address	Register Name	Total Reset Value
0x64	NFC_BADDR_D	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	base_addr_d																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	base_addr_d	Base address of the DDR data area that stores the data to be read or written.

NFC_BADDR_OOB

NFC_BADDR_OOB is a base address register of the OOB area in DMA mode.

Offset Address	Register Name	Total Reset Value
0x68	NFC_BADDR_OOB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	base_addr_oob																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	base_addr_oob	Base address of the OOB area that stores the data to be read. This register is valid only when the NAND flash is written in DMA mode.

NFC_DMA_LEN

NFC_DMA_LEN is a transfer length register in DMA mode.

Offset Address	Register Name	Total Reset Value
0x6C	NFC_DMA_LEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				len_oob												reserved				len_data											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RW	reserved	Reserved.
[28:16]	RW	len_oob	Length of the OOB area when the NAND flash is written in DMA mode. The long words must be 4-byte aligned. This field is valid only in ECC0 mode. In other modes, the OOB length is fixed.
[15:12]	RW	reserved	Reserved.
[11:0]	RW	len_data	Length of the data to be read or written in DMA mode. This field is valid only when rw_nf_disable is 1.

NFC_OP_PARA

NF_OP_PARA is an operation parameter register.

Offset Address	Register Name	Total Reset Value
0x70	NFC_OP_PARA	0x0000_007F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ext_len		oob_ecc_en	data_ecc_en	oob_edc_en	data_edc_en	oob_rw_en	data_rw_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved.
[7:6]	RW	ext_len	Length of the extended data area to be corrected. In 24-bit ECC mode, this field indicates the length of the extended data area in each ECC data block. In boot mode, when the page size is 4 KB, the default length is 8 bytes; when the page size is 8 KB, the default length is 4 bytes. 01: 4 bytes 11: 8 bytes Other values: reserved
[5]	RW	oob_ecc_en	ECC correction enable in OOB area. 0: disabled 1: enabled This field is valid only when data is read.
[4]	RW	data_ecc_en	ECC correction enable. 0: disabled 1: enabled This field is valid only when data is read.
[3]	RW	oob_edc_en	OOB area check enable. 0: disabled 1: enabled In programming mode, the function of generating the ECC code of the OOB area is enabled. In data read mode, the check on the OOB area is enabled.
[2]	RW	data_edc_en	Check enable. 0: disabled 1: enabled In programming mode, ECC code is generated. In data read mode, the check is enabled.

[1]	RW	oob_rw_en	Read/write redundancy enable for the data area of the NAND flash. 0: disabled 1: enabled
[0]	RW	data_rw_en	Read/write enable for the data area of the NAND flash. 0: disabled 1: enabled

NFC_VERSION

NFC_VERSION is a version register.

Offset Address	Register Name	Total Reset Value
0x74	NFC_VERSION	0x0000_0310

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	version_id																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	version_id	Version number.

NFC_BUF_BADDR

NFC_BUF_BADDR is a NANDC buffer base address register.

Offset Address	Register Name	Total Reset Value
0x78	NFC_BUF_BADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				buf_baddr_rd												reserved				buf_baddr_wr											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27:16]	RW	buf_baddr_rd	Indicates the base address from which the buffer is read in DMA mode when rw_nf_disable is 1. Indicates undefined when rw_nf_disable is 0.
[15:12]	RW	reserved	Reserved.
[11:0]	RW	buf_baddr_wr	Indicates the base address from which the buffer is written in DMA mode when rw_nf_disable is 1.

			Indicates undefined when rw_nf_disable is 0.

NFC_RD_LOGIC_ADDR

NFC_RD_LOGIC_ADDR is a logic address register for reading the NAND flash in DMA mode

Offset Address	Register Name	Total Reset Value
0x007C	NFC_RD_LOGIC_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rd_logic_addr															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	rd_logic_addr	Start address (excluding the ECC code) for reading data. For example, if you want to read data from the bad block flag, you can set the field value to 2048 for the 2 KB page size or 4096 for the 4 KB page size. After data is read in DMA mode, the field value is automatically accumulated based on the value of NFC_DMA_LEN[len_data]. The rd_logic_addr field is valid only when data is read in DMA mode and NFC_DMA_CTRL[rw_nf_disable] is 0.

NFC_RD_LOGIC_LEN

NFC_RD_LOGIC_LEN is a logic length register for reading the NAND flash in DMA mode.

Offset Address	Register Name	Total Reset Value
0x0080	NFC_RD_LOGIC_LEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rd_logic_len															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	rd_logic_len	Length (excluding the length of the ECC code) of the data read from the NAND flash in DMA mode. After data is read in DMA mode, the field value is cleared automatically. The rd_logic_addr field is valid only when data is read in DMA mode and NFC_DMA_CTRL[rw_nf_disable] is 0.

NFC_FIFO_EMPTY

NFC_FIFO_EMPTY is an internal FIFO status register.

Offset Address	Register Name	Total Reset Value
0x0090	NFC_FIFO_EMPTY	0x0000_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																empty_dbg															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RO	empty_dbg	Empty status of the internal FIFO, for debugging only.

NFC_BOOT_SET

NFC_BOOT_SET is a boot parameter configuration register.

Offset Address	Register Name	Total Reset Value
0x0094	NFC_BOOT_SET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														addr_num	block_size
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	-	rsv	Reserved.
[1]	RW	addr_num	Number of addresses sent to the NAND flash by the NANDC during booting. 0: 4 address cycles 1: 5 address cycles. The reset value depends on the nfc_addr_num pin.
[0]	RW	block_size	Bus width of the NAND flash during booting. 0: 64 pages 1: 128 pages The reset value depends on the nfc_block_size pin.

NF_STATUS

NF_STATUS is a NAND flash status register.

Offset Address	Register Name	Total Reset Value
0x0098	NF_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								status							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved.
[7:0]	RO	status	Status data read from the NAND flash. This field is valid when NFC_OP is written and NFC_OP[read_status_en] is 1.

Contents

Figures

Tables

5 ETH

5.1 Overview

The Ethernet (ETH) module provides an ETH module interface that is used to receive data or transmit data through the network interface at a speed of 10 Mbit/s or 100 Mbit/s. This module also supports half-duplex or full-duplex operating mode and provides the media independent interface (MII) and reduced media-independent interface (RMII). With the eight configurable DMAC address filter tables, the ETH module filters input frames received through the network interface, limiting the traffic of the CPU port to protect the CPU against heavy traffic.

5.2 Function Description

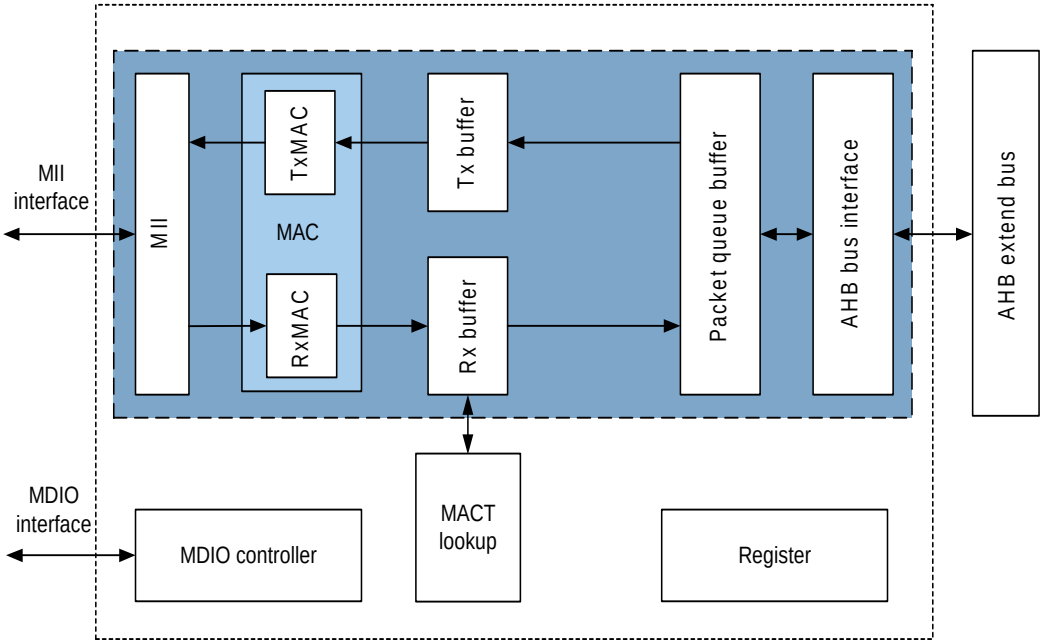
The ETH module has the following features:

- Supports one ETH module interface.
- Supports the rate of 10 Mbit/s or 100 Mbit/s.
- Supports full-duplex or half-duplex operating mode.
- Supports the MII and RMII.
- Supports collision back-off and retransmission and late collision in half-duplex mode.
- Supports the transmission of flow control frames in full-duplex mode.
- Supports detection of frame length validity and the discarding of extra-long and extra-short frames.
- Implements cyclic redundancy check (CRC) on the input frames. The frames with CRC errors are discarded.
- Implements CRC check on the output frames
- Supports short-frame stuffing.
- Supports the loopback to internal and loopback to external in full-duplex mode.
- Supports auto-adaption to automatically query the working state of the physical layer entity sublayer (PHY) chip.
- Provides the management data input/output (MDIO) interfaces with configurable frequency.
- Provides 64 frame management queues for both data receive (RX) and data transmit (TX).

- Provides traffic limit to prevent the CPU against traffic attack.
- Supports the count of received frames and transmitted frames.
- Provides a RX buffer of 512 bytes and a TX buffer of 1536 bytes.
- Supports eight configurable DMAC address filter tables.
- Controls whether to forward or discard broadcast frames, multicast frames, and unicast frames.
- Supports 802.3az (energy-efficient Ethernet).

Figure 5-1 shows the logic block diagram of the ETH module.

Figure 5-1 Logic block diagram of the ETH module



5.3 Signal Description

Table 5-1 and Table 5-2 list signals of the ETH interface.

Table 5-1 MDIO interface signals

Signal	Direction	Description	Pin
MDCK	O	Clock output of MDIO interface	MDCK
MDIO	I/O	Input/output signal of the MDIO interface	MDIO

Table 5-2 MII interface signals

Signal	Direction	Description	Pin
RMII_REF_CLK	I/O	Uplink RMII reference clock	RMII_REFCLK
MII_TXCK	I	MII TX clock	MII_TXCK
MII_TXD[3:0]/ RMII_TXD[1:0]	O	MII/RMII TX data	MII_TXD3−MII_TXD0
MII_TXEN/RMII_TXEN	O	MII/RMII TX data valid	MII_TXEN
MII_TXER	O	MII TX data error indicator	MII_TXER
MII_RXCK	I	MII RX data clock	MII_RXCK
MII_RXD[3:0]/ RMII_RXD[1:0]	I	MII/RMII RX data	MII_RXD3−MII_RXD0
MII_RXDV/RMII_CRS_DV	I	MII/RMII RX data valid	MII_RXDV
MII_RXER	I	MII RX data error indicator	MII_RXER
MII_CRS	I	MII carrier valid	MII_CRS
MII_COL	I	MII collision	MII_COL

5.4 Operating Mode

5.4.1 Process of Receiving Frames

During initialization, software needs to perform the following operations:

- Software needs to request a certain number of buffers. The number is equal to the RX queue depths and the size of each buffer is 2 KB. Then, software writes the header addresses of the buffers to the frame RX queue one by one. The times of the write operation is equal to the configured RX queue depth.
- The configured buffers should not be released during frame receiving. If the configured header address is not a word aligned address, the byte address corresponding to the header address must be a writable address.

The CPU performs the following steps when it is informed that a frame needs to be received:

Step 1 Read the frame descriptor (including the start address and frame length of the RX frame) in the register UD_GLB_IQFRM_DES.

Step 2 Process the data and write 1 to clear GLB_IRQ_RAW[iraw_rx_up] (indicating that the CPU completes the frame receiving).

----End

After receiving a frame of data, software needs to re-apply for a buffer of 2 KB and re-write the header address to the frame descriptor of the current RX queue. Otherwise, the available depth of RX queues equals to the number of buffers assigned to the CPU rather than the value configured by the CPU.

Table 5-5 describes the data structure of the frame descriptor received by the CPU.

Table 5-3 Data structure of the frame descriptor received by the CPU

Bits	Name	Description
[63:32]	rxfrm_saddr	Start address for receiving frames.
[31:18]	reserved	Reserved.
[17:12]	fd_in_addr	Relative address of the frame to be received in the input queue (IQ). It serves as the index (0 to iq_len - 1) of the absolute addresses for storing frames.
[11:0]	fd_in_len	Length of the frame to be received in the IQ.

NOTE
The length of the RX queue can be obtained by querying UD_GLB_ADDRQ_STAT.

The CPU can receive a frame in interrupt or query mode.

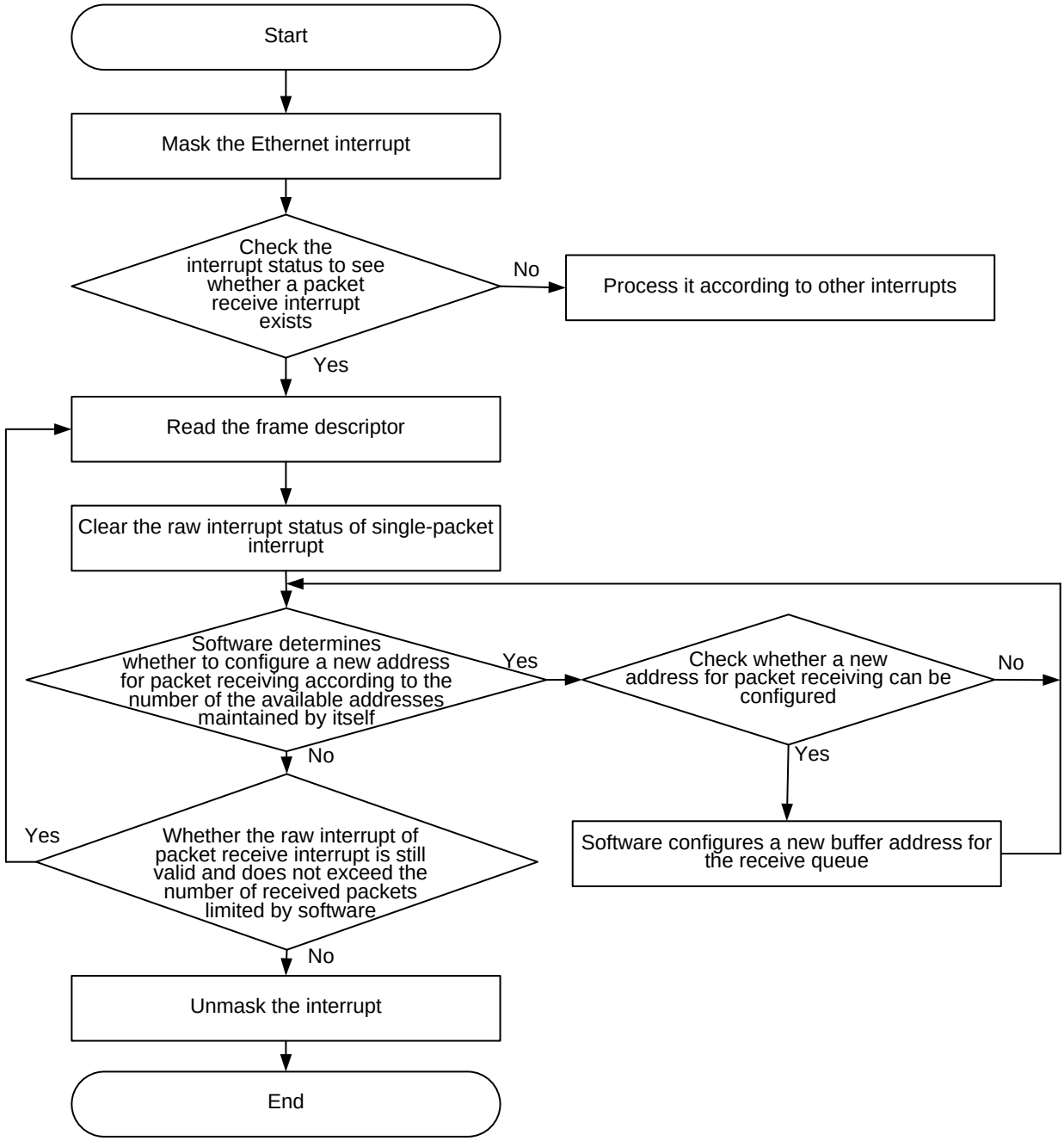
2. Receiving a frame in interrupt mode

   When the CPU enables the frame RX interrupt, depending on the frames to be received, hardware generates frame RX interrupts (single-packet interrupt and multi-packet interrupt) int_rx_up and int_rxd_up.

   int_rx_up indicates that an interrupt is reported each time a packet is received.

   int_rxd_up indicates that an interrupt is reported each time a number of specified packets are received. Figure 5-11 shows the process of receiving a frame in interrupt mode.

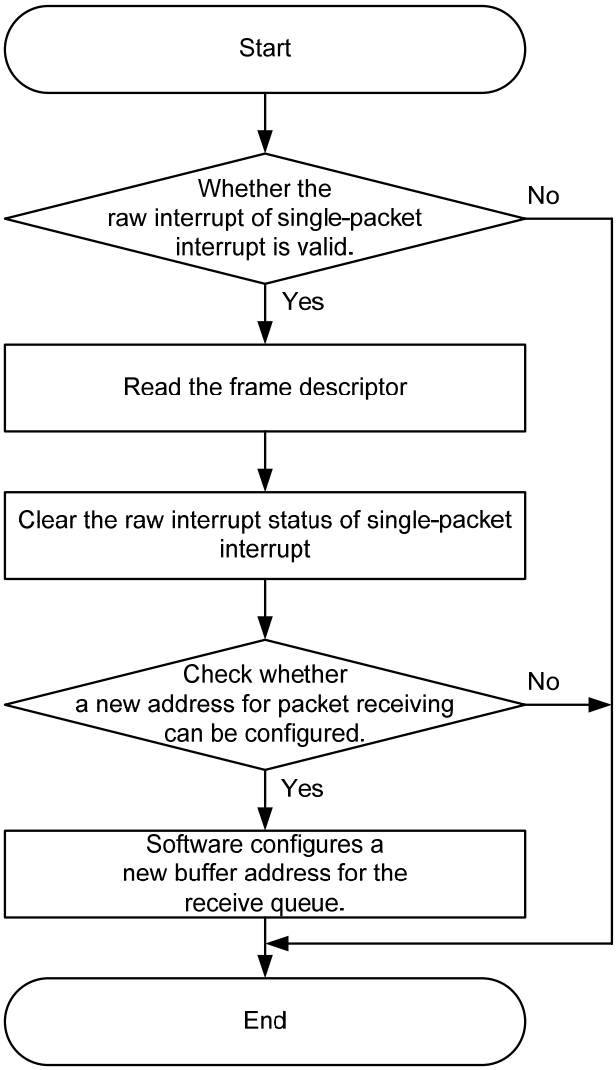
Figure 5-2 Process of receiving a frame in interrupt mode



3. Receiving a frame in query mode

   In this mode, the CPU does not enable the frame RX interrupt bit, namely, GLB_IRQ_ENA[ien_rx_up], but automatically queries GLB_IRQ_RAW[iraw_rx_up]. If GLB_IRQ_RAW[iraw_rx_up] is 1, it indicates that there is a frame to be received by the CPU. Figure 5-12 shows the process of receiving a frame in query mode.

Figure 5-3 Process of receiving a frame in query mode



5.4.2 Process of Transmitting a Frame

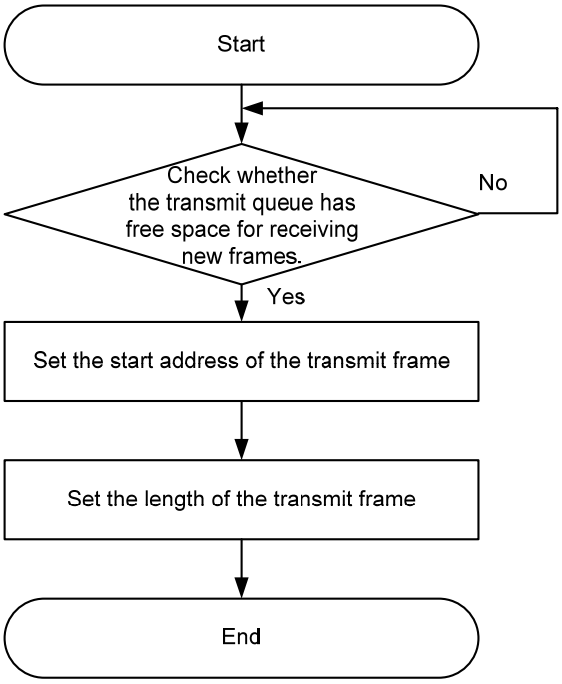
When a frame is transmitted, the CPU checks whether the current queue has any available space. If the space is sufficient, the CPU writes the header address of the buffer and then the length of the TX frame to the frame descriptor of the TX queue. The frame length trigger hardware for writing the TX frame writes the header address and frame length of the TX frame to the TX queue. Each time after a write is performed on the register, a data packet is transmitted. Therefore, software must control the write to the frame length register so that the frame length register is not written arbitrarily.

The frame format is as follows:

Destination MAC	Source MAC	Type	Data	FCS

Figure 5-13 shows the process of transmitting a frame by the CPU.

Figure 5-4 Process of transmitting a frame by the CPU



When the frame transmitted by the CPU is buffered in the SDRAM, the frame descriptor is not included. The frame descriptor is written to UD_GLB_EQ_ADDR and UD_GLB_EQFRM_LEN to notify the ETH module of adding the frame (descriptor) to the queue. Table 5-6 describes the data structure of the frame descriptor transmitted by the CPU.

Table 5-4 Data structure of the frame descriptor transmitted by the CPU

Bits	Name	Description
[42:11]	start_addr_eq	Header address of a frame.
[10:0]	fm_len	Frame length in the unit of byte.

Note: The frames whose fm_len is less than 20 bytes or greater than 1,900 bytes are discarded. In other words, the allowed range is from 20 bytes to 1900 bytes.

NOTE

The usage of the TX queues for the current CPU can be obtained by querying UD_GLB_ADDRQ_STAT.

The CPU can transmit a frame in interrupt or query mode.

2. Transmitting a frame in interrupt mode

   The CPU enables the nonempty-to-empty interrupt (int_freeeq_up) of the TX queue of the ETH module and allows the interrupt to be notified to the CPU. If the TX queue of the ETH module changes from nonempty to empty, it indicates the ETH module can transmit a frame. Then, hardware generates an interrupt to notify the CPU of transmitting the frame.

If software needs to transmit a frame but the current TX queue is full, software enables the interrupt. After the TX queue is empty, an interrupt is generated to instruct software to transmit the waiting frame. Software uses the interrupt to send a group of frames at a time and then releases the buffers for storing the previously transmitted group of frames when the interrupt is valid.

3. Transmitting a frame in query mode

   Software queries the count of the TX frames. If the count is less than the configured depth of TX queue, it notifies the ETH module of the to-be transmitted frame directly. At the same time, it creates a corresponding TX frame index table whose content is the header address of the frame that is written to the TX queue of the Ethernet MAC. After transmitting a frame, the ETH module notifies the CPU of releasing the corresponding TX buffer through the address of the TX queue. After that, the CPU queries the corresponding TX buffer through the address of the TX queue and releases the buffer.

5.4.3 Interrupt Management

Interrupt Status Register

This register indicates the generated interrupt type. For details, see GLB_IRQ_STAT in section 5.6.3 "Description of the Global Control Registers."

Interrupt Enable Register

This register controls whether to generate the related interrupts. For details, see GLB_IRQ_ENA in section 5.6.3 "Description of the Global Control Registers." If an interrupt is enabled, the interrupt status is written to the related interrupt status register.

Raw Interrupt Status Register

This register can read the raw interrupt of a type and transmit it to the CPU. For details, see GLB_IRQ_RAW in section 5.6.3 "Description of the Global Control Registers." To clear the interrupt status, the raw interrupt of the interrupt must be cleared. After the raw interrupt is cleared, the interrupt status is cleared automatically.

5.4.4 Traffic Control

When the number of frames received at a certain interval exceeds the upper limit configured by software, the subsequently received frames are selectively discarded. Through the configuration of UD_GLB_FC_DROPCTRL, the broadcast frames, multicast frames, or unicast frames are discarded if the traffic limit is exceeded. The traffic limit is configured through UD_GLB_FC_RXLIMIT.

Software configures the time interval of traffic restriction through UD_GLB_FC_TIMECTRL. For a 10-bit time interval register, the time slot can be set to up to 1,023. A 17-bit counter is used for counting the time slots of the main clock. The default count is 100,000. For a 100-MHz main clock, the time slot is 1 ms. Software can configure the upper traffic limit of a 20-bit register. If the traffic limit is set to 0, it indicates that traffic is not limited.

5.4.5 Typical Application

Clock Gating

NOTE
When the ETH module is not used, its clocks can be disabled to reduce the power consumption.

To disable the ETH clocks, perform the following steps:

Step 1 Disable the link status of the ETH interface so that the ETH module cannot transmit or RX packets.

Step 2 Clear the RX queues of ETH interface so that the ETH module cannot report the packet RX interrupt.

Step 3 Software delivers a logic command to reset the ETH module and holds the reset status.

Step 4 Set PERI_CRG51 [eth_cken] to 0 to disable the ETH clocks.

----End

To enable the ETH clocks, perform the following steps:

Step 5 Hold the reset status. Set PERI_CRG51 [eth_cken] to 1 to enable the ETH clocks.

Step 6 Set PERI_CRG51 [hrst_eth_s] to 0 to clear the reset status.

Step 7 Enable the link status of the ETH interface to ensure that the ETH module works properly.

----End

Soft Reset

To perform global soft reset on the ETH module, perform the following steps:

Step 1 Disable the link status of the ETH interface and the packet RX interrupt so that software cannot receive or transmit packets.

Step 2 After processing the current received and transmitted packets on the ETH interface, software clears the RX and TX queues and keeps the queue length the same as the value before soft reset. That is, the count values of the related pointers and queues return to 0.

Step 3 Set PERI_CRG51 [hrst_eth_s] to 1 to deliver the soft reset command for the ETH module.

Step 4 Set PERI_CRG51 [hrst_eth_s] to 0 to clear the soft reset on the ETH module.

Step 5 If packets need to be transmitted and received again, software also needs to initialize the RX and TX queues of the ETH interface.

Step 6 Enable the link status of the ETH interface to ensure that the ETH module works properly.

----End

Initialization

To initialize the ETH interface, perform the following steps:

Step 1 Configure the mode for obtaining the interface status.

The status of the ETH interface can be that of the PHY chip by means of auto-adaption or can be configured by the software. During initialization, select the mode for obtaining the interface status by configuring UD_MAC_PORTSEL[stat_ctrl]:

- If UD_MAC_PORTSEL[stat_ctrl] is set to 1, it indicates that the status of the ETH interface is configured by the software. In this case, go to Step 2.
- If UD_MAC_PORTSEL[stat_ctrl] is set to 0, it indicates that the status of the ETH interface is that of the PHY chip by means of auto-adaption. In this case, go to Step 3.

During reset, software configures the working status of the ETH interface.

Step 2 Configure the working status of the PHY chip.

- If UD_MAC_PORTSEL is set to 1, software needs to configure the rate, connection status, and duplex status in UD_MAC_PORTSET according to the actual application environment, and configures the information to the related registers of the PHY chip.
- The ETH module provides a MDIO interface to implement the read/write control for the PHY chip. During software operation, the MDIO interface writes the address of the PHY chip, the address of the register, and related control information to the MDIO_RWCTRL register. When MDIO_RWCTRL[finish] is 1, it indicates the read/write operation on the PHY chip has been finished by hardware. For details about configuration information, see the data sheet related to the PHY chip.

After the configuration is complete, go to Step 4.

Step 3 Configure the working status in auto-adaption mode.

If UD_MAC_PORTSEL[stat_ctrl] is set to 0, you must specify the rate of the PHY chip, duplex mode, address of the connection register, and offset addresses of the registers of such status bits. The information is configured through UD_MDIO_ANEG_CTRL.

Step 4 Set the depth of RX and TX queues.

Set the RX queue depth and TX queue depth in the register UD_GLB_QLEN_SET:

- The RX queue depth indicates the maximum number of buffered frames when data is received.
- The TX queue depth indicates the maximum number of buffered frames when data is transmitted.

The RX and TX queues share 64 management spaces, so the sum of the RX queue depth and the TX queue depth cannot exceed 64. Additionally, either the RX queue depth or the TX queue depth must be more than or equal to 1. If the sum exceeds 64, the depth of the RX queue remains unchanged and the depth of the TX queue is changed to 64 minus the depth of the RX queue.

Software can set the multi-packet interrupt configuration register. By configuring the register UD_GLB_IRQN_SET[int_frm_cnt], software controls how many packets need to be received before a multi-packet interrupt is reported. In addition, software can set the aging time register UD_GLB_IRQN_SET[int_timer].

Step 5 Initialize the buffer of the RX frame queue.

After the reset, software needs to apply for a certain number of buffers that is equal to the configured depth of RX queues. The size of each buffer is 2 KB. Then, software writes the header addresses of the buffers to the RX queue. The number of times of the write operation must be equal to the configured depth of RX queues.

Step 6 Execute the soft reset on the ETH module.

Through the soft reset, the logic circuits and frame management queues inside the ETH module are reset, so that the ETH module returns to the initial status. However, the registers inside the ETH module keep the original values. After clearing the reset, software re-applies for a packet RX buffer and initializes the RX queue. Otherwise, the ETH module cannot receive network packets.

NOTE

After the soft reset of the ETH module, the registers configured by software remain unchanged. For details about these registers, see the register description.

----End

Process of Receiving a Frame in Interrupt Mode

To receive a frame in interrupt mode, perform the following steps:

Step 1 Mask the Ethernet interrupt after entering the interrupt handling program.

Step 2 View the interrupt status bit GLB_IRQ_STAT[int_rx_up] to check whether a frame RX interrupt occurs. If a frame RX interrupt occurs, go to Step 2. Otherwise, continue to process other Ethernet interrupts.

Step 3 Read the frame descriptor UD_GLB_IQFRM_DES. Read the frame data of the related length (fd_in_len) according to the header address of the frame that corresponds to fd_in_addr.

Step 4 Return the raw interrupt signal bit GLB_IRQ_RAW[iraw_rx_up] of the single-packet interrupt to 0 and notify hardware of the completion of packet receiving.

Step 5 According to the number of the remaining available addresses maintained by itself, software determines whether to configure a new address for packet receiving. If a new address for packet receiving does not need to be configured, go to Step 7. Receiving a packet is complete.

Step 6 Read UD_GLB_QSTAT[cpu_addr_in_rdy] to check whether a new address for packet receiving can be configured. If a new address for packet receiving cannot be configured, return to Step 4.

Step 7 Software allocates a new buffer address to the RX queue through the register UD_GLB_IQ_ADDR. Return to Step 4.

Step 8 Read and check the raw interrupt signal bit GLB_IRQ_RAW[iraw_rx_up] of the single-packet interrupt. If the bit is valid and software can continue to receive packets (the upper limit of received packets is not exceeded), return to Step 2.

Step 9 Unmask the Ethernet interrupt.

----End

Process of Receiving a Frame in Query Mode

If the frame RX interrupt GLB_IRQ_ENA[ien_cpu_rx] is disabled, the CPU automatically queries the raw interrupt signal bit GLB_IRQ_RAW[iraw_rx_up] of the single-packet interrupt. If the bit is set to 1, it indicates that a frame needs to be received.

Receive a frame in query mode as follows:

Step 1 Read the raw interrupt signal bit GLB_IRQ_RAW[iraw_rx_up] of the single-packet interrupt. If this bit is invalid, the process ends.

Step 2 Read the frame descriptor UD_GLB_IQFRM_DES. Read the frame data of the related length (fd_in_len) according to the header address of the frame that corresponds to fd_in_addr.

Step 3 Write 1 to clear the raw interrupt signal bit GLB_IRQ_RAW[iraw_rx_up] of the single-packet interrupt and notify hardware of the completion of packet receiving.

Step 4 Read UD_GLB_QSTAT[cpu_addr_in_rdy] to check whether a new address for packet receiving can be configured. If a new address for packet receiving cannot be configured, the process ends.

Step 5 Software allocates a new buffer address to the RX queue through the register UD_GLB_IQ_ADDR.

----End

Process of Transmitting a Frame

Transmit a frame as follows:

Step 1 Read UD_GLB_ADDRQ_STAT[eq_in_rdy] and check whether the TX queue of the ETH module has free space for receiving new TX frames. If the TX queue of the ETH module has no free space, continue to wait and query for a free space.

Step 2 Configure the header address UD_GLB_EQ_ADDR of the frame to be transmitted.

Step 3 Configure the length UD_GLB_EQFRM_LEN of the frame to be transmitted. The configuration for transmitting a frame is complete.

----End

5.5 Register Summary

MDIO Control Registers

Table 5-7 describes the MDIO control registers.

Table 5-5 Summary of the MDIO control registers (base address: 0x1009_0000)

Offset Address	Name	Description	Page
0x1100	MDIO_RWCTRL	MDIO command word register	5-21
0x1104	MDIO_RO_DATA	MDIO read data register	5-23
0x0108	UD_MDIO_PHYADDR	PHY physical address register	5-23
0x010C	UD_MDIO_RO_STAT	PHY chip status register	5-23
0x0110	UD_MDIO_ANEG_CTRL	Offset address configuration register for the PHY chip status	5-24
0x0114	UD_MDIO_IRQENA	Scan mask register for MDIO status changes	5-25

MAC Control Registers

Table 5-8 describes the MAC control registers.

Table 5-6 Summary of the MAC controller registers (base address: 0x1009_0000)

Offset Address	Name	Description	Page
0x0200	UD_MAC_PORTSEL	Port working status control register	5-26
0x0204	UD_MAC_RO_STAT	Port status register	5-27
0x0208	UD_MAC_PORTSET	Port working status configuration register	5-27
0x020C	UD_MAC_STAT_CHANGE	Port status change indicator register for the MAC	5-28
0x0210	UD_MAC_SET	MAC function configuration register	5-29
0x0480	UD_MAC_EEE_INT	Energy efficient Ethernet (EEE) raw interrupt register	5-31
0x0484	UD_MAC_EEE_INTEN	EEE interrupt enable register	5-31
0x0488	UD_MAC_EEE_ENA	EEE enable register	5-32
0x048C	UD_MAC_EEE_TIMER	Timer register required for the EEE function	5-33
0x0490	UD_MAC_EEE_LINK_STATUS	ETH port link status register dedicated for the EEE function	5-33
0x0494	UD_MAC_EEE_CLK_CNT	EEE clock unit counter register	5-34

Global Control Registers

Table 5-9 describes the Ethernet global control registers.

Table 5-7 Summary of the global control registers (base address: 0x1009_0000)

Offset Address	Name	Description	Page
0x1300	GLB_HOSTMAC_L32	Lower 32-bit register for the local MAC address	5-34

Offset Address	Name	Description	Page
0x1304	GLB_HOSTMAC_H16	Upper 16-bit register for the local MAC address	5-35
0x1308	GLB_SOFT_RESET	Internal soft reset register	5-35
0x1310	GLB_FWCTRL	Forward control register	5-36
0x1314	GLB_MACTCTRL	MAC filter table control register	5-36
0x1318	GLB_ENDIAN_MOD	Endian control register	5-37
0x1330	GLB_IRQ_STAT	Interrupt status register	5-38
0x1334	GLB_IRQ_ENA	Interrupt enable register	5-40
0x1338	GLB_IRQ_RAW	Raw interrupt register	5-42
0x1400	GLB_MAC0_L32	MAC filter 0	5-43
0x1404	GLB_MAC0_H16	MAC filter 0	5-43
0x1408	GLB_MAC1_L32	MAC filter 1	5-44
0x140C	GLB_MAC1_H16	MAC filter 1	5-44
0x1410	GLB_MAC2_L32	MAC filter 2	5-45
0x1414	GLB_MAC2_H16	MAC filter 2	5-45
0x1418	GLB_MAC3_L32	MAC filter 3	5-46
0x141C	GLB_MAC3_H16	MAC filter 3	5-46
0x1420	GLB_MAC4_L32	MAC filter 4	5-47
0x1424	GLB_MAC4_H16	MAC filter 4	5-48
0x1428	GLB_MAC5_L32	MAC filter 5	5-48
0x142C	GLB_MAC5_H16	MAC filter 5	5-49
0x1430	GLB_MAC6_L32	MAC filter 6	5-49
0x1434	GLB_MAC6_H16	MAC filter 6	5-50
0x1438	GLB_MAC7_L32	MAC filter 7	5-50
0x143C	GLB_MAC7_H16	MAC filter 7	5-51
0x0340	UD_GLB_IRQN_SET	Multi-packet interrupt configuration register	5-51
0x0344	UD_GLB_QLEN_SET	Queue length configuration register	5-52
0x0348	UD_GLB_FC_LEVEL	Traffic control register	5-53

Offset Address	Name	Description	Page
0x034C	UD_GLB_CAUSE	Cause register for the CPU to which the packet is transmitted	5-53
0x0350	UD_GLB_RXFRM_SADDR	RX frame start address register	5-54
0x0354	UD_GLB_IQFRM_DES	RX frame descriptor register	5-54
0x0358	UD_GLB_IQ_ADDR	RX frame header address register	5-55
0x035C	UD_GLB_BFC_STAT	Counter for traffic control status of forward buffer and aging time of multi-packet interrupt	5-56
0x0360	UD_GLB_EQ_ADDR	TX queue header address register	5-56
0x0364	UD_GLB_EQFRM_LEN	TX queue frame length configuration register	5-57
0x0368	UD_GLB_QSTAT	Queue status register	5-57
0x036C	UD_GLB_ADDRQ_STAT	Address queue status register	5-58
0x0370	UD_GLB_FC_TIMECTRL	Traffic control time configuration register	5-59
0x0374	UD_GLB_FC_RXLIMIT	Traffic control limit configuration register	5-59
0x0378	UD_GLB_FC_DROPCTRL	Packet drop control register for traffic control	5-60

Statistics Counter Control Registers

Table 5-10 describes the statistics counter control registers.

Table 5-8 Summary of the statistics counter control registers (base address: 0x1009_0000)

Offset Address	Name	Description	Page
0x0584	UD_STS_PORTCNT	Port status counter	5-61
0x05A0	UD_PORT2CPU_PKTS	Register for the total number of packets received by the CPU from the uplink or downlink port	5-61

Offset Address	Name	Description	Page
0x05A4	UD_CPU2IQ_ADDRCNT	Register for the count of configuring packet receiving address queue by the CPU	5-62
0x05A8	UD_RX_IRQCNT	Register for the count of reporting single-packet interrupt by the uplink or downlink port	5-62
0x05AC	UD_CPU2EQ_PKTS	Register for the total number of packets transmitted by the CPU to the uplink or downlink port	5-63

Statistics Result Registers

Table 5-11 describes the statistics result registers.

Table 5-9 Summary of the statistics result registers (base address: 0x1009_0000)

Offset Address	Name	Description	Page
0x0600	UD_RX_DVCNT	RXDV rising edge count register	5-63
0x0604	UD_RX_OCTS	Register for the total number of received bytes	5-63
0x0608	UD_RX_RIGHTOCTS	Register for the total number of bytes of received correct packets	5-64
0x060C	UD_HOSTMAC_PKTS	Register for the number of packets matching the local MAC address	5-64
0x0610	UD_RX_RIGHTPKTS	Register for the total number of packets received by the port	5-65
0x0614	UD_RX_BROADPKTS	Register for the number of correct broadcast packets	5-65
0x0618	UD_RX_MULTPKTS	Register for the number of correct multicast packets	5-65
0x061C	UD_RX_UNIPKTS	Register for the number of correct unicast packets	5-66
0x0620	UD_RX_ERRPKTS	Register for the total number of incorrect packets	5-66
0x0624	UD_RX_CRCERR_PKTS	Register for the count of CRC errors	5-67

Offset Address	Name	Description	Page
0x0628	UD_RX_LENERR_PKTS	Register for the number of packets with invalid length	5-67
0x062C	UD_RX_OCRCERR_PKTS	Register for the number of packets with odd nibbles and CRC errors	5-67
0x0630	UD_RX_PAUSE_PKTS	Register for the number of received pause packets	5-68
0x0634	UD_RF_OVERCNT	Register for the count of RXFIFO overflow events	5-68
0x0638	UD_FLUX_TOL_IPKTS	Register for the total number of received packets allowed by the traffic limit	5-69
0x063C	UD_FLUX_TOL_DPKTS	Register for the total number of packets discarded due to traffic limit	5-69
0x064C	UD_MN2CPU_PKTS	Register for the number of packets not forwarded to the CPU port due to MAC limit	5-70
0x0780	UD_TX_PKTS	Register for the total number of packets transmitted successfully	5-71
0x0784	UD_TX_BROADPKTS	Register for the number of broadcast packets transmitted successfully	5-71
0x0788	UD_TX_MULTPKTS	Register for the number of multicast packets transmitted successfully	5-72
0x078C	UD_TX_UNIPKTS	Register for the number of unicast packets transmitted successfully	5-72
0x0790	UD_TX_OCTS	Register for the total number of transmitted bytes	5-72
0x0794	UD_TX_PAUSE_PKTS	Register for the number of transmitted pause frames	5-73
0x0798	UD_TX_RETRYCNT	Register for the total count of retransmission	5-73
0x079C	UD_TX_COLCNT	Register for the total count of collisions	5-73
0x07A0	UD_TX_LC_PKTS	Register for the number of packets with late collision	5-74

Offset Address	Name	Description	Page
0x07A4	UD_TX_COLOK_PKTS	Register for the number of packets transmitted successfully with collisions	5-74
0x07A8	UD_TX_RETRY15_PKTS	Register for the number of packets discarded due to more than 15 times of retransmission	5-74
0x07AC	UD_TX_RETRYN_PKTS	Register for the number of packets with the count of collisions being equal to the threshold	5-75

5.6 Register Description

5.6.1 Description of the MDIO Control Registers

MDIO_RWCTRL

MDIO_RWCTRL is an MDIO command word register.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x1100	MDIO_RWCTRL	0x0000_8000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																finish	reserved	rw		phy_exaddr				frq_dv				phy_inaddr			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	cpu_data_in	Data used by the MDIO module to perform write operation on the PHY chip. During write operation, the CPU first writes the 16-bit data to be written to the MDIO to this register.
[15]	RW	finish	PHY read/write operation complete. 0: Not complete. 1: Complete. When the read/write operation is required for the second time, the CPU must clear this bit first.
[14]	RO	reserved	Reserved.

[13]	RW	rw	PHY read or write access control. 0: Read operation. 1: Write operation.
[12:8]	RW	phy_exaddr	Physical address of the external PHY chip. One MDIO can perform read/write operation on multiple external PHY chips. Each PHY chip has one corresponding address. When the MDIO connects to only one external PHY chip, this bit is equivalent to UD_MDIO_PHYADDR[phy0_addr] or UD_MDIO_PHYADDR[phy1_addr].
[7:5]	RW	frq_dv	Frequency division factor for the MDC (the MDIO interface clock) when the MDIO performs the read/write operation on external PHY chips. Take the frequency 100 MHz of the main clock as an example to describe the matching relations between frq_dv and MDC frequency. 000: The frequency of the working main clock is divided by 50 and the obtained frequency is 2 MHz. 001: The frequency of the working main clock is divided by 100 and the obtained frequency is 1 MHz. 010: The frequency of the working main clock is divided by 200 and the obtained frequency is 512 kHz. 011: The frequency of the working main clock is divided by 400 and the obtained frequency is 256 kHz. 100: The frequency of the working main clock is divided by 800 and the obtained frequency is 128 kHz. 101: The frequency of the working main clock is divided by 1600 and the obtained frequency is 64 kHz. 110: The frequency of the working main clock is divided by 3200 and the obtained frequency is 32 kHz. 111: The frequency of the working main clock is divided by 6400 and the obtained frequency is 16 kHz.
[4:0]	RW	phy_inaddr	Internal register address of the external PHY chip. This address is presented by a 5-bit binary number.

MDIO_RO_DATA

MDIO_RO_DATAMDIO is a read data register. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x1104	MDIO_RO_DATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																cpu_data_out															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RO	cpu_data_out	Data register used by the MDIO module to perform read operation on the PHY chip. The MDIO module first writes the 16-bit data read from the PHY chip to this register.

UD_MDIO_PHYADDR

UD_MDIO_PHYADDR is a PHY physical address register. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0108	UD_MDIO_PHYADDR	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												phy_addr			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved.
[4:0]	RW	phy_addr	Physical address of the external PHY chip.

UD_MDIO_RO_STAT

UD_MDIO_RO_STAT is a PHY status register. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x010C	UD_MDIO_RO_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													speed_mdio2mac	link_mdio2mac	duplex_mdio2mac
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.

[2]	RO	speed_mdio2mac	Port speed working status obtained from the MDIO interface, which is in either 10 Mbit/s or 100 Mbit/s working mode. 0: 10 Mbit/s mode 1: 100 Mbit/s mode
[1]	RO	link_mdio2mac	Port link status obtained from the MDIO interface. 0: No link exists. 1: A link exists.
[0]	RO	duplex_mdio2mac	Port duplex working status obtained from the MDIO interface. 0: half-duplex 1: full-duplex

UD_MDIO_ANEG_CTRL

UD_MDIO_ANEG_CTRLPHY is a offset address configuration register for the PHY status. The register does not support soft reset.

NOTE

The PHY speed status is indicated by bit[14] of the register with the address of 17, internal_addr_speed is set to 0x11 and speed_index is set to 0xE. In this case, the ETH module reads the bit value as the current working speed mode of the PHY through the MDIO interface.

Offset Address	Register Name	Total Reset Value
0x0110	UD_MDIO_ANEG_CTRL	0x0463_1EA9

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	internal_addr_speed	internal_addr_link	internal_addr_duplex		speed_index	link_index	duplex_index
Reset	0 0 0 0	0 1 0 0	0 1 1 0	0 0 1 1	0 0 0 1	1 1 1 0	1 0 1 0	1 0 0 1

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:22]	RW	internal_addr_speed	Address of the register in the PHY chip to store the status information (speed). The default value is set according to Intel 9785.
[21:17]	RW	internal_addr_link	Address of the register in the PHY chip to store the status information (link). The default value is set according to Intel 9785.
[16:12]	RW	internal_addr_duplex	Address of the register in the PHY chip to store the status information (duplex). The default value is set according to Intel 9785.
[11:8]	RW	speed_index	Offset address in the PHY status register that is used to store the speed information. The default value is set according to Intel 9785.

[7:4]	RW	link_index	Offset address in the PHY status register that is used to store the link information. The default value is set according to Intel 9785.
[3:0]	RW	duplex_index	Offset address in the PHY status register that is used to store the duplex information. The default value is set according to Intel 9785.

UD_MDIO_IRQENA

UD_MDIO_IRQENA is a scan mask register for MDIO status changes. The register does not support soft reset.

NOTE

- If the status information about the PHY chip connecting to the port cannot be scanned and obtained by configuring UD_MDIO_ANEG_CTRL, you can scan the PHY status register by using MDIO_RWCTRL to check whether the port status changes and generate an interrupt to notify software of processing the interrupt.
- link_partner status change refers to the change of any bit of link, speed, and duplex for the PHY status.

Offset Address	Register Name	Total Reset Value
0x0114	UD_MDIO_IRQENA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												link_partner_ch_mask	speed_ch_mask	link_ch_mask	duplex_ch_mask
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.
[3]	RW	link_partner_ch_mask	Port link partner status scan change interrupt mask. 0: mask 1: unmask
[2]	RW	speed_ch_mask	Port speed mode scan change interrupt mask. 0: mask 1: unmask
[1]	RW	link_ch_mask	Port link mode scan change interrupt mask. 0: mask 1: unmask

[0]	RW	duplex_ch_mask	Port duplex mode scan change interrupt mask. 0: mask 1: unmask

5.6.2 Description of the MAC Control Registers

MAC control registers are registers for port control. When the port status is valid, after configuring MAC control registers, you need to perform one soft reset on them.

UD_MAC_PORTSEL

UD_MAC_PORTSEL is a port working status control register. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0200	UD_MAC_PORTSEL	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														mii_rmii	stat_ctrl
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1]	RW	mii_rmii	Port interface mode selection. 0: MII interface 1: RMII interface
[0]	RW	stat_ctrl	Port working status information select control register. 0: Use the status information obtained from the MDIO interface. 1: Use the status information set by the CPU.

UD_MAC_RO_STAT

UD_MAC_RO_STAT is a port status register. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0204	UD_MAC_RO_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	reserved	peed_stat	link_stat	duplex_stat
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0			

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2]	RO	speed_stat	Port current speed mode. 0: 10 Mbit/s mode 1: 100 Mbit/s mode
[1]	RO	link_stat	Port current link status. 0: No link exists. 1: A link exists.
[0]	RO	duplex_stat	Port current duplex status. 0: half-duplex 1: full-duplex

UD_MAC_PORTSET

UD_MAC_PORTSET is a port working status configuration register. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0208	UD_MAC_PORTSET	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							speed_stat_dio link_stat_dio duplex_stat_dio
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2]	RW	speed_stat_dio	Port speed mode set by the CPU. 0: 10 Mbit/s mode 1: 100 Mbit/s mode

[1]	RW	link_stat_dio	Port link status set by the CPU. 0: No link exists. 1: A link exists.
[0]	RW	duplex_stat_dio	Port duplex mode set by the CPU. 0: half-duplex 1: full-duplex

UD_MAC_STAT_CHANGE

UD_MAC_STAT_CHANGE is a port status change indicator register. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x020C	UD_MAC_STAT_CHANGE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													speed_stat_ch	link_stat_ch	duplex_stat_ch
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2]	WC	speed_stat_ch	Port speed mode change indicator. 0: No change occurs. 1: A change occurs. Writing 1 clears this register.
[1]	WC	link_stat_ch	Port link status change indicator. 0: No change occurs. 1: A change occurs. Writing 1 clears this register.
[0]	WC	duplex_stat_ch	Port duplex mode change indicator. 0: No change occurs. 1: A change occurs. Writing 1 clears this register.

UD_MAC_SET

UD_MAC_SET is a MAC function configuration register.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0210	UD_MAC_SET	0x2027_55EE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		add_pad_en	crcgen_dis	cntr_rdclr_en	cntr_clr_all	cntr_roll_dis	colthreshold				in_loop_en	ex_loop_en	pause_en	rx_shframe_en	rx_min_thr					len_max											
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	1	1	1	0	1	0	1	0	1	0	1	1	1	1	0	1	1	1	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29]	RW	add_pad_en	Port auto add PAD enable during transmission. 0: disabled 1: enabled
[28]	RW	crcgen_dis	Port CRC generation disable control. 0: TX frame recalculate CRC. 1: TX frame not recalculate CRC.
[27]	RW	cntr_rdclr_en	Port statistics counter read clear enable. 0: disabled 1: enabled
[26]	RW	cntr_clr_all	Port statistics counter clear control. 0: not clear 1: clear **Note:** If cntr_clr_all is set to 1, the next clear all operation can be performed only after this bit is set to 0 and then to 1.
[25]	RW	cntr_roll_dis	Port statistics acyclic counter enable. 0: disabled 1: enabled
[24:21]	RW	colthreshold	Port collision count statistics threshold. The default value is 0x1, which indicates the count of frames with one collision.

[20]	RW	in_loop_en	Port loopback to internal enable. 0: disabled 1: enabled **Note:** Loopback to internal enable and loopback to external enable cannot be configured at the same time. When the network interface is in normal state, you need to perform soft reset on the module after loopback to internal enable is configured instead of loopback to external enable and vice versa.
[19]	RW	ex_loop_en	Port loopback to external enable. 0: disabled 1: enabled **Note:** Loopback to internal enable and loopback to external enable cannot be configured at the same time. When the network interface is in normal state, you need to perform soft reset on the module after loopback to internal enable is configured instead of loopback to external enable and vice versa.
[18]	RW	pause_en	Port pause frame TX enable. 0: disabled 1: enabled
[17]	RW	rx_shframe_en	Port short frame RX enable. 0: disabled 1: enabled **Note:** If rx_shframe_en is set to 1, the minimum RX frame length allowed by the port is that set by rx_min_thr. If rx_shframe_en is set to 0, the minimum RX frame length allowed by the port is 64 bytes (including CRC) by default.
[16:11]	RW	rx_min_thr	Minimum RX frame length allowed by the port. The value range is from 42 bytes to 63 bytes. The default value is 42 bytes. **Note:** If rx_min_thr is set to a value smaller than 42, 42 is used instead of the value.
[10:0]	RW	len_max	Maximum RX frame length allowed by the port. The default value is 1518 bytes. The value is in a range of 1518 bytes to 1535 bytes. **Note:** If len_max is set to a value greater than 2000, 2000 is used instead of the value. If len_max is set to a value smaller than 256, 256 is used instead of the value.

UD_MAC_EEE_INT

UD_MAC_EEE_INT is an EEE raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x0480	UD_MAC_EEE_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											tx_entry_start	rx_leave_lpi	rx_entry_lpi	tx_leave_lpi	tx_entry_lpi
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved.
[4]	RO	tx_entry_start	Raw interrupt that allows the PHY to enter the low-power idle (LPI) state in the ETH TX direction.
[3]	RO	rx_leave_lpi	Raw interrupt that allows the PHY to exit the LPI state in the RX direction.
[2]	RO	rx_entry_lpi	Raw interrupt that allows the PHY to enter the LPI state in the RX direction.
[1]	RO	tx_leave_lpi	Raw interrupt that allows the PHY to exit the LPI state in the TX direction.
[0]	RO	tx_entry_lpi	Raw interrupt that allows the PHY to enter the LPI state in the TX direction.

UD_MAC_EEE_INTEN

UD_MAC_EEE_INTEN is an EEE interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x0484	UD_MAC_EEE_INTEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						tx_entry_start_msk	rx_leave_lpi_msk	rx_entry_lpi_msk	tx_leave_lpi_msk	tx_entry_lpi_msk	tx_entry_start_en	rx_leave_lpi_en	rx_entry_lpi_en	tx_leave_lpi_en	tx_entry_lpi_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved.
[9]	RW	tx_entry_start_msk	Mask of the raw interrupt that allows the PHY to enter the LPI state in the ETH TX direction.
[8]	RW	rx_leave_lpi_msk	Mask of the raw interrupt that allows the PHY to exit the LPI state in the RX direction.
[7]	RW	rx_entry_lpi_msk	Mask of the raw interrupt that allows the PHY to enter the LPI state in the RX direction.
[6]	RW	tx_leave_lpi_msk	Mask of the raw interrupt that allows the PHY to exit the LPI state in the TX direction.
[5]	RW	tx_entry_lpi_msk	Mask of the raw interrupt that allows the PHY to enter the LPI state in the TX direction.
[4]	RO	tx_entry_start_en	Enable for the raw interrupt that allows the PHY to enter the LPI state in the ETH TX direction.
[3]	RO	rx_leave_lpi_en	Enable for the raw interrupt that allows the PHY to exit the LPI state in the RX direction.
[2]	RO	rx_entry_lpi_en	Enable for the raw interrupt that allows the PHY to enter the LPI state in the RX direction.
[1]	RO	tx_leave_lpi_en	Enable for the raw interrupt that allows the PHY to exit the LPI state in the TX direction.
[0]	RO	tx_entry_lpi_en	Enable for the raw interrupt that allows the PHY to enter the LPI state in the TX direction.

UD_MAC_EEE_ENA

UD_MAC_EEE_ENA is an EEE enable register.

Offset Address	Register Name	Total Reset Value
0x0000	UD_MAC_EEE_ENA	0x00F4_2400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	eee_ls_timer																												reserved		eee_assert	eee_enable
Reset	0	0	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RW	eee_ls_timer	LS timer.
[3:2]	RW	reserved	Reserved.
[1]	RW	eee_assert	EEE LPI state enable.
[0]	RW	eee_enable	EEE enable.

UD_MAC_EEE_TIMER

UD_MAC_EEE_TIMER is a timer register required for the EEE function.

Offset Address	Register Name	Total Reset Value
0x048C	UD_MAC_EEE_TIMER	0x001E_2710

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_wk_timer																lpi_cond_timer															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	tx_wk_timer	TX_WK_TIMER.
[15:0]	RW	lpi_cond_timer	LPI_COND_TIMER.

UD_MAC_EEE_LINK_STATUS

UD_MAC_EEE_LINK_STATUS an ETH port link status register dedicated for the EEE function.

Offset Address	Register Name	Total Reset Value
0x0490	UD_MAC_EEE_LINK_STATUS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								phy_link_status
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RW	reserved	Reserved.
[0]	RW	phy_link_status	PHY link status.

UD_MAC_EEE_CLK_CNT

UD_MAC_EEE_CLK_CNT is an EEE clock unit counter register.

Offset Address	Register Name	Total Reset Value
0x0494	UD_MAC_EEE_CLK_CNT	0x0000_0063

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	eee_clk_cnt								
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1 1 0	0 0 1	1

Bits	Access	Name	Description
[31:0]	RW	eee_clk_cnt	EEE clock unit counter.

5.6.3 Description of the Global Control Registers

GLB_HOSTMAC_L32

GLB_HOSTMAC_L32 is a lower 32-bit register for the local MAC address.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x1300	GLB_HOSTMAC_L32	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	local_mac							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	local_mac	Lower 32 bits of the local MAC address.

GLB_HOSTMAC_H16

GLB_HOSTMAC_H16 is an upper 16-bit register for the local MAC address.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x1304	GLB_HOSTMAC_H16	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				local_mac[47:32]			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	local_mac[47:32]	Upper 16 bits of the local MAC address.

GLB_SOFT_RESET

GLB_SOFT_RESET is an internal soft reset register.

The register does not support soft reset.

NOTE

The time for each soft reset must remain for more than 2 ms.

Offset Address	Register Name	Total Reset Value
0x1308	GLB_SOFT_RESET	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								soft_reset
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description

[31:1]	RO	reserved	Reserved.
[0]	RW	soft_reset	Internal soft reset. 0: Not reset. 1: Reset. In soft reset state, this bit must be set to 0to clear soft reset.

GLB_FWCTRL

GLB_FWCTRL is a forward control register.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x1310	GLB_FWCTRL	0x0000_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								fwall2cpu_up	reserved	fw2cpu_ena_up	reserved				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7]	RW	fwall2cpu_up	Indicates whether to forcibly forward all valid input frames to the CPU port. 0: no 0: yes
[6]	RO	reserved	Reserved.
[5]	RW	fw2cpu_ena_up	Function enable of forwarding the input frames to the CPU port. 0: disabled 1: enabled
[4:0]	RO	reserved	Reserved.

GLB_MACTCTRL

GLB_MACTCTRL is a MAC filter table control register.

The register does not support soft reset.

NOTE

- If the highest byte of the destination MAC address is even, the frame is a unicast frame.
- If the highest byte of the destination MAC address is odd, the frame is a multicast frame.
- If all bytes of the destination MAC address are 0xFF, the frame is a broadcast frame.

Offset Address	Register Name	Total Reset Value
0x1314	GLB_MACTCTRL	0x0000_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								mact_ena_up	reserved	broad2cpu_up	reserved	multi2cpu_up	reserved	uni2cpu_up	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7]	RW	mact_ena_up	Enable bit of all MAC filters of the port. 0: disabled (no MAC filter is used) 1: enabled (MAC filters are used)
[6]	RO	reserved	Reserved.
[5]	RW	broad2cpu_up	Indicates whether to forward the input broadcast frames to the CPU port. 0: no 1: yes
[4]	RO	reserved	Reserved.
[3]	RW	multi2cpu_up	Indicates whether to forward the input multicast frames that are not listed in the filter table to the CPU port. 0: no 1: yes
[2]	RO	reserved	Reserved.
[1]	RW	uni2cpu_up	Indicates whether to forward the input unicast frames that are not listed in the filter table to the CPU port. 0: no 1: yes
[0]	RO	reserved	Reserved.

GLB_ENDIAN_MOD

GLB_ENDIAN_MOD is an endian control register.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x1318	GLB_ENDIAN_MOD	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														in_edian	out_edian
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1]	RW	in_edian	RX packet write SDRAM endian configuration. 0: big-endian mode 1: little-endian mode Data consists of bytes.
[0]	RW	out_edian	TX packet read SDRAM endian configuration. 0: big-endian mode 1: little-endian mode

GLB_IRQ_STAT

GLB_IRQ_STAT is an interrupt status register.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x1330	GLB_IRQ_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			int_mdio_finish	reserved				int_rxd_up	int_freeq_up	int_stat_up	int_duplex_up	int_speed_up	int_link_up	int_tx_up	int_rx_up
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved.
[12]	RO	int_mdio_finish	Interrupt status indicates whether the MDIO interface completes the operation required by the CPU. 0: Not completed.

			1: Completed and an interrupt is generated. After this interrupt is generated, software determines whether the MDIO completes the operation by querying MDIO_RWCTRL[finish].
[11:8]	RO	reserved	Reserved.
[7]	RO	int_rxd_up	Interrupt status (multi-packet interrupt) for a frame (frames) on the port to be received by the CPU. 0: The interrupt is invalid. 1: The interrupt is valid. There are frames to be received by the CPU in the RX queue. After this interrupt is generated, software determines whether there are frames to be received by querying GLB_IRQ_RAW[iraw_rxd_up].
[6]	RO	int_freeeq_up	Interrupt status indicates that the status of the port output queue is changed from nonempty to empty, that is, the status of the TX queue buffer is changed from nonempty to empty, that is, the status of the TX queue buffer is changed from nonempty to empty. In this case, the CPU can write a group of new frames to be transmitted. 0: No interrupt is generated. 1: An interrupt is generated. After this interrupt is generated, software determines whether the current TX queue is empty by querying UD_GLB_ADDRQ_STAT[eq_cnt]. If the current TX queue is not empty, it indicates that the interrupt is invalid.
[5]	RO	int_stat_up	Interrupt status for port status changes, indicating that an interrupt is generated when the MDIO obtains the speed change, duplex mode change, and link status change of the PHY chip in auto-adaption mode. 0: The interrupt is invalid. 1: The interrupt is valid. The port status changes. After this interrupt is generated, software determines which status changes according to the configuration of UD_MDIO_IRQENA.
[4]	RO	int_duplex_up	Interrupt status for port duplex mode changes. 0: The interrupt is invalid. 1: The interrupt is valid. The duplex mode changes. After this interrupt is generated, software determines whether the duplex mode changes by querying UD_MAC_STAT_CHANGE[duplex_stat_ch].
[3]	RO	int_speed_up	Interrupt status for port speed mode changes. 0: The interrupt is invalid. 1: The interrupt is valid. The speed mode changes. After this interrupt is generated, software determines whether the speed mode changes by querying UD_MAC_STAT_CHANGE[speed_stat_ch].
[2]	RO	int_link_up	Interrupt status for port link status changes.

			0: The interrupt is invalid. 1: The interrupt is valid. The link status changes. After this interrupt is generated, software determines whether the link status changes by querying UD_MAC_STAT_CHANGE[link_stat_ch].
[1]	RO	int_tx_up	Interrupt status for the completion of transmitting a frame from the CPU by the port. 0: Not completed. 1: Completed and an interrupt is generated. After this interrupt is generated, software determines whether to release the buffer of the TX frames by querying the current TX queue address eq_out_index in UD_GLB_QSTAT.
[0]	RO	int_rx_up	Interrupt status for frames on the port to be received by the CPU. 0: The interrupt is invalid. 1: The interrupt is valid. There are frames to be received by the CPU in the RX queue. After this interrupt program is started, software determines whether frames are received by querying the GLB_IRQ_RAW[iraw_rxd_up] signal.

GLB_IRQ_ENA

GLB_IRQ_ENA is an interrupt enable register.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x1334	GLB_IRQ_ENA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												ien_all	ien_up	reserved					ien_mdio_finish	reserved				ien_rxd_up	ien_freeeq_up	ien_stat_up	ien_duplex_up	ien_speed_up	ien_link_up	ien_tx_up	ien_rx_up
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved.
[19]	RW	ien_all	All interrupts enable. 0: disabled (none of the interrupt can be reported) 1: enabled (all interrupts are reported according to the configuration)

[18]	RW	ien_up	All uplink port interrupts enable. 0: disabled (none of the uplink port interrupt can be reported) 1: enabled (all uplink port interrupts are reported according to the configuration)
[17:13]	RO	reserved	Reserved.
[12]	RW	ien_mdio_finish	Indicator enable for the MDIO to complete the operation required by the CPU. 0: disabled 1: enabled
[11:8]	RO	reserved	Reserved.
[7]	RW	ien_rxd_up	Interrupt enable (multi-packet interrupt) for a frame (frames) on the uplink port to be received by the CPU. 0: disabled 1: enabled
[6]	RW	ien_freeeq_up	Interrupt signal enable for the TX queue of the uplink port to change from nonempty to empty. 0: disabled 1: enabled
[5]	RW	ien_stat_up	Interrupt signal enable for uplink port status changes. 0: disabled 1: enabled
[4]	RW	ien_duplex_up	Interrupt enable for uplink port duplex mode changes. 0: disabled 1: enabled
[3]	RW	ien_speed_up	Interrupt enable for uplink port speed mode changes. 0: disabled 1: enabled
[2]	RW	ien_link_up	Interrupt enable for uplink port link status changes. 0: disabled 1: enabled
[1]	RW	ien_tx_up	Indicator enable for the completion of transmitting a frame from the CPU by the uplink port. 0: disabled 1: enabled
[0]	RW	ien_rx_up	Interrupt enable for frames on the uplink port to be received by the CPU. 0: disabled 1: enabled

GLB_IRQ_RAW

GLB_IRQ_RAW is a raw interrupt register. The register does not support soft reset. Writing 1 clears this register.

Offset Address	Register Name	Total Reset Value
0x1338	GLB_IRQ_RAW	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7	6	5	4	3	2	1	0
Name	reserved					iraw_mdio_finish	reserved	iraw_rxd_up	iraw_freeeq_up	iraw_stat_up	iraw_duplex_up	iraw_speed_up	iraw_link_up	iraw_tx_up	iraw_rx_up
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0 0 0 0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved.
[12]	WC	iraw_mdio_finish	Raw interrupt status for the MDIO to complete the operation required by the CPU. 0: No interrupt is generated. 1: An interrupt is generated.
[11:8]	RO	reserved	Reserved.
[7]	WC	iraw_rxd_up	Raw interrupt status (multi-packet interrupt) for a frame (frames) on the uplink port to be received by the CPU. 0: No interrupt is generated. 1: An interrupt is generated.
[6]	WC	iraw_freeeq_up	Raw interrupt status for the TX queue of the uplink port to change from nonempty to empty, indicating that the TX queue buffer changes from nonempty to empty and the CPU can write a group of new frames to be transmitted. 0: No interrupt is generated. 1: An interrupt is generated.
[5]	WC	iraw_stat_up	Raw interrupt status for uplink port status changes, indicating that an interrupt is generated when the MDIO obtains the speed change, duplex mode change, and link status change of the PHY chip in auto-adaption mode. 0: No interrupt is generated. 1: An interrupt is generated.
[4]	WC	iraw_duplex_up	Raw interrupt status for uplink port duplex mode changes. 0: No interrupt is generated. 1: An interrupt is generated.

[3]	WC	iraw_speed_up	Raw interrupt status for uplink port speed mode changes. 0: The interrupt is invalid. 1: The interrupt is valid. The speed mode changes. Writing 1 clears this register.
[2]	WC	iraw_link_up	Raw interrupt status for uplink port link status changes. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	WC	iraw_tx_up	Raw interrupt status for the completion of transmitting a frame from the CPU by the uplink port. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	WC	iraw_rx_up	Raw interrupt status for frames on the uplink port to be received by the CPU. 0: No interrupt is generated. 1: An interrupt is generated.

GLB_MAC0_L32

GLB_MAC0_L32 is a lower 32-bit register for the filter table MAC0.

Offset Address	Register Name	Total Reset Value
0x1400	GLB_MAC0_L32	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flt_mac0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	flt_mac0	Lower 32 bits of the filter table MAC0.

GLB_MAC0_H16

GLB_MAC0_H16 is an upper 16-bit register for the filter table MAC0.

Offset Address	Register Name	Total Reset Value
0x1404	GLB_MAC0_H16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										fw2cpu_up	reserved			mac0_up	reserved	flt_mac0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved.
[21]	RW	fw2cpu_up	Indicates whether to forward the frames received by the uplink port that match this filter to the CPU port when the uplink port enables this filter. 0: no 1: yes
[20:18]	RO	reserved	Reserved.
[17]	RW	mac0_up	Control for setting this filter to be used by the uplink port. 0: The uplink port does not use this filter. 1: The uplink port uses this filter.
[16]	RO	reserved	Reserved.
[15:0]	RW	flt_mac0	Upper 16 bits of the filter table MAC0.

GLB_MAC1_L32

GLB_MAC1_L32 is a lower 32-bit register for the filter table MAC1.

Offset Address	Register Name	Total Reset Value
0x1408	GLB_MAC1_L32	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flt_mac1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	flt_mac1	Lower 32 bits of the filter table MAC1.

GLB_MAC1_H16

GLB_MAC1_H16 is an upper 16-bit register for the filter table MAC1.

Offset Address	Register Name	Total Reset Value
0x140C	GLB_MAC1_H16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										fw2cpu_up	reserved			mac1_up	reserved	flt_mac1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved.
[21]	RW	fw2cpu_up	Indicates whether to forward the frames received by the uplink port that match this filter to the CPU port when the uplink port enables this filter. 0: no 1: yes
[20:18]	RO	reserved	Reserved.
[17]	RW	mac1_up	Control for setting this filter to be used by the uplink port. 0: The uplink port does not use this filter. 1: The uplink port uses this filter.
[16]	RO	reserved	Reserved.
[15:0]	RW	flt_mac1	Upper 16 bits of the filter table MAC1.

GLB_MAC2_L32

GLB_MAC2_L32 is a lower 32-bit register for the filter table MAC2.

Offset Address	Register Name	Total Reset Value
0x1410	GLB_MAC2_L32	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flt_mac2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	flt_mac2	Lower 32 bits of the filter table MAC2.

GLB_MAC2_H16

GLB_MAC2_H16 is an upper 16-bit register for the filter table MAC2.

Offset Address	Register Name	Total Reset Value
0x1414	GLB_MAC2_H16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										fw2cpu_up	reserved			mac2_up	reserved	flt_mac2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved.
[21]	RW	fw2cpu_up	Indicates whether to forward the frames received by the uplink port that match this filter to the CPU port when the uplink port enables this filter. 0: no 1: yes
[20:18]	RO	reserved	Reserved.
[17]	RW	mac2_up	Control for setting this filter to be used by the uplink port. 0: The uplink port does not use this filter. 1: The uplink port uses this filter.
[16]	RO	reserved	Reserved.
[15:0]	RW	flt_mac2	Upper 16 bits of the filter table MAC2.

GLB_MAC3_L32

GLB_MAC3_L32 is a lower 32-bit register for the filter table MAC3.

Offset Address	Register Name	Total Reset Value
0x1418	GLB_MAC3_L32	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flt_mac3																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	flt_mac3	Lower 32 bits of the filter table MAC3.

GLB_MAC3_H16

GLB_MAC3_H16 is an upper 16-bit register for the filter table MAC3.

Offset Address	Register Name	Total Reset Value
0x141C	GLB_MAC3_H16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										fw2cpu_up	reserved			mac3_up	reserved	flt_mac3															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved.
[21]	RW	fw2cpu_up	Indicates whether to forward the frames received by the uplink port that match this filter to the CPU port when the uplink port enables this filter. 0: no 1: yes
[20:18]	RO	reserved	Reserved.
[17]	RW	mac3_up	Indicates whether to forward the frames received by the downlink port that match this filter to the CPU port when the downlink port enables this filter. 0: Do not forward the frames. 1: Forward the frames.
[16]	RO	reserved	Reserved.
[15:0]	RW	flt_mac3	Upper 16 bits of the filter table MAC3.

GLB_MAC4_L32

GLB_MAC4_L32 is a lower 32-bit register for the filter table MAC4.

Offset Address	Register Name	Total Reset Value
0x1420	GLB_MAC4_L32	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flt_mac4																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	flt_mac4	Lower 32 bits of the filter table MAC4.

GLB_MAC4_H16

GLB_MAC4_H16 is an upper 16-bit register for the filter table MAC4.

Offset Address	Register Name	Total Reset Value
0x1424	GLB_MAC4_H16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										fw2cpu_up		reserved				mac4_up		reserved		flt_mac4											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved.
[21]	RW	fw2cpu_up	Indicates whether to forward the frames received by the uplink port that match this filter to the CPU port when the uplink port enables this filter. 0: no 1: yes
[20:18]	RO	reserved	Reserved.
[17]	RW	mac4_up	Control for setting this filter to be used by the uplink port. 0: The uplink port does not use this filter. 1: The uplink port uses this filter.
[16]	RO	reserved	Reserved.
[15:0]	RW	flt_mac4	Upper 16 bits of the filter table MAC4.

GLB_MAC5_L32

GLB_MAC5_L32 is a lower 32-bit register for the filter table MAC5.

Offset Address	Register Name	Total Reset Value
0x1428	GLB_MAC5_L32	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flt_mac5																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	flt_mac5	Lower 32 bits of the filter table MAC5.

GLB_MAC5_H16

GLB_MAC5_H16 is an upper 16-bit register for the filter table MAC5.

Offset Address	Register Name	Total Reset Value
0x142C	GLB_MAC5_H16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										fw2cpu_up	reserved			mac5_up	reserved	flt_mac5															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved.
[21]	RW	fw2cpu_up	Indicates whether to forward the frames received by the uplink port that match this filter to the CPU port when the uplink port enables this filter. 0: no 1: yes
[20:18]	RO	reserved	Reserved.
[17]	RW	mac5_up	Control for setting this filter to be used by the uplink port. 0: The uplink port does not use this filter. 1: The uplink port uses this filter.
[16]	RO	reserved	Reserved.
[15:0]	RW	flt_mac5	Upper 16 bits of the filter table MAC5.

GLB_MAC6_L32

GLB_MAC6_L32 is a lower 32-bit register for the filter table MAC6.

Offset Address	Register Name	Total Reset Value
0x1430	GLB_MAC6_L32	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flt_mac6																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	flt_mac6	Lower 32 bits of the filter table MAC6.

GLB_MAC6_H16

GLB_MAC6_H16 is an upper 16-bit register for the filter table MAC6.

Offset Address	Register Name	Total Reset Value
0x1434	GLB_MAC6_H16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										fw2cpu_up		reserved				mac6_up		reserved		flt_mac6											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved.
[21]	RW	fw2cpu_up	Indicates whether to forward the frames received by the uplink port that match this filter to the CPU port when the uplink port enables this filter. 0: no 1: yes
[20:18]	RO	reserved	Reserved.
[17]	RW	mac6_up	Control for setting this filter to be used by the uplink port. 0: The uplink port does not use this filter. 1: The uplink port uses this filter.
[16]	RO	reserved	Reserved.
[15:0]	RW	flt_mac6	Upper 16 bits of the filter table MAC6.

GLB_MAC7_L32

GLB_MAC7_L32 is a lower 32-bit register for the filter table MAC7.

Offset Address	Register Name	Total Reset Value
0x1438	GLB_MAC7_L32	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flt_mac7																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	flt_mac7	Lower 32 bits of the filter table MAC7.

GLB_MAC7_H16

GLB_MAC7_H16 is an upper 16-bit register for the filter table MAC7.

Offset Address	Register Name	Total Reset Value
0x143C	GLB_MAC7_H16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										fw2cpu_up		reserved				mac7_up		reserved		flt_mac7											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved.
[21]	RW	fw2cpu_up	Indicates whether to forward the frames received by the uplink port that match this filter to the CPU port when the uplink port enables this filter. 0: no 1: yes
[20:18]	RO	reserved	Reserved.
[17]	RW	mac7_up	Control for setting this filter to be used by the uplink port. 0: The uplink port does not use this filter. 1: The uplink port uses this filter.
[16]	RO	reserved	Reserved.
[15:0]	RW	flt_mac7	Upper 16 bits of the filter table MAC7.

UD_GLB_IRQN_SET

UD_GLB_IRQN_SET is a multi-packet interrupt configuration register.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0340	UD_GLB_IRQN_SET	0x0800_003A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				int_frm_cnt				reserved								age_timer															
Reset	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.

[28:24]	RW	int_frm_cnt	These bits are used to set the multi-packet interrupt function. That is, how many packets must be received before a multi-packet interrupt can be reported. **Note:** The minimum value of int_frm_cnt can be set to 1. In this case, multi-packet interrupt is equivalent to single-packet interrupt.
[23:16]	RO	reserved	Reserved.
[15:0]	RW	age_timer	After the multi-packet interrupt function is enabled, if the number of received packets cannot reach the specified number of packets required for reporting the multi-packet interrupt after a period, this period is defined as the aging time for generating the multi-packet interrupt. **Note:** age_timer is counted in the unit of the main clock cycle divided by 256.

UD_GLB_QLEN_SET

UD_GLB_QLEN_SET is a queue length configuration register.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0344	UD_GLB_QLEN_SET	0x0000_2020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				iq_len				reserved				eq_len			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved.
[13:8]	RW	iq_len	RX (packet RX) queue length configuration. **Note:** iq_len cannot be set to 0. Otherwise, it is forcibly set to 1. The sum of the set values of iq_len and eq_len cannot be greater than 64. Otherwise, the value (non-zero) of iq_len is firstly assigned and the value of eq_len is calculated by the formula: 64 – iq_len.
[7:6]	RO	reserved	Reserved.
[5:0]	RW	eq_len	TX (packet TX) queue length configuration. **Note:** eq_len cannot be set to 0. Otherwise, it is forcibly set to 1.

UD_GLB_FC_LEVEL

UD_GLB_FC_LEVEL is a traffic control register.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0348	UD_GLB_FC_LEVEL	0x3018_0508

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																	qlimit_ena	qlimit_up						reserved				qlimit_down			
Reset	0	0	1	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved.
[14]	RW	qlimit_ena	Traffic control enable for RX queue. 0: Disabled (do not transmit the traffic control message according to the status of RX queue). 1: Enabled (transmit the traffic control message according to the status of RX queue).
[13:8]	RW	qlimit_up	Upper limit of traffic control for RX queue. When the free space of the RX queue is less than the upper limit, if traffic control for RX queue is enabled, the traffic control message is transmitted to the peer end. **Note:** If the upper limit qlimit_up is set to 0, the RX queue fails to enter the traffic control status. The upper limit qlimit_up must be greater than the lower limit qlimit_down.
[7:6]	RO	reserved	Reserved.
[5:0]	RW	qlimit_down	Lower limit of traffic control for RX queue. When the free space of the RX queue is equal to or greater than the upper limit, if the RX queue is in traffic control state, the current traffic control is stopped.

UD_GLB_CAUSE

UD_GLB_CAUSE is a cause register for the CPU to which the packet is transmitted.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x034C	UD_GLB_CAUSE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														mact_cause	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2:0]	RO	mact_cause	Packet matching result types by querying the MAC table. 000: Forced forwarding. 001: Packet whose destination MAC address is the local MAC address. 010: Broadcast packet. 011: Packet matching the MAC table. 100: Multicast packet not matching the MAC table. 101: Unicast packet not matching the MAC table. Others: Reserved.

UD_GLB_RXFRM_SADDR

UD_GLB_RXFRM_SADDR is an RX frame start address register.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0350	UD_GLB_RXFRM_SADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rxfrm_saddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rxfrm_saddr	Start address of the RX frame.

UD_GLB_IQFRM_DES

UD_GLB_IQFRM_DES is an RX frame descriptor register.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0354	UD_GLB_IQFRM_DES	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	fd_vlanid			fd_in_addr		fd_in_len		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved.
[17:12]	RO	fd_in_addr	Relative address of the first frame to be received in the input queue (IQ). It serves as the index (0 to iq_len-1) of the absolute address for storing the frames.
[11:0]	RO	fd_in_len	Length of the frame to be received in the RX queue.

UD_GLB_IQ_ADDR

UD_GLB_IQ_ADDR is an RX frame header address register.

The register does not support soft reset.

NOTE

If the address assigned by software is not word aligned, the logic writes data according to the word aligned address. In this case, the previously written data is invalid. For example, if the configured header address of a frame is 0xF000_8002 (non-word-aligned address), the logic writes 0x00 or other data to both the 0xF000_8000 and 0xF000_8001 addresses. Then, the logic writes the first byte (valid data) of the RX frame to the 0xF000_8002 address, writes the second byte (valid data) of the RX frame to the 0xF000_8003 address. Subsequent data is written to the buffer in sequence. If the configured header address of the RX frame is other non-word-aligned address, the logic writes data in a similar way.

Offset Address	Register Name	Total Reset Value
0x0358	UD_GLB_IQ_ADDR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	startaddr_iq							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	startaddr_iq	Header address (configured by the CPU) of the storage space corresponding to the RX frame. The RX frame requests the bus according to this address.

UD_GLB_BFC_STAT

UD_GLB_BFC_STAT is a counter for traffic control status of forward buffer and aging time of multi-packet interrupt.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x035C	UD_GLB_BFC_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	timerover_cnt																flowctrl_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	timerover_cnt	Register for the count of multi-packet interrupt aging time counter overflow events (the count reaches the configured value). **Note:** If the value of timerover_cnt is too large in a unit of time, it indicates that UD_GLB_IRQN_SET[int_frm_cnt] is set improperly. Multi-packet interrupt is triggered by the aging time. Therefore, the configured value must be reduced.
[15:0]	RO	flowctrl_cnt	Register for the count of the forward buffer of the uplink or downlink port entering the traffic control status. **Note:** If the value of flowctrl_cnt is too large in a unit of time, it indicates that UD_GLB_FC_LEVEL[blimit_up] or UD_GLB_FC_LEVEL[blimit_down] is set to a too small value, or the external network condition is worsened. In this case, the configured value may be reduced.

UD_GLB_EQ_ADDR

UD_GLB_EQ_ADDR is a TX queue header address register.

The register does not support soft reset.

NOTE

If the header address of the TX frame is not word aligned, the logic reads data according to the word aligned address. In this case, the previously read data is invalid and discarded. For example, if the configured header address of the TX frame is 0xF000_8102 (non-word-aligned address), the logic directly discards the byte data read from the 0xF000_8100 and 0xF000_8101 addresses. Then, the logic considers the data read from the 0xF000_8102 address as the first byte (valid data) of the TX frame and considers the data read from the 0xF000_8103 address as the second byte (valid data) of the TX frame. All subsequent data is valid (until the data of the specified frame length is read). If the configured header address of the TX frame is other non-word-aligned address, the logic reads data in a similar way.

Offset Address	Register Name	Total Reset Value
0x0360	UD_GLB_EQ_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	add_fd_addr_out																															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	add_fd_addr_out	Header address of the TX frame added by the CPU to the TX queue.

UD_GLB_EQFRM_LEN

UD_GLB_EQFRM_LEN is a TX queue frame length configuration register.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0364	UD_GLB_EQFRM_LEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								add_fd_len_out							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved.
[10:0]	RW	add_fd_len_out	Length of the TX frame added by the CPU to the TX queue. Configure this register to trigger hardware so that software can write the header address and length of the TX frame to the TX queue for transmission. When transmitting a frame, software must write the header address of the frame before the length of the frame. **Note:** The frames whose add_fd_len_out is less than 20 bytes or greater than 1600 bytes are discarded. In other words, the allowed range is from 20 bytes to 1600 bytes.

UD_GLB_QSTAT

UD_GLB_QSTAT is a queue status register.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0368	UD_GLB_QSTAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				iq_in_index				reserved				cpuw_index				reserved				eq_in_index				reserved				eq_out_index			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:24]	RO	iq_in_index	RX index of the RX (packet RX) queue.
[23:22]	RO	reserved	Reserved.
[21:16]	RO	cpuw_index	RX index of frame header address of the RX (packet RX) queue.
[15:14]	RO	reserved	Reserved.
[13:8]	RO	eq_in_index	RX index of frame descriptor of the TX (packet TX) queue.
[7:6]	RO	reserved	Reserved.
[5:0]	RO	eq_out_index	TX index of frame descriptor of the TX (packet TX) queue.

UD_GLB_ADDRQ_STAT

UD_GLB_ADDRQ_STAT is an address queue status register.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x036C	UD_GLB_ADDRQ_STAT	0x0300_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						cpuaddr_in_rdy	eq_in_rdy	reserved				cpu_cnt				reserved				iq_cnt				reserved				eq_cnt			
Reset	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved.
[25]	RO	cpuaddr_in_rdy	Indicates whether the CPU can configure the frame header address of the RX queue. 0: The CPU cannot configure the frame header address of the RX queue. 1: The CPU can configure the frame header address of the RX queue. **Note:** The values of cpuaddr_in_rdy and eq_in_rdy are set to 0 during reset. The values, however, are set to 1 by the circuit immediately after reset. In other words, after reset, the iq address queue and eq descriptor queue are configurable.

[24]	RO	eq_in_rdy	Indicates whether the CPU can configure the frame descriptor (header address and length) of the TX queue. 0: The CPU cannot configure the frame descriptor (header address and length) of the TX queue. 1: The CPU can configure the frame descriptor (header address and length) of the TX queue.
[23:22]	RO	reserved	Reserved.
[21:16]	RO	cpu_cnt	Header address count for available frames assigned by the CPU to the RX queue.
[15:14]	RO	reserved	Reserved.
[13:8]	RO	iq_cnt	Used length of the RX queue (0 to iq_len).
[7:6]	RO	reserved	Reserved.
[5:0]	RO	eq_cnt	Used length of the TX queue (0 to eq_len).

UD_GLB_FC_TIMECTRL

UD_GLB_FC_TIMECTRL is a traffic control time configuration register.

The register does not support soft reset.

offset Address	Register Name	Total Reset Value
0x0370	UD_GLB_FC_TIMECTRL	0x07FF_86A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				flux_timer_cfg												flux_timer_inter															
Reset	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	1	1	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26:17]	RW	flux_timer_cfg	Traffic limit time interval counter, which is used to count the frequency division clock generated by flux_timer_inter. If this counter is set to 0, traffic limit is not performed.
[16:0]	RW	flux_timer_inter	Traffic limit time slot counter, which is used to count the main clock. The default count is 100,000. For a 100-MHz main clock, the time slot is 1 ms.

UD_GLB_FC_RXLIMIT

UD_GLB_FC_RXLIMIT is a traffic control limit configuration register.

The register does not support soft reset.

offset Address	Register Name	Total Reset Value
0x0374	UD_GLB_FC_RXLIMIT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												flux_cfg																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved.
[19:0]	RW	flux_cfg	Traffic limit upper threshold register. This group of bits is used to limit the number of frames received by software in the traffic limit time interval. The frames received after the configured upper threshold is exceeded are selectively discarded or received according to the configuration. When this group of bits is all set to 0, it indicates that traffic limit is not performed.

UD_GLB_FC_DROPCTRL

UD_GLB_FC_DROPCTRL is a packet drop control register for traffic limit.

The register does not support soft reset.

offset Address	Register Name	Total Reset Value
0x0378	UD_GLB_FC_DROPCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													flux_	flux_	broa
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2]	RW	flux_uni	Indicates whether unicast packets are discarded when the upper threshold of traffic limit is exceeded. 0: Do not discard unicast packets. 1: Discard unicast packets.
[1]	RW	flux_multi	Indicates whether multicast packets are discarded when the upper threshold of traffic limit is exceeded. 0: Do not discard multicast packets. 1: Discard multicast packets.
[0]	RW	flux_broad	Indicates whether broadcast packets are discarded when the upper threshold of traffic limit is exceeded. 0: Do not discard broadcast packets. 1: Discard broadcast packets.

5.6.4 Description of the Statistics Counter Control Registers

UD_STS_PORTCNT

UD_STS_PORTCNT is a port status counter.

The register does not support soft reset.

offset Address	Register Name	Total Reset Value
0x0584	UD_STS_PORTCNT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	rxsof_cnt	rxeof_cnt	rxcrcok_cnt	rxcrcbad_cnt	txsof_cnt	txeof_cnt	txcrcok_cnt	txcrcbad_cnt
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	rxsof_cnt	Count of the frame headers received by the port.
[27:24]	RO	rxeof_cnt	Count of the frame trailers received by the port.
[23:20]	RO	rxcrcok_cnt	Count of the frames without CRC errors received by the port.
[19:16]	RO	rxcrcbad_cnt	Count of the frames with CRC errors received by the port.
[15:12]	RO	txsof_cnt	Count of the frame headers transmitted by the port.
[11:8]	RO	txeof_cnt	Count of the frame trailers transmitted by the port.
[7:4]	RO	txcrcok_cnt	Count of the frames without CRC errors transmitted by the port.
[3:0]	RO	txcrcbad_cnt	Count of the frames with CRC errors transmitted by the port.

UD_PORT2CPU_PKTS

UD_PORT2CPU_PKTS is a register for the total number of packets received by the CPU from the uplink or downlink port.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x05A0	UD_PORT2CPU_PKTS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				pkts_cpu			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.

[15:0]	WC	pkts_cpu	Total number of the packets received by the CPU port from the uplink or downlink port. Writing 0 clears this register. Writing 1 has no effect.

UD_CPU2IQ_ADDRCNT

UD_CPU2IQ_ADDRCNT is a register for the count of configuring packet receiving address queue by the CPU.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x05A4	UD_CPU2IQ_ADDRCNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																addr_cpu															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	WC	addr_cpu	Count of configuring packet receiving address queue by the CPU successfully. Writing 0 clears this register. Writing 1 has no effect.

UD_RX_IRQCNT

UD_RX_IRQCNT is a register for the count of reporting single-packet interrupt by the uplink or downlink port.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x05A8	UD_RX_IRQCNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																pkts_port															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	WC	pkts_port	Count of the frame RX interrupts reported by the uplink or downlink port. Writing 0 clears this register. Writing 1 has no effect.

UD_CPU2EQ_PKTS

UD_CPU2EQ_PKTS is a register for the total number of packets transmitted by the CPU to the uplink or downlink port.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x05AC	UD_CPU2EQ_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																pkts_cpu2tx															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	WC	pkts_cpu2tx	Total number of packets transmitted by the CPU to the uplink or downlink port. Writing 0 clears this register. Writing 1 has no effect.

5.6.5 Description of the Statistics Result Registers

Statistics result registers can be configured in two modes: read only and read clear. If UD_MAC_SET[cntr_rdclr_en] is set to 1, it indicates the read clear mode. If UD_MAC_SET[cntr_rdclr_en] is set to 0, it indicates the read only mode. The following registers are described only in read only mode.

UD_RX_DVCNT

UD_RX_DVCNT is an RXDV rising edge count register.

The register does not support soft reset.

offset Address	Register Name	Total Reset Value
0x0600	UD_rx_DVCNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rxdvrise																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rxdvrise	Count of all RXDV rising edges.

UD_RX_OCTS

UD_RX_OCTS is a register for the total number of bytes received.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0604	UD_RX_OCTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ifinoctets																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	ifinoctets	Count of all received bytes, including the bytes in correct frames, error frames, and preambles. The frames without valid start of frame delimiters (SFDs) are not counted.

UD_RX_RIGHTOCTS

UD_RX_RIGHTOCTS is a register for the total number of bytes of received correct packets.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0608	UD_RX_RIGHTOCTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	octets_rx																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	octets_rx	Count of the received bytes, including the bytes in correct frames and error frames but excluding the bytes in preambles. The frames without valid SFDs are not counted.

UD_HOSTMAC_PKTS

UD_HOSTMAC_PKTS is a register for the number of packets matching the local MAC address.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x060C	UD_HOSTMAC_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	local_mac_match																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	local_mac_match	Count of correct RX frames whose destination MAC address is the same as the local MAC address, excluding short frames, long frames, frames with CRC errors, pause frames, and error TX frames.

UD_RX_RIGHTPKTS

UD_RX_RIGHTPKTS is a register for the total number of packets received by the port.

The register does not support soft reset.

offset Address	Register Name	Total Reset Value
0x0610	UD_RX_RIGHTPKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pkts																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	pkts	Count of all frames.

UD_RX_BROADPKTS

UD_RX_BROADPKTS is a register for the number of correct broadcast packets.

The register does not support soft reset.

offset Address	Register Name	Total Reset Value
0x0614	UD_RX_broadpkts	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	broadcastpkts																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	broadcastpkts	Count of broadcast frames with valid length and without CRC errors, excluding pause frames and error TX frames.

UD_RX_MULTPKTS

UD_RX_MULTPKTS is a register for the number of correct multicast packets.

The register does not support soft reset.

offset Address	Register Name	Total Reset Value
0x0618	UD_RX_multpkts	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	multicastpkts																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	multicastpkts	Count of multicast frames with valid length and without CRC errors, excluding pause frames and error TX frames.

UD_RX_UNIPKTS

UD_RX_UNIPKTS is a register for the number of correct unicast packets.

The register does not support soft reset.

offset Address	Register Name	Total Reset Value
0x061C	UD_RX_UNIpkts	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ifinucastpkts																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	ifinucastpkts	Count of unicast frames with valid length and without CRC errors, excluding pause frames and error TX frames.

UD_RX_ERRPKTS

UD_RX_ERRPKTS is a register for the total number of incorrect packets.

The register does not support soft reset.

offset Address	Register Name	Total Reset Value
0x0620	UD_RX_ERRPKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ifinerrors																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	ifinerrors	Count of all error frames, including frames with CRC errors, short frames, long frames, and error TX frames.

UD_RX_CRCERR_PKTS

UD_RX_CRCERR_PKTS is a register for the count of CRC errors.

The register does not support soft reset.

offset Address	Register Name	Total Reset Value
0x0624	UD_RX_crcerr_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	crcerr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	crcerr	Count of RX frames with valid length (non short and long frames) but with CRC or alignment errors.

UD_RX_LENERR_PKTS

UD_RX_LENERR_PKTS is a register for the number of packets with invalid length.

The register does not support soft reset.

offset Address	Register Name	Total Reset Value
0x0628	UD_RX_LENERR_pkts	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	abnormalsizepkts																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	abnormalsizepkts	Count of frames (short frames and long frames) with invalid length (less than the set minimum valid length or greater than the set maximum valid length).

UD_RX_OCRCERR_PKTS

UD_RX_OCRCERR_PKTS is a register for the number of packets with odd nibbles and CRC errors.

The register does not support soft reset.

offset Address	Register Name	Total Reset Value
0x062C	UD_RX_OCRCERR_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dot3alignmenterr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	dot3alignmenterr	Received frames with odd nibbles and CRC errors.

UD_RX_PAUSE_PKTS

UD_RX_PAUSE_PKTS is a register for the number of received pause packets.

The register does not support soft reset.

offset Address	Register Name	Total Reset Value
0x0630	UD_RX_PAUSE_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dot3pause																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	dot3pause	Count of received pause frames.

UD_RF_OVERCNT

UD_RF_OVERCNT is a register for the count of RXFIFO overflow events.

The register does not support soft reset.

offset Address	Register Name	Total Reset Value
0x0634	UD_RF_OVERCNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dropevents																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	dropevents	Accumulative count of RXFIFO overflow events during the reception of frames.

UD_FLUX_TOL_IPKTS

UD_FLUX_TOL_IPKTS is a register for the total number of received packets allowed by the traffic limit.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0638	UD_flux_TOL_IPKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flux_frame_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	flux_frame_cnt	Total count of correct RX frames allowed by the traffic limit, excluding short frames, long frames, frames with CRC errors, pause frames, and error TX frames.

UD_FLUX_TOL_DPKTS

UD_FLUX_TOL_DPKTS is a register for the total number of packets discarded due to traffic limit. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x063C	UD_flux_TOL_DPKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flux_drop_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	flux_drop_cnt	Count of correct frames discarded due to traffic limit, excluding short frames, long frames, frames with CRC errors, pause frames, and error TX frames.

UD_MN2CPU_PKTS

UD_MN2CPU_PKTS is a register for the number of packets not forwarded to the CPU port due to MAC limit. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x064C	UD_MN2CPU_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mac_not2cpu_pkts																															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	mac_not2cpu_pkts	Number of packets not forwarded to the CPU port due to MAC limit.

UD_TX_PKTS

UD_TX_PKTS is a register for the total number of packets transmitted successfully. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0780	UD_TX_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pkts_tx																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	pkts_tx	Count of all configured TX frames, excluding the frames discarded due to timeout and the TX frames whose length of UD_GLB_EQFRM_LEN is not within valid range.

UD_TX_BROADPKTS

UD_TX_BROADPKTS is a register for the number of broadcast packets transmitted successfully. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0784	UD_TX_BROADPKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	broadcastpkts_tx																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	broadcastpkts_tx	Count of broadcast frames transmitted successfully (excluding retransmission).

UD_TX_MULTPKTS

UD_TX_MULTPKTS is a register for the number of multicast packets transmitted successfully. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0788	UD_TX_MULTPKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	multicastpkts_tx																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	multicastpkts_tx	Count of multicast frames transmitted successfully (excluding retransmission).

UD_TX_UNIPKTS

UD_TX_UNIPKTS is a register for the number of unicast packets transmitted successfully. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x078C	UD_TX_UNIPKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ifoutucastpkts_tx																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	ifoutucastpkts_tx	Count of unicast frames transmitted successfully (excluding retransmission).

UD_TX_OCTS

UD_TX_OCTS is a register for the total number of transmitted bytes. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0790	UD_TX_OCTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	octets_tx																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	octets_tx	Total count of transmitted bytes, including the bytes of retransmit frames, correct frames, and error frames, but excluding the preamble bytes.

UD_TX_PAUSE_PKTS

UD_TX_PAUSE_PKTS is a register for the number of transmitted pause frames. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0794	UD_TX_PAUSE_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dot3outpause																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	dot3outpause	Count of transmitted pause frames.

UD_TX_RETRYCNT

UD_TX_RETRYCNT is a register for the total count of retransmission. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0798	UD_TX_RETRYCNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	retry_times_tx																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	retry_times_tx	Total count of retransmissions of TX frames.

UD_TX_COLCNT

UD_TX_COLCNT is a register for the total count of collisions. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x079C	UD_TX_COLCNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	collisions																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	collisions	Count of collisions.

UD_TX_LC_PKTS

UD_TX_LC_PKTS is a register for the number of packets with late collision. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x07A0	UD_TX_LC_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dot3latecol																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	dot3latecol	Count of packets with late collision.

UD_TX_COLOK_PKTS

UD_TX_COLOK_PKTS is a register for the number of packets transmitted successfully with collisions. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x07A4	UD_TX_COLOK_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dot3col_ok																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	dot3col_ok	Count of packets transmitted successfully with collisions.

UD_TX_RETRY15_PKTS

UD_TX_RETRY15_PKTS is a register for the number of packets discarded due to more than 15 times of retransmission. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x07A8	UD_TX_RETRY15_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dot3excessivecol																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description

[31:0]	RO	dot3excessivecol	Count of the packets discarded due to more than 15 times of retransmission.

UD_TX_RETRYN_PKTS

UD_TX_RETRYN_PKTS is a register for the number of packets with the count of collisions being equal to the threshold. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x07AC	UD_TX_RETRYN_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dot3colcnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	dot3colcnt	Count of packets with the count of collisions being equal to the threshold. This register is set by UD_MAC_SET[colthreshold].

Contents

Figures

6 Video Encoder

6.1 Introduction

The video encoder consists of the video encoding (VENC) unit and JPEG encoder (JPGE). The VENC unit supports H.264 encoding, and the JPGE supports JPEG encoding.

6.2 VENC

6.2.1 Overview

The VENC unit is an encoder that supports H.264 protocol and performs encoding by using hardware. It features low CPU usage, low bus bandwidth, low delay, and low power consumption.

6.2.2 Features

The VENC has the following features

- Supports ITU-T H.264 main profile/baseline profile@ level 4.1 encoding.
  - Motion compensation with 1/2 or 1/4 pixel precision
  - Four subblock types of 16x16, 16x8, 8x16, and 8x8 for interframe encoding
  - Prediction modes of intra 4x4 and intra 16x16 for intraframe encoding
  - Trans4x4
  - Context-based adaptive binary arithmetic coding (CABAC) and context-based adaptive variable-length coding (CAVLC) entropy encoding
  - De-blocking filtering
  - IPCM encoding
- Supports multiple input picture formats:
  - Semi-planar YCbCr4:2:0
  - Semi-planar YCbCr4:2:2
- Supports the typical application of three-stream encoding at 1x720p@30 fps+1xVGA@30 fps+1xQVGA@30 fps.
- Supports configurable picture resolutions.
  - Minimum picture resolution: 160x64

  - Maximum picture resolution: 1920x2048
  - Step of the picture width or height: 4
- Supports region of interest (ROI) encoding.
  - A maximum of eight ROIs
  - ROI encoding control
- Supports on-screen display (OSD) encoding protection.

  OSD encoding protection control
- Supports OSD front-end overlaying.
  - OSD overlaying before encoding for a maximum of eight regions
  - OSD overlaying at the maximum picture size anywhere
  - 129-level alpha blending
  - OSD overlaying control
- Supports constant bit rate (CBR) mode and variable bit rate (VBR) mode.
- Supports the output bit rate ranging from 32 kbit/s to 40 Mbit/s.
- Supports in-loop motion compensated temporal filtering (MCTF) during I and P frame encoding.
- Supports low-power algorithms.

6.2.3 Function Description

Figure 6-1 shows the encoding functional block diagram of the VENC.

Based on related protocols and algorithms, the VENC supports motion estimation, inter-prediction, intra-prediction, motion vector prediction, transform/quantization, inverse transform/inverse quantization, variable length code (VLC) encoding, stream generation, and de-blocking filtering. The video firmware (FMW) controls the bit rate and handles interrupts.

Before the VENC is enabled for video encoding, the software allocates three types of buffers for the VENC in the external DDR SDRAM:

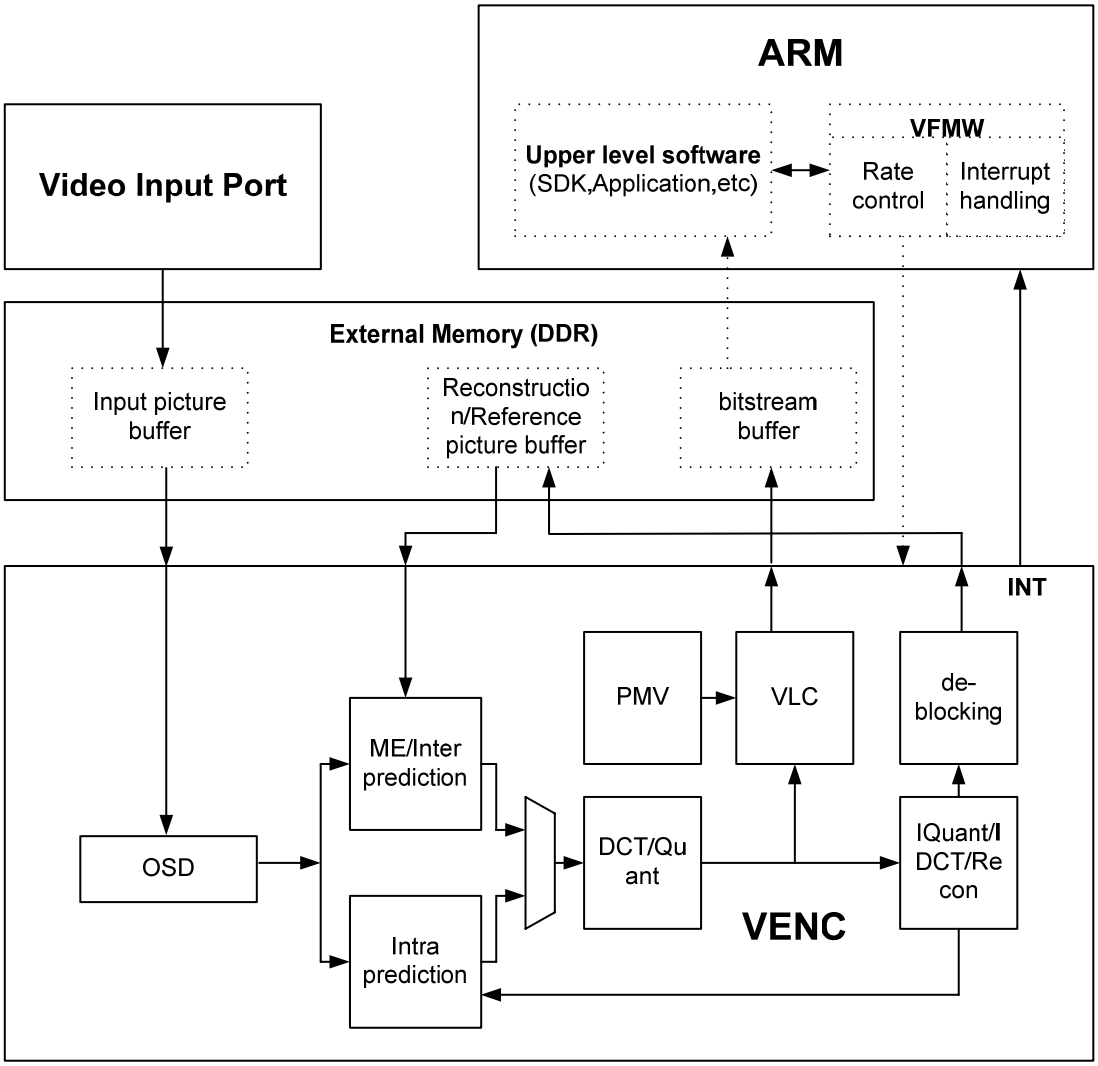
- Input picture buffer

  The VENC reads the source pictures to be encoded from this buffer during encoding. This buffer is typically written by the VICAP module.
- Reconstruction/reference picture buffer

  The VENC writes reconstruction pictures to this buffer during encoding. These reconstruction pictures are used as the reference pictures of subsequent pictures. During the encoding of P frames, reference pictures are read from this buffer.
- Stream buffer

  This buffer stores encoded streams. The VENC writes streams to this buffer during encoding. This buffer is read by software.

Figure 6-1 Encoding function block diagram of the VENC unit



6.3 JPGE

6.3.1 Overview

The JPGE provides high-performance encoding performance by using hardware. It supports snapshot or HD MJPEG encoding.

6.3.2 Features

The JPGE has the following features:

- Supports ISO/IEC 10918-1 (CCITT T.81) baseline process (DCT sequential) encoding.
- Encodes the pictures in the chrominance sampling format of YCbCr4:2:0, YCbCr4:2:2, or YCbCr4:4:4.
- Supports the microprogrammed control unit (MCU) using the interleaved sequence.

- Supports multiple input picture formats.
  - Planar YCbCr4:2:0
  - Planar YCbCr4:2:2
  - Planar YCbCr4:4:4
  - Semi-planar YCbCr4:2:0
  - Semi-planar YCbCr4:2:2
  - Package YCbCr4:2:2
- Supports at most 720p@30 fps.
- Supports configurable picture resolutions.
  - Minimum picture resolution: 64x64
  - Maximum picture resolution: 8192x8192
- Supports the picture width or height step of 4.
- Supports configurable quantization tables.

  An independent quantization table for the Y component, Cb component, and Cr component respectively
- Supports OSD front-end overlaying.
  - OSD overlaying before encoding for a maximum of eight regions
  - OSD overlapping with the maximum size of the source picture and within the picture position range
  - 129-level alpha blending
  - OSD overlaying control

6.3.3 Function Description

Figure 6-2 shows the functional block diagram of the JPGE.

Based on the protocols that require a large number of operands, the JPGE supports OSD, level shift, discrete cosine transform (DCT), quantization, scanning, VLC encoding, and stream generation. The VFMW configures quantization tables and handles interrupts.

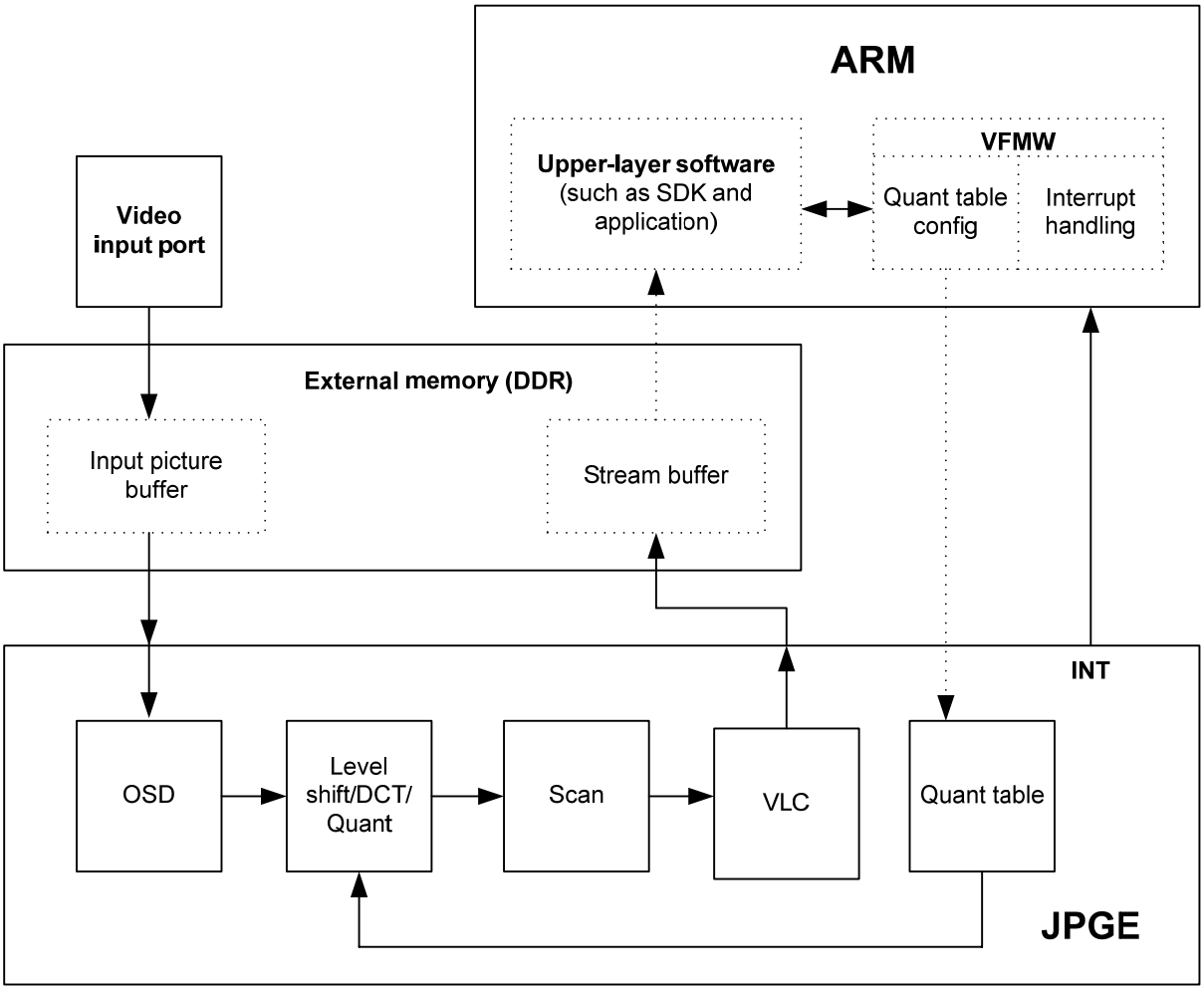
Before the JPGE is enabled for video encoding, the software allocates two types of buffers for the JPGE in the external DDR SDRAM:

- Input picture buffer

  The JPGE reads the source pictures to be encoded from this buffer during encoding. This buffer is generally written by the VICAP module.
- Stream buffer

  This buffer stores encoded streams. The JPGE writes streams to this buffer during encoding. This buffer is read by software.

Figure 6-2 Functional block diagram of the JPGE



Contents

7 Video and Graphics Processing

7.1 TDE

7.1.1 Overview

The two-dimensional engine (TDE) draws graphics using hardware. This significantly reduces the CPU usage and improves the utilization of the memory bandwidth. The TDE reads and writes the information about the bitmap data, filtering/scaling coefficients, parameters of linked list nodes, and linked list over the advanced eXtensible bus (AXI) master interface. By using the advanced peripheral bus (AHB) interface, the TDE obtains the CPU register configuration information.

The graphics data interface includes source channel 1. The functions are as follows:

- Source channel 1 implements direct copy and direct filling during a single-source operation.
- Source channel 1 implements complicated functions such as scaling, anti-flicker, rotation, and lens distortion correction during a single-source operation.

7.1.2 Function Description

The TDE has the following features:

- Source bitmap 1 supports the formats of ARGB4444, ARGB1555, YCbCr422, and YCbCr420.
- The output bitmap supports the formats of ARGB4444, ARGB1555, YCbCr422, YCbCr420.
- Allows the formats of source bitmap 1 and output bitmaps to be configured separately.
- Supports direct copy.
- Supports direct filling.
- Supports anti-flicker.
- Supports monochrome colorkey.
- Supports programmable scanning.
- Supports image rotation by 90º or 270º.
- Supports lens distortion correction vertically.
- Supports the software interface in synchronous/asynchronous linked list mode.
- Provides status interrupts.

7.2 VPSS

7.2.1 Overview

The video processing subsystem (VPSS) implements video processing before encoding. The video processing functions include 3D Gaussian noise adaptive reduction, de-interlace, great ratio scaling, sharpening, and block processing.

The VPSS has the following functions:

- Processes the video source whose width is less than 512 pixels for a node.
- Supports the simultaneous output of the major/minor streams of the encoding channel.
- Supports 1080i/1080p processing by block.
- Supports register linked list configuration.
- Supports the span of 4 KB boundary.
- Supports input/output data formats of YUV420 and YUV422 (conversion from YUV420 to YUV422 is not supported).
- Supports outstanding configuration.
- Supports the low-power mode by using clock gating for memory

7.2.2 Features

The VPSS has the following features:

- Gaussian noise reduction: The noise reduction (NR) module removes the Gaussian noise of the graphics by configuring the parameters. This makes the graphics become smooth and reduces the encoding bit rate.
- De-interlace: The de-interlace (DIE) module restores the interlaced video source to the progressive video source.
- Image sharpening: The LTI and CTI modules extract high-frequency components from pictures before scaling and compensate frequencies for the pictures processed by the scaler. In this way, pictures have sharp edges and clear contours.
- Image processing by block: When the width of an image in a frame is greater than 512, the image is processed by block. In this mode, the maximum width is ∞ in theory.

Contents

Tables

8 Motion Detect Unit

8.1 Overview

As a high-performance hardware acceleration intellectual property (IP), the motion detect unit (MDU) is used to detect the motion status and video occlusion, implement modeling on the video background, and calculate the information about the object (OBJ) region. The OBJ region is a rectangular motion part of the current frame. By using the advanced eXtensible interface (AXI) master bus, the MDU reads picture information, and writes the updated information about the background, sum of absolute differences (SADs), and OBJ regions. By using the slave advanced high-performance bus (APB), the MDU obtains register configurations.

8.2 Function Description

The MDU provides the following features:

- Calculates and outputs the SAD in the unit of 8x8 or 16x16.
- Detects OBJ regions and outputs the information about the OBJ regions.
- Refreshes the background.

8.3 Operating Mode

8.3.1 Software and Hardware for Motion Detection

The software performs the following operations for the pictures to be encoded:

- Allocates the storage space in the double-data rate (DDR).
- Calls the hardware to capture videos or perform scaling.
- Schedules multiple motion detection operations, specifies and divides the regions to be detected, and generates addresses.

The hardware calculates the SADs of input pictures. The details are as follows:

- Detects OBJ regions based on the SAD and threshold, and refreshes the background.

- Outputs the information about OBJ regions, background, and SADs based on the settings of the software.

8.3.2 Software and Hardware for Video Occlusion Detection

Based on the size of OBJ regions output by the hardware, the software checks whether the occlusion threshold is reached. If the threshold is reached, the background is forbidden to refresh, but motion detection is still performed. When the size of OBJ regions is greater than the occlusion threshold, an occlusion alarm is generated.

8.4 Register Summary

Table 8-1 describes the MDU registers.

Table 8-1 Summary of the MDU registers (base address: 0x206C_0000)

Offset Address	Register	Description	Page
0x0000	MDU_INTSTAT	Interrupt status register	8-3
0x0004	MDU_INTEN	Interrupt enable register	8-4
0x0008	MDU_RAWINT	Raw interrupt register	8-5
0x000C	MDU_INTCLR	Interrupt clear register	8-5
0x0020	MDU_VEDIMGSIZE	Picture size configuration register	8-6
0x0024	MDU_MODE	Mode configuration register	8-7
0x0028	MDU_START	MDU start register	8-8
0x002C	MDU_AXI_OUTSTD_NUM	AXI outstanding configuration register	8-8
0x0040	MDU_REF_YADDR	Luminance storage address register of the reference picture	8-9
0x0044	MDU_REF_YSTRIDE	Luminance stride register of the reference picture	8-9
0x0048	MDU_CUR_YADDR	Luminance storage address register of the current picture	8-10
0x004C	MDU_CUR_YSTRIDE	Luminance stride register of the current picture	8-10
0x0060	MDU_MBSAD_ADDR	Macroblock SAD storage address register	8-11
0x0064	MDU_MBSAD_STRIDE	Macroblock SAD storage stride register	8-11
0x0070	MDU_BACKGROUND_ADDR	Luminance storage address register of the background	8-12

Offset Address	Register	Description	Page
0x0074	MDU_BACKGROUND_STRIDE	Luminance stride register of the background	8-12
0x0078	MDU_OBJ_ADDR	OBJ region storage address register	8-12
0x007C	MDU_BG_UP_WEIGHT	Background refresh weight register	8-13
0x0080	MDU_MBSAD_TH	Macroblock motion detection threshold register	8-14
0x0084	MDU_TIMEOUT	Timeout upper limit register	8-14
0x0090	MDU_WND_SIZE	SAD output window configuration register	8-14
0x0094	MDU_MIN_OBJ_SIZE	Minimum window configuration register for boundary search	8-15
0x0098	MDU_MAX_OBJ_CNT	Maximum window configuration register for boundary search	8-16
0x009C	MDU_OBJ_CNT	OBJ region information readback register	8-16
0x00A0	MDU_MAX_OBJ_SIZE	Maximum OBJ region readback register	8-16
0x00A4	MDU_TOTAL_OBJ_SIZE	All OBJ region information readback register	8-17
0x00A8	MDU_MOVE_PIX_CNT	Motion pixel statistics register for an entire frame	8-18
0x00AC	MDU_OBJ_CNT1	OBJ region information readback register based on the background	8-18
0x00B0	MDU_MAX_OBJ_SIZE1	Maximum OBJ region readback register based on the background	8-18
0x00B4	MDU_TOTAL_OBJ_SIZE1	All OBJ region information readback register based on the background	8-19
0x00B8	MDU_MOVE_PIX_CNT1	Motion pixel statistics register for an entire frame based on the background	8-19

8.5 Register Description

MDU_INTSTAT

MDU_INTSTAT is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0000	MDU_INTSTAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mdu_bus_err	mdu_cfg_err	reserved																												mdu_timeout	mdu_endofpic
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	mdu_bus_err	Bus read/write error.
[30]	RO	mdu_cfg_err	Register configuration error.
[29:2]	RO	reserved	Reserved.
[1]	RO	mdu_timeout	MDU timeout interrupt. This interrupt is valid when the timeout detection mode of the MDU is enabled and the working cycle of the MDU is greater than the threshold configured by MDU_TIMEOUT.
[0]	RO	mdu_endofpic	End of picture indicator of the MDU, active high.

MDU_INTEN

MDU_INTEN is an interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x0004	MDU_INTEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mdu_bus_err_en	mdu_cfg_err_en	reserved																												mdu_timeout_en	mdu_endofpic_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	mdu_bus_err_en	BUS read/write error interrupt enable. 0: disabled 1: enabled

[30]	RW	mdu_cfg_err_en	Register configuration error interrupt enable. 0: disabled 1: enabled
[29:2]	RO	reserved	Reserved.
[1]	RW	mdu_timeout_en	MDU timeout interrupt enable. When the timeout detection mode of the MDU is enabled and the working cycle of the MDU is greater than the threshold configured by MDU_TIMEOUT, this interrupt is valid. 0: disabled 1: enabled
[0]	RW	mdu_endofpic_en	End of picture interrupt enable of the MDU 0: disabled 1: enabled

MDU_RAWINT

MDU_RAWINT is a raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x0008	MDU_RAWINT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mdu_bus_err_raw	mdu_cfg_err_raw	reserved																												mdu_timeout_raw	mdu_endofpic_raw
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	mdu_bus_err_raw	Raw bus read/write error interrupt, active high.
[30]	RO	mdu_cfg_err_raw	Raw register configuration error interrupt, active high.
[29:2]	RO	reserved	Reserved.
[1]	RO	mdu_timeout_raw	Raw MDU timeout interrupt, active high.
[0]	RO	mdu_endofpic_raw	Raw end of picture interrupt of the MDU, active high.

MDU_INTCLR

MDU_INTCLR is an interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x000C	MDU_INTCLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mdu_bus_err_clr	mdu_cfg_err_clr	reserved																												mdu_timeout_clr	mdu_endofpic_clr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	mdu_bus_err_clr	Bus read/write error clear, active high.
[30]	RW	mdu_cfg_err_clr	Register configuration error clear, active high.
[29:2]	RO	reserved	Reserved.
[1]	RW	mdu_timeout_clr	MDU timeout interrupt clear. When the timeout detection mode of the MDU is enabled and the working cycle of the MDU is greater than the threshold configured by MDU_TIMEOUT, this interrupt is valid.
[0]	RW	mdu_endofpic_clr	End of picture indicator clear of the MDU, active high.

MDU_VEDIMGSIZE

MDU_VEDIMGSIZE is a picture size configuration register.

Offset Address	Register Name	Total Reset Value
0x0020	MDU_VEDIMGSIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				imgheightinpixelsminus1												reserved				imgwidthinpixelsminus1											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28:16]	RW	imgheightinpixelsminus1	Picture height. The value is in the unit of pixel, and the configured value is obtained by subtracting 1 from the actual height. For example, if the picture height is 352 pixels, this field must be set to 351 pixels.
[15:13]	RO	reserved	Reserved.

[12:0]	RW	imgwidthinpixelsminus1	Picture width. The value is in the unit of pixel, and the configured value is obtained by subtracting 1 from the actual width. For example, if the picture width is 288 pixels, this field must be set to 287 pixels.

MDU_MODE

MDU_MODE is a mode configuration register.

Offset Address	Register Name	Total Reset Value
0x0024	MDU_MODE	0x0000_019C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							mcpi_clkgate_en	mcpi_wrlock_en	timeout_en	md_mod	bg_update_en	eg_find_en	obj_out_en	sad_out_en	sad_mad_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	0	0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved.
[8]	RW	mcpi_clkgate_en	Clock gating enable.
[7]	RW	mcpi_wrlock_en	Register configuration lock enable. If this field is enabled, registers cannot be configured even if the MDU is started until the detection ends. This avoids modifications made to registers.
[6]	RW	timeout_en	MDU timeout detection enable. If this field is enabled, the upper limits of the working cycle that is configured using MDU_TIMEOUT by the software can be automatically queried. 0: disabled 1: enabled
[5]	RW	md_mod	Motion detection mode. 0: background algorithm 1: frame reference algorithm
[4]	RW	bg_update_en	Background refresh enable. 0: disabled 1: enabled This field is valid only when md_mod is set to 0 (background algorithm).

[3]	RW	eg_find_en	Joint detection enable for OBJ regions. 0: disabled 1: enabled If the background algorithm is selected, only the last joint detection based on the background is disabled.
[2]	RW	obj_out_en	OBJ region output enable. If this field is enabled, MDU_OBJ_ADDR must be configured. 0: disabled 1: enabled
[1]	RW	sad_out_en	SAD output enable. If this field is enabled, MDU_MBSAD_ADDR and MDU_MBSAD_STRIDE must be configured. 0: disabled 1: enabled
[0]	RW	sad_mad_sel	Number of SAD output bits. 0: 8 bits 1: 16 bits

MDU_START

MDU_START is an MDU start register.

Offset Address	Register Name	Total Reset Value
0x0028	MDU_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															mdu_start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	WO	mdu_start	MDU start control. 0: The MDU does not work. 1: The MDU is started.

MDU_AXI_OUTSTD_NUM

MDU_AXI_OUTSTD_NUM is an AXI outstanding configuration register.

Offset Address	Register Name	Total Reset Value
0x002C	MDU_AXI_OUTSTD_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														axi_outstd_num	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2:0]	RW	axi_outstd_num	AXI outstanding configuration. The count value is numbered from 0 and the actual value is obtained by adding 1 to the count value.

MDU_REF_YADDR

MDU_REF_YADDR is a luminance storage address register of the reference picture.

Offset Address	Register Name	Total Reset Value
0x0040	MDU_REF_YADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mdu_ref_yaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	mdu_ref_yaddr	Storage address of the Y component of the reference picture. The input raw picture must be Qword-aligned (128 bits). That is, the lower four bits of the address are 0. The hardware automatically sets the lower four bits of the address to 0.

MDU_REF_YSTRIDE

MDU_REF_YSTRIDE is a luminance stride register of the reference picture.

Offset Address	Register Name	Total Reset Value
0x0044	MDU_REF_YSTRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																mdu_ref_ystride																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	mdu_ref_ystride	Luminance stride, in bytes. The lower four bits of Ystride must be set to 0. This is to ensure that the address is 128-bit-aligned after the picture is wrapped. The hardware automatically sets the lower four bits of Ystride to 0. The stride must be an integral multiple of 64 bytes.

MDU_CUR_YADDR

MDU_CUR_YADDR is a luminance storage address register of the current picture.

Offset Address	Register Name	Total Reset Value
0x0048	MDU_CUR_YADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mdu_cur_yaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	mdu_cur_yaddr	Storage address of the Y component of the raw picture. The input raw picture must be Qword-aligned (128 bits). That is, the lower four bits of the address are 0. The hardware automatically sets the lower four bits of the address to 0.

MDU_CUR_YSTRIDE

MDU_CUR_YSTRIDE is a luminance stride register of the current picture.

Offset Address	Register Name	Total Reset Value
0x004C	MDU_CUR_YSTRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																mdu_cur_ystride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	mdu_cur_ystride	Luminance stride, in bytes. The lower four bits of Ystride must be set to 0. This is to ensure that the address is 128-bit-aligned after the picture is wrapped. The hardware automatically sets the lower four bits of Ystride to 0. The stride must be an integral multiple of 64 bytes.

MDU_MBSAD_ADDR

MDU_MBSAD_ADDR is a macroblock SAD storage address register.

Offset Address	Register Name	Total Reset Value
0x0060	MDU_MBSAD_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mdu_mbsad_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	mdu_mbsad_addr	Address for storing the macroblock SAD. The address must be Qword-aligned. Therefore, the lower four bits must be 0.

MDU_MBSAD_STRIDE

MDU_MBSAD_STRIDE is a macroblock SAD storage stride register.

Offset Address	Register Name	Total Reset Value
0x0064	MDU_MBSAD_STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																mdu_mbsad_stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.

[15:0]	RW	mdu_mbsad_stride	Macroblock SAD stride, in bytes. The stride must be 128-bit-aligned. Therefore, the lower four bits must be 0.

MDU_BACKGROUND_ADDR

MDU_BACKGROUND_ADDR is a luminance storage address register of the background.

Offset Address	Register Name	Total Reset Value
0x0070	MDU_BACKGROUND_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bg_yaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	bg_yaddr	Background address. The address must be Qword-aligned. Therefore, the lower four bits must be 0.

MDU_BACKGROUND_STRIDE

MDU_BACKGROUND_STRIDE is a luminance stride register of the background.

Offset Address	Register Name	Total Reset Value
0x0074	MDU_BACKGROUND_STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																bg_ystride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	bg_ystride	Background stride, in bytes. The stride must be 128-bit-aligned. Therefore, the lower four bits must be 0.

MDU_OBJ_ADDR

MDU_OBJ_ADDR is an OBJ region storage address register.

Offset Address	Register Name	Total Reset Value
0x0078	MDU_OBJ_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	obj_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	obj_addr	Address for storing OBJ regions. The address must be Qword-aligned. Therefore, the lower four bits must be 0. An OBJ region is stored as follows: The coordinates of the left, top, right, and bottom points of the OBJ region are stored in sequence in four 16-bit spaces. Therefore, two 32-bit DDRs are used to store an OBJ region. When the DDR is allocated by using the software, the minimum DDR size is calculated as follows: 2 x 32 bits x Maximum number of OBJ regions

MDU_BG_UP_WEIGHT

MDU_BG_UP_WEIGHT is a background refresh weight register.

Offset Address	Register Name	Total Reset Value
0x007C	MDU_BG_UP_WEIGHT	0x0000_0101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																src_weight								weight_sum_exp_2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:8]	RW	src_weight	New picture weight.
[7:0]	RW	weight_sum_exp_2	Exponent of 2 to the weighted sum. When the MDU generates a new background by overlaying the source picture with the existing background, the following formula is used: (Background pixel x ((1<<weight_sum_exp_2) – src_weight) + Pixel of source picture x bg_weight) >> weight_sum_exp_2) The background weight bg_weight is calculated as follows: ((1<<weight_sum_exp_2) – src_weight) The greater the value obtained from background weight bg_weight minus source weight src_weight, the more slowly the background is refreshed. The default value is 0x1, and the maximum value is 0x8.

MDU_MBSAD_TH

MDU_MBSAD_TH is a macroblock motion detection threshold register.

Offset Address	Register Name	Total Reset Value
0x0080	MDU_MBSAD_TH	0x0000_001E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																mdu_mbsad_th															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	mdu_mbsad_th	Threshold for detecting the motion status of the 4x4 macroblock. All calculations of the MDU are based on the 4x4 macroblock.

MDU_TIMEOUT

MDU_TIMEOUT is a timeout upper limit register.

Offset Address	Register Name	Total Reset Value
0x0084	MDU_TIMEOUT	0x0360_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mdu_timeout																															
Reset	0	0	0	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	mdu_timeout	Maximum number of working cycles.

MDU_WND_SIZE

MDU_WND_SIZE is a SAD output window configuration register.

Offset Address	Register Name	Total Reset Value
0x0090	MDU_WND_SIZE	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															sad_wnd_size
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	sad_wnd_size	Size of the SAD output window. The calculations of the MDU are based on the 4x4 macroblock. After the sad_out_en bit of the mode register is enabled, the MDU adds the values of multiple 4x4 macroblocks based on the settings of sad_wnd_size, and outputs the value to the DDR. 0: 8x8 1: 16x16 (default)

MDU_MIN_OBJ_SIZE

MDU_MIN_OBJ_SIZE is the minimum window configuration register for boundary search.

Offset Address	Register Name	Total Reset Value
0x0094	MDU_MIN_OBJ_SIZE	0x0300_0101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	egsearch_timeout																min_obj_size_h								min_obj_size_w							
Reset	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:16]	RW	egsearch_timeout	Boundary search timeout. If the number of points of an OBJ region is greater than the value, the boundary search of the OBJ region stops, and the search for the next region starts.
[15:8]	RW	min_obj_size_h	Minimum height of the OBJ region. The OBJ region whose height is smaller than this value is not reported. The value 1 of min_obj_size_h indicates a 4x4 macroblock.
[7:0]	RW	min_obj_size_w	Minimum width of the OBJ region. The OBJ region whose width is smaller than this value is not reported. The value 1 of min_obj_size_w indicates a 4x4 macroblock.

MDU_MAX_OBJ_CNT

MDU_MAX_OBJ_CNT is the maximum window configuration register for boundary search.

Offset Address	Register Name	Total Reset Value
0x0098	MDU_MAX_OBJ_CNT	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																max_obj_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	max_obj_cnt	Maximum value for detecting the OBJ regions.

MDU_OBJ_CNT

MDU_OBJ_CNT is an OBJ region information readback register.

Offset Address	Register Name	Total Reset Value
0x009C	MDU_OBJ_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_obj_index																obj_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	max_obj_index	Maximum OBJ region index. For the statistics register whose name does not contain the digital suffix, the statistics are obtained when the SAD is calculated and the OBJ region is searched for the first time based on the frame reference algorithm or background algorithm.
[15:0]	RO	obj_cnt	Number of detected OBJ regions.

MDU_MAX_OBJ_SIZE

MDU_MAX_OBJ_SIZE is a maximum OBJ region readback register.

Offset Address	Register Name	Total Reset Value
0x00A0	MDU_MAX_OBJ_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_obj_size																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	max_obj_size	Maximum size of the OBJ region. This value is used to detect video occlusion. The value is in the unit of pixel. The software calculates the percentage of OBJ regions based on this value and compares the value with the size threshold of the OBJ region. If the value is greater than the threshold, the frame occlusion is considered, and the subsequent frames for detecting video occlusion are not used to refresh the background. In addition, the system checks whether the size of the OBJ region is greater than the threshold for consecutive times. If the occlusion time is greater than the time threshold, video occlusion is considered, and an alarm is generated.

MDU_TOTAL_OBJ_SIZE

MDU_TOTAL_OBJ_SIZE is an all OBJ region information readback register.

Offset Address	Register Name	Total Reset Value
0x00A4	MDU_TOTAL_OBJ_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	total_obj_size																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	total_obj_size	Total size of all OBJ regions. This value is used to detect whether a camera is sprayed. The working principle is the same as that of the max_obj_size field. The MDU adds the sizes of all OBJ regions. The size is in the unit of pixel. The size of each OBJ region is calculated as follows: number of 4x4 macroblocks x 16 **NOTE** • In some cases, the OBJ regions may overlap, and the total size of OBJ regions may be greater than the size of the original picture. • Based on the 4x4 macroblock, the height and width of each OBJ region are calculated as follows: Width = (Horizontal coordinate of the right point – Horizontal coordinate of the left point) + 1 Height = (Vertical coordinate of the bottom point – Vertical coordinate of the top point) + 1

MDU_MOVE_PIX_CNT

MDU_MOVE_PIX_CNT is a motion pixel statistics register for an entire frame.

Offset Address	Register Name	Total Reset Value
0x00A8	MDU_MOVE_PIX_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	move_pix_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	move_pix_cnt	Number of motion pixels of an entire frame. This value can be used to detect video occlusion. The working principle is the same as that of the max_obj_size field. Note: The value of this register is based on pixels. Therefore, the register value may be different from the value of total_obj_size.

MDU_OBJ_CNT1

MDU_OBJ_CNT1 is an OBJ region information readback register based on the background.

Offset Address	Register Name	Total Reset Value
0x00AC	MDU_OBJ_CNT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_obj_index1																obj_cnt1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	max_obj_index1	Index of the maximum OBJ region based on the background. The registers with the suffix 1 indicate statistics registers. The statistics are obtained when the background algorithm is used and the SAD is calculated and the OBJ region is searched for the second time.
[15:0]	RO	obj_cnt1	Number of detected OBJ regions based on the background.

MDU_MAX_OBJ_SIZE1

MDU_MAX_OBJ_SIZE1 is a maximum OBJ region readback register based on the background.

Offset Address	Register Name	Total Reset Value
0x00B0	MDU_MAX_OBJ_SIZE1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_obj_size1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	max_obj_size1	Maximum size of the OBJ region based on the background. This value is used to detect video occlusion, and is in the unit of pixel. The software calculates the percentage of OBJ regions based on this value and compares the value with the size threshold of the OBJ region. If the value is greater than the threshold, the frame occlusion is considered, and the subsequent frames for detecting video occlusion are not used to refresh the background. In addition, the system checks whether the size of the OBJ region is greater than the threshold for consecutive times. If the occlusion time is greater than the time threshold, video occlusion is considered, and an alarm is generated.

MDU_TOTAL_OBJ_SIZE1

MDU_TOTAL_OBJ_SIZE1 is a all OBJ region information readback register based on the background.

Offset Address	Register Name	Total Reset Value
0x00B4	MDU_TOTAL_OBJ_SIZE1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	total_obj_size1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	total_obj_size1	Sum of the sizes of all OBJ regions based on the background. This value is used to detect whether a camera is sprayed. The working principle is the same as that of the max_obj_size field.

MDU_MOVE_PIX_CNT1

MDU_MOVE_PIX_CNT1 is a motion pixel statistics register for an entire frame based on the background.

Offset Address	Register Name	Total Reset Value
0x00B8	MDU_MOVE_PIX_CNT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	move_pix_cnt1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	move_pix_cnt1	Number of motion pixels of an entire frame based on the background. This value can be used to detect video occlusion. The working principle is the same as that of the max_obj_size field.

Contents

Figures

Tables

9 Intelligent Video Engine

9.1 Overview

The intelligent video engine (IVE) is a hardware acceleration module in the intelligent analysis system. It implements various functions such as template filter, dilate, erode, image sobel and canny edge extraction, subtract, AND, and OR of images, thresh, integral and histogram statistics. The IVE reads and writes data and linked list node parameters through the AXI Master bus interface. It configures the registers required for the IVE startup and obtains the register status information during IVE running through the APB Slave bus interface.

9.2 Features

The IVE has the following features:

- Supports the DMA.
- Supports 3x3 template filter.
- Supports color space conversion (CSC) from YUV to RGB.
- Supports the compound function of 3x3 template filter + CSC from YUV to RGB.
- Supports gradient computation of operators (such as sobel and scharr) in X/Y direction.
- Supports the computation of canny gradient magnitude and direction.
- Supports 3x3 erode.
- Supports 3x3 dilate.
- Supports image thresh.
- Supports the AND operation of two images.
- Supports subtract of two images.
- Supports the OR operation of two images.
- Supports integral computation.
- Supports histogram statistics.
- Supports a maximum running frequency of 300 MHz.
- Supports independent soft reset.
- Supports 64-bit AXI Master bus and 32-bit APB Slave bus.
- Supports linked list interrupts and node interrupts.

- Supports the query mode.
- Supports gray images in input formats such as SP420 (semi-planar420) and SP422 (semi-planar422).
- Supports gray images in output formats such as SP420, SP422, RGBpackage, and RGBplanar.
- Supports non 8-byte alignment of read/write address of some operators.

9.3 Operating Mode

9.3.1 Hardware Usage

To use the IVE in query mode, perform the following steps:

Step 1 Create task linked lists in the memory.

Step 2 Configure the internal registers LIST_POINTER and INT_EN of the IVE.

Step 3 Configure the internal register IVE_START of the IVE to start the IVE.

Step 4 Check the status of IVE_STATUS during the running to obtain the running status of the IVE. If the IVE is idle, linked list tasks are complete. To continue using the IVE, repeat Step 1 through Step 3.

----End

To use the IVE in interrupt mode, perform the following steps:

Step 1 Create task linked lists in the memory.

Step 2 Configure the internal registers LIST_POINTER and INT_EN of the IVE.

Step 3 Configure the internal register IVE_START of the IVE to start the IVE.

Step 4 In the interrupt service program, determine the interrupt type based on INT_STATUS and configure the internal register INT_RW of the IVE to clear the interrupt of INT_STATUS. Determine the status of the IVE based on IVE_STATUS. The status of IVE_STATUS is idle, indicating that linked list tasks are completed. Go back to Step 1 to start the next linked list operation.

----End

The IVE task linked list adopts the linked list node format at the fixed length and at fixed position. Each node is 8x8 bytes in size, and the number of linked list nodes can be any value.

Figure 9-1 shows the structure of a linked list node.

Figure 9-1 Structure of a linked list node of the IVE

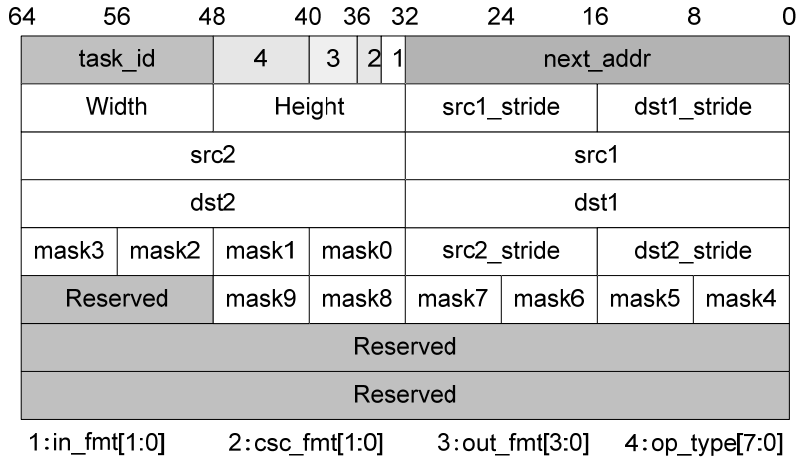


Table 9-1 describes the meanings of the parameters of the IVE linked list node.

Table 9-1 Parameter description of the IVE linked list node

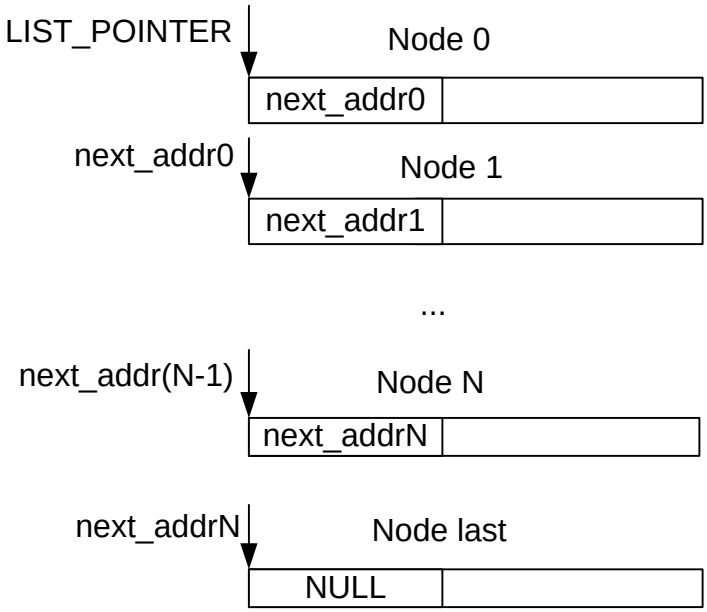
Parameter Register	Description
next_addr	Address of the next node in the memory. The value is 0x00000000, indicating the last node of the current linked list.
in_fmt	Input format of an image. 00: gray image 01: SP420 10: SP422 11: reserved
csc_fmt	CSC mode select. 00: BT601&BT656, ranging from 16 to 235. 01: BT701, ranging from 16 to 235. 10: BT601&BT656, ranging from 0 to 255. 11: BT701 ranging from 0 to 255.

Parameter Register	Description
out_fmt	Output format of an image. CSC: 0000: package 0001: planar Canny: 0000: Output the amplitude only. 0001: Output the amplitude and angle. Thresh: 0000: Set the value to maxvalue when it is greater than the threshold and minvalue when it is smaller than the threshold. 0001: Set the value to maxvalue when it is greater than the threshold and retain the value when it is smaller than the threshold. 0010: Retain the value when it is greater than the threshold and set the value to minvalue when it is smaller than the threshold. Subtract: 0000: Output the absolute difference value. 0001: Move one bit right and then output the difference value.
op_type	Operator type selected by the current node. 0x00: DMA 0x01: filter 0x02: CSC 0x03: filter+CSC 0x04: sobel 0x05: canny 0x06: dilate 0x07: erode 0x08: thresh 0x09: AND 0x0A: subtract 0x0B: OR 0x0C: integral 0x0D: histogram
task_id	Task ID of the current node.
dst1_stride	Output stride signal of destination address 1. Eight bytes are aligned.
src1_stride	Stride signal of source image 1. Eight bytes are aligned.
height	Actual height of the source image.

Parameter Register	Description
width	Actual width of the source image. When the input format is 420 or 422, the value is an even number.
src1	Start address of source image 1. Eight bytes are aligned for operators including the filter, CSC, filter+CSC, sobel, canny, dilate, erode, integral, and histogram.
src2	Start address of source image 2.
dst1	Start address of destination 1. Eight bytes need to be aligned for operators including the start address, filter, CSC, filter+CSC, sobel, canny, dilate, erode, integral, and histogram.
dst2	Start address of destination 2.
dst2_stride	Stride of destination address 2. Eight bytes need to be aligned.
src2_stride	Stride of source image 2. Eight bytes are aligned.
mask0	Template coefficient 00 or threshold of the thresh operator.
mask1	Template coefficient 01 or min_value of the thresh operator.
mask2	Template coefficient 02 or max_value of the thresh operator.
mask3	Template coefficient 10.
mask4	Template coefficient 11.
mask5	Template coefficient 12.
mask6	Template coefficient 20.
mask7	Template coefficient 21.
mask8	Template coefficient 22.
mask9	Sum of the filter operator coefficients.
reserved	Reserved bit.

Template coefficient: indicates the coefficient of the operation template used by 3x3 operators such as filter, filter+CSC, sobel, canny, dilate, and erode.

Figure 9-2 Schematic drawing of the IVE linked list



9.3.2 Interrupt

The IVE generates two types of interrupts:

- Interrupt over the completion of all nodes of the current linked list
- Interrupt over the completion of operations of the current node

9.3.3 Clock Reset

Clock Disable Policy

You can disable the input clock of the IVE to reduce the power consumption. Before disabling the IVE clock, ensure that the IVE is idle by checking the register IVE_STATUS. If IVE_STATUS[0] is 0, the IVE is idle. The configuration of the IVE register is not affected by the clock disable policy. You need to enable the clock before operating internal registers of the IVE.

Clock Reset Policy

The IVE must be reset independently at a specific time; otherwise, bus exceptions may occur. The IVE can be reset independently only when the status register IVE_STATUS of the IVE is idle.

When the system is reset, all internal registers of the IVE are cleared.

9.3.4 Input and Output Data Formats

9.3.4.1 Storage Sequence

In the following descriptions, the data storage sequence is the storage sequence of data in the memory of the little endian system. For convenient description, word and double word are uniformly used as storage units. In actual applications, different operators have special requirements on data storage alignment formats. For details, see section 9.3.4.2 "Functions."

Figure 9-3 Storage of pixels in the memory when the data format is SemPlanar YCbCr422

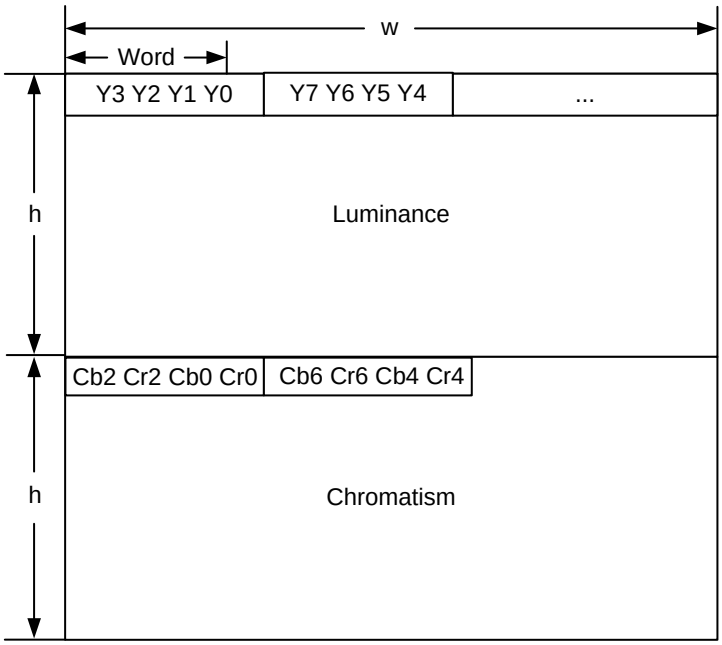


Figure 9-4 Storage of pixels in the memory when the data format is SemPlanar YCbCr420

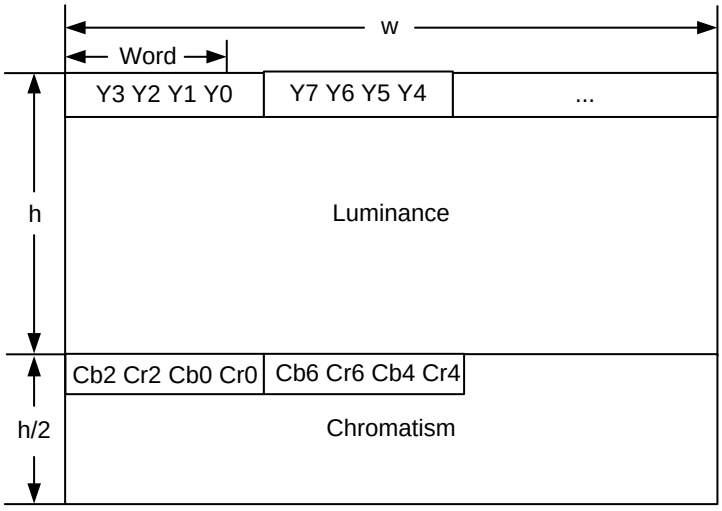


Figure 9-5 Storage of pixels in the memory when the data format is gray image

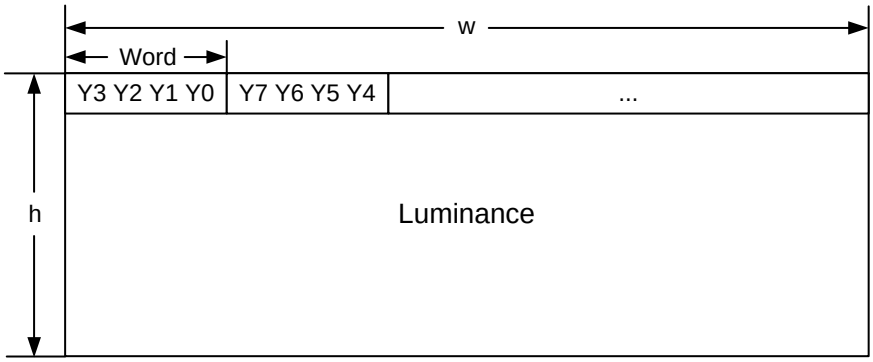


Figure 9-6 Storage of pixels in the memory when the data format is RGB package

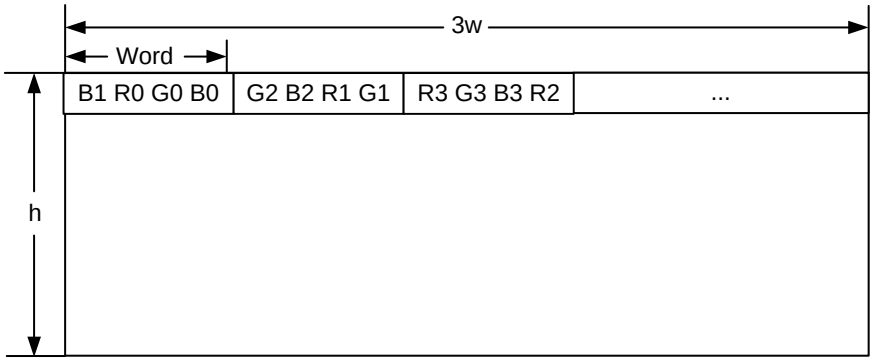


Figure 9-7 Storage of pixels in the memory when the data format is RGB planar

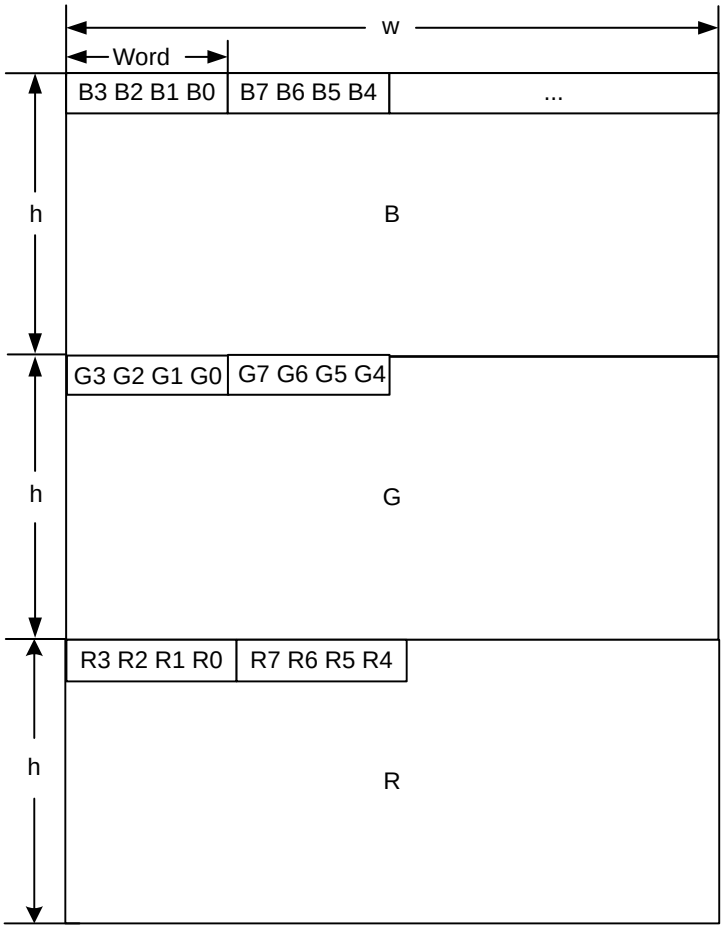


Figure 9-8 Storage of output results in the memory for the sobel operator

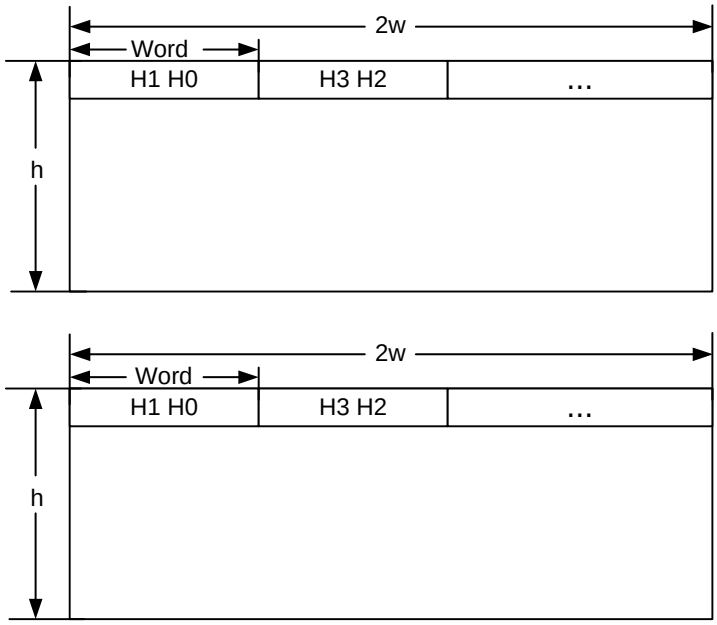


Figure 9-9 Storage of results in the memory for the canny operator

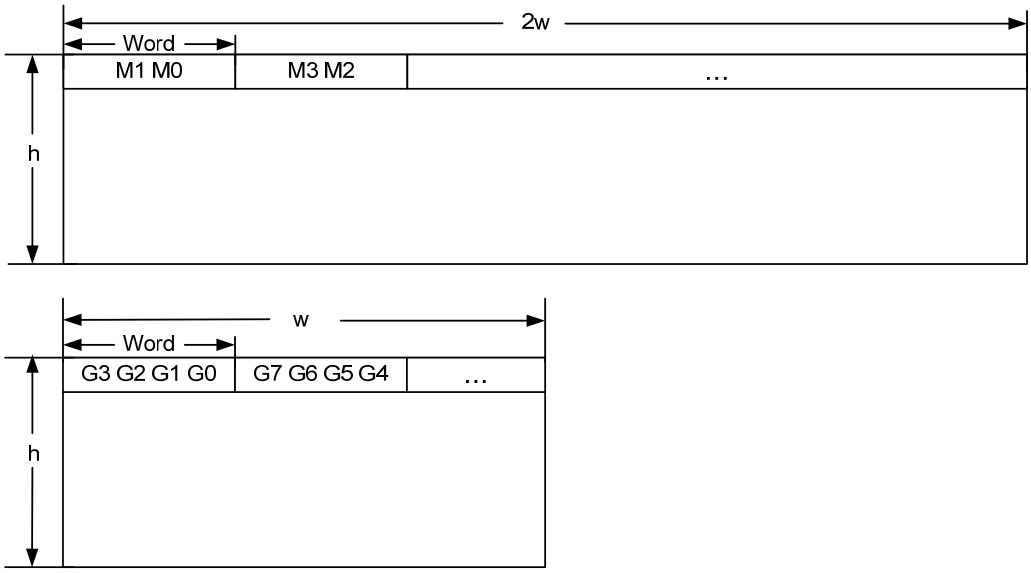


Figure 9-10 Storage of output results in the memory for the integral operator (INTEGRAL_OUT)

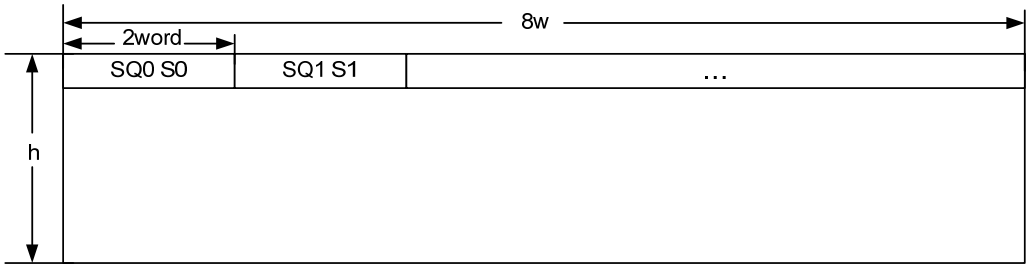
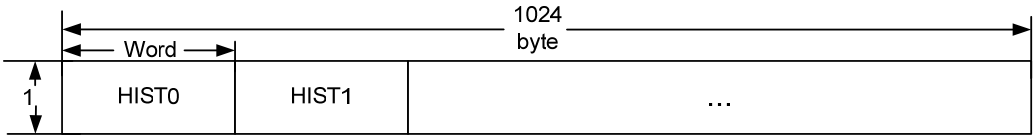


Figure 9-11 Storage of output results in the memory for the histogram operator (HIST_OUT)



9.3.4.2 Functions

The stride of all operators of the IVE needs to meet the following conditions:

When $((src\%8) == 0) \,\&\, \&((width\%8) == 0)$:

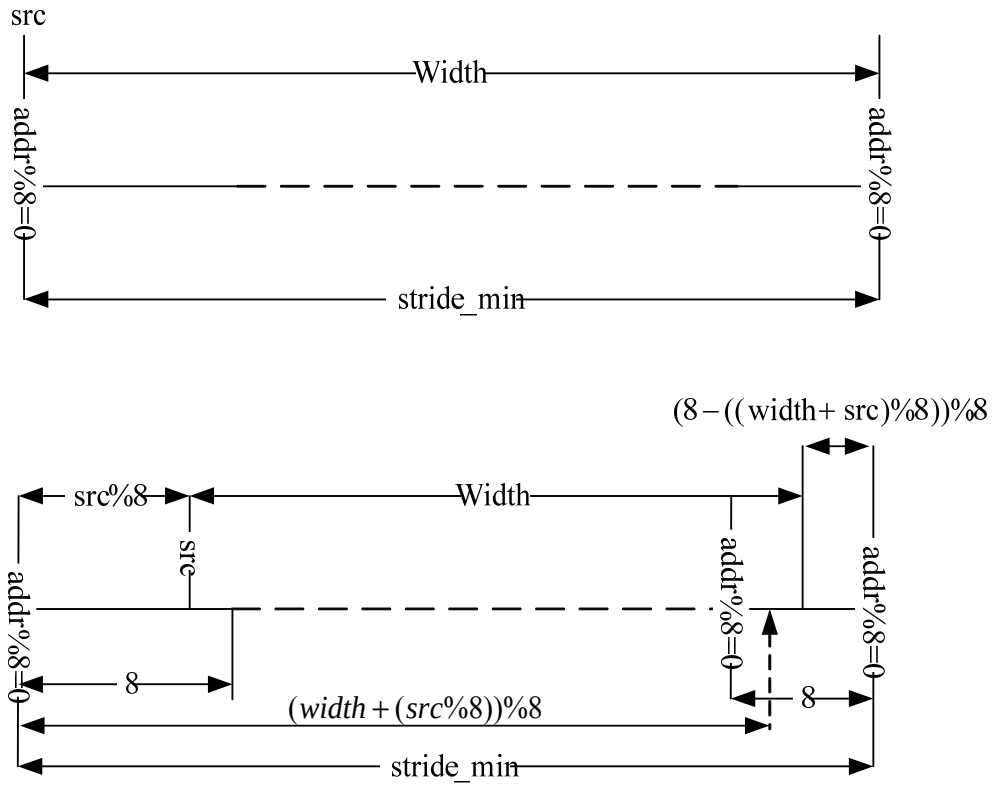
$$\begin{cases} stride \geq width \\ stride\%8 = 0 \end{cases}$$

Else:

$$\begin{cases} \{(8 - ((width + (src\%8))\%8)) + (src\%8) + width\} \leq stride \\ stride\%8 = 0 \end{cases}$$

% indicates the mod operation. See Figure 9-12.

Figure 9-12 Mod operation when the stride of the operator uses the minimum value



DMA

DMA is used to fast transfer data from the rectangular image area. In DMA mode, source data is directly transferred to the target area to overwrite the data in the target area through the internal fast channel.

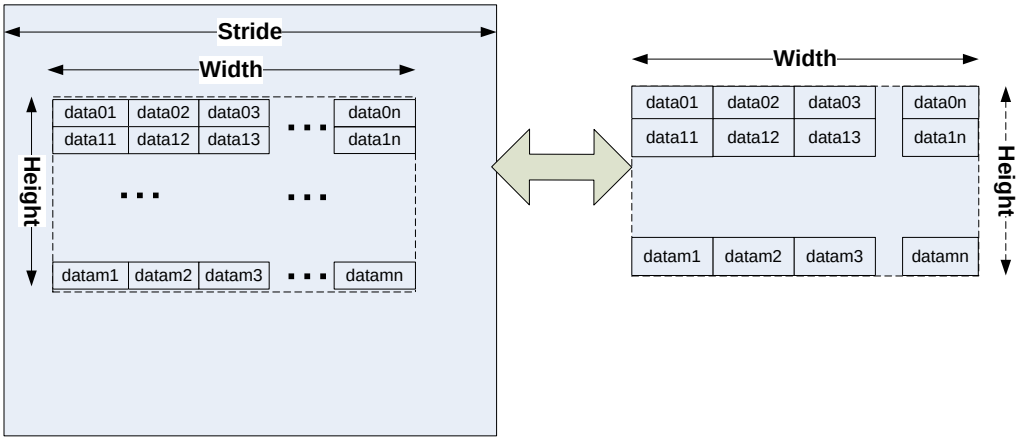
Image resolution: 32x1 to 1920x1080

Address alignment mode: Bytes of the input and output addresses need to be aligned.

Input/output format: gray image -> gray image

Usage method: Set op_type of the node in the linked list to 0x00.

Figure 9-13 Application of DMA data transfer (1)



3×3 Template Filter

This function is used to filter a source image using a 3x3 template and then output the image.

Image resolution: 64x64 to 1920x1024

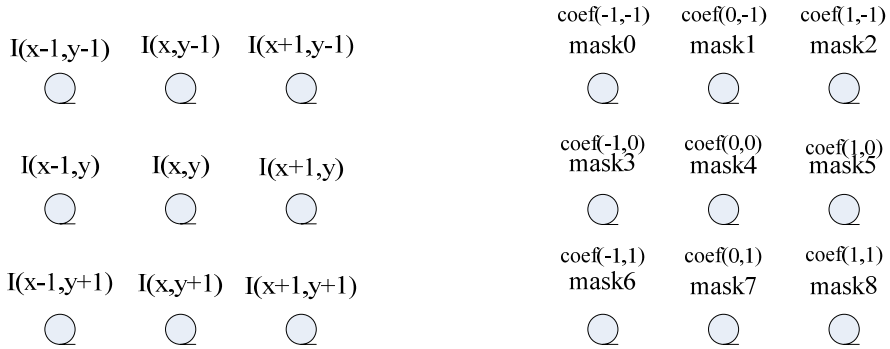
Address alignment mode: Eight bytes of the input and output addresses need to be aligned.

Input/output format: gray image -> gray image; SP420 -> SP420; SP422 -> SP422

Methods:

- Set op_type to 0x1.
- Set the input format.
- Set coefficients mask0, mask1, ..., mask9. The value range of mask0–mask8 is [–128, +127], and the value range of mask9 is [0, 10].

Figure 9-14 Computation formula for 3x3 template filter



$$Iout(x,y) = \left\{ \sum_{-2<j<2} \sum_{-2<i<2} I(x+i, y+j) \bullet coef(i,j) \right\} >> mask9$$

CSC

CSC from YUV to RGB is supported.

Image resolution: 64x64 to 1920x1080

Address alignment mode: Eight bytes of the input and output addresses need to be aligned.

Input/output format: SP420 -> RGB package; SP420 -> RGB planar; SP422 -> RGB package; SP422 -> RGB planar

Methods:

- Set op_type of the linked list node to 0x02.
- Set in_fmt of the linked list node:
  01: 420
  10: 422
- Set out_fmt of the linked list node:
  0000: package
  0001: planar
- Set csc_fmt of the linked list node:
  00: BT601&BT656 (16–235)
  01: BT709 (16–235)
  10: BT601&BT656 (0–255)
  11: BT709 (0–255)

When csc_fmt is 0 or 1, CSC is video conversion from YUV to RGB. The output meets the following condition: 16 ≤ R, G, B ≤ 235.

When csc_fmt is 2 or 3, CSC is image conversion from YUV to RGB. The output meets the following condition: 0 ≤ R, G, B ≤ 255.

The input and output requirements for the video matrix of the conversion from YUV to RGB are as follows:

- 16 ≤ Y ≤ 235
- 16 ≤ Cb, Cr ≤ 240
- 16 ≤ R, G, B ≤ 235

Table 9-2 describes the video matrix algorithm for the conversion from YUV to RGB.

Table 9-2 Video matrix of the conversion from YCbCr to RGB (BT.601)

Method of Calculating the Floating Point for the CSC from RGB to YCbCr:									
R	=	1	×(Y)	+	0.0	×(Cb-128)	+	1.371	×(Cr-128)
G	=	1	×(Y)	–	0.336	×(Cb-128)	–	0.698	×(Cr-128)
B	=	1	×(Y)	+	1.732	×(Cb-128)	+	0.0	×(Cr-128)

Table 9-3 Video matrix of the conversion from YCbCr to RGB (BT.709)

Method of Calculating the Floating Point for the CSC from RGB to YCbCr:									
R	=	1	×(Y)	+	0.0	×(Cb-128)	+	1.540	×(Cr-128)
G	=	1	×(Y)	–	0.183	×(Cb-128)	–	0.459	×(Cr-128)
B	=	1	×(Y)	+	1.816	×(Cb-128)	+	0.0	×(Cr-128)

The input and output requirements for the image matrix of the conversion from YUV to RGB are as follows:

- $16 \leq Y \leq 235$
- $16 \leq U, V \leq 240$
- $0 \leq R, G, B \leq 255$

Table 9-4 describes the image matrix algorithm for the conversion from YUV to RGB.

Table 9-4 Image matrix of the conversion from YCbCr to RGB (BT.601)

Method of Calculating the Floating Point for the CSC from RGB to YCbCr:									
R	=	1.164	×(Y-16)	+	0.0	×(Cb-128)	+	1.596	×(Cr-128)
G	=	1.164	×(Y-16)	–	0.391	×(Cb-128)	–	0.813	×(Cr-128)
B	=	1.164	×(Y-16)	+	2.018	×(Cb-128)	+	0.0	×(Cr-128)

Table 9-5 Image matrix of the conversion from YCbCr to RGB (BT.709)

Method of Calculating the Floating Point for the CSC from RGB to YCbCr:									
R	=	1.164	×(Y-16)	+	0.0	×(Cb-128)	+	1.793	×(Cr-128)
G	=	1.164	×(Y-16)	–	0.213	×(Cb-128)	–	0.534	×(Cr-128)
B	=	1.164	×(Y-16)	+	2.115	×(Cb-128)	+	0.0	×(Cr-128)

3x3 Template Filter + CSC

This function is used to filter a source image as 3x3 template, perform CSC, and then output the image.

Image resolution: 64x64 to 1920x1024

Address alignment mode: Eight bytes of the input and output addresses need to be aligned.

Input/output format: SP420 -> RGB package; SP420 -> RGB planar; SP422 -> RGB package; SP422 -> RGB planar

Methods:

- Set op_type to 0x3.
- Set the CSC coefficient.
- Set the input format and output format.
- Set coefficients mask0, mask1, ..., mask9. The value range of mask0–mask8 is [–128, +127], and the value range of mask9 is [0, 10].

Sobel

Image resolution: 64x64 to 1920x1024

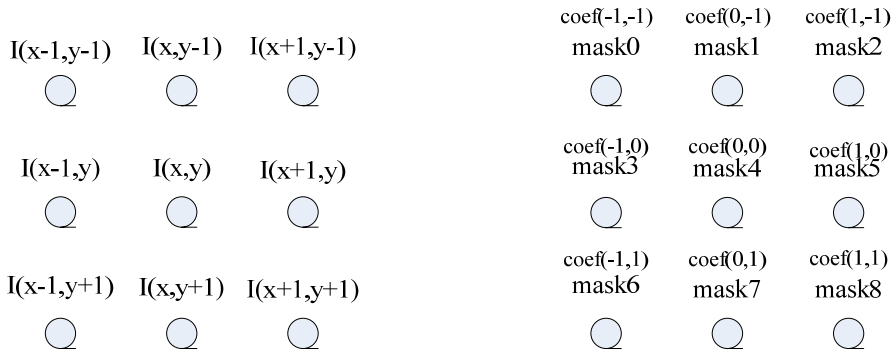
Address alignment mode: Eight bytes of the input and output addresses need to be aligned.

Input/output format: gray image -> SOBEL_OUT

Methods:

- Set op_type to 0x4.
- Set coefficients mask0, mask1, ..., mask8. The value range of mask0–mask8 is [–128, +127].

Figure 9-15 Sobel calculation formulas



$$Hout(x,y) = \sum_{-2<j<2} \sum_{-2<i<2} I(x+i, y+j) \bullet coef(i,j)$$

$$Vout(x,y) = \sum_{-2<j<2} \sum_{-2<i<2} I(x+i, y+j) \bullet coef(j,i)$$

Canny

Image resolution: 64x64 to 1920x1024

Address alignment mode: Eight bytes of the input and output addresses need to be aligned.

Input/output format: gray image -> CANNY_OUT1; gray image -> CANNY_OUT2

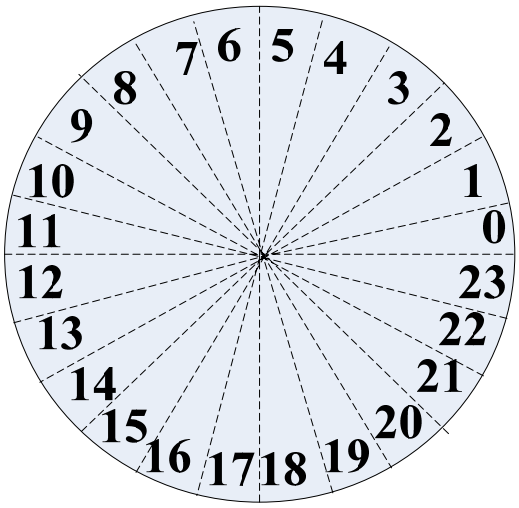
Methods:

- Set op_type to 0x5.
- Set the output format.

- Set coefficients mask0, mask1, ..., mask8. The value range of mask0–mask8 is [–128, +127].

Definition of amplitude: $Mag(x, y) = abs(Hout(x, y)) + abs(Vout(x, y))$

Figure 9-16 Definition of canny angle quantization



Output angle: $\theta = \left[\frac{\arctan(\frac{V}{H}) * 12}{\pi} \right]$

3x3 Dilate

Image resolution: 64x64 to 1920x1024

Address alignment mode: Eight bytes of the input and output addresses need to be aligned.

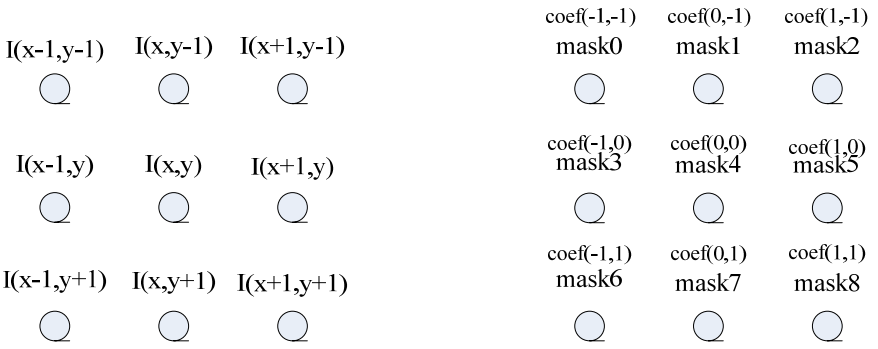
Input/output format: gray image -> gray image

Usage:

- Set op_type to 0x6.
- Set coefficients mask−mask8.
- The input/output data is 0 or 255. The mask value is 0 or 255.

Figure 9-17 shows the formula for calculating the 3x3 dilate operator.

Figure 9-17 Formula for calculating the 3x3 dilate operator



$$Iout(x,y) = f(I(x+(k\,\&\,3)-1, y+(k\%3)-1)\,\&\,coef((k\,\&\,3)-1,(k\%3)-1),|,0,8)$$

$$f(A_k,\Theta,c_{\min},c_{\max}) = A_{c_{\min}}\Theta A_{c_{\min+1}}\cdots\Theta A_{c_{\max}}$$

NOTE

In the preceding formula, | indicates bitwise OR operation, & indicates bitwise AND operation, and % indicates REM operation.

3x3 Erode

Image resolution: 64x64 to 1920x1024

Address alignment mode: Eight bytes of the input and output addresses need to be aligned.

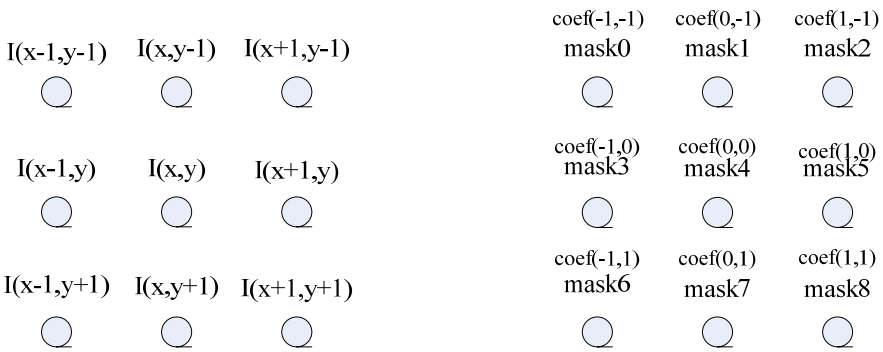
Input/output format: gray image -> gray image

Usage:

- Set op_type to 0x7.
- Set coefficients mask0−mask8.
- The input/output data is 0 or 255. The mask value is 0 or 255.

Figure 9-18 shows the formula for calculating the 3x3 erode operator.

Figure 9-18 Formula for calculating the 3x3 erode operator



$$Iout(x,y) = f(I(x+(k\,\&\,3)-1, y+(k\%3)-1)\,|\,coef((k\,\&\,3)-1,(k\%3)-1),\&,0,8)$$

$$f(A_k,\Theta,c_{\min},c_{\max}) = A_{c_{\min}}\Theta A_{c_{\min+1}}\cdots\Theta A_{c_{\max}}$$

NOTE

In the preceding formula, | indicates bitwise OR operation, & indicates bitwise AND operation, and % indicates REM operation.

Thresh

A fixed threshold is used to perform thresh operation on an image. Three modes are supported:

- mode=2: If the pixel value is above threshold, the pixel value is unchanged. Otherwise, the pixel value is minValue.

$$I_{out}(x,y)=\begin{cases}\min Value & (I(x,y)\le threshold)\\ I(x,y) & (I(x,y)>threshold)\end{cases}$$

- mode=1: If the pixel value is above threshold, the pixel value is maxValue. Otherwise, the pixel value is unchanged.

$$I_{out}(x,y)=\begin{cases}I(x,y) & (I(x,y)\le threshold)\\ \max Value & (I(x,y)>threshold)\end{cases}$$

- mode=0: If the pixel value is above threshold, the pixel value is maxValue. Otherwise, the pixel value is minValue.

$$I_{out}(x,y)=\begin{cases}\min Value & (I(x,y)\le threshold)\\ \max Value & (I(x,y)>threshold)\end{cases}$$

Image resolution: 64x64 to 1920x1080

Address alignment mode: Bytes of the input and output addresses need to be aligned.

Input/output format: gray image -> gray image

Usage:

- Set op_type of the linked list node to 0x08.
- Set linked list nodes mask0, mask1, and mask2 map to threshold, minValue, and maxValue respectively.

AND

CAUTION

The height and width of source image 2 must be consistent with those of source image 1. However, their stride can be different.

The AND operation is performed on the pixel value of source image 2 and source image 1, and then the data is transferred to the target area. The sizes of the two images are the same.

Image resolution: 64x64 to 1920x1080

Address alignment mode: Bytes of the input and output addresses need to be aligned.

Input/output format: gray image -> gray image

Usage: Set op_type of the node in the linked list to 0x09.

$$I_{out}(x, y) = I_{src1}(x, y) \& I_{src2}(x, y)$$

NOTE

In the preceding formula, & indicates bitwise AND operation.

Subtract

CAUTION

The height and width of source image 2 must be consistent with those of source image 1. However, their stride can be different.

The subtract operation is performed on the pixel value of source image 2 and source image 1, and then the data is transferred to the target area. The following two working modes are provided:

0000: Output the absolute difference value, that is, $dst[i, j] = abs(src1[i, j] - src2[i, j]$

0001: Move one bit right, and then output the difference value, with the sign bit reserved, that is, $dst[i, j] = (src1[i, j] - src2[i, j]) >> 1$

For example, if the pixel value in a certain position of image 1 is 0x23, and the pixel value in the corresponding position of image 2 is 0x40, the result is 0x1D in mode 0000 or 0xF1 in mode 0001.

Image resolution: 64x64 to 1920x1080

Address alignment mode: Bytes of the input and output addresses need to be aligned.

Input/output format: gray image -> gray image

Usage:

- Set op_type of the linked list node to 0x0a.
- Set out_fmt of the linked list node to 0x0000 or 0x0001.

OR

CAUTION

The height and width of source image 2 must be consistent with those of source image 1. However, their stride can be different.

The OR operation is performed on the pixel value of source image 2 and source image 1, and then the data is transferred to the target area.

Image resolution: 64x64 to 1920x1080

Address alignment mode: Bytes of the input and output addresses need to be aligned.

Input/output format: gray image -> gray image

Usage: Set op_type of the node in the linked list to 0x0b.

$$I_{out}(x,y) = I_{src1}(x,y) \mid I_{src2}(x,y)$$

NOTE

In the preceding formula, | indicates bitwise OR operation.

Integral

The output format of integral images for pixel values and for squared pixel values is 64 bytes. The integral image for pixel values occupies the lower 28 bits, and the integral image for squared pixel values occupies the upper 36 bits.

Image resolution: 64x64 to 1920x1080

Address alignment mode: Eight bytes of the input and output addresses need to be aligned.

Input/output format: gray image -> INTEGRAL_OUT

Usage: Set op_type of the node in the linked list to 0x0c.

$$I_{sum}(x,y) = \sum_{i\geq 0}^{i\leq x}\sum_{j\geq 0}^{j\leq y} I(i,j)$$

$$I_{sq}(x,y) = \sum_{i\geq 0}^{i\leq x}\sum_{j\geq 0}^{j\leq y} (I(i,j) \bullet I(i,j))$$

$$I_{out}(x,y) = (I_{sum}(x,y) \,\&\, 0\text{x}FFFFFFF) \mid (I_{sq}(x,y) << 28)$$

NOTE

In the preceding formulas, | indicates bitwise OR operation, & indicates bitwise AND operation, and << indicates left shift operation.

Histogram

In the 256-level histogram statistics, a gray image is input, and a 32-bit 256-level histogram statistic value is output.

Image resolution: 64x64 to 1920x1080

Address alignment mode: Eight bytes of the input and output addresses need to be aligned.

Input/output format: gray image -> HIST_OUT

Usage: Set op_type of the node in the linked list to 0x0d.

$$I_{out}(x) = \sum_i \sum_j ((I(i,j) == x)?1:0) \qquad x = 0 \ldots 255$$

9.4 Register Summary

Table 9-6 describes the IVE registers.

Table 9-6 Summary of IVE registers (base address: 0x205E_0000)

Offset Address	Register	Description	Page
0x0000	IVE_START	Start register	9-22
0x0004	INT_EN	Interrupt enable register	9-23
0x0008	INT_RW	Raw interrupt register	9-23
0x000C	INT_STATUS	Interrupt status register	9-24
0x0010	LIST_POINTER	Link table start address register	9-24
0x0014	IVE_STATUS	IVE working status register	9-25
0x0018	IVE_TASK_ID	Completed task ID register	9-25

9.5 Register Description

IVE_START

IVE_START is a start register.

Offset Address	Register Name	Total Reset Value
0x0000	IVE_START	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								ive_start
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	WO	ive_start	IVE start signal, active high.

INT_EN

INT_EN is an interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x0004	INT_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														list_int_en	node_int_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1]	RW	list_int_en	Link table interrupt enable. 0: disabled 1: enabled
[0]	RW	node_int_en	Node interrupt enable. 0: disabled 1: enabled

INT_RW

INT_RW is a raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x0008	INT_RW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														list_int_rw	node_int_rw
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.

[1]	RW	list_int_rw	Link table raw interrupt. After reading an interrupt through INT_STATUS, the software writes INT_RW to clear the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RW	node_int_rw	Node raw interrupt. After reading an interrupt through INT_STATUS, the software writes INT_RW to clear the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

INT_STATUS

INT_STATUS is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0x000C	INT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														list_int_status	node_int_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1]	RO	list_int_status	Link table interrupt status. The software determines whether a linked list interrupt is generated by reading this bit. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	node_int_status	Node interrupt status. The software determines whether a node interrupt is generated by reading this bit. 0: No interrupt is generated. 1: An interrupt is generated.

LIST_POINTER

LIST_POINTER is a linked list start address register.

Offset Address	Register Name	Total Reset Value
0x0010	LIST_POINTER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	link_table_header_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	link_table_header_addr	Address of the first node in the linked list.

IVE_STATUS

IVE_STATUS is an IVE working status register.

Offset Address	Register Name	Total Reset Value
0x0014	IVE_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															ive_working_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RO	ive_working_status	Current working status of the IVE. 0: idle 1: busy

IVE_TASK_ID

IVE_TASK_ID is a completed task ID register.

Offset Address	Register Name	Total Reset Value
0x0018	IVE_TASK_ID	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ive_task_id															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RO	ive_task_id	ID of a task that was just completed. If task IDs are incremental, all tasks before a specified task have been completed.

Contents

Figures

Tables

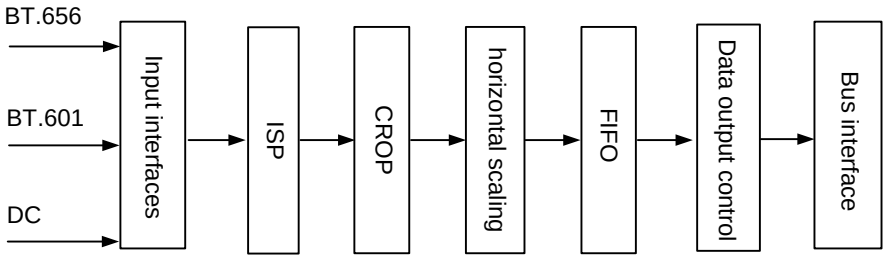
10 Video Interfaces

10.1 VICAP

10.1.1 Overview

The video capture (VICAP) module receives video data over the BT.656 interface, BT.601 interface, or digital camera (DC) interface, and stores the data in the specified addresses of the DDR. During this process, the VICAP module performs horizontal scaling on video data (or simple down sampling or scaling based on channels) and outputs video streams. The VICAP module has a built-in image signal processor (ISP) that can directly receive external raw data (bayer RGB data). Figure 10-1 shows the functional block diagram of the VICAP module.

Figure 10-1 Functional block diagram of the VICAP module



10.1.2 Features

The VICAP module has the following features:

- Supports the maximum input resolution of 1920x1080 or 1600x1200.
- Supports one external interface with the maximum bit width of 12 bits.
- Internally supports one port and processes 1-channel videos. Each channel supports interlaced and progressive input modes.
- Supports BT.656, BT.601, and DC timings.
- Supports SMPTE293M/ITU-R BT.1358 timing (480p/576p) and SMPTE 296M timing (720p).

- Provides a built-in ISP.
- Supports horizontal scaling down at most 15 times (integral multiple).
- Obtains data in a specified window.
- Supports mirror and flip.
- Supports the output storage modes of raw data or SPYCbCr 4:2:2.

10.1.3 Function Description

10.1.3.1 Typical Application

The VICAP module captures video data in multiple input timings and stores the captured data in the DDR. By using different function modes configured by the system, the VICAP module can connect to different external VI interfaces, supporting multiple external input devices.

It uses 17 pins, one clocks, four external sync signals (multiplexed with other pins), and 12 data lines. It also provides one port and one channel. The port parses the timings of an interconnected chip, and the channel processes 1-channel video signals.

The VICAP module supports the following typical input modes:

- 1-channel 720p
- 1-channel raw data

Mixed Timing Input

The interconnected chips are independent of each other, and they can work together in any form.

10.1.3.2 Function Principle

ITU-R BT. 656 YCbCr4:2:2

1. Horizontal timing

Based on the ITU-R BT.656 protocol, sync signals are included in data streams. The special bytes start of active video (SAV) and end of active video (EAV) indicate the start and end of active line data respectively. In video streams, the header of the timing reference code indicates that the following byte is SAV or EAV. The timing reference code consists of FF 00 00. FF and 00 indicate the reserved bytes of the image encoding data, that is, non-image data. Table 10-1 shows the format of the ITU-R BT.656 line data.

Table 10-1 Format of the ITU-R BT.656 YCbCr 4:2:2 line data

Timing Reference Code				Line Blanking Area					Timing Reference Code				YCbCr 4:2:2 with 720 Valid Pixels						
FF	00	00	EAV	80	10	…	80	10	FF	00	00	SAV	Cb0	Y0	Cr0	Y1	…	Cr718	Y719

The difference between SAV and EAV depends on the special bit H. Both SAV and EAV include vertical blanking bit V and field indicator bit F. Table 10-2 describes the formats of SAV and EAV.

Table 10-2 Formats of SAV and EAV

Bit7	Bit6 (F)	Bit5 (V)	Bit4 (H)	Bit[3:0] (P3–P0)
Fixed value 1	Field indicator bit 1st field: F = 0 2nd field: F = 1	Vertical blanking bit VBI: V = 1 Active video: V = 0	SAV: H = 0 EAV: H = 1	Check bits

The ITU-R BT.656 protocol defines valid SAV and EAV by using eight valid reserved bits. Four check bits are used to correct 1-bit error and detect 2-bit errors. Table 10-3 describes the valid SAV and EAV values.

Table 10-3 Valid SAV and EAV values

Code	Binary Value	Field Number	Vertical Blanking Interval or Not
SAV	10000000	1	No
EAV	10011101	1	No
SAV	10101011	1	Yes
EAV	10110110	1	Yes
SAV	11000111	2	No
EAV	11011010	2	No
SAV	11101100	2	Yes
EAV	11110001	2	Yes

The four valid reserved bits including P0, P1, P2, and P3 provide the error correction function. They are determined by the F, V, and H bits, as shown in Table 10-4.

Table 10-4 ITU-R BT.656 correction codes

F	V	H	P3	P2	P1	P0
0	0	0	0	0	0	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	0
1	0	0	0	1	1	1

F	V	H	P3	P2	P1	P0
1	0	1	1	0	1	0
1	1	0	1	1	0	0
1	1	1	0	0	0	1

NOTE

- P0 = F^V^H
- P1 = F^V
- P2 = F^H
- P3 = V^H

2. Vertical timing

The positions of the vertical timings are determined by bit F and bit V of the timing reference codes SAV and EAV. Figure 10-2 shows the vertical timing of the 525-line 60 field/s video system and Figure 10-3 shows the vertical timing of the 625-line 50 field/s video system.

Figure 10-2 Vertical timing of the 525-line 60 fields/s video system

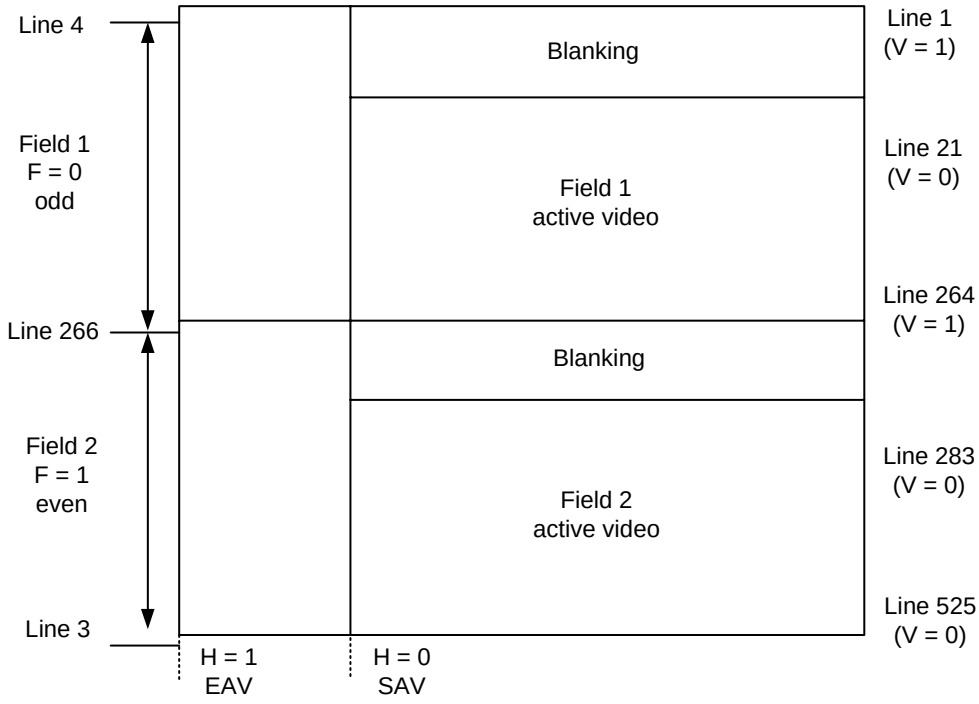
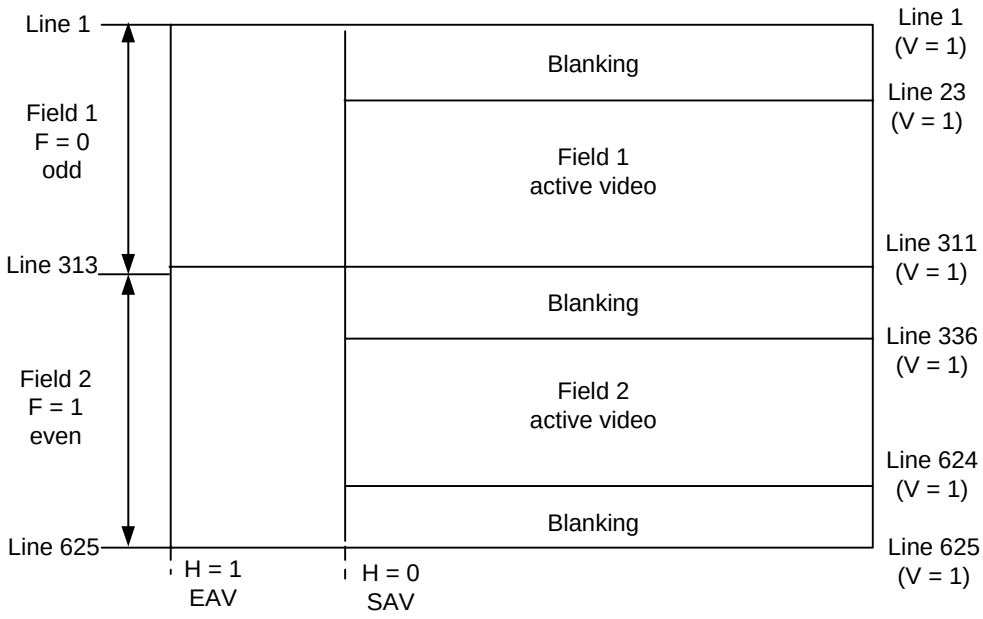


Figure 10-3 Vertical timing of the 625-line 50 fields/s video system



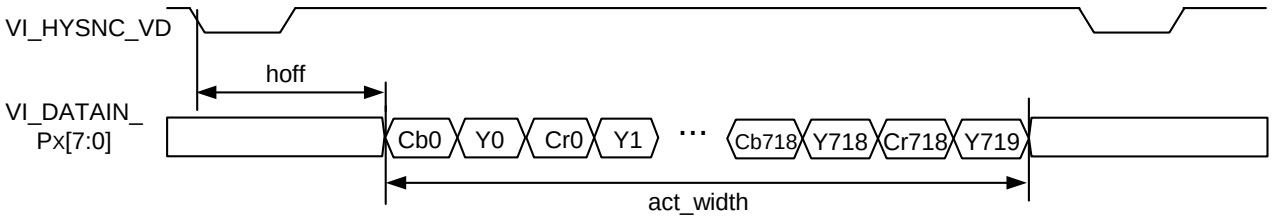
The VICAP module identifies vertical timings based on SAV and EAV regardless of the lines.

ITU-R BT.601 YCbCr4:2:2

1. Horizontal timing

The horizontal pulse indicates the start of a new line, as shown in Figure 10-4. After hoff clock cycles, an input signal passes the line front blanking area and enters the line active data area. The value of hoff is 244 in the NTSC525 line system or 264 in the PAL625 line system. After act_width clock cycles, the input signal passes the line active data area and enters the line back blanking area. The value of act_width can be set and the typical value is 720 or 704. In addition, the horizontal sync polarity is configurable.

Figure 10-4 ITU-R BT.601 horizontal timing



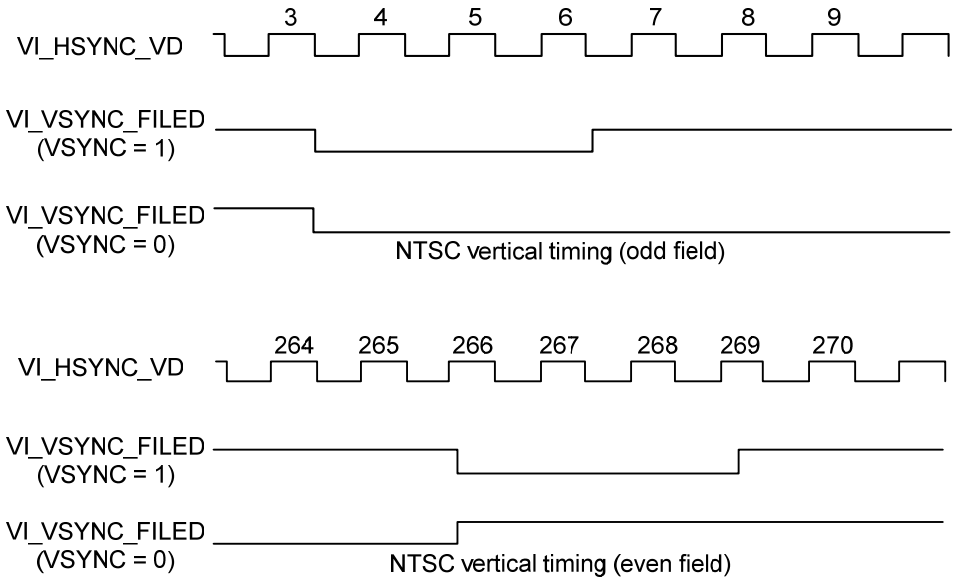
2. Vertical timing

According to the ITU-R BT.601 protocol, the VSYNC and FIELD signals are vertical sync signals. The VSYNC pulse or FIELD transition indicates the start of the odd field or even field. The VICAP module supports two types of vertical synchronization.

Figure 10-5 shows the NTSC vertical sync timings (525 lines) and Figure 10-6 shows the PAL vertical sync timings (625 lines). Where, VI_HSYNC_VD is the horizontal sync pulse, and

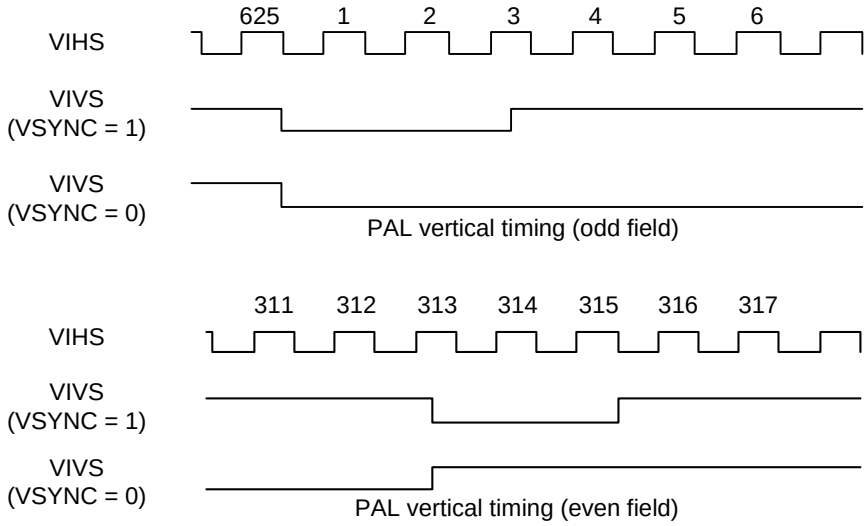
VI_VSYNC_FIELD is the vertical sync pulse when VSYNC is 1 or field sync signal when VSYNC is 0.

Figure 10-5 NTSC vertical sync timing



In NTSC interlaced scanning mode, the level of the vertical sync signal in field 1 becomes low at the start of line 4, retains low for three consecutive lines, and then becomes high at the start of line 7. The VICAP module receives 240-line data from line 22 to line 261. The level of the vertical sync signal in field 2 becomes low in the middle of line 266, retains low for three consecutive lines, and then becomes high in the middle of line 269. The VICAP module receives 240-line data from line 285 to line 524.

Figure 10-6 PAL vertical sync timings



In PAL interlaced scanning mode, the level of the vertical sync signal in field 1 becomes low at the start of line 1, retains low for 2.5 consecutive lines, and then becomes high in the middle of line 3. The VICAP module receives 288-line data from line 24 to line 310. The level of the vertical sync signal in field 2 becomes low in the middle of line 313, retains low for 2.5 consecutive lines, and then becomes high at the start of line 316. The VICAP module receives 288-line data from line 336 to line 623.

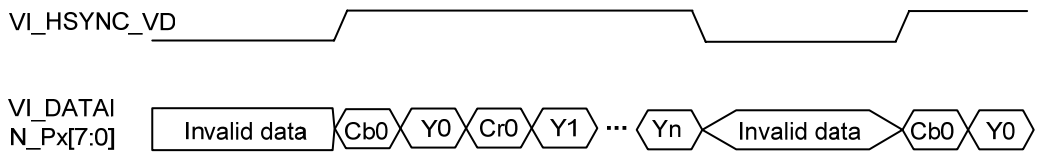
The preceding timings are typical BT.601 vertical timings. The following items are configurable: the number of lines from the start of the field to the active line, the number of field active lines, and vertical sync polarity.

DC Interface Timings

1. Horizontal timing

When a DC is connected to the VICAP module, VI_HSYNC_VD is the data valid signal. The polarity of this signal is configurable. Figure 10-7 shows the horizontal timing.

Figure 10-7 DC horizontal timing



2. Vertical timing

The VICAP module supports the vertical pulse timing and vertical line active timing, as shown in Figure 10-8 and Figure 10-9. In addition, the vertical sync polarity is configurable.

Figure 10-8 DC vertical pulse timing

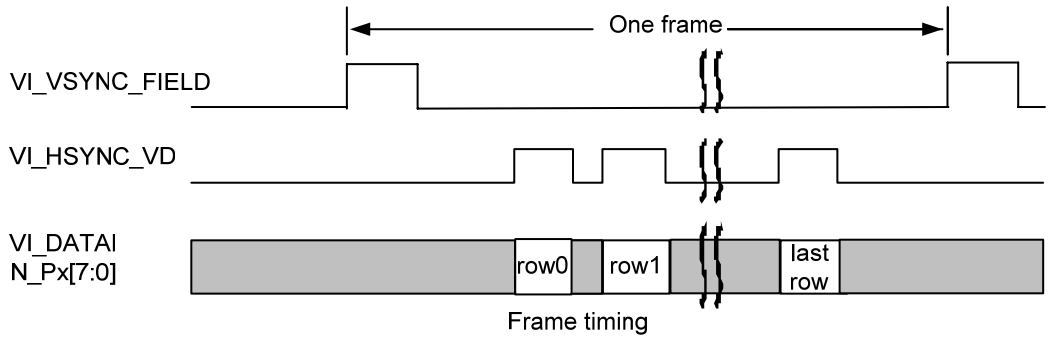
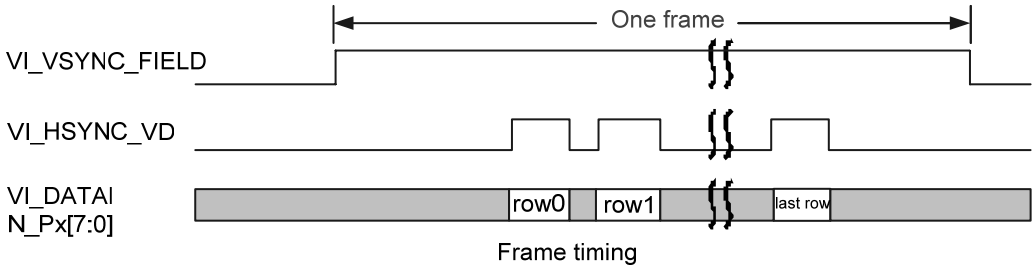


Figure 10-9 DC vertical line active timing

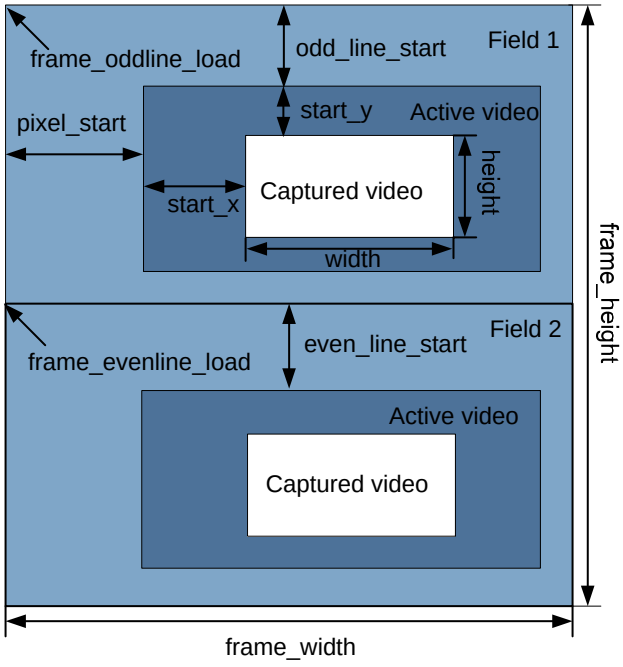


The VICAP module processes the preceding two timings in the same way. To be specific, the VICAP module considers the start of a frame after it detects a rising edge or a falling edge, and then detects the data active signal to check whether the current data is active.

10.1.3.3 Picture Cropping

The active video is shown in Figure 10-10, the actual view range, however, is within the active video range. That is, compared with the boundary of the active video, the boundary of the actual view is shrunk, which avoids the boundary effect.

Figure 10-10 Relationships between the active video area and the horizontal/vertical blanking areas



10.1.3.4 Picture Storage Modes

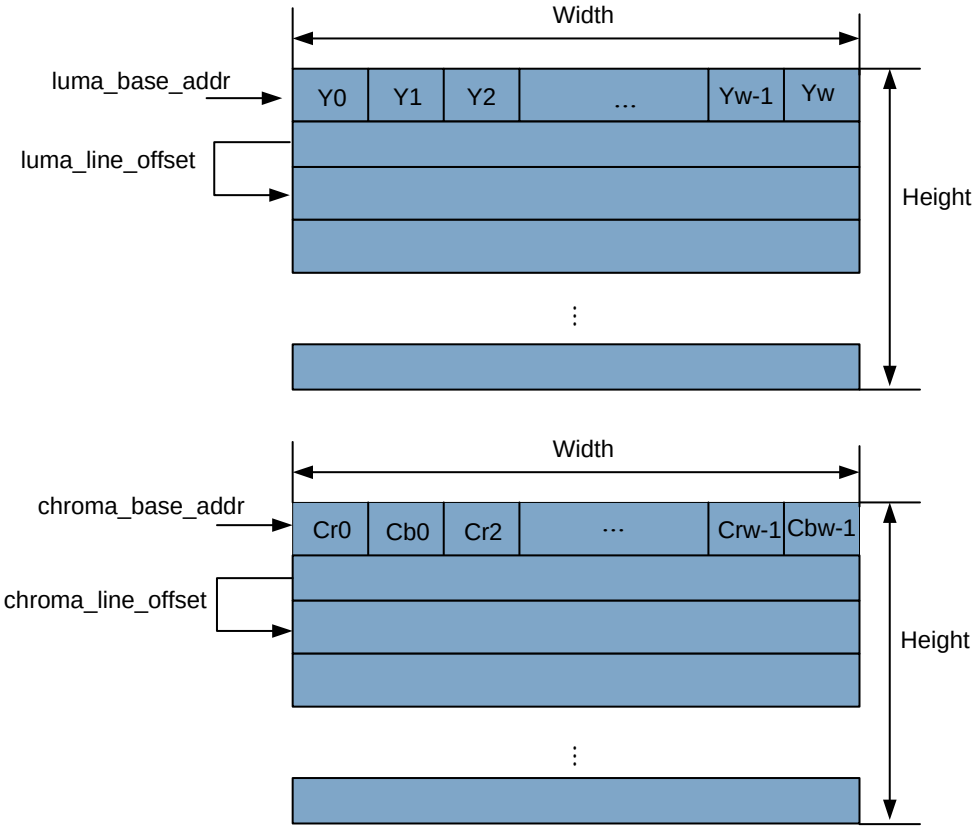
The picture storage modes are as follows:

- Semi-planar YCbCr storage mode

After setting a view area, the system stores the read data in semi-planar mode. That is, the luminance component and the chrominance component are stored in the luminance space and chrominance space of the DDR respectively.

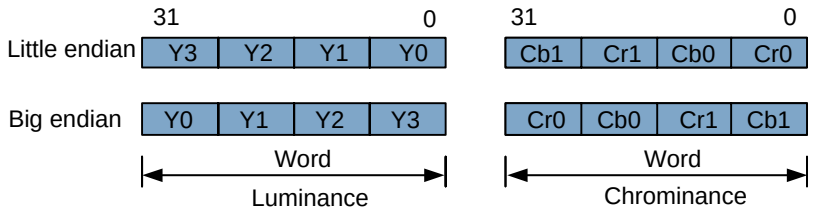
- For one line, the luminance component and chrominance component are stored separately and consecutively.
- For two consecutive lines, the components are stored based on the offset parameter. This parameter defines the storage stride between the start of two lines. The storage locations in the DDR of the luminance component and chrominance component are specified by the start address base_addr. Figure 10-11 shows the mode of storing the YCbCr4:2:2 data captured by the VICAP module.

Figure 10-11 YCbCr4:2:2 storage mode



In the DDR, data is stored by word (32 bits). Four 8-bit pixels constitute a 32-bit word in big endian mode or little endian mode. Figure 10-12 shows how to store the luminance components and chrominance component in big endian mode and little endian mode.

Figure 10-12 Big endian and little endian storage modes



The VICAP module supports only the DDR that stores data in little endian mode.

10.1.3.5 Mirror and Flip

When the pictures captures by the lens are reversed horizontal and vertically due to the reserve installation of the sensor, you can rectify this problem by using the mirror and flip functions of the VICAP module. The functions are implemented by writing reverse DDR address. Note that the start addresses of frames must be 12-bit-aligned.

10.1.4 Operating Mode

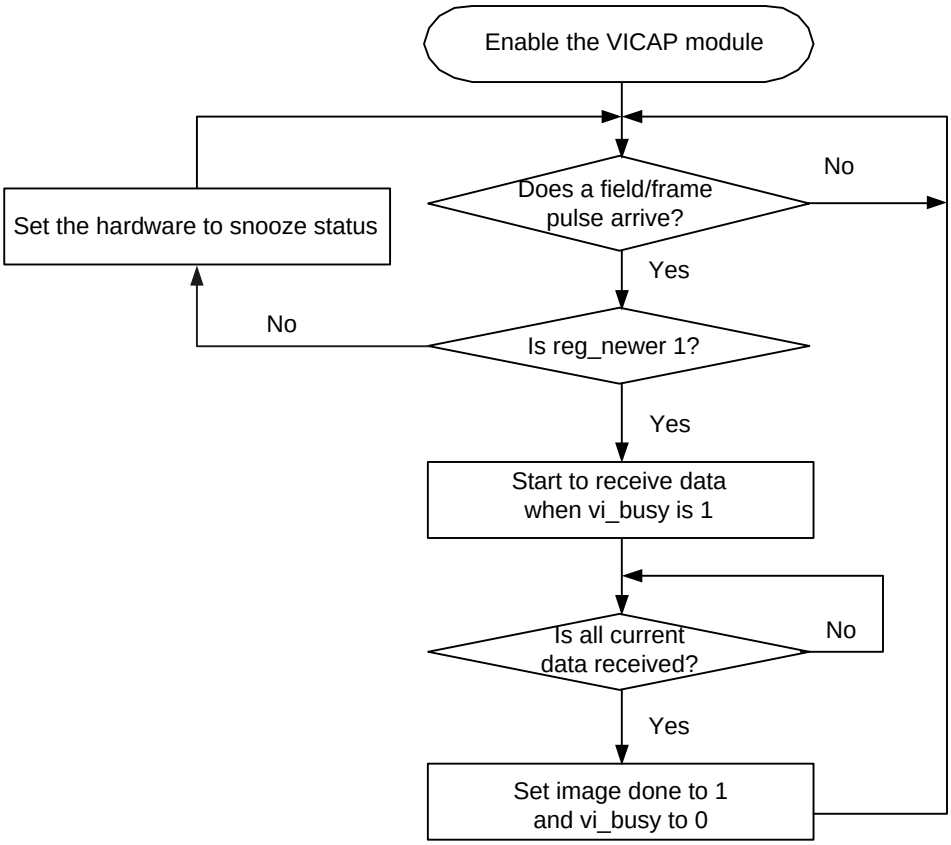
10.1.4.1 reg_newer Function of the VICAP Module

- Before enabling a channel of the VICAP module, the software must perform the following operations:
  - Configure the VICAP attribute register.
  - Write 1 to the reg_newer bit to inform the VICAP module that the current register is ready.
- After the VICAP module is enabled, the VICAP logic starts to work. When a field or a frame arrives:
  - If reg_newer is 0, the VICAP module does not receive data. However, it sets the hardware status to snooze and waits for the next field or frame.
  - If reg_newer is 1, the VICAP module starts to receive data, generates the register update interrupt reg_update_int, and sets the hardware status to busy.
- After all the current data is received, the busy status of the hardware is cleared. When the next field or frame arrives:
  - If reg_newer is 0, the data of the next field or frame is not received.
  - If reg_newer is 1, the data of the next field or frame is received.

10.1.4.2 VICAP Hardware Workflow

Figure 10-13 shows the VICAP hardware workflow.

Figure 10-13 VICAP hardware workflow

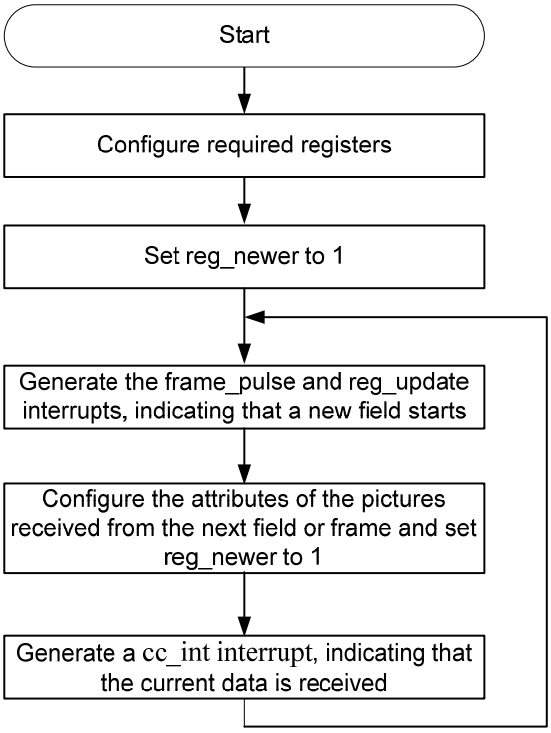


In BT.656, BT.601, or DC mode, after the data of a specified field or frame is received, the VICAP module checks the reg_newer bit when the next field or frame arrives. If reg_newer is 1, it indicates that software updates or confirms corresponding VICAP registers. In this case, the VICAP module automatically loads the register values configured by the software to the working register (this register is inaccessible to software), clears reg_newer, and starts to receive the data of the next field or frame. If reg_newer is 0, the VICAP module starts to receive data only when reg_newer 1 and a new field or frame arrives.

10.1.4.3 Software Configuration Workflow

Figure 10-14 shows the software configuration process in interrupt mode.

Figure 10-14 Software configuration workflow



In BT.656 or DC mod, the timing registers can be ignored; in BT.601 mode, the timing registers must be configured. The timing registers include the vertical sync timing register and horizontal sync register.

10.1.5 Register Summary

Table 10-5 describes the VICAP registers.

Table 10-5 Summary of the VICAP registers (base address: 0x2058_0000)

Offset Address	Register	Description	Page
0x0000	WK_MODE	WK_MODE is a global working configuration register.	10-18
0x0010	AXI_CFG	AXI_CFG is a bus configuration register.	10-19
0x0020	PT_SEL	PT_SEL is a port input select register.	10-19
0x0030	CH_SEL	CH_SEL is a channel input select register.	10-20
0x00E0	APB_TIMEOUT	APB_TIMEOUT is an APB timeout register.	10-20
0x00F0	VICAP_INT	VICAP_INT is an interrupt indicator register.	10-21

Offset Address	Register	Description	Page
0x00F8	VICAP_INT_MASK	VICAP_INT_MASK is an interrupt indicator register.	10-22
0x0100	PT_INTF_MOD	PT_INTF_MOD is a port mode register.	10-23
0x0110	PT_OFFSET0	PT_OFFSET0 is component 0 offset register.	10-23
0x0114	PT_OFFSET1	PT_OFFSET1 is component 1 offset register.	10-24
0x0118	PT_OFFSET2	PT_OFFSET2 is component 2 offset register.	10-24
0x0120	PT_BT656_CFG	PT_BT656_CFG is a BT.	10-25
0x0130	PT_UNIFY_TIMING_CFG	PT_UNIFY_TIMING_CFG is a timing configuration register.	10-26
0x0134	PT_GEN_TIMING_CFG	PT_GEN_TIMING_CFG is a timing restoration module configuration register.	10-28
0x0140	PT_UNIFY_DATA_CFG	PT_UNIFY_DATA_CFG is a data configuration register.	10-29
0x0144	PT_GEN_DATA_CFG	PT_GEN_DATA_CFG is a data generation module configuration register.	10-30
0x0148	PT_GEN_DATA_COEF	PT_GEN_DATA_COEF is a data generation module coefficient register.	10-32
0x014C	PT_GEN_DATA_INIT	PT_GEN_DATA_INIT is a data generation module initial value register.	10-32
0x0150	PT_YUV444_CFG	PT_YUV444_CFG is a YUV444 configuration register.	10-33
0x0160	PT_FSTART_DLY	PT_FSTART_DLY is a port fstart interrupt delay register.	10-33
0x0180	PT_INTF_HFB	PT_INTF_HFB is a horizontal front blanking width register.	10-34
0x0184	PT_INTF_HACT	PT_INTF_HACT is a horizontal active width register.	10-34
0x0188	PT_INTF_HBB	PT_INTF_HBB is a horizontal back blanking width register.	10-35
0x018C	PT_INTF_VFB	PT_INTF_VFB is a vertical front blanking width register.	10-35
0x0190	PT_INTF_VACT	PT_INTF_VACT is a vertical active width register.	10-35
0x0194	PT_INTF_VBB	PT_INTF_VBB is a vertical back blanking width register.	10-36

Offset Address	Register	Description	Page
0x0198	PT_INTF_VBFB	PT_INTF_VBFB is a vertical bottom front blanking width register.	10-36
0x019C	PT_INTF_VBACT	PT_INTF_VBACT is a vertical bottom active width register.	10-37
0x01A0	PT_INTF_VBBB	PT_INTF_VBBB is a vertical bottom back blanking width register.	10-37
0x01B0	PT_FLASH_CFG	PT_FLASH_CFG is a camera flash configuration register.	10-37
0x01C0	PT_FLASH_CYC0	PT_FLASH_CYC0 is flash timing 0 width register.	10-38
0x01C4	PT_FLASH_CYC1	PT_FLASH_CYC1 is flash timing 1 width register.	10-39
0x01D0	PT_SHUTTER_CYC0	PT_SHUTTER_CYC0 is shutter timing 0 width register.	10-39
0x01D4	PT_SHUTTER_CYC1	PT_SHUTTER_CYC1 is shutter timing 1 width register.	10-39
0x01D8	PT_SHUTTER_CYC2	PT_SHUTTER_CYC2 is shutter timing 2 width register.	10-40
0x01DC	PT_SHUTTER_CYC3	PT_SHUTTER_CYC3 is shutter timing 3 width register.	10-40
0x01E0	PT_STATUS	PT_STATUS is a port status register.	10-41
0x01E4	PT_BT656_STATUS	PT_BT656_STATUS is a BT.	10-41
0x01EC	PT_SIZE	PT_SIZE is an input size indicator register.	10-41
0x01F0	PT_INT	PT_INT is a channel interrupt indicator register.	10-42
0x01F8	PT_INT_MASK	PT_INT_MASK is a channel interrupt mask register.	10-43
0x1000	CH_CTRL	CH_CTRL is a channel control register.	10-43
0x1004	CH_REG_NEWER	CH_REG_NEWER is a capture control register.	10-44
0x1010	CH_ADAPTER_CFG	CH_ADAPTER_CFG is a timing adaptation register.	10-44
0x1080	CH_PACK_Y_CFG	CH_PACK_Y_CFG is a Y component control register for the PACK module.	10-45
0x1084	CH_PACK_Y_WIDTH	CH_PACK_Y_WIDTH is a Y component input width register for the PACK module.	10-46

Offset Address	Register	Description	Page
0x1090	CH_PACK_C_CFG	CH_PACK_C_CFG is a C component control register for the PACK module.	10-46
0x1094	CH_PACK_C_WIDTH	CH_PACK_C_WIDTH is a C component input width register for the PACK module.	10-47
0x10B0	CH_DES_Y_CFG	CH_DES_Y_CFG is a Y component configuration register for the DES module.	10-47
0x10B4	CH_DES_Y_FADDR	CH_DES_Y_FADDR is a Y component storage base address register.	10-48
0x10B8	CH_DES_Y_SIZE	CH_DES_Y_SIZE is a Y component storage size register.	10-48
0x10BC	CH_DES_Y_STRIDE	CH_DES_Y_STRIDE is a Y component stride register.	10-49
0x10C0	CH_DES_C_CFG	CH_DES_C_CFG is a C component configuration register for the DES module.	10-49
0x10C4	CH_DES_C_FADDR	CH_DES_C_FADDR is a C component storage base address register.	10-50
0x10C8	CH_DES_C_SIZE	CH_DES_C_SIZE is a C component storage size register.	10-50
0x10CC	CH_DES_C_STRIDE	CH_DES_C_STRIDE is a C component stride register.	10-51
0x10F0	CH_INT	CH_INT is a channel raw interrupt register.	10-51
0x10F8	CH_INT_MASK	CH_INT_MASK is a channel interrupt mask register.	10-53
0x1100	CH_CROP_CFG	CH_CROP_CFG is a crop enable register.	10-54
0x1104	CH_CROP_WIN	CH_CROP_WIN is a crop window register.	10-54
0x1110	CH_CROP0_START	CH_CROP0_START is a crop start position register for region 0.	10-54
0x1114	CH_CROP0_SIZE	CH_CROP0_SIZE is a crop size configuration register for region 0.	10-55
0x1200	CH_CSC_CFG	CH_CSC_CFG is a CSC configuration register.	10-55
0x1210	CH_CSC_COEF0	CH_CSC_COEF0 is CSC coefficient register 0.	10-56
0x1214	CH_CSC_COEF1	CH_CSC_COEF1 is CSC coefficient register 1.	10-56
0x1218	CH_CSC_COEF2	CH_CSC_COEF2 is CSC coefficient register 2.	10-57

Offset Address	Register	Description	Page
0x121C	CH_CSC_COEF3	CH_CSC_COEF3 is CSC coefficient register 3.	10-58
0x1220	CH_CSC_COEF4	CH_CSC_COEF4 is CSC coefficient register 4.	10-58
0x1230	CH_CSC_IN_DC0	CH_CSC_IN_DC0 is CSC input DC component register 0.	10-59
0x1234	CH_CSC_IN_DC1	CH_CSC_IN_DC1 is CSC input DC component register 1.	10-60
0x1238	CH_CSC_OUT_DC0	CH_CSC_OUT_DC0 is CSC output DC component register 0.	10-60
0x123C	CH_CSC_OUT_DC1	CH_CSC_OUT_DC1 is CSC output DC component register 1.	10-60
0x1300	CH_MSC_CFG	CH_MSC_CFG is a block mask configuration register.	10-61
0x1304	CH_MSC_WIN	CH_MSC_WIN is an occlusion window register.	10-62
0x1310	CH_BLOCK0_START	CH_BLOCK0_START is a mask start position register for block 0.	10-62
0x1314	CH_BLOCK1_START	CH_BLOCK1_START is a mask start position register for block 1.	10-63
0x1318	CH_BLOCK2_START	CH_BLOCK2_START is a mask start position register for block 2.	10-63
0x131C	CH_BLOCK3_START	CH_BLOCK3_START is a mask start position register for block 3.	10-64
0x1320	CH_BLOCK0_SIZE	CH_BLOCK0_SIZE is a mask size register for block 0.	10-64
0x1324	CH_BLOCK1_SIZE	CH_BLOCK1_SIZE is a mask size register for block 1.	10-65
0x1328	CH_BLOCK2_SIZE	CH_BLOCK2_SIZE is a mask size register for block 2.	10-65
0x132C	CH_BLOCK3_SIZE	CH_BLOCK3_SIZE is a mask size register for block 3.	10-66
0x1330	CH_BLOCK0_COLOR	CH_BLOCK0_COLOR is a filling color register for block 0.	10-66
0x1334	CH_BLOCK1_COLOR	CH_BLOCK1_COLOR is a filling color register for block 1.	10-67
0x1338	CH_BLOCK2_COLOR	CH_BLOCK2_COLOR is a filling color register for block 2.	10-67

Offset Address	Register	Description	Page
0x133C	CH_BLOCK3_COLOR	CH_BLOCK3_COLOR is a filling color register for block 3.	10-68
0x1400	CH_SKIP_Y_CFG	CH_SKIP_Y_CFG is a Y component skip configuration register.	10-68
0x1404	CH_SKIP_Y_WIN	CH_SKIP_Y_WIN is a Y component skip window register.	10-69
0x1410	CH_SKIP_C_CFG	CH_SKIP_C_CFG is a C component skip configuration register.	10-69
0x1414	CH_SKIP_C_WIN	CH_SKIP_C_WIN is a C component skip window register.	10-69
0x1500	CH_ZME_C_SSIZE	CH_ZME_C_SSIZE is a C component input size register for the zoom module.	10-70
0x1504	CH_ZME_C_DSIZE	CH_ZME_C_DSIZE is a C component output size register for the zoom module.	10-70
0x1510	CH_HFIR_C_SPH	CH_HFIR_C_SPH is a chrominance horizontal scaling parameter configuration register.	10-71
0x1514	CH_HFIR_C_OFFSET	CH_HFIR_C_OFFSET is a chrominance scaling horizontal offset register.	10-71
0x1520	CH_HFIR_C_COEF0	CH_HFIR_C_COEF0 is chrominance horizontal scaling coefficient register 0.	10-72
0x1524	CH_HFIR_C_COEF1	CH_HFIR_C_COEF1 is chrominance horizontal scaling coefficient register 1.	10-72
0x1528	CH_HFIR_C_COEF2	CH_HFIR_C_COEF2 is chrominance horizontal scaling coefficient register 2.	10-73
0x1600	CH_DITHER_CFG	CH_DITHER_CFG is a dither configuration register.	10-73
0x1604	CH_DITHER_COEF0	CH_DITHER_COEF0 is dither coefficient register 0.	10-74
0x1608	CH_DITHER_COEF1	CH_DITHER_COEF1 is dither coefficient register 1.	10-75
0x1610	CH_DITHER_Y_SIZE	CH_DITHER_Y_SIZE is a Y component input size register for the dither module.	10-75
0x1614	CH_DITHER_C_SIZE	CH_DITHER_C_SIZE is a C component input size register for the dither module.	10-75
0x1700	CH_VCDS_CFG	CH_VCDS_CFG is a chrominance vertical down sampling configuration register.	10-76

Offset Address	Register	Description	Page
0x1704	CH_VCDS_COEF	CH_VCDS_COEF is a chrominance vertical down sampling coefficient register.	10-76
0x1800	CH_HLDC_CFG	CH_HLDC_CFG is a horizontal lens distortion correction (HLDC) configuration register.	10-77
0x1804	CH_HLDC_SIZE	CH_HLDC_SIZE is an HLDC input picture size register.	10-77
0x1808	CH_HLDC_DEL	CH_HLDC_DEL is an HLDC output delay register.	10-78
0x1810	CH_HLDC_COEF0	CH_HLDC_COEF0 is HLDC coefficient register 0.	10-78
0x1814	CH_HLDC_COEF1	CH_HLDC_COEF1 is HLDC coefficient register 1.	10-79
0x1818	CH_HLDC_COEF2	CH_HLDC_COEF2 is HLDC coefficient register 2.	10-79
0x181C	CH_HLDC_COEF3	CH_HLDC_COEF3 is HLDC coefficient register 3.	10-80
0x1900	CH_CLIP_Y_CFG	CH_CLIP_Y_CFG is a Y component configuration register for the clip module.	10-80
0x1904	CH_CLIP_C_CFG	CH_CLIP_C_CFG is a C component configuration register for the clip module.	10-81
0x1A00	CH_SUM_Y	CH_SUM_Y is an input picture luminance statistics register.	10-81
0x100F0	ISP_INT	ISP_INT is an ISP interrupt indicator register.	10-82
0x100F8	ISP_INT_MASK	ISP_INT_MASK is an ISP interrupt mask register.	10-83

10.1.6 Register Description

WK_MODE

WK_MODE is a global working configuration register.

Offset Address	Register Name	Total Reset Value
0x0000	WK_MODE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							power_mode
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	power_mode	Clock mode. 0: The low-power mode is disabled. 1: The low-power mode is enabled.

AXI_CFG

AXI_CFG is a bus configuration register.

Offset Address	Register Name	Total Reset Value
0x0010	AXI_CFG	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							outstanding
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:4]	-	reserved	Reserved.
[3:0]	RW	m0_otd	Number of outstandings. The value range is 1−4.

PT_SEL

PT_SEL is a port input select register.

Offset Address	Register Name	Total Reset Value
0x0020	PT_SEL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															pt0_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	pt0_sel	Port input select. 0: external input 1: colorbar

CH_SEL

CH_SEL is a channel input select register.

Offset Address	Register Name	Total Reset Value
0x0030	CH_SEL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															ch0_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	ch0_sel	Channel input select. 0: ISP bypass 1: input from the ISP

APB_TIMEOUT

APB_TIMEOUT is an APB timeout register.

Offset Address	Register Name	Total Reset Value
0x00E0	APB_TIMEOUT	0x8000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved															timeout															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	Timeout enable. 0: disabled 1: enabled
[30:16]	-	reserved	Reserved.
[15:0]	RW	timeout	Timeout threshold. The unit is APB clock.

VICAP_INT

VICAP_INT is an interrupt indicator register.

Offset Address	Register Name	Total Reset Value
0x00F0	VICAP_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved							int_isp	reserved							int_pt0	reserved															int_ch0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	-	reserved	Reserved.
[24]	RO	int_isp	ISP interrupt indicator. 0: No interrupt is generated. 1: An interrupt is generated.
[23:17]	-	reserved	Reserved.
[16]	RO	int_pt0	Port 0 interrupt indicator. 0: No interrupt is generated. 1: An interrupt is generated.
[15:1]	-	reserved	Reserved.

Offset Address	Register Name	Total Reset Value
0x00F0	VICAP_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															int_pt0	reserved															int_ch0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RO	int_ch0	Channel 0 interrupt indicator. 0: No interrupt is generated. 1: An interrupt is generated.

VICAP_INT_MASK

VICAP_INT_MASK is an interrupt indicator register.

Offset Address	Register Name	Total Reset Value
0x00F8	VICAP_INT_MASK	0x0101_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved							int_isp_en	reserved							int_pt0_en	reserved															int_ch0_en
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:25]	-	reserved	Reserved.
[24]	RW	int_isp_en	ISP interrupt enable. 0: masked 1: enabled
[23:17]	-	reserved	Reserved.
[16]	RW	int_pt0_en	Port 0 interrupt enable. 0: masked 1: enabled
[15:1]	-	reserved	Reserved.

Offset Address	Register Name	Total Reset Value
0x00F8	VICAP_INT_MASK	0x0101_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved							int_isp_en	reserved							int_pt0_en	reserved															int_ch0_en
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[0]	RW	int_ch0_en	Channel 0 interrupt enable. 0: masked 1: enabled

PT_INTF_MOD

PT_INTF_MOD is a port mode register.

Offset Address	Register Name	Total Reset Value
0x0100	PT_INTF_MOD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																														mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	Port enable. 0: disabled 1: enabled
[30:1]	-	reserved	Reserved.
[0]	RW	mode	Timing mode. 0: external synchronization 1: BT.656

PT_OFFSET0

PT_OFFSET0 is component 0 offset register.

Offset Address	Register Name	Total Reset Value
0x0110	PT_OFFSET0	0xFFF0_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mask																rev	reserved											offset				
Reset	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	mask	Component 0 mask.
[15]	RW	rev	Whether the data line is reversed. 0: no 1: yes
[14:6]	-	reserved	Reserved.
[5:0]	RW	offset	Component 0 offset.

PT_OFFSET1

PT_OFFSET1 is component 1 offset register.

Offset Address	Register Name	Total Reset Value
0x0114	PT_OFFSET1	0xFFF0_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mask																rev	reserved											offset				
Reset	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	mask	Component 1 mask.
[15]	RW	rev	Whether the data line is reversed. 0: no 1: yes
[14:6]	-	reserved	Reserved.
[5:0]	RW	offset	Component 1 offset.

PT_OFFSET2

PT_OFFSET2 is component 2 offset register.

Offset Address	Register Name	Total Reset Value
0x0118	PT_OFFSET2	0xFFF0_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mask																rev	reserved											offset			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	mask	Component 2 mask.
[15]	RW	rev	Whether the data line is reversed. 0: no 1: yes
[14:6]	-	reserved	Reserved.
[5:0]	RW	offset	Component 2 offset.

PT_BT656_CFG

PT_BT656_CFG is a BT.656 configuration register.

Offset Address	Register Name	Total Reset Value
0x0120	PT_BT656_CFG	0x0000_0303

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																				field_inv	vsync_inv	hsync_inv	reserved				mode			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31]	RW	enable	BT.656 enable. 0: disabled 1: enabled
[30:11]	-	reserved	Reserved.
[10]	RW	field_inv	Field reverse control. 0: not reversed 1: reversed
[9]	RW	vsync_inv	vsync reverse control. 0: not reversed 1: reversed

Offset Address	Register Name	Total Reset Value
0x0120	PT_BT656_CFG	0x0000_0303

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																				field_inv	vsync_inv	hsync_inv	reserved				mode			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[8]	RW	hsync_inv	hsync reverse control. 0: not reversed 1: reversed
[7:4]	-	reserved	Reserved.
[3:0]	RW	mode	Mode select. mode[0] 0: hsync is not an active signal. 1: hsync is an active signal. mode[1] 0: The hsync output is active low. 1: The hsync output is active high. mode[3:2] 00: Component 0 is parsed. 01: Component 1 is parsed. 10: Component 2 is parsed. 11: reserved

PT_UNIFY_TIMING_CFG

PT_UNIFY_TIMING_CFG is a timing configuration register.

Offset Address	Register Name	Total Reset Value
0x0130	PT_UNIFY_TIMING_CFG	0x0008_2801

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					field_inv	field_sel		reserved				vsync_mode		vsync_inv	vsync_sel	reserved	hsync_mode		hsync_and		hsync_inv	hsync_sel		reserved				de_inv	de_sel		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:27]	-	reserved	Reserved.
[26]	RW	field_inv	Field reverse (level-1 processing for field). 0: not reversed 1: reversed
[25:24]	RW	field_sel	Field source select (level-0 processing for field). 00: input field 01: input vsync 10: detected based on the relationship between vsync and hsync 11: 0
[23:21]	-	reserved	Reserved.
[20:19]	RW	vsync_mode	vsync processing mode (level-2 processing for vsync). 00: No operation is performed. 01: Pulses are generated based on the rising edge. 10: Pulses are generated based on the rising and falling edge. 11: reserved
[18]	RW	vsync_inv	vsync reverse (level-1 processing for vsync). 0: not reversed 1: reversed
[17:16]	RW	vsync_sel	vsync source select (level-0 processing for vsync). 00: input vsync 01: input field 10: 0 11: reserved
[15]	-	reserved	Reserved.
[14:13]	RW	hsync_mode	hsync processing mode (level-3 processing for hsync). 0: No operation is performed. 1: Pulses are generated based on the rising edge.

Offset Address	Register Name	Total Reset Value
0x0130	PT_UNIFY_TIMING_CFG	0x0008_2801

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					field_inv	field_sel		reserved				vsync_mode	vsync_inv	vsync_sel		reserved	hsync_mode		hsync_and		hsync_inv	hsync_sel		reserved					de_inv	de_sel	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[12:11]	RW	hsync_and	Whether hsync is calculated with the level-1 processing result of vsync (level-2 processing for hsync). 00: no operation 01: AND 10: exclusive OR 11: reserved
[10]	RW	hsync_inv	hsync reverse (level-1 processing for hsync). 0: not reversed 1: reversed
[9:8]	RW	hsync_sel	hsync source select (level-0 processing for hsync). 00: input vsync 01: input de 10: 0 11: reserved
[7:3]	-	reserved	Reserved.
[2]	RW	de_inv	de reverse (level-1 processing for de). 0: not reversed 1: reversed
[1:0]	RW	de_sel	de source select (level-0 processing for de). 00: input de 01: level-2 processing result of hsync 10: 1 11: 0

PT_GEN_TIMING_CFG

PT_GEN_TIMING_CFG is a timing restoration module configuration register.

Offset Address	Register Name	Total Reset Value
0x0134	PT_GEN_TIMING_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																												vsync_mode	hsync_mode	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	Timing restoration enable. Timings are resorted based on timing parameters. 0: disabled 1: enabled
[30:3]	-	reserved	Reserved.
[2]	RW	vsync_mode	vsync restore. 0: not restored 1: restored
[1]	RW	hsync_mode	hsync restore. 0: not restored 1: restored
[0]	-	reserved	Reserved.

PT_UNIFY_DATA_CFG

PT_UNIFY_DATA_CFG is a data configuration register.

Offset Address	Register Name	Total Reset Value
0x0140	PT_UNIFY_DATA_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																											uv_seq	yc_seq	comp_num		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	Data separation enable. 0: disabled 1: enabled
[30:4]	-	reserved	Reserved.
[3]	RW	uv_seq	CbCr sequence. 0: CbCr 1: CrCb
[2]	RW	yc_seq	YC sequence. 0: CY 1: YC
[1:0]	RW	comp_num	Data component select. 00: component 1 01: component 2 10: component 3 11: reserved

PT_GEN_DATA_CFG

PT_GEN_DATA_CFG is a data generation module configuration register.

Offset Address	Register Name	Total Reset Value
0x0144	PT_GEN_DATA_CFG	0x0000_00E9

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																							data2_move	data1_move	data0_move	vsync_reset	hsync_reset	vsync_move	hsync_move	de_move
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	0	1

Bits	Access	Name	Description
[31]	RW	enable	Timing restoration enable. Timings are resorted based on timing parameters. 0: disabled 1: enabled
[30:8]	-	reserved	Reserved.
[7]	RW	data2_move	Data 2 increment. 0: no increment 1: increment
[6]	RW	data1_move	Data 1 increment. 0: no increment 1: increment
[5]	RW	data0_move	Data 0 increment. 0: no increment 1: increment
[4]	RW	vsync_reset	Data reset for the vsync signal. 0: not reset 1: reset
[3]	RW	hsync_reset	Data reset for the hsync signal. 0: not reset 1: reset
[2]	RW	vsync_move	Data increment for the vsync signal. 0: no increment 1: increment
[1]	RW	hsync_move	Data increment for the hsync signal. 0: no increment 1: increment

Offset Address	Register Name	Total Reset Value
0x0144	PT_GEN_DATA_CFG	0x0000_00E9

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																							data2_move	data1_move	data0_move	vsync_reset	hsync_reset	vsync_move	hsync_move	de_move	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	0	1

Bits	Access	Name	Description
[0]	RW	de_move	Data increment for the de signal. 0: no increment 1: increment

PT_GEN_DATA_COEF

PT_GEN_DATA_COEF is a data generation module coefficient register.

Offset Address	Register Name	Total Reset Value
0x0148	PT_GEN_DATA_COEF	0x0100_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	inc_frame								step_frame								inc_space								step_space							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	inc_frame	Pixel incremental value between frames. The incremental value is accumulated in the upper eight bits of data.
[23:16]	RW	step_frame	Pixel value increment interval between frames. The configured value is the actual value minus 1. The value 0 indicates that the pixel value is incremented in each frame.
[15:8]	RW	inc_space	Data pixel incremental value. The incremental value is accumulated in the upper 10 bits of data.
[7:0]	RW	step_space	Pixel increment interval between pixels. The value 0 indicates that the pixel value is incremented for each pixel.

PT_GEN_DATA_INIT

PT_GEN_DATA_INIT is a data generation module initial value register.

Offset Address	Register Name	Total Reset Value
0x014C	PT_GEN_DATA_INIT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								data2								data1								data0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:16]	RW	data2	Initial V/B value.
[15:8]	RW	data1	Initial U/G value.
[7:0]	RW	data0	Initial Y/R value.

PT_YUV444_CFG

PT_YUV444_CFG is a YUV444 configuration register.

Offset Address	Register Name	Total Reset Value
0x0150	PT_YUV444_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	YUV enable. YUV422 signals are converted into YUV444 signals. 0: disabled 1: enabled
[30:0]	-	reserved	Reserved.

PT_FSTART_DLY

PT_FSTART_DLY is a port fstart interrupt delay register.

Offset Address	Register Name	Total Reset Value
0x0160	PT_FSTART_DLY	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fstart_dly																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	fstart_dly	Delay time. Its unit is port clock.

PT_INTF_HFB

PT_INTF_HFB is a horizontal front blanking width register.

Offset Address	Register Name	Total Reset Value
0x0180	PT_INTF_HFB	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hfb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	hfb	Horizontal front blanking width.

PT_INTF_HACT

PT_INTF_HACT is a horizontal active width register.

Offset Address	Register Name	Total Reset Value
0x0184	PT_INTF_HACT	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hact															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	hact	Horizontal active width. Its unit is clock cycle.

PT_INTF_HBB

PT_INTF_HBB is a horizontal back blanking width register.

Offset Address	Register Name	Total Reset Value
0x0188	PT_INTF_HBB	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hbb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	hbb	Horizontal back blanking width.

PT_INTF_VFB

PT_INTF_VFB is a vertical front blanking width register.

Offset Address	Register Name	Total Reset Value
0x018C	PT_INTF_VFB	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vfb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	vfb	Vertical front blanking width.

PT_INTF_VACT

PT_INTF_VACT is a vertical active width register.

Offset Address	Register Name	Total Reset Value
0x0190	PT_INTF_VACT	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vact															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.

Offset Address	Register Name	Total Reset Value
0x0190	PT_INTF_VACT	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vact															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[15:0]	RW	vact	Vertical active width.

PT_INTF_VBB

PT_INTF_VBB is a vertical back blanking width register.

Offset Address	Register Name	Total Reset Value
0x0194	PT_INTF_VBB	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vbb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	vbb	Vertical back blanking width.

PT_INTF_VBFB

PT_INTF_VBFB is a vertical bottom front blanking width register.

Offset Address	Register Name	Total Reset Value
0x0198	PT_INTF_VBFB	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vbfb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	vbfb	Vertical bottom front blanking width.

PT_INTF_VBACT

PT_INTF_VBACT is a vertical bottom active width register.

Offset Address	Register Name	Total Reset Value
0x019C	PT_INTF_VBACT	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vact															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	vact	Vertical bottom active width.

PT_INTF_VBBB

PT_INTF_VBBB is a vertical bottom back blanking width register.

Offset Address	Register Name	Total Reset Value
0x01A0	PT_INTF_VBBB	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vbbb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	vbbb	Vertical bottom back blanking width.

PT_FLASH_CFG

PT_FLASH_CFG is a camera flash configuration register.

Offset Address	Register Name	Total Reset Value
0x01B0	PT_FLASH_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													shutter_times	shutter_phase	shutter_en	reserved															flash_phase	flash_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	-	reserved	Reserved.
[18]	RW	shutter_times	Shutter pulse times. 0: twice 1: once
[17]	RW	shutter_phase	Shutter signal reverse. 0: not reversed 1: reversed
[16]	WO	shutter_en	Shutter enable. This field is automatically cleared.
[15:2]	-	reserved	Reserved.
[1]	RW	flash_phase	Camera flash signal reverse. 0: not reversed 1: reversed
[0]	WO	flash_en	Camera flash enable. This field is automatically cleared.

PT_FLASH_CYC0

PT_FLASH_CYC0 is flash timing 0 width register.

Offset Address	Register Name	Total Reset Value
0x01C0	PT_FLASH_CYC0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cyc																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cyc	Duration of flash timing 0. Its unit is port clock. The configured value is the actual value minus 1.

PT_FLASH_CYC1

PT_FLASH_CYC1 is flash timing 1 width register.

Offset Address	Register Name	Total Reset Value
0x01C4	PT_FLASH_CYC1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cyc																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cyc	Duration of flash timing 1. Its unit is port clock. The configured value is the actual value minus 1.

PT_SHUTTER_CYC0

PT_SHUTTER_CYC0 is shutter timing 0 width register.

Offset Address	Register Name	Total Reset Value
0x01D0	PT_SHUTTER_CYC0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cyc																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cyc	Duration of shutter timing 0. Its unit is port clock. The configured value is the actual value minus 1.

PT_SHUTTER_CYC1

PT_SHUTTER_CYC1 is shutter timing 1 width register.

Offset Address	Register Name	Total Reset Value
0x01D4	PT_SHUTTER_CYC1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cyc																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cyc	Duration of shutter timing 1. Its unit is port clock. The configured value is the actual value minus 1.

PT_SHUTTER_CYC2

PT_SHUTTER_CYC2 is shutter timing 2 width register.

Offset Address	Register Name	Total Reset Value
0x01D8	PT_SHUTTER_CYC2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cyc																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cyc	Duration of shutter timing 2. Its unit is port clock. The configured value is the actual value minus 1.

PT_SHUTTER_CYC3

PT_SHUTTER_CYC3 is shutter timing 3 width register.

Offset Address	Register Name	Total Reset Value
0x01DC	PT_SHUTTER_CYC3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cyc																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cyc	Duration of shutter timing 3. Its unit is port clock. The configured value is the actual value minus 1.

PT_STATUS

PT_STATUS is a port status register.

Offset Address	Register Name	Total Reset Value
0x01E0	PT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												field	vysnc	hsync	de
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	-	reserved	Reserved.
[3]	RO	field	Field signal output over the port.
[2]	RO	vysnc	vysnc signal output over the port.
[1]	RO	hsync	hsync signal output over the port.
[0]	RO	de	de signal output over the port.

PT_BT656_STATUS

PT_BT656_STATUS is a BT.656 status register.

Offset Address	Register Name	Total Reset Value
0x01E4	PT_BT656_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																seav								reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:8]	RO	seav	Synchronization code.
[7:0]	-	reserved	Reserved.

PT_SIZE

PT_SIZE is an input size indicator register.

Offset Address	Register Name	Total Reset Value
0x01EC	PT_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	height																width															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	height	Picture height. Its unit is pixel.
[15:0]	RO	width	Picture width. Its unit is pixel.

PT_INT

PT_INT is a channel interrupt indicator register.

Offset Address	Register Name	Total Reset Value
0x01F0	PT_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													height_err	width_err	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	-	reserved	Reserved.
[2]	WC	height_err	Status of the picture height change interrupt. Writing 1 clears the status. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	WC	width_err	Status of the picture width change interrupt. Writing 1 clears the status. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	WC	fstart	Status of the field/frame start interrupt. Writing 1 clears the status. 0: No interrupt is generated. 1: An interrupt is generated.

PT_INT_MASK

PT_INT_MASK is a channel interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x01F8	PT_INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													height_err_en	width_err_en	fstart_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	-	reserved	Reserved.
[2]	RW	height_err_en	Picture height change interrupt enable. 0: masked 1: enabled
[1]	RW	width_err_en	Picture width change interrupt enable. 0: masked 1: enabled
[0]	RW	fstart_en	Frame/Field start interrupt enable. 0: masked 1: enabled

CH_CTRL

CH_CTRL is a channel control register.

Offset Address	Register Name	Total Reset Value
0x1000	CH_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	Channel enable. 0: disabled 1: enabled 0x1000–0x1FFF indicates the channel address range.
[30:0]	-	reserved	Reserved.

CH_REG_NEWER

CH_REG_NEWER is a capture control register.

Offset Address	Register Name	Total Reset Value
0x1004	CH_REG_NEWER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															reg_newer
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	reg_newer	Channel updated. This bit is automatically cleared when a frame is received.

CH_ADAPTER_CFG

CH_ADAPTER_CFG is a timing adaptation register.

Offset Address	Register Name	Total Reset Value
0x1010	CH_ADAPTER_CFG	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														vsync_mode	hsync_mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:2]	-	reserved	Reserved.
[1]	RW	vsync_mode	Delay processing for the vsync signal. 0: no delay 1: delay
[0]	RW	hsync_mode	Delay processing for the hsync signal. 0: no delay 1: delay

CH_PACK_Y_CFG

CH_PACK_Y_CFG is a Y component control register for the PACK module.

Offset Address	Register Name	Total Reset Value
0x1080	CH_PACK_Y_CFG	0x0000_0008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mode		reserved																						bitw							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31:30]	RW	mode	PACK mode. 00: normal mode 11: mirror mode Other values: reserved
[29:8]	-	reserved	Reserved.

Offset Address	Register Name	Total Reset Value
0x1080	CH_PACK_Y_CFG	0x0000_0008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mode				reserved																				bitw							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[7:0]	RW	bitw	Data bit width. 0x8: 8 bits 0xC: 12 bits 0x10: 16 bits Other values: reserved

CH_PACK_Y_WIDTH

CH_PACK_Y_WIDTH is a Y component input width register for the PACK module.

Offset Address	Register Name	Total Reset Value
0x1084	CH_PACK_Y_WIDTH	0x0000_27FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												width																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:20]	-	reserved	Reserved.
[19:0]	RW	width	Number of input bits of the PACK module. The configured value is the actual value minus 1.

CH_PACK_C_CFG

CH_PACK_C_CFG is a C component control register for the PACK module.

Offset Address	Register Name	Total Reset Value
0x1090	CH_PACK_C_CFG	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mode		reserved																						bitw							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:30]	RW	mode	PACK mode. 00: normal mode 11: mirror mode Other values: reserved
[29:8]	-	reserved	Reserved.
[7:0]	RW	bitw	Data bit width. 0x10: 8 bits Other values: reserved

CH_PACK_C_WIDTH

CH_PACK_C_WIDTH is a C component input width register for the PACK module.

Offset Address	Register Name	Total Reset Value
0x1094	CH_PACK_C_WIDTH	0x0000_27FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												width																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:20]	-	reserved	Reserved.
[19:0]	RW	width	Number of input bits of the PACK module. The configured value is the actual value minus 1.

CH_DES_Y_CFG

CH_DES_Y_CFG is a Y component configuration register for the DES module.

Offset Address	Register Name	Total Reset Value
0x10B0	CH_DES_Y_CFG	0x003F_0800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	buf_len																dis								reserved						flip	mirror
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	buf_len	Buffer size of the DES module. Its unit is 128 bits and it must be an integral multiple of 16. The configured value is the actual value minus 1.
[15:8]	RW	dis	Minimum interval between two consecutive bus requests. Its unit is channel clock.
[7:2]	-	reserved	Reserved.
[1]	RW	flip	Flip enable. 0: disabled 1: enabled
[0]	RW	mirror	Mirror enable. 0: disabled 1: enabled

CH_DES_Y_FADDR

CH_DES_Y_FADDR is a Y component storage base address register.

Offset Address	Register Name	Total Reset Value
0x10B4	CH_DES_Y_FADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	faddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	faddr	Base address for storing the Y component in raw streams.

CH_DES_Y_SIZE

CH_DES_Y_SIZE is a Y component storage size register.

Offset Address	Register Name	Total Reset Value
0x10B8	CH_DES_Y_SIZE	0x02CF_004F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	height																reserved				width											
Reset	0	0	0	0	0	0	1	0	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	1

Bits	Access	Name	Description
[31:16]	RW	height	Y component output height. Its unit is line. The configured value is the actual value minus 1.
[15:12]	-	reserved	Reserved.
[11:0]	RW	width	Y component output width. Its unit is 128 bits. The configured value is the actual value minus 1.

CH_DES_Y_STRIDE

CH_DES_Y_STRIDE is a Y component stride register.

Offset Address	Register Name	Total Reset Value
0x10BC	CH_DES_Y_STRIDE	0x0000_0500

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	stride	Stride for storing the Y component. Its unit is byte.

CH_DES_C_CFG

CH_DES_C_CFG is a C component configuration register for the DES module.

Offset Address	Register Name	Total Reset Value
0x10C0	CH_DES_C_CFG	0x003F_0800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	buf_len																dis								reserved						flip	mirror
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	buf_len	Buffer size of the DES module. Its unit is 128 bits and it must be an integral multiple of 16. The configured value is the actual value minus 1.
[15:8]	RW	dis	Minimum interval between two consecutive bus requests. Its unit is channel clock.
[7:2]	-	reserved	Reserved.
[1]	RW	flip	Flip enable. 0: disabled 1: enabled
[0]	RW	mirror	Mirror enable. 0: disabled 1: enabled

CH_DES_C_FADDR

CH_DES_C_FADDR is a C component storage base address register.

Offset Address	Register Name	Total Reset Value
0x10C4	CH_DES_C_FADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	faddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	faddr	Base address for storing the C component in raw streams.

CH_DES_C_SIZE

CH_DES_C_SIZE is a C component storage size register.

Offset Address	Register Name	Total Reset Value
0x10C8	CH_DES_C_SIZE	0x02CF_004F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	height																reserved				width											
Reset	0	0	0	0	0	0	1	0	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	1

Bits	Access	Name	Description
[31:16]	RW	height	C component output height. Its unit is line. The configured value is the actual value minus 1.
[15:12]	-	reserved	Reserved.
[11:0]	RW	width	C component output width. Its unit is 128 bits. The configured value is the actual value minus 1.

CH_DES_C_STRIDE

CH_DES_C_STRIDE is a C component stride register.

Offset Address	Register Name	Total Reset Value
0x10CC	CH_DES_C_STRIDE	0x0000_0500

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	stride	Stride for storing the C component. Its unit is byte.

CH_INT

CH_INT is a channel raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x10F0	CH_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									bus_err_y	bus_err_c	update_cfg	field_throw	buf_ovf	cc_int	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	-	reserved	Reserved.
[6]	WC	bus_err_y	Status of the Y data channel bus error interrupt. Writing 1 clears the status. 0: No interrupt is generated. 1: An interrupt is generated.
[5]	WC	bus_err_c	Status of the C data channel bus error interrupt. Writing 1 clears the status. 0: No interrupt is generated. 1: An interrupt is generated.
[4]	WC	update_cfg	Status of the register update interrupt. Writing 1 clears the status. 0: No interrupt is generated. 1: An interrupt is generated.
[3]	WC	field_throw	Status of the field/frame loss interrupt. Writing 1 clears the status. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	WC	buf_ovf	Status of the internal FIFO overflow error interrupt. Writing 1 clears the status. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	WC	cc_int	Status of the capture completion interrupt. Writing 1 clears the status. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	WC	fstart	Status of the field/frame start interrupt. Writing 1 clears the status. 0: No interrupt is generated. 1: An interrupt is generated.

CH_INT_MASK

CH_INT_MASK is a channel interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x10F8	CH_INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									bus_err_y_en	bus_err_c_en	update_cfg	field_throw_en	buf_ovf_en	cc_int_en	fstart_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	-	reserved	Reserved.
[6]	RW	bus_err_y_en	Y data channel bus error interrupt enable. 0: masked 1: enabled
[5]	RW	bus_err_c_en	C data channel bus error interrupt enable. 0: masked 1: enabled
[4]	RW	update_cfg	Register update interrupt enable. 0: masked 1: enabled
[3]	RW	field_throw_en	Field/Frame loss interrupt enable. 0: masked 1: enabled
[2]	RW	buf_ovf_en	Internal FIFO overflow error interrupt enable. 0: masked 1: enabled
[1]	RW	cc_int_en	Capture completion interrupt enable. 0: masked 1: enabled
[0]	RW	fstart_en	Field/Frame start interrupt enable. 0: masked 1: enabled

CH_CROP_CFG

CH_CROP_CFG is a crop enable register.

Offset Address	Register Name	Total Reset Value
0x1100	CH_CROP_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															n0_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	n0_en	Region 0 enable.

CH_CROP_WIN

CH_CROP_WIN is a crop window register.

Offset Address	Register Name	Total Reset Value
0x1104	CH_CROP_WIN	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	height																width															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RW	height	Window height. Its unit is pixel. The configured value is the actual value minus 1.
[15:0]	RW	width	Window width. Its unit is pixel. The configured value is the actual value minus 1.

CH_CROP0_START

CH_CROP0_START is a crop start position register for region 0.

Offset Address	Register Name	Total Reset Value
0x1110	CH_CROP0_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	y_start																x_start															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	y_start	Number of the line from which pictures start to be captured.
[15:0]	RW	x_start	Number of the pixel from which pictures start to be captured.

CH_CROP0_SIZE

CH_CROP0_SIZE is a crop size configuration register for region 0.

Offset Address	Register Name	Total Reset Value
0x1114	CH_CROP0_SIZE	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	height																width															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RW	height	Height of the captured picture. Its unit is line. The configured value is the actual value minus 1.
[15:0]	RW	width	Width of a line in the captured picture. Its unit is pixel. The configured value is the actual value minus 1.

CH_CSC_CFG

CH_CSC_CFG is a CSC configuration register.

Offset Address	Register Name	Total Reset Value
0x1200	CH_CSC_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	CSC enable. 0: disabled 1: enabled
[30:0]	-	reserved	Reserved.

CH_CSC_COEF0

CH_CSC_COEF0 is CSC coefficient register 0.

Offset Address	Register Name	Total Reset Value
0x1210	CH_CSC_COEF0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef01												reserved				coef00												reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RW	coef01	CSC coefficient. Its format is (s, 4, 8). The value consists of a 1-bit signed part, a 4-bit integral part, and an 8-bit fractional part.
[18:16]	-	reserved	Reserved.
[15:3]	RW	coef00	CSC coefficient. Its format is (s, 4, 8). The value consists of a 1-bit signed part, a 4-bit integral part, and an 8-bit fractional part.
[2:0]	-	reserved	Reserved.

CH_CSC_COEF1

CH_CSC_COEF1 is CSC coefficient register 1.

Offset Address	Register Name	Total Reset Value
0x1214	CH_CSC_COEF1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef10												reserved				coef02												reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RW	coef10	CSC coefficient. Its format is (s, 4, 8). The value consists of a 1-bit signed part, a 4-bit integral part, and an 8-bit fractional part.
[18:16]	-	reserved	Reserved.
[15:3]	RW	coef02	CSC coefficient. Its format is (s, 4, 8). The value consists of a 1-bit signed part, a 4-bit integral part, and an 8-bit fractional part.
[2:0]	-	reserved	Reserved.

CH_CSC_COEF2

CH_CSC_COEF2 is CSC coefficient register 2.

Offset Address	Register Name	Total Reset Value
0x1218	CH_CSC_COEF2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef12												reserved				coef11												reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RW	coef12	CSC coefficient. Its format is (s, 4, 8). The value consists of a 1-bit signed part, a 4-bit integral part, and an 8-bit fractional part.
[18:16]	-	reserved	Reserved.
[15:3]	RW	coef11	CSC coefficient. Its format is (s, 4, 8). The value consists of a 1-bit signed part, a 4-bit integral part, and an 8-bit fractional part.

Offset Address	Register Name	Total Reset Value
0x1218	CH_CSC_COEF2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef12												reserved				coef11												reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[2:0]	-	reserved	Reserved.

CH_CSC_COEF3

CH_CSC_COEF3 is CSC coefficient register 3.

Offset Address	Register Name	Total Reset Value
0x121C	CH_CSC_COEF3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef21												reserved				coef20												reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RW	coef21	CSC coefficient. Its format is (s, 4, 8). The value consists of a 1-bit signed part, a 4-bit integral part, and an 8-bit fractional part.
[18:16]	-	reserved	Reserved.
[15:3]	RW	coef20	CSC coefficient. Its format is (s, 4, 8). The value consists of a 1-bit signed part, a 4-bit integral part, and an 8-bit fractional part.
[2:0]	-	reserved	Reserved.

CH_CSC_COEF4

CH_CSC_COEF4 is CSC coefficient register 4.

Offset Address	Register Name	Total Reset Value
0x1220	CH_CSC_COEF4	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			reserved	coef22			reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:19]	RW	reserved	CSC coefficient. Its format is (s, 4, 8). The value consists of a 1-bit signed part, a 4-bit integral part, and an 8-bit fractional part.
[18:16]	-	reserved	Reserved.
[15:3]	RW	coef22	CSC coefficient. Its format is (s, 4, 8). The value consists of a 1-bit signed part, a 4-bit integral part, and an 8-bit fractional part.
[2:0]	-	reserved	Reserved.

CH_CSC_IN_DC0

CH_CSC_IN_DC0 is CSC input DC component register 0.

Offset Address	Register Name	Total Reset Value
0x1230	CH_CSC_IN_DC0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	in_dc1			reserved	in_dc0			reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:21]	RW	in_dc1	DC offset of the input G component. It is a signed integer.
[20:16]	-	reserved	Reserved.
[15:5]	RW	in_dc0	DC offset of the input R component. It is a signed integer.
[4:0]	-	reserved	Reserved.

CH_CSC_IN_DC1

CH_CSC_IN_DC1 is CSC input DC component register 1.

Offset Address	Register Name	Total Reset Value
0x1234	CH_CSC_IN_DC1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												reserved				in_dc2												reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RW	reserved	Reserved.
[20:16]	-	reserved	Reserved.
[15:5]	RW	in_dc2	DC offset of the input B component. It is a signed integer.
[4:0]	-	reserved	Reserved.

CH_CSC_OUT_DC0

CH_CSC_OUT_DC0 is CSC output DC component register 0.

Offset Address	Register Name	Total Reset Value
0x1238	CH_CSC_OUT_DC0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	out_dc1												reserved				out_dc0												reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RW	out_dc1	DC offset of the input U component. It is a signed integer.
[20:16]	-	reserved	Reserved.
[15:5]	RW	out_dc0	DC offset of the output Y component. It is a signed integer.
[4:0]	-	reserved	Reserved.

CH_CSC_OUT_DC1

CH_CSC_OUT_DC1 is CSC output DC component register 1.

Offset Address	Register Name	Total Reset Value
0x123C	CH_CSC_OUT_DC1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												reserved				out_dc2												reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RW	reserved	Reserved.
[20:16]	-	reserved	Reserved.
[15:5]	RW	out_dc2	DC offset of the output V component. It is a signed integer.
[4:0]	-	reserved	Reserved.

CH_MSC_CFG

CH_MSC_CFG is a block mask configuration register.

Offset Address	Register Name	Total Reset Value
0x1300	CH_MSC_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												msc3_en	msc2_en	msc1_en	msc0_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	-	reserved	Reserved.
[3]	RW	msc3_en	Block 3 mask enable. 0: disabled 1: enabled
[2]	RW	msc2_en	Block 2 mask enable. 0: disabled 1: enabled
[1]	RW	msc1_en	Block 1 mask enable. 0: disabled 1: enabled

Offset Address	Register Name	Total Reset Value
0x1300	CH_MSC_CFG	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	reserved							msc3_en	msc2_en	msc1_en	msc0_en
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	msc0_en	Block 0 mask enable. 0: disabled 1: enabled

CH_MSC_WIN

CH_MSC_WIN is an occlusion window register.

Offset Address	Register Name	Total Reset Value
0x1304	CH_MSC_WIN	0xFFFF_FFFF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	height				width			
Reset	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:16]	RW	height	Window height. Its unit is pixel. The configured value is the actual value minus 1.
[15:0]	RW	width	Window width. Its unit is pixel. The configured value is the actual value minus 1.

CH_BLOCK0_START

CH_BLOCK0_START is a mask start position register for block 0.

Offset Address	Register Name	Total Reset Value
0x1310	CH_BLOCK0_START	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	y_start			reserved	x_start		

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27:16]	RW	y_start	Vertical start point for masking block 0.
[15:12]	-	reserved	Reserved.
[11:0]	RW	x_start	Horizontal start point for masking block 0.

CH_BLOCK1_START

CH_BLOCK1_START is a mask start position register for block 1.

Offset Address	Register Name	Total Reset Value
0x1314	CH_BLOCK1_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				y_start												reserved				x_start											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27:16]	RW	y_start	Vertical start point for masking block 1.
[15:12]	-	reserved	Reserved.
[11:0]	RW	x_start	Horizontal start point for masking block 1.

CH_BLOCK2_START

CH_BLOCK2_START is a mask start position register for block 2.

Offset Address	Register Name	Total Reset Value
0x1318	CH_BLOCK2_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				y_start												reserved				x_start											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27:16]	RW	y_start	Vertical start point for masking block 2.
[15:12]	-	reserved	Reserved.

Offset Address	Register Name	Total Reset Value
0x1318	CH_BLOCK2_START	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	y_start			reserved	x_start		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[11:0]	RW	x_start	Horizontal start point for masking block 2.

CH_BLOCK3_START

CH_BLOCK3_START is a mask start position register for block 3.

Offset Address	Register Name	Total Reset Value
0x131C	CH_BLOCK3_START	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	y_start			reserved	x_start		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27:16]	RW	y_start	Vertical start point for masking block 3.
[15:12]	-	reserved	Reserved.
[11:0]	RW	x_start	Horizontal start point for masking block 3.

CH_BLOCK0_SIZE

CH_BLOCK0_SIZE is a mask size register for block 0.

Offset Address	Register Name	Total Reset Value
0x1320	CH_BLOCK0_SIZE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	blk_height			reserved	blk_width		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.

Offset Address	Register Name	Total Reset Value
0x1320	CH_BLOCK0_SIZE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	blk_height			reserved	blk_width		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[27:16]	RW	blk_height	Vertical height for masking block 0. The configured value is the actual value minus 1.
[15:12]	-	reserved	Reserved.
[11:0]	RW	blk_width	Horizontal width for making block 0. The configured value is the actual value minus 1.

CH_BLOCK1_SIZE

CH_BLOCK1_SIZE is a mask size register for block 1.

Offset Address	Register Name	Total Reset Value
0x1324	CH_BLOCK1_SIZE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	blk_height			reserved	blk_width		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27:16]	RW	blk_height	Vertical height for masking block 1. The configured value is the actual value minus 1.
[15:12]	-	reserved	Reserved.
[11:0]	RW	blk_width	Horizontal width for making block 1. The configured value is the actual value minus 1.

CH_BLOCK2_SIZE

CH_BLOCK2_SIZE is a mask size register for block 2.

Offset Address	Register Name	Total Reset Value
0x1328	CH_BLOCK2_SIZE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	blk_height			reserved	blk_width		

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27:16]	RW	blk_height	Vertical height for masking block 2. The configured value is the actual value minus 1.
[15:12]	-	reserved	Reserved.
[11:0]	RW	blk_width	Horizontal width for making block 2. The configured value is the actual value minus 1.

CH_BLOCK3_SIZE

CH_BLOCK3_SIZE is a mask size register for block 3.

Offset Address	Register Name	Total Reset Value
0x132C	CH_BLOCK3_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				blk_height												reserved				blk_width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27:16]	RW	blk_height	Vertical height for masking block 3. The configured value is the actual value minus 1.
[15:12]	-	reserved	Reserved.
[11:0]	RW	blk_width	Horizontal width for making block 3. The configured value is the actual value minus 1.

CH_BLOCK0_COLOR

CH_BLOCK0_COLOR is a filling color register for block 0.

Offset Address	Register Name	Total Reset Value
0x1330	CH_BLOCK0_COLOR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								blk_cr								blk_cb								blc_y							

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:16]	RW	blk_cr	Cr component of the filling color of block 0.
[15:8]	RW	blk_cb	Cb component of the filling color of block 0.
[7:0]	RW	blc_y	Y component of the filling color of block 0.

CH_BLOCK1_COLOR

CH_BLOCK1_COLOR is a filling color register for block 1.

Offset Address	Register Name	Total Reset Value
0x1334	CH_BLOCK1_COLOR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								blk_cr								blk_cb								blc_y							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:16]	RW	blk_cr	Cr component of the filling color of block 1.
[15:8]	RW	blk_cb	Cb component of the filling color of block 1.
[7:0]	RW	blc_y	Y component of the filling color of block 1.

CH_BLOCK2_COLOR

CH_BLOCK2_COLOR is a filling color register for block 2.

Offset Address	Register Name	Total Reset Value
0x1338	CH_BLOCK2_COLOR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								blk_cr								blk_cb								blc_y							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:16]	RW	blk_cr	Cr component of the filling color of block 2.
[15:8]	RW	blk_cb	Cb component of the filling color of block 2.

Offset Address	Register Name	Total Reset Value
0x1338	CH_BLOCK2_COLOR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								blk_cr								blk_cb								blc_y							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	blc_y	Y component of the filling color of block 2.

CH_BLOCK3_COLOR

CH_BLOCK3_COLOR is a filling color register for block 3.

Offset Address	Register Name	Total Reset Value
0x133C	CH_BLOCK3_COLOR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								blk_cr								blk_cb								blc_y							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:16]	RW	blk_cr	Cr component of the filling color of block 3.
[15:8]	RW	blk_cb	Cb component of the filling color of block 3.
[7:0]	RW	blc_y	Y component of the filling color of block 3.

CH_SKIP_Y_CFG

CH_SKIP_Y_CFG is a Y component skip configuration register.

Offset Address	Register Name	Total Reset Value
0x1400	CH_SKIP_Y_CFG	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	skip_cfg																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RW	skip_cfg	Skip configuration.

CH_SKIP_Y_WIN

CH_SKIP_Y_WIN is a Y component skip window register.

Offset Address	Register Name	Total Reset Value
0x1404	CH_SKIP_Y_WIN	0x0003_0007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														height		reserved												width			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Access	Name	Description
[31:18]	-	reserved	Reserved.
[17:16]	RW	height	Window height. Its unit is pixel. The configured value is the actual value minus 1.
[15:3]	-	reserved	Reserved.
[2:0]	RW	width	Window width. Its unit is pixel. The configured value is the actual value minus 1.

CH_SKIP_C_CFG

CH_SKIP_C_CFG is a C component skip configuration register.

Offset Address	Register Name	Total Reset Value
0x1410	CH_SKIP_C_CFG	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	skip_cfg																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RW	skip_cfg	Skip configuration.

CH_SKIP_C_WIN

CH_SKIP_C_WIN is a C component skip window register.

Offset Address	Register Name	Total Reset Value
0x1414	CH_SKIP_C_WIN	0x0003_0007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														height		reserved												width			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Access	Name	Description
[31:18]	-	reserved	Reserved.
[17:16]	RW	height	Window height. Its unit is pixel. The configured value is the actual value minus 1.
[15:3]	-	reserved	Reserved.
[2:0]	RW	width	Window width. Its unit is pixel. The configured value is the actual value minus 1.

CH_ZME_C_SSIZE

CH_ZME_C_SSIZE is a C component input size register for the zoom module.

Offset Address	Register Name	Total Reset Value
0x1500	CH_ZME_C_SSIZE	0x0000_04FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																width															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	width	Picture width. Its unit is pixel. The configured value is the actual value minus 1.

CH_ZME_C_DSIZE

CH_ZME_C_DSIZE is a C component output size register for the zoom module.

Offset Address	Register Name	Total Reset Value
0x1504	CH_ZME_C_DSIZE	0x0000_04FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																width															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	width	Picture width. Its unit is pixel. The configured value is the actual value minus 1.

CH_HFIR_C_SPH

CH_HFIR_C_SPH is a chrominance horizontal scaling parameter configuration register.

Offset Address	Register Name	Total Reset Value
0x1510	CH_HFIR_C_SPH	0x0000_1000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved															ratio				reserved											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	Chrominance horizontal scaling enable. 0: disabled 1: enabled
[30:16]	-	reserved	Reserved.
[15:12]	RW	ratio	Chrominance horizontal scaling ratio. It is calculated by dividing the input width by the output width. If horizontal pre-processing is enabled, the input width after pre-processing is used. The ratio is in the format of (u, 4). That is, the ratio consists of a 1-bit unsigned bit and a 4-bit integral part.
[11:0]	-	reserved	Reserved.

CH_HFIR_C_OFFSET

CH_HFIR_C_OFFSET is a chrominance scaling horizontal offset register.

Offset Address	Register Name	Total Reset Value
0x1514	CH_HFIR_C_OFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																offset				reserved												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	-	reserved	Reserved.
[16:12]	RW	offset	Chrominance horizontal start position offset. It is in the format of (s, 5). That is, the offset consists of a 1-bit signed part and a 4-bit integral part. The offset is expressed as the complementary code and ranges from –4 to +15.
[11:0]	-	reserved	Reserved.

CH_HFIR_C_COEF0

CH_HFIR_C_COEF0 is chrominance horizontal scaling coefficient register 0.

Offset Address	Register Name	Total Reset Value
0x1520	CH_HFIR_C_COEF0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		coef2										coef1								coef0											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	-	reserved	Reserved.
[29:20]	RW	coef2	Chrominance horizontal scaling and filtering coefficient 2.
[19:10]	RW	coef1	Chrominance horizontal scaling and filtering coefficient 1.
[9:0]	RW	coef0	Chrominance horizontal scaling and filtering coefficient 0. Only 8-tap horizontal scaling at an integral ratio is supported.

CH_HFIR_C_COEF1

CH_HFIR_C_COEF1 is chrominance horizontal scaling coefficient register 1.

Offset Address	Register Name	Total Reset Value
0x1524	CH_HFIR_C_COEF1	0x0000_01FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				coef5								coef4												coef3							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:30]	-	reserved	Reserved.
[29:20]	RW	coef5	Chrominance horizontal scaling and filtering coefficient 5.
[19:10]	RW	coef4	Chrominance horizontal scaling and filtering coefficient 4.
[9:0]	RW	coef3	Chrominance horizontal scaling and filtering coefficient 3.

CH_HFIR_C_COEF2

CH_HFIR_C_COEF2 is chrominance horizontal scaling coefficient register 2.

Offset Address	Register Name	Total Reset Value
0x1528	CH_HFIR_C_COEF2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												coef7												coef6							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	-	reserved	Reserved.
[19:10]	RW	coef7	Chrominance horizontal scaling and filtering coefficient 7.
[9:0]	RW	coef6	Chrominance horizontal scaling and filtering coefficient 6.

CH_DITHER_CFG

CH_DITHER_CFG is a dither configuration register.

Offset Address	Register Name	Total Reset Value
0x1600	CH_DITHER_CFG	0xE000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dither_md				reserved																											
Reset	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RW	dither_md	Dither mode select. 000: 12-bit inputs, 10-bit outputs, no dithering, and direct bit truncation 001: 12-bit inputs, 10-bit outputs, and time-domain dithering 010: 12-bit inputs, 10-bit outputs, and spatial-domain dithering 011: 12-bit inputs, 8-bit outputs, and time-domain and spatial-domain dithering 100: 12-bit inputs, 10-bit outputs, and round off 101: 12-bit inputs, 8-bit outputs, and round off 111: no operation
[28:0]	-	reserved	Reserved.

CH_DITHER_COEF0

CH_DITHER_COEF0 is dither coefficient register 0.

Offset Address	Register Name	Total Reset Value
0x1604	CH_DITHER_COEF0	0x3860_8000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dither_coef3								dither_coef2								dither_coef1								dither_coef0							
Reset	0	0	1	1	1	0	0	0	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	dither_coef3	Dither coefficient in time-domain mode.
[23:16]	RW	dither_coef2	Dither coefficient in time-domain mode.
[15:8]	RW	dither_coef1	Dither coefficient in time-domain mode.
[7:0]	RW	dither_coef0	Dither coefficient in time-domain mode.

CH_DITHER_COEF1

CH_DITHER_COEF1 is dither coefficient register 1.

Offset Address	Register Name	Total Reset Value
0x1608	CH_DITHER_COEF1	0xFBE7_0F1E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dither_coef7								dither_coef6								dither_coef5								dither_coef4							
Reset	1	1	1	1	1	0	1	1	1	1	1	0	0	1	1	1	0	0	0	0	1	1	1	1	0	0	0	1	1	1	1	0

Bits	Access	Name	Description
[31:24]	RW	dither_coef7	Dither coefficient in time-domain mode.
[23:16]	RW	dither_coef6	Dither coefficient in time-domain mode.
[15:8]	RW	dither_coef5	Dither coefficient in time-domain mode.
[7:0]	RW	dither_coef4	Dither coefficient in time-domain mode.

CH_DITHER_Y_SIZE

CH_DITHER_Y_SIZE is a Y component input size register for the dither module.

Offset Address	Register Name	Total Reset Value
0x1610	CH_DITHER_Y_SIZE	0x0000_04FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved.
[12:0]	RW	width	Width of a picture line. Its unit is pixel. The configured value is the actual value minus 1.

CH_DITHER_C_SIZE

CH_DITHER_C_SIZE is a C component input size register for the dither module.

Offset Address	Register Name	Total Reset Value
0x1614	CH_DITHER_C_SIZE	0x0000_04FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved.
[12:0]	RW	width	Width of a picture line. Its unit is pixel. The configured value is the actual value minus 1.

CH_VCDS_CFG

CH_VCDS_CFG is a chrominance vertical down sampling configuration register.

Offset Address	Register Name	Total Reset Value
0x1700	CH_VCDS_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	Down sampling enable. 0: disabled 1: enabled
[30:0]	-	reserved	Reserved.

CH_VCDS_COEF

CH_VCDS_COEF is a chrominance vertical down sampling coefficient register.

Offset Address	Register Name	Total Reset Value
0x1704	CH_VCDS_COEF	0x0000_001F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												coef1				reserved												coef0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[31:21]	-	reserved	Reserved.
[20:16]	RW	coef1	Down sampling coefficient 1.
[15:5]	-	reserved	Reserved.
[4:0]	RW	coef0	Down sampling coefficient 0.

CH_HLDC_CFG

CH_HLDC_CFG is a horizontal lens distortion correction (HLDC) configuration register.

Offset Address	Register Name	Total Reset Value
0x1800	CH_HLDC_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																														round_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	Lens distortion correction enable. 1: disabled 1: enabled
[30:1]	-	reserved	Reserved.
[0]	RW	round_en	Round off enable. 1: disabled 1: enabled

CH_HLDC_SIZE

CH_HLDC_SIZE is an HLDC input picture size register.

Offset Address	Register Name	Total Reset Value
0x1804	CH_HLDC_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27:16]	RW	height	Input picture height for HLDC. Its unit is pixel. The configured value is the actual value minus 1.
[15:12]	-	reserved	Reserved.
[11:0]	RW	width	Input picture width for HLDC. Its unit is pixel. The configured value is the actual value minus 1.

CH_HLDC_DEL

CH_HLDC_DEL is an HLDC output delay register.

Offset Address	Register Name	Total Reset Value
0x1808	CH_HLDC_DEL	0x0000_00F0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																delay															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	delay	Output delay.

CH_HLDC_COEF0

CH_HLDC_COEF0 is HLDC coefficient register 0.

Offset Address	Register Name	Total Reset Value
0x1810	CH_HLDC_COEF0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								c2								reserved				c1											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.
[25:16]	RW	c2	Vertical coordinate of the distortion center.
[15:11]	-	reserved	Reserved.
[10:0]	RW	c1	Horizontal coordinate of the distortion center.

CH_HLDC_COEF1

CH_HLDC_COEF1 is HLDC coefficient register 1.

Offset Address	Register Name	Total Reset Value
0x1814	CH_HLDC_COEF1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								k2								reserved				k1											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	-	reserved	Reserved.
[24:16]	RW	k2	Ellipse mapping coefficient k2.
[15:11]	-	reserved	Reserved.
[10:0]	RW	k1	Ellipse mapping coefficient k1.

CH_HLDC_COEF2

CH_HLDC_COEF2 is HLDC coefficient register 2.

Offset Address	Register Name	Total Reset Value
0x1818	CH_HLDC_COEF2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								hc2								reserved								hc1							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:16]	RW	hc2	Trapezoid mapping coefficient hc2.
[15:8]	-	reserved	Reserved.
[7:0]	RW	hc1	Trapezoid mapping coefficient hc1.

CH_HLDC_COEF3

CH_HLDC_COEF3 is HLDC coefficient register 3.

Offset Address	Register Name	Total Reset Value
0x181C	CH_HLDC_COEF3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					f_h										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	-	reserved	Reserved.
[10:0]	RW	f_h	Coefficient f_h.

CH_CLIP_Y_CFG

CH_CLIP_Y_CFG is a Y component configuration register for the clip module.

Offset Address	Register Name	Total Reset Value
0x1900	CH_CLIP_Y_CFG	0xFFFF_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max												reserved				min												reserved			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RW	max	Maximum output value. The value format is (u, 8, 4). That is, the value consists of a 1-bit unsigned part, an 8-bit integral part, and a 4-bit fractional part.
[19:16]	-	reserved	Reserved.
[15:4]	RW	min	Minimum output value. The value format is (u, 8, 4). That is, the value consists of a 1-bit unsigned part, an 8-bit integral part, and a 4-bit fractional part.
[3:0]	-	reserved	Reserved.

CH_CLIP_C_CFG

CH_CLIP_C_CFG is a C component configuration register for the clip module.

Offset Address	Register Name	Total Reset Value
0x1904	CH_CLIP_C_CFG	0xFFFF_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max												reserved				min												reserved			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RW	max	Maximum output value. The value format is (u, 8, 4). That is, the value consists of a 1-bit unsigned part, an 8-bit integral part, and a 4-bit fractional part.
[19:16]	-	reserved	Reserved.
[15:4]	RW	min	Minimum output value. The value format is (u, 8, 4). That is, the value consists of a 1-bit unsigned part, an 8-bit integral part, and a 4-bit fractional part.
[3:0]	-	reserved	Reserved.

CH_SUM_Y

CH_SUM_Y is an input picture luminance statistics register.

Offset Address	Register Name	Total Reset Value
0x1A00	CH_SUM_Y	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sum_y																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sum_y	Luminance statistics.

ISP_INT

ISP_INT is an ISP interrupt indicator register.

Offset Address	Register Name	Total Reset Value
0x100F0	ISP_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								int7	int6	int5	int4	int3	int2	int1	int0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved.
[7]	WC	int7	ISP interrupt 7 indicator. Writing 1 clears the indicator. 0: No interrupt is generated. 1: An interrupt is generated.
[6]	WC	int6	ISP interrupt 6 indicator. Writing 1 clears the indicator. 0: No interrupt is generated. 1: An interrupt is generated.
[5]	WC	int5	ISP interrupt 5 indicator. Writing 1 clears the indicator. 0: No interrupt is generated. 1: An interrupt is generated.
[4]	WC	int4	ISP interrupt 4 indicator. Writing 1 clears the indicator. 0: No interrupt is generated. 1: An interrupt is generated.
[3]	WC	int3	ISP interrupt 3 indicator. Writing 1 clears the indicator. 0: No interrupt is generated. 1: An interrupt is generated.

Offset Address	Register Name	Total Reset Value
0x100F0	ISP_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								int7	int6	int5	int4	int3	int2	int1	int0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[2]	WC	int2	ISP interrupt 2 indicator. Writing 1 clears the indicator. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	WC	int1	ISP interrupt 1 indicator. Writing 1 clears the indicator. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	WC	int0	ISP interrupt 0 indicator. Writing 1 clears the indicator. 0: No interrupt is generated. 1: An interrupt is generated.

ISP_INT_MASK

ISP_INT_MASK is an ISP interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x100F8	ISP_INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								int7_en	int6_en	int5_en	int4_en	int3_en	int2_en	int1_en	int0_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved.
[7]	RW	int7_en	ISP interrupt 7 mask. 0: No interrupt is generated. 1: An interrupt is generated.
[6]	RW	int6_en	ISP interrupt 6 mask. 0: No interrupt is generated. 1: An interrupt is generated.

Offset Address	Register Name	Total Reset Value
0x100F8	ISP_INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								int7_en	int6_en	int5_en	int4_en	int3_en	int2_en	int1_en	int0_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[5]	RW	int5_en	ISP interrupt 5 mask. 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RW	int4_en	ISP interrupt 4 mask. 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RW	int3_en	ISP interrupt 3 mask. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RW	int2_en	ISP interrupt 2 mask. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RW	int1_en	ISP interrupt 1 mask. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RW	int0_en	ISP interrupt 0 mask. 0: No interrupt is generated. 1: An interrupt is generated.

10.2 VDP

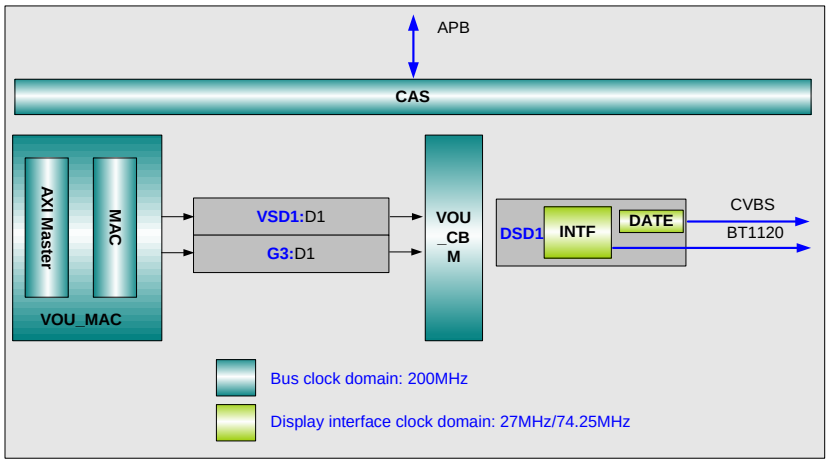
10.2.1 Overview

The video display (VDP) module reads video and graphics data from the DDR, overlays the data on the video and graphics layers, and transmits the data through the display channel.

10.2.2 Function Description

Figure 10-15 shows the overall architecture of the VDP module.

Figure 10-15 Overall architecture of the VDP module



- Surfaces: data paths of bus inputs. The surface reads the bus data of a layer and processes data. The surfaces include video layers VSD1, and graphics layers G3.
- Display channel: Display channels include standard-definition display channel DSD1.
- Crossbar and mixer (CBM): It overlays the video layer and graphics layers.
- MAC: bus request arbitration module of each layer. Each module reads data from the DDR over the AXI bus. The MAC arbitrates when layers raise requests.
- Control and status (CAS): It configures registers over the APB and reports the status of other modules to the CPU.

The VDP registers are classified into:

- Global registers

  Include the bus configuration register, interrupt register, and version register.
- Surface registers

  Include the video layer configuration register and graphics layer configuration register.
- Display channel registers

  Include the DSD1 configuration registers.

The VDP module has the following features:

- Digital output interfaces: ITU-R BT.1120 HD output
- Analog output interfaces: CVBS output from DSD1
- Video layer
  - Input pixel formats: semi-planar YCbCr4:2:2 and semi-planar YCbCr4:2:0
  - Global alpha
  - Color space conversion (CSC) and adjustment of luminance, contrast, hue, and saturation
  - Vertical chrominance up sampling
  - Horizontal chrominance up sampling
  - Read/write on regions 0 (for VSD1)
- Graphics layer

  - One graphics layer: graphics layers 3.
  - Data formats: ARGB4444 and ARGB1555
  - Global alpha and pixel alpha
  - Three data extended modes

    Lower bits stuffed with 0s

    Lower bits stuffed with the MSB

    Lower bits stuffed with upper bits
  - Even width and height
  - Minimum input/output resolution 32x32 and maximum input/output resolution 1920x1080 for G3
- Overlay
  - 256-level alpha blending of one background layer, one video layers, and one graphics layer. The priorities of graphics layers and video layers can be set and the alpha value of the layer with the highest priority is used during overlay.
  - Adjustment of the size and position of each overlay layer
  - Adjustment of the luminance, contrast, hue, and saturation of overlaid pictures–
- The VDP module has one SD channel. The channel has a s vertical timing interrupt (indicating the end of a field/frame), one low bandwidth interrupt.

10.2.3 Operating Mode

10.2.3.1 Clock Configuration

The VDP module has three clock sources:

- VPLL0
- VPLL2
- AXI bus clock

Table 10-6 describe the mappings between channel interface types and PLL configurations. To look up the PLL configuration based on a channel, perform the following steps:

Step 1 Specify a channel.

Step 2 Look up the interface type in the table corresponding to the specified channel.

Step 3 Look up the PLL and DATA and DAC configurations in the corresponding interface type row.

----End

Table 10-6 Clock configuration of DSD1

	DSD1	PLL0, PLL1, or PLL2 (MHz)	SDATE (MHz)	DAC0 (MHz)
CVBS	27	27	54	54
BT1120	74.25	74.25	N/A	N/A

10.2.3.2 Reset

The VDP module can be reset by a hard reset or soft reset.

The VDP module has the following three soft reset signals (writing 1 to the corresponding clock reset control bit resets the corresponding module and writing 0 deasserts the reset):

- DSD channels Soft reset
- AXI bus soft reset

CAUTION

Before soft-reset the AXI bus, do as follows:

- Disable all layers.
- Configure the bus reset request after the next field/frame interrupt is detected.

10.2.3.3 Bus Configurations

AXI Masters

The VDP module provides one master interface to improve the bus access efficiency. As the VDP module supports AXI master interfaces, VSD1, or G3 can read or write data over master.

Register Configuration

The VDP registers are read and written over the APB interface. The APB clock is 100 MHz. For the Hi3518, the base address of VDP registers is 0x205C_0000, the register addressing space is 64 KB, and the address offset range is 0x0000–0xFFFF.

Outstanding Configuration

The depth of the AXI master outstanding ranges from 0 to 7. When the outstanding depth is set to 0, the AXI master does not operate the bus.

10.2.3.4 Analog Output Interfaces

The SD channels support one CVBS output interface. The VDP module provides the following analog output interfaces:

- DSD1->CVBS
- PAL and NTSC norms supported by the CVBS interfaces

10.2.3.5 Digital Output Interfaces

The VDP module supports ITU-R BT.1120 interface

ITU-R BT.1120 Interface

The VDP module supports the BT.1120 interface.

- External synchronization, line/field synchronization, and data active

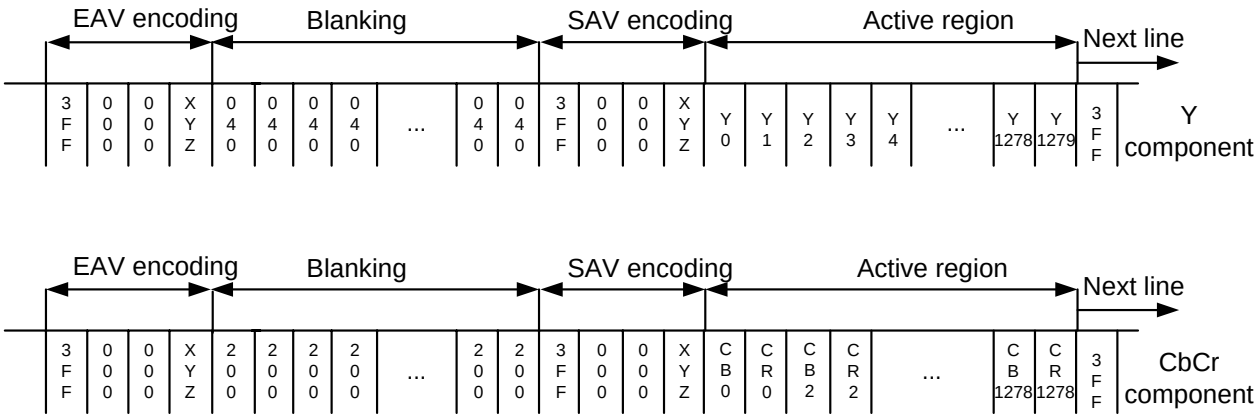
- Maximum output resolution of 1920x1080
- Data Y/C exchange

In BT.656 mode, sync signals are included in video data streams. The special bytes SAV and EAV in data streams indicate the start and end of the line respectively.

According to the ITU-R BT.1120 YCbCr 4:2:2, the ratio of sampled luminance signals to sampled chrominance signals is 2:1. Two luminance signals share a CbCr signal.

Figure 10-16 shows the scanning timing at the resolution of 1280x720p. Luminance signals and chrominance signals are transmitted in different channels, and the clock frequency is 74.25 MHz.

Figure 10-16 Horizontal timing of the BT.1120 interface



10.2.3.6 Video Layers

Features

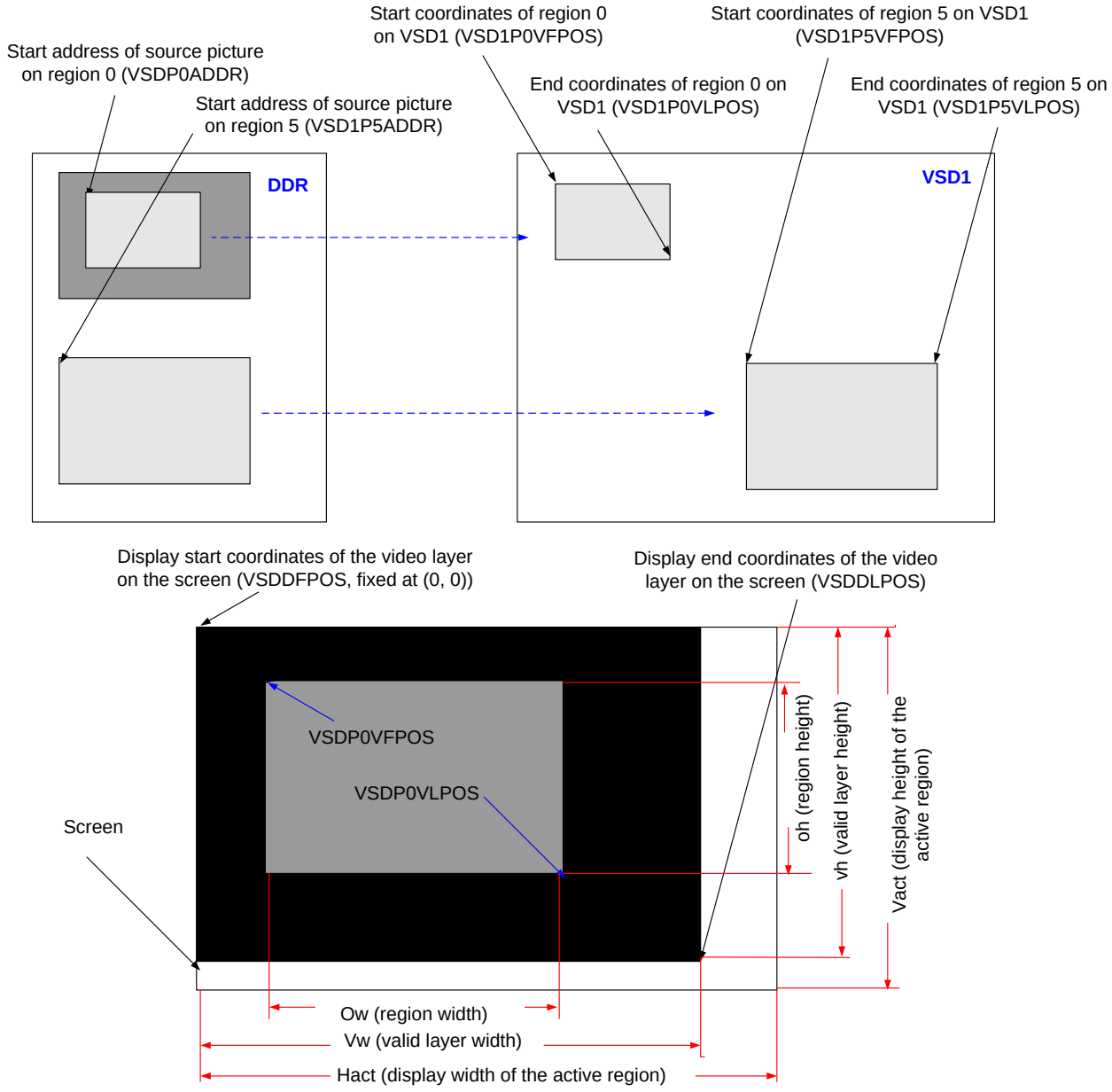
- VSD1 supports only one region.
- Input pixel formats of semi-planar420 and semi-planar422
- Minimum input resolution of 32x32 and maximum input resolution of 1920x1080
- Minimum output resolution of 32x32 and maximum output resolution of 1920x1080
- A multiple of 2 for the input horizontal resolution and a multiple of 4 for the input vertical resolution
- Interlaced mode and progressive mode
- User-defined source luminance and chrominance start addresses, 2-byte-aligned
- User-defined source luminance and chrominance stride, 16-byte-aligned
- Optional horizontal chrominance up scaling (IFIR), replication mode, bilinear interpolation, and 6-tap filtering
- CSC from YCbCr to RGB and adjustment of contrast, hue, and saturation
- User-defined display position, anywhere on the screen
- Frame/field update mode
- User-defined global alpha ranging from 0 to 255

Display Position

The VDP module allows you to set the video display position.

- The video layer has three sets of coordinates.
- Source start coordinates for reading data. The VDP module is configured with the start address calculated by the CPU.
- Start and end coordinates of the video layer relative to the displayed area
- Display start and end coordinates of the video layer on the screen
- The combination of three sets of coordinates enables video sources to be displayed anywhere on the screen.

Figure 10-17 Three sets of coordinates



CAUTION

The display start coordinates of the video layer on the screen must be set to (0, 0).

420-422 (Vertical Chrominance Up Sampling)

When YUV420 data is input, 2x vertical scaling must be performed on the chrominance to convert the data format into YUV422. The data format of the VSD1 is converted in replication mode.

IFIR (Horizontal Chrominance Up Sampling)

After horizontal chrominance up sampling, the YUV422 data format is converted into YUV444.

This function can be implemented in three ways:

- Replication
- Bilinear interpolation
- 8-tap filtering

CSC

- CSC between YUV709 and YUV601
- CSC between RGB and YUV

10.2.3.7 Graphics Layers

CSC

The CSCs among RGB2YCbCr601and RGB2YCbCr709 are supported.

Alpha Processing

The alpha value sources of graphics layers are as follows:

- Pixel alpha value: overlay attribute of a pixel
- Global alpha value: overlay attributes of a layer

There is a special case for the pixel alpha value. In RGB1555 format, the alpha value is only one bit. This bit is the index of the alpha value rather than the actual alpha value. The index value is used to select the actual alpha value from the alpha register. When the index value is 0, alpha0 is selected; when the index value is other values, alpha1 is selected.

10.2.3.8 Layer Overlay

The VDP supports one mixer. The data of the mixer is output through specific channels. The mapping between mixers and output channel is as follows: MIX4 —> DSD1

The binding relationship is as follows: VSD1 and G3 are always bound to mixer 4.

The following configurations are performed:

Step 1 Disable related VO interfaces.

Step 2 Configure sur_attrix to determine the connections of layers.

Step 3 Configure the registers of each layer.

Step 4 Configure the priority of each layer.

Step 5 Enable related VO interfaces.

----End

10.2.3.9 Processing Functions of HD Channels

Timing Configuration

NOTE

- HFB = horizontal front blanking
- HBB = horizontal back blanking
- HACT = horizontal active
- HPW = horizontal pulse width
- VFB = vertical front blanking
- VBB = vertical back blanking
- VACT = vertical active
- VPW = vertical pulse width
- BVFB = bottom vertical front blanking
- BVBB = bottom vertical back blanking
- BVACT = bottom vertical active
- BVPW = bottom vertical pulse width
- HMID = horizontal middle

The VDP output interfaces support typical and non-typical timings to connect to different interfaces.

- Maximum resolution 1920x1080 for the DSD1 interface
- Interface horizontal timing parameters
  - HFB: 16-bit width, 1–65535 clock cycles
  - HBB: 16-bit width, 1–65535 clock cycles
  - HACT: 16-bit width, 1–65535 clock cycles
  - HPW: 16-bit width, 1–65535 clock cycles
- Interface vertical timing parameters
  - VFB: 8-bit width, 1–256 lines
  - VBB: 8-bit width, 5–256 lines
  - VACT: 12-bit width, 1–256 lines
  - VPW: 16-bit width, 1–65535 lines
- Interlaced timing parameters
  - BVFB: 8-bit width, 1–256 lines
  - BVBB: 8-bit width, 5–256 lines
  - BVACT: 12-bit width, 1–256 lines
  - BVPW: 16-bit width, 1–65535 lines

– HMID: 16-bit, 1–65535 clock cycles. The clock cycle indicate the clock cycle of a pixel relative to the active region in a line.

CAUTION

- Number of clocks in a line = HFB + HBB + HACT x (n clock/pixel). Note that HDW must be smaller than HBB.
- Number of frames in a line = VFB + VBB + VACT. Note that VPW must be smaller than VBB and BVPW must be smaller than BVBB.
- Interfaces must be disabled before you set all timing parameters.

DFIR

You can determine whether to enable the DFIR function. Typically, the 1, 2, 1 filtering mode is used and the filtering performance is 1 pixel/clock.

Clip

The VDP provides flexible clip function.

- According to the interface timing protocol, the output data must be within a range. If the data exceeds the range, the data must be clipped.
- You can determine whether to enable the clip function. The upper and lower limits for clipping can be configured and the clipping performance is 1 pixel/clock.

Gamma Correction

The VDP module supports gamma correction. You can determine whether to enable gamma correction.

10.2.3.10 Processing Functions of SD Channels

The VDP supports one video channels. The details are as follows:

- SD channels of DSD1
- Maximum resolution 1920x1080
- CVBS interface supported only by DSD1
- Chrominance down sampling DFIR enable
- Clip enable
- User-defined upper and lower limits for clipping

10.2.3.11 Interrupts

The VDP interrupts are classified into:

- Vertical timing interrupt
- Low bandwidth interrupt
- VDAC non-load interrupt

Vertical Timing Interrupt

The VDP module supports the vertical timing interrupt. The positions of generating interrupts can be configured. The details are as follows:

- The vertical timing interrupt indicates the end of a frame or field.
- Interrupt generation modes: generated by frame and generated by field.
- Mode of generating vertical timing interrupts configured as generated by frame in progressive display mode.
- Mode of generating vertical timing interrupts configured as generated by frame or by field in interlaced display mode. You are advised to set the interrupt generation mode to generated by field for HD and generated by field for SD.
- Configurable interrupt mask.
- Configurable threshold of vertical timing interrupts.
- Separate enabling and disabling of each interrupt source. Writing 1 clears the interrupt.

Low Bandwidth Interrupt

The VDP module supports the low bandwidth interrupt. The details are as follows:

- The low bandwidth interrupt that indicates the low bandwidth information about a frame or field
- Interrupt generation modes: generated by frame and generated by field.
- Mode of generating vertical timing interrupts configured as generated by frame in progressive display mode.
- Mode of generating vertical timing interrupts configured as generated by frame or by field in interlaced display mode. You are advised to set the interrupt generation mode to generated by field for HD and generated by field for SD.
- Configurable interrupt mask.
- Separate enabling and disabling of each interrupt source. Writing 1 clears the interrupt.

VDAC Non-Load Interrupt

The VDP module allows the VDAC connection status to be reported as interrupts. The details are as follows:

- The VDP module has a VDAC non-load interrupt, indicating that the current VDAC does not connect to any load.
- Configurable interrupt mask.
- Separate enabling and disabling of each interrupt source. Writing 1 clears the interrupt.

10.2.4 Register Summary

Table 10-8 describes the VDP registers.

Table 10-8 Summary of VDP registers (base address: 0x205C_0000)

Offset Address	Register	Description	Page
0x4000	VSD1CTRL	VSD control register	10-99

Offset Address	Register	Description	Page
0x4004	VSD1UPD	VSD channel update enable register	10-100
0x4010	VSD1CADDR	VSD current frame address register	10-100
0x4014	VSD1CCADDR	VSD current frame chrominance address register	10-101
0x4024	VSD1STRIDE	VSD surface stride register	10-101
0x4028	VSD1IRESO	VSD input resolution register	10-101
0x4034	VSD1CBMPARA	VSD overlay parameter register	10-102
0x4060	VSD1DFPOS	VSD surface start position (in the display window) register	10-102
0x4064	VSD1DLPOS	VSD surface end position (in the display window) register	10-103
0x4068	VSD1VFPOS	VSD surface content start position (in the display window) register	10-103
0x406C	VSD1VLPOS	VSD surface content end position (in the display window) register	10-104
0x4070	VSD1BK	Video layer background color register	10-104
0x4080	VSD1CSCIDC	VSD input DC component register for CSC	10-105
0x4084	VSD1CSCODC	VSD output DC component register for CSC	10-105
0x4088	VSD1CSCP0	VSD CSC parameter 0 register	10-106
0x408C	VSD1CSCP1	VSD CSC parameter 1 register	10-107
0x4090	VSD1CSCP2	VSD CSC parameter 2 register	10-107
0x4094	VSD1CSCP3	VSD CSC parameter 3 register	10-108
0x4098	VSD1CSCP4	VSD CSC parameter 4 register	10-108
0x4180	VSD1IFIRCOEF01	VSD IFIR filtering coefficients 0–1 register	10-109

Offset Address	Register	Description	Page
0x4184	VSD1IFIRCOEF23	VSD IFIR filtering coefficients 2–3 register	10-109
0x4188	VSD1IFIRCOEF45	VSD IFIR filtering coefficients 4–5 register	10-110
0x418C	VSD1IFIRCOEF67	VSD IFIR filtering coefficients 6–7 register	10-110
0x4400	VSD1P0RESO	VSD region 0 resolution register	10-110
0x4404	VSD1P0LADDR	VSD region 0 address register	10-111
0x4408	VSD1P0CADDR	VSD region 0 chrominance address register	10-111
0x440C	VSD1P0STRIDE	VSD region 0 stride register	10-112
0x4410	VSD1P0VFPOS	VSD region 0 video start position register	10-112
0x4414	VSD1P0VLPOS	VSD region 0 video end position register	10-113
0x4C04	VSD116REGIONEN	VSD1 region enable register	10-113
0x9600	G3CTRL	G3 control register	10-114
0x9604	G3UPD	G3 update enable register	10-114
0x9608	G3ADDR	G3 address register	10-115
0x960C	G3STRIDE	G3 stride register	10-115
0x9610	G3CBMPARA	G3 overlay parameter register	10-116
0x9614	G3CKEYMAX	G3 maximum colorkey register	10-117
0x9618	G3CKEYMIN	G3 minimum colorkey register	10-117
0x961C	G3CMASK	G3 colorkey mask value register	10-118
0x9620	G3IRESO	G3 input resolution register	10-118
0x9624	G3ORESO	G3 output resolution register	10-119
0x962C	G3DFPOS	G3 surface start position (in the display window) register	10-119
0x9630	G3DLPOS	G3 surface end position (in the display window) register	10-120
0x96A0	G3CSCIDC	G3 input DC component register for CSC	10-120

Offset Address	Register	Description	Page
0x96A4	G3CSCODC	G3 output DC component register for CSC	10-121
0x96A8	G3CSCP0	G3 CSC parameter 0 register	10-121
0x96AC	G3CSCP1	G3 CSC parameter 1 register	10-122
0x96B0	G3CSCP2	G3 CSC parameter 2 register	10-123
0x96B4	G3CSCP3	G3 CSC parameter 3 register	10-123
0x96B8	G3CSCP4	G3 CSC parameter 4 register	10-124
0x9E0C	CBMBKG4	SD1 overlay background color register	10-124
0xAC00	DSD1CTRL	DSD1 global control register	10-125
0xAC04	DSD1VSYNC	DSD1 vertical timing register	10-127
0xAC08	DSD1HSYNC1	DSD1 horizontal timing register 1	10-127
0xAC0C	DSD1HSYNC2	DSD1 horizontal timing register 2	10-128
0xAC10	DSD1VPLUS	DSD1 bottom vertical sync timing register in interlaced output mode	10-129
0xAC14	DSD1PWR	DSD1 sync signal pulse width register	10-129
0xAC1C	DSD1VTTHD	DSD1 vertical timing threshold register	10-130
0xAC40	DSD1CLIPL	DSD1 clip lower threshold register	10-131
0xAC44	DSD1CLIPH	DSD1 clip upper threshold register	10-131
0xACF0	DSD1STATE	DSD1 status register	10-132
0xC204	DATE_COEFF1	DATE amplitude configuration register	10-133
0xC21C	DATE_COEFF7	DATE teletext configuration register	10-134
0xC220	DATE_COEFF8	DATE teletext configuration register	10-137
0xC224	DATE_COEFF9	DATE teletext configuration register	10-137
0xC228	DATE_COEFF10	DATE teletext configuration register	10-137

Offset Address	Register	Description	Page
0xC22C	DATE_COEFF11	DATE closed caption configuration register	10-139
0xC230	DATE_COEFF12	DATE closed caption configuration register	10-139
0xC234	DATE_COEFF13	DATE CGMS configuration register	10-140
0xC238	DATE_COEFF14	DATE CGMS configuration register	10-140
0xC23C	DATE_COEFF15	DATE WSS configuration register	10-141
0xC240	DATE_COEFF16	DATE VPS configuration register	10-141
0xC244	DATE_COEFF17	DATE VPS configuration register	10-142
0xC248	DATE_COEFF18	DATE VPS configuration register	10-142
0xC24C	DATE_COEFF19	DATE VPS configuration register	10-142
0xC250	DATE_COEFF20	DATE teletext configuration register	10-143
0xC258	DATE_COEFF22	DATE discrete time oscillator (DTO) initial phase configuration register	10-144
0xC280	DATE_ISRMASK	DATE interrupt mask register	10-144
0xC284	DATE_ISRSTATE	DATE interrupt status register	10-144
0xC288	DATE_ISR	DATE interrupt register	10-144
0xC400	DATE1_COEFF0	DATE1 norm parameter configuration register	10-146
0xC404	DATE1_COEFF1	DATE1 amplitude configuration register	10-150
0xC41C	DATE1_COEFF7	DATE1 teletext configuration register	10-151
0xC420	DATE1_COEFF8	DATE1 teletext configuration register	10-154
0xC424	DATE1_COEFF9	DATE1 teletext configuration register	10-154
0xC428	DATE1_COEFF10	DATE1 teletext configuration register	10-155

Offset Address	Register	Description	Page
0xC42C	DATE1_COEFF11	DATE1 closed caption configuration register	10-156
0xC430	DATE1_COEFF12	DATE1 closed caption configuration register	10-156
0xC434	DATE1_COEFF13	DATE1 CGMS configuration register	10-157
0xC438	DATE1_COEFF14	DATE1 CGMS configuration register	10-157
0xC43C	DATE1_COEFF15	DATE1 WSS configuration register	10-158
0xC440	DATE1_COEFF16	DATE1 VPS configuration register	10-158
0xC444	DATE1_COEFF17	DATE1 VPS configuration register	10-159
0xC448	DATE1_COEFF18	DATE1 VPS configuration register	10-159
0xC44C	DATE1_COEFF19	DATE1 VPS configuration register	10-160
0xC450	DATE1_COEFF20	DATE1 teletext configuration register	10-160
0xC454	DATE1_COEFF21	DATE1 output matrix control register	10-161
0xC458	DATE1_COEFF22	DATE1 DTO initial phase configuration register	10-163
0xC45C	DATE1_COEFF23	DATE1 video output delay configuration register	10-164
0xC480	DATE1_ISRMASK	DATE1 interrupt mask register	10-165
0xC484	DATE1_ISRSTATE	DATE1 interrupt status register	10-166
0xC488	DATE1_ISR	DATE1 interrupt register	10-165
0xC490	DATE1_VERSION	DATE1 version register	10-167
0xC4AC	DATE_DACDET1	VDAC detection register 1	10-167
0xC4B0	DATE_DACDET2	VDAC detection register 2	10-167
0xCE00	VOCTRL	VO control register	10-168
0xCE04	VOINTSTA	VO interrupt status register	10-169

Offset Address	Register	Description	Page
0xCE08	VOMSKINTSTA	VO masked interrupt status register	10-170
0xCE0C	VOINTMSK	VDP interrupt mask register	10-171
0xCE10	VOUVERSION1	VDP version register 1	10-172
0xCE14	VOUVERSION2	VDP version register 2	10-173

10.2.5 Register Description

VSD1CTRL

VSD1CTRL is a VSD control register (non-instant register). It is used to configure the layer information

Offset Address	Register Name	Total Reset Value
0x4000	VSD1CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_en	reserved											ifir_mode		vup_mode		reserved												ifmt			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	surface_en	Surface enable (non-instant register). 0: disabled 1: enabled
[30:20]	-	reserved	Reserved.
[19:18]	RW	ifir_mode	Horizontal chrominance IFIR mode. 00: reserved 01: chrominance IFIR copy mode 10: bilinear interpolation 11: 6-tap FIR
[17]	-	vup_mode	Register update mode. 0: update by field 1: update by frame
[16:4]	-	reserved	Reserved.

[3:0]	RW	ifmt	Input data format. 0x3: SPYCbCr420 0x4: SPYCbCr422 Other values: reserved

VSD1UPD

VSD1UPD is a VSD channel update enable register.

Offset Address	Register Name	Total Reset Value
0x4004	VSD1UPD	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							regup
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	regup	Surface register update. After the registers at this layer are configured, the registers are updated when the value 1 is written to this bit. After updates, this bit is cleared automatically by the hardware.

VSD1CADDR

VSD1CADDR is a VSD current frame address register. In package pixel format, the address is the address of the frame buffer; in semi-planar pixel format, the address is the address of the luminance frame buffer.

Offset Address	Register Name	Total Reset Value
0x4010	VSD1CADDR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	surface_caddr							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	surface_caddr	Address of the current frame.

VSD1CCADDR

VSD1CCADDR is a VSD current frame chrominance address register. In package pixel format, the address is invalid; in semi-planar pixel format, the address is the address of the luminance frame buffer.

Offset Address	Register Name	Total Reset Value
0x4014	VSD1CCADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_ccaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_ccaddr	Chrominance address of the current frame.

VSD1STRIDE

VSD1STRIDE is a VSD surface stride register.

Offset Address	Register Name	Total Reset Value
0x4024	VSD1STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_cstride																surface_stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	surface_cstride	Stride of the chrominance frame buffer (valid in semi-planar format), 128-bit alignment.
[15:0]	RW	surface_stride	Stride of the frame buffer (valid in semi-planar format, luminance stride), 128-bit alignment.

VSD1IRESO

VSD1IRESO is a VSD input resolution register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x4028	VSD1IRESO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ih												iw											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:12]	RW	ih	Height (in line). The value is the actual height minus 1. The frame height is referenced.
[11:0]	RW	iw	Width (in pixel). The value is the actual width minus 1.

VSD1CBMPARA

VSD1CBMPARA is a VSD overlay parameter register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x4034	VSD1CBMPARA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								galpha							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.
[7:0]	RW	galpha	Overlay global alpha value. The value ranges from 0 to 128. The value 128 indicates opaque, and the value 0 indicates full transparent.

VSD1DFPOS

VSD1DFPOS is a VSD surface start position (in the display window) register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x4060	VSD1DFPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								disp_yfpos												disp_xfpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:12]	RW	disp_yfpos	Start coordinate of the display column. The frame height is referenced and the unit is line.
[11:0]	RW	disp_xfpos	Start coordinate of the display row.

VSD1DLPOS

VSD1DLPOS is a VSD surface end position (in the display window) register (non-instant register). The end position is in the unit of pixel.

Offset Address	Register Name	Total Reset Value
0x4064	VSD1DLPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								disp_ylpos												disp_xlpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:12]	RW	disp_ylpos	End coordinate of the display column. The frame height is referenced and the unit is line.
[11:0]	RW	disp_xlpos	End coordinate of the display row.

VSD1VFPOS

VSD1VFPOS is a VSD surface content start position (in the display window) register (non-instant register). The start position is in the unit of pixel.

Offset Address	Register Name	Total Reset Value
0x3068	VSD1VFPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								disp_ylpos												disp_xlpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:12]	RW	video_yfpos	Start coordinate of the video column. The frame height is referenced and the unit is line.
[11:0]	RW	video_xfpos	Start coordinate of the video row.

VSD1VLPOS

VSD1VLPOS is a VSD surface content end position (in the display window) register (non-instant register). The end position is in the unit of pixel.

Offset Address	Register Name	Total Reset Value
0x306C	VSD1VLPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								video_ylpos												video_xlpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:12]	RW	video_ylpos	End coordinate of the video column. The frame height is referenced and the unit is line.
[11:0]	RW	video_xlpos	End coordinate of the video row.

VSD1BK

VSD1BK is a video layer background color register.

Offset Address	Register Name	Total Reset Value
0x4070	VSD1BK	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	vbk_alpha		vbk_y		vbk_cb		vbk_cr	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	vbk_alpha	Levels 0–128 of the background filling color of the video layer.
[23:16]	RW	vbk_y	Y component.
[15:8]	RW	vbk_cb	Cb component.
[7:0]	RW	vbk_cr	Cr component.

VSD1CSCIDC

VSD1CSCIDC is a VSD input DC component register for CSC (instant register).

Offset Address	Register Name	Total Reset Value
0x4080	VSD1CSCIDC	0x0000_0000

Bit	31 30 29 28	27	26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	csc_en	cscidc2		cscidc1		cscidc0		
Reset	0 0 0 0	0	0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27]	RW	csc_en	CSC enable. 0: disabled 1: enabled
[26:18]	RW	cscidc2	DC parameter of input component 2. The MSB is the signed bit. The value is expressed as the complementary code.
[17:9]	RW	cscidc1	DC parameter of input component 1. The MSB is the signed bit. The value is expressed as the complementary code.
[8:0]	RW	cscidc0	DC parameter of input component 0. The MSB is the signed bit. The value is expressed as the complementary code.

VSD1CSCODC

VSD1CSCODC is a VSD output DC component register for CSC (instant register).

Offset Address	Register Name	Total Reset Value
0x4084	VSD1CSCODC	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	cscodc2		cscodc1		cscodc0		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	-	reserved	Reserved.
[26:18]	RW	cscodc2	DC parameter of output component 2. The MSB is the signed bit. The value is expressed as the complementary code.
[17:9]	RW	cscodc1	DC parameter of output component 1. The MSB is the signed bit. The value is expressed as the complementary code.
[8:0]	RW	cscodc0	DC parameter of output component 0. The MSB is the signed bit. The value is expressed as the complementary code.

VSD1CSCP0

VSD1CSCP0 is VSD CSC parameter 0 register (instant register).

Offset Address	Register Name	Total Reset Value
0x4088	VSD1CSCP0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	cscp01			reserved	cscp00		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RW	cscp01	5.8 data format. The value consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complementary code.
[15:13]	-	reserved	Reserved.
[12:0]	RW	cscp00	5.8 data format. The value consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complementary code.

VSD1CSCP1

VSD1CSCP1 is VSD CSC parameter 1 register (instant register).

Offset Address	Register Name	Total Reset Value
0x408C	VSD1CSCP1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp10												reserved				cscp02											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RW	cscp10	5.8 data format. The value consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complementary code.
[15:13]	-	reserved	Reserved.
[12:0]	RW	cscp02	5.8 data format. The value consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complementary code.

VSD1CSCP2

VSD1CSCP2 is VSD CSC parameter 2 register (instant register).

Offset Address	Register Name	Total Reset Value
0x4090	VSD1CSCP2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp12												reserved				cscp11											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RW	cscp12	5.8 data format. The value consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complementary code.
[15:13]	-	reserved	Reserved.

[12:0]	RW	cscp11	5.8 data format. The value consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complementary code.

VSD1CSCP3

VSD1CSCP3 is VSD CSC parameter 3 register (instant register).

Offset Address	Register Name	Total Reset Value
0x4094	VSD1CSCP3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp21												reserved				cscp20											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RW	cscp21	5.8 data format. The value consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complementary code.
[15:13]	-	reserved	Reserved.
[12:0]	RW	cscp20	5.8 data format. The value consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complementary code.

VSD1CSCP4

VSD1CSCP4 is VSD CSC parameter 4 register (instant register).

Offset Address	Register Name	Total Reset Value
0x4098	VSD1CSCP4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				cscp22											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved.

[12:0]	RW	cscp22	5.8 data format. The value consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complementary code.

VSD1IFIRCOEF01

VSD1IFIRCOEF01 is a VSD IFIR filtering coefficients 0–1 register.

Offset Address	Register Name	Total Reset Value
0x4180	VSD1IFIRCOEF01	0x000D_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								coef1								reserved								coef0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.
[25:16]	RW	coef1	IFIR filtering coefficient 1.
[15:10]	-	reserved	Reserved.
[9:0]	RW	coef0	IFIR filtering coefficient 0.

VSD1IFIRCOEF23

VSD1IFIRCOEF23 is a VSD IFIR filtering coefficients 2–3 register.

Offset Address	Register Name	Total Reset Value
0x4184	VSD1IFIRCOEF23	0x0132_03C1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								coef3								reserved								coef2							
Reset	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	1

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.
[25:16]	RW	coef3	IFIR filtering coefficient 3.
[15:10]	-	reserved	Reserved.
[9:0]	RW	coef2	IFIR filtering coefficients 2.

VSD1IFIRCOEF45

VSD1IFIRCOEF45 is a VSD IFIR filtering coefficients 4–5 register.

Offset Address	Register Name	Total Reset Value
0x4188	VSD1IFIRCOEF45	0x003C_0132

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								coef5								reserved								coef4							
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.
[25:16]	RW	coef5	IFIR filtering coefficient 5.
[15:10]	-	reserved	Reserved.
[9:0]	RW	coef4	IFIR filtering coefficient 4.

VSD1IFIRCOEF67

VSD1IFIRCOEF67 is a VSD IFIR filtering coefficients 6–7 register.

Offset Address	Register Name	Total Reset Value
0x418C	VSD1IFIRCOEF67	0x0000_000D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								coef7								reserved								coef6							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.
[25:16]	RW	coef7	IFIR filtering coefficient 7.
[15:10]	-	reserved	Reserved.
[9:0]	RW	coef6	IFIR filtering coefficient 6.

VSD1P0RESO

VSD1P0RESO is a VSD1 region 0 resolution register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x4400 (m = 0–63)	VSD1P0RESO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								h												w											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	reserved	Reserved.
[23:12]	RW	h	Height (in line). The frame height is referenced. The value is the actual height minus 1. Note: The actual height must be an even number.
[11:0]	RW	w	Width (in pixel). The value is the actual width minus 1. Note: The actual width must be an even number.

VSD1P0LADDR

VSD1P0LADDR is a VSD1 region 0 address register.

Offset Address	Register Name	Total Reset Value
0x4404	VSD1P0LADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_addr	Start address of VSD1 region 0.

VSD1P0CADDR

VSD1P0CADDR is a VSD1 region 0 chrominance address register.

Offset Address	Register Name	Total Reset Value
0x4408	VSD1P0CADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_addr	Chrominance start address of VSD1 region 0.

VSD1P0STRIDE

VSD1P0STRIDE is a VSD1 region 0 stride register.

Offset Address	Register Name	Total Reset Value
0x440C	VSD1P0STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_cstride																surface_stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	surface_cstride	Stride of the chrominance buffer of VSD1 region 0 (valid in semi-planar format), 128-bit alignment.
[15:0]	RW	surface_stride	Stride of the buffer of VSD1 region 0 (valid in semi-planar format, luminance stride), 128-bit alignment.

VSD1P0VFPOS

VSD1P0VFPOS is a VSD1 region 0 video start position register. The start position is in the unit of pixel.

Offset Address	Register Name	Total Reset Value
0x4410	VSD1P0VFPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								video_yfpos												video_xfpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	reserved	Reserved.

[23:12]	RW	video_yfpos	Start coordinate of the video column. The frame height is referenced and the unit is line.
[11:0]	RW	video_xfpos	Start coordinate of the video row.

VSD1P0VLPOS

VSD1P0VLPOS is a VSD1 region 0 video end position register (non-instant register). The end position is in the unit of pixel.

Offset Address	Register Name	Total Reset Value
0x4414	VSD1P0VLPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								video_ylpos												video_xlpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	reserved	Reserved.
[23:12]	RW	video_ylpos	Start coordinate of the video column. The frame height is referenced and the unit is line.
[11:0]	RW	video_xlpos	Start coordinate of the video row.

VSD116REGIONEN

VSD116REGIONEN is a VSD1 region 0 enable register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x4C04	VSD116REGIONEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															p0_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RW	reserved	Reserved.
[0]	RW	p0_en	VSD1 region 0 enable. 0: disabled 1: enabled

G3CTRL

G3CTRL is the G3 control register (non-instant register). It is used to configure the layer information

Offset Address	Register Name	Total Reset Value
0x9600	G3CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_en	reserved			upd_mode	read_mode	reserved																bitext		ifmt							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	surface_en	Surface enable (non-instant register). 0: disabled 1: enabled
[30:28]	-	reserved	Reserved.
[27]	RW	upd_mode	Update mode. 0: update by frame 1: update by field
[26]	RW	read_mode	Data read mode. 0: The read mode is automatically selected based on the interface read mode. That is, the progressive read mode is selected in progressive display mode, and the interlaced read mode is selected in interlaced display mode. 1: The progressive read mode is selected forcibly.
[25:10]	RW	reserved	Reserved.
[9:8]	RW	bitext	Bit extend mode of the input bitmap. 0X: lower bits stuffed with 0s 10: lower bits stuffed with the MSB 11: lower bits stuffed with upper bits
[7:0]	RW	ifmt	Input data format. 0x49: ARGB1555 0x68: ARGB8888 Other values: reserved

G3UPD

G3UPD is the G3 channel update enable register.

Offset Address	Register Name	Total Reset Value
0x9604	G3UPD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															regup
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	regup	Surface register update. After the registers at this layer are configured, the registers are updated when the value 1 is written to this bit. After updates, this bit is cleared automatically by the hardware

G3ADDR

G3ADDR is the G3 address register. When the horizontal pixel offsets, the address is calculated according to the description of G3SFPOS.

Offset Address	Register Name	Total Reset Value
0x9608	G3ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_addr	Address of the surface frame buffer.

G3STRIDE

G3STRIDE is the G3 stride register.

Offset Address	Register Name	Total Reset Value
0x960C	G3STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																surface_stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	–	reserved	Reserved.
[15:0]	RW	surface_stride	Stride of the frame buffer.

G3CBMPARA

G3CBMPARA is the G3 overlay parameter register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x9610	G3CBMPARA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																key_mode	key_en	reserved	palpha_en	reserved			palpha_range	galpha								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15]	RW	key_mode	Colorkey mode. 0: The color is regarded as the colorkey when the following condition is met: Keymin ≤ Pixel ≤ Keymax 1: The color is regarded as the colorkey when either of the following conditions is met: Pixel ≤ Keymin or Pixel ≥ Keymax
[14]	RW	key_en	Colorkey enable. 0: disabled 1: enabled
[13]	-	reserved	Reserved.
[12]	RW	palpha_en	Pixel alpha enable. 0: disabled 1: enabled
[11:9]	RW	reserved	Reserved.

[8]	RW	palpha_range	Pixel alpha range. 0: 0–128 1: 0–255
[7:0]	RW	galpha	Overlay global alpha value. This value ranges from 0 to 255. The value 255 indicates opaque, and the value 0 indicates full transparent.

G3CKEYMAX

G3CKEYMAX is the G3 maximum colorkey register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x9614	G3CKEYMAX	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	va0		keyr_max		keyg_max		keyb_max	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	va0	Alpha0 value. When the data format is alphaRGB1555 and the alpha value is 0, the alpha0 value is used.
[23:16]	RW	keyr_max	Maximum value of colorkey R component.
[15:8]	RW	keyg_max	Maximum value of colorkey G component.
[7:0]	RW	keyb_max	Maximum value of colorkey B component.

G3CKEYMIN

G3CKEYMIN is the G3 minimum colorkey register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x9618	G3CKEYMIN	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	va1		keyr_min		keyg_min		keyb_min	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	va1	Alpha1 value. When the data format is alphaRGB1555 and the alpha value is 1, the alpha1 value is used.
[23:16]	RW	keyr_min	Minimum value of colorkey R component.
[15:8]	RW	keyg_min	Minimum value of colorkey G component.

Offset Address	Register Name	Total Reset Value
0x9618	G3CKEYMIN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	val								keyr_min								keyg_min								keyb_min							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	keyb_min	Minimum value of colorkey B component.

G3CMASK

G3CMASK is the G3 colorkey mask register (non-instant register). When the corresponding bit is 0, the colorkey is compared. In this case, this bit can be ignored.

Offset Address	Register Name	Total Reset Value
0x961C	G3CMASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								kmsk_r								kmsk_g								kmsk_b							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:16]	RW	kmsk_r	R component of colorkey mask.
[15:8]	RW	kmsk_g	G component of colorkey mask.
[7:0]	RW	kmsk_b	B component of colorkey mask.

G3IRESO

G3IRESO is the G3 input resolution register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x9620	G3IRESO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ih												iw											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.

[23:12]	RW	ih	Height (in line). The value is the actual height minus 1. Note: In interlaced output mode, the actual layer height must be an even number. There is no such limitation in progressive output mode.
[11:0]	RW	iw	Width (in pixel). The value is the actual width minus 1. Note: The actual layer width must be an even number.

G3ORESO

G3ORESO is the G3 output resolution register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x9624	G3ORESO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								oh												ow											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:12]	RW	oh	Height (in line). The value is the actual height minus 1. Note: In interlaced output mode, the actual layer height must be an even number. There is no such limitation in progressive output mode.
[11:0]	RW	ow	Width (in pixel). The value is the actual width minus 1. Note: The actual layer width must be an even number.

G3DFPOS

G3DFPOS is the G3 surface start position (in the display window) register (non-instant register). The start position is in the unit of pixel.

Offset Address	Register Name	Total Reset Value
0x962C	G3DFPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								disp_yfpos												disp_xfpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:12]	RW	disp_yfpos	Column start coordinate.

[11:0]	RW	disp_xfpos	Row start coordinate.

G3DLPOS

G3DLPOS is the G3 surface end position (in the display window) register (non-instant register). The end position is in the unit of pixel.

Offset Address	Register Name	Total Reset Value
0x9630	G3DLPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								disp_ylpos												disp_xlpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:12]	RW	disp_ylpos	Column end coordinate.
[11:0]	RW	disp_xlpos	Row end coordinate.

G3CSCIDC

G3CSCIDC is the G3 input DC component register for CSC (instant register).

Offset Address	Register Name	Total Reset Value
0x96A0	G3CSCIDC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				csc_mode	csc_en	cscidc2										cscidc1								cscidc0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28]	RW	csc_mode	CSC mode. 0: RGB to YUV 601 1: RGB to YUV 709
[27]	RW	csc_en	CSC enable. 0: disabled 1: enabled

[26:18]	RO	cscidc2	DC parameter of input component 2. The MSB is the signed bit. The value is expressed as the complementary code.
[17:9]	RO	cscidc1	DC parameter of input component 1. The MSB is the signed bit. The value is expressed as the complementary code.
[8:0]	RO	cscidc0	DC parameter of input component 0. The MSB is the signed bit. The value is expressed as the complementary code.

G3CSCODC

G3CSCODC is the G3 output DC component register for CSC (instant register).

Offset Address	Register Name	Total Reset Value
0x96A4	G3CSCODC	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		cscodc2		cscodc1		cscodc0	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	-	reserved	Reserved.
[26:18]	RO	cscodc2	DC parameter of output component 2. The MSB is the signed bit. The value is expressed as the complementary code.
[17:9]	RO	cscodc1	DC parameter of output component 1. The MSB is the signed bit. The value is expressed as the complementary code.
[8:0]	RO	cscodc0	DC parameter of output component 0. The MSB is the signed bit. The value is expressed as the complementary code.

G3CSCP0

G3CSCP0 is the G3 CSC parameter 0 register (instant register).

Offset Address	Register Name	Total Reset Value
0x96A8	G3CSCP0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp01												reserved				cscp00											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RO	cscp01	5.8 data format. The value consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complementary code.
[15:13]	-	reserved	Reserved.
[12:0]	RO	cscp00	5.8 data format. The value consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complementary code.

G3CSCP1

G3CSCP1 is the G3 CSC parameter 1 register (instant register).

Offset Address	Register Name	Total Reset Value
0x96AC	G3CSCP1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp10												reserved				cscp02											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RO	cscp10	5.8 data format. The value consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complementary code.
[15:13]	-	reserved	Reserved.
[12:0]	RO	cscp02	5.8 data format. The value consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complementary code.

G3CSCP2

G3CSCP2 is the G3 CSC parameter 2 register (instant register).

Offset Address	Register Name	Total Reset Value
0x96B0	G3CSCP2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp12												reserved				cscp11											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RO	cscp12	5.8 data format. The value consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complementary code.
[15:13]	-	reserved	Reserved.
[12:0]	RO	cscp11	5.8 data format. The value consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complementary code.

G3CSCP3

G3CSCP3 is the G3 CSC parameter 3 register (instant register).

Offset Address	Register Name	Total Reset Value
0x96B4	G3CSCP3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp21												reserved				cscp20											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved.
[28:16]	RO	cscp21	5.8 data format. The value consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complementary code.

[15:13]	-	reserved	Reserved.
[12:0]	RO	cscp20	5.8 data format. The value consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complementary code.

G3CSCP4

G3CSCP4 is the G3 CSC parameter 4 register (instant register).

Offset Address	Register Name	Total Reset Value
0x96B8	G3CSCP4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				cscp22											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved.
[12:0]	RO	cscp22	5.8 data format. The value consists of a 1-bit signed bit, a 4-bit integral part, and an 8-bit fractional part. The value is expressed as the complementary code.

CBMBKG4

CBMBKG4 is the SD1 overlay background color register.

Offset Address	Register Name	Total Reset Value
0x9E0C	CBMBKG4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								cbm_bkgy								cbm_bkgcb								cbm_bkgcr							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:16]	RW	cbm_bkgy	Overlay background color of mixer 4, Y component.
[15:8]	RW	cbm_bkgcb	Overlay background color of mixer 4, Cb component.
[7:0]	RW	cbm_bkgcr	Overlay background color of mixer 4, Cr component.

CBMMIX4

CBMMIX4 is the mixer 4 priority configuration register (non-instant register). The register configuration takes effect only when the VSYNC signal is valid.

Offset Address	Register Name	Total Reset Value
0x9E20	CBMMIX4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								mixer_prio1				mixer_prio0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved.
[7:4]	RW	mixer_prio1	Priority 1 of the overlay layer of mixer 4. 0x0: no overlay layer 0x5: VSD1 0xC: G3 Other values: reserved
[3:0]	RW	mixer_prio0	Priority 0 of the overlay layer of mixer 4. 0x0: no overlay layer 0x5: VSD1 0xC: G3 Other values: reserved

DSD1CTRL

DSD1CTRL is the DSD1 global control register.

CAUTION

You must configure this register before configuring DSDCTRL[intf_en]. Otherwise, the configuration does not take effect.

Offset Address	Register Name	Total Reset Value
0xAC00	DSD1CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	intf_en	reserved																				idv	ihs	ivs	iop	synm	intfb		intfdm			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	intf_en	Display interface enable (instant register). Data is output over the interface only when this bit is enabled. 0: disabled 1: enabled
[30:11]	-	reserved	Reserved.
[10]	RW	idv	Output phase reverse enable for the data valid signal (instant field). 0: disabled 1: enabled
[9]	RW	ihs	Output phase reverse enable for the horizontal sync pulse (instant field). 0: disabled 1: enabled
[8]	RW	ivs	Output phase reverse enable for the vertical sync pulse (instant field). 0: disabled 1: enabled
[7]	RW	iop	Progressive or interlaced display (instant field). 0: interlaced display 1: progressive display
[6]	RW	synm	Sync mode (instant field). 0: timing label mode (such as BT.656) 1: sync signal mode (such as LCD display)
[5:4]	RW	intfb	Bit width mode of the output interface (instant field). 00: single-component mode (each clock outputs one component) Other values: reserved
[3:0]	RW	intfdm	Interface data format (instant field). 0x0: YCbCr422 Other values: reserved

DSD1VSYNC

DSD1VSYNC is the DSD1 vertical timing register. In interlaced output mode, this register indicates the top vertical sync timing; in progressive output mode, this register indicates the frame vertical sync timing. The setting of this register takes effect immediately after configuration. That is, the timing of the VSYNC pin is affected immediately.

CAUTION

You must configure this register before configuring DSDCTRL[intf_en]. Otherwise, the configuration does not take effect.

Offset Address	Register Name	Total Reset Value
0xAC04	DSD1VSYNC	0x0011_511F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				vfb								vbb								vact											
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	0	1	0	0	0	1	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27:20]	RW	vfb	In interlaced output mode: TVFB In progressive output mode: VFB Unit: line
[19:12]	RW	vbb	In interlaced output mode: TVBB In progressive output mode: VBB + VPW Unit: line
[11:0]	RW	vact	In interlaced output mode: height of an active picture in the top field In progressive output format: height of an active picture in a frame. The register value is the actual value minus 1. Unit: line

DSD1HSYNC1

DSD1HSYNC1 is DSD1 horizontal timing register 1. In interlaced or progressive output mode, this register is the horizontal sync timing configuration register. The setting of this register takes effect immediately after configuration. That is, the timing of the HSYNC pin is affected immediately.

CAUTION

You must configure this register before configuring DSDCTRL[intf_en]. Otherwise, the configuration does not take effect.

Offset Address	Register Name	Total Reset Value
0xAC08	DSD1HSYNC1	0x0107_02CF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hbb																hact															
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1	0	0	0	0	0	0	1	0	1	1	0	0	1	1	1	1

Bits	Access	Name	Description
[31:16]	RW	hbb	HBB. Unit: pixel
[15:0]	RW	hact	Number of horizontal pixels in an active region.

DSD1HSYNC2

DSD1HSYNC2 is DSD1 horizontal timing register 2. In interlaced or progressive output mode, this register is the horizontal sync timing configuration register. The setting of this register takes effect immediately after configuration. That is, the timing of the HSYNC pin is affected immediately.

CAUTION

You must configure this register before configuring DSDCTRL[intf_en]. Otherwise, the configuration does not take effect.

Offset Address	Register Name	Total Reset Value
0xAC0C	DSD1HSYNC2	0x0000_0017

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hfb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.

[15:0]	RW	hfb	HFB. Unit: pixel

DSD1VPLUS

DSD1VPLUS is the DSD1 bottom vertical sync timing register in interlaced output mode.

CAUTION

You must configure this register before configuring DSDCTRL[intf_en]. Otherwise, the configuration does not take effect.

Offset Address	Register Name	Total Reset Value
0xAC10	DSD1VPLUS	0x0011_611F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				bvfb								bvbb								bvact											
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	1	0	0	0	0	1	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27:20]	RW	bvfb	In interlaced output mode: BVFB Unit: line
[19:12]	RW	bvbb	In interlaced output mode: BVBB + VPW Unit: line
[11:0]	RW	bvact	In interlaced output mode: height of an active picture in the bottom field. The register value is the actual value minus 1. Unit: line

DSD1PWR

DSD1PWR is the DSD1 sync signal pulse width register.

CAUTION

You must configure this register before configuring DSDCTRL[intf_en]. Otherwise, the configuration does not take effect.

Offset Address	Register Name	Total Reset Value
0xAC14	DSD1PWR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								vpw								hpw															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved.
[23:16]	RW	vpw	VPW minus 1. Unit: pixel
[15:0]	RW	hpw	HPW minus 1. Unit: pixel

DSD1VTTHD

DSD1VTTHD is the DSD1 vertical timing threshold register (instant register). It can be used to set two thresholds for generating two interrupts separately.

Offset Address	Register Name	Total Reset Value
0xAC1C	DSD1VTTHD	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																thd1_mode	reserved			vtmgthd1											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15]	RW	thd1_mode	Threshold 1 interrupt generation mode. 0: frame mode. The threshold count is in the unit of frame. 1: field mode. The threshold count is in the unit of field in interlaced display mode.

[14:13]	-	reserved	Reserved.
[12:0]	RW	vtmgthd1	Vertical timing threshold 1. When the vertical timing counter reaches this threshold, the VOINTSTA[dsdvtthd_int1] interrupt is triggered.

DSD1CLIPL

DSD1CLIPL is the DSD1 clip lower threshold register (instant register).

Offset Address	Register Name	Total Reset Value
0xAC40	DSD1CLIPL	0x4010_1010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clipen	dfir_en	clipcl2										clipcl1										clipcl0									
Reset	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31]	RW	clipen	Output clip enable (instant field). 0: disabled 1: enabled
[30]	RW	dfir_en	Horizontal chrominance down scaling enable. 0: disabled 1: enabled
[29:20]	RW	clipcl2	Lower threshold Y/R of component 2, unsigned integer.
[19:10]	RW	clipcl1	Lower threshold Cb/G of component 1, unsigned integer.
[9:0]	RW	clipcl0	Lower threshold Cr/B of component 0, unsigned integer.

DSD1CLIPH

DSD1CLIPH is the DSD1 clip upper threshold register (instant register). For example, the output data needs to be clipped in BT.656 output mode.

Offset Address	Register Name	Total Reset Value
0xAC44	DSD1CLIPH	0x00EB_F0F0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				clipch2												clipch1								clipch0							
Reset	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	1	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0

Bits	Access	Name	Description
[31:30]	-	reserved	Reserved.
[29:20]	RW	clipch2	Upper threshold Y/R of component 2, unsigned integer.
[19:10]	RW	clipch1	Upper threshold Cb/G of component 1, unsigned integer.
[9:0]	RW	clipch0	Upper threshold Cr/B of component 0, unsigned integer.

DSD1STATE

DSD1STATE is the DSD1 status register.

Offset Address	Register Name	Total Reset Value
0xACF0	DSD1STATE	0x0000_0110

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													bottom_field	vblank	vback_blank
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:3]	-	reserved	Reserved.
[2]	RW	bottom_field	DSD1 top/bottom field flag. 0: top field 1: bottom field
[1]	RW	vblank	DSD1 blanking region flag. 0: active region 1: blanking region

[0]	RW	vback_blank	DSD1 back blanking region flag. 0: non-back blanking region 1: back blanking region

DATE_COEFF1

DATE_COEFF1 is the DATE amplitude configuration register.

Offset Address	Register Name	Total Reset Value
0xC204	DATE_COEFF1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	c_gain			cvbs_limit_en	wss_seq	vps_seq	cgms_seq	cc_seq	c_limit_en	amp_outside										date_test_en	date_test_mode				dac_test							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RW	c_gain	Adjustment of the chrominance sync gain amplitude.
[28]	RW	cvbs_limit_en	CVBS amplitude limit enable. 0: disabled 1: enabled
[27]	RW	wss_seq	Sequence of transmitting the bits of the WSS data. 0: from upper bits to lower bits 1: from lower bits to upper bits
[26]	RW	vps_seq	Sequence of transmitting the bits of the VPS data. 0: from upper bits to lower bits 1: from lower bits to upper bits
[25]	RW	cgms_seq	Sequence of transmitting the bits of the CGMS data. 0: from upper bits to lower bits 1: from lower bits to upper bits
[24]	RW	cc_seq	Sequence of transmitting the bits of the closed caption data. 0: from upper bits to lower bits 1: from lower bits to upper bits

[23]	RW	c_limit_en	Chrominance amplitude limit enable. 0: disabled 1: enabled
[22:13]	RW	amp_outside	Pulse amplitude input of the external AGC.
[12]	RW	date_test_en	Test valid signal. 0: invalid 1: valid
[11:10]	RW	date_test_mode	Test mode signal.
[9:0]	RW	dac_test	DAC test value input.

DATE_COEFF7

DATE_COEFF7 is a DATE teletext configuration register.

Offset Address	Register Name	Total Reset Value
0xC21C	DATE_COEFF7	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tt22_enf1	tt21_enf1	tt20_enf1	tt19_enf1	tt18_enf1	tt17_enf1	tt16_enf1	tt15_enf1	tt14_enf1	tt13_enf1	tt12_enf1	tt11_enf1	tt10_enf1	tt09_enf1	tt08_enf1	tt07_enf1	tt22_enf2	tt21_enf2	tt20_enf2	tt19_enf2	tt18_enf2	tt17_enf2	tt16_enf2	tt15_enf2	tt14_enf2	tt13_enf2	tt12_enf2	tt11_enf2	tt10_enf2	tt09_enf2	tt08_enf2	tt07_enf2
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	tt22_enf1	Control of the teletext in line 22 in the odd field. 0: disabled 1: enabled
[30]	RW	tt21_enf1	Control of the teletext in line 21 in the odd field. 0: disabled 1: enabled
[29]	RW	tt20_enf1	Control of the teletext in line 20 in the odd field. 0: disabled 1: enabled
[28]	RW	tt19_enf1	Control of the teletext in line 19 in the odd field. 0: disabled 1: enabled

[27]	RW	tt18_enf1	Control of the teletext in line 18 in the odd field. 0: disabled 1: enabled
[26]	RW	tt17_enf1	Control of the teletext in line 17 in the odd field. 0: disabled 1: enabled
[25]	RW	tt16_enf1	Control of the teletext in line 16 in the odd field. 0: disabled 1: enabled
[24]	RW	tt15_enf1	Control of the teletext in line 15 in the odd field. 0: disabled 1: enabled
[23]	RW	tt14_enf1	Control of the teletext in line 14 in the odd field. 0: disabled 1: enabled
[22]	RW	tt13_enf1	Control of the teletext in line 13 in the odd field. 0: disabled 1: enabled
[21]	RW	tt12_enf1	Control of the teletext in line 12 in the odd field.0: disabled 1: enabled
[20]	RW	tt11_enf1	Control of the teletext in line 11 in the odd field.0: disabled 1: enabled
[19]	RW	tt10_enf1	Control of the teletext in line 10 in the odd field. 0: disabled 1: enabled
[18]	RW	tt09_enf1	Control of the teletext in line 9 in the odd field. 0: disabled 1: enabled
[17]	RW	tt08_enf1	Control of the teletext in line 8 in the odd field. 0: disabled 1: enabled
[16]	RW	tt07_enf1	Control of the teletext in line 7 in the odd field. 0: disabled 1: enabled
[15]	RW	tt22_enf2	Control of teletext in line 22 in the even field. 0: disabled 1: enabled

[14]	RW	tt21_enf2	Control of teletext in line 21 in the even field. 0: disabled 1: enabled
[13]	RW	tt20_enf2	Control of teletext in line 20 in the even field. 0: disabled 1: enabled
[12]	RW	tt19_enf2	Control of teletext in line 19 in the even field. 0: disabled 1: enabled
[11]	RW	tt18_enf2	Control of teletext in line 18 in the even field. 0: disabled 1: enabled
[10]	RW	tt17_enf2	Control of teletext in line 17 in the even field. 0: disabled 1: enabled
[9]	RW	tt16_enf2	Control of teletext in line 16 in the even field. 0: disabled 1: enabled
[8]	RW	tt15_enf2	Control of teletext in line 15 in the even field. 0: disabled 1: enabled
[7]	RW	tt14_enf2	Control of teletext in line 14 in the even field. 0: disabled 1: enabled
[6]	RW	tt13_enf2	Control of teletext in line 13 in the even field. 0: disabled 1: enabled
[5]	RW	tt12_enf2	Control of teletext in line 12 in the even field. 0: disabled 1: enabled
[4]	RW	tt11_enf2	Control of teletext in line 11 in the even field. 0: disabled 1: enabled
[3]	RW	tt10_enf2	Control of teletext in line 10 in the even field. 0: disabled 1: enabled

[2]	RW	tt09_enf2	Control of teletext in line 9 in the even field. 0: disabled 1: enabled
[1]	RW	tt08_enf2	Control of teletext in line 8 in the even field. 0: disabled 1: enabled
[0]	RW	tt07_enf2	Control of teletext in line 7 in the even field. 0: disabled 1: enabled

DATE_COEFF8

DATE_COEFF8 is a DATE teletext configuration register.

Offset Address	Register Name	Total Reset Value
0xC220	DATE_COEFF8	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tt_staddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	tt_staddr	Start address of the teletext data.

DATE_COEFF9

DATE_COEFF9 is a DATE teletext configuration register.

Offset Address	Register Name	Total Reset Value
0xC224	DATE_COEFF9	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tt_edaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	tt_edaddr	End address of the teletext data.

DATE_COEFF10

DATE_COEFF10 is a DATE teletext configuration register.

CAUTION

The teletext function is supported in both 625-line mode and 525-line mode. The tt_mode bit is set to 01 in 625-line mode or 10 in 525-line mode.

Offset Address	Register Name	Total Reset Value
0xC228	DATE_COEFF10	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tt_ready	reserved																		nabts_100ire	full_page	tt_highest	tt_mode		tt_pktoff							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	tt_ready	When software sets related parameters through the bus, this bit is set to 1 and the teletext module starts to work. When the teletext module completes data transfer, this bit is set to 0. The bit status can be queried through software for the next configuration.
[30:13]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[12]	RW	nabts_100ire	NABTS-NTSC data height. 0: 70 IRE 1: 100 IRE
[11]	RW	full_page	Teletext data transmission mode. 0: normal mode. The teletext data is transmitted from the blanking line. 1: full page mode. The teletext data can also be transmitted from the active video region.
[10]	RW	tt_highest	Teletext priority control. 0: The teletext data has the highest priority. 1: The teletext data has the lowest priority.
[9:8]	RW	tt_mode	Teletext mode. This field is set to 01 in 625-line mode, indicating WST-PAL. This field is set to 10 in 525-line mode, indicating NABTS-NTSC.
[7:0]	RW	tt_pktoff	Offset address of the teletext packet.

DATE_COEFF11

DATE_COEFF11 is a DATE closed caption configuration register.

Offset Address	Register Name	Total Reset Value
0xC22C	DATE_COEFF11	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										cc_enf1	cc_enf2	date_clf1												date_clf2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RW	reserved	Reserved.
[21]	RW	cc_enf1	Closed caption odd field enable. 0: disabled 1: enabled
[20]	RW	cc_enf2	Closed caption even field enable. 0: disabled 1: enabled
[19:10]	RW	date_clf1	Configuration line of the closed caption odd field.
[9:0]	RW	date_clf2	Configuration line of the closed caption even field.

DATE_COEFF12

DATE_COEFF12 is a DATE closed caption configuration register.

Offset Address	Register Name	Total Reset Value
0xC230	DATE_COEFF12	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cc_f1data																cc_f2data															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	cc_f1data	Data of the closed caption odd field.
[15:0]	RW	cc_f2data	Data of the closed caption even field.

DATE_COEFF13

DATE_COEFF13 is a DATE CGMS configuration register.

Offset Address	Register Name	Total Reset Value
0xC234	DATE_COEFF13	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										cg_enf1	cg_enf2	cg_f1data																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[21]	RW	cg_enf1	CGMS odd field enable. 0: disabled 1: enabled
[20]	RW	cg_enf2	CGMS even field enable. 0: disabled 1: enabled
[19:0]	RW	cg_f1data	Data of the CGMS odd field.

DATE_COEFF14

DATE_COEFF14 is a DATE CGMS configuration register.

Offset Address	Register Name	Total Reset Value
0xC238	DATE_COEFF14	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												cg_f2data																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[19:0]	RW	cg_f2data	Data of the CGMS even field.

DATE_COEFF15

DATE_COEFF15 is a DATE WSS configuration register.

CAUTION

The WSS is available only in 625-line mode and is fixed at line 23.

Offset Address	Register Name	Total Reset Value
0xC23C	DATE_COEFF15	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																	wss_en	wss_data													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[14]	RW	wss_en	WSS enable. 0: disabled 1: enabled
[13:0]	RW	wss_data	WSS data.

DATE_COEFF16

DATE_COEFF16 is a DATE VPS configuration register.

Offset Address	Register Name	Total Reset Value
0xC240	DATE_COEFF16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved							vps_en	vps_data																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.

[24]	RW	vps_en	VPS enable. 0: disabled 1: enabled
[23:0]	RW	vps_data	VPS data from bit 23 to bit 0. Bit 0 is the LSB.

DATE_COEFF17

DATE_COEFF17 is a DATE VPS configuration register.

Offset Address	Register Name	Total Reset Value
0xC244	DATE_COEFF17	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vps_data																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	vps_data	VPS data from bit 55 to bit 24. Bit 0 is the LSB.

DATE_COEFF18

DATE_COEFF18 is a DATE VPS configuration register.

Offset Address	Register Name	Total Reset Value
0xC248	DATE_COEFF18	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vps_data																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	vps_data	VPS data from bit 87 to bit 56. Bit 0 is the LSB.

DATE_COEFF19

DATE_COEFF19 is a DATE VPS configuration register.

CAUTION

The VPS is available only in 625-line mode and is fixed at line 16.

Offset Address	Register Name	Total Reset Value
0xC24C	DATE_COEFF19	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vps_data															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[15:0]	RW	vps_data	VPS data from bit 103 to bit 88. Bit 0 is the LSB.

DATE_COEFF20

DATE_COEFF20 is a DATE teletext configuration register.

Offset Address	Register Name	Total Reset Value
0xC250	DATE_COEFF20	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												tt06_enf1		tt06_enf2	tt05_enf2
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[2]	RW	tt06_enf1	Control of teletext in line 6 in the odd field. 0: disabled 1: enabled
[1]	RW	tt06_enf2	Control of teletext in line 6 in the even field. 0: disabled 1: enabled
[0]	RW	tt05_enf2	Control of teletext in line 5 in the even field. 0: disabled 1: enabled

DATE_COEFF22

DATE_COEFF22 is the DATE DTO initial phase configuration register.

Offset Address	Register Name	Total Reset Value
0xC258	DATE_COEFF22	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								video_phase_delta							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[10:0]	RW	video_phase_delta	DTO initial phase.

DATE_ISRMASK

DATE_ISRMASK is the DATE interrupt mask register.

Offset Address	Register Name	Total Reset Value
0xC280	DATE_ISRMASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															tt_mask
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[0]	RW	tt_mask	Teletext interrupt mask. 0: enabled 1: masked

DATE_ISRSTATE

DATE_ISRSTATE is the DATE interrupt status register.

Offset Address	Register Name	Total Reset Value
0xC284	DATE_ISRSTATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															tt_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[0]	W1C	tt_status	Teletext interrupt flag. After the DATE module reads all the teletext data, the bit is set to 1. Writing 1 to this bit clears this bit.

DATE_ISR

DATE_ISR is the DATE interrupt register.

Offset Address	Register Name	Total Reset Value
0xC288	DATE_ISR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															tt_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[0]	RW	tt_int	Teletext interrupt. It is the interrupt status after tt_status is masked by tt_mask. 0: No interrupt is generated. 1: An interrupt is generated.

DATE_VERSION

DATE_VERSION is the DATE version register.

Offset Address	Register Name	Total Reset Value
0xC290	DATE_VERSION	0x0000_0024

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0

Bits	Access	Name	Description
[31:0]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.

DATE1_COEFF0

DATE1_COEFF0 is the DATE1 norm parameter configuration register.

Offset Address	Register Name	Total Reset Value
0xC400	DATE1_COEFF0	0x5284_14FC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clpf_sel		dis_ire	reserved			scanline	rgb_en	vbi_lpf_en	fm_sel	style_sel		sync_mode_sel		sync_mode_scart	length_sel	agc_amp_sel	luma_dl		reserved	oversam_en		lunt_en	oversam2_en	chlp_en	sylp_en	chgain_en	tt_seq				
Reset	0	1	0	1	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0	1	0	1	0	0	1	1	1	1	1	1	0	0

Bits	Access	Name	Description
[31:30]	RW	clpf_sel	Bandwidth select of the chrominance low-pass filter. 00: 1.1 MHz (NTSC) 01: 1.3 MHz (PAL) 10: 1.6 MHz (for test) 11: reserved
[29]	RW	dis_ire	For the (M) NTSC and (M, N) PAL norms, the black level is 7.5 IRE higher than the blanking level; for other norms, the black level is equal to the blanking level. This bit controls whether the black level is 7.5 IRE higher than the blanking level. 0: The black level is 7.5 IRE higher than the blanking level. 1: The black level is equal to the blanking level.

[28:26]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[25]	RW	scanline	Number of scanned lines in each frame based on norms. For the (M) NTSC, NTSC-J, and (M) PAL norm, each line contains 525 lines; for the (B, D, J, H, I) PAL, (N) PAL, and (Nc) PAL norms, each frame contains 625 lines. 0: 525 lines in a frame 1: 625 lines in a frame
[24]	RW	rgb_en	When intf_sel is set to 100, this bit determines whether the component signal is RGB or YPbPr. 0: YPbPr 1: RGB
[23]	RW	vbi_lpf_en	VBI data low-pass filtering enable. 0: disabled 1: enabled
[22]	RW	fm_sel	FMSECAM frequency modulation select. 0: sin used for SECAM frequency modulation 1: cos used for SECAM frequency modulation
[21:18]	RW	style_sel	CVBS/S-Video output signal norm when this bit works with the scanline bit. When the scanline bit is 0 (525 scanned lines in a frame), the definition of the style_sel bit is as follows: 0x1: (M) NTSC 0x2: NTSC-J 0x4: (M) PAL Other values: reserved When the scanline bit is 1 (625 scanned lines in a frame), the definition of the style_sel bit is as follows: 0x1: (B, D, G, H, I) PAL 0x2: (N) PAL 0x4: (Nc) PAL 0x8: SECAM Other values: reserved

[17:16]	RW	sync_mode_sel	bit[17]: specifies whether there are sync signals in three channels during component output. This bit takes effect only when the sync_mode_scart bit is set to 0. bit[17] is valid only when the intf_sel is set to 100 (component output enabled). The definition of bit[17] is as follows: 0: Only one channel contains sync signals using component output. 1: Three channels contain sync signals during component output. When bit[17] is set to 0, the sync channel must be the Y channel for YPbPr output and G channel for RGB output. bit[16]: specifies whether there are blanking radixes during RGB output. bit[16] is valid only when the intf_sel is set to 100 and the rgb_en bit is set to 1. The definition of bit[16] is as follows: 0: There are no blanking radixes during RGB output. 1: There are blanking radixes during RGB output.
[15]	RW	sync_mode_scart	Overlay sync control of the components of three channels. 0: Component sync output is configured based on sync_mode_sel[1]. 1: The components of the three channels are not overlaid and synchronized. In this case, sync_mode_sel bit[1] must be set to 0.
[14]	RW	length_sel	Active width of each video line (in pixel). 0: output according to the active line width in BT.601 mode 1: output according to the active line width in BT.470 mode. When this bit is set to 0, the active width of the line is 720 pixels. When this bit is set to 1, the active width of the line is 704 pixels for the 625-line norm or 712 pixels for the 525-line norm. Currently, the BT.601 mode and BT.470 mode cannot be changed dynamically. You can change the mode only after reset. The BT.601 mode is recommended and this mode is the default value after power-on reset.
[13]	RW	agc_amp_sel	AGC pulse select. 0: The AGC pulse is generated based on the on-chip default value (recommended). 1: The AGC pulse is generated based on DATE_COEFF1[amp_outside].

[12:9]	RW	luma_dl	Forward or backward offset of the chrominance signal relative to the luminance signal, in the unit of half a pixel width. bit[12]: offset direction of the chrominance signal relative to the luminance signal. 0: backward offset 1: forward offset bit[11:9]: absolute offset of the chrominance signal relative to the luminance signal. The value is in binary format and ranges from 0 to 7. 000: The chrominance signal is aligned with the luminance signal. No adjustment is required. 001–111: The chrominance signal offsets from the luminance signal forward or backward by one to seven units.
[8]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[7:6]	RW	oversam_en	Level-1 oversampling enable. Both the luminance oversampling and chrominance oversampling are controlled. bit[7]: luminance oversampling enable. 0: disabled 1: enabled bit[6]: chrominance oversampling enable. 0: disabled 1: enabled
[5]	RW	lunt_en	Luminance notch enable. 0: disabled 1: enabled
[4]	RW	oversam2_en	Level-2 oversampling enable. Both the luminance channel and chrominance channel are controlled. 0: disabled 1: enabled
[3]	RW	chlp_en	Chrominance low-pass filtering enable. 0: disabled 1: enabled
[2]	RW	sylp_en	Sync low-pass filtering enable. 0: disabled 1: enabled
[1]	RW	chgain_en	Chrominance gain enable. 0: disabled 1: enabled

[0]	RW	tt_seq	Sequence of transmitting the bits of the teletext data. 0: from upper bits to lower bits 1: from lower bits to upper bits

DATE1_COEFF1

DATE1_COEFF1 is the DATE1 amplitude configuration register.

Offset Address	Register Name	Total Reset Value
0xC404	DATE1_COEFF1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	c_gain			cvbs_limit_en	wss_seq	vps_seq	cgms_seq	cc_seq	c_limit_en	amp_outside										date_test_en	date_test_mode				dac_test							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RW	c_gain	Adjustment of the chrominance sync gain amplitude.
[28]	RW	cvbs_limit_en	CVBS amplitude limit enable. 0: disabled 1: enabled
[27]	RW	wss_seq	Sequence of transmitting the bits of the WSS data. 0: from upper bits to lower bits 1: from lower bits to upper bits
[26]	RW	vps_seq	Sequence of transmitting the bits of the VPS data. 0: from upper bits to lower bits 1: from lower bits to upper bits
[25]	RW	cgms_seq	Sequence of transmitting the bits of the CGMS data. 0: from upper bits to lower bits 1: from lower bits to upper bits
[24]	RW	cc_seq	Sequence of transmitting the bits of the closed caption data. 0: from upper bits to lower bits 1: from lower bits to upper bits

[23]	RW	c_limit_en	Chrominance amplitude limit enable. 0: disabled 1: enabled
[22:13]	RW	amp_outside	Pulse amplitude input of the external AGC.
[12]	RW	date_test_en	Test valid signal. 0: invalid 1: valid
[11:10]	RW	date_test_mode	Test mode signal.
[9:0]	RW	dac_test	DAC test value input.

DATE1_COEFF7

DATE1_COEFF7 is a DATE1 teletext configuration register.

Offset Address	Register Name	Total Reset Value
0xC41C	DATE1_COEFF7	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tt22_enf1	tt21_enf1	tt20_enf1	tt19_enf1	tt18_enf1	tt17_enf1	tt16_enf1	tt15_enf1	tt14_enf1	tt13_enf1	tt12_enf1	tt11_enf1	tt10_enf1	tt09_enf1	tt08_enf1	tt07_enf1	tt22_enf2	tt21_enf2	tt20_enf2	tt19_enf2	tt18_enf2	tt17_enf2	tt16_enf2	tt15_enf2	tt14_enf2	tt13_enf2	tt12_enf2	tt11_enf2	tt10_enf2	tt09_enf2	tt08_enf2	tt07_enf2
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	tt22_enf1	Control of teletext in line 22 in the odd field. 0: disabled 1: enabled
[30]	RW	tt21_enf1	Control of teletext in line 21 in the odd field. 0: disabled 1: enabled
[29]	RW	tt20_enf1	Control of teletext in line 20 in the odd field. 0: disabled 1: enabled
[28]	RW	tt19_enf1	Control of teletext in line 19 in the odd field. 0: disabled 1: enabled

[27]	RW	tt18_enf1	Control of teletext in line 18 in the odd field. 0: disabled 1: enabled
[26]	RW	tt17_enf1	Control of teletext in line 17 in the odd field. 0: disabled 1: enabled
[25]	RW	tt16_enf1	Control of teletext in line 16 in the odd field. 0: disabled 1: enabled
[24]	RW	tt15_enf1	Control of teletext in line 15 in the odd field. 0: disabled 1: enabled
[23]	RW	tt14_enf1	Control of teletext in line 14 in the odd field. 0: disabled 1: enabled
[22]	RW	tt13_enf1	Control of teletext in line 13 in the odd field. 0: disabled 1: enabled
[21]	RW	tt12_enf1	Control of teletext in line 12 in the odd field. 0: disabled 1: enabled
[20]	RW	tt11_enf1	Control of teletext in line 11 in the odd field. 0: disabled 1: enabled
[19]	RW	tt10_enf1	Control of teletext in line 10 in the odd field. 0: disabled 1: enabled
[18]	RW	tt09_enf1	Control of teletext in line 9 in the odd field. 0: disabled 1: enabled
[17]	RW	tt08_enf1	Control of teletext in line 8 in the odd field. 0: disabled 1: enabled
[16]	RW	tt07_enf1	Control of teletext in line 7 in the odd field. 0: disabled 1: enabled

[15]	RW	tt22_enf2	Control of teletext in line 22 in the even field. 0: disabled 1: enabled
[14]	RW	tt21_enf2	Control of teletext in line 21 in the even field. 0: disabled 1: enabled
[13]	RW	tt20_enf2	Control of teletext in line 20 in the even field. 0: disabled 1: enabled
[12]	RW	tt19_enf2	Control of teletext in line 19 in the even field. 0: disabled 1: enabled
[11]	RW	tt18_enf2	Control of teletext in line 18 in the even field. 0: disabled 1: enabled
[10]	RW	tt17_enf2	Control of teletext in line 17 in the even field. 0: disabled 1: enabled
[9]	RW	tt16_enf2	Control of teletext in line 16 in the even field. 0: disabled 1: enabled
[8]	RW	tt15_enf2	Control of teletext in line 15 in the even field. 0: disabled 1: enabled
[7]	RW	tt14_enf2	Control of teletext in line 14 in the even field. 0: disabled 1: enabled
[6]	RW	tt13_enf2	Control of teletext in line 13 in the even field. 0: disabled 1: enabled
[5]	RW	tt12_enf2	Control of teletext in line 12 in the even field. 0: disabled 1: enabled
[4]	RW	tt11_enf2	Control of teletext in line 11 in the even field. 0: disabled 1: enabled

[3]	RW	tt10_enf2	Control of teletext in line 10 in the even field. 0: disabled 1: enabled
[2]	RW	tt09_enf2	Control of teletext in line 9 in the even field. 0: disabled 1: enabled
[1]	RW	tt08_enf2	Control of teletext in line 8 in the even field. 0: disabled 1: enabled
[0]	RW	tt07_enf2	Control of teletext in line 7 in the even field. 0: disabled 1: enabled

DATE1_COEFF8

DATE1_COEFF8 is a DATE1 teletext configuration register.

Offset Address	Register Name	Total Reset Value
0xC420	DATE1_COEFF8	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tt_staddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	tt_staddr	Start address of the teletext data.

DATE1_COEFF9

DATE1_COEFF9 is a DATE1 teletext configuration register.

Offset Address	Register Name	Total Reset Value
0xC424	DATE1_COEFF9	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tt_edaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	tt_edaddr	End address of the teletext data.

DATE1_COEFF10

DATE1_COEFF10 is a DATE1 teletext configuration register.

CAUTION

The teletext function is supported in both 625-line mode and 525-line mode. The tt_mode bit is set to 01 in 625-line mode or 10 in 525-line mode.

Offset Address	Register Name	Total Reset Value
0xC428	DATE1_COEFF10	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tt_ready	reserved																		nabts_100ire	full_page	tt_highest	tt_mode		tt_pktoff							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	tt_ready	When software sets related parameters through the bus, this bit is set to 1 and the teletext module starts to work. When the teletext module completes data transfer, this bit is set to 0. The bit status can be queried through software for the next configuration.
[30:13]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[12]	RW	nabts_100ire	NABTS-NTSC data height. 0: 70 IRE 1: 100 IRE
[11]	RW	full_page	Teletext data transmission mode. 0: normal mode. The teletext data is transmitted from the blanking line. 1: full page mode. The teletext data can also be transmitted from the active video region.
[10]	RW	tt_highest	Teletext priority control. 0: The teletext data has the highest priority. 1: The teletext data has the lowest priority.

[9:8]	RW	tt_mode	Teletext mode. This field is set to 01 in 625-line mode, indicating WST-PAL. This field is set to 10 in 525-line mode, indicating NABTS-NTSC.
[7:0]	RW	tt_pktoff	Offset address of the teletext packet.

DATE1_COEFF11

DATE1_COEFF11 is a DATE1 closed caption configuration register.

Offset Address	Register Name	Total Reset Value
0xC42C	DATE1_COEFF11	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										cc_enf1	cc_enf2	date_clf1										date_clf2									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RW	reserved	Reserved.
[21]	RW	cc_enf1	Closed caption odd field enable. 0: disabled 1: enabled
[20]	RW	cc_enf2	Closed caption even field enable. 0: disabled 1: enabled
[19:10]	RW	date_clf1	Configuration line of the closed caption odd field.
[9:0]	RW	date_clf2	Configuration line of the closed caption even field.

DATE1_COEFF12

DATE1_COEFF12 is a DATE1 closed caption configuration register.

Offset Address	Register Name	Total Reset Value
0xC430	DATE1_COEFF12	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cc_f1data																cc_f2data															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	cc_f1data	Data of the closed caption odd field.
[15:0]	RW	cc_f2data	Data of the closed caption even field.

DATE1_COEFF13

DATE1_COEFF13 is a DATE1 CGMS configuration register.

Offset Address	Register Name	Total Reset Value
0xC434	DATE1_COEFF13	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										cg_enf1	cg_enf2	cg_f1data																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[21]	RW	cg_enf1	CGMS odd field enable. 0: disabled 1: enabled
[20]	RW	cg_enf2	CGMS even field enable. 0: disabled 1: enabled
[19:0]	RW	cg_f1data	Data of the CGMS odd field.

DATE1_COEFF14

DATE1_COEFF14 is a DATE1 CGMS configuration register.

Offset Address	Register Name	Total Reset Value
0xC438	DATE1_COEFF14	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												cg_f2data																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[19:0]	RW	cg_f2data	Data of the CGMS even field.

DATE1_COEFF15

DATE1_COEFF15 is a DATE1 WSS configuration register.

CAUTION

The WSS is available only in 625-line mode and is fixed at line 23.

Offset Address	Register Name	Total Reset Value
0xC43C	DATE1_COEFF15	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																	wss_en	wss_data													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[14]	RW	wss_en	WSS enable. 0: disabled 1: enabled
[13:0]	RW	wss_data	WSS data.

DATE1_COEFF16

DATE1_COEFF16 is a DATE1 VPS configuration register.

Offset Address	Register Name	Total Reset Value
0xC440	DATE1_COEFF16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								vps_en	vps_data																						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[24]	RW	vps_en	VPS enable. 0: disabled 1: enabled
[23:0]	RW	vps_data	VPS data from bit 23 to bit 0. Bit 0 is the LSB.

DATE1_COEFF17

DATE1_COEFF17 is a DATE1 VPS configuration register.

Offset Address	Register Name	Total Reset Value
0xC444	DATE1_COEFF17	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vps_data																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	vps_data	VPS data from bit 55 to bit 24. Bit 0 is the LSB.

DATE1_COEFF18

DATE1_COEFF18 is a DATE1 VPS configuration register.

Offset Address	Register Name	Total Reset Value
0xC448	DATE1_COEFF18	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vps_data																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	vps_data	VPS data from bit 87 to bit 56. Bit 0 is the LSB.

DATE1_COEFF19

DATE1_COEFF19 is a DATE1 VPS configuration register.

CAUTION

The VPS is available only in 625-line mode and is fixed at line 16.

Offset Address	Register Name	Total Reset Value
0xC44C	DATE1_COEFF19	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vps_data															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[15:0]	RW	vps_data	VPS data from bit 103 to bit 88. Bit 0 is the LSB.

DATE1_COEFF20

DATE1_COEFF20 is a DATE1 teletext configuration register.

Offset Address	Register Name	Total Reset Value
0xC450	DATE1_COEFF20	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													tt06_enf1	tt06_enf2	tt05_enf2
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[2]	RW	tt06_enf1	Control of teletext in line 6 in the odd field. 0: disabled 1: enabled
[1]	RW	tt06_enf2	Control of teletext in line 6 in the even field. 0: disabled 1: enabled
[0]	RW	tt05_enf2	Control of teletext in line 5 in the even field. 0: disabled 1: enabled

DATE1_COEFF21

DATE1_COEFF21 is the DATE1 output matrix control register.

Offset Address	Register Name	Total Reset Value
0xC454	DATE1_COEFF21	0x0065_1432

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									dac5_in_sel			reserved	dac4_in_sel			reserved	dac3_in_sel			reserved	dac2_in_sel			reserved	dac1_in_sel			reserved	dac0_in_sel		
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1	0	0	0	1	0	1	0	0	0	0	1	1	0	0	1	0

Bits	Access	Name	Description
[31:23]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.

[22:20]	RW	dac5_in_sel	DAC5 output mode select. 000: 0 001: CVBS 010: G/Y 011: B/Pb 100: R/Pr 101: svideo_y 110: svideo_c 111: 0
[19]	-	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[18:16]	RW	dac4_in_sel	DAC4 output mode select. 000: 0 001: CVBS 010: G/Y 011: B/Pb 100: R/Pr 101: svideo_y 110: svideo_c 111: 0
[15]	-	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[14:12]	RW	dac3_in_sel	DAC3 output mode select. 000: 0 001: CVBS 010: G/Y 011: B/Pb 100: R/Pr 101: svideo_y 110: svideo_c 111: 0
[11]	-	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.

[10:8]	RW	dac2_in_sel	DAC2 output mode select. 000: 0 001: CVBS 010: G/Y 011: B/Pb 100: R/Pr 101: svideo_y 110: svideo_c 111: 0
[7]	-	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[6:4]	RW	dac1_in_sel	DAC1 output mode select. 000: 0 001: CVBS 010: G/Y 011: B/Pb 100: R/Pr 101: svideo_y 110: svideo_c 111: 0
[3]	-	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[2:0]	RW	dac0_in_sel	DAC0 output mode select. 000: 0 001: CVBS 010: G/Y 011: B/Pb 100: R/Pr 101: svideo_y 110: svideo_c 111: 0

DATE1_COEFF22

DATE1_COEFF22 is the DATE1 DTO initial phase configuration register.

Offset Address	Register Name	Total Reset Value
0xC458	DATE1_COEFF22	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					video_phase_delta										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[10:0]	RW	video_phase_delta	DTO initial phase.

DATE1_COEFF23

DATE1_COEFF23 is the DATE1 video output delay configuration register.

Offset Address	Register Name	Total Reset Value
0xC45C	DATE1_COEFF23	0x0065_4321

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								dac5_out_dly				reserved	dac4_out_dly			reserved	dac3_out_dly			reserved	dac2_out_dly			reserved	dac1_out_dly			reserved	dac0_out_dly		
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1	0	1	0	0	0	0	1	1	0	0	1	0	0	0	0	1

Bits	Access	Name	Description
[31:23]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[22:20]	RW	dac5_out_dly	DAC5 output delay cycle. The value is in the unit of a 54 MHz clock cycle and the value n indicates n delay cycles.
[19]	-	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[18:16]	RW	dac4_out_dly	DAC4 output delay cycle. The value is in the unit of a 54 MHz clock cycle and the value n indicates n delay cycles.
[15]	-	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.

[14:12]	RW	dac3_out_dly	DAC3 output delay cycle. The value is in the unit of a 54 MHz clock cycle and the value n indicates n delay cycles.
[11]	-	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[10:8]	RW	dac2_out_dly	DAC2 output delay cycle. The value is in the unit of a 54 MHz clock cycle and the value n indicates n delay cycles.
[7]	-	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[6:4]	RW	dac1_out_dly	DAC1 output delay cycle. The value is in the unit of a 54 MHz clock cycle and the value n indicates n delay cycles.
[3]	-	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[2:0]	RW	dac0_out_dly	DAC0 output delay cycle. The value is in the unit of a 54 MHz clock cycle and the value n indicates n delay cycles.

DATE1_ISRMASK

DATE1_ISRMASK is the DATE1 interrupt mask register.

Offset Address	Register Name	Total Reset Value
0xC480	DATE1_ISRMASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															tt_mask
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[0]	RW	tt_mask	Teletext interrupt mask. 0: enabled 1: masked

DATE1_ISRSTATE

DATE1_ISRSTATE is the DATE1 interrupt status register.

Offset Address	Register Name	Total Reset Value
0xC484	DATE1_ISRSTATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															tt_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[0]	W1C	tt_status	Teletext interrupt flag. After the DATE module reads all the teletext data, the bit is set to 1. Writing 1 to this bit clears this bit.

DATE1_ISR

DATE1_ISR is the DATE1 interrupt register.

Offset Address	Register Name	Total Reset Value
0xC488	DATE1_ISR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															tt_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.
[0]	RW	tt_int	Teletext interrupt. It is the interrupt status after tt_status is masked by tt_mask. 0: No interrupt is generated. 1: An interrupt is generated.

DATE1_VERSION

DATE1_VERSION is the DATE1 version register.

Offset Address	Register Name	Total Reset Value
0xC490	DATE1_VERSION	0x0000_0024

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0

Bits	Access	Name	Description
[31:0]	RW	reserved	Reserved. Writing to this field has no effect and reading this field returns 0.

DATE_DACDET1

DATE_DACDET1 is VDAC detection register 1.

Offset Address	Register Name	Total Reset Value
0xC4AC	DATE_DACDET1	0x000D_0303

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								det_line								reserved								vdac_det_high							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:26]	RW	reserved	Reserved.
[25:16]	RW	det_line	Line where the detected level is located. The line must be in the vertical blanking region but not in the pre- and post-equalization region and field sync field. This field indicates the number of line after the field sync region where the detected level is located.
[15:10]	RW	reserved	Reserved.
[9:0]	RW	vdac_det_high	Detected level.

DATE_DACDET2

DATE_DACDET2 is VDAC detection register 2.

Offset Address	Register Name	Total Reset Value
0xC4B0	DATE_DACDET2	0x0030_0118

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vdac_det_en	reserved							det_pixel_wid								reserved								det_pixel_sta							
Reset	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0

Bits	Access	Name	Description
[31]	RW	vdac_det_en	VDAC automatic detection enable. 0: disabled 1: enabled
[30:27]	RW	reserved	Reserved.
[26:16]	RW	det_pixel_wid	Number of clock cycles during which the detected level lasts. The clock is 27 MHz.
[15:11]	RW	reserved	Reserved.
[10:0]	RW	det_pixel_sta	Pixel start position in a line. It must be in the horizontal blanking region but not in the chrominance sub-carrier region. This field indicates the number of pixel after the line sync region.

VOCTRL

VOCTRL is a VO control register.

Offset Address	Register Name	Total Reset Value
0xCE00	VOCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vo_ck_gt_en	reserved									bus_dbg_en		outstd_wid0				reserved			vo_id_sel	outstd_rid0				outstd_rid1				arb_mode			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	-	vo_ck_gt_en	Clock gating enable. 0: disabled 1: enabled

[30]	RW	vo_id_sel	VOU read ID select. 0: 0 1: 1
[29:28]	-	reserved	Reserved.
[27:24]	RW	awid_cfg	ID written by the AXI bus.
[23:22]	-	reserved	Reserved.
[21:20]	RW	bus_dbg_en	Bus debugging enable. 00: normal mode 01: read-write loopback mode for bus test 10: write loopback mode for bus test Other values: reserved
[19:16]	RW	outstd_wid0	Outstanding of the AXI bus write channel.
[15:12]	RW	arid_cfg1	ID1 of the AXI bus read channel.
[11:8]	RW	outstd_rid0	ID0 of the AXI bus read channel.
[7:4]	RW	outstd_rid1	Outstanding of the AXI bus read channel.
[3:0]	RW	arb_mode	Arbitration mode of requesting data for each internal surface bus of the VOU. 0000: The polling mode is used. 0001: The graphics layer takes priority. Other values: reserved

VOINTSTA

VOINTSTA is a VO interrupt status register. It is a read-only register.

Offset Address	Register Name	Total Reset Value
0xCE04	VOINTSTA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	be_int	reserved	vdac_int	reserved					g3rr_int	reserved		vsd1rr_int	reserved																dsduf_int	reserved	dsdvtthd1_int	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	be_int	Bus error interrupt (AXI_Master). 0: No interrupt is generated. 1: An interrupt is generated.

Offset Address	Register Name	Total Reset Value
0xCE04	VOINTSTA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	be_int	reserved	vdac_int	reserved					g3rr_int	reserved		vsd1rr_int	reserved																dsduf_int	reserved	dsdvtthd1_int	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[30]	RO	reserved	Reserved.
[29]	RO	vdac_int	VDAC connection interrupt.
[28:24]	RO	reserved	Reserved.
[23]	RO	g3rr_int	G3 register update interrupt.
[22:21]	RO	reserved	Reserved.
[20]	RO	vsd1rr_int	VSD1 register update interrupt.
[19:4]	RO	reserved	Reserved.
[3]	RO	dsduf_int	DSD low-bandwidth alarm interrupt.
[2]	RO	reserved	Reserved.
[1]	RO	dsdvtthd1_int	DSD1 vertical timing interrupt.
[0]	RO	reserved	Reserved.

VOMSKINTSTA

VOMSKINTSTA is a VO masked interrupt status register. Writing 1 clears this register.

Offset Address	Register Name	Total Reset Value
0xCE08	VOMSKINTSTA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	be_int	reserved	vdac_int	reserved					g3rr_int	reserved		vsd1rr_int	reserved																dsduf_int	reserved	dsdvtthd1_int	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	be_int	Bus error interrupt (AXI_Master). 0: No interrupt is generated. 1: An interrupt is generated.
[30]	RO	reserved	Reserved.
[29]	RO	vdac_int	VDAC connection interrupt.
[28:24]	RO	reserved	Reserved.
[23]	RO	g3rr_int	G3 register update interrupt.
[22:21]	RO	reserved	Reserved.
[20]	RO	vsd1rr_int	VSD1 register update interrupt.
[19:4]	RO	reserved	Reserved.
[3]	RO	dsduf_int	DSD low-bandwidth alarm interrupt.
[2]	RO	reserved	Reserved.
[1]	RO	dsdvtthd1_int	DSD1 vertical timing interrupt.
[0]	RO	reserved	Reserved.

VOINTMSK

VOINTMSK is a VDP interrupt mask register. It corresponds to VOINTSTA. When the corresponding bit is set to 1, the interrupt is enabled; when the corresponding bit is set to 0, the interrupt is masked.

Offset Address	Register Name	Total Reset Value
0xCE0C	VOINTMSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	be_intmask	reserved	vdac_intmask	reserved					g3rr_intmask	reserved		vsd1rr_intmask	reserved																dsduf_intmask	reserved	dsdvtthd1_intmask	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	be_intmask	Bus error interrupt (AXI_Master). 0: No interrupt is generated. 1: An interrupt is generated.
[30]	RO	reserved	Reserved.
[29]	RO	vdac_ic_int	VDAC connection interrupt.
[28:24]	RO	reserved	Reserved.
[23]	RO	g3rr_intmsk	G3 register update interrupt.
[22:21]	RO	reserved	Reserved.
[20]	RO	vsd1rr_intmask	VSD1 register update interrupt.
[19:4]	RO	reserved	Reserved.
[3]	RO	dsduf_intmask	DSD low-bandwidth alarm interrupt.
[2]	RO	reserved	Reserved.
[1]	RO	dsdvtthd1_intmask	DSD1 vertical timing interrupt.
[0]	RO	reserved	Reserved.

VOUVERSION1

VOUVERSION1 is VDP version register 1.

Offset Address	Register Name	Total Reset Value
0xCE10	VOUVERSION1	0x7675_6F76

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vouversion0																															
Reset	0	1	1	1	0	1	1	0	0	1	1	1	0	1	0	1	0	1	1	0	1	1	1	1	0	1	1	1	0	1	1	0

Bits	Access	Name	Description
[31:0]	RO	vouversion0	VDP version.

VOUVERSION2

VOUVERSION2 is VDP version register 2.

Offset Address	Register Name	Total Reset Value
0xCE14	VOUVERSION2	0x3030_3134

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vouversion1																															
Reset	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0	1	0	0	1	1	0	1	0	0

Bits	Access	Name	Description
[31:0]	RO	vouversion1	VDP version.

VOMUX

VOMUX is a VO interface multiplexing register.

Offset Address	Register Name	Total Reset Value
0xCE1C	VOMUX	0x0004_001B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								bt1120_sel_yc	reserved																						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1

Bits	Access	Name	Description
[31:24]	RW	reserved	Reserved.

[23]	RW	bt1120_sel_yc	BT.1120 Y/C position select. 0: The upper eight bits are used to transmit the Y component, and the lower eight bits are used to transmit the C component. 1: The upper eight bits are used to transmit the C component, and the lower eight bits are used to transmit the Y component.
[22:0]	-	reserved	Reserved.

Contents

Figures

Tables

11 ISP

11.1 Features

The image signal processor (ISP) has the following features:

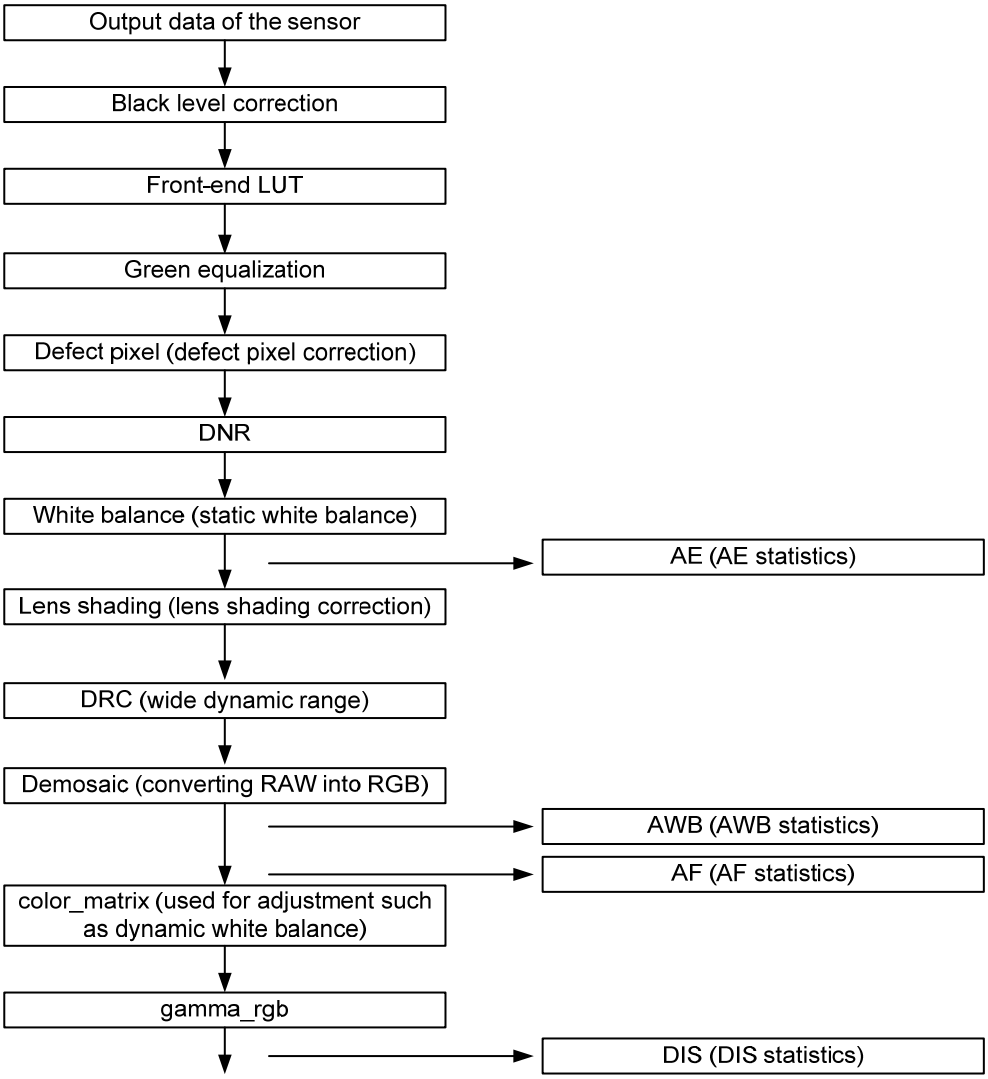
- Supports black level correction.
- Supports defect pixel correction.
- Supports domain noise reduction (DNR).
- Supports gamma correction.
- Supports dynamic range compression (DRC).
- Supports automatic white balance (AWB) with the 17x15 region weight setting.
- Supports automatic exposure (AE) with the 17x15 region weight setting.
- Supports auto focus (AF) with the 17x15 region weight setting.
- Supports digital anti-shake function.
- Supports the output of statistics.
- Supports lens shading correction.
- Supports image edge sharpening.
- Supports the maximum image resolution of 1920x1080
- . Supports the minimum image resolution of 480x240
- Supports the minimum horizontal blanking zone of 32 pixels.
- Supports the minimum vertical blanking zone of 19 lines.

11.2 Function Description

11.2.1 Function Block Diagram

Figure 11-1 shows the function block diagram of the ISP.

Figure 11-1 ISP architecture



11.2.2 Function Description

Sensor Offset Module

This module provides the sensor-related black-level correction function and supports the offset setting of four components (R, Gr, Gb, and B).

Front-end LUT Module

This module corrects the sensor-related gamma curve. The gamma curve is composed of 129 points with each point represented by a 12-bit data segment. The points between the given data points are obtained through interpolation. The gamma curve requires that gamma[0] is 0x000 and gamma[128] is 0xFFF.

Green Equalization Module

This module suppresses the noise in the green channel.

Defect Pixel Module

This module corrects defect pixels for the sensor. The defect pixels can be classified into dynamic defect pixels and static defect pixels. A maximum of 1024 static defect pixels can be corrected after detection. The number of dynamic defect pixels that can be corrected is not limited, and detection is not required before correction. The detection of static defect pixels, however, is more accurate than the detection of dynamic pixels.

DNR Module

This module provides the DNR function.

White Balance Module

This module provides the white balance function and supports the gain and offset setting of four components (R, Gr, Gb, and B).

Shading Module

This module corrects the lens shading. It supports the gain setting of three components (R, G, and B) for the pixels. Each pixel gain is represented by an 8-bit data segment. You can set the pixel gain for a maximum of 64x64 points and obtain the other points through interpolation.

DRC Module

This module provides the vision-based DRC function. It restrains the brightness in the bright regions of an image to prevent overexposure and increases the brightness of the dark regions to record more details. With the DRC function, a blurred image can become clear.

Demosaic Module

This module performs the conversion from Bayer to RGB color space.

Color_matrix Module

This module provides matrix manipulation function, as shown in Figure 11-2. The R, G, and B are the input data, and the R', G', and B' are the output data. The color_matrix module dynamically adjusts the matrix coefficients to implement AWB, saturation adjustment, and color correction.

Figure 11-2 Matrix manipulation of the color_matrix module

$$\begin{pmatrix} R' \\ G' \\ B' \end{pmatrix} = \begin{pmatrix} m_{RR} & m_{RG} & m_{RB} \\ m_{GR} & m_{GG} & m_{GB} \\ m_{BR} & m_{BG} & m_{BB} \end{pmatrix} \cdot \begin{pmatrix} R \\ G \\ B \end{pmatrix}$$

Gamma_rgb Module

This module adjusts the output gamma curve. The gamma curve is composed of 65 points with each point represented by a 16-bit data segment. The points between the given data points are obtained through interpolation. The gamma curve requires that gamma[0] is 0x000 and gamma[64] is 0xFFF.

AE Module

This module collects the AE statistics. The software can adjust the sensor based on the AE statistics to implement the AE function. The AE module divides an image into 7x9 regions (7 rows and 9 columns) and sets the weight for each region. Each region is further divided into five segments for histogram statistics collection. The histogram statistics are normalized to 0xFFFF. Therefore, only the statistics on segments 0, 1, 3, and 4 are stored. The software can read the final weighted statistics or the statistics on each region.

AWB Module

This module collects the AWB statistics. The software can adjust the color_matrix module based on the AWB statistics to implement the AWB function. The AWB module divides an image into 7x9 regions (7 rows and 9 columns) and sets the weight for each region. The module then collects the R/G and B/G values of each region and the number of pixels involved in the value collection. The software can read the final weighted statistics and the statistics on each region.

AF Module

This module collects the AF statistics. The software can adjust the lens based on the AF statistics to implement the AF function. The AF module divides an image into 7x9 regions (7 rows and 9 columns) and sets the weight for each region. The module then collects the edge sharpness of each region. The software can reads the final weighted statistics or the statistics on each region.

DIS Module

This module implements the digital anti-shake function and collects the anti-shake statistics. It collects the information about the relationship between images with the horizontal offset ranging from –32 pixels to 31 pixels and between the images with the vertical offset ranging from –32 pixels to 31 pixels and calculates the final offset.

11.3 Fixed-Point Number Format

The format of a fixed-point number is represented by a.b, in which a indicates the width of integer part and b indicates the width of fractional part.

For example, the number 4.8 indicates that the upper 4 bits are used for the integer part and the lower 8 bits are used for the fractional part.

11.4 Register Summary

Table 11-1 describes the ISP registers.

Table 11-1 Summary of ISP registers (base address: 0x205A_0000)

Offset Address	Register	Description	Page
0x0010	ACTIVE_WIDTH	ACTIVE_WIDTH is a picture width register.	11-14
0x0014	ACTIVE_HEIGHT	ACTIVE_HEIGHT is a picture height register.	11-15
0x0018	RGGB_START	RGGB_START is an RGGB mode register.	11-15
0x0030	CONFIG_BUFFER_MODE	CONFIG_BUFFER_MODE is an update mode configuration register.	11-16
0x0040	BYPASS	BYPASS is a bypass register.	11-17
0x0044	AE_SWITCH	AE_SWITCH is an AE region statistics position control register.	11-18
0x0048	AWB_SWITCH	AWB_SWITCH is an AWB statistics position control register.	11-19
0x004C	AF_SWITCH	AF_SWITCH is an AF statistics position control register.	11-19
0x0050	DIS_SWITCH	DIS_SWITCH is a DIS statistics position control register.	11-20
0x0054	HISTOGRAM_SWITCH	HISTOGRAM_SWITCH is an AE global statistics position control register.	11-20
0x0080	INTERRUPT0	INTERRUPT0 is interrupt 0 register.	11-21
0x0084	INTERRUPT1	INTERRUPT1 is interrupt 1 register.	11-21
0x0088	INTERRUPT2	INTERRUPT2 is interrupt 2 register.	11-22
0x008C	INTERRUPT3	INTERRUPT3 is interrupt 3 register.	11-22
0x0090	INTERRUPT4	INTERRUPT4 is interrupt 4 register.	11-23
0x0094	INTERRUPT5	INTERRUPT5 is interrupt 5 register.	11-23
0x0098	INTERRUPT6	INTERRUPT6 is interrupt 6 register.	11-23
0x009C	INTERRUPT7	INTERRUPT7 is interrupt 7 register.	11-24
0x0130	INPUTPORT_CTRL	INPUTPORT_CTRL is an input port control register.	11-24
0x0134	INPUTPORT_STATUS	INPUTPORT_STATUS is an input port status register.	11-25

Offset Address	Register	Description	Page
0x0140	SENSOR_R_BLACK	SENSOR_R_BLACK is an R component black level register for the sensor offset module.	11-26
0x0144	SENSOR_GR_BLACK	SENSOR_GR_BLACK is a Gr component black level register for the sensor offset module.	11-26
0x0148	SENSOR_GB_BLACK	SENSOR_GB_BLACK is a Gb component black level register for the sensor offset module.	11-27
0x014C	SENSOR_B_BLACK	SENSOR_B_BLACK is a B component black level register for the sensor offset module.	11-27
0x0188	FRONTEND_LUT_STATUS	FRONTEND_LUT_STATUS is a front-end LUT status register.	11-28
0x01C0	GE_CTRL1	GE_CTRL1 is green equalization module control register 1.	11-28
0x01C4	GE_CTRL2	GE_CTRL2 is green equalization module control register 2.	11-29
0x01C8	GE_CTRL3	GE_CTRL3 is green equalization module control register 3.	11-30
0x01CC	GE_CTRL4	GE_CTRL4 is green equalization module control register 4.	11-30
0x01D0	GE_CTRL5	GE_CTRL5 is green equalization module control register 5.	11-31
0x01D4	GE_CTRL6	GE_CTRL6 is green equalization module control register 6.	11-31
0x01E8	HP_DEFECT_PIXEL_CTRL	HP_DEFECT_PIXEL_CTRL is a defect pixel module control register.	11-31
0x01EC	HP_COUNT	HP_COUNT is a defect pixel count register for the defect pixel module.	11-32
0x01F0	HP_TABLE_START	HP_TABLE_START is a defect pixel start address register for the defect pixel module.	11-33
0x01F4	HP_COUNT_IN	HP_COUNT_IN is a written defect pixel count register for the defect pixel module.	11-33
0x0850	HP_TABLE_LUT_ADDR	HP_TABLE_LUT_ADDR is a lookup table (LUT) address register for the defect pixel module.	11-34

Offset Address	Register	Description	Page
0x0854	HP_TABLE_LUT_WRITE_DATA	HP_TABLE_LUT_WRITE_DATA is an LUT write data register for the defect pixel module.	11-34
0x0858	HP_TABLE_LUT_READ_DATA	HP_TABLE_LUT_READ_DATA is an LUT read data register for the defect pixel module.	11-34
0x0200	DNR_CTRL1	DNR_CTRL1 is DNR module control register 1.	11-35
0x0204	DNR_CTRL2	DNR_CTRL2 is DNR module control register 2.	11-36
0x0208	DNR_CTRL3	DNR_CTRL3 is DNR module control register 3.	11-36
0x020C	DNR_THRESH_2H	DNR_THRESH_2H is a horizontal intermediate-frequency noise threshold register for the DNR module.	11-36
0x0210	DNR_THRESH_4H	DNR_THRESH_4H is a horizontal low-frequency noise threshold register for the DNR module.	11-37
0x0214	DNR_THRESH_0V	DNR_THRESH_0V is a vertical high-frequency noise threshold register for the DNR module.	11-37
0x0218	DNR_THRESH_1V	DNR_THRESH_1V is a vertical green noise threshold register for the DNR module.	11-38
0x021C	DNR_THRESH_2V	DNR_THRESH_2V is a vertical intermediate-frequency noise threshold for the DNR module.	11-38
0x0220	DNR_THRESH_4V	DNR_THRESH_4V is a vertical low-frequency noise threshold for the DNR module.	11-38
0x0224	DNR_THRESH_SHORT	DNR_THRESH_SHORT is a short exposure noise threshold register for the DNR module.	11-39
0x0228	DNR_THRESH_LONG	DNR_THRESH_LONG is a long exposure noise threshold register for the DNR module.	11-39
0x022C	DNR_STRENGTH0	DNR_STRENGTH0 is a high-frequency component denoise strength register for the DNR module.	11-40

Offset Address	Register	Description	Page
0x0230	DNR_STRENGTH1	DNR_STRENGTH1 is a green component denoise strength register for the DNR module.	11-40
0x0234	DNR_STRENGTH2	DNR_STRENGTH2 is an intermediate-frequency denoise strength register for the DNR module.	11-40
0x0238	DNR_STRENGTH4	DNR_STRENGTH4 is a low-frequency denoise strength register for the DNR module.	11-41
0x0970	RADIAL_LUT1	RADIAL_LUT1 is radial LUT 1 register for the DNR module.	11-41
0x0974	RADIAL_LUT2	RADIAL_LUT2 radial LUT 2 register for the DNR module.	11-42
0x098C	RADIAL_LUT3	RADIAL_LUT3 radial LUT 3 register for the DNR module.	11-42
0x0990	RADIAL_LUT4	RADIAL_LUT4 radial LUT 4 register for the DNR module.	11-43
0x0780	DNR_NOISE_PROFILE_LUT1	DNR_NOISE_PROFILE_LUT1 is a noise profile LUT write data register for the DNR module.	11-43
0x0784	DNR_NOISE_PROFILE_LUT2	DNR_NOISE_PROFILE_LUT2 is a noise profile LUT write data register for the DNR module.	11-44
0x07FC	DNR_NOISE_PROFILE_LUTn	DNR_NOISE_PROFILE_LUTn is a noise profile LUT write data register for the DNR module.	11-44
0x0270	DNR_EXP_THRESH	DNR_EXP_THRESH is a long/short exposure threshold register for the DNR module.	11-45
0x0274	DNR_RATIO_SHORT	DNR_RATIO_SHORT is a short exposure noise profile LUT multiplier register for the DNR module.	11-45
0x0278	DNR_RATIO_LONG	DNR_RATIO_LONG is a long exposure noise profile LUT multiplier register for the DNR module.	11-46
0x02C0	WB_GAIN00	WB_GAIN00 is an R component gain register for the white balance module.	11-46
0x02C4	WB_GAIN01	WB_GAIN01 is a Gr component gain register for the white balance module.	11-47
0x02C8	WB_GAIN10	WB_GAIN10 is a Gb component gain register for the white balance module.	11-47

Offset Address	Register	Description	Page
0x02CC	WB_GAIN11	WB_GAIN11 is a B component gain register for the white balance module.	11-48
0x02D0	WB_BLACK00	WB_BLACK00 is an R component black level register for the white balance module.	11-48
0x02D4	WB_BLACK01	WB_BLACK01 is a Gr component black level register for the white balance module.	11-49
0x02D8	WB_BLACK10	WB_BLACK10 is a Gb component black level register for the white balance module.	11-49
0x02DC	WB_BLACK11	WB_BLACK11 is a B component black level register for the white balance module.	11-49
0x0300	SHADING_CTRL	SHADING_CTRL is a lens shading module control module.	11-50
0x0304	SHADING_RX	SHADING_RX is an R component center horizontal coordinate register for the lens shading module.	11-50
0x0308	SHADING_RY	SHADING_RY is an R component center vertical coordinate register for the lens shading module.	11-51
0x030C	SHADING_GX	SHADING_GX is a G component center horizontal coordinate register for the lens shading module.	11-51
0x0310	SHADING_GY	SHADING_GY is a G component center vertical coordinate register for the lens shading module.	11-52
0x0314	SHADING_BX	SHADING_BX is a B component center horizontal coordinate register for the lens shading module.	11-52
0x0318	SHADING_BY	SHADING_BY is a B component center vertical coordinate register for the lens shading module.	11-52
0x031C	SHADING_MULTR	SHADING_MULTR is an R component shading factor for the lens shading module.	11-53
0x0320	SHADING_MULTG	SHADING_MULTG is a G component shading factor for the lens shading module.	11-53
0x0324	SHADING_MULTB	SHADING_MULTB is a B component shading factor for the lens shading module.	11-54
0x0380	DRC_ENABLE	DRC_ENABLE is a DRC enable register.	11-54
0x0384	DRC_STRENGTH	DRC_STRENGTH is a DRC strength register.	11-54

Offset Address	Register	Description	Page
0x0388	DRC_CTRL	DRC_CTRL is a DRC module control register.	11-55
0x03C8	DRC_LOOKUP1_ENABLE	DRC_LOOKUP1_ENABLE is a DRC LUT1 enable register.	11-55
0x0820	DRC_LUT1_ADDR	DRC_LOOKUP1_ENABLE is a DRC LUT1 address register.	11-56
0x0824	DRC_LUT1_DATA	DRC_LOOKUP1_ENABLE is a DRC LUT1 data register.	11-56
0x03E8	DRC_LOOKUP2_ENABLE	DRC_LOOKUP1_ENABLE is a DRC LUT2 enable register.	11-57
0x0830	DRC_LUT2_ADDR	DRC_LOOKUP1_ENABLE is a DRC LUT2 address register.	11-57
0x0834	DRC_LUT2_DATA	DRC_LOOKUP1_ENABLE is a DRC LUT2 data register.	11-58
0x0400	DEMOSAIC_VH_SLOPE	DEMOSAIC_VH_SLOPE is a maximum vertical/horizontal slope register for the demosaic module.	11-58
0x0404	DEMOSAIC_AA_SLOPE	DEMOSAIC_AA_SLOPE is an AA slope register.	11-59
0x0408	DEMOSAIC_VA_SLOPE	DEMOSAIC_VA_SLOPE is a VA slope register.	11-59
0x040C	DEMOSAIC_UU_SLOPE	DEMOSAIC_UU_SLOPE is a UU slope register.	11-60
0x0410	DEMOSAIC_SAT_SLOPE	DEMOSAIC_SAT_SLOPE is an SAT slope register.	11-60
0x0414	DEMOSAIC_VH_THRESH	DEMOSAIC_VH_THRESH is a VH threshold register.	11-60
0x0418	DEMOSAIC_AA_THRESH	DEMOSAIC_AA_THRESH is an AA threshold register.	11-61
0x041C	DEMOSAIC_VA_THRESH	DEMOSAIC_VA_THRESH is a VA threshold register.	11-61
0x0420	DEMOSAIC_UU_THRESH	DEMOSAIC_UU_THRESH is a UU threshold register.	11-62
0x0424	DEMOSAIC_SAT_THRESH	DEMOSAIC_AA_OFFSET is an AA threshold register.	11-62
0x0428	DEMOSAIC_VH_OFFSET	DEMOSAIC_VH_OFFSET is a vertical/horizontal offset register for the demosaic module.	11-62

Offset Address	Register	Description	Page
0x042C	DEMOSAIC_AA_OFFSET	DEMOSAIC_AA_OFFSET is an AA offset register.	11-63
0x0430	DEMOSAIC_VA_OFFSET	DEMOSAIC_VA_OFFSET is a VA offset register.	11-63
0x0434	DEMOSAIC_UU_OFFSET	DEMOSAIC_UU_OFFSET is a UU offset register.	11-64
0x0438	DEMOSAIC_SAT_OFFSET	DEMOSAIC_SAT_OFFSET is an SAT offset register.	11-64
0x043C	DEMOSAIC_SHARP_ALT_D	DEMOSAIC_SHARP_ALT_D is an edge sharpen strength register.	11-64
0x0440	DEMOSAIC_SHARP_ALT_UD	DEMOSAIC_SHARP_ALT_UD is a flat area sharpen strength register.	11-65
0x0444	DEMOSAIC_LUM_THRESH	DEMOSAIC_LUM_THRESH is an LUM threshold register.	11-65
0x0448	DEMOSAIC_NP_OFFSET	DEMOSAIC_NP_OFFSET is an NP offset register.	11-66
0x0450	DEMOSAIC_AC_THRESH	DEMOSAIC_AC_THRESH is an AC threshold register.	11-66
0x0454	DEMOSAIC_AC_SLOPE	DEMOSAIC_AC_SLOPE is an AC slope register.	11-66
0x0458	DEMOSAIC_AC_OFFSET	DEMOSAIC_AC_OFFSET is an AC offset register.	11-67
0x045C	DEMOSAIC_FC_SLPOE	DEMOSAIC_FC_SLPOE is an anti-false color strength register.	11-67
0x0C00	NP_LUT_WEIGHT1	NP_LUT_WEIGHT1 is noise profile LUT weight 1 register.	11-68
0x0C04	NP_LUT_WEIGHT2	NP_LUT_WEIGHT2 is noise profile LUT weight 2 register.	11-68
0x0C7C	NP_LUT_WEIGHTn	NP_LUT_WEIGHTn is noise profile LUT weight n register.	11-68
0x04A4	CCM_CTRL	CCM_CTRL is a color matrix module control register.	11-69
0x0480	CCM_COEFFT_RR	CCM_COEFFT_RR is an RR position coefficient register for the color matrix module.	11-69
0x0484	CCM_COEFFT_RG	CCM_COEFFT_RG is an RG position coefficient register for the color matrix module.	11-70

Offset Address	Register	Description	Page
0x0488	CCM_COEFFT_RB	CCM_COEFFT_RB is an RB position coefficient register for the color matrix module.	11-70
0x048C	CCM_COEFFT_GR	CCM_COEFFT_GR is a GR position coefficient register for the color matrix module.	11-71
0x0490	CCM_COEFFT_GG	CCM_COEFFT_GG is a GG position coefficient register for the color matrix module.	11-71
0x0494	CCM_COEFFT_GB	CCM_COEFFT_GB is a GB position coefficient register for the color matrix module.	11-72
0x0498	CCM_COEFFT_BR	CCM_COEFFT_BR is a BR position coefficient register for the color matrix module.	11-72
0x049C	CCM_COEFFT_BG	CCM_COEFFT_BG is a BG position coefficient register for the color matrix module.	11-72
0x04A0	CCM_COEFFT_BB	CCM_COEFFT_BB is a BB position coefficient register for the color matrix module.	11-73
0x04A8	CCM_COEFFT_WBR	CCM_COEFFT_WBR is an R component white balance gain register for the color matrix module.	11-73
0x04AC	CCM_COEFFT_WBG	CCM_COEFFT_WBG is a G component white balance gain register for the color matrix module.	11-74
0x04B0	CCM_COEFFT_WBB	CCM_COEFFT_WBB is a B component white balance gain register for the color matrix module.	11-74
0x0600	METERING_HIST_THRESH01	METERING_HIST_THRESH01 is segment 0 and segment 1 boundary point register for histogram statistics.	11-75
0x0604	METERING_HIST_THRESH12	METERING_HIST_THRESH12 is segment 1 and segment 2 boundary point register for histogram statistics.	11-75
0x0608	METERING_HIST_THRESH34	METERING_HIST_THRESH34 is segment 3 and segment 4 boundary point register for histogram statistics.	11-76
0x060C	METERING_HIST_THRESH45	METERING_HIST_THRESH45 is segment 4 and segment 5 boundary point register for histogram statistics.	11-76

Offset Address	Register	Description	Page
0x0620	METERING_HIST0	METERING_HIST0 is histogram statistics register for segment 0.	11-76
0x0624	METERING_HIST1	METERING_HIST1 is histogram statistics register for segment 1.	11-77
0x0628	METERING_HIST3	METERING_HIST3 is histogram statistics register for segment 3.	11-77
0x062C	METERING_HIST4	METERING_HIST4 is histogram statistics register for segment 4.	11-78
0x0630	AE_NODES_USED	AE_NODES_USED is an AE active region register.	11-78
0x0640	METERING_AWB_WHITE_LEVEL	METERING_AWB_WHITE_LEVEL is an AWB brightest point register.	11-78
0x0644	METERING_AWB_BLACK_LEVEL	METERING_AWB_BLACK_LEVEL is an AWB darkest point register.	11-79
0x0648	METERING_AWB_CR_REF_MAX	METERING_AWB_CR_REF_MAX is the maximum Cr value register for the AWB reference white point.	11-79
0x064C	METERING_AWB_CR_REF_MIN	METERING_AWB_CR_REF_MIN is the minimum Cr value register for the AWB reference white point.	11-80
0x0650	METERING_AWB_CB_REF_MAX	METERING_AWB_CB_REF_MAX is the maximum Cb value register for the AWB reference white point.	11-80
0x0654	METERING_AWB_CB_REF_MIN	METERING_AWB_CB_REF_MIN is the minimum Cb value register for the AWB reference white point.	11-80
0x0658	METERING_AWB_RG	METERING_AWB_RG is an AWB output G/R register.	11-81
0x065C	METERING_AWB_BG	METERING_AWB_BG is an AWB output G/B register.	11-81
0x0660	METERING_AWB_SUM	METERING_AWB_SUM is an AWB reference white point count register.	11-82
0x0670	AWB_NODES_USED	AWB_NODES_USED is an AWB active region register.	11-82
0x068C	AF_METRICS_SHIFT	AF_METRICS_SHIFT is an AF metric conversion register.	11-83
0x0680	METERING_AF_METRICS	METERING_AF_METRICS is an AF metric statistics register.	11-83

Offset Address	Register	Description	Page
0x0684	METERING_AF_THRESHOLD_WRITE	METERING_AF_THRESHOLD_WRITE is a preset AF threshold register.	11-83
0x0688	METERING_AF_THRESHOLD_READ	METERING_AF_THRESHOLD_READ is an updated AF threshold register.	11-84
0x0690	AF_NODES_USED	AF_NODES_USED is an AF active region register.	11-84
0x0694	AF_NP_OFFSET	AF_NP_OFFSET is an AF noise profile offset register.	11-85
0x06C0	HISTOGRAM_CTRL	HISTOGRAM_CTRL is a histogram control register.	11-85
0x06C4	SCALE_CTRL	SCALE_CTRL is a scale control register.	11-86
0x06C8	TOTAL_PIXELS	TOTAL_PIXELS is a total pixel number register.	11-87
0x06CC	COUNTED_PIXEL	COUNTED_PIXEL is an involved pixel count register for statistics.	11-87
0x06D0	HISTOGRAM_DATA_SHIFT	HISTOGRAM_DATA_SHIFT is a global statistical data offset register.	11-88
0x0B00	METERING_AWB_WEIGHT	METERING_AWB_WEIGHT is an AWB window weight register.	11-88
0x04C0	GAMMA_STATUS	GAMMA_CTRL is a gamma module status register.	11-89
0x0700	DIS_CTRL	DIS_CTRL is a DIS module control register.	11-90
0x0704	DIS_OFFSET_X	DIS_OFFSET_X is horizontal offset register for the DIS module.	11-91
0x0708	DIS_OFFSET_Y	DIS_OFFSET_Y is a vertical offset register for the DIS module.	11-91

11.4.2 Register Description

ACTIVE_WIDTH

ACTIVE_WIDTH is a picture width register.

Offset Address	Register Name	Total Reset Value
0x0010	ACTIVE_WIDTH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ActiveWidth															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:0]	RW	ActiveWidth	Active video width (in pixel).

ACTIVE_HEIGHT

ACTIVE_HEIGHT is a picture height register.

Offset Address	Register Name	Total Reset Value
0x0014	ACTIVE_HEIGHT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ActiveHeight															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:0]	RW	ActiveHeight	Active video height (in line).

RGGB_START

RGGB_START is an RGGB mode register.

Offset Address	Register Name	Total Reset Value
0x0018	RGGB_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														RGGBstart	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RW	reserved	Reserved.

Offset Address	Register Name	Total Reset Value
0x0018	RGGB_START	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							RGGBstart
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[1:0]	RW	RGGBstart	Start color of the RGGB pattern. 00: R Gr Gb B 01: Gr R B Gb 10: Gb B R Gr 11: B Gb

CONFIG_BUFFER_MODE

CONFIG_BUFFER_MODE is an update mode configuration register.

Offset Address	Register Name	Total Reset Value
0x0030	CONFIG_BUFFER_MODE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							ConfigBufferMode
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:2]	RW	reserved	Reserved.
[1:0]	RW	ConfigBufferMode	Double-buffer mode select. 00: disabled (configuration are updated immediately) 01: blocked (configuration are not updated) 10: local (module configurations are updated during local vertical blanking) 11: global (all module configurations are updated during ISP vertical blanking)

BYPASS

BYPASS is a bypass register.

Offset Address	Register Name	Total Reset Value
0x0040	BYPASS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					ISPfullbypassenable	ISPprocessingbypassmode		reserved				reserved		reserved		Bypassgamma		Bypasscolor		Bypassdemosaic		BypassDRC		reserved		Bypassradial		reserved		Bypassgain		Bypassdenoise		Bypassdefectpixel		Bypassgreenequalize		Bypassgammafe		Bypassbalancefe		Bypassvideotestgen	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RW	reserved	Reserved.
[26]	RW	ISPfullbypassenable	Output is connected directly to input.
[25:24]	RW	ISPprocessingbypassmode	00: full processing 01: bypass entire ISP processing (video input and output ports are still connected) and output raw sensor data 10: bypass entire ISP processing (video input and output ports are still connected) and output raw sensor data in most significant bits of channels 1 and 2 11: connect output to ground
[23:19]	RW	reserved	Reserved.
[18]	RW	reserved	Reserved.
[17:15]	RW	reserved	Reserved.
[14]	RW	Bypassgamma	Bypass gamma table.
[13]	RW	Bypasscolor	Bypass color matrix.
[12]	RW	Bypassdemosaic	Bypass demosaic module (output raw data).
[11]	RW	BypassDRC	Bypass DRC.
[10]	RW	reserved	Reserved.
[9]	RW	Bypassradial	Bypass shading.
[8:7]	RW	reserved	Reserved.
[6]	RW	Bypassgain	Bypass black level/gain.

Offset Address	Register Name	Total Reset Value
0x0040	BYPASS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					ISPfullbypassenable	ISPprocessingbypassmode		reserved				reserved		reserved		Bypassgamma		Bypasscolor		Bypassdemosaic		BypassDRC	reserved	Bypassradial		reserved		Bypassgain		Bypassdenoise		Bypassdefectpixel		Bypassgreenequalize		Bypassgammafe		Bypassbalancefe		Bypassvideotestgen	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[5]	RW	Bypassdenoise	Bypass denoise.
[4]	RW	Bypassdefectpixel	Bypass defect pixel.
[3]	RW	Bypassgreenequalize	Bypass green equalization.
[2]	RW	Bypassgammafe	Bypass WDR compression front-end lookup.
[1]	RW	Bypassbalancefe	Bypass front-end black level adjustment.
[0]	RW	Bypassvideotestgen	Bypass video test generator.

AE_SWITCH

AE_SWITCH is an AE region statistics position control register.

Offset Address	Register Name	Total Reset Value
0x0044	AE_SWITCH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														AEswitch	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RW	reserved	Reserved.

Offset Address	Register Name	Total Reset Value
0x0044	AE_SWITCH	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							AEswitch
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[1:0]	RW	AEswitch	AE tap in the pipeline. 00: after static WB 01: immediately from sensor (for WDR compression modes) 10: after shading 11: after front-end LUT (for WDR compression modes)

AWB_SWITCH

AWB_SWITCH is an AWB statistics position control register.

Offset Address	Register Name	Total Reset Value
0x0048	AWB_SWITCH	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							AWBswitch
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:1]	RW	reserved	Reserved.
[0]	RW	AWBswitch	AWB tap in the pipeline. 0: immediately before color matrix 1: immediately after color matrix (for sensors with strong color channel crosstalk)

AF_SWITCH

AF_SWITCH is an AF statistics position control register.

Offset Address	Register Name	Total Reset Value
0x004C	AF_SWITCH	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								AFswitch
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RW	reserved	Reserved.
[0]	RW	AFswitch	AF tap in the pipeline. 0: enabled 1: disabled

DIS_SWITCH

DIS_SWITCH is a DIS statistics position control register.

Offset Address	Register Name	Total Reset Value
0x0050	DIS_SWITCH	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								DISswitch
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:2]	RW	reserved	Reserved.
[1:0]	RW	DISswitch	DIS tap in the pipeline. 00: end of pipeline 01: after DRC 10: after defect pixel 11: switched off

HISTOGRAM_SWITCH

HISTOGRAM_SWITCH is an AE global statistics position control register.

Offset Address	Register Name	Total Reset Value
0x0054	HISTOGRAM_SWITCH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														Histogramswitch	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RW	reserved	Reserved.
[1:0]	RW	Histogramswitch	AE tap in the pipeline. 00: same as AE 01: immediately from sensor (for WDR compression modes) 10: after shading 11: after front-end LUT (for WDR compression modes)

INTERRUPT0

INTERRUPT0 is interrupt 0 register.

Offset Address	Register Name	Total Reset Value
0x0080	INTERRUPT0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												Interrupt0source			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RW	reserved	Reserved.
[4:0]	RW	Interrupt0source	Interrupt source select.

INTERRUPT1

INTERRUPT1 is interrupt 1 register.

Offset Address	Register Name	Total Reset Value
0x0084	INTERRUPT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												Interrupt1source			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RW	reserved	Reserved.
[4:0]	RW	Interrupt1source	Interrupt source select.

INTERRUPT2

INTERRUPT2 is interrupt 2 register.

Offset Address	Register Name	Total Reset Value
0x0088	INTERRUPT2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												Interrupt2source			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RW	reserved	Reserved.
[4:0]	RW	Interrupt2source	Interrupt source select.

INTERRUPT3

INTERRUPT3 is interrupt 3 register.

Offset Address	Register Name	Total Reset Value
0x008C	INTERRUPT3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												Interrupt3source			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RW	reserved	Reserved.
[4:0]	RW	Interrupt3source	Interrupt source select.

INTERRUPT4

INTERRUPT4 is interrupt 4 register.

Offset Address	Register Name	Total Reset Value
0x0090	INTERRUPT4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												Interrupt4source			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RW	reserved	Reserved.
[4:0]	RW	Interrupt4source	Interrupt source select.

INTERRUPT5

INTERRUPT5 is interrupt 5 register.

Offset Address	Register Name	Total Reset Value
0x0094	INTERRUPT5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												Interrupt5source			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RW	reserved	Reserved.
[4:0]	RW	Interrupt5source	Interrupt source select.

INTERRUPT6

INTERRUPT6 is interrupt 6 register.

Offset Address	Register Name	Total Reset Value
0x0098	INTERRUPT6	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												Interrupt6source			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RW	reserved	Reserved.

Offset Address	Register Name	Total Reset Value
0x0098	INTERRUPT6	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											Interrupt6source			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[4:0]	RW	Interrupt6source	Interrupt source select.

INTERRUPT7

INTERRUPT7 is interrupt 7 register.

Offset Address	Register Name	Total Reset Value
0x009C	INTERRUPT7	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											Interrupt7source			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RW	reserved	Reserved.
[4:0]	RW	Interrupt7source	Interrupt source select.

INPUTPORT_CTRL

INPUTPORT_CTRL is an input port control register.

Offset Address	Register Name	Total Reset Value
0x0130	INPUTPORT_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								freezeconfig	reserved			moderequest			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.

Offset Address	Register Name	Total Reset Value
0x0130	INPUTPORT_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								freezeconfig	reserved					moderequest		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7]	RW	freezeconfig	0: normal operation 1: retain the previous configuration state
[6:3]	RW	reserved	Reserved.
[2:0]	RW	moderequest	000: safe stop 001: safe start 010: urgent stop 011: urgent start 100: reserved 101: safer start 110: reserved 111: reserved

INPUTPORT_STATUS

INPUTPORT_STATUS is an input port status register.

Offset Address	Register Name	Total Reset Value
0x0134	INPUTPORT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														modestatus	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RW	reserved	Reserved.

Offset Address	Register Name	Total Reset Value
0x0134	INPUTPORT_STATUS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							modestatus
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[2:0]	RW	modestatus	For bit 0: 1: started 0: stopped For bits 1 and 2: reserved

SENSOR_R_BLACK

SENSOR_R_BLACK is an R component black level register for the sensor offset module.

Offset Address	Register Name	Total Reset Value
0x0140	SENSOR_R_BLACK	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				Black00			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:0]	RW	Black00	Black offset for color channel 00 (R).

SENSOR_GR_BLACK

SENSOR_GR_BLACK is a Gr component black level register for the sensor offset module.

Offset Address	Register Name	Total Reset Value
0x0144	SENSOR_GR_BLACK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																Black01															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:0]	RW	Black01	Black offset for color channel 01 (Gr).

SENSOR_GB_BLACK

SENSOR_GB_BLACK is a Gb component black level register for the sensor offset module.

Offset Address	Register Name	Total Reset Value
0x0148	SENSOR_GB_BLACK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																Black10															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:0]	RW	Black10	Black offset for color channel 10 (Gb).

SENSOR_B_BLACK

SENSOR_B_BLACK is a B component black level register for the sensor offset module.

Offset Address	Register Name	Total Reset Value
0x014C	SENSOR_B_BLACK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																Black11															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:0]	RW	Black11	Black offset for color channel 11 (B).

FRONTEND_LUT_STATUS

FRONTEND_LUT_STATUS is a front-end LUT status register.

Offset Address	Register Name	Total Reset Value
0x0188	FRONTEND_LUT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													MCUready	MCUpriority	Enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2]	RO	MCUready	LUT is ready to receive the data from the CPU.
[1]	0x0	MCUpriority	Priority of CPU port. 0: low 1: high
[0]	RO	Enable	front-end look-up enable. 0: off 1: on

GE_CTRL1

GE_CTRL1 is green equalization module control register 1.

Offset Address	Register Name	Total Reset Value
0x01C0	GE_CTRL1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												showdynamicdefectpixel	dpenable	reserved	geenable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RW	reserved	Reserved.
[3]	RW	showdynamicdefectpixel	Show defect pixel. 0: off 1: on
[2]	RW	dpenable	Defect pixel enable. 0: off 1: on
[1]	RW	reserved	Reserved.
[0]	RW	geenable	Green equalization enable. 0: off 1: on

GE_CTRL2

GE_CTRL2 is green equalization module control register 2.

Offset Address	Register Name	Total Reset Value
0x01C4	GE_CTRL2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								gestrength							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.

Offset Address	Register Name	Total Reset Value
0x01C4	GE_CTRL2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								gestrength							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gestrength	Green equalization strength.

GE_CTRL3

GE_CTRL3 is green equalization module control register 3.

Offset Address	Register Name	Total Reset Value
0x01C8	GE_CTRL3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				dpthreshold												reserved				debugsel											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	reserved	Reserved.
[27:16]	RW	dpthreshold	Green equalization configuration.
[15:12]	RW	reserved	Reserved.
[11:0]	RW	debugsel	Debug port select.

GE_CTRL4

GE_CTRL4 is green equalization module control register 4.

Offset Address	Register Name	Total Reset Value
0x01CC	GE_CTRL4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				gethreshold											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved.
[11:0]	RW	gethreshold	Green equalization configuration.

GE_CTRL5

GE_CTRL5 is green equalization module control register 5.

Offset Address	Register Name	Total Reset Value
0x01D0	GE_CTRL5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				dpslope											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved.
[11:0]	RW	dpslope	Slope for the HP mask function.

GE_CTRL6

GE_CTRL6 is green equalization module control register 6.

Offset Address	Register Name	Total Reset Value
0x01D4	GE_CTRL6	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								gesens								reserved				geslope											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	reserved	Reserved.
[23:16]	RW	gesens	STD-DEV sensitivity.
[15:12]	RW	reserved	Reserved.
[11:0]	RW	geslope	Slope for the GE mask function.

HP_DEFECT_PIXEL_CTRL

HP_DEFECT_PIXEL_CTRL is a defect pixel module control register.

Offset Address	Register Name	Total Reset Value
0x01E8	HP_DEFECT_PIXEL_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											DetectionTrigger	ShowStaticDefect_Pixels	Enable	ShowReference	PointerReset
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RW	reserved	Reserved.
[4]	RW	DetectionTrigger	Start detection on 0-1 transition.
[3]	RW	ShowStaticDefect_Pixels	Show the pixels that have been detected as defect pixels.
[2]	RW	Enable	Correction enable. 0: off 1: on
[1]	RW	ShowReference	Show reference values that are compared with actual values to detect defect pixels.
[0]	RW	PointerReset	Reset defect-pixel table pointer each frame. This field is set when the defect-pixel table has been written from the MCU.

HP_COUNT

HP_COUNT is a defect pixel count register for the defect pixel module.

Offset Address	Register Name	Total Reset Value
0x01EC	HP_COUNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						DefectPixelCount									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved.

Offset Address	Register Name	Total Reset Value
0x01EC	HP_COUNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						DefectPixelCount									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[9:0]	RO	DefectPixelCount	Number of defect pixels detected.

HP_TABLE_START

HP_TABLE_START is a defect pixel start address register for the defect pixel module.

Offset Address	Register Name	Total Reset Value
0x01F0	HP_TABLE_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						TableStart									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved.
[9:0]	RO	TableStart	Address of the first defect pixel in stored defect pixels.

HP_COUNT_IN

HP_COUNT_IN is a written defect pixel count register for the defect pixel module.

Offset Address	Register Name	Total Reset Value
0x01F4	HP_COUNT_IN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						DefectPixelCountIn									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RW	reserved	Reserved.
[9:0]	RW	DefectPixelCountIn	Number of defect pixels in the written table.

HP_TABLE_LUT_ADDR

HP_TABLE_LUT_ADDR is a lookup table (LUT) address register for the defect pixel module.

Offset Address	Register Name	Total Reset Value
0x0850	HP_TABLE_LUT_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						TableLUTAddr									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RW	reserved	Reserved.
[9:0]	RW	TableLUTAddr	LUT address register (valid range 0 to 1023)

HP_TABLE_LUT_WRITE_DATA

HP_TABLE_LUT_WRITE_DATA is an LUT write data register for the defect pixel module.

Offset Address	Register Name	Total Reset Value
0x0854	HP_TABLE_LUT_WRITE_DATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												TableLUTWriteData																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RW	reserved	Reserved.
[21:0]	RW	TableLUTWriteData	LUT write data register.

HP_TABLE_LUT_READ_DATA

HP_TABLE_LUT_READ_DATA is an LUT read data register for the defect pixel module.

Offset Address	Register Name	Total Reset Value
0x0858	HP_TABLE_LUT_READ_DATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												TableLUTReadData																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved.
[21:0]	RO	TableLUTReadData	LUT read data register.

DNR_CTRL1

DNR_CTRL1 is DNR module control register 1.

Offset Address	Register Name	Total Reset Value
0x0200	DNR_CTRL1	0x0000_0411

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rmcenterx																reserved				intconfig				rmenable	Intselect	Filterselect	Enable	Rsvd			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1

Bits	Access	Name	Description
[31:16]	RW	rmcenterx	Horizontal coordinates of the shading map.
[15:12]	RW	reserved	Reserved.
[11:8]	RW	intconfig	Intensity blending with mosaic raw.
[7]	RW	rmenable	Lens shading correction enable. 0: off 1: on
[6]	RW	Intselect	Intensity filter select.
[5]	RW	Filterselect	Denoise filter fine tuning.
[4]	RW	Enable	Denoise enable. 0: off 1: on
[3:0]	RW	Rsvd	Reserved.

DNR_CTRL2

DNR_CTRL2 is DNR module control register 2.

Offset Address	Register Name	Total Reset Value
0x0204	DNR_CTRL2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rmoffcentermult																rmcentery															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	rmoffcentermult	Normalizing factor for sum of squares.
[15:0]	RW	rmcentery	Vertical coordinates of the shading map.

DNR_CTRL3

DNR_CTRL3 is DNR module control register 3.

Offset Address	Register Name	Total Reset Value
0x0208	DNR_CTRL3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																Thresh1h								Thresh0h							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:8]	RW	Thresh1h	Noise threshold for the horizontal green-only filter.
[7:0]	RW	Thresh0h	Noise threshold for high horizontal spatial frequencies.

DNR_THRESH_2H

DNR_THRESH_2H is a horizontal intermediate-frequency noise threshold register for the DNR module.

Offset Address	Register Name	Total Reset Value
0x020C	DNR_THRESH_2H	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								Thresh2h							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.
[7:0]	RW	Thresh2h	Noise threshold for medium horizontal spatial frequencies.

DNR_THRESH_4H

DNR_THRESH_4H is a horizontal low-frequency noise threshold register for the DNR module.

Offset Address	Register Name	Total Reset Value
0x0210	DNR_THRESH_4H	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								Thresh4h							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.
[7:0]	RW	Thresh4h	Noise threshold for low horizontal spatial frequencies.

DNR_THRESH_0V

DNR_THRESH_0V is a vertical high-frequency noise threshold register for the DNR module.

Offset Address	Register Name	Total Reset Value
0x0214	DNR_THRESH_0V	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								Thresh0v							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.
[7:0]	RW	Thresh0v	Noise threshold for high vertical spatial frequencies.

DNR_THRESH_1V

DNR_THRESH_1V is a vertical green noise threshold register for the DNR module.

Offset Address	Register Name	Total Reset Value
0x0218	DNR_THRESH_1V	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								Thresh1v							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.
[7:0]	RW	Thresh1v	Noise threshold for the vertical green-only filter.

DNR_THRESH_2V

DNR_THRESH_2V is a vertical intermediate-frequency noise threshold for the DNR module.

Offset Address	Register Name	Total Reset Value
0x021C	DNR_THRESH_2V	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								Thresh2v							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.
[7:0]	RW	Thresh2v	Noise threshold for medium vertical spatial frequencies.

DNR_THRESH_4V

DNR_THRESH_4V is a vertical low-frequency noise threshold for the DNR module.

Offset Address	Register Name	Total Reset Value
0x0220	DNR_THRESH_4V	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								Thresh4v							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.

Offset Address	Register Name	Total Reset Value
0x0220	DNR_THRESH_4V	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								Thresh4v							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	Thresh4v	Noise threshold for low vertical spatial frequencies.

DNR_THRESH_SHORT

DNR_THRESH_SHORT is a short exposure noise threshold register for the DNR module.

Offset Address	Register Name	Total Reset Value
0x0224	DNR_THRESH_SHORT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ThreshShort							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.
[7:0]	RW	ThreshShort	Noise threshold adjustment for short exposure data.

DNR_THRESH_LONG

DNR_THRESH_LONG is a long exposure noise threshold register for the DNR module.

Offset Address	Register Name	Total Reset Value
0x0228	DNR_THRESH_LONG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ThreshLong							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.
[7:0]	RW	ThreshLong	Noise threshold adjustment for long exposure data.

DNR_STRENGTH0

DNR_STRENGTH0 is a high-frequency component denoise strength register for the DNR module.

Offset Address	Register Name	Total Reset Value
0x022C	DNR_STRENGTH0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								Strength0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.
[7:0]	RW	Strength0	Noise reduction effect for high spatial frequencies.

DNR_STRENGTH1

DNR_STRENGTH1 is a green component denoise strength register for the DNR module.

Offset Address	Register Name	Total Reset Value
0x0230	DNR_STRENGTH1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								Strength1							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.
[7:0]	RW	Strength1	Noise reduction effect for the green-only filter.

DNR_STRENGTH2

DNR_STRENGTH2 is an intermediate-frequency denoise strength register for the DNR module.

Offset Address	Register Name	Total Reset Value
0x0234	DNR_STRENGTH2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								Strength2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.
[7:0]	RW	Strength2	Noise reduction effect for medium spatial frequencies.

DNR_STRENGTH4

DNR_STRENGTH4 is a low-frequency denoise strength register for the DNR module.

Offset Address	Register Name	Total Reset Value
0x0238	DNR_STRENGTH4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								Strength4							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.
[7:0]	RW	Strength4	Noise reduction effect for low spatial frequencies.

RADIAL_LUT1

RADIAL_LUT1 is radial LUT 1 register for the DNR module.

Offset Address	Register Name	Total Reset Value
0x0970	RADIAL_LUT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rmshadinglut_3_								rmshadinglut_2_								rmshadinglut_1_								rmshadinglut_0_							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	rmshadinglut_3_	Radial LUT.
[23:16]	RW	rmshadinglut_2_	Radial LUT.
[15:8]	0x0	rmshadinglut_1_	Radial LUT.

Offset Address	Register Name	Total Reset Value
0x0970	RADIAL_LUT1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	rmshadinglut_3_		rmshadinglut_2_		rmshadinglut_1_		rmshadinglut_0_	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[7:0]	RW	rmshadinglut_0_	Radial LUT.

RADIAL_LUT2

RADIAL_LUT2 radial LUT 2 register for the DNR module.

Offset Address	Register Name	Total Reset Value
0x0974	RADIAL_LUT2	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	rmshADinglut_7_		rmshadinglut_6_		rmshadinglut_5_		rmshadinglut_4_	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	rmshADinglut_7_	Radial LUT.
[23:16]	RW	rmshadinglut_6_	Radial LUT.
[15:8]	0x0	rmshadinglut_5_	Radial LUT.
[7:0]	0x0	rmshadinglut_4_	Radial LUT.

RADIAL_LUT3

RADIAL_LUT3 radial LUT 3 register for the DNR module.

Offset Address	Register Name	Total Reset Value
0x098C	RADIAL_LUT3	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	rmshadinglut_31_		rmshadinglut_30_		rmshadinglut_29_		rmshadinglut_28_	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	rmshadinglut_31_	Radial LUT.
[23:16]	RW	rmshadinglut_30_	Radial LUT.

Offset Address	Register Name	Total Reset Value
0x098C	RADIAL_LUT3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rmshadinglut_31_								rmshadinglut_30_								rmshadinglut_29_								rmshadinglut_28_							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:8]	0x0	rmshadinglut_29_	Radial LUT.
[7:0]	RW	rmshadinglut_28_	Radial LUT.

RADIAL_LUT4

RADIAL_LUT4 radial LUT 4 register for the DNR module.

Offset Address	Register Name	Total Reset Value
0x0990	RADIAL_LUT4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								rmshadinglut_32_							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.
[7:0]	RW	rmshadinglut_32_	Radial LUT.

DNR_NOISE_PROFILE_LUT1

DNR_NOISE_PROFILE_LUT1 is a noise profile LUT write data register for the DNR module.

Offset Address	Register Name	Total Reset Value
0x0780	DNR_NOISE_PROFILE_LUT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Weightlut_3_								Weightlut_2_								Weightlut_1_								Weightlut_0_							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	Weightlut_3_	Noise profile LUT.
[23:16]	0x0	Weightlut_2_	Noise profile LUT.
[15:8]	RW	Weightlut_1_	Noise profile LUT.

Offset Address	Register Name	Total Reset Value
0x0780	DNR_NOISE_PROFILE_LUT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Weightlut_3_								Weightlut_2_								Weightlut_1_								Weightlut_0_							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	Weightlut_0_	Noise profile LUT.

DNR_NOISE_PROFILE_LUT2

DNR_NOISE_PROFILE_LUT2 is a noise profile LUT write data register for the DNR module.

Offset Address	Register Name	Total Reset Value
0x0784	DNR_NOISE_PROFILE_LUT2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Weightlut_7_								Weightlut_6_								Weightlut_5_								Weightlut_4_							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	Weightlut_7_	Noise profile LUT.
[23:16]	0x0	Weightlut_6_	Noise profile LUT.
[15:8]	RW	Weightlut_5_	Noise profile LUT.
[7:0]	RW	Weightlut_4_	Noise profile LUT.

DNR_NOISE_PROFILE_LUTn

DNR_NOISE_PROFILE_LUTn is a noise profile LUT write data register for the DNR module.

Offset Address	Register Name	Total Reset Value
0x07FC	DNR_NOISE_PROFILE_LUTn	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Weightlut_127_								Weightlut_126_								Weightlut_125_								Weightlut_124_							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	Weightlut_127_	Noise profile LUT.

Offset Address	Register Name	Total Reset Value
0x07FC	DNR_NOISE_PROFILE_LUTn	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Weightlut_127_								Weightlut_126_								Weightlut_125_								Weightlut_124_							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[23:16]	RW	Weightlut_126_	Noise profile LUT.
[15:8]	0x0	Weightlut_125_	Noise profile LUT.
[7:0]	RW	Weightlut_124_	Noise profile LUT.

DNR_EXP_THRESH

DNR_EXP_THRESH is a long/short exposure threshold register for the DNR module.

Offset Address	Register Name	Total Reset Value
0x0270	DNR_EXP_THRESH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ExpThresh															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:0]	RW	ExpThresh	Threshold for determining long/short exposure data.

DNR_RATIO_SHORT

DNR_RATIO_SHORT is a short exposure noise profile LUT multiplier register for the DNR module.

Offset Address	Register Name	Total Reset Value
0x0274	DNR_RATIO_SHORT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ShortRatio							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.

Offset Address	Register Name	Total Reset Value
0x0274	DNR_RATIO_SHORT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ShortRatio							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	ShortRatio	Multiplier that applies to short exposure data for noise profile calculation. Format: unsigned 6.2-bit fixed-point

DNR_RATIO_LONG

DNR_RATIO_LONG is a long exposure noise profile LUT multiplier register for the DNR module.

Offset Address	Register Name	Total Reset Value
0x0278	DNR_RATIO_LONG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								LongRatio							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.
[7:0]	RW	LongRatio	Multiplier that applies to long exposure data for noise profile calculation. Format: unsigned 6.2-bit fixed-point

WB_GAIN00

WB_GAIN00 is an R component gain register for the white balance module.

Offset Address	Register Name	Total Reset Value
0x02C0	WB_GAIN00	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				Gain00											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved.

Offset Address	Register Name	Total Reset Value
0x02C0	WB_GAIN00	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				Gain00											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[11:0]	RW	Gain00	Multiplier for color channel 00 (R). Format: unsigned 4.8-bit fixed-point

WB_GAIN01

WB_GAIN01 is a Gr component gain register for the white balance module.

Offset Address	Register Name	Total Reset Value
0x02C4	WB_GAIN01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				Gain01											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved.
[11:0]	RW	Gain01	Multiplier for color channel 01 (Gr). Format: unsigned 4.8-bit fixed-point

WB_GAIN10

WB_GAIN10 is a Gb component gain register for the white balance module.

Offset Address	Register Name	Total Reset Value
0x02C8	WB_GAIN10	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				Gain10											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved.
[11:0]	RW	Gain10	Multiplier for color channel 10 (Gb). Format: unsigned 4.8-bit fixed-point

WB_GAIN11

WB_GAIN11 is a B component gain register for the white balance module.

Offset Address	Register Name	Total Reset Value
0x02CC	WB_GAIN11	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				Gain11											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved.
[11:0]	RW	Gain11	Multiplier for color channel 11 (B). Format: unsigned 4.8-bit fixed-point

WB_BLACK00

WB_BLACK00 is an R component black level register for the white balance module.

Offset Address	Register Name	Total Reset Value
0x02D0	WB_BLACK00	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																Black00															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:0]	RW	Black00	Black offset for color channel 00(R).

WB_BLACK01

WB_BLACK01 is a Gr component black level register for the white balance module.

Offset Address	Register Name	Total Reset Value
0x02D4	WB_BLACK01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																Black01															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:0]	RW	Black01	Black offset for color channel 01 (Gr).

WB_BLACK10

WB_BLACK10 is a Gb component black level register for the white balance module.

Offset Address	Register Name	Total Reset Value
0x02D8	WB_BLACK10	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																Black10															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:0]	RW	Black10	Black offset for color channel 10 (Gb).

WB_BLACK11

WB_BLACK11 is a B component black level register for the white balance module.

Offset Address	Register Name	Total Reset Value
0x02DC	WB_BLACK11	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																Black11															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:0]	RW	Black11	Black offset for color channel 11 (B).

SHADING_CTRL

SHADING_CTRL is a lens shading module control module.

Offset Address	Register Name	Total Reset Value
0x0300	SHADING_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															Enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RW	reserved	Reserved.
[0]	RW	Enable	Lens shading correction enable. 0: off 1: on

SHADING_RX

SHADING_RX is an R component center horizontal coordinate register for the lens shading module.

Offset Address	Register Name	Total Reset Value
0x0304	SHADING_RX	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																centerRx															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:0]	RW	centerRx	Rx coordinates of the shading map.

SHADING_RY

SHADING_RY is an R component center vertical coordinate register for the lens shading module.

Offset Address	Register Name	Total Reset Value
0x0308	SHADING_RY	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																centerRy															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:0]	RW	centerRy	Ry coordinates of the shading map.

SHADING_GX

SHADING_GX is a G component center horizontal coordinate register for the lens shading module.

Offset Address	Register Name	Total Reset Value
0x030C	SHADING_GX	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																centerGx															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:0]	RW	centerGx	Gx coordinates of the shading map.

SHADING_GY

SHADING_GY is a G component center vertical coordinate register for the lens shading module.

Offset Address	Register Name	Total Reset Value
0x0310	SHADING_GY	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																centerGy															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:0]	RW	centerGy	Gy coordinates of the shading map.

SHADING_BX

SHADING_BX is a B component center horizontal coordinate register for the lens shading module.

Offset Address	Register Name	Total Reset Value
0x0314	SHADING_BX	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																centerBx															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:0]	RW	centerBx	Bx coordinates of the shading map.

SHADING_BY

SHADING_BY is a B component center vertical coordinate register for the lens shading module.

Offset Address	Register Name	Total Reset Value
0x0318	SHADING_BY	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																centerBy															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:0]	RW	centerBy	By coordinates of the shading map.

SHADING_MULTR

SHADING_MULTR is an R component shading factor for the lens shading module.

Offset Address	Register Name	Total Reset Value
0x031C	SHADING_MULTR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																offcentermultR															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:0]	RW	offcentermultR	Normalizing factor for sum of squares.

SHADING_MULTG

SHADING_MULTG is a G component shading factor for the lens shading module.

Offset Address	Register Name	Total Reset Value
0x0320	SHADING_MULTG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																offcentermultG															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:0]	RW	offcentermultG	Normalizing factor for sum of squares.es

SHADING_MULTB

SHADING_MULTB is a B component shading factor for the lens shading module.

Offset Address	Register Name	Total Reset Value
0x0324	SHADING_MULTB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																offcentermultB															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:0]	RW	offcentermultB	Normalizing factor for sum of squares.

DRC_ENABLE

DRC_ENABLE is a DRC enable register.

Offset Address	Register Name	Total Reset Value
0x0380	DRC_ENABLE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															Enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RW	reserved	Reserved.
[0]	RW	Enable	DRC enable. 0: off 1: on

DRC_STRENGTH

DRC_STRENGTH is a DRC strength register.

Offset Address	Register Name	Total Reset Value
0x0384	DRC_STRENGTH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								Strength							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.
[7:0]	RW	Strength	Strength of dynamic range compression. When other parameters are default values, increase the visibility of shadows.

DRC_CTRL

DRC_CTRL is a DRC module control register.

Offset Address	Register Name	Total Reset Value
0x0388	DRC_CTRL	0x0000_0010

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		slopemin		slopemax		varianceintensity	VarianceSpace
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	reserved	Reserved.
[23:16]	RW	slopemin	Restrict the minimum slope (gain) that can be generated by the adaptive algorithm.
[15:8]	RW	slopemax	Restrict the maximum slope (gain) which can be generated by the adaptive algorithm.
[7:4]	RW	varianceintensity	Degree of luminance sensitivity of the algorithm.
[3:0]	RW	VarianceSpace	Degree of spatial sensitivity of the algorithm.

DRC_LOOKUP1_ENABLE

DRC_LOOKUP1_ENABLE is a DRC LUT1 enable register.

Offset Address	Register Name	Total Reset Value
0x03C8	DRC_LOOKUP1_ENABLE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2	1	0
Name	reserved								RevPerceptEnable	reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0	0

Bits	Access	Name	Description
[31:2]	RW	reserved	Reserved.
[1]	RW	RevPerceptEnable	DRC look-up 1 enable. 0: off 1: on
[0]	RW	reserved	Reserved.

DRC_LUT1_ADDR

DRC_LOOKUP1_ENABLE is a DRC LUT1 address register.

Offset Address	Register Name	Total Reset Value
0x0820	DRC_LUT1_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								revperceptlutaddr							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	RW	reserved	Reserved.
[6:0]	RW	revperceptlutaddr	LUT address register (valid range 0 to 64).

DRC_LUT1_DATA

DRC_LOOKUP1_ENABLE is a DRC LUT1 data register.

Offset Address	Register Name	Total Reset Value
0x0824	DRC_LUT1_DATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RevPerceptLUTWriteData																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	RevPerceptLUTWriteData	LUT write data register.

DRC_LOOKUP2_ENABLE

DRC_LOOKUP1_ENABLE is a DRC LUT2 enable register.

Offset Address	Register Name	Total Reset Value
0x03E8	DRC_LOOKUP2_ENABLE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2	1	0
Name	reserved								FwdPerceptEnable	reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0	0

Bits	Access	Name	Description
[31:2]	RW	reserved	Reserved.
[1]	RW	FwdPerceptEnable	DRC look-up 2 enable. 0: off 1: on
[0]	RW	reserved	Reserved.

DRC_LUT2_ADDR

DRC_LOOKUP1_ENABLE is a DRC LUT2 address register.

Offset Address	Register Name	Total Reset Value
0x0830	DRC_LUT2_ADDR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							FwdPerceptLUTAddr
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:7]	RW	reserved	Reserved.
[6:0]	RW	FwdPerceptLUTAddr	LUT address register (valid range 0 to 64).

DRC_LUT2_DATA

DRC_LOOKUP1_ENABLE is a DRC LUT2 data register.

Offset Address	Register Name	Total Reset Value
0x0834	DRC_LUT2_DATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				FwdPerceptLUTWriteData											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved.
[11:0]	RW	FwdPerceptLUTWriteData	LUT write data register.

DEMOSAIC_VH_SLOPE

DEMOSAIC_VH_SLOPE is a maximum vertical/horizontal slope register for the demosaic module.

Offset Address	Register Name	Total Reset Value
0x0400	DEMOSAIC_VH_SLOPE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								VHSlope							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.
[7:0]	RW	VHSlope	Slope of vertical/horizontal blending threshold in 4.4 logarithmic format.

DEMOSAIC_AA_SLOPE

DEMOSAIC_AA_SLOPE is an AA slope register.

Offset Address	Register Name	Total Reset Value
0x0404	DEMOSAIC_AA_SLOPE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								AASlope							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.

Offset Address	Register Name	Total Reset Value
0x0404	DEMOSAIC_AA_SLOPE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								AASlope							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	AASlope	Slope of angular blending threshold in 4.4 logarithmic format.

DEMOSAIC_VA_SLOPE

DEMOSAIC_VA_SLOPE is a VA slope register.

Offset Address	Register Name	Total Reset Value
0x0408	DEMOSAIC_VA_SLOPE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								VASlope							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.
[7:0]	RW	VASlope	Slope of VH-AA (VA) blending threshold in 4.4 logarithmic format.

DEMOSAIC_UU_SLOPE

DEMOSAIC_UU_SLOPE is a UU slope register.

Offset Address	Register Name	Total Reset Value
0x040C	DEMOSAIC_UU_SLOPE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								UUSlope							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.
[7:0]	RW	UUSlope	Slope of undefined blending threshold in 4.4 logarithmic format.

DEMOSAIC_SAT_SLOPE

DEMOSAIC_SAT_SLOPE is an SAT slope register.

Offset Address	Register Name	Total Reset Value
0x0410	DEMOSAIC_SAT_SLOPE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								SatSlope							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.
[7:0]	RW	SatSlope	Slope of saturation blending threshold in linear format 2.6.

DEMOSAIC_VH_THRESH

DEMOSAIC_VH_THRESH is a VH threshold register.

Offset Address	Register Name	Total Reset Value
0x0414	DEMOSAIC_VH_THRESH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				VHThresh											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved.
[11:0]	RW	VHThresh	Threshold for the range of vertical/horizontal blending in 0.12 format.

DEMOSAIC_AA_THRESH

DEMOSAIC_AA_THRESH is an AA threshold register.

Offset Address	Register Name	Total Reset Value
0x0418	DEMOSAIC_AA_THRESH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				AAThresh											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved.
[11:0]	RW	AAThresh	Threshold for the range of angular blending in 0.12 format.

DEMOSAIC_VA_THRESH

DEMOSAIC_VA_THRESH is a VA threshold register.

Offset Address	Register Name	Total Reset Value
0x041C	DEMOSAIC_VA_THRESH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				VAThresh											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved.
[11:0]	RW	VAThresh	Threshold for the range of VA blending in 0.12 format.

DEMOSAIC_UU_THRESH

DEMOSAIC_UU_THRESH is a UU threshold register.

Offset Address	Register Name	Total Reset Value
0x0420	DEMOSAIC_UU_THRESH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				UUThresh											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved.
[11:0]	RW	UUThresh	Threshold for the range of undefined blending in 0.12 format.

DEMOSAIC_SAT_THRESH

DEMOSAIC_AA_OFFSET is an AA threshold register.

Offset Address	Register Name	Total Reset Value
0x0424	DEMOSAIC_SAT_THRESH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				SatThresh											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved.
[11:0]	RW	SatThresh	Threshold for the range of saturation blending in signed 2.9 format.

DEMOSAIC_VH_OFFSET

DEMOSAIC_VH_OFFSET is a vertical/horizontal offset register for the demosaic module.

Offset Address	Register Name	Total Reset Value
0x0428	DEMOSAIC_VH_OFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				VHOffset											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved.
[11:0]	RW	VHOffset	Offset for vertical/horizontal blending threshold in 0.12 format.

DEMOSAIC_AA_OFFSET

DEMOSAIC_AA_OFFSET is an AA offset register.

Offset Address	Register Name	Total Reset Value
0x042C	DEMOSAIC_AA_OFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				AAOffset											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved.
[11:0]	RW	AAOffset	Offset for angular blending threshold in 0.12 format.

DEMOSAIC_VA_OFFSET

DEMOSAIC_VA_OFFSET is a VA offset register.

Offset Address	Register Name	Total Reset Value
0x0430	DEMOSAIC_VA_OFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				VAOffset											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved.
[11:0]	RW	VAOffset	Offset for VA blending threshold in 0.12 format.

DEMOSAIC_UU_OFFSET

DEMOSAIC_UU_OFFSET is a UU offset register.

Offset Address	Register Name	Total Reset Value
0x0434	DEMOSAIC_UU_OFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				UUOffset											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved.
[11:0]	RW	UUOffset	Offset for undefined blending threshold in 0.12 format.

DEMOSAIC_SAT_OFFSET

DEMOSAIC_SAT_OFFSET is an SAT offset register.

Offset Address	Register Name	Total Reset Value
0x0438	DEMOSAIC_SAT_OFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				SatOffset											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved.
[11:0]	RW	SatOffset	Offset for saturation blending threshold in signed 2.9 format.

DEMOSAIC_SHARP_ALT_D

DEMOSAIC_SHARP_ALT_D is an edge sharpen strength register.

Offset Address	Register Name	Total Reset Value
0x043C	DEMOSAIC_SHARP_ALT_D	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								sharpaltd							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.
[7:0]	RW	sharpaltd	Directional sharp mask strength in signed 4.4 format.

DEMOSAIC_SHARP_ALT_UD

DEMOSAIC_SHARP_ALT_UD is a flat area sharpen strength register.

Offset Address	Register Name	Total Reset Value
0x0440	DEMOSAIC_SHARP_ALT_UD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								sharpaltud							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.

Offset Address	Register Name	Total Reset Value
0x0440	DEMOSAIC_SHARP_ALT_UD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								sharpaltud							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	sharpaltud	Non-directional sharp mask strength in signed 4.4 format.

DEMOSAIC_LUM_THRESH

DEMOSAIC_LUM_THRESH is an LUM threshold register.

Offset Address	Register Name	Total Reset Value
0x0444	DEMOSAIC_LUM_THRESH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				lumthresh											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved.
[11:0]	RW	lumthresh	Luminance threshold for directional sharpening.

DEMOSAIC_NP_OFFSET

DEMOSAIC_NP_OFFSET is an NP offset register.

Offset Address	Register Name	Total Reset Value
0x0448	DEMOSAIC_NP_OFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								npoffset							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.
[7:0]	RW	npoffset	Noise profile offset in logarithmic 4.4 format.

DEMOSAIC_AC_THRESH

DEMOSAIC_AC_THRESH is an AC threshold register.

Offset Address	Register Name	Total Reset Value
0x0450	DEMOSAIC_AC_THRESH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				ACThresh											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved.
[11:0]	RW	ACThresh	Threshold for the range of AC blending in signed 2.9 format.

DEMOSAIC_AC_SLOPE

DEMOSAIC_AC_SLOPE is an AC slope register.

Offset Address	Register Name	Total Reset Value
0x0454	DEMOSAIC_AC_SLOPE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ACSlope							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.
[7:0]	RW	ACSlope	Slope of AC blending threshold in linear 2.6 format.

DEMOSAIC_AC_OFFSET

DEMOSAIC_AC_OFFSET is an AC offset register.

Offset Address	Register Name	Total Reset Value
0x0458	DEMOSAIC_AC_OFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				ACOffset											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved.

Offset Address	Register Name	Total Reset Value
0x0458	DEMOSAIC_AC_OFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				ACOffset											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[11:0]	RW	ACOffset	Offset for AC blending threshold in signed 2.9 format.

DEMOSAIC_FC_SLPOE

DEMOSAIC_FC_SLPOE is an anti-false color strength register.

Offset Address	Register Name	Total Reset Value
0x045C	DEMOSAIC_FC_SLPOE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								FCSlope							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.
[7:0]	RW	FCSlope	Slope (strength) of false color correction.

NP_LUT_WEIGHT1

NP_LUT_WEIGHT1 is noise profile LUT weight 1 register.

Offset Address	Register Name	Total Reset Value
0x0C00	NP_LUT_WEIGHT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Weightlut_3_								Weightlut_2_								Weightlut_1_								Weightlut_0_							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	Weightlut_3_	Noise profile LUT.
[23:16]	RW	Weightlut_2_	Noise profile LUT.
[15:8]	0x0	Weightlut_1_	Noise profile LUT.
[7:0]	RW	Weightlut_0_	Noise profile LUT.

NP_LUT_WEIGHT2

NP_LUT_WEIGHT2 is noise profile LUT weight 2 register.

Offset Address	Register Name	Total Reset Value
0x0C04	NP_LUT_WEIGHT2	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	Weightlut_7_		Weightlut_6_		Weightlut_5_		Weightlut_4_	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	Weightlut_7_	Noise profile LUT.
[23:16]	0x0	Weightlut_6_	Noise profile LUT.
[15:8]	RW	Weightlut_5_	Noise profile LUT.
[7:0]	RW	Weightlut_4_	Noise profile LUT.

NP_LUT_WEIGHTn

NP_LUT_WEIGHTn is noise profile LUT weight n register.

Offset Address	Register Name	Total Reset Value
0x0C7C	NP_LUT_WEIGHTn	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	Weightlut_127_		Weightlut_126_		Weightlut_125_		Weightlut_124_	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	Weightlut_127_	Noise profile LUT.
[23:16]	RW	Weightlut_126_	Noise profile LUT.
[15:8]	RW	Weightlut_125_	Noise profile LUT.
[7:0]	RW	Weightlut_124_	Noise profile LUT.

CCM_CTRL

CCM_CTRL is a color matrix module control register.

Offset Address	Register Name	Total Reset Value
0x04A4	CCM_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															Enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RW	reserved	Reserved.
[0]	RW	Enable	Color matrix enable. 0: off 1: on

CCM_COEFFT_RR

CCM_COEFFT_RR is an RR position coefficient register for the color matrix module.

Offset Address	Register Name	Total Reset Value
0x0480	CCM_COEFFT_RR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																CoefftR_R															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:0]	RW	CoefftR_R	Matrix coefficient for red-red multiplier. Format: sign/magnitude 8.8-bit fixed-point

CCM_COEFFT_RG

CCM_COEFFT_RG is an RG position coefficient register for the color matrix module.

Offset Address	Register Name	Total Reset Value
0x0484	CCM_COEFFT_RG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																CoefftR_G															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:0]	RW	CoefftR_G	Matrix coefficient for red-green multiplier. Format: sign/magnitude 8.8-bit fixed-point

CCM_COEFFT_RB

CCM_COEFFT_RB is an RB position coefficient register for the color matrix module.

Offset Address	Register Name	Total Reset Value
0x0488	CCM_COEFFT_RB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																CoefftR_B															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:0]	RW	CoefftR_B	Matrix coefficient for red-blue multiplier. Format: sign/magnitude 8.8-bit fixed-point

CCM_COEFFT_GR

CCM_COEFFT_GR is a GR position coefficient register for the color matrix module.

Offset Address	Register Name	Total Reset Value
0x048C	CCM_COEFFT_GR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																CoefftG_R															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.

Offset Address	Register Name	Total Reset Value
0x048C	CCM_COEFFT_GR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																CoefftG_R															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:0]	RW	CoefftG_R	Matrix coefficient for green-red multiplier. Format: sign/magnitude 8.8-bit fixed-point

CCM_COEFFT_GG

CCM_COEFFT_GG is a GG position coefficient register for the color matrix module.

Offset Address	Register Name	Total Reset Value
0x0490	CCM_COEFFT_GG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																CoefftG_G															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:0]	RW	CoefftG_G	Matrix coefficient for green-green multiplier. Format: sign/magnitude 8.8-bit fixed-point

CCM_COEFFT_GB

CCM_COEFFT_GB is a GB position coefficient register for the color matrix module.

Offset Address	Register Name	Total Reset Value
0x0494	CCM_COEFFT_GB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																CoefftG_B															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:0]	RW	CoefftG_B	Matrix coefficient for green-blue multiplier. Format: sign/magnitude 8.8-bit fixed-point

CCM_COEFFT_BR

CCM_COEFFT_BR is a BR position coefficient register for the color matrix module.

Offset Address	Register Name	Total Reset Value
0x0498	CCM_COEFFT_BR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																CoefftB_R															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:0]	RW	CoefftB_R	Matrix coefficient for blue-red multiplier. Format: sign/magnitude 8.8-bit fixed-point

CCM_COEFFT_BG

CCM_COEFFT_BG is a BG position coefficient register for the color matrix module.

Offset Address	Register Name	Total Reset Value
0x049C	CCM_COEFFT_BG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																CoefftB_G															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:0]	RW	CoefftB_G	Matrix coefficient for blue-green multiplier. Format: sign/magnitude 8.8-bit fixed-point

CCM_COEFFT_BB

CCM_COEFFT_BB is a BB position coefficient register for the color matrix module.

Offset Address	Register Name	Total Reset Value
0x04A0	CCM_COEFFT_BB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																CoefftB_B															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:0]	RW	CoefftB_B	Matrix coefficient for blue-blue multiplier. Format: sign/magnitude 8.8-bit fixed-point

CCM_COEFFT_WBR

CCM_COEFFT_WBR is an R component white balance gain register for the color matrix module.

Offset Address	Register Name	Total Reset Value
0x04A8	CCM_COEFFT_WBR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																CoefftWBR															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:0]	RW	CoefftWBR	White balance gain for red. Format: sign/magnitude 8.8-bit fixed-point

CCM_COEFFT_WBG

CCM_COEFFT_WBG is a G component white balance gain register for the color matrix module.

Offset Address	Register Name	Total Reset Value
0x04AC	CCM_COEFFT_WBG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																CoefftWBG															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:0]	RW	CoefftWBG	White balance gain for green. Format: sign/magnitude 8.8-bit fixed-point

CCM_COEFFT_WBB

CCM_COEFFT_WBB is a B component white balance gain register for the color matrix module.

Offset Address	Register Name	Total Reset Value
0x04B0	CCM_COEFFT_WBB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																CoefftWBB															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:0]	RW	CoefftWBB	White balance gain for blue. Format: sign/magnitude 8.8-bit fixed-point

METERING_HIST_THRESH01

METERING_HIST_THRESH01 is segment 0 and segment 1 boundary point register for histogram statistics.

Offset Address	Register Name	Total Reset Value
0x0600	METERING_HIST_THRESH01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								HistThresh01							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.
[7:0]	RW	HistThresh01	Histogram threshold for bin 0/1 boundary.

METERING_HIST_THRESH12

METERING_HIST_THRESH12 is segment 1 and segment 2 boundary point register for histogram statistics.

Offset Address	Register Name	Total Reset Value
0x0604	METERING_HIST_THRESH12	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								HistThresh12							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.
[7:0]	RW	HistThresh12	Histogram threshold for bin 1/2 boundary.

METERING_HIST_THRESH34

METERING_HIST_THRESH34 is segment 3 and segment 4 boundary point register for histogram statistics.

Offset Address	Register Name	Total Reset Value
0x0608	METERING_HIST_THRESH34	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								HistThresh34							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.
[7:0]	RW	HistThresh34	Histogram threshold for bin 2/3 boundary.

METERING_HIST_THRESH45

METERING_HIST_THRESH45 is segment 4 and segment 5 boundary point register for histogram statistics.

Offset Address	Register Name	Total Reset Value
0x060C	METERING_HIST_THRESH45	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								HistThresh45							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.
[7:0]	RW	HistThresh45	Histogram threshold for bin 3/4 boundary.

METERING_HIST0

METERING_HIST0 is histogram statistics register for segment 0.

Offset Address	Register Name	Total Reset Value
0x0620	METERING_HIST0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																Hist0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RO	Hist0	Normalized histogram results for bin 0.

METERING_HIST1

METERING_HIST1 is histogram statistics register for segment 1.

Offset Address	Register Name	Total Reset Value
0x0624	METERING_HIST1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																Hist1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RO	Hist1	Normalized histogram results for bin 1.

METERING_HIST3

METERING_HIST3 is histogram statistics register for segment 3.

Offset Address	Register Name	Total Reset Value
0x0628	METERING_HIST3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																Hist3															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RO	Hist3	Normalized histogram results for bin 3.

METERING_HIST4

METERING_HIST4 is histogram statistics register for segment 4.

Offset Address	Register Name	Total Reset Value
0x062C	METERING_HIST4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																Hist4															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RO	Hist4	Normalized histogram results for bin 4.

AE_NODES_USED

AE_NODES_USED is an AE active region register.

Offset Address	Register Name	Total Reset Value
0x0630	AE_NODES_USED	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																AEXPNodesUsedVert								AEXPNodesUsedHoriz							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:8]	RW	AEXPNodesUsedVert	Number of vertical active zones.
[7:0]	RW	AEXPNodesUsedHoriz	Number of horizontal active zones.

METERING_AWB_WHITE_LEVEL

METERING_AWB_WHITE_LEVEL is an AWB brightest point register.

Offset Address	Register Name	Total Reset Value
0x0640	METERING_AWB_WHITE_LEVEL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						WhiteLevelAWB									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RW	reserved	Reserved.
[9:0]	RW	WhiteLevelAWB	Upper limit of valid data for AWB.

METERING_AWB_BLACK_LEVEL

METERING_AWB_BLACK_LEVEL is an AWB darkest point register.

Offset Address	Register Name	Total Reset Value
0x0644	METERING_AWB_BLACK_LEVEL	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved					BlackLevelAWB		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved.
[11:0]	RW	BlackLevelAWB	Lower limit of valid data for AWB.

METERING_AWB_CR_REF_MAX

METERING_AWB_CR_REF_MAX is the maximum Cr value register for the AWB reference white point.

Offset Address	Register Name	Total Reset Value
0x0648	METERING_AWB_CR_REF_MAX	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved					CrRefMaxAWB		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved.
[11:0]	RW	CrRefMaxAWB	Maximum value of R/G for white region. Format: unsigned 4.8-bit fixed-point

METERING_AWB_CR_REF_MIN

METERING_AWB_CR_REF_MIN is the minimum Cr value register for the AWB reference white point.

Offset Address	Register Name	Total Reset Value
0x064C	METERING_AWB_CR_REF_MIN	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved					CrRefMinAWB		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved.

Offset Address	Register Name	Total Reset Value
0x064C	METERING_AWB_CR_REF_MIN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				CrRefMinAWB											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[11:0]	RW	CrRefMinAWB	Minimum value of R/G for white region. Format: unsigned 4.8-bit fixed-point

METERING_AWB_CB_REF_MAX

METERING_AWB_CB_REF_MAX is the maximum Cb value register for the AWB reference white point.

Offset Address	Register Name	Total Reset Value
0x0650	METERING_AWB_CB_REF_MAX	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				CbRefMaxAWB											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved.
[11:0]	RW	CbRefMaxAWB	Maximum value of B/G for white region. Format: unsigned 4.8-bit fixed-point

METERING_AWB_CB_REF_MIN

METERING_AWB_CB_REF_MIN is the minimum Cb value register for the AWB reference white point.

Offset Address	Register Name	Total Reset Value
0x0654	METERING_AWB_CB_REF_MIN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				CbRefMinAWB											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved.

Offset Address	Register Name	Total Reset Value
0x0654	METERING_AWB_CB_REF_MIN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				CbRefMinAWB											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[11:0]	RW	CbRefMinAWB	Minimum value of B/G for white region. Format: unsigned 4.8-bit fixed-point

METERING_AWB_RG

METERING_AWB_RG is an AWB output G/R register.

Offset Address	Register Name	Total Reset Value
0x0658	METERING_AWB_RG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				AWBRG											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RO	AWBRG	AWB output R/G. Format: unsigned 4.8-bit fixed-point

METERING_AWB_BG

METERING_AWB_BG is an AWB output G/B register.

Offset Address	Register Name	Total Reset Value
0x065C	METERING_AWB_BG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				AWBBG											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved.
[11:0]	RO	AWBBG	AWB output B/G. Format: unsigned 4.8-bit fixed-point

METERING_AWB_SUM

METERING_AWB_SUM is an AWB reference white point count register.

Offset Address	Register Name	Total Reset Value
0x0660	METERING_AWB_SUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AWBSUM																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	AWBSUM	Format: unsigned 4.8-bit fixed-point

AWB_NODES_USED

AWB_NODES_USED is an AWB active region register.

Offset Address	Register Name	Total Reset Value
0x0670	AWB_NODES_USED	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																AWBNodesUsedVert								AWBNodesUsedHoriz							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.
[15:8]	RW	AWBNodesUsedVert	Number of vertical active zones.
[7:0]	RW	AWBNodesUsedHoriz	Number of horizontal active zones.

AF_METRICS_SHIFT

AF_METRICS_SHIFT is an AF metric conversion register.

Offset Address	Register Name	Total Reset Value
0x068C	AF_METRICS_SHIFT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												AFmetricsshift			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RW	reserved	Reserved.
[3:0]	RW	AFmetricsshift	Metrics scaling factor. The default value is 0x03. Format: unsigned 4-bit integer

METERING_AF_METRICS

METERING_AF_METRICS is an AF metric statistics register.

Offset Address	Register Name	Total Reset Value
0x0680	METERING_AF_METRICS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																AFmetrics															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RO	AFmetrics	Integrated and normalized measure of contrast. Format: unsigned 16-bit integer

METERING_AF_THRESHOLD_WRITE

METERING_AF_THRESHOLD_WRITE is a preset AF threshold register.

Offset Address	Register Name	Total Reset Value
0x0684	METERING_AF_THRESHOLD_WRITE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																AFthresholdwrite															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.

Offset Address	Register Name	Total Reset Value
0x0684	METERING_AF_THRESHOLD_WRITE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																AFthresholdwrite																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:0]	RW	AFthresholdwrite	Recommended value of AF threshold (or 0 to use threshold from previous frame). Format: unsigned 16-bit integer

METERING_AF_THRESHOLD_READ

METERING_AF_THRESHOLD_READ is an updated AF threshold register.

Offset Address	Register Name	Total Reset Value
0x0688	METERING_AF_THRESHOLD_READ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFintensityread																AFthresholdread															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	AFintensityread	Calculated value of AF intensity. Format: unsigned 16-bit integer
[15:0]	RO	AFthresholdread	Calculated value of AF threshold. Format: unsigned 16-bit integer

AF_NODES_USED

AF_NODES_USED is an AF active region register.

Offset Address	Register Name	Total Reset Value
0x0690	AF_NODES_USED	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																AFNodesUsedVert								AFNodesUsedHoriz							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved.

Offset Address	Register Name	Total Reset Value
0x0690	AF_NODES_USED	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																AFNodesUsedVert								AFNodesUsedHoriz							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:8]	RW	AFNodesUsedVert	Number of vertical active zones.
[7:0]	RW	AFNodesUsedHoriz	Number of horizontal active zones.

AF_NP_OFFSET

AF_NP_OFFSET is an AF noise profile offset register.

Offset Address	Register Name	Total Reset Value
0x0694	AF_NP_OFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								AFNPoffset							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.
[7:0]	RW	AFNPoffset	AF noise profile offset. Format: unsigned 4.4-bit fixed-point

HISTOGRAM_CTRL

HISTOGRAM_CTRL is a histogram control register.

Offset Address	Register Name	Total Reset Value
0x06C0	HISTOGRAM_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										offsety	offsetx	skipy		skipx			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RW	reserved	Reserved.
[5]	RW	offsety	0: start from the first row 1: start from the second row
[4]	RW	offsetx	0: start from the first column 1: start from the second column
[3:2]	RW	skipy	Histogram decimation in vertical direction. 00: every pixel 01: every the second pixel 10: every the fourth pixel 11: every the eighth pixel
[1:0]	RW	skipx	Histogram decimation in horizontal direction. 00: every the second pixel 01: every the fourth pixel 10: every the eighth pixel 11: every the sixteenth pixel

SCALE_CTRL

SCALE_CTRL is a scale control register.

Offset Address	Register Name	Total Reset Value
0x06C4	SCALE_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								scaletop				scalebottom			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved.

Offset Address	Register Name	Total Reset Value
0x06C4	SCALE_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								scaletop				scalebottom			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:4]	RW	scaletop	Scale of top half of the range. 000: 1x 001: 2x 010: 4x 011: 8x 100: 16x Other values: reserved
[3:0]	RW	scalebottom	Scale of bottom half of the range. 000: 1x 001: 2x 010: 4x 011: 8x 100: 16x Other values: reserved

TOTAL_PIXELS

TOTAL_PIXELS is a total pixel number register.

Offset Address	Register Name	Total Reset Value
0x06C8	TOTAL_PIXELS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TotalPixels																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	TotalPixels	Total number of pixels processed (skip x and skip y are taken into account).

COUNTED_PIXEL

COUNTED_PIXEL is an involved pixel count register for statistics.

Offset Address	Register Name	Total Reset Value
0x06CC	COUNTED_PIXEL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CountedPixels																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	CountedPixels	Number of pixels accumulated (with non-zero weight).

HISTOGRAM_DATA_SHIFT

HISTOGRAM_DATA_SHIFT is a global statistical data offset register.

Offset Address	Register Name	Total Reset Value
0x06D0	HISTOGRAM_DATA_SHIFT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														Histogramdatashift	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2:0]	RO	Histogramdatashift	Data shift for the histogram.

METERING_AWB_WEIGHT

METERING_AWB_WEIGHT is an AWB window weight register.

Offset Address	Register Name	Total Reset Value
0x0B00	METERING_AWB_WEIGHT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				AWBWeight_0_3_				reserved				AWBWeight_0_2_				reserved				AWBWeight_0_1_				reserved				AWBWeight_0_0_			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	reserved	Reserved.
[27:24]	RW	AWBWeight_0_3_	Sets zone weighting for AWB.
[23:20]	0x0	reserved	Reserved.
[19:16]	0x0	AWBWeight_0_2_	Sets zone weighting for AWB.
[15:12]	0x0	reserved	Reserved.
[11:8]	0x0	AWBWeight_0_1_	Sets zone weighting for AWB.
[7:4]	0x0	reserved	Reserved.
[3:0]	RW	AWBWeight_0_0_	Sets zone weighting for AWB.

GAMMA_STATUS

GAMMA_CTRL is a gamma module status register.

Offset Address	Register Name	Total Reset Value
0x04C0	GAMMA_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													MCUready	MCUpriority	Enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2]	RO	MCUready	LUT is ready to receive the data from the CPU.
[1]	0x0	MCUpriority	Priority of CPU port. 0: low 1: high

Offset Address	Register Name	Total Reset Value
0x04C0	GAMMA_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													MCUready	MCUpriority	Enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RO	Enable	Gamma enable. 0: off 1: on

DIS_CTRL

DIS_CTRL is a DIS module control register.

Offset Address	Register Name	Total Reset Value
0x0700	DIS_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ManualOffsetX								reserved						Shiftmux		reserved					rsvd		manualcontrol
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	reserved	Reserved.
[23:16]	RW	ManualOffsetX	Manual X offset control.
[15:10]	RW	reserved	Reserved.
[9:8]	RW	Shiftmux	Scaling factor for the internal accumulators. 00: There is no shift. 01: Internal results are multiplied by 4. 10: Internal results are multiplied by 16. 11: Internal results are multiplied by 64.

Offset Address	Register Name	Total Reset Value
0x0700	DIS_CTRL	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10	9 8	7 6 5 4	3 2	1	0
Name	reserved		ManualOffsetX		reserved		Shiftmux	reserved	rsvd		manualcontrol
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0 0	0 0 0 0	0 0	0	0

Bits	Access	Name	Description
[7:3]	RW	reserved	Reserved.
[2:1]	RW	rsvd	Reserved.
[0]	RW	manualcontrol	DIS and manual output offset enable.

DIS_OFFSET_X

DIS_OFFSET_X is horizontal offset register for the DIS module.

Offset Address	Register Name	Total Reset Value
0x0704	DIS_OFFSET_X	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10	9 8	7 6 5 4	3 2	1	0
Name	reserved		OffsetX		reserved			ManualOffsetY			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0 0	0 0 0 0	0 0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:16]	RO	OffsetX	Calculated X offset.
[15:8]	0x0	reserved	Reserved.
[7:0]	RO	ManualOffsetY	Manual Y offset control.

DIS_OFFSET_Y

DIS_OFFSET_Y is a vertical offset register for the DIS module.

Offset Address	Register Name	Total Reset Value
0x0708	DIS_OFFSET_Y	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								Corrruntimes								reserved								OffsetY							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	reserved	Reserved.
[23:16]	RW	Corrruntimes	Multiplier for correlation block size to obtain correlation range in +-8 increments.
[15:8]	RW	reserved	Reserved.
[7:0]	RW	OffsetY	Calculated Y offset.

Contents

Figures

Tables

12 Audio Interfaces

12.1 SIO

12.1.1 Overview

The sonic input/output (SIO) interfaces are used to connect to the internal audio CODEC to play and record music clips (voices). The Hi3518 provides one SIO interface and supports the input and output of voice talkback.

12.1.2 Features

The SIO interfaces support I^2S mode. I^2S interfaces are used to work with the audio CODEC to implement talkback and record audio clips. The SIO interfaces also support directory memory access (DMA) operations.

I²S Interfaces

The I^2S interfaces have the following features:

- Transmit or receive the left-/right-channel 16-/18-/20-/24-/32-bit data.
- Support the sampling rate ranging from 8 kHz to 192 kHz.
- Each I^2S TX channel or I^2S RX channel has its independent FIFO. The left channel and the right channel also have their independent FIFOs. The FIFO is 16-location deep and the FIFO threshold can be adjusted.
- Support the function of enabling the TX channel and the RX channel independently.
- In 16-bit transfer mode, the data received by the left and right channels can be combined into 32-bit data and then stored in the receive FIFO, and the data transmitted by the left and right channels can be combined into 32-bit data and then written to the transmit FIFO. This improves the buffer performance of FIFOs.

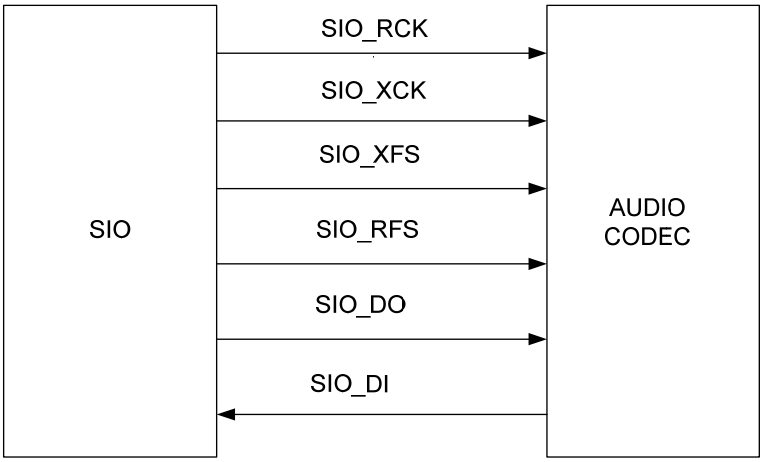
12.1.3 Function Description

Typical Application

SIO is used to input or output audios to implement talkback. The following describes the typical connections of the I^2S interface.

Figure 12-1 shows the typical connections of the I^2S interface.

Figure 12-1 Connection diagram of the I²S interface in master mode



The SIO transmits the bit stream clock and audio channel select signal to the audio CODEC.

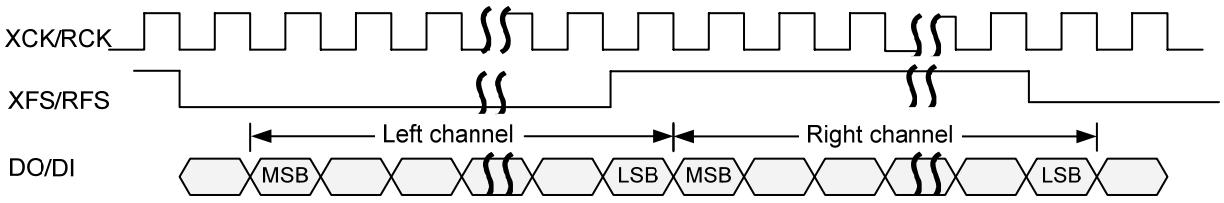
Function Principle

An SIO interface receives the audio data transmitted over the internal bus, and transmits the audio data to the interconnected audio CODEC over the I²S interface at a specified sampling rate. After that, the audio CODEC performs digital-to-analog (DA) conversion on the audio data and plays the audio. At the same time, the SIO interface receives the audio data after analog-to-digital (AD) conversion performed by the audio CODEC through the I²S interface, and stores the data into the internal FIFO. Then, the CPU fetches the data and stores it. In this way, the audio recording function is complete.

The data transferred through the I²S interface consists of the right-channel data and the left-channel data, which are distinguished from the levels of the XFS (RFS) signal, as shown in Figure 12-2. Data is sampled on the rising edge of the XCK/RCK clock according to the protocol. The MSB is valid in next clock cycle of XFS/RFS. The MSB and LSB are transferred in sequence.

Figure 12-2 shows the timing of the I²S interface.

Figure 12-2 Timing of the I²S interface



12.1.4 Operating Mode

Clock Gating

When no audio is being recorded or played, you can configure PERI_CRG35 to disable the SIO clocks after SIO_CT_SET [rx_enable] and SIO_CT_SET [tx_enable] are set to 0. The details are as follows: Write 0 to PERI_CRG35 [sio0_cken] to disable the SIO0 clock.

You can enable the SIO clocks by setting the related registers to 1. That is, write 1 to PERI_CRG35 [sio0_cken] to enable the SIO0 clock.

Clock Configuration

When SIO0 works, select the frequency dividers of the bit stream clock and sync clock by configuring PERI_CRG35 [sio0_bclk_div] and PERI_CRG35 [sio0_fsclk_div] respectively.

Soft Reset

Soft-reset SIO0 by setting PERI_CRG35 [sio0_srst_req] to 1. After reset, each configuration register is restored to its default value. Therefore, these registers must be reinitialized.

Audio Playing and Recording in Interrupt mode or Query Mode

Initialization

The initialization is implemented as follows:

Step 1 Set SIO_CT_SET/SIO_CT_CLR[rx_enable] and SIO_CT_SET/SIO_CT_CLR[tx_enable] to 0 to disable the SIO.

Step 2 Select the I^2S mode by setting SIO_MODE[sio_mode].

Step 3 Configure the clock frequency.

Step 4 Set the bit width by configuring SIO_DATA_WIDTH_SET and SIO_SIGNED_EXT.

Step 5 Set the thresholds of the RX FIFO and TX FIFO by configuring SIO_CT_SET[rx_fifo_threshold] and SIO_CT_SET [tx_fifo_threshold] respectively.

Step 6 Configure SIO_I^2S_POS_MERGE_EN and SIO_I^2S_START_POS based on the modes of reading and writing the FIFO, and configure SIO_CT_SET[tx_data_merge_en] and SIO_CT_SET[rx_data_merge_en].

Step 7 Set the SIO interrupt mask register SIO_INTMASK and SIO_CT_SET[intr_en] as required.

Step 8 Configure the internal audio CODECs.

----End

Audio Playing

To play audio clips, do as follows:

Step 1 Set SIO_CT_SET [tx_fifo_disable] to 1 and then to 0 to clear the remaining data in the TX FIFO.

Step 2 Write the data to be transmitted to the TX FIFO, and write 1 to SIO_CT_SET[tx_enable] to start data transmission.

Step 3 In query mode, check the status of TX FIFO by reading SIO_TX_STA; in interrupt mode, report an interrupt according to the interrupt status indicated by SIO_INTSTATUS[tx_intr]. When the data depth of the TX FIFO is below the threshold, write data to the TX FIFO. When data is transmitted completely, go to step 4. Ensure that data underflow does not occur in the TX FIFO before data is transmitted completely. Otherwise, the sound may be discontinuous.

Step 4 Set SIO_CT_SET [tx_enable] to 0.

----End

Audio Recording

To record audio clips, do as follows:

Step 1 Set SIO_CT_SET[rx_fifo_disable] to 1 and then to 0 to clear the remaining data in the RX_FIFO.

Step 2 Set SIO_CT_SET[rx_enable] to 1 to start data reception.

Step 3 In query mode, check the status of the RX FIFO by reading SIO_RX_STA; in interrupt mode, check the status of the RX FIFO by reading the related interrupt status bit. When the data depth of the RX FIFO is above the threshold, read data from the RX FIFO. When data is received completely, go to step 4. Ensure that data overflow does not occur in the RX FIFO before data is received completely. Otherwise, data loss occurs.

Step 4 Set SIO_CT_SET[rx_enable] to 0 to read all the remaining data in the RX FIFO.

----End

Audio Playing and Recording in DMA Mode

Initialization

The audio playing and recording in DMA mode is performed in the same way as that in interrupt mode or query mode.

Audio Playing

To play audio clips, perform the following steps:

Step 1 Set SIO_INTMASK[tx_intr] to 1 to mask transmit interrupts.

Step 2 Configure the DMA data channel, including the data transfer source address, destination address, amount of data to be transferred, and transfer type. For details, see the configuration description of DMA.

Step 3 Set SIO_CT_SET [tx_fifo_disable] to 1 and then to 0 to clear the remaining data in the TX FIFO.

Step 4 Write the initial data to the TX FIFO to ensure that the data depth is above the FIFO threshold. You can write the all-0s data, which indicates mute. If no initial data is written to the FIFO, the SIO reports FIFO underflow because the DMA does not write data to the FIFO when audio playing is started. If the initial data is written to the FIFO, the FIFO underflow upon the start of the audio playing can be prevented.

Step 5 Set SIO_CT_SET[tx_enable] to 1 to start audio playing.

Step 6 Check whether the data is transmitted completely according to the DMA interrupt. If the data is transmitted completely, set SIO_CT_SET[tx_enable] to 0.

----End

Audio Recording

To record audio clips, perform the following steps:

Step 1 Configure the DMA data channel, including the data transfer source, destination address, amount of data to be transferred, and transfer type. For details, see the configuration description of DMA.

Step 2 Set SIO_CT_SET[rx_fifo_disable] to 1 and then to 0 to clear the remaining data in the RX FIFO.

Step 3 Set SIO_CT_SET[rx_enable] to 1 to start data reception.

Step 4 If you want to stop audio recording, set SIO_CT_SET[rx_enable] to 0.

----End

12.1.5 Register Summary

The base address for SIO registers is 0x1004_0000.Figure 12-1 describes the SIO registers.

Table 12-1 Summary of SIO registers

Offset address	Register	Description	Page
0x03C	SIO_VERSION	SIO version register	12-6
0x040	SIO_MODE	SIO mode register	12-7
0x044	SIO_INTSTATUS	SIO interrupt status register	12-8
0x048	SIO_INTCLR	SIO interrupt clear register	12-9
0x04C	SIO_I^{2}S_LEFT_XD	I^{2}S left channel data transmit register	12-10
0x050	SIO_I^{2}S_RIGHT_XD	I^{2}S right channel data transmit register	12-11
0x054	SIO_I^{2}S_LEFT_RD	I^{2}S left channel data receive register	12-11
0x058	SIO_I^{2}S_RIGHT_RD	I^{2}S right channel data receive register	12-12
0x05C	SIO_CT_SET	I^{2}S control set register	12-12
0x060	SIO_CT_CLR	I^{2}S control clear register	12-14
0x064	RESERVED	Reserved	-
0x068	SIO_RX_STA	SIO receive status register	12-16
0x06C	SIO_TX_STA	SIO transmit status register	12-17
0x070–0x074	RESERVED	Reserved	-

Offset address	Register	Description	Page
0x078	SIO_DATA_WIDTH_SET	I^2S data width configuration register	12-17
0x07C	SIO_I^2S_START_POS	Data access start position control register of I^2S left and right channels	12-18
0x080	I^2S_POS_FLAG	Current position status register of I^2S left and right channels	12-19
0x084	SIO_SIGNED_EXT	Upper-bit sign extend enable register	12-20
0x088	SIO_I^2S_POS_MERGE_EN	Access position merging enable of I^2S left and right channels	12-20
0x08C	SIO_INTMASK	SIO interrupt mask register	12-21
0x090–0x09C	RESERVED	Reserved	-
0x0A0	SIO_I^2S_DUAL_RX_CHN	Data receive register after enabling of I^2S left and right channel data access position merging	12-22
0x0C0	SIO_I^2S_DUAL_TX_CHN	Data transmit register after enabling of I^2S left and right channel data access position merging	12-22

12.1.6 Register Description

SIO_VERSION

SIO_VERSION is an SIO version register. It is used to record the SIO version number and perform the SIO self-test.

offset Address	Register Name	Total Reset Value
0x03C	SIO_VERSION	0x0000_0013

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							sio_loop	version							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1

Bits	Access	Name	Description
[31:9]	-	reserved	Reserved.

[8]	RW	sio_loop	SIO loop or normal mode select. 0: normal mode 1: Data transmit and receive loop mode. It is used for the self-test of the SIO. In the mode, the SIO receive serial data line is directly connected to the SIO transmit serial data line at the external interface of the SIO.
[7:0]	RO	version	Version number of the SIO.

SIO_MODE

SIO_MODE is an SIO mode register. It is used to select the basic operating mode of the SIO as follows:

- In master mode, the clock reset generator (CRG) transmits clocks and sync signals to the CODEC and SIO.
- In slave mode, the external CODEC transmits clocks and sync signals to the SIO.

For details about the master/slave mode selection of the I^2S, see "Clock Configuration" in section 12.1.4 "Operating Mode."

offset Address	Register Name	Total Reset Value
0x040	SIO_MODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										chn_num		ext_rec_en	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	-	reserved	Reserved.
[5:4]	RW	chn_num	Number of channels during multi-channel data receive. 00: 2 channels 01: 4 channels 10: 8 channels 11: 16 channels
[3]	RW	ext_rec_en	In standard data receive mode, the I^2S interface receives both the left-channel and right-channel data. For the I^2S interface in multi-channel data receive mode, the number of channels is configurable. Additionally, the bit width of the channels must be 8 bits or 16 bits. 0: standard data receive mode of the I^2S interface 1: extended multi-channel data receive mode of the I^2S interface
[2:0]	RW	reserved	Reserved. This bit must be set to 0.

SIO_INTSTATUS

SIO_INTSTATUS is an SIO interrupt status register.

Take the receive interrupt as an example. When the data depth of the RX FIFO is above the threshold, the high level is always latched to the interrupt status register and the interrupts are generated continuously. That is, even if the CPU clears the interrupt, the interrupt status register is set to 1 in the next clock cycle. Therefore, the following processing mode of the CPU is recommended:

Step 1 Write 1 to SIO_CT_CLR[intr_en] to disable the global interrupt enable bit.

Step 2 Read the interrupt status register SIO_INTSTATUS.

Step 3 Perform related operations according to the interrupt source.

Step 4 Write 1 to the related bit of SIO_INTCLR to clear the interrupt.

Step 5 Write 1 to SIO_CT_SET[intr_en] to enable the global interrupt enable bit.

----End

The transmit interrupt and receive interrupt are generated in the same way. Therefore, it is recommended that the transmit interrupt is processed in the similar way.

This register is a raw interrupt status register. If the related interrupt bit is masked and the interrupt condition is met, the related interrupt status bit is set to 1 and no interrupt is triggered.

Offset Address	Register Name	Total Reset Value
0x044	SIO_INTSTATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										tx_left_fifo_under	tx_right_fifo_under	rx_left_fifo_over	rx_right_fifo_over	tx_intr	rx_intr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	-	reserved	Reserved.
[5]	RO	tx_left_fifo_under	In I^{2}S mode, this bit indicates the left channel TX FIFO underflow interrupt status. 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RO	tx_right_fifo_under	In I^{2}S mode, this bit indicates the right channel TX FIFO underflow interrupt status. 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RO	rx_left_fifo_over	In I^{2}S mode, this bit indicates the left channel RX FIFO overflow interrupt status. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	rx_right_fifo_over	In I^{2}S mode, this bit indicates the right channel RX FIFO overflow interrupt status. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	tx_intr	Interrupt status when the TX FIFO is below the threshold. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	rx_intr	Interrupt status when the RX FIFO is above the threshold. 0: No interrupt is generated. 1: An interrupt is generated.

SIO_INTCLR

SIO_INTCLR is an SIO interrupt clear register. It can be cleared by bits.

Offset Address	Register Name	Total Reset Value
0x048	SIO_INTCLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										tx_left_fifo_under	tx_right_fifo_under	rx_left_fifo_over	rx_right_fifo_over	tx_intr	rx_intr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	-	reserved	Reserved.
[5]	WO	tx_left_fifo_under	In I^{2}S mode, this bit indicates left channel TX FIFO underflow interrupt clear. 0: not cleared 1: cleared
[4]	WO	tx_right_fifo_under	In I^{2}S mode, this bit indicates right channel TX FIFO underflow interrupt clear. 0: not cleared 1: cleared
[3]	WO	rx_left_fifo_over	In I^{2}S mode, it indicates left channel RX FIFO overflow interrupt clear. 0: not cleared 1: cleared
[2]	WO	rx_right_fifo_over	In I^{2}S mode, this bit indicates right channel RX FIFO overflow interrupt clear. 0: not cleared 1: cleared
[1]	WO	tx_intr	Interrupt clear when the TX FIFO is below the threshold. 0: not cleared 1: cleared
[0]	WO	rx_intr	Interrupt clear when the RX FIFO is above the threshold. 0: not cleared 1: cleared

SIO_I²S_LEFT_XD

SIO_I^{2}S_LEFT_XD is an I^{2}S left channel data transmit register.

The SIO module places the valid data in the lower-bit area when writing data to the register. For example, when the data width is 8 bits, bit[7:0] are valid and bit[31:8] are invalid; when

the data width is 16 bits, bit[15:0] are valid and bit[31:16] are invalid. The bits beyond the valid data width are automatically set to 0 by the SIO module.

offset Address	Register Name	Total Reset Value
0x04C	SIO_I²S_LEFT_XD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_left_data																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	tx_left_data	Left channel transmit data.

SIO_I²S_RIGHT_XD

SIO_I²S_LEFT_XD is an I²S right channel data transmit register.

The SIO module places the valid data in the lower-bit area when writing data to the register. For example, when the data width is 8 bits, bit[7:0] are valid and bit[31:8] are invalid; when the data width is 16 bits, bit[15:0] are valid and bit[31:16] are invalid. The bits beyond the valid data width are automatically set to 0 by the SIO module.

Offset Address	Register Name	Total Reset Value
0x050	SIO_I²S_RIGHT_XD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_right_data																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	tx_right_data	Right channel transmit data.

SIO_I²S_LEFT_RD

SIO_I²S_LEFT_RD is an I²S left channel data receive register.

The SIO module places the received valid data in the low-bit area of the register. For example, when the data width is 8 bits, bit[7:0] are valid and bit[31:8] are invalid; when the data width is 16 bits, bit[15:0] are valid and bit[31:16] are invalid. The bits beyond the valid data width are automatically set to 0 by the SIO module.

Offset Address	Register Name	Total Reset Value
0x054	SIO_I²S_LEFT_RD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	rx_left_data
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	rx_left_data	I²S left channel receive data.

NOTE

When data reception is disabled in I²S mode, the right-channel data may not be written to the FIFO. In this case, the left-channel FIFO has one data segment more than the right-channel FIFO. Therefore, the data in the left-channel and right-channel FIFOs must be cleared before the CPU starts the next data reception.

SIO_I²S_RIGHT_RD

SIO_I²S_RIGHT_RD is an I²S right channel data receive register.

The SIO module places the received valid data in the low-bit area of the register. For example, when the data width is 8 bits, bit[7:0] are valid and bit[31:8] are invalid; when the data width is 16 bits, bit[15:0] are valid and bit[31:16] are invalid. The bits beyond the valid data width are automatically set to 0 by the SIO module.

Offset Address	Register Name	Total Reset Value
0x058	SIO_I²S_RIGHT_RD	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	rx_right_data
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	rx_right_data	I²S right channel receive data.

NOTE

When data reception is disabled in I²S mode, the right-channel data may not be written to the FIFO. In this case, the left-channel FIFO has one data segment more than the right-channel FIFO. Therefore, the data in the left-channel and right-channel FIFOs must be cleared before the CPU starts the next data reception.

SIO_CT_SET

To operate the SIO control register by bits, the SIO_CT_SET register with the address 0x05C is provided. When 1 is written to the related bit of the register, the bit is set to 1. Writing 0 has no effect. This is a read/write register.

Offset Address	Register Name	Total Reset Value
0x05C/0x060	SIO_CT_SET	0x0000_8000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Name	reserved	rst_n	intr_en	rx_enable	tx_enable	rx_fifo_disable	tx_fifo_disable	rx_data_merge_en	tx_data_merge_en	rx_fifo_threshold	tx_fifo_threshold
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1	0	0	0	0	0	0	0	0 0 0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15]	RW	rst_n	I^2S channel reset, active low. This bit is used to reset the transmit and receive modules (including the FIFOs) in I^2S mode. Therefore, the RX FIFO and TX FIFO status registers are changed to 0. This bit does not reset the CPU interface register module.
[14]	RW	intr_en	Global interrupt enable. 0: disabled 1: enabled
[13]	RW	rx_enable	RX channel enable. 0: disabled 1: enabled
[12]	RW	tx_enable	TX channel enable. 0: disabled 1: enabled
[11]	RW	rx_fifo_disable	RX FIFO disable. 0: enabled 1: disabled
[10]	RW	tx_fifo_disable	TX FIFO disable. 0: enabled 1: disabled

[9]	RW	rx_data_merge_en	Data receive merging enable. This bit is valid only when the data width is 16 bits in I^2S mode. 0: disabled 1: enabled If this bit is 1, the left-channel and right-channel data is merged into a 32-bit data and then is stored in the FIFO. The left-channel 16 bits occupy the 16 MSBs, and the right-channel 16 bits occupy the 16 LSBs. Therefore, the usage and buffer capacity of the FIFO is improved. The CPU reads data from the RX_FIFO in the following order. That is, reads the 32-bit data (formed by merging the16-bit left-channel data and 16-bit right-channel data) from the left-channel FIFO, and then reads the 32-bit data from the right-channel FIFO. The CPU reads data in this manner repeatedly.
[8]	RW	tx_data_merge_en	Data transmit merging enable. It is valid only when the data bit width is 16 bits in I^2S mode. 0: disabled 1: enabled If this bit is 1, the left-channel and right-channel data is merged into a 32-bit data and then is stored in the FIFO. The left-channel 16 bits occupy the 16 MSBs, and the right-channel 16 bits occupy the 16 LSBs. Therefore, the usage and buffer capacity of the FIFO is improved. The CPU writes data into the TX_FIFO in the following order. That is, writes the 32-bit data (formed by merging the16-bit left-channel data and 16-bit right-channel data) to the left-channel FIFO, and then writes the 32-bit data to the right-channel FIFO. The CPU writes data in this manner repeatedly.
[7:4]	RW	rx_fifo_threshold	RX_FIFO threshold. When rx_right_depth ≥ (rx_fifo_threshold + 1), the receive interrupt and DMA request are reported.
[3:0]	RW	tx_fifo_threshold	TX_FIFO threshold. When the tx_right_depth < (tx_fifo_threshold + 1), the transmit interrupt and DMA request are reported.

SIO_CT_CLR

To facilitate the bit operation on the SIO control register, the SIO_CT_CLR register with the address of 0x06 is provided. When 1 is written to the related bit of the register, the bit is set to 1. Writing 0 has no effect. This is a write-only register.

Offset Address	Register Name	Total Reset Value
0x05C/0x060	SIO_CT_SET	0x0000_8000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rst_n	intr_en	rx_enable	tx_enable	rx_fifo_disable	tx_fifo_disable	rx_data_merge_en	tx_data_merge_en	rx_fifo_threshold				tx_fifo_threshold			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15]	RW	rst_n	I^2S channel reset, active low. This bit is used to reset the transmit and receive modules (including the FIFOs) in I^2S mode. Therefore, the RX_FIFO and TX_FIFO status registers are changed to 0. This bit does not reset the CPU interface register module.
[14]	RW	intr_en	Global interrupt enable. 0: disabled 1: enabled
[13]	RW	rx_enable	RX channel enable. 0: disabled 1: enabled
[12]	RW	tx_enable	TX channel enable. 0: disabled 1: enabled
[11]	RW	rx_fifo_disable	RX FIFO enable. 0: enabled 1: disabled
[10]	RW	tx_fifo_disable	TX FIFO disable. 0: enabled 1: disabled

[9]	RW	rx_data_merge_en	Data receive merging enable. This bit is valid only when the data width is 16 bits in I^2S mode. 0: disabled 1: enabled If this bit is 1, the left-channel and right-channel data is merged into a 32-bit data and then is stored in the FIFO. The left-channel 16 bits occupy the upper 16 bits, and the right-channel 16 bits occupy the lower16 bits. Therefore, the usage and buffer capacity of the FIFO is improved. The CPU reads data from the RX FIFO in the following sequence. That is, the 32-bit data (formed by merging the16-bit left-channel data and 16-bit right-channel data) from the left-channel FIFO and the 32-bit data from the right-channel FIFO are read in sequence. The CPU reads data in this manner repeatedly.
[8]	RW	tx_data_merge_en	Data transmit merging enable. It is valid only when the data bit width is 16 bits in I^2S mode. 0: disabled 1: enabled If this bit is 1, the left-channel and right-channel data is merged into a 32-bit data and then is stored in the FIFO. The left-channel 16 bits occupy the upper 16 bits, and the right-channel 16 bits occupy the lower 16 bits. Therefore, the usage and buffer capacity of the FIFO is improved. The CPU writes data into the TX_FIFO in the following sequence. That is, the 32-bit data (formed by merging the16-bit left-channel data and 16-bit right-channel data) is written to the left-channel FIFO, and then the 32-bit data is written to the right-channel FIFO. The CPU writes data in this manner repeatedly.
[7:4]	RW	rx_fifo_threshold	RX FIFO threshold. When the following condition is met, the receive interrupt and DMA request are reported: rx_right_depth ≥ (rx_fifo_threshold + 1)
[3:0]	RW	tx_fifo_threshold	TX FIFO threshold. When the following condition is met, the transmit interrupt and DMA request are reported: tx_right_depth < (tx_fifo_threshold + 1)

SIO_RX_STA

SIO_RX_STA is an SIO receive status register.

Offset Address	Register Name	Total Reset Value
0x068	SIO_RX_STA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						rx_left_depth					rx_right_depth					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	-	reserved	Reserved.
[9:5]	RO	rx_left_depth	Left channel RX FIFO depth indicator. These bits are valid only in I^{2}S mode.
[4:0]	RO	rx_right_depth	In I^{2}S mode, it indicates the right channel RX FIFO depth indicator.

SIO_TX_STA

SIO_TX_STA is an SIO transmit status register.

Offset Address	Register Name	Total Reset Value
0x06C	SIO_TX_STA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						tx_left_depth					tx_right_depth					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved.
[9:5]	RO	tx_left_depth	Left channel TX FIFO depth indicator. These bits are valid only in I^{2}S mode.
[4:0]	RO	tx_right_depth	In I^{2}S mode, it indicates the right channel TX FIFO depth indicator.

SIO_DATA_WIDTH_SET

SIO_DATA_WIDTH_SET is an I^{2}S data width configuration register.

Offset Address	Register Name	Total Reset Value

0x078	SIO_DATA_WIDTH_SET	0x0000_0009

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								reserved		rx_mode			tx_mode		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

Bits	Access	Name	Description
[31:6]	-	reserved	Reserved.
[5:3]	RW	rx_mode	Length of the data to be received. 000: 8 bits 001: 16 bits 010: 18 bits 011: 20 bits 100: 24 bits. 101: 32 bits. 110–111: reserved The data length of 16 bits, 18 bits, 20 bits, 24 bits, or 32 bits is supported in I^2S mode. For multi-channel data reception, only the data length of 8 bits or 16 bits is supported in I^2S mode.
[2:0]	RW	tx_mode	Length of the data to be transmitted. For the I^2S mode: 000: reserved 001: 16 bits 010: 18 bits 011: 20 bits 100: 24 bits. 101: 32 bits. 110–111: reserved

SIO_I²S_START_POS

SIO_I^2S_START_POS is a start operation position control register of I^2S left and right channels.

This register controls whether the initial access starts from the left channel or right channel after the left-channel and right-channel data access address merging is enabled.

Offset Address	Register Name	Total Reset Value
0x07C	SIO_I^2S_START_POS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	reserved	start_pos_write	start_pos_read
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		

Bits	Access	Name	Description
[31:2]	-	reserved	Reserved.
[1]	RW	start_pos_write	When writing data to the TX FIFO: 0: Start the access from the left channel. 1: Start the access from the right channel.
[0]	RW	start_pos_read	When reading data from the RX FIFO: 0: Start the access from the left channel. 1: Start the access from the right channel.

I²S_POS_FLAG

I²S_POS_FLAG is a current operation position status register of I²S left and right channels.

This register controls whether the subsequent access starts from the left channel or the right channel after the left-channel and right-channel data access address merging is enabled.

Offset Address	Register Name	Total Reset Value
0x080	I²S_POS_FLAG	0x0000_0000

Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Name	reserved | start_pos_write | start_pos_read
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:2]	-	reserved	Reserved.
[1]	RO	start_pos_write	When writing data into the TX FIFO: 0: Start the subsequent access from the left channel. 1: Start the subsequent access from the right channel.
[0]	RO	start_pos_read	When reading data from the RX FIFO: 0: Start the subsequent access from the left channel. 1: Start the subsequent access from the right channel.

SIO_SIGNED_EXT

SIO_SIGNED_EXT is an upper-bit sign extend enable register. This upper-bit sign extend enable bit is valid only for the received data rather than the transmitted data. The sign extension function is supported by the received data in I²S mode.

Assume that the received valid data width is 8 bits, 16 bits, 18 bits, 20 bits, or 24 bits and the upper-bit sign extend enable bit is enabled. When the receive data is converted into 32-bit data, the invalid upper bit of the 32 bits are set to the value corresponding to the MSB of the received data and then written to the RX FIFO.

The following example is based on the data width of 16 bits:

```
if (data_rx[15] == 1)
data_rx[31:16] = 0xffff;
else
data_rx[31:16] = 0x0000;
```

Offset Address	Register Name	Total Reset Value
0x084	SIO_SIGNED_EXT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															signed_ext_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	signed_ext_en	Upper-bit sign extend enable. 0: disabled 1: enabled

SIO_I²S_POS_MERGE_EN

SIO_I²S_POS_MERGE_EN is a data access position merging enable register of the I²S left and right channels.

When you read/write the FIFO data of the SIO in DMA mode over the I²S interface, the CPU needs to continuously configure the DMA operation addresses due to the different data addresses of the left and right channels. To improve the CPU efficiency, the access position merging bit of the left-channel and right-channel is used.

When the access position merging bit is enabled, both the right-channel and left-channel data is read through SIO_I²S_DUAL_RX_CHN register and written through the SIO_I²S_DUAL_TX_CHN register.

Offset Address	Register Name	Total Reset Value
0x088	SIO_I2S_POS_MERGE_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															merge_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	merge_en	Data access position merging enable of the I^{2}S left and right channels. 0: disabled 1: enabled

SIO_INTMASK

SIO_INTMASK is an SIO Interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x08C	SIO_INTMASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										tx_left_fifo_under	tx_right_fifo_under	rx_left_fifo_over	rx_right_fifo_over	tx_intr	rx_intr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Bits	Access	Name	Description
[31:6]	-	reserved	Reserved.
[5]	RW	tx_left_fifo_under	In I^{2}S mode, this bit indicates left channel TX FIFO underflow interrupt mask. 0: not masked 1: masked
[4]	RW	tx_right_fifo_under	In I^{2}S mode, this bit indicates right channel TX FIFO underflow interrupt mask. 0: not masked

			1: masked
[3]	RW	rx_left_fifo_over	In I²S mode, this bit indicates left channel RX FIFO overflow interrupt mask. 0: not masked 1: masked
[2]	RW	rx_right_fifo_over	In I²S mode, this bit indicates right channel RX FIFO overflow interrupt mask. 0: not masked 1: masked
[1]	RW	tx_intr	Interrupt mask when the TX_FIFO is below the threshold. 0: not masked 1: masked
[0]	RW	rx_intr	Interrupt mask when the RX_FIFO is above the threshold. 0: not masked 1: masked

SIO_I²S_DUAL_RX_CHN

SIO_I2S_DUAL_RX_CHN is a data receive register after enabling of I²S left and right channel data access position merging.

Offset Address	Register Name	Total Reset Value
0x0A0	SIO_I2S_DUAL_RX_CHN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_data																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rx_data	Received data.

SIO_I²S_DUAL_TX_CHN

SIO_I²S_DUAL_TX_CHN is a data transmit register after enabling of I²S left and right channel data access position merging.

Offset Address	Register Name	Total Reset Value
0x0C0	SIO_I²S_DUAL_TX_CHN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_data																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	tx_data	Transmitted data.

12.2 Audio Codec

12.2.1 Overview

The Hi3518 is integrated with high-performance audio CODECs, including high-quality stereo playback DAC (96 dB DR A-weighted), single-ended line out; high-quality stereo recording ADC (90 dB DR A-weighted), two single-ended stereo inputs; 6 dB to 37 dB MIC input, and analog gain control at 1 dB step. The I^2S data interface supports a standard sampling frequency ranging from 8 kHz to 192 kHz. It can work at two sampling frequencies at the same time. It also supports digital audio mixing.

12.2.2 Features

The audio CODEC module has the following features:

- 96 dBA DR stereo DAC (the Hi3518C supports only the audio-left channel)
- Single-ended stereo line out
- DAC digital volume control range: –121 dB to 6 dB, at 1 dB step
- 90 dBA DR stereo ADC
- Analog volume control range of ADC channel: 6 dB to 37 dB, at 1 dB step
- Digital volume control range of ADC channel: –96 dB to 30 dB, at 1 dB step
- Two alternative single-ended stereo inputs
- Provides internal MIC biasing
- Master and slave I^2S data interfaces, supporting 24 bits, 20 bits, 18 bits, and 16 bits, in binary format
- Audio sampling frequencies: 48 kHz, 44.1 kHz, and 32 kHz

  The sampling frequencies of each series are as follows:

  The 32 kHz sampling frequencies series include 8 kHz, 16 kHz, 32 kHz, 64 kHz, and 128 kHz.

  The 44.1 kHz sampling frequencies series include 11.025 kHz, 22.05 kHz, 44.1 kHz, 88.2 kHz, and 176.4 kHz. The 48 kHz sampling frequencies series include 12 kHz, 24 kHz, 48 kHz, 96 kHz, and 192 kHz.

12.2.3 Function Description

The audio CODEC module provides the recording and playing function. In the case of audio recording, analog signals are input from the MIC or line-in end, the gain is amplified at the analog part, and the signals converted into digital signals and output from the I^2S interface. Stereo recording is supported. In the case of playback, audio signals are input through the I^2S interface, converted into analog signals by the DAC, and then output. Stereo playing is supported.

Recording Mode

In recording mode, the MIC or line-in signals are input from the analog input end, processed by using the programmable gain method, converted by the ADC, filtered and volume-adjusted at the digital part, and finally output from the I^2S interface. Then, the entire recording procedure is complete.

The procedure is as follows:

Step 1 Power on the audio CODEC module, and the reference voltage works normally one second later.

Step 2 Configure the registers according to register descriptions.

Step 3 Input analog audio signals to start recording. Signals are then output from the I^2S interface.

----End

Playing Mode

In playing mode, audio signals are transmitted from the I^2S interface to the DAC digital part for filtering and volume control, filtering is performed at the analog part, and finally output by the lineout end.

The procedure is as follows:

Step 1 Power on the audio CODEC module, and the reference voltage works normally one second later.

Step 2 Configure the registers according to register descriptions.

Step 3 Transmit signals from the I^2S interface, and then output analog audio signals from the lineout end.

----End

12.2.4 Register Summary

The audio CODEC is controlled by using the registers of the system controller with the base address 0x2005_0000. The offset addresses of these registers are 0x0068, 0x006C, 0x0070, 0x0074, 0x0078, and 0x007C. That is, no interface is provided for controlling the audio CODEC.

12.2.5 Register Description

For details about the registers related to the audio CODEC, see section 3.4.5 "Register Summary" and section 3.4.6 "Register Description."

Contents

Figures

Tables

13 Peripherals

13.1 I²C Controller

13.1.1 Overview

The inter-integrated circuit (I^2C) module serves as the slave device on the advanced peripheral bus (APB) or the master device on the I^2C bus. The I^2C module is used to read/write data from/to the slave device on the I^2C bus through the CPU. When writing data to and reading data from the slave device, the CPU configures the I^2C configuration register over APB bus and transmits the control information and the data to be used to the I^2C data communication register. After parsing the commands, the I^2C module transmits the data of the data channel register to the slave device over I^2C bus and notifies the CPU of the final status to the CPU by using interrupts after transmitting the data. The CPU reads data from the slave device in the similar way.

13.1.2 Function Description

The I^2C module has the following features:

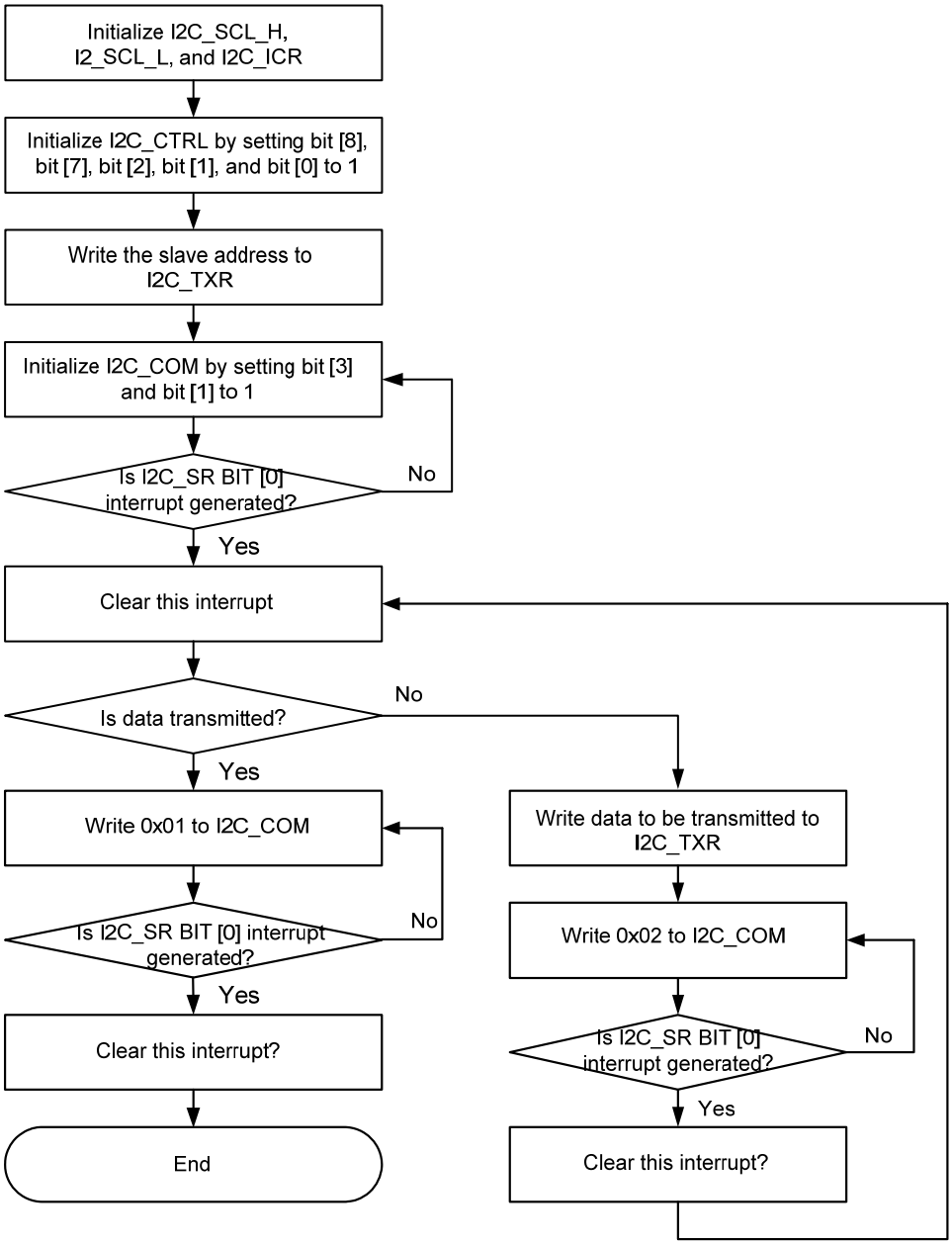
- Provides the master I^2C interface. The working reference clock of the I^2C module is the APB clock.
- Serves as the slave device on the APB bus or the master device on the I^2C bus, and supports the bus arbitration in the case of multiple master devices.
- Supports clock synchronization and bit and byte waiting.
- Supports interrupts or polling.
- Supports 7-bit standard address and 10-bit extended address.
- Supports standard mode (100 kbit/s) and high-speed mode (400 kbit/s).
- Supports general call and start byte.
- Incompatible with the CBUS component on the I^2C bus.
- Filters the received serial data (SDA) and serial clock (SCL) signals.

13.1.3 Operating Mode

13.1.3.1 Process of Transmitting Data Through the I²C Master

The I^2C master can write data to the slave or receive data from the slave. Figure 13-1 shows how the I^2C master transmits data.

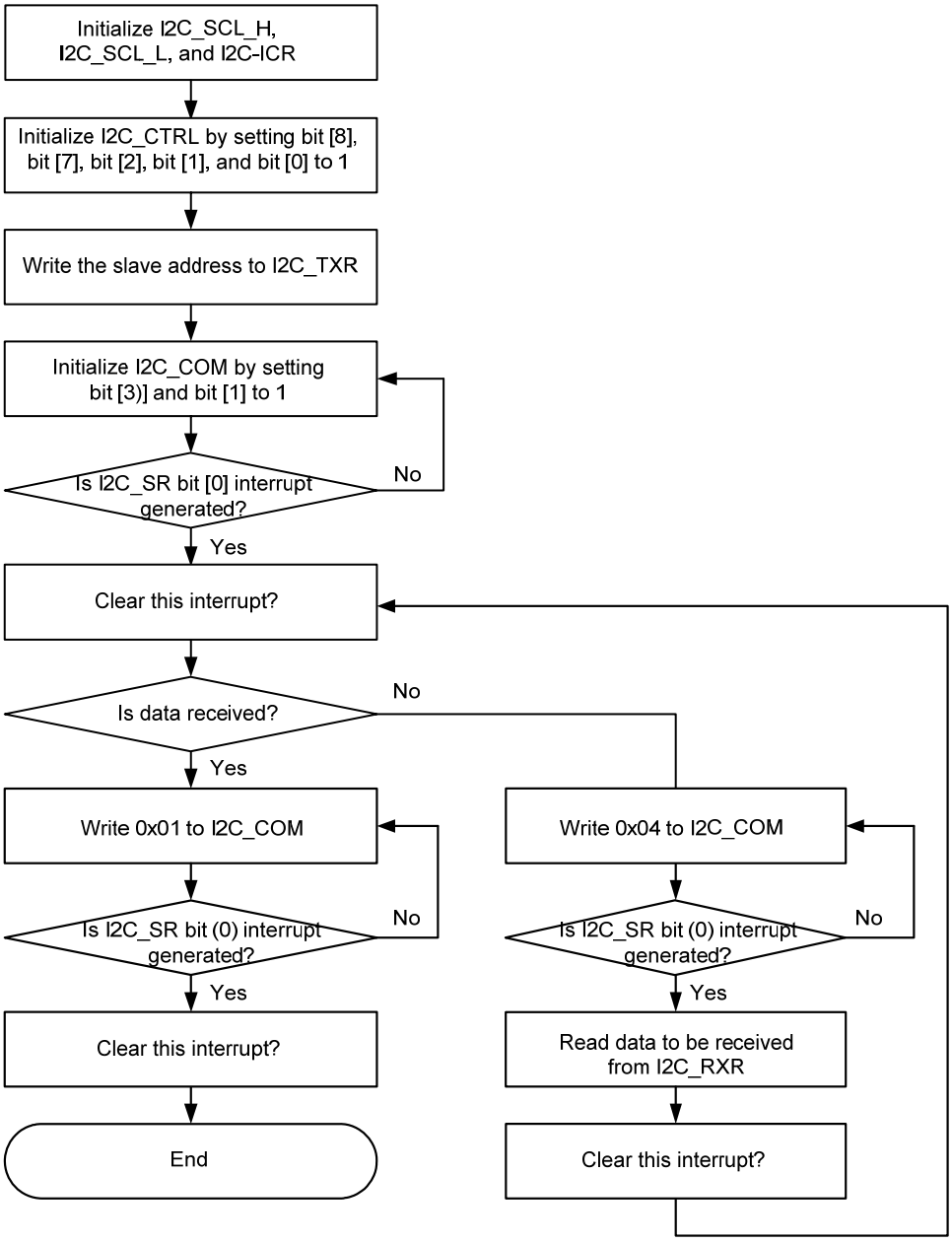
Figure 13-1 Process of transmitting data through the I²C master



13.1.3.2 Process of Receiving Data Through the I²C Master

Figure 13-2 shows how the I²C master receives data.

Figure 13-2 Process of receiving data through the I²C master



13.1.4 Register Summary

The Hi3518 contains an I²C module and the base address of I²C registers is 0x200D_0000.

Table 13-1 describes the I²C registers.

Table 13-1 Summary of I²C registers

Address	Register	Type	Description	Page
0x00	I2C_CTRL	RW	I²C control register	13-4
0x04	I2C_COM	RW	I²C command register	13-5
0x08	I2C_ICR	RW	I²C interrupt clear register	13-6
0x0C	I2C_SR	RO	I²C status register	13-7
0x10	I2C_SCL_H	RW	I²C SCL high-level cycle number register	13-8
0x14	I2C_SCL_L	RW	I²C SCL low-level cycle number register	13-9
0x18	I2C_TXR	RW	I²C transmit data register	13-10
0x1C	I2C_RXR	RO	I²C receive data register	13-11

13.1.5 Register Description

I2C_CTRL

I2C_CTRL is an I²C control register. It is used to enable the I²C module and mask interrupts.

Offset Address	Register Name	Total Reset Value
0x00	I2C_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							i2c_en	int_mask	int_start_mask	int_stop_mask	int_tx_mask	int_rx_mask	int_ack_err_mask	int_arb_loss_mask	int_done_mask
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	-	reserved	Reserved.
[8]	RW	i2c_en	I²C enable. 0: disabled 1: enabled
[7]	RW	int_mask	Global I²C interrupt mask. 0: masked 1: not masked.

[6]	RW	int_start_mask	Master start condition transmit end interrupt mask. 0: masked 1: not masked.
[5]	RW	int_stop_mask	Master stop condition transmit end interrupt mask. 0: masked 1: not masked.
[4]	RW	int_tx_mask	Master transmit interrupt mask. 0: masked 1: not masked.
[3]	RW	int_rx_mask	Master receive interrupt mask. 0: masked 1: not masked.
[2]	RW	int_ack_err_mask	Slave ACK error interrupt mask. 0: masked 1: not masked.
[1]	RW	int_arb_loss_mask	Bus arbitration failure interrupt mask. 0: masked 1: not masked.
[0]	RW	int_done_mask	Bus transfer done interrupt mask. 0: masked 1: not masked.

I2C_COM

I2C_COM is an I^2C command register. It is used to configure the commands for the I^2C module.

CAUTION

During or before the configuration of system initialization, the corresponding interrupts must be cleared. I2C_COM bit[3:0] are automatically cleared after the initialization.

Offset Address	Register Name	Total Reset Value
0x04	I2C_COM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											op_ack	op_start	op_rd	op_we	op_stop
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	-	reserved	Reserved.
[4]	RW	op_ack	Indicates whether to send an ACK when the master serves as the receiver. 0: yes 1: no
[3]	RW	op_start	Start condition operation. 0: The operation is complete. 1: The operation is valid.
[2]	RW	op_rd	Read operation. 0: The operation is complete. 1: The operation is valid.
[1]	RW	op_we	Write operation. 0: The operation is complete. 1: The operation is valid.
[0]	RW	op_stop	Stop condition operation. 0: The operation is complete. 1: The operation is valid.

I2C_ICR

I2C_ICR is an I^2C interrupt clear register.

CAUTION

When a new interrupt is generated, the I^2C module automatically clears certain bits of I2C_ICR.

Offset Address	Register Name	Total Reset Value
0x08	I2C_ICR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									clr_int_start	clr_int_stop	clr_int_tx	clr_int_rx	clr_int_ack_err	clr_int_arb_loss	clr_int_done
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	-	reserved	Reserved.
[6]	WC	clr_int_start	Master start condition transmit end interrupt clear. 0: not cleared 1: cleared
[5]	WC	clr_int_stop	Master stop condition transmit end interrupt clear. 0: not cleared 1: cleared
[4]	WC	clr_int_tx	Master transmit interrupt clear. 0: not cleared 1: cleared
[3]	WC	clr_int_rx	Master receive interrupt clear. 0: not cleared 1: cleared
[2]	WC	clr_int_ack_err	Slave ACK error interrupt clear. 0: not cleared 1: cleared
[1]	WC	clr_int_arb_loss	Bus arbitration failure interrupt clear. 0: not cleared 1: cleared
[0]	WC	clr_int_done	Bus transfer done interrupt clear. 0: not cleared 1: cleared

I2C_SR

I2C_SR is an I^2C status register. It is used to read the operating status of the I^2C module.

CAUTION

I2C_SR bit[1] indicates an I^2C bus arbitration failure. When I2C_SR bit[1] is valid, the current operation fails. Before clearing I2C_SR bit[1], you need to clear other interrupts and clear I2C_COM or write a new command to I2C_COM in sequence.

Offset Address	Register Name	Total Reset Value
0x0C	I2C_SR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								bus_busy	int_start	int_stop	int_tx	int_rx	int_ack_err	int_arb_loss	int_done
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved.
[7]	RO	bus_busy	Bus busy. 0: idle 1: busy
[6]	RO	int_start	Master start condition transmit end interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[5]	RO	int_stop	Master stop condition transmit end interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RO	int_tx	Master transmit interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RO	int_rx	Master receive interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	int_ack_err	Slave ACK error interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	int_arb_loss	Bus arbitration failure interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

[0]	RO	int_done	Bus transfer done interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

I2C_SCL_H

I2C_SCL_H is an I^{2}C SCL high-level cycle number register. It is used to configure the number of SCL high-level cycles of the working I^{2}C module.

CAUTION

During or before the configuration of system initialization, you must set I2C_CTRL bit[7] to 0.

Offset Address	Register Name	Total Reset Value
0x10	I2C_SCL_H	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																scl_h															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	scl_h	Number of SLC high-level cycles x 2.

Assume that the frequency of the system clock is 108 MHz, I2C_SCL_H is set to *m*, and the SCL high-level period is DelTim. DelTim is calculated as follows:

Deltim = 1/108 x (m + 1) x 2, (in the unit of μs)

If the required SCL high-level period is 5 μs, the value m of I2C_SCL_H is:

m = (5 x 108)/2 – 1 = 269

When the frequency of the system clock is 108 MHz, the maximum SCL high-level period is 606 μs.

I2C_SCL_L

I2C_SCL_L is an I^{2}C SCL low-level cycle number register. It is used to configure the number of SCL low-level cycles when the I^{2}C module works.

CAUTION

During or before the configuration of system initialization, you must set I2C_CTRL bit[7] to 0.

Offset Address	Register Name	Total Reset Value
0x14	I2C_SCL_L	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																scl_l															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	scl_l	Number of SLC low-level cycles x 2.

Assume that the frequency of the system clock is 108 MHz, I2C_SCL_L is set to m, and the SCL low-level period is DelTim. DelTim is calculated as follows:

Deltim = 1/108 x (m + 1) x 2, (in the unit of μs)

If the required SCL low-level period is 5 μs, the value m of I2C_SCL_L is:

m = (5 x 108)/2 – 1 = 269

When the frequency of the system clock is 108 MHz and the maximum SCL low-level period is 606 μs.

I2C_TXR

I2C_TXR is an I^2C transmit data register. It is used to enable the I^2C module to transmit data.

CAUTION

When data is transmitted completely, the I^2C module does not modify I2C_TXR.

Offset Address	Register Name	Total Reset Value
0x18	I2C_TXR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								i2c_txr							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved.
[7:0]	RW	i2c_txr	Data is transmitted by the master

I2C_RXR

I2C_RXR is an I^2C receive data register. It is used to enable the master to receive the data from the slave.

CAUTION

When I2C_SR bit[3] is 1, the I2C_RXR data is valid. The data is remained until the next start operation starts.

Offset Address	Register Name	Total Reset Value
0x1C	I2C_RXR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								i2c_rxr							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved.
[7:0]	RO	i2c_rxr	Data is received by the master.

13.2 SPI

13.2.1 Overview

The serial peripheral interface (SPI) controller implements serial-to-parallel conversion and parallel-to-serial conversion, and serves as a master to communicate with peripherals in

synchronous and serial modes. The SPI controller supports three types of peripheral interfaces including the SPI, TI synchronous serial interface, and MicroWire interface.

13.2.2 Features

CAUTION

The Hi3518A has two serial peripheral interface (SPIs). Each SPI supports a chip select (CS). The Hi3518C has no SPI.

The Hi3518A SPIs are master interfaces. The working reference clock is the APB bus clock. SPI_CLK output by the SPI supports the maximum working frequency of 22.5 MHz.

The SPI controller has the following features:

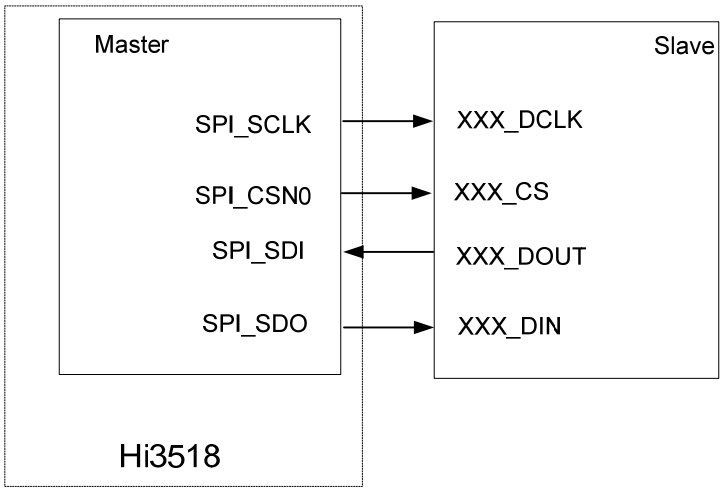
- Supports programmable frequency of the interface clock.
- Supports two separate FIFOs. One acts as a receive FIFO and the other one acts as a transmit FIFO. Each of them is 16-bit wide and 256-location deep.
- Supports programmable serial data frame length: 4 bits to 16 bits.
- Provides internal loopback test mode.
- Supports the direct memory access (DMA) operation.
- Supports three types of peripheral interfaces including the SPI, MicroWire interface, and TI synchronous serial interface.
- Supports SPI in full-duplex mode and configurable clock polarity and phase.
- Supports MicroWire in half-duplex mode.
- Supports TI synchronous serial interface in full-duplex mode.

13.2.3 Function Description

Typical Application

Figure 13-3 shows the application block diagram when the SPI is connected to a slave device. The default chip select pin SPI_CSN0 is used.

Figure 13-3 Application block diagram when the SPI is connected to a single slave device



13.2.4 Peripheral Bus Timings

The meanings of the abbreviations and acronyms in Figure 13-4 to Figure 13-11 are as follows:

- MSB: most significant bit
- LSB: least significant bit
- Q: Q is an undefined signal

SPI

NOTE

SPO indicates the polarity of SPICLKOUT and SPH indicates the phase of SPICLKOUT. They correspond to SPICR0 bit[7:6].

(1)SPO = 0, SPH = 0

Figure 13-4 shows the SPI single frame format.

Figure 13-4 SPI single frame format (SPO = 0, SPH = 0)

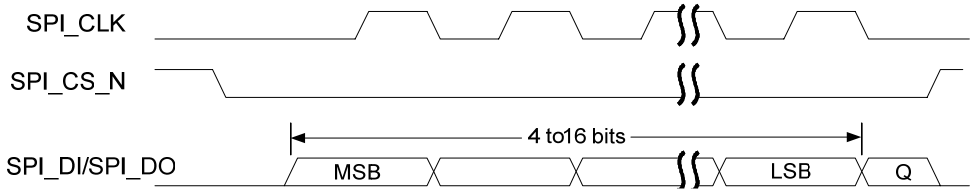
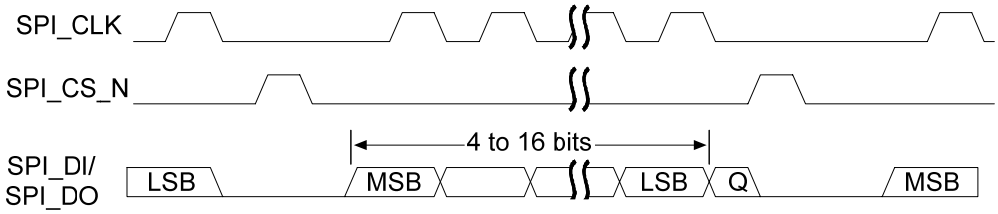


Figure 13-5 shows the SPI continuous frame format.

Figure 13-5 SPI continuous frame format (SPO = 0, SPH = 0)



When the SPI is idle in this mode:

- The SPI_CLK signal is set to low.
- The SPI_CS_N signal is set to high.
- The transmit data line SPI_DO is forced to low.

When the SPI is enabled and valid data is ready in the transmit FIFO, data transfer starts if the SPI_CS_N signal is set to low. The data from the slave device is transferred to the receive data line SIP_DI of the master device immediately. Half SPI_CLK clock cycle later, the valid master data is transmitted to SPI_DO. At this time, both the master and slave data become valid. The SPI_CLK pin changes to high level in the next half SPI_CLK clock cycle. Then, data is captured on the rising edge and is transmitted on the falling edge of the SPI_CLK clock.

If a single word is transferred, SPI_CS_N is restored to high level one SPI_CLK clock later after the last bit is captured.

For continuous transfer, the SPI_CS_N signal must pull up the SPI_CLK clock by one clock cycle between the transfers of two words. When SPH is 0, the slave select pin fixes the data of the internal serial device register. Therefore, the master device must pull up the SPI_CS_N signal between the transfers of two words in continuous transfer. When the continuous transfer ends, SPI_CS_N is restored to high level one SPI_CLK clock cycle later after the last bit is captured.

(2) SPO = 0, SPH = 1

Figure 13-6 shows the SPI single frame format.

Figure 13-6 SPI single frame format (SPO = 0, SPH = 1)

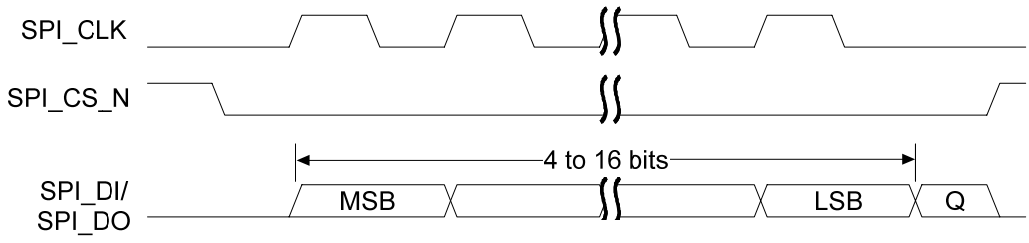
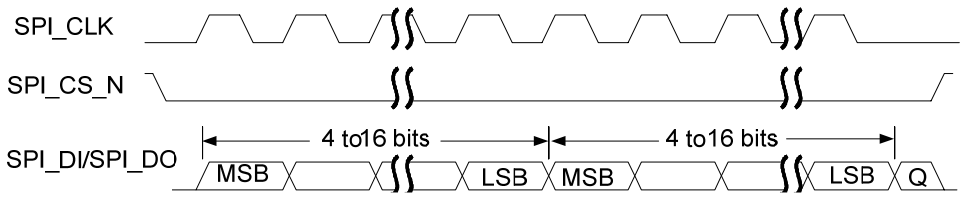


Figure 13-7 shows the SPI continuous frame format.

Figure 13-7 SPI continuous frame format (SPO = 0, SPH = 1)



When the SPI is idle in this mode:

- The SPI_CLK signal is set to low.
- The SPI_CS_N signal is set to high.
- The transmit data line SPI_DO is forced to low.

When the SPI is enabled and valid data is ready in the transmit FIFO, data transfer start if the SPI_CS_N signal is set to low. The master and slave data become valid on their respective transfer line half SPI_CLK clock cycle later. Meanwhile, SPI_CLK becomes valid from the first rising edge. Then, data is captured on the falling edge and is transmitted on the rising edge of the SPI_CLK clock.

If a single word is transferred, SPI_CS_N is restored to high level one SPI_CLK clock later after the last bit is captured.

For a continuous transfer, SPI_CS_N remains low between the transfers of two words. When the continuous transfer ends, SPI_CS_N is restored to high level one SPI_CLK clock cycle later after the last bit is captured.

(3) SPO = 1, SPH = 0

Figure 13-8 shows the SPI single frame format.

Figure 13-8 SPI single frame format (SPO = 1, SPH = 0)

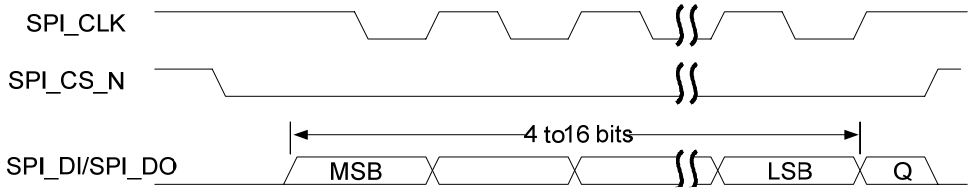
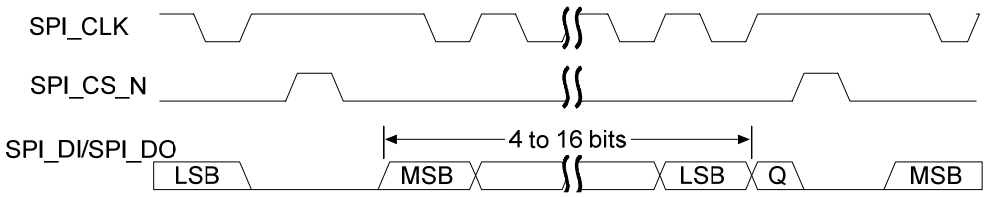


Figure 13-9 shows the SPI continuous frame format.

Figure 13-9 SPI continuous frame format (SPO = 1, SPH = 0)



When the SPI is idle in this mode:

- The SPI_CLK signal is set to high.
- The SPI_CS_N signal is set to high.
- The transmit data line SPI_DO is forced to low.

When the SPI is enabled and valid data is ready in the transmit FIFO, data transfer starts if the SPI_CS_N signal is set to low. The data from the slave device is transferred to the receive data line SPI_DI of the master device immediately. Half SPI_CLK clock cycle later, the valid master data is transmitted to SPI_DO. After another half SPI_CLK clock cycle, the SPI_CLK master pin is set to low. Then, data is captured on the falling edge and is transmitted on the rising edge of the SPI_CLK clock.

If a single word is transferred, SPI_CS_N is restored to high level after one SPI_CLK clock since the data of the last bit is captured.

For a continuous transfer, the SPI_CS_N signal must be pulled up between the transfers of two words. This is because that when SPH is 0, the slave select pin fixes the data of the internal serial device register. SPI_CS_N is restored to high level one SPI_CLK clock later after the last bit is captured.

(4) SPO = 1, SPH = 1

Figure 13-10 shows the SPI single frame format.

Figure 13-10 SPI single frame format (SPO = 1, SPH = 1)

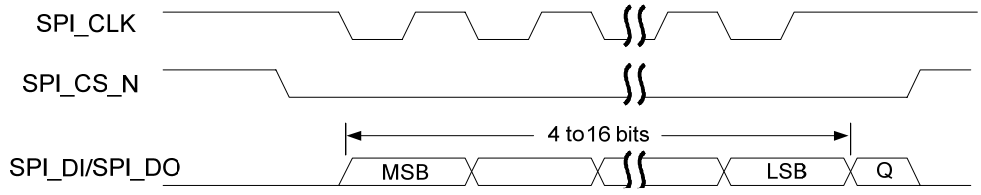
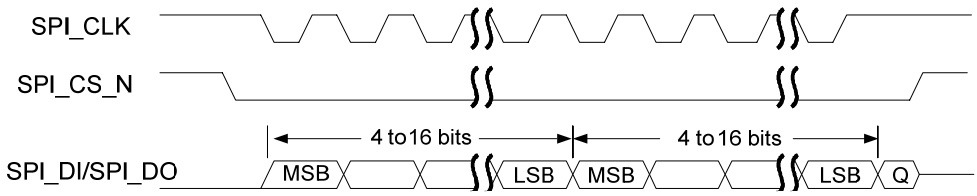


Figure 13-11 shows the SPI continuous frame format.

Figure 13-11 SPI continuous frame format (SPO = 1, SPH = 1)



When the SPI is idle in this mode:

- The SPI_CLK signal is set to high.
- The SPI_CS_N signal is set to high.
- The transmit data line SPI_DO is forced to low.

When the SPI is enabled and valid data is ready in the transmit FIFO, data transfer starts if the SPI_CS_N signal is set to low. Half SPI_CLK clock cycle later, the master data and slave data are valid on respective transfer line. Meanwhile, SPI_CLK becomes valid from a falling edge of SPI_CLK. Then, data is captured on the rising edge and is transmitted on the falling edge of the SPI_CLK clock. If a single word is being transmitted, SPI_CS_N is restored to high level one SPI_CLK clock cycle later after the last bit is captured.

For a continuous transfer, the SPI_CS_N signal remains low. SPI_CS_N is restored to high level one SPI_CLK clock cycle after the last bit is captured. For a continuous transfer, SPI_CS_N remains low during transfer. The method of ending data transfer is the same as that in single transfer mode.

(5) Interface timings

Figure 13-12 SPI timings

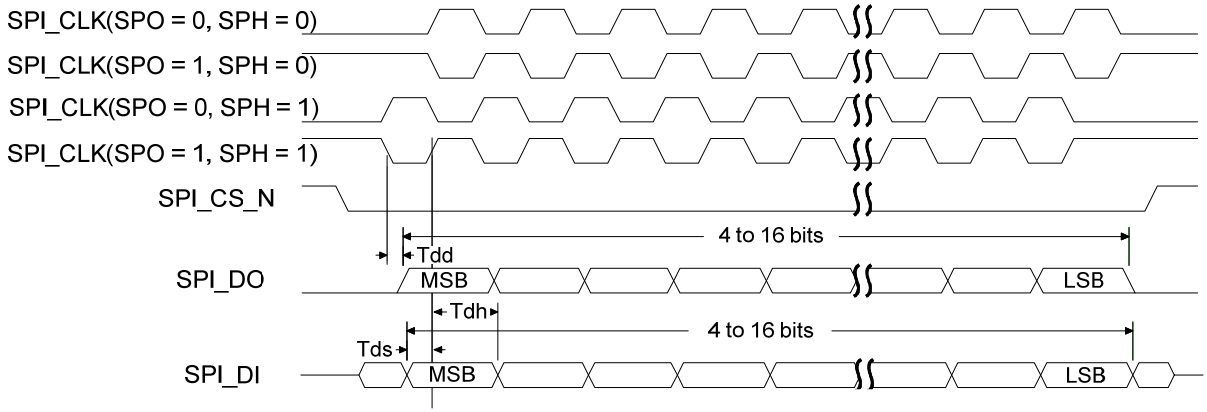


Table 13-2 Timing parameters of the SPI

Parameter	Description	Min	Max	Unit
Tdd	Output data delay	– 3.5	5	ns
Tds	Input control signal setup time	23	None	ns

Parameter	Description	Min	Max	Unit
Tdh	Input control signal hold time	0	None	ns

TI Synchronous Serial Interface

Figure 13-13 shows the TI synchronous serial single frame format.

Figure 13-13 TI synchronous serial single frame format

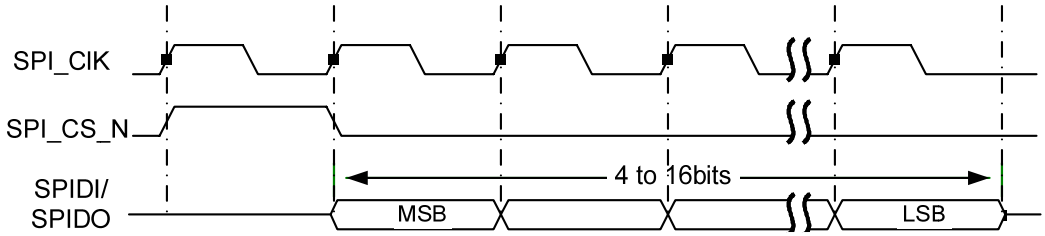
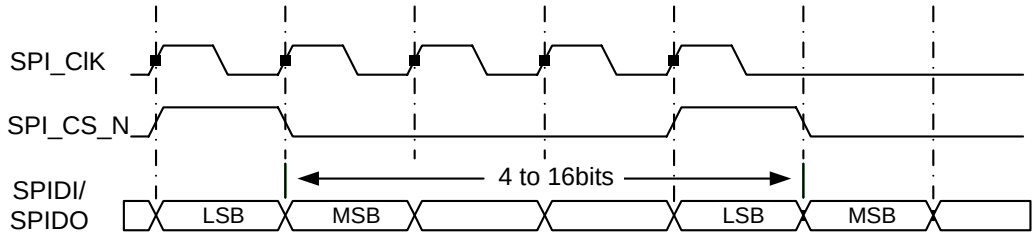


Figure 13-14 shows the TI synchronous serial continuous frame format.

Figure 13-14 TI synchronous serial continuous frame format



When the SPI is idle in this mode:

- The SPI_CK signal is set to low.
- The SPI_CS_N signal is set to low.
- The transfer data line SPI_DO retains high impedance.

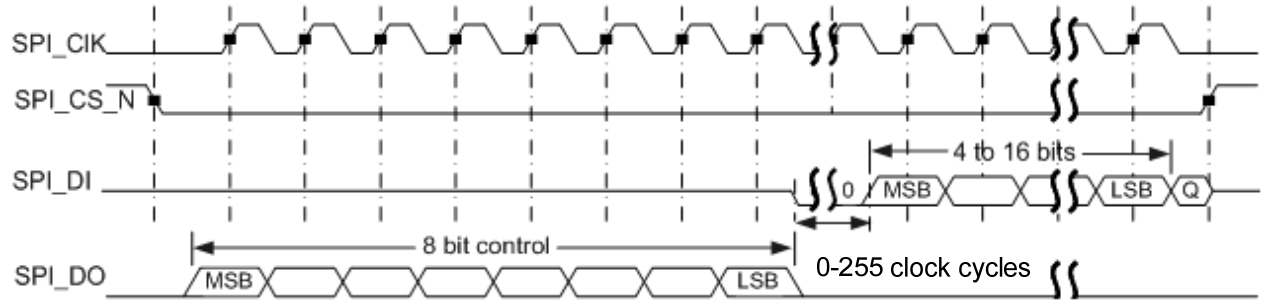
If there is data in the transmit FIFO, SPI_CS_N generates a high-level pulse in one SPI_CK clock cycle. Then, the data to be transmitted is transferred from the transmit FIFO to the transmit logic serial shift register. In addition, the MSBs of the data frames with the length of 4–16 bits are shifted and output from SPI_DO on the next rising edge of the SPI_CK clock. Similarly, the MSB of the data received from the external serial slave device is shifted and input from the SPI_DI pin.

The SPI and off-chip serial device stores the data in the serial shift register on the falling edge of the SPI_CK clock. The receive serial register transmits the data to the receive FIFO on the rising edge of the first SPI_CK clock after receiving the LSB.

National Semiconductor Microwire Interface

Figure 13-15 shows the national semiconductor microwire single frame format.

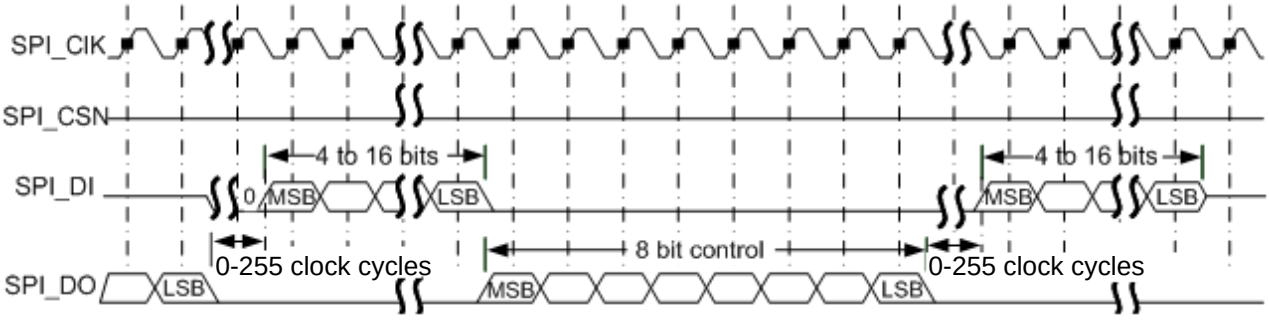
Figure 13-15 National semiconductor microwire single frame format



0 to 255 clock cycles can be delayed between the end of SPI_DO LSB and the start of SPI_DI MSB.

Figure 13-16 shows the national semiconductor microwire continuous frame format.

Figure 13-16 National semiconductor microwire continuous frame format



0 to 255 clock cycles can be delayed between the end of SPI_DO LSB and the start of SPI_DI MSB.

The microwire format is similar to the SPI format because both of them use the technology of transferring master-slave information. The only difference is that the SPI works in full-duplex mode and the microwire interface works in half-duplex mode. Before the SPI transmits serial data to the external chip, an 8-bit control word needs to be added. In this process, the SPI does not receive any data. After data transfer is complete, the external chip decodes the received data. One clock cycle later after 8-bit control information is transmitted, the slave device starts to respond to the required data. The returned data length is 4 bits to 16 bits, and the length of the entire frame is 13 bits to 25 bits.

When the SPI is idle in this mode:

- The SPI_CLK signal is set to low.
- The SPI_CS_N signal is set to high level.
- The transmit data signal SPI_DO is forced to low level.

Writing one control byte to the transmit FIFO starts a data transfer. The data transfer is triggered on a falling edge of SPI_CS_N. The data of the transmit FIFO is sent to the serial

shift register. The MSB of the 8-bit control frame is transmitted to the SPI_DO pin. During frame transfer, SPI_CS_N remains low. Whereas SPI_DI retains high impedance.

The off-chip serial slave device latches the data to the serial shift register on each rising edge of the SPI_CLK clock. After the slave device latches the data of the last bit, the slave device starts to decode the received data in the next clock cycle. Then, the slave device provides the data required by the SPI. Each bit is written to SPI_DI on the falling edge of the SPI_CK clock. For a single data transfer, SPI_CS_N is pulled up at the end of the frame one clock cycle after the last bit is written to the receive serial register. In this way, the received data is transmitted to the receive FIFO.

The start and end for a continuous data transfer are the same as those for a signal data transfer. During the continuous data transfer, SPI_CS_N retains low and the data transferred is continuous. The control word of the next frame is adjacent to the LSB of the previous frame. When the LSB of the frame is latched to the SPI, each received value is originated from the receive shift register on the falling edge of the SPI_CLK clock.

13.2.5 Operating Mode

Working Modes

The SPI working modes include the data transmission in the interrupt or query mode and the data transmission in the DMA mode.

Clock and Reset

The frequency of the output SPI clock is calculated as follows:

Fsspclkout = Fsspclk/[CPSDVR x (1 + SCR)]

Fsspclk is the working reference clock of the SPI and its value is 1/2 of the bus clock.

For details about CPSDVR and SCR, query the corresponding registers.

The SPI working reference clock supports clock gating, which is implemented by using the PERI_CRG57 bit[12] register. Writing 0 to the corresponding bit disables the clock and writing 1 to the corresponding bit enables the clock. The default value is 1 after power on.

The SPI of the Hi3518A supports separate soft reset, which is controlled by using the PERI_CRG57 bit[12] register. Writing 0 to the corresponding bit stops soft reset and writing 1 to the corresponding bit starts soft reset. The default value is 0 after power on.

Interrupts

The SPI has five interrupts. Four of them have separate interrupts sources and maskable and active high.

- SPIRXINTR

  Receive FIFO interrupt request. When there are four or more valid data segments in the receive FIFO, the interrupt is set to 1.
- SPITXINTR

  Transmit FIFO interrupt request. When there are four or less valid data segments in the transmit FIFO, the interrupt is set to 1.
- SPIRORINTR

Receive overrun interrupt request. When the FIFO is full and new data is written to the FIFO, the FIFO is overrun and the interrupt is set to 1. In this case, the data is written to the receive shift register rather than the FIFO.

- SPIRTINTR

  Receive timeout interrupt request. When the receive FIFO is not empty and the SPI is idle for more than a fixed 32-bit cycle, the interrupt is set to 1.

  It indicates that data in the receive FIFO needs to be transmitted. When the receive FIFO is empty or new data is transmitted to SPIRXD, the interrupt is cleared. The interrupt can also be cleared by writing to the SPIICR[RTIC] register.

- SPIINTR

  Combined interrupt. This interrupt is obtained by performing an OR operation on the preceding four interrupts. If any of the preceding four interrupts is set to 1 and enabled, SPIINTR is set to 1.

For details about how to connect the SPIINTR of SPI, see "Interrupts" in this section.

Initialization

The initialization is implemented as follows:

1. Write 0 to SPICR1[sse] to disable the SPI.
2. Write to SPICR0 to set the parameters such as the frame format and transfer data bit width.
3. Configure SPICPSR to set the required clock divider.
4. In the interrupt mode, configure SPIIMSC to enable the corresponding interrupts or disable the generation of corresponding interrupts in query or DMA mode.
5. Configure SPITXFIFOCR and SPIRXFIFOCR in interrupt or DMA mode.
6. Configure SPIDMACR to enable the DMA function of the SPI in DMA mode.

----End

Data Transfer in Query Mode

The full status of the transmit or receive FIFO is not considered, because the depth of the transmit FIFO or receive FIFO is 512.

Perform the following steps:

1. Write 1 to SPICR1[sse] to enable the SPI.
2. Write the data to be transmitted to SPIDR continuously.
3. Poll SPISR until SPISR[BSY] is 0, SPISR[TFE] is 1, and SPISR[RNE] is 1. If SPISR[BSY] is 0, the bus is busy; if SPISR[TFE] is 1, the transmit FIFO is empty; if SPISR[RNE] is 1, the receive FIFO is not empty.
4. Read data until the receive FIFO is empty. You can check whether the receive FIFO is empty by querying SPISR[RNE].

CAUTION

The SPI/Microwire has full-duplex features. That is, a data segment is received after a data segment is transmitted. Even if only data is transmitted, the receive FIFO must be cleared.

5. Write 0 to SPICR1[sse] to disable the SPI.

----End

Data Transfer in Interrupt Mode

Perform the following steps:

1. Write 1 to SPICR1 [sse] to disable the SPI.
2. Write the data to be transmitted to SPIDR continuously.
3. Wait for the interrupt SPIRXINTR and read data in cyclic mode until all data is read.

   Note that the full-duplex features of the SPI/Microwire. That is, a data segment is received after a data segment is transmitted. Even if only data is transmitted, the receive FIFO must be cleared.
4. Write 0 to SPICR1 [sse] to disable the SPI.

----End

Data Transfer in DMA Mode

Perform the following steps:

1. Obtain a DMAC channel.
2. Write 1 to SPICR1 [sse] to disable the SPI.
3. Transmit data.
   a. Configure the parameters of the configuration register and control register related to the DMAC channel.
   b. Start the DMAC and respond to the DMA request of the SPI transmit FIFO for the data transfer.
   c. Check whether all data is transmitted by viewing the DMA interrupt. If all data is transmitted, disable the DMA transmit function of the SPI.
4. Receive data
   a. Configure the parameters of the configuration register and control register related to the DMAC channel.
   b. Start the DMAC and respond to the DMA request of the SSP receive FIFO for the data transfer.
   c. Check whether all data is received by viewing the DMA interrupt. If all data is received, disable the DMA receive function of the SPI.
5. Write 0 to SPICR1 [sse] to disable the SPI.

----End

13.2.6 Register Summary

Table 13-3 describes the registers.

- The base address of SPI registers is 0x200C_0000.
- The base address of SPI registers is 0x200E_0000.

Table 13-3 Summary of SPI registers

Offset Address	Register	Description	Page
0x000	SPICR0	Control register 0	13-23
0x004	SPICR1	Control register 1	13-25
0x008	SPIDR	Data register	13-26
0x00C	SPISR	Status register	13-26
0x010	SPICPSR	Clock divider register	13-27
0x014	SPIIMSC	Interrupt mask register	13-27
0x018	SPIRIS	Raw interrupt status register	13-28
0x01C	SPIMIS	Masked interrupt status register	13-29
0x020	SPIICR	Interrupt clear register	13-30
0x024	SPIDMACR	DMA control register	13-30
0x028	SPITXFIFOCR	Transmit FIFO control register	13-31
0x02C	SPIRXFIFOCR	Receive FIFO control register	13-32

13.2.7 Register Description

SPICR0

SPICR0 is SPI control register 0.

Offset Address	Register Name	Total Reset Value
0x000	SPICR0	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SCR								SPH	SPO	FRF		DSS			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:8]	RW	SCR	Serial clock rate, ranging from 0 to 255. The value of the SCR is used to generate the transmit and receive bit rates of the SPI. The formula is as follows: FSPICLK/(CPSDVSR (1 + SCR). CPSDVSR is an even ranging from 2 to 254, and it is configured by SPICPSR.
[7]	RW	SPH	SPICLKOUT phase. For details, see the "SPI frame format of Peripheral Bus Timings" in section 14.2.4.
[6]	RW	SPO	SPICLKOUT polarity. For details, see the "SPI Frame Format of Peripheral Bus Timings" in section 14.2.4.
[5:4]	RW	FRF	Frame format select. 00: Motorola SPI frame format 01: TI synchronous serial frame format 10: National microwire frame format 11: reserved
[3:0]	RW	DSS	Data width. 0011: 4 bits 1000: 9 bits 1101: 14 bits 0100: 5 bits 1001: 10 bits 1110: 15 bits 0101: 6 bits 1010: 11 bits 1111: 16 bits 0110: 7 bits 1011: 12 bits 0111: 8 bits 1100: 13 bits Other values: reserved

SPICR1

SPICR1 is SPI control register 1.

Offset Address	Register Name	Total Reset Value
0x004	SPICR1	0x7F00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WaitEn	WaitVal							reserved			BigEnd	reserved	MS	SSE	LBM
Reset	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15]	RW	WaitEn	Wait enable. This bit is valid when the SPICR0[FRF] is set to the national microwire frame format. 0: disabled 1: enabled
[14:8]	RW	WaitVal	Number of waiting beats between read and write when in the national microwire frame format. When WaitEn is 1 and the frame format is national microwire, WaitVal is valid.
[7:5]	RW	reserved	Reserved.
[4]	RW	BigEnd	Data endian mode. 0: little endian 1: big endian
[3]	RW	reserved	Reserved.
[2]	RW	MS	Master or slave mode. This bit can be changed only when the SPI is disabled. 0: master mode (default value) 1: reserved
[1]	RW	SSE	SPI enable. 0: disabled 1: enabled
[0]	RW	LBM	Loopback mode. 0: A normal serial port operation is enabled. 1: The output of the transmit serial shift register is connected to the input of the receive serial shift register.

SPIDR

SPIDR is a data register.

Offset Address	Register Name	Total Reset Value
0x008	SPIDR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:0]	RW	DATA	transmit or receive FIFO. Read: receive FIFO Write: transmit FIFO If the data is less than 16 bits, the data must be aligned to the right. The transmit logic ignores the unused upper bits, and the receive logic automatically aligns the data to the right.

SPISR

SPISR is a status register.

Offset Address	Register Name	Total Reset Value
0x00C	SPISR	0x0003

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved											BSY	RFF	RNE	TNF	TFE
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[15:5]	RW	reserved	Reserved.
[4]	RW	BSY	SPI busy flag. 0: idle 1: busy
[3]	RW	RFF	Whether the receive FIFO is full. 0: not full 1: full.

[2]	RW	RNE	Whether the receive FIFO is not empty. 0: empty 1: not empty
[1]	RW	TNF	Whether the transmit FIFO is not full. 0: full 1: not full
[0]	RW	TFE	Whether the transmit FIFO is empty. 0: not empty 1: empty

SPICPSR

SPICPSR is a clock divider register.

Offset Address	Register Name	Total Reset Value
0x010	SPICPSR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								CPSDVSR							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:8]	RW	reserved	Reserved.
[7:0]	RW	CPSDVSR	Clock divider. The value must be an even ranging from 2 to 254. It depends on the frequency of the input clock SPICLK. The LSB is read as 0.

SPIIMSC

SCIIMSC is an interrupt mask register. The value 0 indicates an interrupt is masked and the value1 indicates an interrupt is not masked.

Offset Address	Register Name	Total Reset Value
0x014	SPIIMSC	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												TXIM	RXIM	RTIM	RORIM
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:4]	RW	reserved	Reserved.
[3]	RW	TXIM	Transmit FIFO interrupt mask. 0: The interrupt masked when only half of or less data is left in the transmit FIFO. 1: The interrupt not masked when only half of or less data is left the transmit FIFO.
[2]	RW	RXIM	Receive FIFO interrupt mask. 0: The interrupt is masked when only half of or less data is left in the receive FIFO. 1: The interrupt is not masked when only half of or less data is left in the receive FIFO.
[1]	RW	RTIM	Receive timeout interrupt mask. 0: masked 1: not masked
[0]	RW	RORIM	Receive overflow interrupt mask. 0: masked 1: not masked When the value is 1, the hardware stream control function is enabled. That is, when the receive FIFO is full, the SPI stops transmitting data.

SPIRIS

SPIRIS is a raw interrupt status register. The value 0 indicates no interrupts are generated, and the value 1 indicates interrupts are generated.

Offset Address	Register Name	Total Reset Value
0x018	SPIRIS	0x0008

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												TXRIS	RXRIS	RTRIS	RORRIS
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[15:4]	RO	reserved	Reserved.
[3]	RO	TXRIS	Raw transmit FIFO interrupt status.
[2]	RO	RXRIS	Raw receive FIFO interrupt status.
[1]	RO	RTRIS	Raw receive timeout interrupt status.
[0]	RO	RORRIS	Raw receive overflow interrupt status.

SPIMIS

SPIMIS is a masked interrupt status register. The value 0 indicates no interrupts are generated, and the value 1 indicates interrupts are generated.

Offset Address	Register Name	Total Reset Value
0x01C	SPIMIS	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												TXMIS	RXMIS	RTMIS	RORMIS
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:4]	RO	reserved	Reserved.
[3]	RO	TXMIS	Status of the masked transmit FIFO interrupt.
[2]	RO	RXMIS	Status of the masked transmit FIFO interrupt.
[1]	RO	RTMIS	Status of the masked receive timeout interrupt.
[0]	RO	RORMIS	Status of the masked receive overflow interrupt.

SPIICR

SCIICR is an interrupt clear register. Writing 1 clears an interrupt, and writing 0 has no effect.

Offset Address	Register Name	Total Reset Value
0x020	SPIICR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														RTIC	RORIC
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:2]	RO	reserved	Reserved.
[1]	RO	RTIC	Receive timeout interrupt clear.
[0]	RO	RORIC	Receive overflow interrupt clear.

SPIDMACR

SCIDMACR is a DMA control register.

Offset Address	Register Name	Total Reset Value
0x024	SPIDMACR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														TXDMAE	RXDMAE
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:2]	WO	reserved	Reserved.
[1]	WO	TXDMAE	DMA transmit FIFO enable. 0: disabled 1: enabled
[0]	WO	RXDMAE	DMA receive FIFO enable. 0: disabled 1: enabled

SPITXFIFOCR

SPITXFIFOCR is a transmit FIFO control register.

Offset Address	Register Name	Total Reset Value
0x028	SPITXFIFOCR	0x0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										TXINTSize			DMATXBRSize		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[15:6]	RW	reserved	Reserved.
[5:3]	RW	TXINTSize	Threshold for generating the transmit FIFO request interrupt. That is, when the number of data segments in the transmit FIFO is less than or equal to the value of TXINTSize, TXRIS is valid. 000: 1 001: 4 010: 8 011: 16 100: 32 101: 64 110: 64 111: 64
[2:0]	RW	DMATXBRSize	Threshold for generating the transmit FIFO request DMA transfer burst. That is, when the number of data segments in the transmit FIFO is less than or equal to the configured value (256 – DMATXBRSize), is valid. The width of the transmit FIFO is 16 bits. 000: 1 001: 4 010: 8 011: 16 100: 32 101: 64 110: 128 111: 128

SPIRXFIFOCR

SPIRXFIFOCR is a receive FIFO control register.

Offset Address	Register Name	Total Reset Value
0x02C	SPIRXFIFOCR	0x0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										RXINTSize			DMARXBRSize		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[15:6]	RW	reserved	Reserved.
[5:3]	RW	RXINTSize	Threshold for generating the receive FIFO request interrupt. That is, when the number of data segments in the transmit FIFO is less than or equal to the configured value (256 – RXINTSize), RXRIS is valid. The width of the receive FIFO is 16 bits. 000: 1 001: 4 010: 8 011: 16 100: 32 101: 64 110: 64 111: 64
[2:0]	RW	DMARXBRSize	Burst transfer threshold. When this threshold is reached, the receive FIFO asks the DMA to perform a burst transfer. That is, when number of data segments in the transmit FIFO is less than or equal to the value of DMARXBRSize, DMARXBREQ is valid. 000: 1 001: 4 010: 8 011: 16 100: 32 101: 64 110: 128 111: 224

13.3 UART

13.3.1 Overview

The universal asynchronous receiver transmitter (UART) interface is an asynchronous serial communication interface. It performs serial-to-parallel conversion on the data received from peripherals and transmits the converted data to the internal bus. It also performs parallel-to-serial conversion on the data that is transmitted to peripherals. The UART is mainly used to interconnect the Hi3531 with the UART of an external chip so that the two chips can communicate with each other.

The Hi3518A provides three UART units (UART0 to UART2), and the Hi3518C provides two UART units (UART0 and UART1).

- UART0: a two-wire UART for debugging
- UART1: a four-wire UART (for the Hi3518A) or three-wire UART (for the Hi3518C) for controlling the pan, tile, and zoom (PTZ). The Hi3518C has no CTSN signal.
- UART2: a two-wire UART for generating alarms or connecting to a universal UART device

13.3.2 Features

The UART unit has the following features:

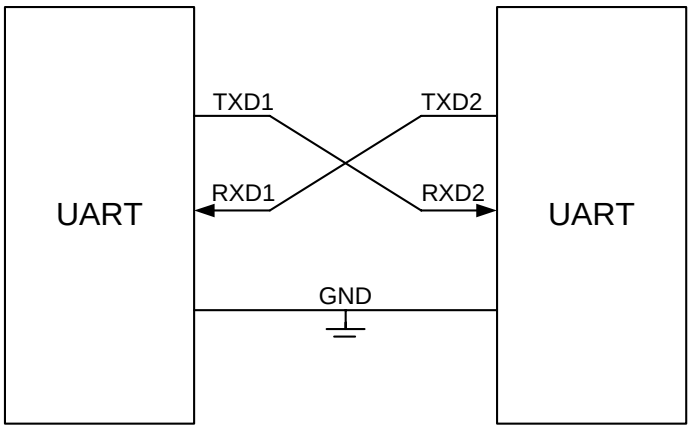
- Supports16x8-bit transmit first-in, first-out (FIFO) and 16x12-bit receive FIFO.
- Supports programmable widths for the data bit and stop bit. The width of the data bit can be set to 5 bits, 6 bits, 7 bits, or 8 bits and width of the stop bit can be set to 1 bit or 2 bits by programming.
- Supports parity check or no check.
- Supports the programmable transfer rate.
- Supports receive FIFO interrupts, transmit FIFO interrupts, receive timeout interrupts, and error interrupts.
- Supports the query of the raw interrupt status and the masked interrupt status.
- Allows the UART or the transmit/receive function of the UART to be disabled by programming to reduce power consumption.
- Allows the UART clock to be disabled to reduce power consumption.
- Supports DMA.

13.3.3 Function Description

Application Block Diagram

Figure 13-17 shows the typical application of the UART.

Figure 13-17 Typical application block diagram of the UART

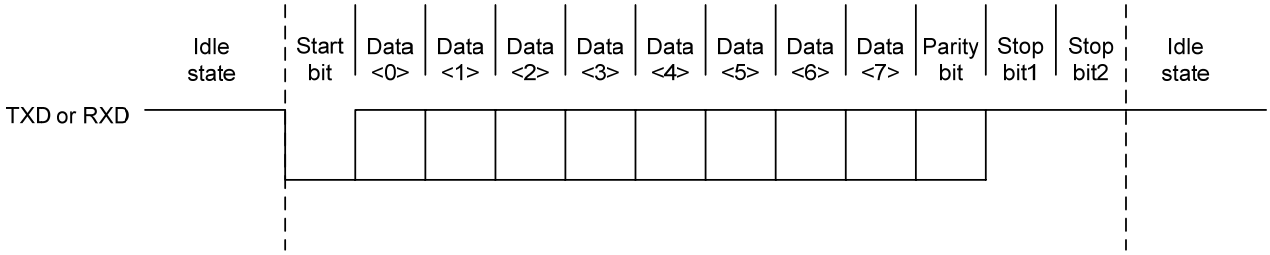


The UART serves as an asynchronous bidirectional serial bus. Through the UARTs connected by two data lines, a simplified and effective data transfer mode is implemented.

Function Principle

A frame transfer of the UART involves the start signal, data signal, parity bit, and stop signal, as shown in Figure 13-18. The data frame is output from the TXD end of one UART and then is input to the RXD end of the other UART.

Figure 13-18 Frame format of the UART



The definitions of the start signal, data signal, parity bit, and stop signal are as follows:

- Start signal (start bit)

  It is the start flag of a data frame. According to the UART protocol, the low level of the TXD signal indicates the start of a data frame. When the UART does not transmit data, the level must remain high.
- Data signal (data bit)

  The data bit width can be set to 5 bits, 6 bits, 7 bits, or 8 bits according to the requirements in different applications.
- Parity bit

  It is a 1-bit error correction signal. The UART parity bit can be an odd parity bit, even parity bit, or stick parity bit. The UART can enable and disable the parity bit. For details, see the description of the UART_LCR_H register.
- Stop signal (stop bit)

It is the stop bit of a data frame. The stop bit width can be set to 1 bit or 2 bits. The high level of TXD indicates the end of the data frame.

13.3.4 Operating Mode

13.3.4.1 Baud Rate Configuration

The operating baud rate of the UART can be set by configuring the registers UART_IBRD and UART_FBRD. The baud rate is calculated as follows:

Current baud rate = Frequency of the UART reference clock (1/2 bus clock frequency)/(16 x Frequency divider)

The clock frequency divider consists of the integral part and the fractional part that correspond to UART_IBRD and UART_FBRD respectively.

For example, assume that the frequency of the UART reference clock is 60 MHz. If UART_IBRD is set to 0x1E and UART_FBRD is set to 0x00, the current baud rate is calculated as follows: 60/(16 x 30) = 0.125 Mbit/s

The typical UART baud rates are 9600 bit/s, 14,400 bit/s, 19,200 bit/s, 38,400 bit/s, 57,600 bit/s, 76,800 bit/s, 115,200 bit/s, 230,400 bit/s, and 460,800 bit/s.

The following examples show how to calculate the clock divider and how to configure the clock divider register:

If the required baud rate is 230,400 bit/s and the frequency of the UART reference clock is 100 MHz, the clock divider is calculated as follows: $(100x10^6)/(16 \times 230,400) = 27.1267$. The integral part IBRD is 27 and the fractional part FBRD is 0.1267.

To calculate the value of the 6-bit UART_FBRD register, do as follows: calculate the value of *m* by using the following formula: $m = integer (FBRD \times 2^n + 0.5) = (0.1267 \times 2^6 + 0.5) = 8$(n = the width of UART_FBRD). Then set UART_IBRD to 0x001B and set UART_FBRD to 0x08.

If the fractional part of the frequency divider is set to 8, the actual divisor of the baud rate is 27 + 8/64 = 27.125, the baud rate is (100 x 16)/(16 x 27.125) = 230,414.75, and the error rate is (230,414.75 – 230,400)/230,400 x 100 = 0.006%.

The maximum error rate is 1/64 x 100 = 1.56% when the 6-bit UART_FBRD is used. If the value of *m* is 1, the total error rate is greater than 64 clock cycles.

13.3.4.2 Soft Reset

The UART controller can be separately reset by configuring the CRG registers.

- The UART0 controller can be separately reset by setting PERI_CRG57[uart0_srst_req] to 1.
- The UART1 controller can be separately reset by setting PPERI_CRG57[uart1_srst_req] to 1.
- The UART2 controller can be separately reset by setting PERI_CRG57[uart2_srst_req] to 1.

After reset, the configuration registers are restored to default values. Therefore, these registers must be initialized again.

13.3.4.3 Data Transfer in Interrupt or Query Mode

Initialization

The initialization is implemented as follows:

1. Write 0 to UART_CR bit[0] to disable the UART.
2. Write to UART_IBRD and UART_FBRD to configure the transfer rate.
3. Configure UART_CR and UART_LCR_H to set the UART operating mode.
4. Configure UART_IFLS to set the thresholds of transmit and receive FIFOs.
5. If the driver runs in interrupt mode, set UART_IMSC to enable the corresponding interrupt; if the driver runs in query mode, disable the generation of corresponding interrupts.
6. Write 1 to UART_CR bit[0] to enable the UART.

----End

Data Transmission

To transmit data, perform the following steps:

1. Write the data to be transmitted to UART_DR and start data transmission.
2. In query mode, check the TX_FIFO status by reading UART_FR bit[5] during the continuous data transmission. According to the TX_FIFO status, determine whether to transmit data to TX_FIFO. In interrupt mode, check the TX_FIFO status by reading the corresponding interrupt status bits and then determine whether to transmit data to TX_FIFO.
3. Check whether the UART transmits all data by reading UART_FR bit[7]. If UART_FR bit[7] is 1, the UART transmits all data.

----End

Data Reception

To receive data, perform the following steps:

- In query mode, detect the RX_FIFO status by reading UART_FR[rxfe] during data reception and then determine whether to read data from the RX_FIFO according to the RX_FIFO status.
- In interrupt mode, determine whether to read data from RX_FIFO according to corresponding interrupt status bits.

13.3.4.4 Data Transfer in DMA Mode

Initialization

The initialization is implemented as follows:

1. Write 0 to UART_CR[uarten] to disable the UART.
2. Write to UART_IBRD and UART_FBRD to configure the transfer rate.
3. Configure UART_CR and UART_LCR_H to set the UART operating mode.

4. Configure UART_IFLS to set the thresholds of transmit and receive FIFOs.
5. If the driver runs in interrupt mode, set UART_IMSC to enable the corresponding interrupts; if the driver runs in query mode, disable the generation of corresponding interrupts.
6. Write 1 to UART_CR[uarten] to enable the UART.

----End

Data Transmission

The following is an example using the DMA mode. To transmit data, perform the following steps:

1. Configure the DMA data channel, including the data transmission source, destination address, number of data segments to be transmitted, and transmission type. For details, see the description in section 3.5 "DMAC."
2. Set UART_DMACR to 0x2 to enable the DMA transmit function of the UART.
3. Check whether the data is transmitted completely based on the interrupt report status of the DMA. If all data is transmitted, disable the DMA transmit function of the UART.

----End

Data Reception

The following is an example using the DMA mode. To receive data, perform the following steps:

1. Configure the DMA data channel, including data transfer source and destination addresses, data receive area address, number of data segments to be transmitted, and transfer type.
2. Set UART_DMACR to 0x1 to enable the DMA receive function of the UART.
3. Check whether the data is received completely by querying the DMA status. If all data is received, disable the DMA receive function of the UART.

----End

13.3.5 Register Summary

The Hi3518A provides three UART units: UART0, UART1, and UART2. The Hi3518C provides two UART units: UART0 and UART1. Their base addresses are as follows:

- The base address of UART0 registers is 0x2008_0000.
- The base address of UART1 registers is 0x2009_0000.
- The base address of UART2 registers is 0x200A_0000.

Table 13-4 describes the UART registers.

Table 13-4 Summary of UART registers

Offset Address	Register	Description	Page
0x000	UART_DR	Data register	13-38
0x004	UART_RSR	Receive status register or error clear register	13-39
0x008 – 0x014	RESERVED	Reserved	-
0x018	UART_FR	Flag register	13-40
0x01C – 0x020	RESERVED	Reserved	-
0x024	UART_IBRD	Integral baud rate register	13-41
0x028	UART_FBRD	Fractional baud rate register	13-42
0x02C	UART_LCR_H	Transfer mode control register	13-43
0x030	UART_CR	Control register	13-44
0x034	UART_IFLS	Interrupt FIFO threshold select register	13-46
0x038	UART_IMSC	Interrupt mask register	13-47
0x03C	UART_RIS	Raw interrupt status register	13-48
0x040	UART_MIS	Masked interrupt status register	13-49
0x044	UART_ICR	Interrupt clear register	13-50
0x048	UART_DMACR	DMA control register	13-51

13.3.6 Register Description

UART_DR

UART_DR is a UART data register that stores the received data and the data to be transmitted. The receive status can be queried by reading this register.

Offset Address	Register Name	Total Reset Value
0x000	UART_DR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				oe	be	pe	fe	data							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:12]	-	reserved	Reserved.

[11]	RO	oe	Overflow error. 0: No overflow error occurs. 1: An overflow error occurs. That is, a data segment is received when the receive FIFO is full.
[10]	RO	be	Break error. 0: No break error occurs. 1: A break error occurs. That is, the time of receive data input signal keeping low is longer than a full word transfer. A full word consists of a start bit, a data bit, a parity bit, and a stop bit.
[9]	RO	pe	Parity error. 0: No parity error occurs. 1: A parity error occurs.
[8]	RO	fe	Frame error. 0: No frame error occurs. 1: A frame error (namely, stop bit error) occurs.
[7:0]	RW	data	Data received and to be transmitted.

UART_RSR

UART_RSR is a receive status register or error clear register.

- It acts as the receive status register when being read.
- It acts as the error clear register when being written.

You can query the receive status by reading UART_DR. The status information about the break, frame, and parity read from UART_DR has priority over that read from UART_RSR. That is, the status read from UART_DR changes faster than that read from UART_RSR.

UART_RSR is reset when any value is written to it.

Offset Address	Register Name	Total Reset Value
0x004	UART_RSR	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved				oe	be	pe	fe
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:4]	-	reserved	Reserved.

[3]	RW	oe	Overflow error. 0: No overflow error occurs. 1: An overflow error occurs. When the FIFO is full, the next data segment cannot be written to the FIFO and an overflow occurs in the shift register. Therefore, the contents in the FIFO are valid. In this case, the CPU must read the data immediately to spare the FIFO.
[2]	RW	be	Break error. 0: No break error occurs. 1: A break error occurs. A break error occurs when the time of the receive data signal keeping low is longer than a full word transfer. A full word consists of a start bit, a data bit, a parity bit, and a stop bit.
[1]	RW	pe	Parity error. 0: No parity error occurs. 1: A parity error occurs when the received data is checked. In FIFO mode, the error is associated with the data at the top of the FIFO.
[0]	RW	fe	Frame error. 0: No frame error occurs. 1: The stop bit of the received data is incorrect. The valid stop bit is 1.

UART_FR

UART_FR is a UART flag register.

Offset Address	Register Name	Total Reset Value
0x018	UART_FR	0x0012

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								txfe	rxff	txff	rxfe	busy	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

Bits	Access	Name	Description
[15:8]	-	reserved	Reserved.

[7]	RO	txfe	The definition of the bit is determined by the status of UART_LCR_H [fen]. If UART_LCR_H [fen] is 0, this bit is set to 1 when the transmit holding register is empty. If UART_LCR_H [fen] is 1, the bit is set to 1 when the transmit FIFO is empty.
[6]	RO	rxff	The definition of the bit is determined by the status of UART_LCR_H [fen]. If UART_LCR_H [fen] is 0, this bit is set to 1 when the receive holding register is full. If UART_LCR_H [fen] is 1, this bit is set to 1 when the receive FIFO is full.
[5]	RO	txff	The definition of the bit is determined by the status of UART_LCR_H [fen]. If UART_LCR_H [fen] is 0, this bit is set to 1 when the transmit holding register is full. If UART_LCR_H [fen] is 1, the bit is set to 1 when the transmit FIFO is full.
[4]	RO	rxfe	The definition of the bit is determined by the status of UART_LCR_H [fen]. If UART_LCR_H [fen] is 0, this bit is set to 1 when the receive holding register is empty. If UART_LCR_H [fen] is 1, this bit is set to 1 when the receive FIFO is empty.
[3]	RO	busy	UART busy/idle status. 0: The UART is idle or data transmission is complete. 1: The UART is busy in transmitting data. If the bit is set to 1, the status is kept until the entire byte (including all stop bits) is transmitted from the shift register. Regardless of whether the UART is enabled, this bit is set to 1 when the transmit FIFO is not empty.
[2:0]	-	reserved	Reserved.

UART_IBRD

UART_IBRD is an integral baud rate register.

Offset Address	Register Name	Total Reset Value
0x024	UART_IBRD	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	baud divint															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:0]	RW	baud divint	Clock frequency divider corresponding to the integral part of the baud rate. All bits are cleared after reset.

UART_FBRD

UART_FBRD is a fractional baud rate register.

CAUTION

- The values of UART_IBRD and UART_FBRD can be updated only after the current data is transmitted and received completely.
- The minimum clock frequency divider is 1 and the maximum divider is 65,535 (2^{16} – 1). That is, UART_IBRD cannot be 0 and UART_FBRD is ignored if UART_IBRD is 0. Similarly, if UART_IBRD is equal to 65,535 (0xFFFF), UART_IBRD must be 0. If UART_FBRD is greater than 0, the data fails to be transmitted or received.
- Assume that UART_FBRD is set to 0x1E and UART_IBRD is set to 0x01. This indicates that the integral part of the clock frequency divider is 30 and the fractional part of the clock frequency divider is 0.015625. Therefore, the clock frequency divider is 30.015625.
- Baud rate of the UART = Internal bus frequency/(16 x clock divider) = Internal bus frequency/(16 x 30.015625).

Offset Address	Register Name	Total Reset Value
0x028	UART_FBRD	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved		baud divfrac					
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	-	reserved	Reserved.
[5:0]	RW	band divfrac	Clock frequency divider corresponding to the fractional part of the baud rate. All bits are cleared after reset.

UART_LCR_H

UART_LCR_H is a transfer mode control register. The registers UART_LCR_H, UART_IBRD, and UART_FBRD are combined to form a 30-bit register. If UART_IBRD and UART_FBRD are updated, UART_LCR_H must be updated at the same time.

Offset Address	Register Name	Total Reset Value
0x02C	UART_LCR_H	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								sps	wlen		fen	stp2	eps	pen	brk
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:8]	-	reserved	Reserved.
[7]	RW	sps	Parity select. When bit 1, bit 2, and bit 7 of this register are set to 1, the parity bit is 0 during transmission and detection. When bit 1 and bit 7 of this register are set to 1 and bit 2 is set to 0, the parity bit is 1 during transmission and detection. When bit 1, bit 2, and bit 7 are cleared, the stick parity bit is disabled.
[6:5]	RW	wlen	Count of bits in a transmitted or received frame. 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits
[4]	RW	fen	Transmit/receive FIFO enable. 0: disabled 1: enabled
[3]	RW	stp2	2-bit stop bit at the end of a transmitted frame. 0: There is no 2-bit stop bit at the end of the transmitted frame. 1: There is a 2-bit stop bit at the end of the transmitted frame. The receive logic does not check for the 2-bit stop bit during data reception.

[2]	RW	eps	Parity select during data transmission and reception. 0: The odd parity is generated or checked during data transmission and reception. 1: The even parity is generated or checked during data transmission and reception. When UART_LCR_H [fen] is 0, this bit becomes invalid.
[1]	RW	pen	Parity enable. 0: The parity is disabled. 1: The parity is generated on the transmit side and checked on the receive side.
[0]	RW	brk	Break transmit. 0: invalid 1: After the current data transmission is complete, UTXD outputs low level continuously. Note: This bit must retain 1 during the period of at least two full frames to ensure the break command is executed properly. In general, the bit must be set to 0.

UART_CR

UART_CR is a UART control register.

To configure UART_CR, perform thollowing steps:

1. Write 0 to UART_CR[uarten] to disable the UART.
2. Wait until the current data transmission or reception is complete.
3. Clear UART_LCR_H [fen].
4. Configure UART_CR.
5. Write 1 to UART_CR[uarten] to enable the UART.

----End

Offset Address	Register Name	Total Reset Value
0x030	UART_CR	0x0300

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ctsen	rtsen	reserved		rts	dtr	rxe	txe	lbe	reserved						uarten
Reset	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15]	RW	ctsen	CTS hardware flow control enable. 0: disabled 1: enabled. Data is transmitted only when the nUARTCTS signal is valid.
[14]	RW	rtsen	RTS hardware flow control enable. 0: disabled 1: enabled. The data reception request is raised only when the receive FIFO has available space.
[13:12]	-	reserved	Reserved.
[11]	RW	rts	Request transmit. This bit is the inversion of the status output signal nUARTRTS of the UART modem. 0: The output signal retains. 1: When this bit is set to 1, the output signal is 0.
[10]	RW	dtr	Data transmit ready. This bit is the inversion of the status output signal nUARTDTR of the UART modem. 0: The output signal retains. 1: When this bit is set to 1, the output signal is 0.
[9]	RW	rxe	UART receive enable. 0: disabled 1: enabled If the UART is disabled during data reception, the current data reception is stopped abnormally.
[8]	RW	txe	UART transmit enable. 0: disabled 1: enabled If the UART is disabled during data transmission, the current data transmission is stopped abnormally.

[7]	RW	lbe	Loopback enable. 0: disabled 1: UARTTXD is looped back to UARTRXD.
[6:1]	-	reserved	Reserved.
[0]	RW	uarten	UART enable. 0: disabled 1: enabled If the UART is disabled during data reception and transmission, the data transfer is stopped abnormally.

UART_IFLS

UART_IFLS is an interrupt FIFO threshold select register. It is used to set a threshold for triggering a FIFO interrupt (UART_TXINTR or UART_RXINTR).

Offset Address	Register Name	Total Reset Value
0x034	UART_IFLS	0x0012

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										rxiflsel			txiflsel		
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

Bits	Access	Name	Description
[15:6]	-	reserved	Reserved.
[5:3]	RW	rxiflsel	Receive interrupt FIFO threshold select. A receive interrupt is triggered when any of the following conditions is met: 000: receive FIFO ≥ 1/8 full 001: receive FIFO ≥ 1/4 full 010: receive FIFO ≥ 1/2 full 011: receive FIFO ≥ 3/4 full 100: receive FIFO ≥ 7/8 full 101 – 111: reserved

[2:0]	RW	txiflsel	Transmit interrupt FIFO threshold select. A transmit interrupt is triggered when any of the following conditions is met: 000: transmit FIFO ≤ 1/8 full 001: transmit FIFO ≤ 1/4 full 011: transmit FIFO ≤ 3/4 full 010: transmit FIFO ≤ 1/2 full 100: transmit FIFO ≤ 7/8 full 101 – 111: reserved

UART_IMSC

UART_IMSC is an interrupt mask register. It is used to mask interrupts.

Offset Address	Register Name	Total Reset Value
0x038	UART_IMSC	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					oeim	beim	peim	feim	rtim	txim	rxim	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:11]	-	reserved	Reserved.
[10]	RW	oeim	Mask status of the overflow error interrupt. 0: masked 1: not masked
[9]	RW	beim	Mask status of the break error interrupt. 0: masked 1: not masked
[8]	RW	peim	Mask status of the parity interrupt. 0: masked 1: not masked
[7]	RW	feim	Mask status of the frame error interrupt. 0: masked 1: not masked
[6]	RW	rtim	Mask status of the receive timeout interrupt. 0: masked 1: not masked

[5]	RW	txim	Mask status of the transmit interrupt. 0: masked 1: not masked
[4]	RW	rxim	Mask status of the receive interrupt. 0: masked 1: not masked
[3:0]	-	reserved	Reserved.

UART_RIS

UART_RIS is a raw interrupt status register. The contents of this register are not affected by the UART_IMSC register.

Offset Address	Register Name	Total Reset Value
0x03C	UART_RIS	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					oeris	beris	peris	feris	rtris	txris	rxris	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:11]	-	reserved	Reserved.
[10]	RO	oeris	Status of the raw overflow error interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RO	beris	Status of the raw break error interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	peris	Status of the raw parity interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[7]	RO	feris	Status of the raw error interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[6]	RO	rtris	Status of the raw receive timeout interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

[5]	RO	txris	Status of the raw transmit interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RO	rxris	Status of the raw receive interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[3:0]	-	reserved	Reserved.

UART_MIS

UART_MIS is a masked interrupt status register. The contents of this register are the results obtained after the raw interrupt status is ANDed with the interrupt mask status.

Offset Address	Register Name	Total Reset Value
0x040	UART_MIS	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					oemis	bemis	pemis	femis	rtmis	txmis	rxmis	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:11]	-	reserved	Reserved.
[10]	RO	oemis	Status of the masked overflow error interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RO	bemis	Status of the masked break error interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	pemis	Status of the masked parity interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[7]	RO	femis	Status of the masked error interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[6]	RO	rtmis	Status of the masked receive timeout interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

[5]	RO	txmis	Status of the masked transmit interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RO	rxmis	Status of the masked receive interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[3:0]	-	reserved	Reserved.

UART_ICR

UART_ICR is an interrupt clear register. When 1 is written to it, the corresponding interrupt is cleared. Writing 0 has no effect.

Offset Address	Register Name	Total Reset Value
0x044	UART_ICR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					oeic	beic	peic	feic	rtic	txic	rxic	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:11]	-	reserved	Reserved.
[10]	WO	oeic	Overflow error interrupt clear. 0: invalid 1: cleared
[9]	WO	beic	Break error interrupt clear. 0: invalid 1: cleared
[8]	WO	peic	Parity interrupt clear. 0: invalid 1: cleared
[7]	WO	feic	Error interrupt clear. 0: invalid 1: cleared
[6]	WO	rtic	Receive timeout interrupt clear. 0: invalid 1: cleared

[5]	WO	txic	Transmit interrupt clear. 0: invalid 1: cleared
[4]	WO	rxic	Receive interrupt clear. 0: invalid 1: cleared
[3:0]	-	reserved	Reserved.

UART_DMACR

UART_DMACR is a DMA control register. It is used to control whether to enable the DMA operation of the transmit and receive FIFOs.

Offset Address	Register Name	Total Reset Value
0x048	UART_DMACR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													dmaonerr	txdmae	rxdmae
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:3]	-	reserved	Reserved.
[2]	RW	dmaonerr	Receive channel DMA enable when the UART error interrupt (UARTEINTR) occurs. 0: When UARTEINTR is valid, the DMA output request (UARTRXDMASREQ or UARRTXDMABREQ) of the receive channel is valid. 1: When UARTEINTR is valid, the DMA output request (UARTRXDMASREQ or UARRTXDMABREQ) of the receive channel is invalid.
[1]	RW	txdmae	Transmit FIFO DMA enable. 0: disabled 1: enabled
[0]	RW	rxdmae	Receive FIFO DMA enable. 0: disabled 1: enabled

13.4 IR Interface

NOTE

This section applies only to the Hi3518A.

13.4.1 Overview

The infrared (IR) module receives data over the IR interface.

13.4.2 Features

The IR module has the following features:

- Allows to disable the IR receive module by using software.
- Supports two operating modes:
  - Mode 0: supports decoding in four formats (including NEC with simple repeat code, NEC with full repeat code, SONY, and TC9012), error detection on received data, and IR wakeup.
  - Mode 1: supports the symbol level width detection in any data format.
- In mode 0, supports the receive data overflow interrupt, receive data frame format error interrupt, receive data frame interrupt, key release interrupt, and combined interrupt.
- In mode 1, supports the receive symbol overflow interrupt, receive symbol interrupt, symbol timeout interrupt, and combined interrupt.
- Supports the query of the raw interrupt status and the masked interrupt status.
- Supports interrupt clear and mask (write to clear).
- Supports IR wakeup.
- Supports the reference clock frequency ranging from 1 MHz to 128 MHz and controls the clock frequency divider by software programming, enabling the frequency of the working clock to be prescaled to 1 MHz.

13.4.3 Function Description

The IR module receives infrared signals transmitted by the infrared remote control, decodes the signals, and then transmits the decoded signals to the ARM system. The ARM system performs corresponding operations according to the received codes, which implements expected functions. The IR module connects to the APB of the ARM subsystem. When the chip is in the low-power state (the CPU is at a low frequency), the IR module generates an interrupt after receiving a complete frame, and transmits the interrupt to the CPU. In this way, the IR wake function is implemented.

The analysis of the signals transmitted by various infrared remote controls shows that the lead codes in the infrared commands vary according to remote controls. In addition, the subsequent control commands and the bits of command codes are also different. This is because infrared remote controls are not designed based on a unified infrared remote control standard. The basic encoding principles, however, are the same. That is, the pulses with different periods and duty ratios are used to represent 0 and 1. The duty ratios and pulse cycles may vary according to remote controls. Based on preceding differences, the code formats of the infrared data are classified into NEC with simple repeat code, NEC with full repeat code, TC9012 code, and SONY code.

Table 13-5 to Table 13-7 describe the code formats of the received infrared data.

Table 13-5 Code formats of the received infrared data (NEC with simple repeat code)

Data Format		**NEC with Simple Repeat Code**			
		uPD6121G	**D6121/BU5777/D1913**	**LC7461M-C13**	**AEHA**
Lead code (10 μs)	LEAD_S	900	900	900	337.6
	LEAD_E	450	450	450	168.8
Bit0 (10 μs)	B0_L	56	56	56	42.2
	B0_H	56	56	56	42.2
Bit1 (10 μs)	B1_L	56	56	56	42.2
	B1_H	169	169	169	126.6
Simple repeat code (10 μs)	SLEAD_S	900	900	900	337.6
	SLEAD_E	225	225	225	337.6
Burst (10 μs)		55	55	55	42.2
Frame length (10 μs)		108,00	10,800	10,800	8,777.6 – 12,828.8
Valid data bit		32	32	42	48

Table 13-6 Code formats of the received infrared data (NEC with full repeat code)

Data Format		**NEC with Full Repeat Code**						
		uPD6121G	**LC7461M-C13**	**MN6024-C5D6**	**MN6014-C6D6**	**MATNEW**	**MN6030**	**PANASONIC**
Lead code (10 μs)	LEAD_S	900	900	337.6	349.2	348.8	349	352
	LEAD_E	450	450	337.6	349.2	374.4	349	352
Bit 0 (10 μs)	B0_L	56	56	84.4	87.3	43.6	87.3	88
	B0_H	56	56	84.4	87.3	43.6	87.3	88
Bit 1 (10 μs)	B1_L	56	56	84.4	87.3	43.6	87.3	88
	B1_H	169	169	253.2	174.6	130.8	261.9	264
Simple repeat code (10 μs)	SLEAD_S	None	None	None	None	None	None	None
	SLEAD_E							
Burst (10 μs)		55	55	84.4	87.3	43.6	87.3	88
Frame length (10 μs)		10,800	10,800	10,130	10,470	12,413.6 – 16,594.4	10,500	10,400

Data Format	NEC with Full Repeat Code						
	uPD6121G	LC7461 M-C13	MN602 4-C5D6	MN6014 -C6D6	MATNEW	MN6030	PANA SONIC
Valid data bit	32	42	22	24	48	22	22

Table 13-7 Code formats of the received infrared data (TC9012 code and SONY code)

Data Format		TC9012	SONY			
		TC9012F/9243	SONY-D7C5	SONY-D7C6	SONY-D7C8	SONY-D7C13
Lead code (10 µs)	LEAD_S	450	240	240	240	240
	LEAD_E	450	60	60	60	60
Bit0 (10 µs)	B0_L	56	60	60	60	60
	B0_H	56	60	60	60	60
Bit1 (10 µs)	B1_L	56	120	120	120	120
	B1_H	169	60	60	60	60
Simple repeat code (10 µs)	SLEAD_S	None	None	None	None	None
	SLEAD_E					
Burst (10 µs)		56	None	None	None	None
Frame length (10 µs)		10,800	4500	4500	4500	4500
Valid data bit		32	12	13	15	20

13.4.3.1 NEC with Simple Repeat Code

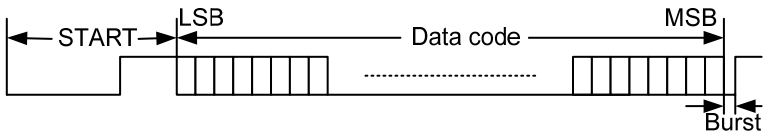
Frame Format

The NEC with simple repeat code consists of the following:

- Start code (lead code): Consists of a start code (low level) and an end code (high level).
- Data code: The valid bits and the definition of each bit depend on specific code format. During data code reception, its LSB is received first.
- Burst signal: It is used to receive the last data bit.

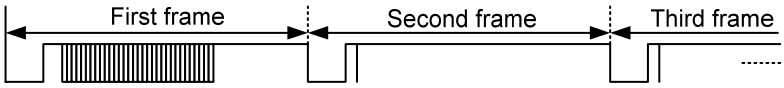
Figure 13-19 shows the frame format of transmitting a single NEC with simple repeat code.

Figure 13-19 Frame format for transmitting a single NEC with simple repeat code



If a complete data frame is received after the key is held down for more than one frame length, the subsequently received data frame consists only of a simple lead code and a burst signal. The lead code also consists of a start code (low level) and an end code (high level). Figure 13-20 shows the frame format for transmitting NEC with simple repeat codes by pressing the key continuously.

Figure 13-20 Frame format for transmitting NEC with simple repeat codes by pressing the key continuously



Code Format

Figure 13-21 shows the definitions of bit0 and bit1 of the NEC with simple repeat code.

Figure 13-21 Definitions of bit0 and bit1 of the NEC with simple repeat code

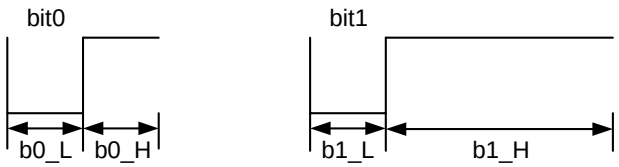


Figure 13-22 shows the format for transmitting a single NEC with simple repeat code. Figure 13-23 shows the format for transmitting consecutive NEC with simple repeat codes.

Figure 13-22 Format for transmitting a single NEC with simple repeat code

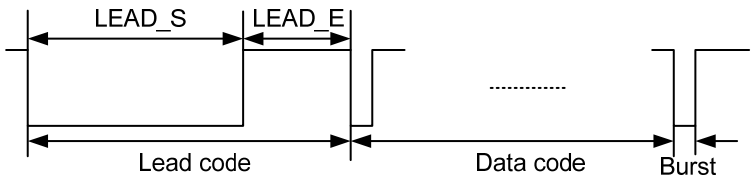
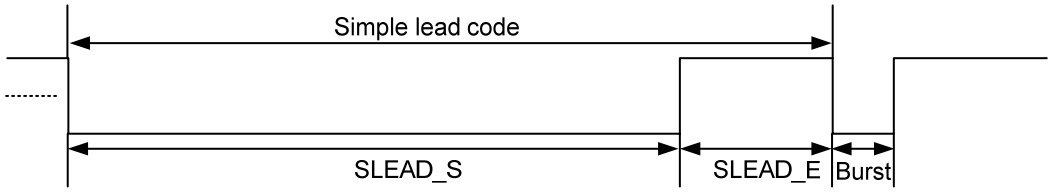


Figure 13-23 Code format for transmitting consecutive NEC with simple repeat codes



NOTE

The pulse width of the high and low levels and the frame length depend on specific code formats. See Table 13-5 to Table 13-7.

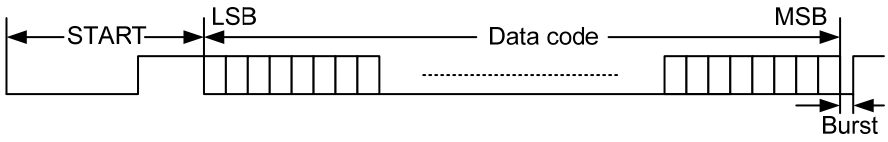
The frame length must be less than or equal to 160 ms. Otherwise, the simple lead code cannot be identified.

13.4.3.2 NEC with Full Repeat Code

Frame Format

The data format of the NEC with full repeat code consists of the following parts: START (lead code), data code, and burst. START (lead code): Consists of a start code (low level) and an end code (high level). Data code: The valid bits and the definition of each bit are determined by the specific code format. During data code reception, the LSB is received first. Burst signal: It is used to receive the last data bit. Figure 13-24 shows the frame format for transmitting a single NEC with full repeat code.

Figure 13-24 Frame format for transmitting a single NEC with full repeat code



If a complete data frame (first frame) is received after the key is held down for more than one frame length, the subsequently received data frame is still a complete data frame. That is, the first frame is transmitted repeatedly based on the frame length. Figure 13-25 shows the frame format for transmitting NEC with full repeat codes by pressing the key continuously.

Figure 13-25 Frame format for transmitting NEC with full repeat codes by pressing the key continuously

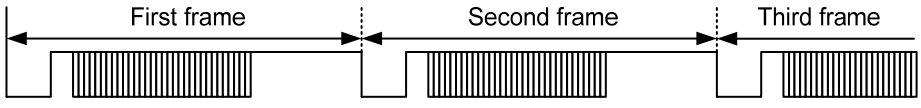


Figure 13-24 and Figure 13-25 show that the only difference between the NEC with simple repeat code and the NEC with full repeat code is the format of the repeat frame. For the NEC with simple repeat code, the simple lead code is transmitted; for the NEC with full repeat code, the complete frame is transmitted. That is, the first frame and the repeat frame are the same.

Code Format

Figure 13-26 shows the definitions of bit0 and bit1 of the NEC with full repeat code.

Figure 13-26 Definitions of bit0 and bit1 of the NEC with full repeat code

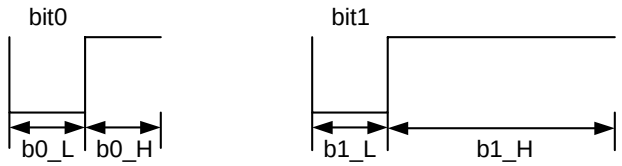
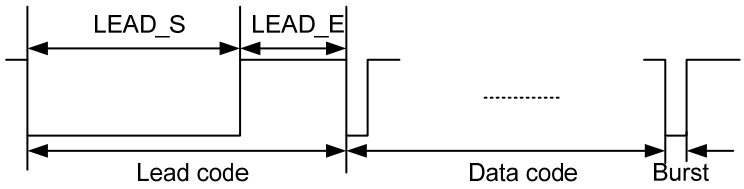


Figure 13-27 shows the format for transmitting a single NEC with full repeat code.

Figure 13-27 Format for transmitting a single NEC with full repeat code



NOTE

The pulse width of the high and low levels and the frame length depend on specific code formats. See Table 13-5 to Table 13-7.

13.4.3.3 TC9012 Code

Frame Format

CAUTION

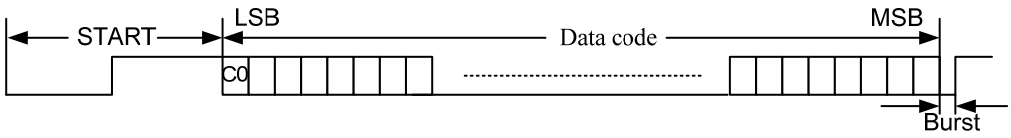
According to the features of the TC9012 code, the first bit of all key codes must be all 1s or all 0s. Otherwise, unnecessary frames are generated when the key are pressed continuously.

The TC9012 code consists of the following parts:

- START code (lead code): Consists of a start code (low level) and an end code (high level).
- Data code: The valid bits and the definition of each bit depend on the specific code pattern. During data code reception, its LSB is received first.
- Burst signal: It is used to receive the last data bit.

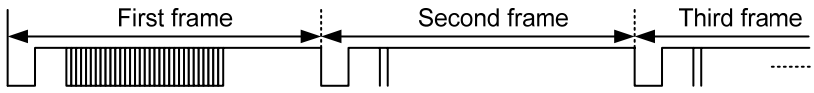
Figure 13-28 shows the frame format for transmitting a single TC9012 code.

Figure 13-28 Frame format for transmitting a single TC9012 code



When a complete data frame is received after the key is held down for more than one frame length, the subsequently received data frame consists of a lead code, a data bit, and a burst signal. The lead code also consists of a start code (low level) and an end code (high level). The data bit is the complement of the first data bit (C0) received in the previous frame. Figure 13-29 shows the frame format for transmitting TC9012 codes by pressing the key continuously.

Figure 13-29 Frame format for transmitting TC9012 codes by pressing the key continuously



Code Format

Figure 13-30 shows the definitions of bit0 and bit1 of the TC9012 code.

Figure 13-30 Definitions of bit0 and bit1 of the TC9012 code

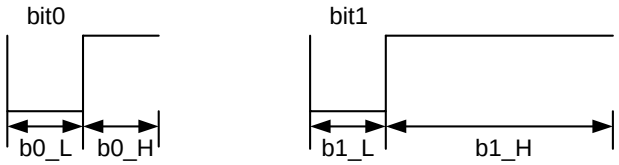


Figure 13-31 shows the format for transmitting a single TC9012 code.

Figure 13-31 Format for transmitting a single TC9012 code

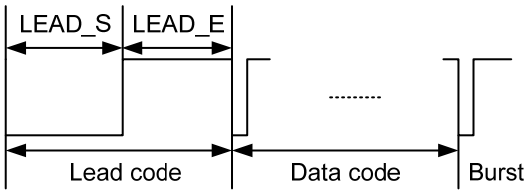


Figure 13-32 shows the format for transmitting consecutive TC9012 codes when C0 is 1.

Figure 13-32 Format for transmitting consecutive TC9012 codes (C0 = 1)

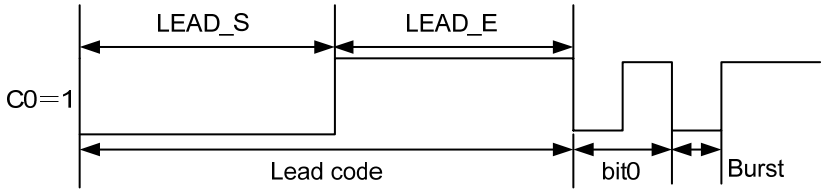
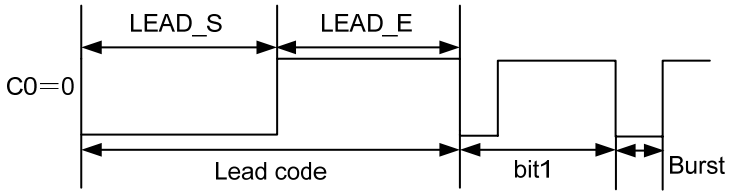


Figure 13-33 shows the format for transmitting consecutive TC9012 codes when C0 is 0.

Figure 13-33 Format for transmitting consecutiveTC9012 codes (C0 = 0)



NOTE

The pulse width of the high level and low level and the frame length depend on specific code patterns. For details, see Table 13-5 to Table 13-7. In addition, the frame length must be less than or equal to 160 ms. Otherwise, the repeat frame cannot be identified.

13.4.3.4 SONY Code

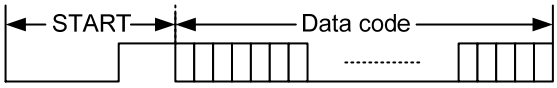
Frame Format

A SONY code consists of the following parts:

- START code (lead code): Consists of a start code (low level) and an end code (high level).
- Data code: The valid bits and the definition of each bit are determined by the specific code pattern.

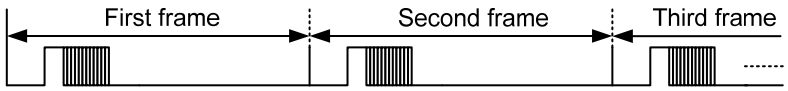
During reception, the LSB is received first. Figure 13-34 shows the frame format for transmitting a single SONY code.

Figure 13-34 Frame format for transmitting a single SONY code



When a complete data frame is received after the key is pressed for more than one frame length, the subsequently received data frame is also a complete data frame. Figure 13-35 shows the frame format for continuously transmitting SONY codes by pressing the key.

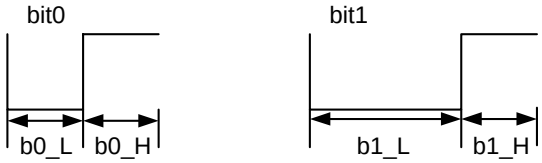
Figure 13-35 Frame format for continuously transmitting SONY codes by pressing the key



Code Format

Figure 13-36 shows the definitions of bit0 and bit1 of a SONY code.

Figure 13-36 Definitions of bit0 and bit1 of a SONY code



NOTE

The pulse width of the high level and low level and the frame length depend on specific code patterns. For details, see Table 13-5 to Table 13-7.

13.4.4 Operating Mode

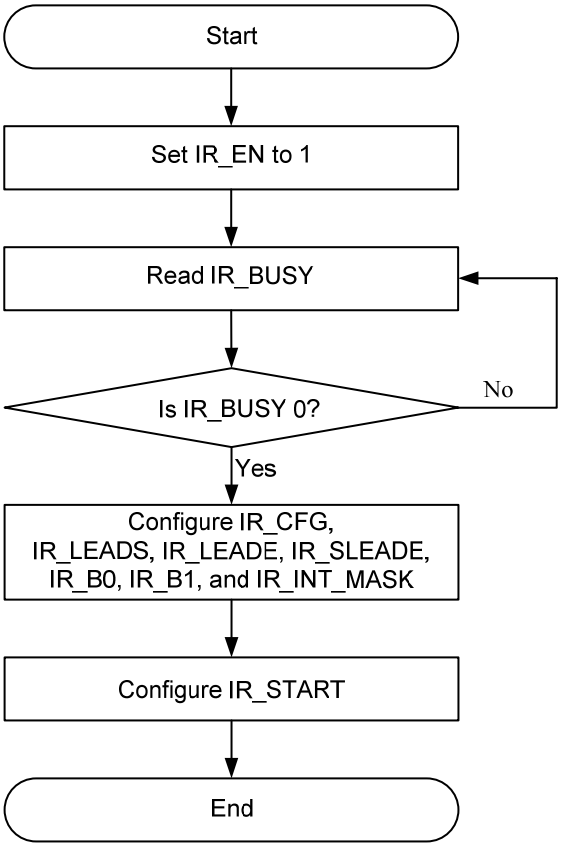
Soft Reset

When CRG_PERCTRL57[ir_srst_req] is set to 1, the IR module is soft-reset separately. After reset, each configuration register is restored its default value. Therefore, these registers must be reinitialized.

Instances of Configuring Registers

Figure 13-37 shows the process of initializing the IR module.

Figure 13-37 Process of initializing the IR module

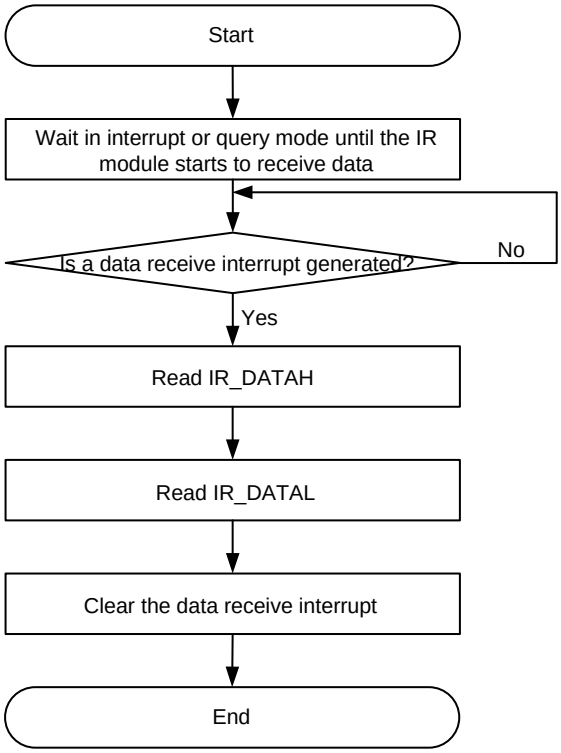


To initialize the IR module, perform the following steps:

1. Select the address space of the IR module.
2. Set IR_EN bit [0] to 1 to enable the IR receive module.
3. Read
4. IR_BUSY to check the current status of the IR module.
   - If the value of
   - IR_BUSY is 1, the IR module is busy. Then continue to read
   - IR_BUSY. Note that configuring other control registers of the IR module by using software has no effect in this case.
   - If the value of is 0, the IR module is idle. Then go to 5.
5. Configure IR_CFG, IR_LEADS, IR_LEADE, IR_SLEADE, IR_B0, IR_B1, and IR_INT_MASK. Note: You can update corresponding registers as required. If the registers are not updated, the original values are retained.
6. Configure IR_STARTafter all IR control registers are configured. This is because IR_START is used to generate the start signal. If IR_START is configured, the IR module starts to receive infrared data based on the values of IR control registers.

----End

Figure 13-38 Process of reading the decoded data



To read the decoded data, perform the following steps:

1. Select the address space of the IR module.
2. Wait in interrupt or query mode until data frames are received.
   - In interrupt mode, when the CPU receives an interrupt request signal from the IR module, read the value of IR_INT_STATUS[intms_rcv]. If the value is 1, the IR module receives a data frame. Then, go to 3. If the value is 0, repeat 2 to wait for an interrupt.
   - In query mode, continuously read the value of IR_INT_STATUS[intrs_rcv] by using software or read the value at intervals. If the value is 1, the IR module receives a data frame. Then, go to 3. If the value is 0, the IR module does not receive any data frame. Then, repeat 2 to continue the query.
3. Read IR_DATAH. If the number of data bits in one frame is less than or equal to 32, skip this step.
4. Read IR_DATAL.
5. Clear the data receive interrupt.

   ----End

13.4.5 Register Summary

Table 13-8 describes IR registers.

Table 13-8 Summary of IR registers (base address: 0x2007_0000)

Offset Address	Register	Description	Page
0x000	IR_EN	IR receive enable control register	13-63
0x004	IR_CFG	IR configuration register	13-64
0x008	IR_LEADS	Lead code start bit margin configuration register (valid when IR_CFG[ir_mode] is 0 only)	13-66
0x00C	IR_LEADE	Lead code end bit margin configuration register (valid when IR_CFG[ir_mode] is 0 only)	13-67
0x010	IR_SLEADE	Simple lead code end bit margin configuration register (valid when IR_CFG[ir_mode] is 0 only)	13-68
0x014	IR_B0	Data 0 level judge margin configuration register (used only when IR_CFG[ir_mode] is 0)	13-69
0x018	IR_B1	Data 1 level judge margin configuration register (used only when IR_CFG[ir_mode] is 0)	13-71
0x01C	IR_BUSY	Configuration busy flag register	13-72
0x020	IR_DATAH	Upper 16-bit IR receive decoded data register (IR_CFG[ir_mode] = 0) or symbol count register in the symbol FIFO (IR_CFG[ir_mode] = 1)	13-72
0x024	IR_DATAL	Lower 32-bit IR receive decoded data register (IR_CFG[ir_mode] = 0) or IR received symbol width register (IR_CFG[ir_mode] = 1)	13-73
0x028	IR_INT_MASK	IR interrupt mask register	13-74
0x02C	IR_INT_STATUS	IR interrupt status register	13-76
0x030	IR_INT_CLR	IR interrupt clear register	13-78
0x034	IR_START	IR start configuration register	13-79

13.4.6 Register Description

IR_EN

IR_EN is an IR receive enable control register.

CAUTION

Before configuring other registers, you must set IR_EN[ir_en] to 1 by using software. When IR_EN[ir_en] is 0, other registers are read-only and the read values are their reset values.

Offset Address	Register Name	Total Reset Value
0x000	IR_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															ir_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	ir_en	IR receive module enable. 0: disabled 1: enabled.

IR_CFG

IR_CFG is an IR configuration register.

CAUTION

Before configuring this register, you must set

IR_BUSY[ir_busy] to 0 and set IR_EN[ir_en] to 1. Otherwise, the original value is retained after configuration.

The reference clock frequency supported by the IR module ranges from 1 MHz to 128 MHz. The relationship between the frequency and the clock frequency divider ir_freq is as follows:

- When the reference clock frequency is 1 MHz, ir_freq must be set to 0x00.
- If the reference clock frequency is 128 MHz, ir_freq must be set to 0x7F.

When the frequency of the IR reference clock is not an integer ranging from 1 MHz to 128 MHz, the clock frequency divider is rounded off. For example, if the reference clock frequency is 12.1 MHz, the clock frequency divider is 0x0B; if the reference clock frequency is 12.8 MHz, the clock frequency divider is 0x0C.

The relationship between the frequency offset and the count deviation is as follows: If the base frequency is f and the frequency variation is D_f, the frequency offset ratio is D_f/f. If the count deviation of the counter is Dcnt, and the judge level width is s (in μs), the count

deviation Dcnt is calculated as follows: Dcnt = |0.1 x s x ratio|Therefore, when the clock has frequency offset, the valid range of the parameter value needs to be changed. If the frequency increases, the corresponding margin range is changed to [min + Dcnt, max + Dcnt]. Where, min and max indicate the margins without frequency offset. If the frequency decreases, the offset range is changed to [min – Dcnt, max – Dcnt]. Take the margin of the start bit in the lead code as an example. If the base frequency is 100 MHz, and the frequency increases by 0.1 MHz, then the ratio is 0.001 (0.1/100). Assume that s is 9000 µs. Dcnt is calculated as follows: Dcnt = |0.1 x 9,000 x 0.001| = 1. In this case, the margin range of ir_leads must be changed to [0x033D, 0x3CD].

Offset Address	Register Name	Total Reset Value
0x004	IR_CFG	0x3E80_1F0B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ir_max_level_width																ir_format		ir_bits						ir_mode	ir_freq						
Reset	0	0	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	1	0	1	1

Bits	Access	Name	Description
[31:16]	RW	ir_max_level_width	Invalid when IR_CFG[ir_mode] is 0. Indicates the maximum level width (in 10 µs) of a symbol whenIR_CFG[ir_mode] is 1. This width indicates the end of a symbol stream.
[15:14]	RW	ir_format	Indicates the data code format when IR_CFG[ir_mode] is 0. 00: NEC with simple repeat code 01: TC9012 code 10: NEC with full repeat code 11: SONY code For details about the relationship between code types and code formats, see Table 13-5 to Table 13-7. Indicates the symbol format when IR_CFG[ir_mode] is 1. bit[15]: reserved The definitions of bit[14] are as follows: 0: The symbol is from low to high, and the symbol stream ends at the high level. 1: The symbol is from high to low, and the symbol stream ends at the low level.

[13:8]	RW	ir_bits	Indicates the number of data bits in a frame when IR_CFG[ir_mode] is 0. 0x00 – 0x2F: 1 – 48 data bits in a frame 0x30 – 0x3F: reserved If ir_bits is set to a value ranging from 0x30 to 0x3F by using software, the setting has no effect and the original value is retained. Indicates the symbol receive interrupt threshold when IR_CFG[ir_mode] is 1. bit[13]: reserved bit[12:8]: 0x0 – 0x1F. 0x0 indicates that an interrupt is reported when there is at least one symbol in the FIFO; 0x1F indicates that an interrupt is reported when there are at least 32 symbols in the FIFO, and so on.
[7]	RW	ir_mode	IR operating mode. 0: The decoded complete data frames are output. 1: Only the symbol width is output.
[6:0]	RW	ir_freq	Frequency divider of the working clock. 0x00 – 0x7F: correspond to the working clock divider 1 – 128 respectively.

IR_LEADS

IR_LEADS is a lead code start bit margin configuration register (valid only when IR_CFG[ir_mode] = 0).

CAUTION

Before setting this register, you must set

IR_BUSY[ir_busy] to 0 and set IR_EN[ir_en] to 1. Otherwise, the original value of the register and the reserved value are retained after setting.

The margin must be considered based on the typical value of the specific code type for accurately judging the start bit of the lead code. For details about the typical values of specified code types, see the values of LEAD_S in Table 13-5 to Table 13-7.

- For a pulse width whose typical value is greater than or equal to 400 (10 μs precision), the recommended margin is 8% of the typical value. Take the D6121 code as an example. If the typical value of LEAD_S is 900, the values of cnt_leads_min and cnt_leads_max are calculated as follows:

  cnt_leads_min = 900 x 92% = 828 = 0x33C cnt_leads_max = 900 x 108% = 972 = 0x3CC
- For a pulse width whose typical value is less than 400 (10 μs precision), the recommended margin is 20% of the typical value. Take the SONY-D7C5 as an example.

If the typical value of LEAD_S is 240, the values of cnt_leads_min and cnt_leads_max are calculated as follows:

cnt_leads_min = 240 x 80% = 192 = 0xC0 cnt_leads_max = 240 x 120% = 288 = 0x120

The basic configuration principle is as follows: cnt_leads_max is greater than or equal to cnt_leads_min, and cnt_leads_min is greater than cnt0_b_max and cnt1_b_max.

Offset Address	Register Name	Total Reset Value
0x008	IR_LEADS	0x033C_03CC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								cnt_leads_min								reserved								cnt_leads_max							
Reset	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.
[25:16]	RW	cnt_leads_min	Minimum pulse width of the start bit of the lead code. 0x000 – 0x007: reserved
[15:10]	-	reserved	Reserved.
[9:0]	RW	cnt_leads_max	Maximum pulse width of the start bit of the lead code. 0x000 – 0x007: reserved

IR_LEADE

IR_LEADE is a lead code end bit margin configuration register (valid only when IR_CFG[ir_mode] = 0).

CAUTION

- Before setting this register, you must set
- IR_BUSY[ir_busy] to 0 and set IR_EN[ir_en] to 1. Otherwise, the original value of the register and the reserved value are retained after setting.
- For the NEC with simple repeat code, the margins of cnt_sleade and cnt_leade cannot be overlapped. Otherwise, when the actual count value is within the overlapped range, the simple lead code cannot be identified. As a result, a frame format error occurs.

The margin must be considered based on the typical value of the specific code type for accurately judging the end bit of the lead code. The margin is about 8% of the type value. For details about the typical values of specific code types, see the values of LEAD_E in Table 13-5 to Table 13-7.

- For the pulse width whose typical values is greater than or equal to 400 (10 μs precision), the recommended margin is 8% of the typical value. Take the D6121 code as an example.

If the typical value of LEAD_E is 450, the values of cnt_leade_min and cnt_leade_max are calculated as follows:

cnt_leade_min = 450 x 92% = 414 = 0x19E cnt_leade_max = 450 x 108% = 486 = 0x1E6

- For a pulse width whose typical value is less than 400 (10 μs precision), the recommended margin is 20% of the typical value. Take the SONY-D7C5 code as an example. If the typical value of LEAD_E is 60, the values of cnt_leade_min and cnt_leade_max are calculated as follows:

  cnt_leade_min = 60 x 80% = 48 = 0x030 cnt_leade_max = 60 x 120% = 72 = 0x048

The basic configuration principle is as follows: cnt_leade_max is greater than or equal to cnt_leade_min.

Offset Address	Register Name	Total Reset Value
0x00C	IR_LEADE	0x019E_01E6

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								cnt_leade_min								reserved								cnt_leade_max							
Reset	0	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0

Bits	Access	Name	Description
[31:25]	-	reserved	Reserved.
[24:16]	RW	cnt_leade_min	Minimum pulse width of the end bit of the lead code. 0x000 – 0x007: reserved
[15:9]	-	reserved	Reserved.
[8:0]	RW	cnt_leade_max	Maximum pulse width of the end bit of the lead code. 0x000 – 0x007: reserved

IR_SLEADE

IR_SLEADE is a simple lead code end bit margin configuration register (IR_CFG[ir_mode] = 0).

CAUTION

- Before setting this register, you must set
- IR_BUSY[ir_busy] to 0 and set IR_EN[ir_en] to 1. Otherwise, the original value of the register and the reserved value are retained after setting.
- For the NEC with simple repeat code, the margins of cnt_sleade and cnt_leade cannot be overlapped. Otherwise, when the actual count value is within the overlapped range, the simple lead code cannot be identified. As a result, a frame format error occurs.
- This register must be configured only for the NEC with simple repeat code.

The margin must be considered based on the typical value of the specific code type for accurately judging the end bit of the simple lead code. For details about the typical values of specific code types, see the values of SLEAD_E in Table 13-5 to Table 13-7.

- For a pulse width whose typical value is greater than or equal to 225 (10 µs precision), the recommended margin is 8% of the typical value. Take the D6121 code as an example. If the typical value of SLEAD_E is 225, the values of cnt_sleade_min and cnt_sleade_max are calculated as follows:
  cnt_sleade_min = 225 x 92% = 207 = 0xCF cnt_sleade_max = 225 x 108% = 243 = 0xF3
- For a pulse width whose typical value is less than 225 (10 µs precision), the recommended margin is 20% of the typical value. For example, if the typical value of SLEAD_E of a code type is 60, the values of cnt_sleade_min and cnt_sleade_max are calculated as follows:
  cnt_sleade_min = 60 x 80% = 48 = 0x30 cnt_sleade_max = 60 x 120% = 72 = 0x48

The basic configuration principle is as follows: cnt_sleade_max is greater than or equal to cnt_sleade_min.

Offset Address	Register Name	Total Reset Value
0x010	IR_SLEADE	0x00CF_00F3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								cnt_sleade_min								reserved								cnt_sleade_max							
Reset	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1

Bits	Access	Name	Description
[31:25]	-	reserved	Reserved.
[24:16]	RW	cnt_sleade_min	Minimum pulse width of the end bit of the simple lead code. 0x000 – 0x007: reserved
[15:9]	-	reserved	Reserved.
[8:0]	RW	cnt_sleade_max	Maximum pulse width of the start bit of the simple lead code. 0x000 – 0x007: reserved

IR_B0

IR_B0 is data 0 level judge margin configuration register (valid only when IR_CFG[ir_mode] = 0).

CAUTION

- Before setting this register, you must set
- IR_BUSY[ir_busy] to 0 and set IR_EN[ir_en] to 1. Otherwise, the original value of the register and the reserved value are retained after setting.
- For the preceding four code types, the margins for judging the levels of bit0 and bit1 cannot be overlapped. Otherwise, when the actual count value is within the overlapped range, bit1 cannot be identified and is regarded as bit0 by mistake.

A margin must be considered based on the typical value of the specific code type to accurately judging bit0. The margin is about 20% of the typical value.

- For details about the typical values of the NEC with full repeat code, NEC with simple repeat code, and TC9012 code, see the values of B0_H in Table 13-5 to Table 13-7. Take the D6121 code as an example. If the typical value of B0_H is 56 (10 μs precision), the values of cnt0_b_min and cnt0_b_max are calculated as follows:

  cnt0_b_min = 56 x 80% = 45 = 0x2D cnt0_b_max = 56 x 120% = 67 = 0x43
- For details about the typical value of the SONY code, see the values of B0_L in Table 13-5 to Table 13-7. Take the SONY-D7C5 code as an example. If the typical value of B0_L is 60 (10 μs precision), the values of cnt0_b_min and cnt0_b_max are calculated as follows:

  cnt0_b_min = 60 x 80% = 48 = 0x30 cnt0_b_max = 60 x 120% = 72 = 0x48

The basic configuration principle is as follows: cnt0_b_max is greater than or equal to cnt0_b_min.

Offset Address	Register Name	Total Reset Value
0x018	IR_B1	0x0087_00CB

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								cnt0_b_min								reserved								cnt0_b_max							
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1	1

Bits	Access	Name	Description
[31:25]	-	reserved	Reserved.
[24:16]	RW	cnt0_b_min	Minimum pulse width of the level for judging bit0. 0x000 – 0x007: reserved
[15:9]	-	reserved	Reserved.
[8:0]	RW	cnt0_b_max	Maximum pulse width of the level for judging bit0. 0x000 – 0x007: reserved

IR_B1

IR_B1 is data 1 judge level margin configuration register (valid only when IR_CFG[ir_mode] = 0).

CAUTION

- Before setting this register, you must set
- IR_BUSY bit[0] to 0 and set IR_EN bit[0] to 1. Otherwise, the original value of the register and the reserved value are retained after setting.
- For the preceding four code types, the margins for judging the levels of bit0 and bit1 cannot be overlapped. Otherwise, when the actual count value is within the overlapped range, bit1 cannot be identified and is regarded as bit0 by mistake.

A margin must be considered based on the typical value of the specific code type for accurately judging bit1. The margin is about 20% of the typical value.

- For details about the typical values of the NEC with simple repeat code, NEC with simple repeat code, and TC9012 code, see the values of B1_H in Table 13-5 to Table 13-7. Take the D6121 code as an example. If the typical value of B1_H is 169 (10 µs precision), the values of cnt1_b_min and cnt1_b_max are calculated as follows:

  cnt1_b_min = 169 x 80% = 135 = 0x87 cnt1_b_max = 169 x 120% = 203 = 0xCB
- For details about the typical value of the SONY code, see the values of B1_L in Table 13-5 to Table 13-7. Take the SONY-D7C5 code as an example. If the typical value of B1_L is 120 (10 µs precision), the values of cnt1_b_min and cnt1_b_max are calculated as follows:

  cnt1_b_min = 120 x 80% = 96 = 0x60 cnt1_b_max = 120 x 120% = 144 = 0x90

The basic configuration principle is as follows: cnt1_b_max is greater than or equal to cnt1_b_min.

Offset Address	Register Name	Total Reset Value
0x018	IR_B1	0x0087_00CB

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								cnt1_b_min								reserved								cnt1_b_max							
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1	1

Bits	Access	Name	Description
[31:25]	-	reserved	Reserved.
[24:16]	RW	cnt1_b_min	Minimum pulse width of the level for judging bit1. 0x000 – 0x007: reserved
[15:9]	-	reserved	Reserved.
[8:0]	RW	cnt1_b_max	Maximum pulse width of the level for judging bit1. 0x000 – 0x007: reserved

IR_BUSY

IR_BUSY is a configuration busy flag register.

Offset Address	Register Name	Total Reset Value
0x01C	IR_BUSY	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															ir_busy
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RO	ir_busy	Busy status flag. 0: idle. In this case, software can configure data. 1: Indicates the busy state. In this state, software cannot configure data.

IR_DATAH

IR_DATAH is an upper 16-bit IR receive decoded data register (IR_CFG[ir_mode] = 0) or symbol count register in the symbol FIFO (IR_CFG[ir_mode] = 1)

The IR_DATAH register stores the upper 16 bits of the decoded data received by the IR, whereas IR_DATAL stores the lower 32 bits of the decoded data received by the IR. The data bits depend on the valid data bits in a frame and the specific code. For details, see the valid data bits in Table 13-5 to Table 13-7.

Data is stored as follows: The data is stored in IR_DATAH and IR_DATAL in sequence from MSB to LSB. That is, after IR_DATAL is full, the remaining data is stored in IR_DATAH. The unused upper bits are reserved. Data is read as follows: IR_DATAH and IR_DATAL are read in sequence.

The hardware receives all data bits without checking the definition of each data bit. The software is responsible for processing data bits.

Offset Address	Register Name	Total Reset Value
0x020	IR_DATAH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ir_datah															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.

Offset Address	Register Name	Total Reset Value
0x020	IR_DATAH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ir_datah															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:0]	RO	ir_datah	Indicates the upper 16 bits of the decoded data received by the IR module when IR_CFG[ir_mode] is 0. Indicates the symbol count in the symbol FIFO when IR_CFG[ir_mode] is 1. bit[15:6]: reserved bit[5:0]: number of symbols in the symbol FIFO.

IR_DATAL

IR_DATAL is a lower 32-bit IR receive decoded data register (IR_CFG[ir_mode] = 0) or IR receive symbol width register (IR_CFG[ir_mode] = 1).

Offset Address	Register Name	Total Reset Value
0x024	IR_DATAL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ir_datal																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	ir_datal	Indicates the lower 32 bits of the decoded data received by the IR module when IR_CFG[ir_mode] is 0. Indicates the width of the symbol received by the IR module when IR_CFG[ir_mode] is 1. The definitions of bit[31:16] are as follows: Indicates the high-level width (a multiple of 10 μs) of the symbol received by the IR when the symbol level is from low to high. Indicates the low-level width (a multiple of 10 μs) of the symbol received by the IR module when the symbol level is from high to low. The definitions of bit[15:0] are as follows: Indicates the low-level width (a multiple of 10 μs) of the symbol received by the IR module when the symbol level is from low to high. Indicates the high-level width (a multiple of 10 μs) of the symbol received by the IR module when the symbol level is from high to

Offset Address	Register Name	Total Reset Value
0x024	IR_DATAL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ir_datal																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
			low.

IR_INT_MASK

IR_INT_MASK is an IR interrupt mask register.

CAUTION

- Before setting this register, you must set IR_EN[ir_en] to 1. Otherwise, the original value of the register is retained after setting.
- If all interrupts are masked, the IR wake-up function is unavailable.
- When IR_CFG[ir_mode] is 0, IR_INT_MASK bit[3:0] are valid; when IR_CFG[ir_mode] is 1, IR_INT_MASK bit[18:16] are valid.

The definitions of the interrupts related to the register are as follows:

- Receive data overflow interrupt

  If the CPU does not fetch the current frame and the next frame is already received, the next frame overwrites the current frame and a raw receive data overflow error interrupt is reported.
- Receive data frame format error interrupt

  If the received data frame is not complete or the data pulse width does not meet the margin requirements, a raw receive frame format error interrupt is reported.
- Receive data frame interrupt

  After a complete frame data is received, a raw receive data frame interrupt is reported.
- Key release detection interrupt

  For the NEC with simple repeat code and TC9012 code, if the start synchronous code is not detected again within 160 ms after the previously detected start synchronous code, or a valid data frame rather than a simple lead code is detected, a raw key release detection interrupt is reported. Both the NEC with full repeat code and the SONY code do not support the key release detection interrupt.
- Receive symbol overflow interrupt

  If the symbol FIFO is full because the CPU does not fetch the data in time and the subsequent symbol is already received, a raw receive symbol overflow error interrupt is reported.

- Receive symbol interrupt

  If a complete symbol is received and the symbol count of the symbol FIFO is above the threshold configured by IR_CFG[ir_bits], a raw receive symbol interrupt is reported.

- Symbol timeout interrupt

  If no new symbol interrupt is received during the period configured by IR_CFG[ir_max_level_width] after a valid symbol is received, a raw symbol timeout interrupt is reported.

The hardware does not identify the interrupt priority. An interrupt is generated if one or more masked interrupt sources are valid.

Offset Address	Register Name	Total Reset Value
0x028	IR_INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													intm_overrun	intm_time_out	intm_symb_rcv	reserved												intm_release	intm_overflow	intm_framerr	intm_rcv
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	-	reserved	Reserved.
[18]	RW	intm_overrun	Symbol overflow interrupt mask when IR_CFG[ir_mode] is 1. 0: not masked 1: masked
[17]	RW	intm_time_out	Symbol timeout interrupt mask when IR_CFG[ir_mode] is 1. 0: not masked 1: masked
[16]	RW	intm_symb_rcv	Receive N symbol interrupt mask when IR_CFG[ir_mode] is 1. 0: not masked 1: masked
[15:4]	-	reserved	Reserved.
[3]	RW	intm_release	Key release interrupt mask when IR_CFG[ir_mode] is 0. 0: not masked 1: masked
[2]	RW	intm_overflow	Receive data overflow interrupt mask when IR_CFG[ir_mode] is 0. 0: not masked 1: masked

[1]	RW	intm_framerr	Receive data frame format error interrupt mask when IR_CFG[ir_mode] is 0. 0: not masked 1: masked
[0]	RW	intm_rcv	Receive data frame interrupt mask when IR_CFG[ir_mode] is 0. 0: not masked 1: masked

IR_INT_STATUS

IR_INT_STATUS is an IR interrupt status register.

CAUTION

- When IR_CFG[ir_mode] is 0, IR_INT_STATUS bit[3:0] and IR_INT_STATUS bit[19:16] are valid.
- When IR_CFG[ir_mode] is 1, IR_INT_STATUS bit[10:8] and IR_INT_STATUS bit[26:24] are valid.

Offset Address	Register Name	Total Reset Value
0x02C	IR_INT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					intms_overrun	intms_time_out	intms_symb_rcv	reserved				intms_release	intms_overflow	intms_framerr	intms_rcv	reserved					intrs_overrun	intrs_time_out	intrs_symb_rcv	reserved				intrs_release	intrs_overflow	intrs_framerr	intrs_rcv
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	-	reserved	Reserved.
[26]	RO	intms_overrun	Masked symbol overflow interrupt status when IR_CFG[ir_mode] is 1. 0: No interrupt is generated. 1: An interrupt is generated.
[25]	RO	intms_time_out	Masked symbol timeout interrupt status when IR_CFG[ir_mode] is 1. 0: No interrupt is generated. 1: An interrupt is generated.

[24]	RO	intms_symb_rcv	Masked receive symbol interrupt status when IR_CFG[ir_mode] is 1. 0: No interrupt is generated. 1: An interrupt is generated.
[23:20]	-	reserved	Reserved.
[19]	RO	intms_release	Masked key release interrupt status when IR_CFG[ir_mode] is 0. 0: No interrupt is generated. 1: An interrupt is generated.
[18]	RO	intms_overflow	Masked receive data overflow error interrupt status when IR_CFG[ir_mode] is 0. 0: No interrupt is generated. 1: An interrupt is generated.
[17]	RO	intms_framerr	Masked receive data frame format error interrupt status when IR_CFG[ir_mode] is 0. 0: No interrupt is generated. 1: An interrupt is generated.
[16]	RO	intms_rcv	Masked receive data frame interrupt status when IR_CFG[ir_mode] is 0. 0: No interrupt is generated. 1: An interrupt is generated.
[15:11]	-	reserved	Reserved.
[10]	RO	intrs_overrun	Raw symbol overflow interrupt status when IR_CFG[ir_mode] is 1. 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RO	intrs_time_out	Raw symbol timeout interrupt status when IR_CFG[ir_mode] is 1. 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	intrs_symb_rcv	Raw receive symbol interrupt status when IR_CFG[ir_mode] is 1. 0: No interrupt is generated. 1: An interrupt is generated.
[7:4]	-	reserved	Reserved.
[3]	RO	intrs_release	Raw key release interrupt status when IR_CFG[ir_mode] is 0. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	intrs_overflow	Raw receive data overflow error interrupt status when IR_CFG[ir_mode] is 0. 0: No interrupt is generated. 1: An interrupt is generated.

[1]	RO	intrs_framerr	Raw receive data frame format error interrupt status when IR_CFG[ir_mode] is 0. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	intrs_rcv	Raw receive data frame interrupt status when IR_CFG[ir_mode] is 0. 0: No interrupt is generated. 1: An interrupt is generated.

IR_INT_CLR

IR_INT_CLR is an IR interrupt clear register.

CAUTION

- When IR_CFG[ir_mode] is 0, IR_INT_CLR bit[3:0] are valid.
- When IR_CFG [ir_mode] is 1, IR_INT_CLR bit[18:16] are valid.

Offset Address: 0x030 | Register Name: IR_INT_CLR | Total Reset Value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													intc_overrun	intc_time_out	intc_symb_rcv	reserved												intc_release	intc_overflow	intc_framerr	intc_rcv
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	-	reserved	Reserved.
[18]	WC	intc_overrun	When IR_CFG[ir_mode] is 1, this bit indicates whether the symbol overflow interrupt request is cleared. 0: no effect 1: cleared
[17]	WC	intc_time_out	When IR_CFG[ir_mode] is 1, this bit indicates whether the symbol timeout interrupt request is cleared. 0: no effect 1: cleared

[16]	WC	intc_symb_rcv	When IR_CFG[ir_mode] is 1, this bit indicates whether the receive symbol interrupt request is cleared. 0: no effect 1: cleared
[15:4]	-	reserved	Reserved.
[3]	WC	intc_release	When IR_CFG[ir_mode] is 0, this bit indicates whether the key release interrupt request is cleared. 0: no effect 1: cleared
[2]	WC	intc_overflow	When IR_CFG[ir_mode] is 0, this bit indicates whether the receive data overflow error interrupt request is cleared. 0: no effect 1: cleared
[1]	WC	intc_framerr	When IR_CFG[ir_mode] is 0, this bit indicates whether the receive data frame format error interrupt request is cleared. 0: no effect 1: cleared
[0]	WC	intc_rcv	When IR_CFG[ir_mode] is 0, this bit indicates whether the receive data frame interrupt request is cleared. 0: no effect 1: cleared If a receive data frame interrupt is generated and the software writes 1 to the bit without reading the data in IR_DATAL, the interrupt cannot be cleared.

IR_START

IR_START is an IR start configuration register.

After other registers are configured, IR_START can be started when any value is written to the corresponding address during the startup of the IR module.

Offset Address	Register Name	Total Reset Value
0x034	IR_START	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								ir_start
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.

Offset Address	Register Name	Total Reset Value
0x034	IR_START	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								ir_start
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[0]	WO	ir_start	IR start configuration register.

13.5 GPIO

13.5.1 Overview

The Hi3518A supports 12 groups of general purpose input/output (GPIO) pins. Each group of GPIO pins provides eight programmable input/output pins except that group 11 provides only seven programmable input/output pins. Each pin can be configured as input or output and these pins are used to generate input signals or output signals for special purposes. As input, each GPIO pin can act as an interrupt source; as output, each GPIO pin can be set to 0 or 1 separately.

Table 13-9 lists the unavailable GPIO pins for the Hi3518C compared with the Hi3518A. For details about other GPIO pins, see chapter 2 "Hardware for the Hi3518C."

Table 13-9 Unavailable GPIO pins for the Hi3518C

Pin	Description
GPIO1_0	Unavailable for the Hi3518C
GPIO1_4	Unavailable for the Hi3518C
GPIO1_5	Unavailable for the Hi3518C
GPIO1_6	Unavailable for the Hi3518C
GPIO1_7	Unavailable for the Hi3518C
GPIO2_4	Unavailable for the Hi3518C
GPIO2_6	Unavailable for the Hi3518C
GPIO2_7	Unavailable for the Hi3518C
GPIO5_0	Unavailable for the Hi3518C
GPIO5_4	Unavailable for the Hi3518C

Pin	Description
GPIO5_5	Unavailable for the Hi3518C
GPIO5_6	Unavailable for the Hi3518C
GPIO5_7	Unavailable for the Hi3518C
GPIO6_2	Unavailable for the Hi3518C
GPIO7_5	Unavailable for the Hi3518C
GPIO7_6	Unavailable for the Hi3518C
GPIO7_7	Unavailable for the Hi3518C
GPIO8_0	Unavailable for the Hi3518C
GPIO8_1	Unavailable for the Hi3518C
GPIO8_2	Unavailable for the Hi3518C
GPIO8_3	Unavailable for the Hi3518C
GPIO8_4	Unavailable for the Hi3518C
GPIO8_5	Unavailable for the Hi3518C
GPIO8_6	Unavailable for the Hi3518C
GPIO8_7	Unavailable for the Hi3518C
GPIO9_0	Unavailable for the Hi3518C
GPIO9_1	Unavailable for the Hi3518C
GPIO9_2	Unavailable for the Hi3518C
GPIO9_3	Unavailable for the Hi3518C
GPIO9_4	Unavailable for the Hi3518C
GPIO9_5	Unavailable for the Hi3518C
GPIO9_6	Unavailable for the Hi3518C
GPIO9_7	Unavailable for the Hi3518C

CAUTION

For details about the number of GPIO pins and multiplexing relationship between GPIO pins and other pins, see Chapter 2 "Hardware." For details about control modes, see section 2.1.5 "Description of Multiplexing Registers".

For the multiplexed GPIO pins that are output by default, note that the pins that connect to the chip and the components must be input.

13.5.2 Features

The GPIO module has the following features:

- Each GPIO pin can be configured as input or output.
  - As input, each GPIO pin can act as an interrupt source, that is, each GPIO pin can be controlled by an interrupt separately.
  - As output, each GPIO can be set to 0 or 1 separately.
- The GPIO interrupts are controlled by using seven registers such as GPIO_IS. These registers enable you to select the interrupt source, interrupt edge (falling edge or rising edge), and interrupt trigger modes (level-sensitive mode or edge-sensitive mode). For details about the corresponding interrupt registers of GPIO pins, see section 3.3 "Interrupt System."
  - When multiple interrupts occur at the same time, these interrupts are combined as one interrupt to report. For details about the GPIO interrupt mapping, see section 3.3 "Interrupt System".
  - The GPIO_IS, GPIO_IBE, and GPIO_IEV registers determine the features of the interrupt source and interrupt trigger type.

  GPIO_RIS and GPIO_MIS are used to read the raw interrupt status and masked interrupt status respectively. GPIO_IE controls the final report status of each interrupt. In addition, GPIO_IC is provided to clear the interrupt status separately.

13.5.3 Function Description

Each group of GPIO pins consist of eight programmable I/O pins (excluding GPIO11). Each pin can be configured as input or output and these pins are used to generate input signals or output signals for special purposes.

The GPIO module can generate maskable interrupts based on the level or transition value. The general purpose input output interrupt (GPIOINTR) informs the interrupt controller of the occurrence of interrupts.

13.5.4 Operating Mode

Interface Reset

During power-on reset, all registers are cleared, and therefore the pins work as input pins by default.

When the reset signal is valid, the status of the GPIO is as follows:

- The interrupt becomes invalid after the corresponding bit of GPIO_IE is cleared.
- All registers are cleared.
- All pins are configured as input.
- The raw interrupt register is cleared.
- The triggering mode of the interrupt is set to edge-sensitive.

GPIO

Each pin can be configured as input or output. To configure a GPIO pin, perform the following steps:

1. Enable the required GPIO pins by configuring corresponding pins according to the description of IO_CONFIG.
2. Configure the GPIO as input or output by using the GPIO_DIR register.
   - As input: The external signals are transmitted through the GPIO pin. In this case, the values of the input signals can be viewed by checking the GPIO_DATA register.

     Note: The input signals are also transmitted to the pins that are multiplexed with the GPIO pins.
   - As output: The values are written to the GPIO_DATA register and output by using the GPIO in sequence.

   NOTE
   If the GPIO interrupt function is enabled, an interrupt is generated when the output signal meets the triggering condition.

   ----End

Interrupt Operation

To generate an interrupt rather than a pseudo interrupt, perform the following steps:

1. Select the edge-sensitive mode or level-sensitive mode by configuring the GPIO_IS register.
2. Select the falling-/rising-edge-sensitive mode or high-/low-level-sensitive mode by configuring the GPIO_IEV register.
3. If the edge-sensitive mode is selected, select single-edge-sensitive mode or dual-edge-sensitive mode by configuring the GPIO_IBE register.

   Ensure that the GPIO data lines are stable during preceding operations.
4. Write 0xFF to the GPIO_IC register to clear the interrupt.
5. Set the GPIO_IE to 1 to enable the interrupt.

   ----End

The GPIO interrupts are controlled by seven registers. When one or more GPIO pins generate interrupts, a combined interrupt is output to the interrupt controller. The differences between the edge-sensitive mode and level-sensitive mode are as follows:

- Edge-sensitive mode: Software must clear this interrupt to enable superior interrupts.
- Level-sensitive mode: The external interrupt source must keep this level until the processor identifies this interrupt.

13.5.5 Register Summary

Table 13-10 lists the base addresses of 12 groups of GPIO registers.

Table 13-10 Base addresses of 12 groups of GPIO registers

Register	Base Address
GPIO11	0x201F_0000
GPIO10	0x201E_0000

Register	Base Address
GPIO9	0x201D_0000
GPIO8	0x201C_0000
GPIO7	0x201B_0000
GPIO6	0x201A_0000
GPIO5	0x2019_0000
GPIO4	0x2018_0000
GPIO3	0x2017_0000
GPIO2	0x2016_0000
GPIO1	0x2015_0000
GPIO0	0x2014_0000

Table 13-11 describes the offset addresses and definitions of a group of internal GPIO registers. GPIO0 to GPIO11 also have the same internal GPIO registers.

NOTE

- Register address of GPIOn = GPIOn base address + Offset address of the register
- The value of n ranges from 0 to 11.

Table 13-11 Summary of GPIO registers

Offset Address	Register	Description	Page
0x000 – 0x3FC	GPIO_DATA	GPIO data register	13-85
0x400	GPIO_DIR	GPIO direction control register	13-85
0x404	GPIO_IS	GPIO interrupt trigger register	13-86
0x408	GPIO_IBE	GPIO interrupt dual-edge trigger register	13-86
0x40C	GPIO_IEV	GPIO interrupt trigger event register	13-87
0x410	GPIO_IE	GPIO interrupt mask register	13-87
0x414	GPIO_RIS	GPIO raw interrupt status register	13-88
0x418	GPIO_MIS	GPIO masked interrupt status register	13-88
0x41C	GPIO_IC	GPIO interrupt clear register	13-89

13.5.6 Register Description

GPIO_DATA

GPIO_DATA is a GPIO data register. It is used to buffer the input or output data.

When the corresponding bit of the GPIO_DIR is configured as output, the values written to the GPIO_DATA register are sent to the corresponding pin (note that the pin multiplexing configuration must be correct). If the bit is configured as input, the value of the corresponding input pin is read.

CAUTION

If the corresponding bit of GPIO_DIR is configured as input, the pin value is returned after a valid read; if the corresponding bit is configured as output, the written value is returned after a valid read.

Through PADDR[9:2], the GPIO_DATA register masks the read and write operations on the register. The register corresponds to 256 address spaces. PADDR[9:2] corresponds to GPIO_DATA[7:0]. When the corresponding bit is high, it can be read or written. When the corresponding bit is low, no operations are supported. For example:

- If the address is 0x3FC (0b11_1111_1100), the operations on all the eight bits of GPIO_DATA[7:0] are valid.
- If the address is 0x200 (0b10_0000_0000), only the operation on GPIO_DATA[7] is valid.

Offset Address	Register Name	Total Reset Value
0x000 – 0x3FC	GPIO_DATA	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_data							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_data	Indicates the GPIO input data when the GPIO is configured as input; indicates the GPIO output data when the GPIO is configured as output. Each bit can be controlled separately. The register is used together with GPIO_DIR.

GPIO_DIR

GPIO_DIR is a GPIO direction control register. It is used to configure the direction of each GPIO pin.

Offset Address	Register Name	Total Reset Value
0x400	GPIO_DIR	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_dir							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_dir	GPIO direction control register. Bit[7:0] correspond to GPIO_DATA [7:0] respectively. Each bit can be controlled separately. 0: input 1: output

GPIO_IS

GPIO_IS is a GPIO interrupt trigger register. It is used to configure the interrupt trigger mode.

Offset Address	Register Name	Total Reset Value
0x404	GPIO_IS	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_is							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_is	GPIO interrupt trigger control register. Bit[7:0] correspond to GPIO_DATA [7:0]. Each bit is controlled separately. 0: edge-sensitive mode 1: level-sensitive mode

GPIO_IBE

GPIO_IBE is a GPIO interrupt dual-edge trigger register. It is used to configure the edge trigger mode of each GPIO pin.

Offset Address	Register Name	Total Reset Value
0x408	GPIO_IBE	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_ibe							

Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_ibe	GPIO interrupt edge control register. Bit[7:0] correspond to GPIO_DATA [7:0] respectively. Each bit is controlled independently. 0: single-edge-sensitive mode. The GPIO_IEV register controls whether the interrupt is rising-edge-sensitive or falling-edge-sensitive. 1: dual-edge-sensitive mode

GPIO_IEV

GPIO_IEV is a GPIO interrupt event register. It is used to configure the interrupt trigger event of each GPIO pin.

Offset Address	Register Name	Total Reset Value
0x40C	GPIO_IEV	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_iev							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_iev	GPIO interrupt trigger event register. Bit[7:0] correspond to GPIO_DATA [7:0]. Each bit is controlled separately. 0: falling-edge-sensitive mode or low-level-sensitive mode 1: rising-edge-sensitive mode or high-level-sensitive mode.

GPIO_IE

GPIO_IE is a GPIO interrupt mask register. It is used to mask GPIO interrupts.

Offset Address	Register Name	Total Reset Value
0x410	GPIO_IE	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_ie							

Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_ie	GPIO interrupt mask register. Bit[7:0] correspond to GPIO_DATA [7:0]. Each bit is controlled separately. 0: masked 1: not masked

GPIO_RIS

GPIO_RIS is a GPIO raw interrupt status register. It is used to query the raw interrupt status of each GPIO pin.

Offset Address	Register Name	Total Reset Value
0x414	GPIO_RIS	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_ris							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	gpio_ris	GPIO raw interrupt status register. Bit[7:0] correspond to GPIO_DATA [7:0], indicating the unmasked interrupt status. The status cannot be masked and controlled by the GPIO_IE register. 0: An interrupt is generated. 1: No interrupt occurs.

GPIO_MIS

GPIO_MIS is a GPIO masked interrupt status register. It is used to query the masked interrupt status of each GPIO pin.

Offset Address	Register Name	Total Reset Value
0x418	GPIO_MIS	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_mis							

Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	gpio_mis	GPIO masked interrupt status register. Bit[7:0] correspond to GPIO_DATA [7:0], indicating the masked interrupt status. The status is controlled by the GPIO_IE register. 0: The interrupt is invalid. 1: The interrupt is valid.

GPIO_IC

GPIO_IC is a GPIO interrupt clear register. It is used to clear the interrupts generated by GPIO pins and clear the GPIO_RIS and GPIO_MIS registers.

Offset Address	Register Name	Total Reset Value
0x41C	GPIO_IC	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_ic							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	WC	gpio_ic	GPIO interrupt clear register. Bit[7:0] correspond to GPIO_DATA [7:0]. Each bit is controlled separately. 0: no effect 1: cleared

13.6 USB 2.0 Host

13.6.1 Overview

The USB 2.0 host controller supports the high-speed (480 Mbit/s), full-speed (12 Mbit/s), and low-speed (1.5 Mbit/s) data transfer modes. It complies with the USB 2.0, open host controller interface (OHCI) V1.0a, and enhanced host controller interface (EHCI) V1.0 protocols. The USB 2.0 host controller has a root hub. As a part of the USB system, the root hub is used to extend the USB port. By using hardware logic in the controller, the following functions are achieved:

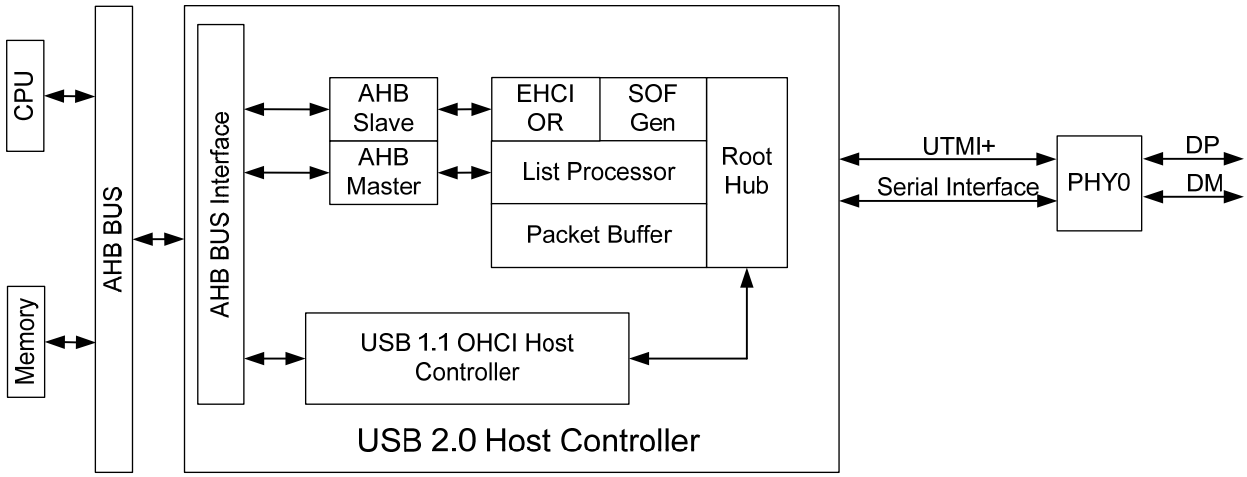
- Controls and processes data transfer.
- Parses data packets and packages data.
- Encodes and decodes the signals transmitted through the USB port.
- Provide interfaces (such as the interrupt vector interface) for the driver.

13.6.2 Function Description

Logic Block Diagram

Figure 13-39 shows the logic block diagram of the USB 2.0 host controller.

Figure 13-39 Logic block diagram of the USB 2.0 host controller



UTMI: USB2.0 Transceiver Macrocell Interface
EHCI: Enhanced Host Controller Interface
OHCI: Open Host Controller Interface

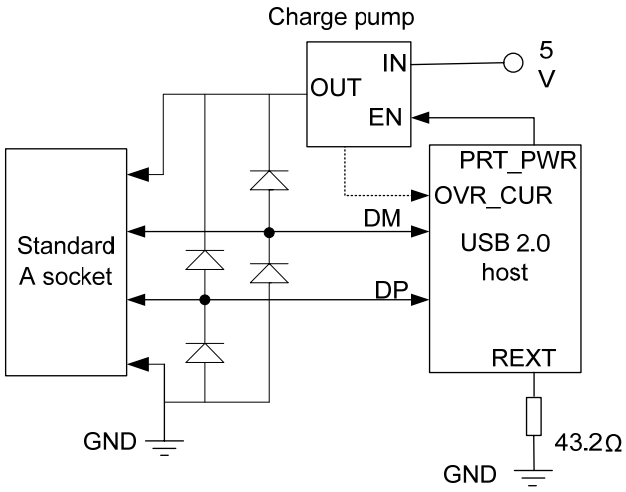
Typical Application

Figure 13-40 shows the reference design of the USB 2.0 host controller.

CAUTION

- The impedance of DP or DM is 45 Ω ±1% and no extra matched resistors are required.
- The REXT resistor is a ±1% resistor.
- If high-speed electrostatic discharge (ESD) components are used, 1 pF capacitors are recommended.

Figure 13-40 Reference design of the USB 2.0 host controller



Functions

The USB 2.0 host controller has the following features:

- Fully compatible with USB 2.0.
- Complies with OHCI V1.0a and EHCI V1.0 protocols.
- Supports high-speed, full-speed, and low-speed devices.
- Supports low-power solutions.
- Supports four basic data transfer modes including control transfer, bulk transfer, isochronous transfer, and interrupt transfer.
- Supports a maximum of 127 devices by using USB hubs

Working Principle

The USB 2.0 host controller supports the following four standard transfer modes:

- Control transfer

  This mode is applicable to the data transfer between endpoints 0 of USB host and the USB device. For the USB devices of specific models, other endpoints may be used. The control transfer is bidirectional and the transferred data amount is small. Depending on the device and transfer speed, 8-byte data, 16-byte data, 32-byte data, or 64-byte data can be transferred.
- Bulk transfer

  This mode is applicable to the data transfer in bulk when there is no limit on the bandwidth and time interval. This mode is the best choice when the transfer speed is very low and multiple data transfers are delayed. In this case, bulk transfer is performed after all other types of data transfers are complete. In the bulk transfer mode, data is transferred between the USB host and USB device without errors by using the error detection and retransmission mechanism.
- Isochronous transfer

This mode is applicable to the stream data transfer with strict time requirements and strong error tolerance or the instant data transfer at a constant transfer rate. This mode provides a fixed bandwidth and time interval.

- Interrupt transfer

  This mode is applicable to the data transfer when the data is scattered, unpredictable, and is of small volume. In this mode, the device is checked whether there is interrupt data to be sent at a fixed interval. The query frequency ranges from 1 ms to 255 ms and it depends on the device endpoint mode. The typical interrupt transfer mode is unidirectional and only input is available for the USB host.

13.6.3 Operating Mode

Pin Polarity Control

The valid polarity of USB_PWREN can be configured by setting PERIPHCTRL20 [usbpwr_p_ctrl]. The valid polarity of USB_OVRCUR can be configured by setting PERIPHCTRL20 [usbovr_p_ctrl].

Clock Gating

If the USB 2.0 host controller is not used, its clock can be disabled to reduce power consumption.

To disable the clock, perform the following steps:

1. Write 1 to PERI_CRG46 [usbphy_port0_treq], PERI_CRG46[usbphy_ req], PERI_CRG46[usb_ctrl_utmi0_req], PERI_CRG46[usb_ctrl_hub_req], and PERI_CRG46[usb_ahb_srst_req] respectively to reset the USB controller and PHY.
2. Set PERI_CRG46 [usb_cken] to 0 to disable the clocks of the USB 2.0 host controller.

----End

To enable the clocks, perform the following steps:

1. Set PERI_CRG46 [usb_cken] to 1 to enable the clocks of the USB 2.0 host controller.
2. Deassert the reset on the USB controller and PHY. For details, see "Reset Clear."

----End

Reset Deassert

By default, the USB controller and PHY are reset after power-on. To deassert reset, perform the following steps:

1. Delay at least 10 μs.
2. Write 0 to PERI_CRG46[usbphy_port0_treq] to deassert the soft reset on USB PHY port0.
3. Write 0 to PERI_CRG46[usbphy_req] to deassert the reset on the USB PHY.
4. After 250 μs delay, write 0 to PERI_CRG46[usb_ctrl_utmi0_req] to deassert the soft reset on USB controller port0; write 0 to PERI_CRG46[usb_ctrl_hub_req] to deassert the soft reset on the hub of the USB controller.

5. Write 0 to PERI_CRG46[usb_ahb_srst_req] to deassert the soft reset on the USB bus.

----End

Resetting Port0 During the Working Process

To reset port0 during the working process, perform the following steps:

1. Write 1 to PERI_CRG46[usb_ctrl_utmi0_req] to soft-reset port0 of the USB controller.
2. Write 1 to PERI_CRG46[usbphy_port0_treq] to soft-reset port0 of the USB PHY.
3. After 200 μs delay, write 0 to PERI_CRG46[usbphy_port0_treq] to deassert the reset on port0 of the USB PHY.
4. Write 0 to PERI_CRG46[usb_ctrl_utmi0_req] to deassert the reset on port0 of the USB controller.

----End

Suspend and Resume

Suspending PHY 0: Port0 enters the suspend mode after software sets the system mode to suspend mode by using the EHCI and OHCI registers.

Resuming port0: After the software sets the system mode to another mode rather than suspend mode by using the EHCI and OHCI registers, if PERI_USB1 [COMMONONN] is 1, the software can initiate a USB operation at least 225 μs later; if PERIPHCTRL21 [commononn] is 0, the software can initiate a USB operation at least 5 μs later.

Adjusting the Quality of the USB TX Signal

If the USB eye pattern on the board does not meet the requirements of the template defined by the USB protocol, you can adjust the quality of the USB TX signal.

Perform the following steps:

1. Write 1 to PERIPHCTRL21[phy0_txpreemphasistune] to enable the preemphasis function of USB port0.
2. Write 1 to PERIPHCTRL21[phy0_txrisetune] to reduce the up or down time of high-speed signals.
3. Write 1111 to PERIPHCTRL21[phy0_txverftune] to increase the DC level.

----End

NOTE

If the USB eye pattern on the board does not meet the requirements of the template defined by the USB protocol, ensure that the preceding registers are configured.

13.6.4 Register Summary

NOTE

The USB module is a standard USB 2.0 host controller and the internal registers are standard EHCI and OHCI registers. For details, see the EHCI and OHCI protocols. The following section describes the registers that are specially defined only by some vendors.

Table 13-12 describes the USB registers.

Table 13-12 Summary of USB registers (base address: 0x100B_0000)

Offset Address	Register	Description	Page
0x90	INTNREG00	Micro-frame length configuration register	13-94
0x94	RESERVED	Reserved	-
0x98	RESERVED	Reserved	-
0x9C	RESERVED	Reserved	-
0xA0	INTNREG04	Debug register	13-95
0xA4	INTNREG05	Control and status register	13-96
0xA8	INTNREG06	AHB error status register	13-96
0xAC	INTNREG07	AHB error address register	13-97

NOTE

The base address of the EHCI register is 0x100B_0000 and the base address of the OHCI register is 0x100A_0000. The base address of Table 13-12 is that of the EHCI register.

13.6.5 Register Description

INTNREG00

INTNREG00 is a micro-frame length configuration register.

Offset Address	Register Name	Total Reset Value
0x90	INTNREG00	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				val											en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	-	reserved	Reserved.
[13:1]	RW	val	Value of the micro-frame counter. This register is used only for emulation. In normal mode, the micro-frame length is 125 μs defined by the protocol. During emulation, you can change the micro-frame length by configuring this register as required to reduce the emulation time.
[0]	RW	en	Register enable. 0: disabled 1: enabled

INTNREG04

INTNREG04 is a debug register.

Offset Address	Register Name	Total Reset Value
0xA0	INTNREG04	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										auto_en	nak_reldfix_en	reserved	scaledwn_enum_time	hccparam_en	hcsparam_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	-	reserved	Reserved.
[5]	RW	auto_en	Automatic feature enable. 0: enabled. The suspend signal is valid when the run/stop bit is reset by software, but the hchalted bit is not set. 1: disabled. The port is not suspended when software clears the run/stop bit. The default value is 0.
[4]	RW	nak_reldfix_en	NAK reload enable. 0: enabled 1: disabled
[3]	-	reserved	Reserved.
[2]	RW	scaledwn_enum_time	Port enumeration time scale down enable. 0: disabled 1: enabled
[1]	RW	hccparam_en	HCCPARAMS register write enable. 0: disabled 1: enabled
[0]	RW	hcsparam_en	HCSPARAMS register write enable. 0: disabled 1: enabled

INTNREG05

INTNREG05 is a control and status register. It is used to read or write to the PHY.

Offset Address	Register Name	Total Reset Value
0xA4	INTNREG05	0x0000_1000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18	17	16	15 14 13	12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				vbusy	vport		vcontrol_loadm	vcontrol	vstatus	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0	0	0 0 0	1	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:18]	-	reserved	Reserved.
[17]	RO	vbusy	The value 1 indicates that the hardware is writing data. This bit is cleared only when the process ends.
[16:13]	RW	vport	Port ID. It cannot exceed the supported number of ports.
[12]	RW	vcontrol_loadm	Load enable. 0: enabled 1: disabled
[11:8]	RW	vcontrol	Port control signal.
[7:0]	RO	vstatus	Port status signal.

INTNREG06

INTNREG06 is an AHB error status register.

Offset Address	Register Name	Total Reset Value
0xA8	INTNREG06	0x0000_0000

Bit	31	30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	err_capture	reserved					hbusrt_err	num_beat_err	num_beat_ok
Reset	0	0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31]	RW	err_capture	AHB error.
[30:12]	-	reserved	Reserved.

[11:9]	RO	hbusrt_err	hbrust value during a control transfer when an AHB error occurs.
[8:4]	RO	num_beat_err	Number of beats during a burst transfer when an AHB error occurs. The maximum number of beats is 16. 0x00 – 0x10: valid 0x11 – 0x1F: reserved
[3:0]	RO	num_beat_ok	Number of completed beats during a burst transfer when an AHB error occurs.

INTNREG07

INTNREG07 is an AHB error address register.

Offset Address	Register Name	Total Reset Value
0xAC	INTNREG07	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	err_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	err_addr	Address during a control transfer when an AHB error occurs.

13.7 MMC/SD/SDIO Controller

13.7.1 Function Description

Functional Block Diagram

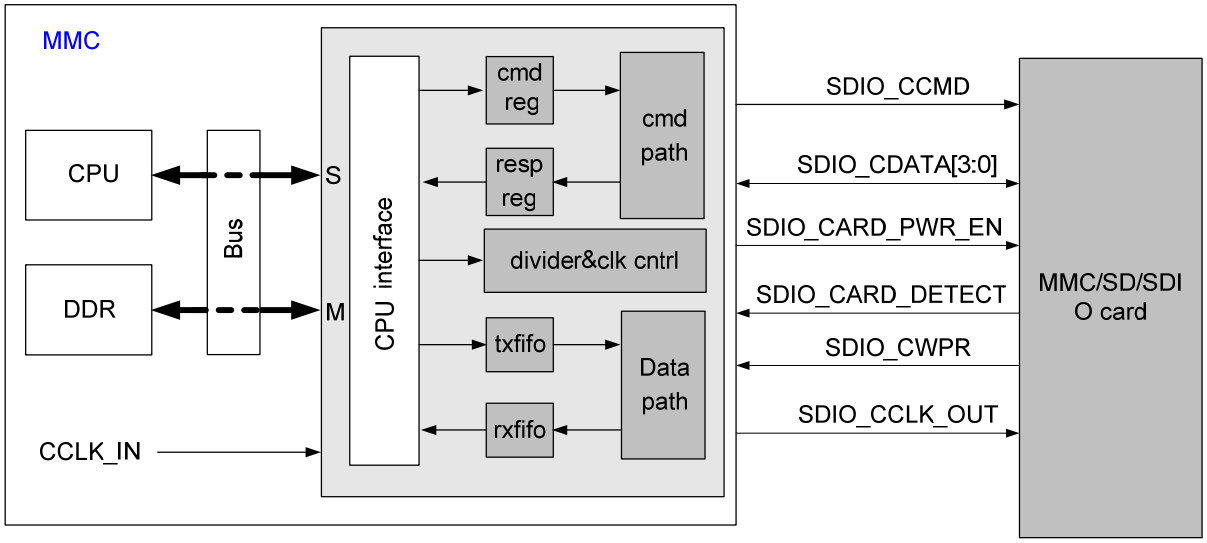
The MMC/SD/SDIO controller (MMC controller for short) controls the read/write operations on the secure digital (SD) card and multimedia card (MMC), and supports various extended devices such as Bluetooth and Wi-Fi devices based on the secure digital input/output (SDIO) protocol. The Hi3518 provides one MMC controller for controlling the SD card, MMC, and SDIO device.

The MMC controller can control the devices that comply with the following protocols:

- Secure Digital Memory (SD mem – version 2.00)
- Secure Digital I/O (SDIO – version 2.0)
- MultiMediaCard (MMC – version 4.3)

Figure 13-41 shows the functional block diagram of the MMC controller.

Figure 13-41 Functional block diagram of the MMC controller



NOTE

S indicates slave interface and M indicates master interface.

Connected to the system through the internal bus, the MMC controller consists of the following parts:

- Command path

  It is used to transmit commands and receive responses.
- Data path

  It is used to perform data read and write operations by working with the command path.
- Interface clock control unit

  It is used to change the frequency of the interface clock as required and enable or disable the interface clock. SDIO_CLK_OUT can be generated by dividing CCLK_IN.

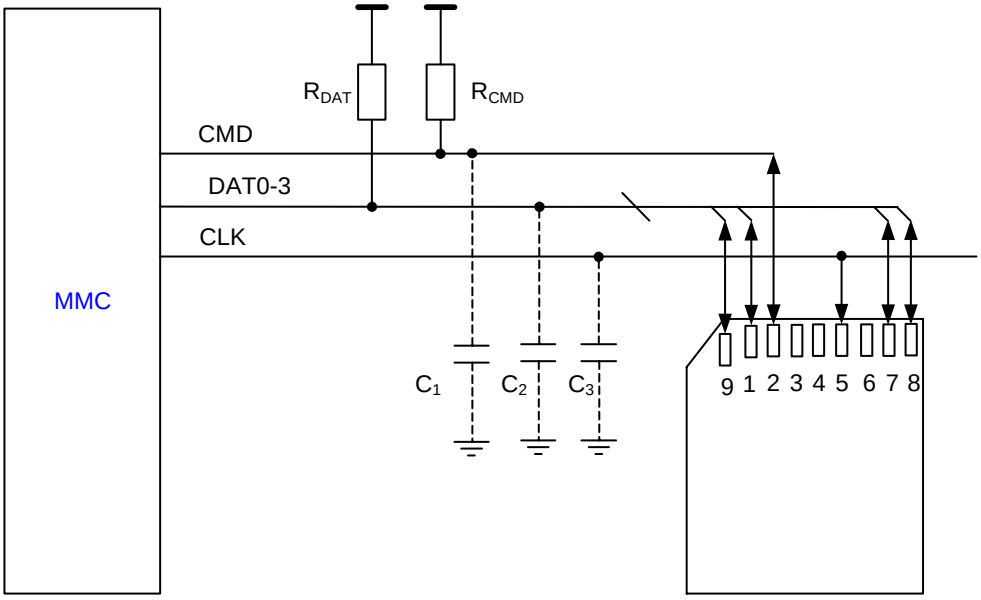
The MMC controller has the following features:

- Transfers data by using the internal direct memory access controller (IDMAC).
- Supports one transmit FIFO and one receive FIFO. The depth of each FIFO is 256 words.
- Supports configurable burst size during DMA transfer and configurable FIFO threshold.
- Supports FIFO overflow and underflow interrupts to avoid errors during data transfer.
- Supports the cyclic redundancy check (CRC) generation and check for data and commands.
- Supports programmable frequency of the interface clock.
- Disables the MMC clock and interface clock in low-power mode.
- Supports 1-bit or 4-bit data width based on the connected component.
- Reads or writes data blocks with the size of 1 byte to 65,535 bytes.
- Reads/writes stream data from/to the MMC card.
- Supports the suspend operation, resume operation, and read wait operation on the SDIO card.

Typical Application

Figure 13-42 shows the typical application circuit of the MMC controller.

Figure 13-42 Typical application circuit of the MMC controller



The MMC controller exchanges commands and data with the connected card over a clock signal line, a bidirectional command signal line, and four bidirectional data signal lines. Both the command signal line and data signal lines work in pull-up mode. Table 13-13 describes the pull-up resistors and the load capacitance of each signal line.

Table 13-13 Load parameters of signal lines

Parameter	Min	Max	Description
R_{DAT} R_{CMD}	10 kΩ	100 kΩ	Pull-up resistors
Load capacitance Cx	None	30 pF	$C_x = C_{mmchost} + C_{bus} + C_{card}$The maximum capacitance of each card (C_{card}) is 10 pF; therefore, the sum of $C_{mmchost}$ and C_{bus} must be less than 30 pF.
Inductance of each signal line	None	16 nH	Fpp ≤ 20 MHz

CAUTION

Besides the signal lines in Figure 13-33, the card slot also provides the mechanical write protection signal and card detection signal. However, the signal interfaces are not provided in Figure 13-33.

Commands and Responses

All interactions between the MMC controller and the card, including initializing the card, reading/writing to registers, querying the status, and transferring data, are implemented by using commands.

A MMC command is a segment of 48-bit serial data consisting of a start bit, a transmission bit, a command sequence, a CRC bit, and an end bit. After receiving a command, the card returns a 48-bit or a 136-bit response based on the command type.

Figure 13-43 Format of an MMC command

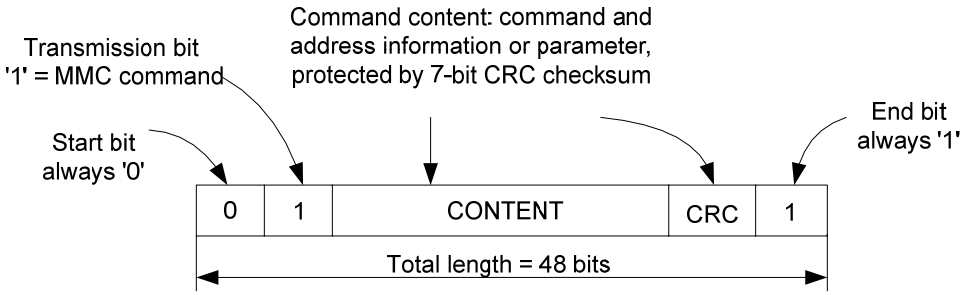
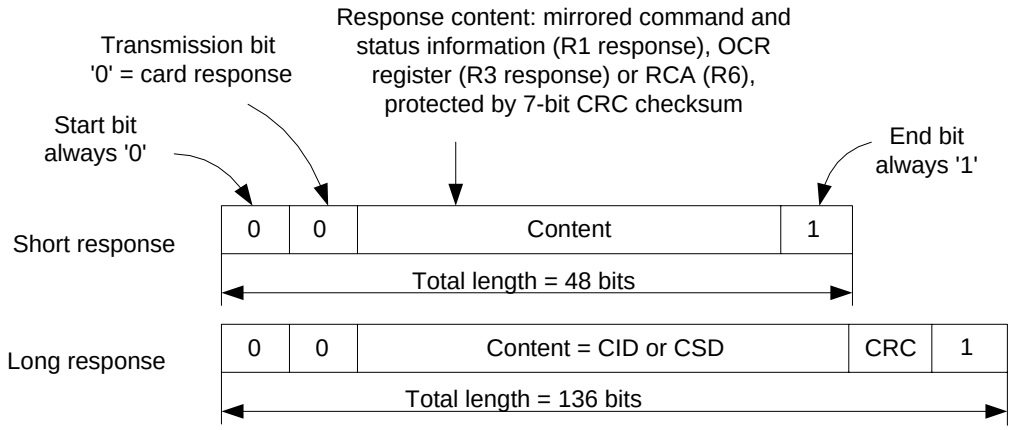


Figure 13-44 Format of the response to an MMC command



Commands are classified into the following two types based on whether data is transferred:

- Non-data transfer command

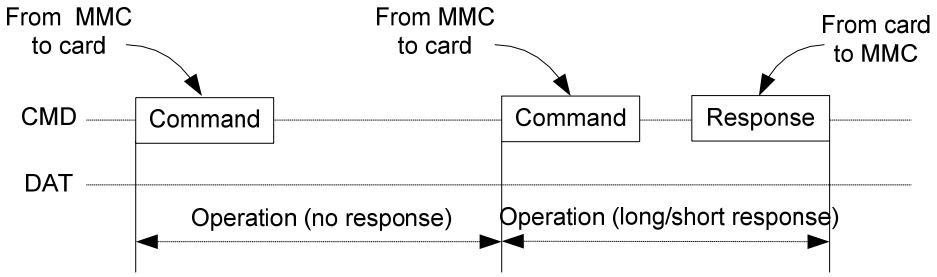
  The MMC controller transmits/receives commands to/from the card through the command signal line.
- Data transfer command

  Besides the interaction on the command line, data is also transferred through the data lines DAT0 to DAT7.

(1) Non-data transfer command

Figure 13-45 shows the operations between the MMC controller and the card by running a non-data transfer command.

Figure 13-45 Operations by running an MMC non-data transfer command



(2) Data transfer command

The MMC supports the following data transfer commands:

- Stream data read/write command

  Only the MMC card supports the stream data read/write command. In this case, only the data line DAT0 is used for data transfer, and no CRC check is performed.
- Single-block read/write command

  After this command is executed, one single data block is read and written each time. No stop command is required for stopping each data transfer.
- Multi-block read/write command
  - Predefined block count mode

    Before the multi-block read/write command is executed, the block count command is transmitted to specify the number of data blocks to be transferred.
  - Open-ended mode

    After a read/write command is transmitted, a stop command is required for stopping data transfer at the end of data transfer.

  The difference between the two modes lies on how the MMC controller notifies the card of the end of each data transfer. The SD card supports only the open-ended mode, whereas the MMC supports both modes.

  The multi-block read/write command for the SDIO card is different from the preceding two modes. To be specific, the command parameter contains the number of data blocks to be transferred when the read/write command is transmitted.

Responses are classified into the following three types:

- Command without response

  For example, the card reset command.
- Short response command

  For example, the data transfer command and card status query command.
- Long response command

  This type of commands are used to read only the information about the card identification (CID) and card specific data (CSD) registers of a card.

Data Transfer

The single-block read/write command and the multi-block read/write command are widely used during data transfer. The data block during the data transfer of the SD card and MMC is 512 bytes; the block size during the data transfer of the SDIO card can be customized

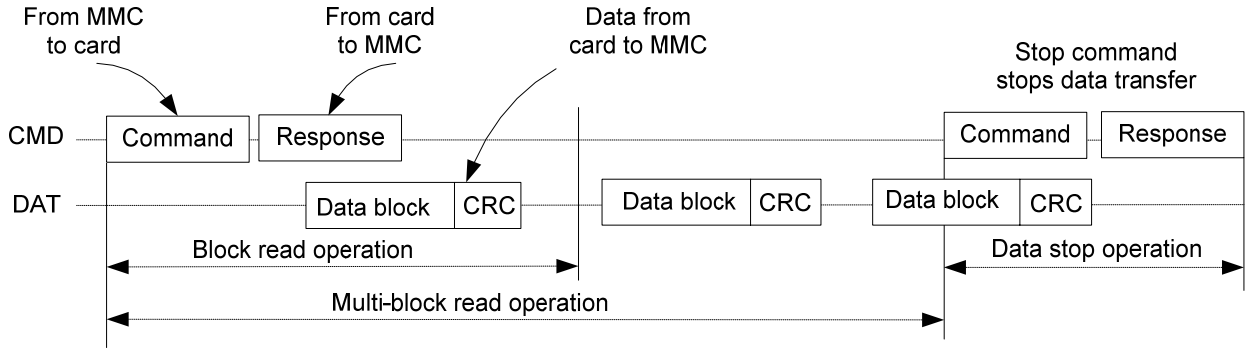
NOTE

During the data transfer by using the block read/write command, the total data amount to be transferred must be an integral multiple of the block size.

All data transfer commands are short response commands with data transferred through data lines. Figure 13-46 and Figure 13-47 show the relationships among the commands, responses, and timings of data lines.

(1) Single-block and multi-block read operations

Figure 13-46 Single-block and multi-block read operations

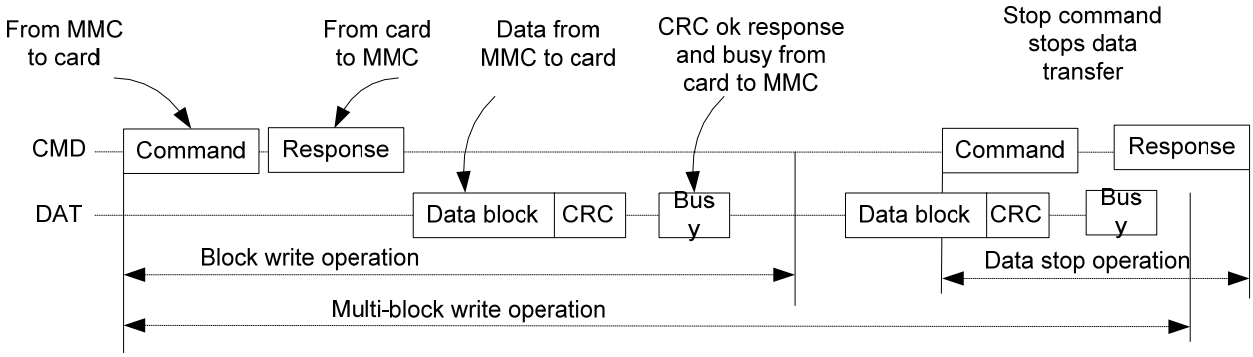


The MMC controller transmits a single-block or multi-block command to a card. When a response is being received, data is received by blocks. Each data block contains a CRC check bit for ensuring the integrity of the transferred data.

In a single-block read operation, the data transfer is completed after the MMC controller receives a data block. In a multi-block read operation, the MMC controller needs to transmit a stop command to end the data transfer after receiving multiple data blocks only in open-ended mode.

(2) Single-block and multi-block read operations

Figure 13-47 Single-block and multi-block write operations



The MMC controller transmits a single-block or multi-block command to a card. After receiving a response, the MMC controller starts to transmit data to the card by blocks. Each data block contains a CRC bit. The card performs CRC on each data block and transfers the CRC status to the MMC controller. This ensures that data is transferred properly.

In a single-block write operation, the data transfer is completed after the MMC controller transmits a data block. In a multi-block write operation, the MMC controller needs to transmit a stop command to end the data transfer after transmitting multiple data blocks only in open-ended mode. After a write operation, the card may be busy in programming the flash memory. The MMC controller can perform the next operation on the card only after it confirms that the card is not busy by querying the status of the signal line DAT0.

(3) Data transfer format

During the block read/write operations, the 1- or 4-bit data line can be used to transfer data between the MMC controller and the card. Before a data transfer command is transmitted, the data transfer widths of the MMC controller and card must be the same (1 bit or 4 bits). You can set the data bit width of the MMC controller by configuring MMC_CTYPE and set the data bit width of the card by transmitting the corresponding command.

Figure 13-48 shows the data transfer format in 1-bit mode, and Figure 13-49 shows the data transfer format in 4-bit mode.

Figure 13-48 Data transfer format in 1-bit mode

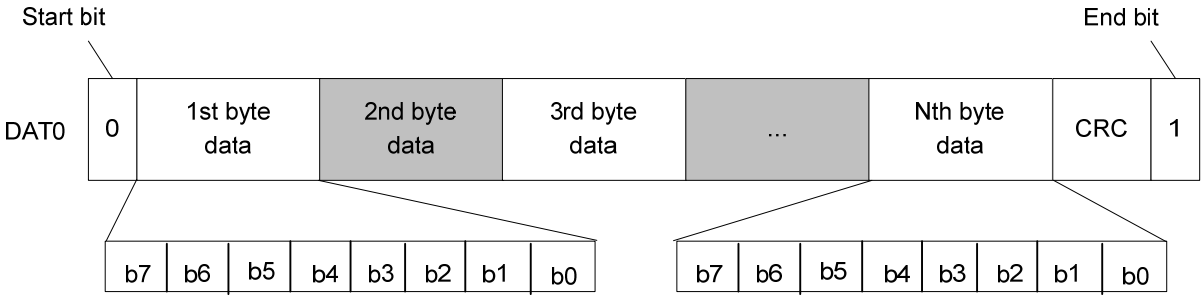
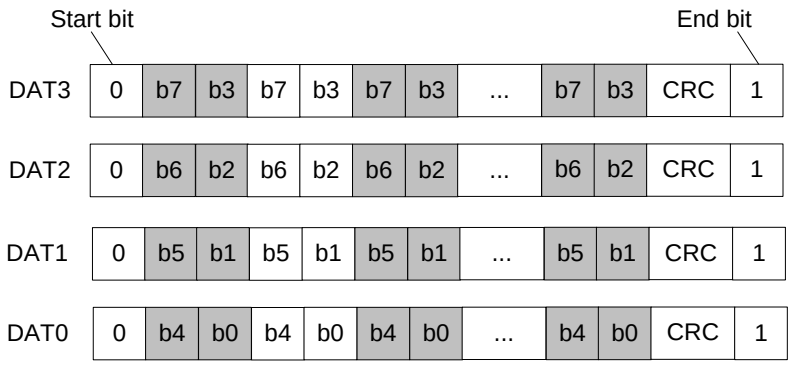


Figure 13-49 Data transfer format in 4-bit mode



13.7.2 Timing and Parameters

13.7.2.1 Timing Parameters

Table 13-14 describes the timing parameters of the MMC interface.

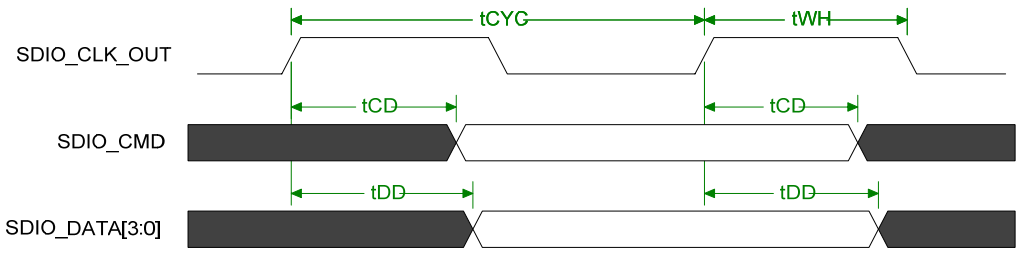
Table 13-14 Timing parameters of the MMC interface

Parameter	Description	Min	Max	Unit
tCYC	Card clock cycle	20	None	ns
tWH	High level duration of the card clock	0.5tCYC	0.5tCYC	ns
tCCLK_IN	Working clock cycle of the MMC module	20 or 41.67		ns
tCD	SDIO_CMD output delay	0.6tCCLK_IN – 5.0	0.6tCCLK_IN + 1.2	ns
tDD	SDIO_DATA output delay	0.6tCCLK_IN – 4.7	0.6tCCLK_IN + 2.1	ns
tCS	SDIO_CMD input setup time	5.0	None	ns
tCH	SDIO_CMD input hold time	0.7	None	ns
tDS	SDIO_DATA input setup time	5.3	None	ns
tDH	SDIO_DATA input hold time	0.7	None	ns

13.7.2.2 Interface Timings

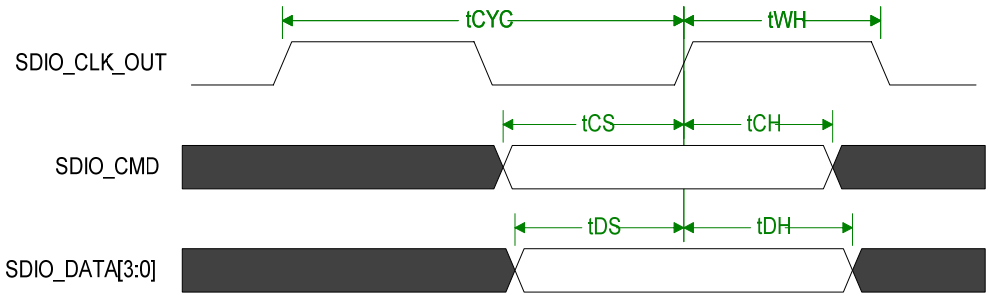
Output Timing

Figure 13-50 Output timing



Input Timing

Figure 13-51 Input timing



13.7.3 Application Notes

Clock Gating

When the software completes the current command or data transfer and does not start a new data transfer, the SDIO_CCLK_OUT clock can be disabled if the MMC controller is idle.

Perform the following steps:

1. Read MMC_STATUS.
2. If both MMC_STATUS[Command fsm_states] and MMC_STATUS[data_state_mc_busy] are 0, write 0 to MMC_CTRL to mask the MMC interrupt, enable the DMA request, and go to 3; If any of [Command fsm_states] and [data_state_mc_busy] is not 0, wait with delay, and go to step 1.
3. Write 0 to PERI_CRG49 bit[1] to disable SDIO.
4. If you need to restart the working clock, write 1 to PERI_CRG49 bit[1].

----End

Soft Reset

If the MMC controller cannot restore to the idle state due to exceptions during the data transfer, you can soft-reset the SDIO module by writing 1 toPERI_CRG49 bit[0]. In addition, you can query MMC_STATUS[Data_busy] to check whether the MMC controller is idle.

Before using the MMC controller, you are advised to soft-reset the MMC controller after hot-swapping the card.

Configuring the Working Clock

Before using the MMC controller, you need to configure the frequency of its working clock. You can set the frequency of the MMC working clock to 24 MHz or 50 MHz by configuring PERI_CRG49 bit[2].

Configuring the Interface Clock

Clock frequencies vary according to the MMCs complying with different protocols and the status of MMCs. The MMC controller provides an internal even frequency divider that generates appropriate interface clocks by dividing the frequency of the working clock. The relationship between the frequencies of the working clock CCLK_IN and the interface clock SDIO_CCLK_OUT of the MMC controller is as follows:

$F_{SDIO\_CCLK\_OUT} = F_{CCLK\_IN}/(2 \times clk\_divider)$

Where, clk_divider is the value of MMC_CLKDIV[clk_divider]. Clock frequencies vary according to card types. The maximum value of $F_{SDIO\_CCLK\_OUT}$ is 50 MHz.

Before changing the clock frequency of an MMC, ensure that no data or command is being transferred. In addition, to avoid the occurrence of glitches in the output clock of the MMC, you need to perform the following steps:

1. Disable the interface clock.

   Set MMC_CLKNA to 0x0000_0000, set MMC_CMD[Start_cmd], MMC_CMD[Update_clk_regs_only], and MMC_CMD[Wait_prvdata_complete] to 1, and wait until MMC_CMD[Start_cmd] is cleared automatically.

2. Set the clock divider.

   Configure MMC_CLKDIV based on the required clock frequency, set MMC_CMD[Start_cmd] and MMC_CMD[Update_clk_regs_only] to 1, and wait until MMC_CMD[Start_cmd] is cleared automatically.

3. Enable the interface clock again.

   Set MMC_CLKENA to 0x0000_0001, set MMC_CMD[Start_cmd] and MMC_CMD[Update_clk_regs_only] to 1, and wait until MMC_CMD[Start_cmd] is cleared automatically.

----End

CAUTION

The values of MMC_CMD and MMC_CMD are loaded only after MMC_CLKDIV[Start_cmd] and MMC_CLKENA[Update_clk_only] are set to 1. After the values are loaded successfully, the MMC controller clears MMC_CMD[Start_cmd] automatically. If a command is being executed, a hardware locked error (HLE) interrupt is generated. In this case, you need to clear the interrupt, and then transmit a command again.

When a command is being executed or data is being transferred, the clock parameter values of the card cannot be changed.

Initialization

Before commands and data are exchanged between a card and the MMC controller, the MMC controller needs to be initialized. Perform the following steps:

1. Configure the frequency of the working clock of the MMC controller. For details, see "Working Clock Configuration" in section 13.7.3 "Application Notes."
2. Soft-reset the MMC controller after the card is powered on and the command and data signal lines are pulled up and become stable. For details, see "Soft Reset" in section 13.7.3 "Application Notes."
3. Clear interrupts. Set all bits of MMC_RINTSTS bit[15:0] to 1 to clear raw interrupt status bits.
4. Configure MMC_INTMASK. Set all bits of MMC_INTMASK bit[15:0] to 1 to enable all interrupt sources.

   If data is transferred in DMA mode, set MMC_INTMASK bit[4] and MMC_INTMASK bit[5] to 0 to mask the transmit/receive FIFO data request interrupts.
5. Set MMC_CTRL[Int_enable] to 1 to enable the MMC interrupt.
6. Configure the timeout parameter register MMC_TMOUT.
7. Configure the FIFO parameter register MMC_FIFOTH.

----End

After the preceding steps, the interface clock can be configured and commands can be transmitted to the card.

Non-Data Transfer Command

If the MMC controller receives a response (correct response, error response, or timeout response) after transmitting a command, the MMC controller sets MMC_RINTSTS bit[2] to 1. Short responses are stored in MMC_RESP0, and long responses are stored in MMC_RESP0 to MMC_RESP3. MMC_RESP3 bit[31] is the MSB, and MMC_RESP0 bit[0] is the LSB. After a command is transmitted, its error status is reflected by the response command and the corresponding error bit of MMC_RINTSTS.

To transmit a non-data transfer command, perform the following steps:

1. Set the corresponding command parameters of MMC_CMDARG.
2. Configure the command register MMC_CMD based on the description in Table 13-15.
3. Wait until the MMC controller runs the command. If the command is executed, the MMC controller clears MMC_CMD[Start_cmd] automatically.
4. Check whether an HLE interrupt is generated by MMC_RINTSTS bit[12].
5. Wait until the command is executed. If the MMC controller receives a response (correct response, error response, or timeout response), the MMC controller sets MMC_RINTSTS bit[2] to 1. This indicates that the command is executed.
6. Check whether there is any response exception and read the response value if necessary.

   You can check the response timeout error, response CRC error, and response error by reading MMC_RINTSTS bit[8], MMC_RINTSTS bit[6], and MMC_RINTSTS bit[1] respectively.

----End

CAUTION

The values of MMC_CMD, MMC_CMDARG, MMC_BYTCNT, and MMC_BLKSIZ are loaded only after MMC_CMDARG[Start_cmd] is set to 1 and MMC_CMD[Update_clock_registes_only] is set to 0. After the values are loaded successfully, the MMC controller clears MMC_CMD[Start_cmd] automatically.

If other commands are being executed, an HLE interrupt is generated. In this case, you need to perform the preceding operations again. When a non-data transfer command is executed, the values of MMC_BYTCNT and MMC_BLKSIZ are ignored.

Table 13-15 Default values of MMC_CMD when a non-data transfer command is executed

Parameter	Value	Description
Start_cmd	1	Indicates that a command starts to be transmitted.
Update_clock_registes_only	0	Indicates a non-clock parameter update command.
data_transfer_expected	0	Indicates a non-data transfer command
card_number	0	-
cmd_index	Cmd index	Command index.
send_initialization	0	Indicates that this bit is set to 1 when a command is a card reset command such as CMD0.
stop_abort_cmd	0	Indicates that this bit is set to 1 when a command is a data transfer stop command such as CMD12.
rsponse_length	0	Indicates that this bit is set to 1 when the response is a long response.
rsponse_expect	1	Indicates that this bit is set to 0 when a command is not responded, such as CMD0, CMD4, or CMD15.
Wait_prvdata_complete	1 or 0	Indicates that the MMC controller must wait until the current data transfer command is executed before transmitting another command. You are advised to set this bit to the fixed value 1 except that the command is used for querying the card status during data transfer or stopping the current data transfer.
Check_response_crc	1 or 0	Indicates whether the MMC controller checks the responded CRC bit.

Reading a Single Data Block or Multiple Data Blocks

To read a single data block or multiple data blocks, perform the following steps:

1. Write 1 to MMC_CTRL[fifo_reset] to reset the FIFO pointer, and query and wait until this bit is cleared automatically.
2. Write the number of bytes to be transmitted to MMC_BYTCNT.
3. Write the block size to MMC_BLKSIZ.
4. Write the start address for reading data to MMC_CMDARG.
5. Configure MMC_CMD according to the description in Table 13-16.

   For the SD card or MMC, you need to read a single data block by running CMD17, and read multiple data blocks by running CMD18; for the SDIO card, you need to read a single data block or multiple data blocks by running CMD53.

   The MMC controller starts to run commands after MMC_CMD is written. After commands are transferred to the bus, the cmd_done interrupt is generated.
6. Check the values of MMC_RINTSTS bit[5] and MMC_RINTSTS bit[10]. If any or both of them are 1, read the data in the FIFO by reading MMC_DATA. This ensures that the MMC controller can receive the subsequent data. In addition, check data error interrupts, that is, check the values of MMC_RINTSTS bit[7], MMC_RINTSTS bit[9], MMC_RINTSTS bit[13], and MMC_RINTSTS bit[15]. In this case, you can transmit a stop command to stop the data transfer by using the software.
7. If MMC_RINTSTS bit[3] is 1, data transfer is complete. In this case, read the remaining data in the FIFO by reading MMC_DATA.
8. If MMC_CMD[Send_auto_stop] is set to 1 during the command execution, the MMC controller automatically transmits a stop command to stop the data transfer. For details, see "Configuration for Using the Auto-Stop Function" in section 13.7.3 "Application Notes."

----End

Table 13-16 Default values of MMC_CMD when a single data block or multiple data blocks are read

Parameter	Value	Description
Start_cmd	1	Indicates that a command starts to be transmitted.
Update_clock_registes_only	0	Indicates a non-clock parameter update command.
card_number	0	-
send_initialization	0	Indicates that this bit is set to 1 when a command is a card reset command such as CMD0.
stop_abort_cmd	0	Indicates that this bit is set to 1 when a command is a data transfer stop command such as CMD12.

Parameter	Value	Description
send_auto_stop	0 or 1	For details, see "Configuration for Using the Auto-Stop Function" in section 13.7.3 "Application Notes."
transfer_mode	0	Indicates block transfer.
read/write	0	Indicates that data is read from the card.
rsponse_length	0	Indicates that all responses to data commands are short responses.
data_transfer_expected	1	Indicates a data transfer command.
rsponse_expect	1	Indicates that this bit is set to 0 when a command is not responded such as CMD0, CMD4, or CMD15.
cmd_index	Cmd index	Indicates the command index.
Wait_prvdata_complete	1 or 0	Indicates that the master device must wait until the current data transfer command is executed before transmitting another command. You are advised to set this bit to the fixed value 1 except that the command is used for querying the card status or stopping the current data transfer.
Check_response_crc	1 or 0	Indicates whether the MMC controller checks the responded CRC bit.

Writing a Single Data Block or Multiple Data Blocks

To write a single data block or multiple data blocks, perform the following steps:

1. Write 1 to MMC_CTRL[fifo_reset] to reset the FIFO pointer, and query and wait until this bit is cleared automatically.
2. Write the size of the data to be transmitted to MMC_BYTCNT.
3. Write the block size to MMC_BLKSIZ.
4. Write the start address for writing data to MMC_CMDARG.
5. Write data to the FIFO by writing to MMC_DATA. The FIFO needs to be filled with data completely at the very beginning.
6. Configure MMC_CMD according to the description in Table 13-17.

   For the SD card or MMC, you need to write a single data block by running CMD24, and write multiple data blocks by running CMD25; for the SDIO card, you need to write a single data block or multiple data blocks by running CMD53.
7. Check the values of MMC_RINTSTS bit[4] and MMC_RINTSTS bit[10]. If any or both of them are 1, fill the FIFO with data by writing to MMC_DATA. In addition, check data error interrupts, that is, check the values of MMC_RINTSTS bit[7], MMC_RINTSTS bit[9], MMC_RINTSTS bit[13], and MMC_RINTSTS bit[15]. If necessary, you can transmit a stop

command to stop the data transfer by using the software. If MMC_RINTSTS bit[3] is 1, the data transfer is complete.

8. If MMC_CMD[Send_auto_stop] is set to 1 during the command execution, the MMC controller automatically transmits a stop command to stop the data transfer. For details, see "Configuration for Using the Auto-Stop Function" in section 13.7.3 "Application Notes."
9. Query and wait until the value of MMC_STATUS[data_busy] is changed from 1 to 0.

----End

Table 13-17 Default values of MMC_CMD when a single data block or multiple data blocks are written

Parameter	Value	Description
Start_cmd	1	Indicates that a command starts to be transmitted.
Update_clock_registes_only	0	Indicates a non-clock parameter update command.
card_number	0	-
send_initialization	0	Indicates that this bit is set to 1 when a command is a card reset command such as CMD0.
stop_abort_cmd	0	Indicates that this bit is set to 1 when a command is a data transfer stop command such as CMD12.
send_auto_stop	0 or 1	For details, see "Configuration for Using the Auto-Stop Function" in section 13.7.3 "Application Notes."
transfer_mode	0	Indicates block transfer.
read_write	1	Indicates that data is written to the card.
rsponse_length	0	Indicates that all responses to data commands are short responses.
data_transfer_expected	1	Indicates a data transfer command.
rsponse_expect	1	Indicates that this bit is set to 0 when a command is not responded such as CMD0, CMD4, or CMD15.
cmd_index	Cmd index	-
Wait_prvdata_complete	1 or 0	Indicates that the master device must wait until the current data transfer command is executed before transmitting another command. You are advised to set this bit to the fixed value 1 except that the command is used for querying the card status or stopping the current data transfer.
Check_response_crc	1 or 0	Indicates whether the MMC controller checks the responded CRC bit.

Reading/Writing Stream Data

The modes of reading/writing stream data are the same as those of reading/writing data blocks, except that MMC_CMD[Transfer_mode] needs to be set to 1. During a stream data transfer, the auto-stop function is required.

Transferring Data by Using the IDMAC

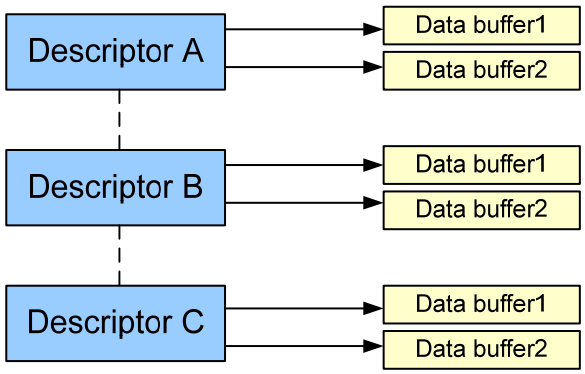
The MMC controller has an embedded IDMAC that transfers data from the original address to the destination address based on the specified descriptor.

Descriptor

The IDMAC supports the following two types of descriptors:

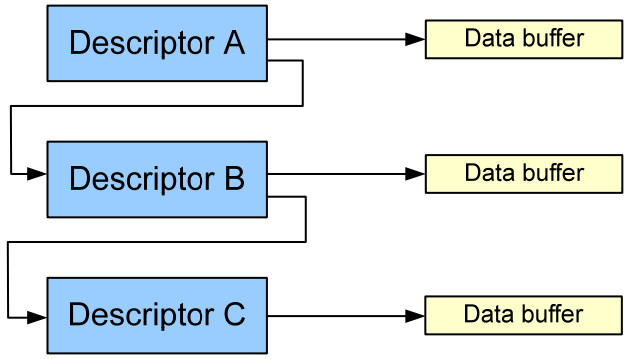
- Dual-buffer descriptor. For this type of descriptor, the span between two descriptors is determined by the DSL bit of MMC_BMOD. Figure 13-52 shows the structure of the dual-buffer descriptor.

Figure 13-52 Structure of the dual-buffer descriptor



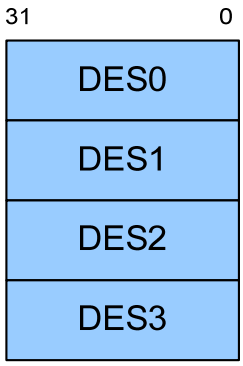
- Linked descriptor. For this type of descriptor, each descriptor points to a unique buffer and the next descriptor. Figure 13-53 shows the structure of the linked descriptor.

Figure 13-53 Structure of the linked descriptor



Each descriptor must be word-aligned, and each descriptor contains 16-byte control and status information. Figure 13-54 shows the internal structure of 32-bit descriptors.

Figure 13-54 Internal structure of 32-bit descriptors



DES0 is used to protect the control and status information. Table 13-18 describes the definition of each bit.

Table 13-18 Definition of each bit of DES0

Bits	Register	Description
31	OWN	Indicates the attributes of the descriptor. 0: The descriptor belongs to the CPU. 1: The descriptor belongs to the IDMAC. After data is transferred by using the IDMAC, the IDMAC clears this bit.
30	CES	Indicates the error status when a card is read. 0: No error occurs. 1: An error occurs.
29:6	RES	Reserved
5	ER	Indicates the link end of the descriptor. 0: The descriptor is not the last one on the link. 1: The descriptor is the last one on the link. This bit is valid only for the dual-buffer descriptor.
4	CH	Indicates the definition of the second address in DES3. 0: The second address in DES3 is the address of the second buffer. 1: The second address in DES3 is the address of the next descriptor. When this bit is 1, DES1[25:13] must be 0.
3	FS	Indicates that the descriptor contains the first data buffer when this bit is 1. If the size of the first data buffer is 0, the next descriptor contains the start data.
2	LD	Indicates that the descriptor points to the last data buffer when this bit is 1.
1	DIC	Indicates that the data transfer completion interrupt is masked when this bit is 1.

Bits	Register	Description
0	RES	Reserved

DES1 is used to specify the buffer size. Table 13-19 describes the definition of each bit of DES1.

Table 13-19 Definition of each bit of DES1

Bits	Register	Description
31: 26	RES	Reserved
25: 13	BS2	Indicates the number of bytes in the second data buffer. This value must be an integral multiple of 4. This bit is invalid when DES0[4] is 1.
12: 0	BS1	Indicates the number of bytes in the first data buffer. This value must be an integral multiple of 4.

DES2 is the address pointer of the first data buffer. Table 13-20 describes the definition of each bit of DES2.

Table 13-20 Definition of each bit of DES2

Bits	Register	Description
31: 0	BAP1	Indicates the physical address of the first data buffer. The address must be word-aligned.

DES3 indicates the second address. Table 13-21 describes the definition of each bit of DES3.

Table 13-21 Definition of each bit of DES3

Bits	Register	Description
31: 0	BAP2	Indicates the physical address of the second data buffer when dual-buffer descriptors are used, or indicates the physical address of the next descriptor when DES0[4] is 1.

Initialization

Perform the following steps:

1. Configure MMC_BMOD to set bus parameters.
2. Configure MMC_IDINTEN to mask unnecessary registers.
3. Create transmit/receive descriptor linked lists, configure MMC_DBADDR, and set the start address.

4. The IDMAC attempts to obtain descriptors from the descriptor linked lists.

----End

Transmission

Perform the following steps:

1. Create the descriptors DES0 to DES3 by using the CPU, set DES0 bit[31] (OWN bit) to 1, and provide data buffers.
2. Write data commands to MMC_CMD.
3. Set TX_Wmark by using MMC_FIFOTH.
4. The IDMAC obtains descriptors and check whether the value of the OWN bit is 1. If the OWN bit is not 1, wait until the CPU releases descriptors. During this process, the IDMAC enters the suspend state. Therefore, the CPU needs to configure MMC_PLDMND to enable the IDMAC to obtain descriptors again.
5. The IDMAC transfers data from data buffers to the internal FIFO of the MMC controller when the OWN bit is 1.
6. If the interrupts are enabled, the corresponding bit of the IDMAC status register MMC_IDSTS is updated and the OWN bit is cleared after data transfer.

----End

Reception

Perform the following steps:

1. Create the descriptors DES0 to DES3 by using the CPU, and set the DES0 bit[31] (OWN bit) to 1.
2. Write read commands to MMC_CMD.
3. Set RX_WMark by using MMC_FIFOTH.
4. The IDMAC obtains descriptors and check whether the value of the OWN bit is 1. If the OWN bit is not 1, wait until the CPU releases descriptors. During this process, the IDMAC enters the suspend state. Therefore, the CPU needs to configure MMC_PLDMND to enable the IDMAC to obtain descriptors again.
5. The IDMAC transfers data from the internal FIFO of the MMC controller to the external data buffers when the OWN bit is 1.
6. If the interrupts are enabled, the corresponding bit of the IDMAC status register MMC_IDSTS is updated and the OWN bit is cleared after data transfer.

----End

Auto-Stop Function Configuration

When multiple data blocks are read or written, a stop command is required to stop each data transfer. The stop command can be transmitted in non-data transfer command mode or by using the auto-stop function.

The auto-stop function is applicable in the following scenarios:

- SD card

  Multi-block read/write operation by running CMD18 or CMD25
- MMC
  - Stream data read/write operation
  - Multi-block read/write operation in open-ended mode by running CMD18 or CMD25

Before using the auto-stop function of the MMC controller, you are advised to perform the followings steps:

1. Set MMC_CMD[Send_auto_stop] to 1 during the block transfer command operation.
2. After data transfer, the MMC controller automatically transmits a stop command to enable the card to restore to the corresponding state.
3. Read MMC_RINTSTS[auto_cmd_done] to check whether the stop command is executed. The response is stored in MMC_RESP1.

----End

Stopping or Aborting the Data Transfer

The stop command is used to interrupt the data transfer between the MMC controller and the card, whereas the abort command is used to interrupt the I/O data transfer only in SDIO_IOONLY or SDIO_COMBO mode.

The two commands are used as follows:

- Stop command

  This command can be transmitted at any time during data transfer, because this command is used to stop the data transfer. In this case, you need to set MMC_CMD bit[5:0] to CMD12, MMC_CMD bit[14] to 1, and MMC_CMD bit[13] to 0.
- Abort command

  This command is available only for SDIO_IOONLY or SDIO_COMBO. To abort the data transfer, you need to configure the CCCR[ASx] register of the SDIO card by running the CMD52 command.

Suspend and Resume Operations

An SDIO card can store the data of a maximum of seven functional devices. The MMC controller can suspend the data transfer of a device by performing the suspend operation. Then the SD interface bus is available for another device with higher priority. After the device with higher priority transfers data, the MMC controller can resume the suspended data transfer of the previous device.

The suspend and resume operations are implemented by configuring the corresponding bits of the CCCR register of the SDIO card. The CCCR register is written or read by running the CMD52 command.

To implement a suspend operation, perform the following steps:

1. Query the SBS bit of the CCCR register to check whether the SDIO card supports suspend and resume operations.
2. Query the FSx and bus status (BS) bits of the CCCR register to check whether the functional device to be suspended is transferring data.

If the BS bit is 1, the device specified by the FSx bit is transferring data.

3. Set the bus release (BR) bit of the CCCR register to 1 to suspend the current data transfer.
4. Check whether the BS and the BR bits of the CCCR register are cleared.

   The BS bit retains 1 when the data bus is being used. The BR bit retains 1 before the bus is released completely. When both the BR and BS bits are 0, the data transfer of the selected functional device is suspended.
5. If the current read operation is suspended, MMC_CTRL[Abort_read_data] needs to be set to 1 to restart the data transfer function of the MMC controller after the suspend operation. Then MMC_CTRL[Abort_read_data] is cleared automatically.
6. Read MMC_TCBCNT to query the number of transferred bytes.

----End

To implement a resume operation, perform the following steps:

1. Query the transfer status of the card to check whether the bus is idle.
2. If the card is disconnected, run the CMD7 command to select it. The card status can be queried by running the CMD52 or CMD53 command.
3. Check whether the device to be resumed is ready for data transfer by querying the RF bit of the CCCR register. If the RF bit is 1, the device is ready for data transfer.
4. Run the CMD52 command to write the device ID to the FS bit of the CCCR register to resume the data transfer, and enable the MMC controller to enter the data transfer state (that is, write the block size to MMC_BLKSIZ, and write the amount of remaining data to be transferred to MMC_BYTCNT).

   For details about the configuration of MMC_CMDARG, see Table 13-22. The configuration of MMC_CMD is similar to the configuration during block transfer.
5. The data transfer is resumed after the CMD52 command is transmitted successfully. Read the resume data flag (DF) bit of the SDIO device. If this bit is 1, data transfer starts when the transfer function is resumed. If this bit is 0, no data is ready for transferring.
6. If the DF bit is 0, the MMC generates a data timeout error interrupt a period of time later during data read.

----End

Table 13-22 Reference configuration of MMC_CMDARG when the resume operation is performed

MMC_CMDARG	Value	Description
Bit[31]	1	Indicates the read/write flag.
Bit[30:28]	0	Indicates the ID of a functional device that accesses the CCCR register.
Bit[27]	1	Indicates the real-time flag, that is, write-to-read.
Bit[26]	None	-

MMC_CMDARG	Value	Description
Bit[25:9]	0x0D	Indicates the register address.
Bit[8]	None	-
Bit[7:0]	ID of the functional device that is resumed	Indicates write data.

CAUTION

The MMC controller cannot be woken up after the system enters the low-power mode.

Read Wait Operation

The read wait operation is performed to suspend the data transfer of the device that is using the SDIO card. The MMC controller determines the duration of pausing the data transfer.

To implement a read wait operation, perform the following steps:

1. Check whether the card supports the read wait operation.

   You can read the SRW bit of the CCCR register by running the CMD52 command. If the SRW bit is 1, all the devices supporting the card support the read wait operation.

2. Set MMC_CTRL[Read_wait] to 1.

3. If you want to resume the data transfer, clear MMC_CTRL[Read_wait].

----End

13.7.4 Register Summary

Table 13-23 describes the MMC registers.

Table 13-23 Summary of MMC registers (base address: 0x1002_0000)

Offset Address	Register	Description	Page
0x0000	MMC_CTRL	MMC control register	13-120
0x0004	MMC_PWREN	Power_en control register	13-121
0x0008	MMC_CLKDIV	Clock divider register	13-122
0x000C	MMC_CLKSRC	Clock source select register of the SD card	13-122
0x0010	MMC_CLKENA	Clock enable register	13-123
0x0014	MMC_TMOUT	Timeout register	13-124
0x0018	MMC_CTYPE	Card type register	13-124

Offset Address	Register	Description	Page
0x001C	MMC_BLKSIZ	Block size configuration register	13-125
0x0020	MMC_BYTCNT	Block transfer count register	13-125
0x0024	MMC_INTMASK	Interrupt mask register	13-125
0x0028	MMC_CMDARG	Command parameter register	13-126
0x002C	MMC_CMD	Command register	13-127
0x0030	MMC_RESP0	Response register 0	13-130
0x0034	MMC_RESP1	Response register 1	13-130
0x0038	MMC_RESP2	Response register 2	13-130
0x003C	MMC_RESP3	Response register 3	13-131
0x0040	MMC_MINTSTS	Masked interrupt status register	13-131
0x0044	MMC_RINTSTS	Raw interrupt status register	13-132
0x0048	MMC_STATUS	Status register	13-133
0x004C	MMC_FIFOTH	FIFO threshold register	13-135
0x0050	MMC_CDETECT	Card detection register	13-136
0x0054	MMC_WRTPRT	Card write protection register	13-136
0x005C	MMC_TCBCNT	Count of bytes transmitted to the card register	13-137
0x0060	MMC_TBBCNT	Count of bytes transmitted from the bus interface unit (BIU) FIFO register	13-137
0x0080	MMC_BMOD	Bus mode register	13-138
0x0084	MMC_PLDMND	Poll demand register	13-139
0x0088	MMC_DBADDR	Base address register of the descriptor linked list	13-139
0x008C	MMC_IDSTS	IDMAC status register	13-139
0x0090	MMC_IDINTEN	IDMAC interrupt enable register	13-141
0x0094	MMC_DSCADDR	Address register of the current descriptor	13-142
0x0098	MMC_BUFADDR	Address register of the current data buffer	13-142
0x0100	MMC_DATA	Data register (entrance address of the FIFO)	13-143

13.7.5 Register Description

MMC_CTRL

MMC_CTRL is a MMC control register.

Offset Address	Register Name	Total Reset Value
0x0000	MMC_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						Use_internal_dmac	reserved																Abort_read_data	Send_irq_response	Read_wait	Dma_enable	Int_enable	reserved	Dma_reset	Fifo_reset	Controller_reset
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.
[25]	RW	Use_internal_dmac	Whether to transfer data by using the IDMAC. 0: The CPU transfers data by using the slave interface. 1: The CPU transfers data by using the IDMAC.
[24]	-	reserved	Reserved.
[23:9]	-	reserved	Reserved.
[8]	RW	Abort_read_data	Whether to abort the data transfer during data read. 0: invalid 1: After transmitting a suspend command during data read, the software polls the card to check when suspend occurs. After the suspend occurs, the software sets the bit to 1. This enables the data transfer state machine to be restored to idle state for the next block transfer. After the state machine restores to the idle status, this bit is cleared automatically.
[7]	RW	Send_irq_response	Transmit interrupt response control. 0: invalid 1: An interrupt request (IRQ) response is transmitted automatically. After the response is transmitted, this bit is cleared automatically. To wait for the interrupt generated by the MMC controller, the host transmits the CMD40 command and waits for the interrupt response from the MMC controller. If you do not want the host to keep in the interrupt wait state, set this bit to 1 and transmit the CMD40 command to restore the host to the idle state.

[6]	RW	Read_wait	Read wait control. 0: disabled 1: enabled This bit is valid only for the SDIO card that supports the read wait function.
[5]	RW	Dma_enable	Reserved. The system uses the IDMAC.
[4]	RW	Int_enable	Global interrupt enable. 0: disabled 1: enabled The interrupt output is valid only when this bit is valid and the interrupt source is enabled.
[3]	-	reserved	Reserved.
[2]	RW	Dma_reset	Soft reset control for the IDMAC. 0: invalid 1: reset the internal DMA interface This bit is automatically reset after two AHB clock cycles.
[1]	RW	Fifo_reset	Soft reset control for the internal FIFO. 0: invalid 1: reset the FIFO pointer This bit is reset automatically after the reset operation is complete.
[0]	RW	Controller_reset	Soft reset control for the controller. 0: invalid 1: reset the MMC/SD/SDIO host module

MMC_PWREN

MMC_PWREN is a Power_en control register.

Offset Address	Register Name	Total Reset Value
0x0004	MMC_PWREN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															Power_enable

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	Power_enable	Power control. 0: power off 1: power on This value is used to drive the SDIOn_CARD_POWER_EN (n = 0 or 1) pin.

MMC_CLKDIV

MMC_CLKDIV is a clock divider register that shows the ratio of the frequency of the module output clock to the frequency of the input clock. For example, if the module input clock is 40 MHz and the register value is set to 1, the output clock is 20 MHz.

The clock divider is 2 x N. If the value of *N* is 0x0, it indicates no frequency division (2 x 0 = 0); if the value of *N* is 0x1, the frequency is divided by 2; if the value of *N* is 0xFF, the frequency is divided by 510.

Offset Address	Register Name	Total Reset Value
0x0008	MMC_CLKDIV	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								Clk_divider0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved.
[7:0]	RW	Clk_divider0	Clock divider 0. The clock divider is 2 x N. If the value of N is 0, it indicates no frequency division; if the value of N is 0x1, the frequency is divided by 2; if the value of N is 0xFF, the frequency is divided by 510.

MMC_CLKSRC

MMC_CLKSRC is a clock source select register of the SD card.

Offset Address	Register Name	Total Reset Value
0x000C	MMC_CLKSRC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															Clk_source
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	Clk_source	This bit must be set to 0.

MMC_CLKENA

MMC_CLKENA is a clock enable register.

Offset Address	Register Name	Total Reset Value
0x0010	MMC_CLKENA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															Cclk_low_power	reserved															Cclk_enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	-	reserved	Reserved.
[16]	RW	Cclk_low_power	Card low-power control for disabling the card clock. 0: non lower-power mode 1: low-power mode When the card is idle, the card clock is disabled. This function is used only for the MMC and SD card, because the card clock of the SDIO card must be retained for detecting interrupts.
[15:1]	RW	reserved	Reserved.
[0]	RW	Cclk_enable	Card clock enable. 0: disabled 1: enabled

MMC_TMOUT

MMC_TMOUT is a timeout register.

Offset Address	Register Name	Total Reset Value
0x0014	MMC_TMOUT	0xFFFF_FF40

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Data_timeout																								response_timeout							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	Data_timeout	Timeout during the data transfer of the card, in unit of the mmc_clk cycle of the card. The timeout is also the data starvation timeout of the CPU
[7:0]	RW	response_timeout	Response timeout, in unit of the mmc_clk cycle of the card.

MMC_CTYPE

MMC_CTYPE is a card type register.

Offset Address	Register Name	Total Reset Value
0x0018	MMC_CTYPE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															Card_width	reserved															Card_width1
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	-	reserved	Reserved.
[16]	RW	Card_width_0	Bus width of the card. This field must be set to 0 (non 8-bit mode). The bus width of the card is set to 1-bit mode or 4-bit mode, which depends on the value of bit[0].
[15:1]	RW	reserved	Reserved.
[0]	RW	Card_width_1	Bus width of the card. 0: 1-bit mode 1: 4-bit mode

MMC_BLKSIZ

MMC_BLKSIZ is a block size configuration register.

Offset Address	Register Name	Total Reset Value
0x001C	MMC_BLKSIZ	0x0000_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																Block_size															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved.
[15:0]	RW	Block_size	Block size. The initial size of each block is 512 bytes.

MMC_BYTCNT

MMC_BYTCNT is a block transfer count register.

Offset Address	Register Name	Total Reset Value
0x0020	MMC_BYTCNT	0x0000_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Byte_count																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	Byte_count	Number of transferred bytes. The number must be an integral multiple of the block size. If the data transfer is not block transfer, this register must be set to 0. In this case, the software needs to transmit a stop or an abort command to control the data transfer.

MMC_INTMASK

MMC_INTMASK is an interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x0024	MMC_INTMASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	17	16	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												Sdio_int_mask			Int_mask															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	-	reserved	Reserved.
[16]	RW	Sdio_int_mask	SDIO interrupt mask. 0: masked 1: enabled
[15:0]	RW	Int_mask	Interrupt mask. 0: masked 1: enabled Bit[15]: end-bit error (read)/write no CRC (EBE) Bit[14]: auto command done (ACD) Bit[13]: start-bit error (SBE) Bit[12]: hardware locked write error (HLE) Bit[11]: FIFO underrun/overrun error (FRUN) Bit[10]: data starvation-by-host timeout (HTO) Bit[9]: data read timeout (DTO) Bit[8]: response timeout (RTO) Bit[7]: data CRC error (DCRC) Bit[6]: response CRC error (RCRC) Bit[5]: receive FIFO data request (RXDR) Bit[4]: transmit FIFO data request (TXDR) Bit[3]: data transfer over (DTO) Bit[2]: command done (CD) Bit[1]: response error (RE) Bit[0]: card detect (CD)

MMC_CMDARG

MMC_CMDARG is a command parameter register.

Offset Address	Register Name	Total Reset Value
0x0028	MMC_CMDARG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Cmd_arg																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	Cmd_arg	Command parameter that is transferred to the card. The command parameter is related to the protocol, and each command corresponds to a command parameter.

MMC_CMD

MMC_CMD is a command register.

Offset Address	Register Name	Total Reset Value
0x002C	MMC_CMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Start_cmd	reserved			Boot_mode	Disable_boot	Expect_boot_ack	Enable_boot	reserved		Update_clock_registes_only	Card_number					Send_initialization	Stop_abort_cmd	wait_prvdata_complete	Send_auto_stop	Transfer_mode	Read_write	data_transfer_expected	Check_repsonse_crc_	Response_length		Response_expect	Cmd_index				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	Start_cmd	Start control. 0: do not start 1: start a command After the command is transferred to the card interface unit (CIU), this bit is cleared. The CPU does not allow modifications to this register. Otherwise, an HLE interrupt is generated. After transmitting a command, the CPU queries this bit, and transmits the next command when the value of this bit changes to 0.
[30:28]	-	reserved	Reserved.

[27]	RW	Boot_mode	Boot mode. 0: boot mode 1: alternative boot mode
[26]	RW	Disable_boot	Boot disable. If the software enables this bit and the Start_cmd bit at the same time, the controller aborts the boot operation. The Enable_boot and Disable_boot bits cannot be enabled at the same time.
[25]	RW	Expect_boot_ack	Boot response enable. If the software enables this bit and the Enable_boot bit at the same time, the controller detects the boot response signal in "0 – 1 – 0" sequence.
[24]	RW	Enable_boot	Boot enable. This bit is available when the boot mode is mandatory. If the software enables this bit and the Start_cmd bit, the controller pulls down the CMD signal to start the boot process. The Enable_boot and Disable_boot bits cannot be enabled at the same time.
[23:22]	-	reserved	Reserved.
[21]	RW	Update_clock_registes_only	Automatic update. 0: The normal command sequence is used. That is, the values of MMC_CMD, MMC_CMDARG, MMC_TMOUT, MMC_CTYPE, MMC_BLKSIZ, and MMC_BYTCNT are transferred from the BIU to the CIU. The CIU uses the new values of registers when running new commands. 1: No command is transmitted, and only the clock register values in the card clock domain are updated. The values of MMC_CLKDIV, MMC_CLKSRC, and MMC_CLKENA are transferred to the card clock domain. The card clock can be changed (frequency change and clock enable) even no command is transmitted. Each time the card clock is changed; this bit must be set to 1. In this case, no command is transmitted to the card, and no command done interrupt is generated.
[20:16]	RW	Card_number	Serial number of the card that is being used.
[15]	RW	Send_initialization	Whether to transmit the initialization sequence. 0: do not transmit the initialization sequence before transmitting the Send_initialization command (high level in 80 clock cycles) 1: transmit the initialization sequence before transmitting the Send_initialization command When a card is powered on, the initialization sequence must be transmitted for initialization before any command is transmitted. That is, this bit must be set to 1.

[14]	RW	Stop_abort_cmd	Whether to transmit the stop/abort command when data is being transferred in open-ended mode or in fixed length mode. 0: do not transmit the stop/abort command 1: transmit the stop/abort command for stopping the current data transfer
[13]	RW	wait_prvdata_complete	Whether to transmit a command immediately. 0: transmit a command immediately even though the previous data transfer is not complete 1: transmit a command only when the previous data transfer is complete The typical value is 0. If this bit is set to 0, the transfer status can be read during data transfer, and the interrupt transfer is supported.
[12]	RW	Send_auto_stop	Whether to transmit the stop command. 0: do not transmit the stop command after data transfer 1: transmit the stop command after data transfer In non-data transfer mode, this bit is ignored.
[11]	RW	Transfer_mode	Transfer mode. 0: block transfer mode 1: stream transfer mode In non-data transfer mode, this bit is ignored.
[10]	RW	Read_write	Read/write control. 0: read data from the card 1: write data to the card In non-data transfer mode, this bit is ignored.
[9]	RW	data_transfer_expected	Data transfer indicator. 0: No data is output from the card. 1: Data is output from the card.
[8]	RW	Check_repsonse_crc_	Whether to perform the CRC check. 0: do not check the CRC response 1: check the CRC response No valid CRC is returned when some commands are responded. To prevent the host from performing CRC, the software needs to disable this function based on related commands.
[7]	RW	Response_length	Response length. 0: Short responses are output from the card 1: Long responses are output from the card The length of a long response is 128 bits, whereas the length of a short response is 32 bits.
[6]	RW	Response_expect	Whether to output response. 0: No response is output from the card. 1: Responses are output from the card.

[5:0]	RW	Cmd_index	Command index.

MMC_RESP0

MMC_RESP0 is response register 0.

Offset Address	Register Name	Total Reset Value
0x0030	MMC_RESP0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Response0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	Response0	Bit[31:0] of a response.

MMC_RESP1

MMC_RESP1 is response register 1.

Offset Address	Register Name	Total Reset Value
0x0034	MMC_RESP1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Response1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	Response1	Bit[63:32] of a long response. After the CIU transmits an auto-stop command, the corresponding response is stored in this register, and the response to the previous command is still stored in MMC_RESP0. The auto-stop command is available only during data transfer, and the corresponding response is always a short response.

MMC_RESP2

MMC_RESP2 is response register 2.

Offset Address	Register Name	Total Reset Value
0x0038	MMC_RESP2	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	Response2							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	Response2	Bit[95:64] of a long response.

MMC_RESP3

MMC_RESP3 is response register 3.

Offset Address	Register Name	Total Reset Value
0x003C	MMC_RESP3	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	Response3							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	Response3	Bit[127:96] of a long response.

MMC_MINTSTS

MMC_MINTSTS is a masked interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0040	MMC_MINTSTS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			Sdio_interrupt	Int_status			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:17]	-	reserved	Reserved.

[16]	RO	Sdio_interrupt	SDIO interrupt mask status. The SDIO interrupt is valid only when MMC_INTMASK [sdio_int_mask] is enabled. 0: No SDIO interrupt is output from the card. 1: An SDIO interrupt is output from the card.
[15:0]	RO	Int_status	Status of each interrupt. Bit[15]: end-bit error (read)/write no CRC (EBE) Bit[14]: auto command done (ACD) Bit[13]: start-bit error (SBE) Bit[12]: hardware locked write error (HLE) Bit[11]: FIFO underrun/overrun error (FRUN) Bit[10]: data starvation by the host timeout (HTO) Bit[9]: data read timeout (DTO) Bit[8]: response timeout (RTO) Bit[7]: data CRC error (DCRC) Bit[6]: response CRC error (RCRC) Bit[5]: receive FIFO data request (RXDR) Bit[4]: transmit FIFO data request (TXDR) Bit[3]: data transfer over (DTO) Bit[2]: command done (CD) Bit[1]: response error (RE) Bit[0]: card detect (CD)

MMC_RINTSTS

MMC_RINTSTS is a raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0044	MMC_RINTSTS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17	16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				Sdio_interrupt	Int_status			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:17]	-	reserved	Reserved.

[16]	RW	Sdio_interrupt	Raw SDIO interrupt status. 0: No SDIO interrupt is output from the card. 1: An SDIO interrupt is output from the card. The value of the interrupt status bit is independent of the interrupt mask status.
[15:0]	RW	Int_status	Raw status of each interrupt. Writing 1 clears the bits, and writing 0 has no effect. The value of the interrupt status bit is independent of the interrupt mask status. Bit[15]: end-bit error (read)/write no CRC (EBE) Bit[14]: auto command done (ACD) Bit[13]: start-bit error (SBE) Bit[12]: hardware locked write error (HLE) Bit[11]: FIFO underrun/overrun error (FRUN) Bit[10]: data starvation by the host timeout (HTO) Bit[9]: data read timeout (DRTO)/Boot Data Start (BDS) Bit[8]: response timeout (RTO)/Boot Ack Received (BAR) Bit[7]: data CRC error (DCRC) Bit[6]: response CRC error (RCRC) Bit[5]: receive FIFO data request (RXDR) Bit[4]: transmit FIFO data request (TXDR) Bit[3]: data transfer over (DTO) Bit[2]: command done (CD) Bit[1]: response error (RE) Bit[0]: card detect (CD)

MMC_STATUS

MMC_STATUS is a status register.

Offset Address	Register Name	Total Reset Value
0x0048	MMC_STATUS	0x0000_0106

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				FIFO_count												Response_index					data_state_mc_busy	Data_busy	Data_3_status	Commandfsm_states					Fifo_full	Fifo_empty	Fifo_tx_watermark	Fifo_rx_watermark

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	0

Bits	Access	Name	Description
[31:30]	-	reserved	Reserved.
[29:17]	RO	FIFO_count	FIFO count.
[16:11]	RO	Response_index	Serial number of the previous response, including the response to the auto-stop command.
[10]	RO	data_state_mc_busy	0: The data transmit/receive state machine is idle. 1: The data transmit/receive state machine is busy.
[9]	RO	Data_busy	This field value depends on the reverse level of DATA0. 0: idle (DATA0 is high level) 1: busy (DATA0 is low level)
[8]	RO	Data_3_status	Card detection signal. This field value depends on the level of DATA3. 0: No card is inserted (DATA3 is low level). 1: A card is inserted (DATA3 is high level).
[7:4]	RO	Commandfsm_states	Status of the command state machine. 0x0: idle 0x1: send init sequence 0x2: Tx cmd start bit 0x3: Tx cmd tx bit 0x4: Tx cmd index +arg 0x5: Tx cmd crc7 0x6: Tx cmd end bit 0x7: Rx resp start bit 0x8: Rx resp IRQ response 0x9: Rx resp tx bit 0xA: Rx resp cmd idx 0xB: Rx resp data 0xC: Rx resp crc7 0xD: Rx resp end bit 0xE: Cmd path wait NCC 0xF: wait, CMD-to-response turnaround
[3]	RO	Fifo_full	FIFO full flag. 0: empty 1: full
[2]	RO	Fifo_empty	FIFO empty flag. 0: not empty 1: empty

[1]	RO	Fifo_tx_watermark	Whether the FIFO reaches the transmit watermark level. 0: no 1: yes
[0]	RO	Fifo_rx_watermark	Whether the FIFO reaches the receive watermark level. 0: no 1: yes

MMC_FIFOTH

MMC_FIFOTH is a FIFO threshold register.

Offset Address	Register Name	Total Reset Value
0x004C	MMC_FIFOTH	0x00FF_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				RX_Wmark												reserved				TX_Wmark											
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved.
[27:16]	RW	RX_Wmark	FIFO threshold watermark level during data read. If the data amount in the FIFO is above the threshold, a DMA request is enabled. After a data transfer, a DMA request is raised for transferring the remaining data no matter whether the threshold is reached. In non-DMA mode, the RXDR interrupt is enabled. If the data amount in the FIFO is not above the threshold after a data transfer, no interrupt is generated. In this case, the software needs to read the remaining data by querying the DTD interrupt. If a data transfer is complete in DMA mode, the DMA raises a single transfer request to read data until the DTD interrupt is generated even though the remaining data amount is below the threshold. Restriction: RX_WMark ≤ FIFO_DEPTH – 2 Recommendation: A request is raised when the value of [(FIFO_DEPTH/2) – 1] is above the threshold.
[15:12]	RW	reserved	Reserved.

[11:0]	RW	TX_Wmark	FIFO threshold watermark level during data transmit. If the data amount in the FIFO is below the threshold, a DMA request is enabled. After a data transfer, a DMA request is raised for transferring the remaining data no matter whether the threshold is reached. In non-DMA mode, the RXDR interrupt is enabled. If the data amount in the FIFO is not above the threshold after a data transfer, no interrupt is generated. In this case, the software needs to read the remaining data by querying the DTD interrupt. If a data transfer is complete in DMA mode, the DMA raises a single transfer request to read data until the DTD interrupt is generated even though the remaining data amount is below the threshold. Restriction: TX_WMark ≤ FIFO_DEPTH – 2 Recommendation: This field must be less than or equal to FIFO_DEPTH/2.

MMC_CDETECT

MMC_CDETECT is a card detection register.

Offset Address	Register Name	Total Reset Value
0x0050	MMC_CDETECT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								Card_detect_n
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RO	Card_detect_n	Card detection signal. The value depends on the SDIO_CARD_DETECT pin.

MMC_WRTPRT

MMC_WRTPRT is a card write protection register.

Offset Address	Register Name	Total Reset Value
0x0054	MMC_WRTPRT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															Write_protect
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RO	Write_protect	Card write protection signal. The value depends on the SDIO_CWPR pin.

MMC_TCBCNT

MMC_TCBCNT is a count of bytes transmitted to the card register.

Offset Address	Register Name	Total Reset Value
0x005C	MMC_TCBCNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	trans_card_byte_count																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	trans_card_byte_count	Count of bytes transmitted from the CIU to the card. When this register is accessed through a 32-bit AHB, the 32-bit data needs to be read at a time. This avoids the read-coherency error.

MMC_TBBCNT

MMC_TBBCNT is a count of bytes transmitted from the BIU FIFO register.

Offset Address	Register Name	Total Reset Value
0x0060	MMC_TBBCNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	trans_fifo_byte_count																															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	trans_fifo_byte_count	Count of bytes transferred between the CPU/DMA and BIU FIFO. When this register is accessed through a 32-bit AHB, the 32-bit data needs to be read at a time. This avoids the read-coherency error.

MMC_BMOD

MMC_BMOD is a bus mode register.

Offset Address	Register Name	Total Reset Value
0x0080	MMC_BMOD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					PBL			DE	DSL					FB	SWR
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	-	reserved	Reserved.
[10:8]	RW	PBL	Length of the IDMAC burst transfer. 000: 1 001: 4 010: 8 011: 16 1xx: reserved
[7]	RW	DE	IDMAC enable. 0: disabled 1: enabled
[6:2]	RW	DSL	Span between two descriptors, that is, number of words between two non-linked descriptors. This field is valid only for the dual-buffer descriptors.
[1]	RW	FB	Fixed burst length type. 0: single and INCR burst types 1: single, INCR4, INCR8, and INCR16 burst types

[0]	RW	SWR	Soft reset control for the internal register of the IDMAC. 0: not reset 1: reset After reset, this bit is automatically cleared one clock cycle later.

MMC_PLDMND

MMC_PLDMND is a poll demand register.

Offset Address	Register Name	Total Reset Value
0x0084	MMC_PLDMND	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PD																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	PD	If DES0[OWN] is 0, the IDMAC enters the suspend state. The CPU can write any value to this register to enable the IDMAC to obtain descriptors again.

MMC_DBADDR

MMC_DBADDR is a base address register of the descriptor linked list.

Offset Address	Register Name	Total Reset Value
0x0088	MMC_DBADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SDL																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	SDL	Start address of the descriptor linked list, that is, the base address of the first descriptor.

MMC_IDSTS

MMC_IDSTS is an IDMAC status register.

Offset Address	Register Name	Total Reset Value
0x008C	MMC_IDSTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																FSM				EB				AIS	NIS	reserved			CES	DU	reserved		FBE	RI	TI
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	-	reserved	Reserved.
[16:13]	RW	FSM	Current state of the IDMAC state machine. 0: DMA_IDLE 1: DMA_SUSPEND 2: DESC_RD 3: DESC_CHK 4: DMA_RD_REQ_WAIT 5: DMA_WR_REQ_WAIT 6: DMA_RD 7: DMA_WR 8: DESC_CLOSE This bit is read-only.
[12:10]	RW	EB	Bus error type. 001: The transmit operation is aborted. 010: The receive operation is aborted. Other values: reserved
[9]	RW	AIS	Abnormal total interrupt. The value of this bit is obtained after the values of FBE, DU, and CES bits are ORed. Writing 1 clears this bit.
[8]	RW	NIS	Normal total interrupt. The value of this bit is obtained after the values of the TI and RI bits are ORed. Writing 1 clears this bit.
[7:6]	-	reserved	Reserved.
[5]	RW	CES	Card error indicator. This bit indicates the card status when data is being received.
[4]	RW	DU	Descriptor invalid interrupt. When DES0[OWN] is 0, this bit is set to 1. Writing 1 clears this bit.
[3]	-	reserved	Reserved.
[2]	RW	FBE	Fatal bus error interrupt. If this bit is set to 1, the IDMAC stops all accesses through the bus. Writing 1 clears this bit.

[1]	RW	RI	Receive done interrupt. This bit indicates that the data of a descriptor is received. Writing 1 clears this bit.
[0]	RW	TI	Transmit done interrupt. This bit indicates that a descriptor finishes transmitting data. Writing 1 clears this bit.

MMC_IDINTEN

MMC_IDINTEN is an IDMAC interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x0090	MMC_IDINTEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						AI	NI	reserved				CES	DU	reserved		FBE	RI	TI
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	-	reserved	Reserved.
[9]	RW	AI	Abnormal interrupt enable. 0: disabled 1: The FBE, DU, and CES interrupts are enabled.
[8]	RW	NI	Normal interrupt enable. 0: disabled 1: The TI and RI interrupts are enabled.
[7:6]	-	reserved	Reserved.
[5]	RW	CES	Card error interrupt enable. 0: disabled 1: enabled
[4]	RW	DU	Descriptor invalid interrupt enable. 0: disabled 1: enabled
[3]	-	reserved	Reserved.
[2]	RW	FBE	Fatal bus error interrupt enable. 0: disabled 1: enabled

[1]	RW	RI	Receive interrupt enable. 0: disabled 1: enabled
[0]	RW	TI	Transmit interrupt enable. 0: disabled 1: enabled

MMC_DSCADDR

MMC_DSCADDR is an address register of the current descriptor.

Offset Address	Register Name	Total Reset Value
0x0094	MMC_DSCADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HAD																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	HAD	Descriptor pointer. The value is automatically refreshed during data transfer. The register points to the start address of the descriptor that will be used by the IDMAC.

MMC_BUFADDR

MMC_BUFADDR is an address register of the current data buffer.

Offset Address	Register Name	Total Reset Value
0x0098	MMC_BUFADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HBA																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	HBA	Data buffer pointer. The value is automatically refreshed during data transfer. The register points to the start address of the data buffer that is being used by the IDMAC.

MMC_DATA

MMC_DATA is a data register for storing the FIFO entrance address. Before the FIFO is read or written, MMC_STATUS[fifo_count] must be read to query the remaining space of the FIFO. This confirms the data bytes to be read or written based on the remaining space. In this way, FIFO overflow is avoided.

Offset Address	Register Name	Total Reset Value
0x0100	MMC_DATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	DATA	Address for reading/writing to the FIFO. If the address ranges from 0x100 to 0x100+FIFO_DEPTH, the FIFO is selected.

13.8 SAR ADC

13.8.1 Overview

The successive approximation register analog-to-digital converter (SAR ADC) is a 10-bit ADC that has two channels.

13.8.2 Features

The SAR ADC has the following features:

- Supports a 4 MHz working clock and a maximum of 200 kHz sampling clock.
- Supports 3.3 V analog voltage VDDA and 1.2 V digital voltage VDDD.
- Allows the maximum reference voltage VREF to be set to VDDA (3.3 V).
- Measures 0.01 VREF to 0.99 x VREF. The minimum granularity is 3.3 V/1023.
- Supports power down.
- Provides maskable conversion completion interrupts.

13.8.3 Operating Mode

13.8.3.1 Power Down

When ADC_POWERDOWN[adc_pwrdown] is 1, the SAR ADC is disabled, and analog-to-digital conversion is unavailable.

Analog-to-digital conversion is available only when ADC_POWERDOWN[adc_pwrdown] is 0.

13.8.3.2 Reset

The SAR ADC can be reset by configuring PERI_CRG32 bit[0] (sar_adc_srst_req).

To be specific, set PERI_CRG32[sar_adc_srst_req] to 1 to reset the SAR ADC, and set PERI_CRG32[sar_adc_srst_req] to 0 to deassert reset on the SAR ADC.

13.8.3.3 SAR_ADC Conversion

This section uses an ADC conversion on channel 0 as an example. To perform an ADC conversion, perform the following steps:

1. Set ADC_POWERDOWN[adc_pwrdown] to 0 and PERI_CRG32[sar_adc_cken] to 1 to enable the SAR_ADC to enter the working state.
2. Set ADC_CTRL[adc_chsel] to 0 to select channel 0.
3. Set ADC_INT_MASK[adc_int_mask] to 0 to enable the conversion completion interrupt.
4. Set ADC_CTRL[adc_start] to 1 to enable an analog-to-digital conversion.
5. Wait for the conversion completion interrupt.
6. Read ADC_RESULT[adc_result_reg] to query the conversion result.
7. Set ADC_INT_CLR[adc_int_clr] to 1 to clear the interrupt.

   To perform multiple conversions, repeat 4 to 7.

----End

13.8.4 Register Summary

Table 13-24 describes the SAR ADC registers.

Table 13-24 Summary of SAR ADC registers (base address: 0x200B_0000)

Offset Address	Register	Description	Page
0x0000	ADC_STATUS	ADC conversion status register	13-145
0x0004	ADC_CTRL	ADC conversion control register	13-145
0x0008	ADC_POWERDOWN	ADC mode control register	13-146
0x000C	ADC_INT_STATUS	Masked ADC conversion completion interrupt register	13-146
0x0010	ADC_INT_MASK	ADC conversion completion interrupt mask register	13-147
0x0014	ADC_INT_CLR	ADC conversion completion interrupt clear register	13-147
0x0018	ADC_INT_RAW	Raw ADC conversion completion interrupt register	13-148
0x001C	ADC_RESULT	ADC conversion result register	13-148

13.8.5 Register Description

ADC_STATUS

ADC_STATUS is an ADC conversion status register.

Offset Address	Register Name	Total Reset Value
0x0000	ADC_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															adc_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	WC	adc_status	ADC conversion status. The value 1 indicates that the conversion is being performed. After the conversion is complete, writing any value clears the register.

ADC_CTRL

ADC_CTRL is an ADC conversion control register.

Offset Address	Register Name	Total Reset Value
0x0004	ADC_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															adc_chsel	reserved															adc_start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	-	reserved	Reserved.
[16]	RW	adc_chsel	ADC conversion channel select. 0: channel 0 1: channel 1
[15:1]	-	reserved	Reserved.

Offset Address	Register Name	Total Reset Value
0x0004	ADC_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															adc_chsel	reserved															adc_start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[0]	RW	adc_start	ADC conversion start. Writing 1 starts a conversion. After the conversion is complete, hardware automatically sets this field to 0.

ADC_POWERDOWN

ADC_POWERDOWN is an ADC mode control register.

Offset Address	Register Name	Total Reset Value
0x0008	ADC_POWERDOWN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															adc_pwrdown
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	adc_pwrdown	ADC mode select. 0: normal mode 1: power-down mode

ADC_INT_STATUS

ADC_INT_STATUS is a masked ADC conversion completion interrupt register.

Offset Address	Register Name	Total Reset Value
0x000C	ADC_INT_STATUS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								adc_masked_int
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RO	adc_masked_int	Masked ADC conversion completion interrupt.

ADC_INT_MASK

ADC_INT_MASK is an ADC conversion completion interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x0010	ADC_INT_MASK	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								adc_int_mask
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	adc_int_mask	ADC conversion completion interrupt mask. 0: not masked 1: masked

ADC_INT_CLR

ADC_INT_CLR is an ADC conversion completion interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x0014	ADC_INT_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															adc_int_clr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RW	adc_int_clr	ADC conversion completion interrupt clear. Writing 1 clears the interrupt. After the interrupt is cleared, hardware automatically sets this field to 0.

ADC_INT_RAW

ADC_INT_RAW is a raw ADC conversion completion interrupt register.

Offset Address	Register Name	Total Reset Value
0x0018	ADC_INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															adc_raw_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved.
[0]	RO	adc_raw_int	Raw ADC conversion completion interrupt.

ADC_RESULT

ADC_RESULT is an ADC conversion result register.

Offset Address	Register Name	Total Reset Value
0x001C	ADC_RESULT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						adc_result_reg									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	-	reserved	Reserved.
[9:0]	RO	adc_result_reg	ADC conversion result.

13.9 PWM

13.9.1 Overview

The Hi3518 has a pulse width modulation (PWM) module that supports 3-channel independent outputs.

13.9.2 Features

Each channel of PWM output has the following features:

- Provides an internal 16-bit counter with configurable output frequency. The maximum frequency of the output square waves is 1.5 MHz, and the minimum frequency of the output square waves is 0.045 Hz (3 MHz/67108863).
- Allows you to set the number of high levels (26 bits).
- Provides a 10-bit counter and allows you to set the number of pulses. A maximum of 1023 pulses are supported. If the pulse output mode is set to infinite mode, there is no limitation on the number of pulses.

13.9.3 Operating Mode

The internal working clock of the PWM module is 3 MHz. Below takes PWM0 as an example to configure 1-channel PWM output:

1. Calculate the number of required cycles and high levels.
2. Set PWM0_CTRL bit[0] to 0 to disable the PWM output.
3. Write the corresponding values to PWM0_CFG0, PWM0_CFG1, and PWM0_CFG2.
4. Set PWM0_CTRL bit[0] to 1 to enable the PWM output.
5. Read back the data of PWM0_STATE0, PWM0_STATE1, and PWM0_STATE2 to verify that the configuration takes effect.

----End

For example, to output a 3 kHz waveform with 72.5% high levels and 10 pulses (the duty ratio is 72.5%), calculate the number of high levels as follows:

- Cycle = 3 MHz/1 kHz ≈ 1000 (0x00003E8 in hexadecimal)
- Number of high levels = Cycle x Duty ratio = 1000 x 72.5% = 725 (0x00002D5 in hexadecimal)

To output a desired waveform, perform the following steps:

1. Read PWM0_STATE2 bit[10] until it is 0. This indicates that the PWM module is idle and can output square waves.
2. Write 0x0 to PWM0_CTRL.
3. Write 0x0000_03E8 to PWM0_CFG0.
4. Write 0x0000_02D5 to PWM0_CFG1.
5. Write 0x0000_000A to PWM0_CFG2.
6. Write 0x1 to PWM0_CTRL.

   NOTE

   The following steps can be skipped. They are used to check whether the square wave is output as expected.

7. Read PWM0_STATE2 bit[10] until it is 1. This indicates that the PWM module is outputting square waves.
8. Read PWM0_STATE0 and compare the queried value with 0x0000_03E8.
9. Read PWM0_STATE1 and compare the queried value with 0x0000_02D5.
10. Read PWM0_STATE2 bit[9:0] and compare the queried value with 0x0A. If PWM0_STATE2 bit[10] is 1, the PWM module is outputting square waves. If PWM0_STATE2 bit[10] is 0, the configured number of square waves are output.

----End

13.9.4 Register Summary

Table 13-25 describes the PWM registers.

Table 13-25 Summary of PWM registers (base address: 0x2013_0000)

Offset Address	Register	Description	Page
0x0000	PWM0_CFG0	PWM0 configuration 0 register	13-151
0x0004	PWM0_CFG1	PWM0 configuration 1 register	13-152
0x0008	PWM0_CFG2	PWM0 configuration 2 register	13-152
0x000C	PWM0_CTRL	PWM0 control register	13-152
0x0010	PWM0_STATE0	PWM0 status 0 register	13-153
0x0014	PWM0_STATE1	PWM0 status 1 register	13-153

Offset Address	Register	Description	Page
0x0018	PWM0_STATE2	PWM0 status 2 register	13-154
0x0020	PWM1_CFG0	PWM1 configuration 0 register	13-155
0x0024	PWM1_CFG1	PWM1 configuration 1 register	13-155
0x0028	PWM1_CFG2	PWM1 configuration 2 register	13-155
0x002C	PWM1_CTRL	PWM1 control register	13-156
0x0030	PWM1_STATE0	PWM1 status 0 register	13-156
0x0034	PWM1_STATE1	PWM1 status 1 register	13-157
0x0038	PWM1_STATE2	PWM1 status 2 register	13-157
0x0040	PWM2_CFG0	PWM2 configuration 0 register	13-158
0x0044	PWM2_CFG1	PWM2 configuration 1 register	13-159
0x0048	PWM2_CFG2	PWM2 configuration 2 register	13-159
0x004C	PWM2_CTRL	PWM2 control register	13-159
0x0050	PWM2_STATE0	PWM2 status 0 register	13-160
0x0054	PWM2_STATE1	PWM2 status 1 register	13-160
0x0058	PWM2_STATE2	PWM2 status 2 register	13-161

13.9.5 Register Description

PWM0_CFG0

PWM0_CFG0 is PWM0 configuration 0 register.

Offset Address	Register Name	Total Reset Value
0x0000	PWM0_CFG0	0x0000_018F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								pwm0_period																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.
[25:0]	RW	pwm0_period	Number of cycles for PWM0. This field cannot be set to 0 or 1. Otherwise, the output level is high.

PWM0_CFG1

PWM0_CFG1 is PWM0 configuration 1 register.

Offset Address	Register Name	Total Reset Value
0x0004	PWM0_CFG1	0x0000_00C7

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								pwm0_duty																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.
[25:0]	RW	pwm0_duty	Number of level beats for PWM0. If the field value is equal to the number of cycles, the output level is always high.

PWM0_CFG2

PWM0_CFG2 is PWM0 configuration 2 register.

Offset Address	Register Name	Total Reset Value
0x0008	PWM0_CFG2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						pwm0_num									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	-	reserved	Reserved.
[9:0]	RW	pwm0_num	Number of square waves output by PWM0.

PWM0_CTRL

PWM0_CTRL is PWM0 control register.

Offset Address	Register Name	Total Reset Value
0x000C	PWM0_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													pwm0_keep	pwm0_inv	pwm0_enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	-	reserved	Reserved.
[2]	RW	pwm0_keep	PWM output mode. 0: The number of square waves output by PWM0 is fixed. 1: PWM0 always outputs square waves.
[1]	RW	pwm0_inv	PWM output control. 0: PWM0 outputs square waves in normal mode. 1: PWM0 outputs square waves in inverted mode.
[0]	RW	pwm0_enable	PWM0 enable. 0: disabled 1: enabled

PWM0_STATE0

PWM0_STATE0 is PWM0 status 0 register.

Offset Address	Register Name	Total Reset Value
0x0010	PWM0_STATE0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								pwm0_period_st																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.
[25:0]	RO	pwm0_period_st	Number of count cycles for the internal module of PWM0.

PWM0_STATE1

PWM0_STATE1 is PWM0 status 1 register.

Offset Address	Register Name	Total Reset Value
0x0014	PWM0_STATE1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								pwm0_duty_st																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.
[25:0]	RO	pwm0_duty_st	Number of high level beats for the internal module of PWM0.

PWM0_STATE2

PWM0_STATE2 is PWM0 status 2 register.

Offset Address	Register Name	Total Reset Value
0x0018	PWM0_STATE2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												pwm0_cnt_st								pwm0_keep_st	pwm0_busy	pwm0_period_st									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	-	reserved	Reserved.
[21:12]	RO	pwm0_cnt_st	Number of remaining square waves output by PWM0. This field is valid only when the following conditions are met: pwm0_busy == 1, pwm0_keep_st == 0
[11]	RO	pwm0_keep_st	Square wave output mode for the internal module of PWM0. 0: The number of output square waves is fixed. 1: Square waves are always output.
[10]	RO	pwm0_busy	Working status of PWM0. 0: Wave output is complete and PWM0 is idle. 1: PWM0 is outputting square waves.
[9:0]	RO	pwm0_period_st	Number of output square waves for the internal module of PWM0.

PWM1_CFG0

PWM1_CFG0 is PWM1 configuration 0 register.

Offset Address	Register Name	Total Reset Value
0x0020	PWM1_CFG0	0x0000_018F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								pwm1_period																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.
[25:0]	RW	pwm1_period	Number of cycles for PWM1. This field cannot be set to 0 or 1. Otherwise, the output level is high.

PWM1_CFG1

PWM1_CFG1 is PWM1 configuration 1 register.

Offset Address	Register Name	Total Reset Value
0x0024	PWM1_CFG1	0x0000_00C7

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								pwm1_duty																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.
[25:0]	RW	pwm1_duty	Number of level beats for PWM1. If the field value is equal to the number of cycles, the output level is always high.

PWM1_CFG2

PWM1_CFG2 is PWM1 configuration 2 register.

Offset Address	Register Name	Total Reset Value
0x0028	PWM1_CFG2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						pwm1_num									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	-	reserved	Reserved.
[9:0]	RW	pwm1_num	Number of square waves output by PWM1.

PWM1_CTRL

PWM1_CTRL is PWM1 control register.

Offset Address	Register Name	Total Reset Value
0x002C	PWM1_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													pwm1_keep	pwm1_inv	pwm1_enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	-	reserved	Reserved.
[2]	RW	pwm1_keep	PWM output mode. 0: The number of square waves output by PWM1 is fixed. 1: PWM1 always outputs square waves.
[1]	RW	pwm1_inv	PWM output control. 0: PWM1 outputs square waves in normal mode. 1: PWM1 outputs square waves in inverted mode.
[0]	RW	pwm1_enable	PWM1 enable. 0: disabled 1: enabled

PWM1_STATE0

PWM1_STATE0 is PWM1 status 0 register.

Offset Address	Register Name	Total Reset Value
0x0030	PWM1_STATE0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								pwm1_period_st																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.
[25:0]	RO	pwm1_period_st	Number of count cycles for the internal module of PWM1.

PWM1_STATE1

PWM1_STATE1 is PWM1 status 1 register.

Offset Address	Register Name	Total Reset Value
0x0034	PWM1_STATE1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								pwm1_duty_st																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.
[25:0]	RO	pwm1_duty_st	Number of high level beats for the internal module of PWM1.

PWM1_STATE2

PWM1_STATE2 is PWM1 status 2 register.

Offset Address	Register Name	Total Reset Value
0x0038	PWM1_STATE2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												pwm1_cnt_st								pwm1_keep_st	pwm1_busy	pwm1_period_st									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	-	reserved	Reserved.
[21:12]	RO	pwm1_cnt_st	Number of remaining square waves output by PWM1. This field is valid only when the following conditions are met: pwm1_busy == 1, pwm1_keep_st == 0
[11]	RO	pwm1_keep_st	Square wave output mode for the internal module of PWM1. 0: The number of output square waves is fixed. 1: Square waves are always output.
[10]	RO	pwm1_busy	Working status of PWM1. 0: Wave output is complete and PWM1 is idle. 1: PWM1 is outputting square waves.
[9:0]	RO	pwm1_period_st	Number of output square waves for the internal module of PWM1.

PWM2_CFG0

PWM2_CFG0 is PWM2 configuration 0 register.

Offset Address	Register Name	Total Reset Value
0x0040	PWM2_CFG0	0x0000_018F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								pwm2_period																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.
[25:0]	RW	pwm2_period	Number of cycles for PWM2. This field cannot be set to 1 or 0. Otherwise, the output level is high.

PWM2_CFG1

PWM2_CFG1 is PWM2 configuration 1 register.

Offset Address	Register Name	Total Reset Value
0x0044	PWM2_CFG1	0x0000_00C7

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								pwm2_duty																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.
[25:0]	RW	pwm2_duty	Number of level beats for PWM2. If the field value is equal to the number of cycles, the output level is always high.

PWM2_CFG2

PWM2_CFG2 is PWM2 configuration 2 register.

Offset Address	Register Name	Total Reset Value
0x0048	PWM2_CFG2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						pwm2_num									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	-	reserved	Reserved.
[9:0]	RW	pwm2_num	Number of square waves output by PWM2.

PWM2_CTRL

PWM2_CTRL is PWM2 control register.

Offset Address	Register Name	Total Reset Value
0x004C	PWM2_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													pwm2_keep	pwm2_inv	pwm2_enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	-	reserved	Reserved.
[2]	RW	pwm2_keep	PWM output mode. 0: The number of square waves output by PWM2 is fixed. 1: PWM2 always outputs square waves.
[1]	RW	pwm2_inv	PWM output control. 0: PWM2 outputs square waves in normal mode. 1: PWM2 outputs square waves in inverted mode.
[0]	RW	pwm2_enable	PWM2 enable. 0: disabled 1: enabled

PWM2_STATE0

PWM2_STATE0 is PWM2 status 0 register.

Offset Address	Register Name	Total Reset Value
0x0050	PWM2_STATE0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								pwm2_period_st																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.
[25:0]	RO	pwm2_period_st	Number of count cycles for the internal module of PWM2.

PWM2_STATE1

PWM2_STATE1 is PWM2 status 1 register.

Offset Address	Register Name	Total Reset Value
0x0054	PWM2_STATE1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								pwm2_duty_st																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved.
[25:0]	RO	pwm2_duty_st	Number of high level beats for the internal module of PWM2.

PWM2_STATE2

PWM2_STATE2 is PWM2 status 2 register.

Offset Address	Register Name	Total Reset Value
0x0058	PWM2_STATE2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												pwm2_cnt_st								pwm2_keep_st	pwm2_busy	pwm2_num_st									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	-	reserved	Reserved.
[21:12]	RO	pwm2_cnt_st	Number of remaining square waves output by PWM2. This field is valid only when the following conditions are met: pwm2_busy == 1, pwm2_keep_st == 0
[11]	RO	pwm2_keep_st	Square wave output mode for the internal module of PWM2. 0: The number of output square waves is fixed. 1: Square waves are always output.
[10]	RO	pwm2_busy	Working status of PWM2. 0: Wave output is complete and PWM2 is idle. 1: PWM2 is outputting square waves.
[9:0]	RO	pwm2_num_st	Number of output square waves for the internal module of PWM2.

Contents

Tables

14 Differences Between the Hi3518A and the Hi3518C

Table 14-1 describes the differences between the Hi3518A and the Hi3518C.

Table 14-1 Differences between the Hi3518A and the Hi3518C

Item	Hi3518A	Hi3518C
Reset	Internal or external reset, which can be configured	Internal reset
WDG[a]	Supported	Not supported
Double-data rate (DDR) capacity	2 Gbits	1 Gbit
Efficient energy Ethernet (EEE) function	Supported	Not supported
Composite video broadcast signal (CVBS) output	Supported	Not supported
NAND flash	Supported	Not supported
Infrared (IR)	Supported	Not supported
Synchronous serial port (SSP)	Two ports	Not supported
Secure digital (SD) card write protection	Supported	Not supported
Universal serial bus (USB) over-current protection	Supported	Not supported
Camera flash and shutter control	Supported	Not supported

Item	Hi3518A	Hi3518C
Universal asynchronous receiver transmitter (UART) interface	Three interfaces, including two 2-wire interfaces and one 4-wire interface	Two interfaces, including one 2-wire interface and one 3-wire interface
Audio interface	Stereo	Mono

a: For details, see the *Hardware Design Differences Between the Hi3518A and the Hi3518C.*