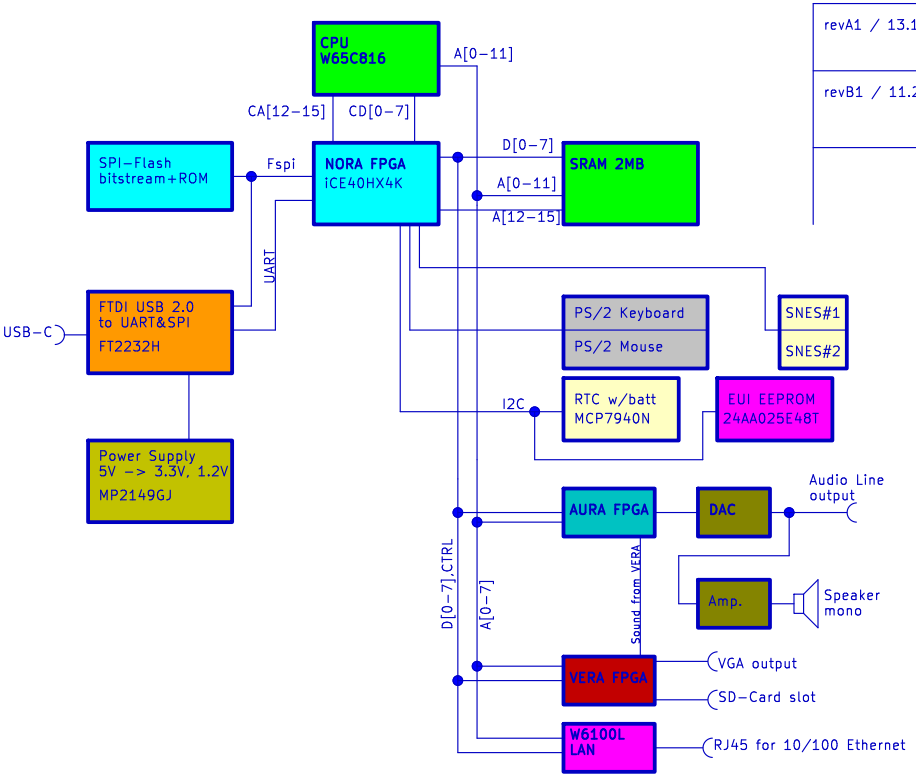
X65 SBC rev.B1

Single-Board-Computer WITH THE 65816 (6502) CPU, 2MB RAM, VGA, Sound, 2x PS/2, 2x SNES Joypad, Ethernet LAN

Block Diagram:



Revision History:

revA1 / 13.1.2024	Initial design based on MOBO+VABO rev001. PCB 180x100mm, 4-L.
revB1 / 11.2.2024	Change green LED resistors to 2k7 (depends on LED). Remove D504 (USB ESD). Add 5V and +3.3V pins to J601 internal mem.bus connector. Changed AURA FPGA footprint to the smaller EP pad.

Schematic sheets:

CPU+SRAM
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NORA FPGA
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Soubor: 03-nora_fpga.kicad_sch

LEDs, RTC, SNES
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USB-Terminal
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PS2 Kbd+Mouse, UEXT
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FID101 Fiducial
FID102 Fiducial
FID103 Fiducial
FID104 Fiducial

H101 MountingHole
H102 MountingHole
H103 MountingHole
H104 MountingHole
GND

Internet links:
www.x65.eu
www.jsykora.info
github.com/jsyk/x65

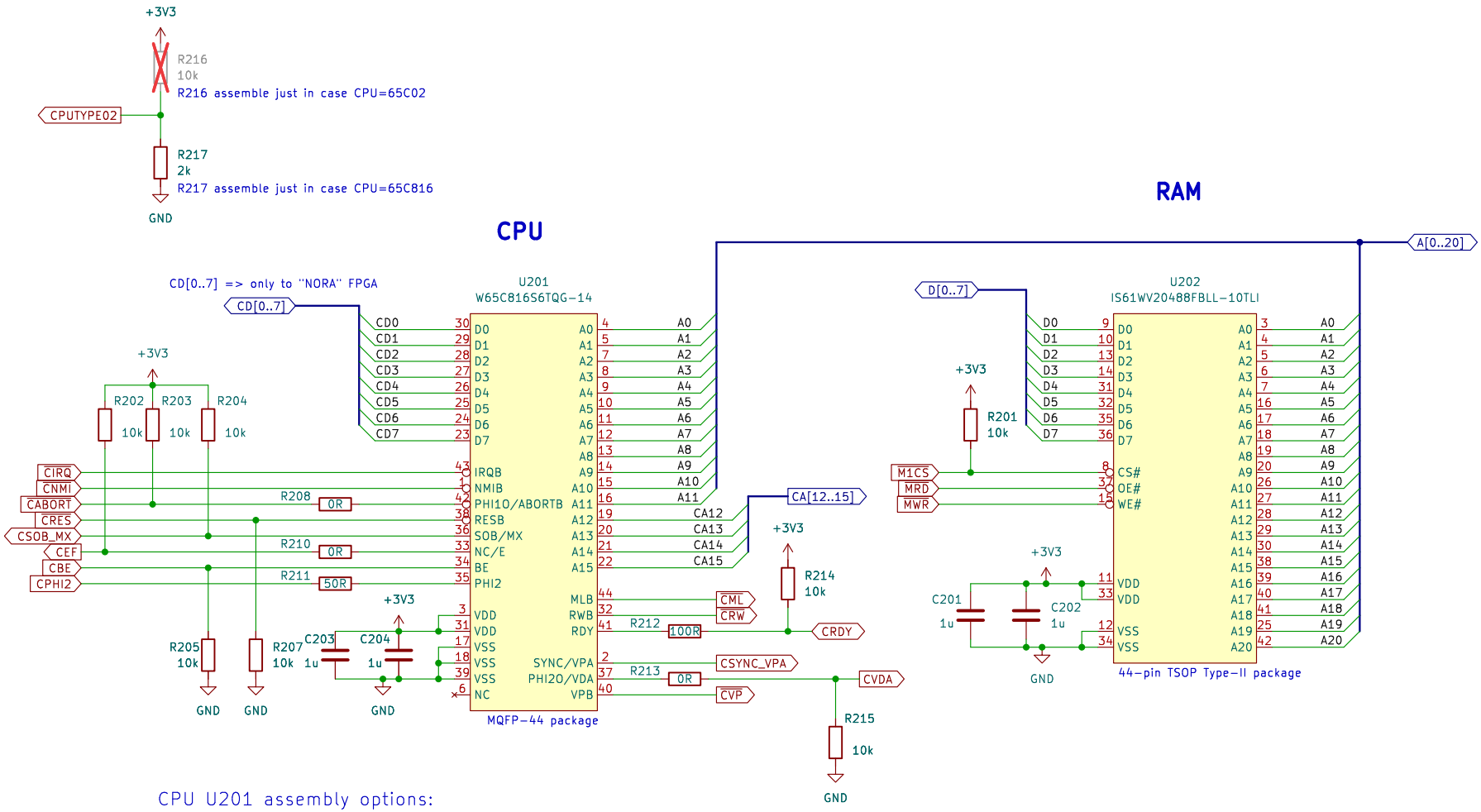
X65 IS
OPEN SOURCE:
+ CIRCUIT SCHEMATIC
+ PCB LAYOUT
+ VERILOG FPGA DESIGN
+ TOOLS USED
+ ORIGINAL SOFTWARE

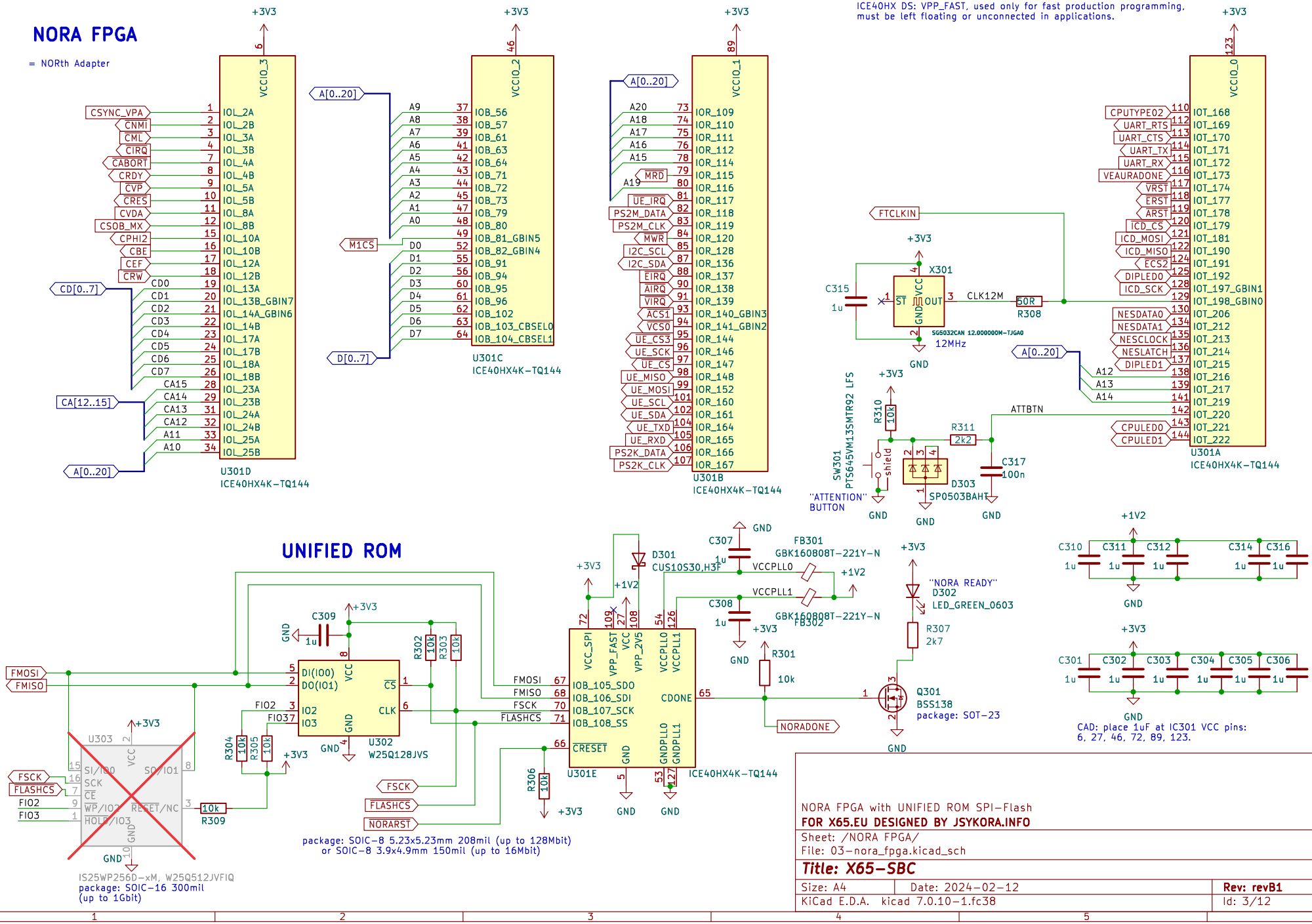
X65 Single Board Computer
FOR X65.EU DESIGNED BY JSYKORA.INFO

Sheet: /
File: x65-sbc-revB1.kicad_sch

Title: X65-SBC

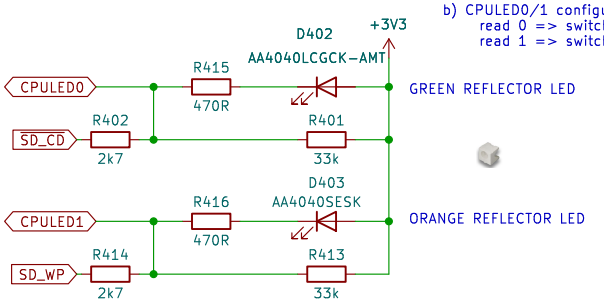
Size: A4	Date: 2024-02-12	**Rev: revB1**
KiCad E.D.A. kicad 7.0.10-1.fc38		Id: 1/12

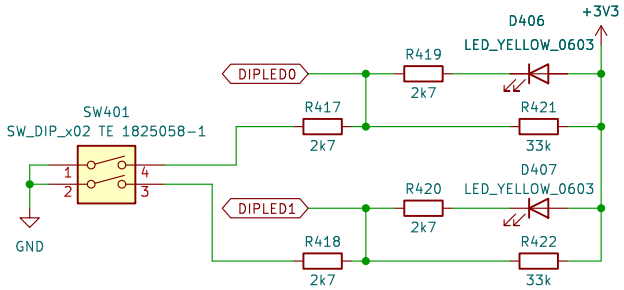

+3V3
R216
10k
R216 assemble just in case CPU=65C02
CPUTYPE02
R217
2k
R217 assemble just in case CPU=65C816
GND
CPU
RAM
CD[0..7] => only to "NORA" FPGA
CD[0..7]
U201
W65C816S6TQG-14
MQFP-44 package
A[0..20]
D[0..7]
U202
IS61WV20488FBLL-10TLI
44-pin TSOP Type-II package
R202
R203
R204
10k
R201
R205
R207
C203
C204
1u
C201
C202
R208
0R
R210
0R
R211
50R
R212
100R
R213
0R
R214
R215
CIRQ
CNMI
CABORT
CRES
CSOB_MX
CEF
CBE
CPHI2
CA[12..15]
CML
CRW
CRDY
CSYNC_VPA
CVDA
CVP
M1CS
MRD
MWR
CPU U201 assembly options:
a) W65C02S6TQG-14 => 8-bit CPU
=> do not populate R208, R210, R213, R217.
=> do populate R216 (so that CPUTYPE02=Hi)
DEFAULT
b) W65C816S6TQG-14 => 16-bit CPU
=> as shown in the schematic.
65816 CPU, 2MB SRAM
FOR X65.EU DESIGNED BY JSYKORA.INFO
Sheet: /CPU+SRAM/
File: 02-cpu_sram.kicad_sch
Title: X65-SBC
Size: A4
Date: 2024-02-12
Rev: revB1
KiCad E.D.A. kicad 7.0.10-1.fc38
Id: 2/12

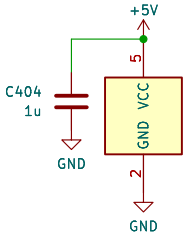

NORA FPGA
= NORth Adapter
ICE40HX DS: VPP_FAST, used only for fast production programming, must be left floating or unconnected in applications.
U301D ICE40HX4K-TQ144
U301C ICE40HX4K-TQ144
U301B ICE40HX4K-TQ144
U301A ICE40HX4K-TQ144
UNIFIED ROM
U302 W25Q128JVS
U303
IS25WP256D-xM, W25Q512JVFIQ
package: SOIC-16 300mil
(up to 1Gbit)
package: SOIC-8 5.23x5.23mm 208mil (up to 128Mbit)
or SOIC-8 3.9x4.9mm 150mil (up to 16Mbit)
U301E ICE40HX4K-TQ144
"ATTENTION" BUTTON
"NORA READY"
D302 LED_GREEN_0603
Q301 BSS138 package: SOT-23
CAD: place 1uF at IC301 VCC pins: 6, 27, 46, 72, 89, 123.
NORA FPGA with UNIFIED ROM SPI-Flash
FOR X65.EU DESIGNED BY JSYKORA.INFO
Sheet: /NORA FPGA/
File: 03-nora_fpga.kicad_sch
Title: X65-SBC
Size: A4
Date: 2024-02-12
Rev: revB1
KiCad E.D.A. kicad 7.0.10-1.fc38
Id: 3/12

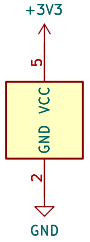
User LEDs

Dual purpose CPULED0/1 signals:
a) CPULED0/1 configured as OUTPUT DRIVING:
set 0 => LED ON
set 1 => LED OFF
b) CPULED0/1 configured as INPUT:
read 0 => switch SD_CD or SD_WP closed.
read 1 => switch SD_CD or SD_WP open.

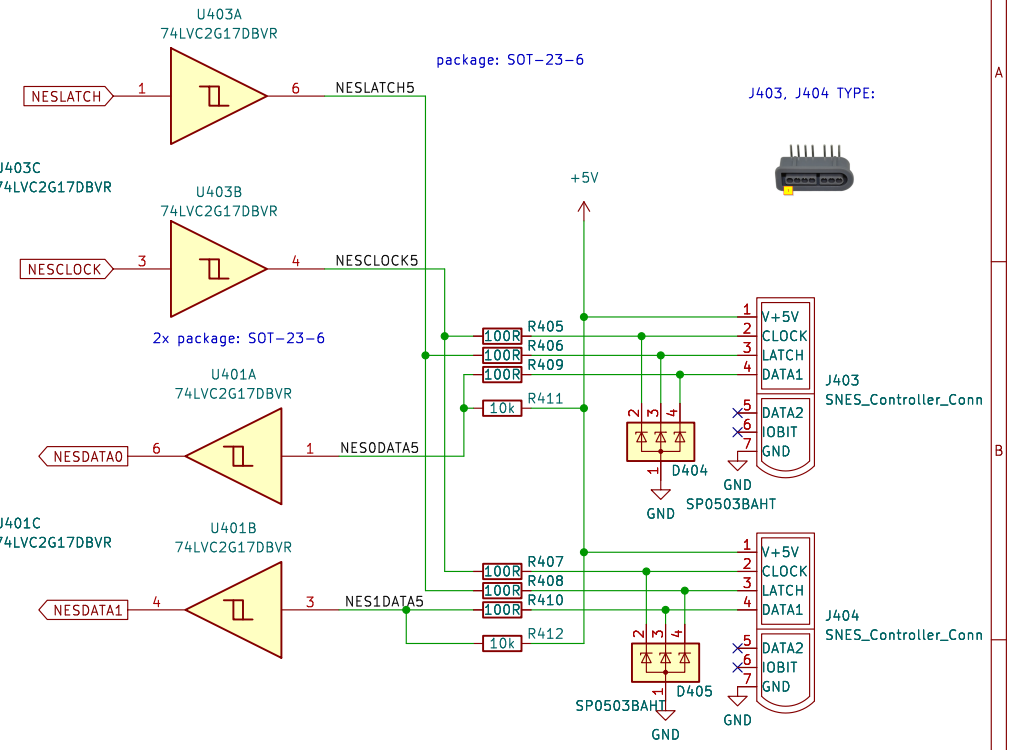




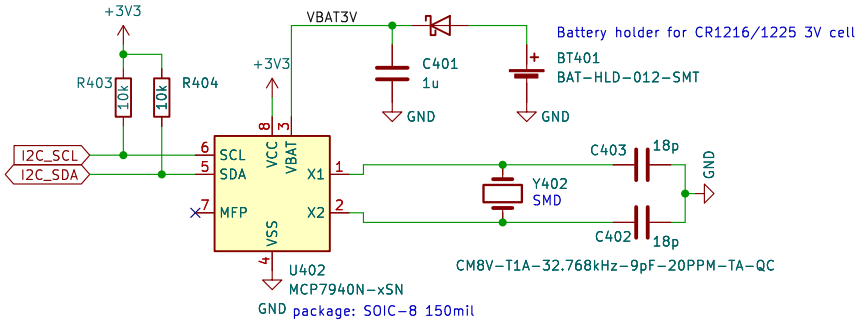




2x SNES JOYPAD CONTROLLER PORTS



RTC



MCP7940N datasheet says:
* crystal loading shall be 6-9pf; 12pf not recommended!
* CX should be 2* X_loading, so that in parallel the crystal see the expected capacitance
* layout must be according to the DS.

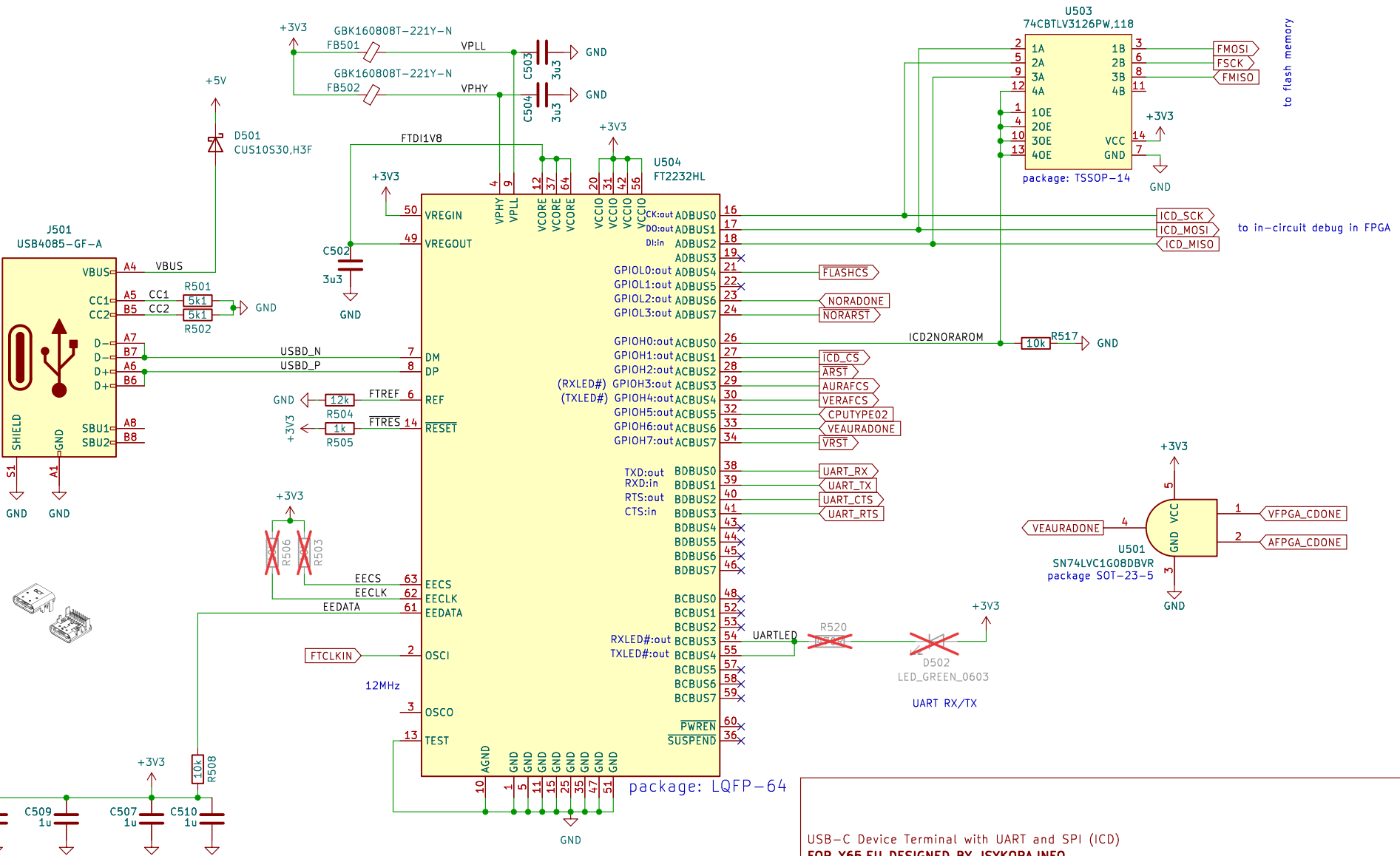
RTC/MCP7940N I2C DEVICE ADDRESS (8b=shifted) = 0b1101_111W = 0xDE, that is 7-bit addr 0x6F
PS2 CONTROLLER (IN NORA) I2C DEVICE ADDRESS (8b=shifted) = 0b1000010W = 0x84, that is 7-bit addr 0x42

User LEDs, SNES Joystick, RTC
FOR X65.EU DESIGNED BY JSYKORA.INFO
Sheet: /LEDs, RTC, SNES/
File: 04-rtc_snes.kicad_sch

Title: X65-SBC

Size: A4	Date: 2024-02-12	**Rev: revB1**
KiCad E.D.A. kicad 7.0.10-1.fc38		Id: 4/12

USB 2.0 WITH USB-C / UART TERMINAL AND ICD (In-Circuit Debugger)



USB-C Device Terminal with UART and SPI (ICD)

FOR X65.EU DESIGNED BY JSYKORA.INFO

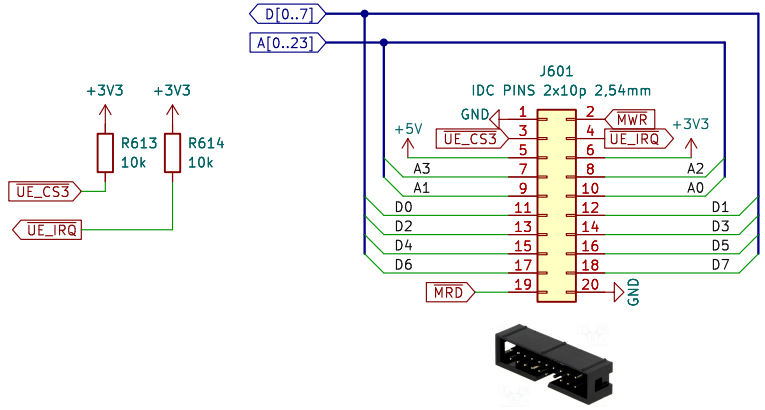
Sheet: /USB-Terminal/

File: 05-usbdev.kicad_sch

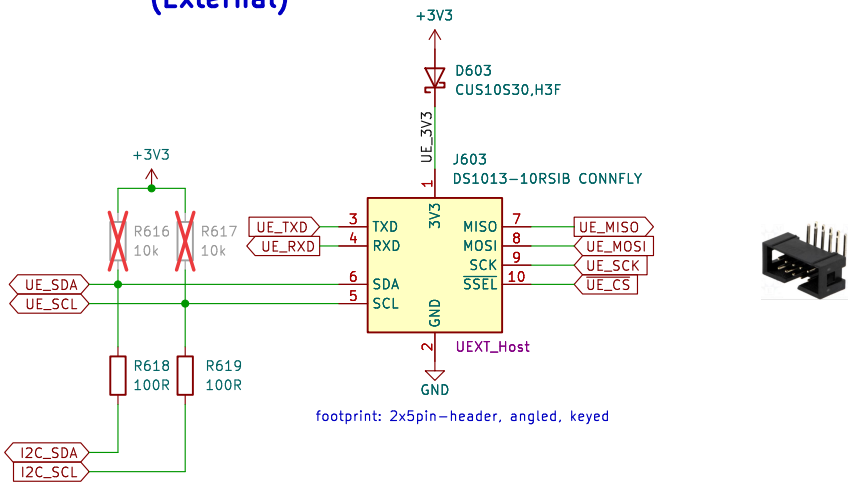
Title: X65-SBC

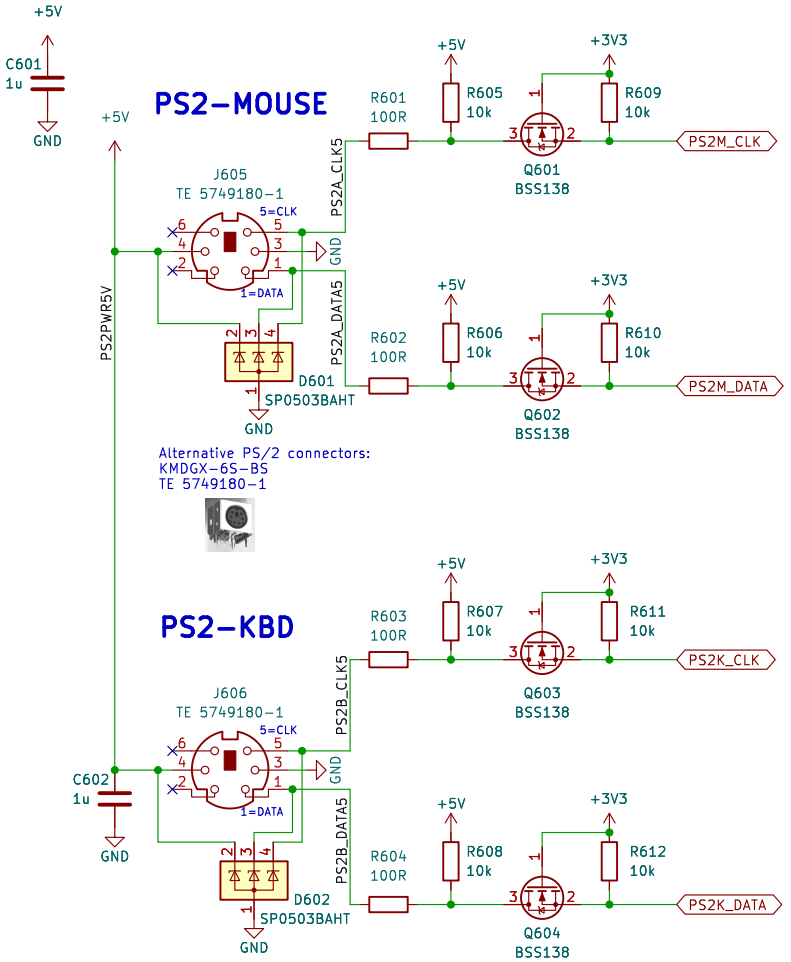
Size: A4	Date: 2024-02-12	**Rev: revB1**
KiCad E.D.A. kicad 7.0.10-1.fc38		Id: 5/12

Extension Connector (Internal)



UEXT HOST Connector (External)





Extension Connectors, PS2 KBD and Mouse ports

FOR X65.EU DESIGNED BY JSYKORA.INFO

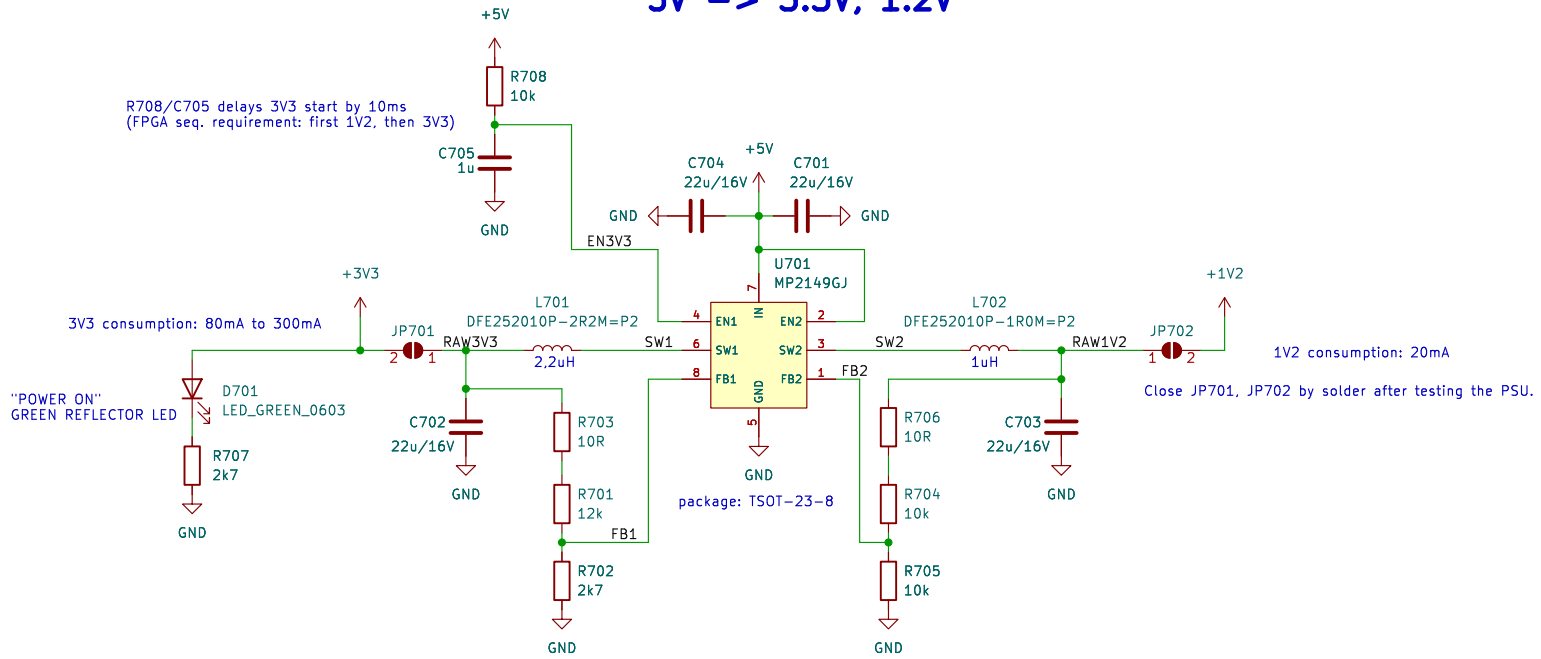
Sheet: /PS2 Kbd+Mouse, UEXT/

File: 06-ps2_uext.kicad_sch

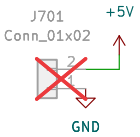
Title: X65-SBC

Size: A4	Date: 2024-02-12	**Rev: revB1**
KiCad E.D.A. kicad 7.0.10-1.fc38		Id: 6/12

POWER SUPPLY
5V -> 3.3V, 1.2V



Alternative power input connector



GND testpoints

Power supplies 3.3V and 1.2V

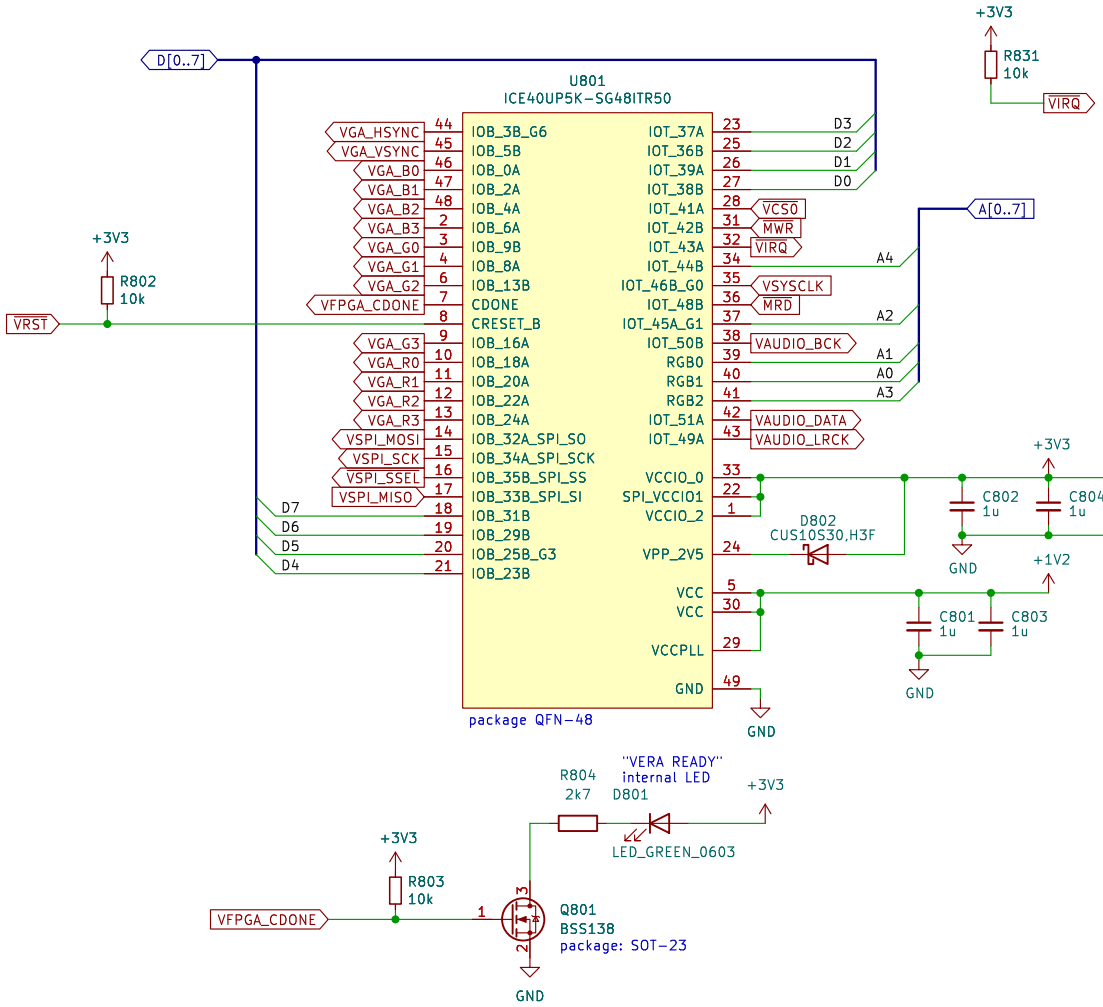
FOR X65.EU DESIGNED BY JSYKORA.INFO

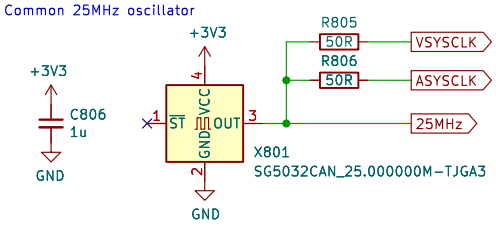
Sheet: /Power Supply/
File: 07-pwrsup.kicad_sch

Title: X65-SBC

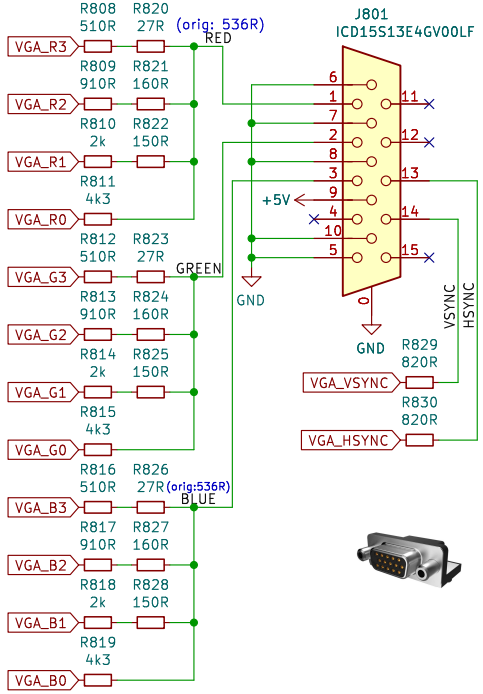
Size: A4	Date: 2024-02-12	**Rev: revB1**
KiCad E.D.A. kicad 7.0.10-1.fc38		Id: 7/12

"VERA" FPGA – Video Embedded Retro Adapter





VGA interface



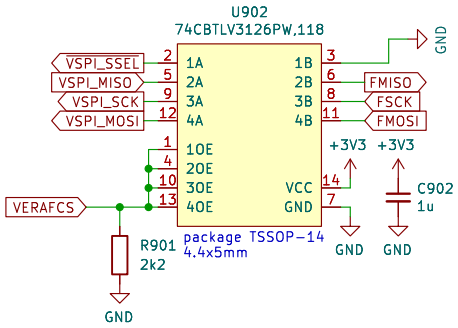
This schematic contains portions of work done by Frank van den Hoe
for the project VERA: https://github.com/fvdhoef/vera-module

VERA FPGA – VGA Adapter
FOR X65.EU DESIGNED BY JSYKORA.INFO
Sheet: /VERA FPGA/
File: 08-vera_fpga.kicad_sch

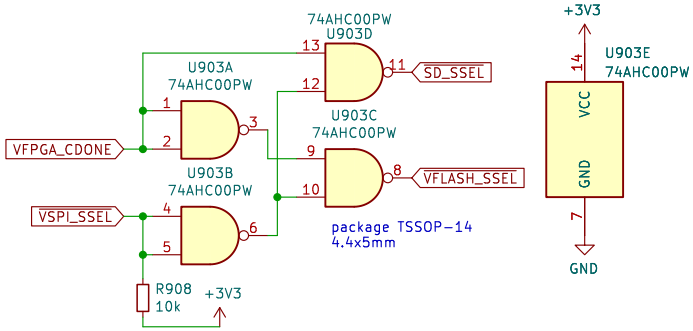
Title: X65-SBC

Size: A4	Date: 2024-02-12	**Rev: revB1**
KiCad E.D.A. kicad 7.0.10-1.fc38		Id: 8/12

FTDI/ICD access multiplexer to VERA SPI flash memory

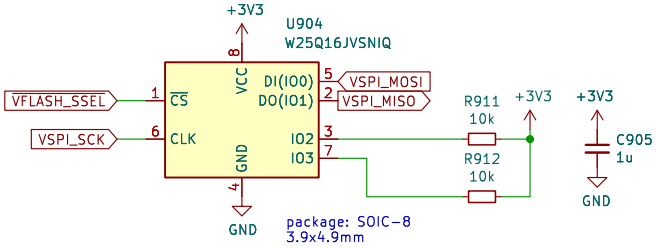


VERA SPI pins multiplexing

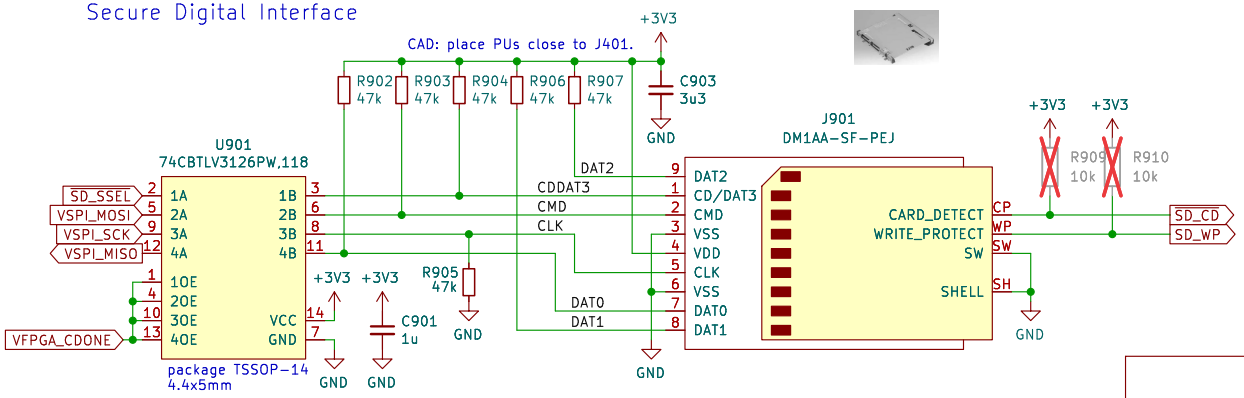


Inputs		Outputs		
VFPGA_CDONE	VSPI_SSEL	SD_SSEL	VFLASH_SSEL	Description
0	0	1	0	FPGA configuring from the SPI-Flash, or FTDI/ICD accessing.
0	1	1	1	FPGA empty/in-reset
1	0	0	1	FPGA loaded; User Design r/w to SDC
1	1	1	1	FPGA loaded; idle

SPI flash for VERA Bitstream



Secure Digital Interface



This schematic contains portions of work done by Frank van den Hoe for the project VERA: https://github.com/fvdhoef/vera-module

SD-Card slot, SPI-Flash for VERA

FOR X65.EU DESIGNED BY JSYKORA.INFO

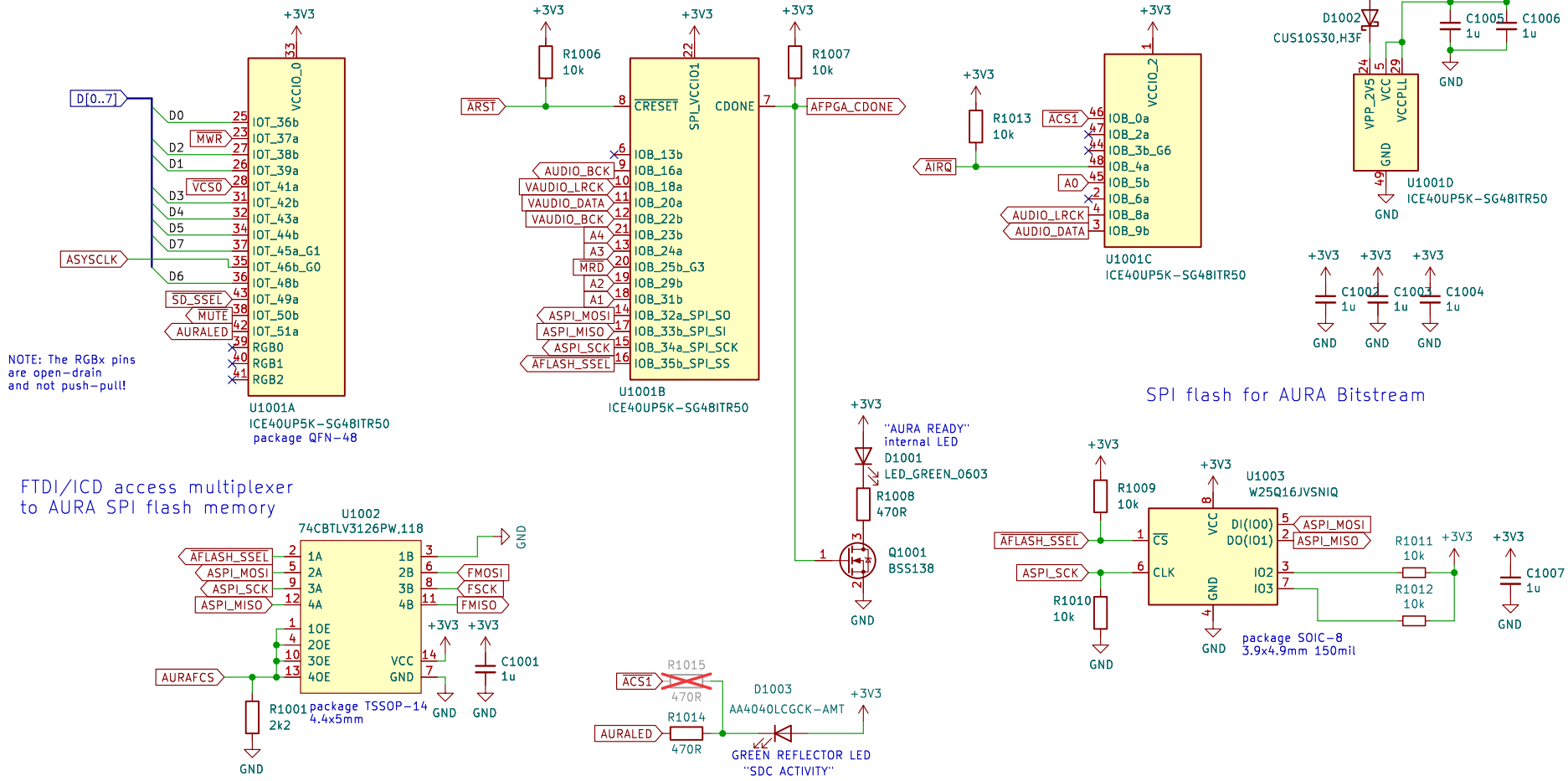
Sheet: /SD-Card/
File: 09-sdcard.kicad_sch

Title: X65-SBC

Size: A4	Date: 2024-02-12	**Rev: revB1**
KiCad E.D.A. kicad 7.0.10-1.fc38		Id: 9/12

"AURA" FPGA – Audio Retro Adapter

AURA implements the YM2151 FM-Synthesis (the chip is long out of production).
Design is based on IKAOPM core.



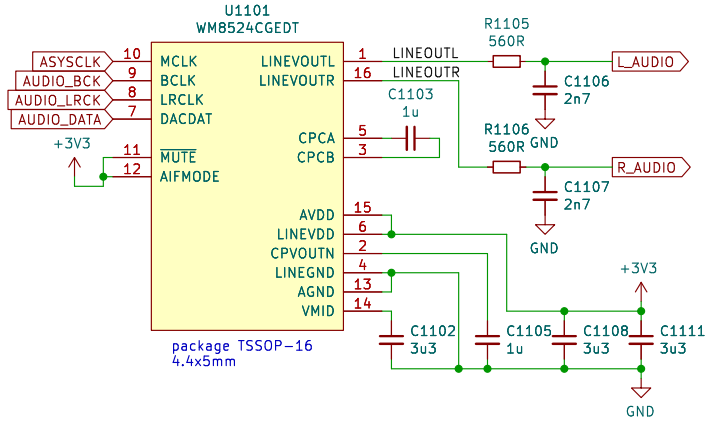
AURA FPGA – OPM Sound Adapter
FOR X65.EU DESIGNED BY JSYKORA.INFO

Sheet: /AURA FPGA/
File: 10-aura_fpga.kicad_sch

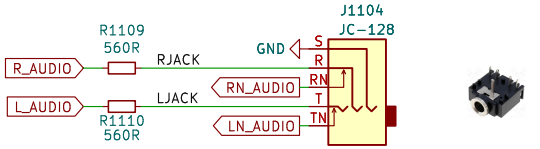
Title: X65-SBC

Size: A4	Date: 2024-02-12	**Rev: revB1**
KiCad E.D.A. kicad 7.0.10-1.fc38		Id: 10/12

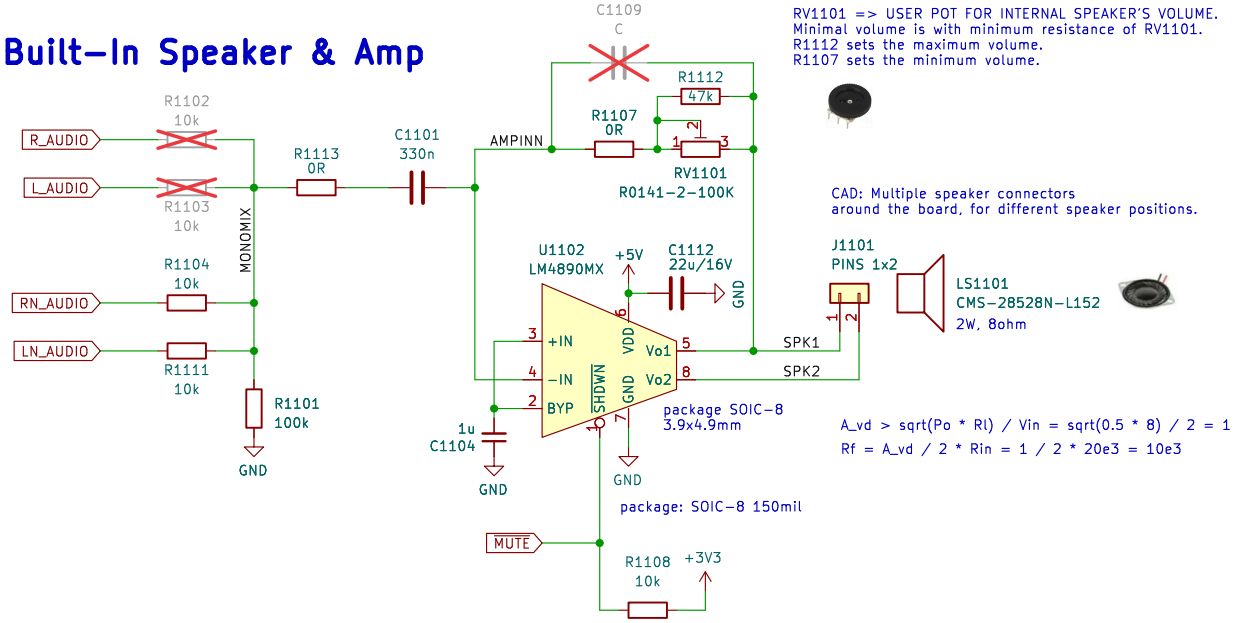
Audio DAC (PCM/PSG in VERA, FM in AURA)



3.5mm jack – AUDIO LINE output



Built-In Speaker & Amp



RV1101 => USER POT FOR INTERNAL SPEAKER'S VOLUME.
Minimal volume is with minimum resistance of RV1101.
R1112 sets the maximum volume.
R1107 sets the minimum volume.

CAD: Multiple speaker connectors
around the board, for different speaker positions.

A_vd > sqrt(Po * Rl) / Vin = sqrt(0.5 * 8) / 2 = 1
Rf = A_vd / 2 * Rin = 1 / 2 * 20e3 = 10e3

Sound DAC and output port
FOR X65.EU DESIGNED BY JSYKORA.INFO

Sheet: /Sound Output/
File: 11-sndout.kicad_sch

Title: X65-SBC

Size: A4	Date: 2024-02-12	**Rev: revB1**
KiCad E.D.A. kicad 7.0.10-1.fc38		Id: 11/12

10/100Mbit Ethernet Interface

CAD: resistor termination on MDI should be placed close to U801.

XSCI requires 25MHz @ 1.2V levels, rise/fall time <8ns

Pin RSET requires 12.3k resistor to GND.

EEPROM with Factory Pre-Programmed Unique EUI-48 = MAC address for Wiznet

EEPROM 24AA025E48 I2C DEVICE ADDRESS (8b=shifted) = 0b1010_000W = 0xA0, that is 7-bit address = 0x28

Ethernet LAN Adapter with WIZNET
FOR X65.EU DESIGNED BY JSYKORA.INFO

Sheet: /Ethernet/
File: 12-ethernet.kicad_sch

Title: X65-SBC

Size: A4	Date: 2024-02-12	**Rev: revB1**
KiCad E.D.A. kicad 7.0.10-1.fc38		Id: 12/12