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SL800

STEbus SERIAL I/O CARD

TECHNICAL REFERENCE MANUAL

VERSION 4.2

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1 INTRODUCTION

The SL800 is one of a range of powerful input/output cards manufactured by DSP Design. The SL800 provides eight serial communications channels on the one card, an approach that allows efficient and economical solutions to I/O intensive STEbus system problems.

The eight identical serial ports offer RS-232 and RS-423 compatibility. A full set of handshaking lines is provided, and both synchronous and asynchronous operation is possible.

The key to the functionality of the SL800 is the powerful I/O chips which drive the interface lines. Zilog SCC (8530) chips are used, offering a wealth of features.

Partially populated versions of the SL800 are available on special order. The SL200, SL400 and SL600 are two channel, four channel and six channel versions, respectively.

Related I/O cards from DSP Design are the SP800, an 80 line parallel I/O card, the SL801, an eight channel RS-422/RS-485 serial I/O card, the SPL440, which provides 4 serial channels and 40 parallel lines and a dual IEEE-488 controller card, the SP488.

Also available is the SD800 board - a chassis mounting PCB which accepts the two 50 way cables from the SL800 and routes the signals to eight 25-way D-Type connectors.

2 HARDWARE OVERVIEW

* Eight serial ports controlled by four Zilog 8530 Serial Communication Controller (SCC) chips.

* Occupies 16 I/O locations, jumper selectable.

* Supports vectored and non-vectored interrupts using the STEbus Attention Request (ATNRQ*) lines.

* Supports DMA data transfer using the ATNRQ* lines for high speed transfer of serial data.

* The four SCC chips support a wide range of synchronous and asynchronous communication protocols, as well as digital phase locked loop clock recovery, NRZI, FM and Manchester data encoding and powerful baud rate generation features.

* The buffering on the four SCC chips offers two RS-423 (RS-232 compatible) channels with flexible handshake and synchronous clock options.

* I/O signals are taken from the SL800 card by a high density 100 position connector. Flat ribbon cable is used and pin assignments have been chosen for ease of interface.

* Fully conforms to IEEE 1000 (STEbus) specification.

3 BUS INTERFACE

The SL800 is mapped into the I/O space of the STEbus. It makes use of the Attention Request lines to support both vectored and non-vectored interrupts and DMA transfers.

3.1 ADDRESSING THE SL800

The card occupies 16 I/O locations. Four I/O chips each occupy four locations. The base address can be set by jumpers at jumper area E5 to any 16 byte block within the 4k STEbus I/O space. Appendix B contains instructions for selecting the address.

Within the 16 byte block chosen the registers in the SCC chips are addressed as follows:

Locations 0-3H : SCC No.1

0 Control and Status Registers for Channel B
1 Data Registers for Channel B
2 Control and Status Registers for Channel A
3 Data Registers for Channel A

Locations 4-7H : SCC No.2

4 Control and Status Registers for Channel B
5 Data Registers for Channel B
6 Control and Status Registers for Channel A
7 Data Registers for Channel A

Locations 8-BH : SCC No.3

8 Control and Status Registers for Channel B
9 Data Registers for Channel B
A Control and Status Registers for Channel A
B Data Registers for Channel A

Locations C-FH : SCC No.4

C Control and Status Registers for Channel B
D Data Registers for Channel B
E Control and Status Registers for Channel A
F Data Registers for Channel A

Programming of the SCC chip is described in the SCC Technical Manual (see Appendix A).

There are no other registers on the SL800 other than the registers within the four I/O chips. The registers are accessed by performing STEbus I/O cycles, using for instance Z80 IN and OUT instructions.

3.2 ACCESS TIMES

The STEbus data transfer acknowledge signal, DATACK*, is asserted some time after the access begins. DATACK* is generated by a counter circuit which counts periods of the 16MHz SYSCLK signal. The time is dependent on the frequency of the PCLK signal used in the board and the type of cycle in progress. It is longer for vector fetch cycles (see below) than for read and write cycles, and it is shorter for an 8MHz PCLK than for a 4MHz PCLK. Since the access from the STEbus will typically occur asynchronously with respect to SYSCLK, there will be an uncertainty in the SL800 access time. The following table lists the access times, defined as the time from DATSTB* and ADRSTB* becoming true and DATACK* becoming true.

SL800 ACCESS TIMES

CYCLE TYPE	4MHz PCLK	8MHz PCLK
Read Cycle	570-860 ns	320-490 ns
Write Cycle	570-860 ns	320-490 ns
Vector Fetch Cycle	1570-1860 ns	820-990 ns

Code run at full speed may violate the valid access recovery period of a 4MHz SCC. When accessing SCCs with date codes prior to approximately 8640 (week 40 1986), non-access instructions totalling 1.7us must be executed between successive accesses to the same SCC chip. When accessing SCCs with date codes from approximately 8640 onwards non-access instructions totalling 1us should be executed between successive accesses to the same SCC chip.

Users with 8MHz SCCs will be supplied with additional data specifying the valid access recovery period of the 8MHz SCC.

3.3 PCLK FREQUENCY

The SCC chips come in three speed variants: 4MHz, 6MHz and 8MHz. The 4MHz and 8MHz chips can be used on the SL800. The 8MHz parts give faster access times from the STEbus but more importantly can communicate at higher speeds with the outside world. This is of particular interest for serial communications - the maximum serial data rate for the SCC is 1Mbit/sec for the 4MHz part and 2Mbit/sec for the 8MHz part.

If the 4MHz chips are installed the frequency of the PCLK clock signal to the chips should be 4MHz. If 8MHz chips are installed the frequency of the PCLK signal can be 8MHz or 4MHz. The frequency of PCLK is selected at jumper area E1.

Appendix B contains instructions for setting up this jumper area.

3.4 INTERRUPTS

The SL800 can support both vectored and non-vectored interrupts. Any of the eight ATNRQ* signals can be used as the interrupt request signal from the SL800.

The ATNRQ* signal used by the SL800 is selected with the jumper area E3. Appendix B describes how this area should be set up.

The STEbus specification describes "explicit" and "implicit" responses to interrupt requests. An implicit response is the non-vectored interrupt response. In this mode the processor, having detected an interrupt request from the SL800 must poll the SCC chips to determine the cause of the interrupt and must reset the interrupt by the appropriate I/O accesses.

The explicit response is defined by the STEbus specification (section 6.3.2) as follows:

> "An explicit response to an attention request is where a Master uses the Vector-Fetch data transfer sequence to discover which device within a system is requesting attention, and to simultaneously acknowledge to the board requesting attention that its request has been granted and that the requesting device may release the attention request line."

The SCC chips support this vector fetch cycle. Typically the sequence of events is as follows. An event such as the arrival of a serial character causes one of the chips to assert its INT- pin which in turn asserts an ATNRQ* signal on the STEbus. The processor (such as the 64180 CPU on the SX180 card from DSP Design) responds by performing an interrupt acknowledge cycle which in turn causes an STEbus vector fetch cycle to begin. Hardware on the SL800 recognises the vector fetch cycle and asserts the INTACK- signal to the SCC chips. One of the chips responds by placing an interrupt vector on the STEbus data bus. The processor reads this vector and uses it as a pointer, via a vector table, to an appropriate interrupt service routine.

The SCC chips can be programmed to return either a fixed vector or a vector which differs depending on the source of the interrupt. This further aids the system designer since it reduces or eliminates the code required to discover the nature of the interrupt and hence speeds interrupt latency time.

It is possible that more than one interrupt event occurs concurrently. In this case a "daisy chain" mechanism ensures that only the interrupt with the highest priority generates the vector. Interrupting events are automatically prioritised within each SCC chip. When a potential conflict exists between chips this is resolved by the hardware daisy chain; only the chip closest to the start of the chain will provide the vector. The interrupt mechanism is fully described in references 1, 2 and 3 in Appendix A.

Within the hardware daisy chain the priority is as follows:

SCC No.1 (highest priority)
SCC No.2
SCC No.3
SCC No.4 (lowest priority)

The interrupt daisy chain does not exist between STEbus cards. This means that within a system only one slave card using vectored interrupts can assert any given ATNRQ* line.

Jumper area E4 must be set to enable or disable vectored interrupts. Appendix B describes the setting up of this jumper area.

3.5 DMA TRANSFERS

The ATNRQ* lines can also be used as DMA request signals for high speed data transfer to and from the serial ports.

There are four SCC chips, each with two channels. Each channel has a receive and a transmit capability. This means that there is a total of 16 DMA "streams" possible. Only one ATNRQ* signal can be used by the SL800 as a DMA request line. This means that at any time only one DMA stream can be active out of the 16 possible streams.

The W/REQA- and W/REQB- pins on all of the SCC chips are connected together and are used to drive an ATNRQ* pin. These pins can be programmed to act as DMA request pins for the transmit or receive sections of the SCC. The SCC Technical Manual section 3.5 describes the DMA mode operation.

Since all eight pins are connected together, the pins not being used as the DMA request pin must be programmed as open drain outputs (ie left as WAIT- mode outputs). Only the pin which is to be used as the DMA request pin should be programmed for the REQUEST- mode.

Jumper area E2 is used to select the ATNRQ* line used as a DMA request signal. Appendix B describes setting up this jumper area.

4 SERIAL PORTS

Eight serial ports are provided on the SL800. These ports are implemented using four Zilog SCC chips. The ports have RS-423 buffers. RS-423 is an enhanced version of RS-232, and compatible with RS-232.

The partially populated versions of the SL800 (the SL200, SL400 and SL600) are identical in all respects to the SL800 except that they have fewer serial channels. The SL200 has only SCC No.1, the SL400 has SCC No.1 and SCC No.2, and the SL600 has SCC No.1, No.2 and No.3.

4.1 FACILITIES OF THE SCC CHIPS

This section should be treated only as a summary of the features offered by the SCCs. Full details are given in the SCC Technical Manual (see Appendix A), and a summary of features and register use is given in the data sheet in Appendix E.

The SCC chips provide support for handling the wide variety of serial communication protocols available. Bit-oriented synchronous, byte-oriented synchronous and asynchronous protocols are supported, with the usual facilities for variable data size, parity checking, stop bits and baud rates.

A number of special features are provided by the SCC. NRZ, NRZI, FM and Manchester data encoding are provided. A digital phase-locked loop is built in for clock recovery. Baud rates may be set by internally dividing the 4MHz or 8MHz PCLK signal, or the clock may externally sourced, or two pins of the SCC can be used for a crystal oscillator.

A good range of handshake signals, interrupt options and DMA modes are provided.

The W/REQ- pins of each SCC chip are all joined to the DMA request circuit which asserts an ATNRQ* pin. This feature allows high speed transfer of data between the processor and one of the SCC channels.

4.2 RS-423 SIGNALS

RS-423 is an enhanced version of the RS-232 standard. It is compatible with RS-232. References 4 and 5 in Appendix A describe the RS-423 standard.

With the exception of a clock option the eight channels are

identical. Each channel has the following RS-423 level signals available on the 100 way connector J2:

Signal	Function	Direction	Connected to:
TxD	transmit data	output	SCC TxD pin
RTS	request to send	output	SCC RTS- pin
DTR	data terminal ready	output	SCC DTR- pin
CLKOUT	clock output	output	jumper area *
RxD	receive data	input	SCC RxD pin
CTS	clear to send	input	SCC CTS- pin
DCD	data carrier detect	input	SCC DCD- pin
CLKIN	clock input	input	jumper area *

* See Appendix B for details of the relationship between jumper areas E6-E13 and the eight serial channels.

A 75173 chip is used to buffer the input signals. Two uA9636A chips drive the outputs.

The RS-423 driver chips, the uA9636A chips, each have a resistor which controls their slew rate. Reference 5 (see Appendix A) gives a recommended rise time of 5-15uS for a 19200 baud rate. A 5uS rise time is given by a 47k resistor. For other times, see the data sheet for this chip.

4.3 CLOCK OPTIONS

The only options in the serial port circuitry are related to the clock options, for synchronous data transfer.

Jumper area E6 selects the options for channel B and jumper E7 for channel A of SCC No.1. This section refers only to SCC No.1, but the other three SCC's have identical circuitry. E6 and E7 are the jumper areas for SCC No.1. The corresponding pairs of jumper areas for SCC No.2, No.3 and No.4 are E8 and E9, E10 and E11, and E12 and E13 respectively (see Appendix B).

Both jumper areas E6 and E7 allow the interconnection of: SCC pins TRxC-, RTxC- and SYNC-, one RS-423 receiver output and one RS-423 transmitter input. E7 has provision for connecting a crystal to the RTxCA- and SYNCA- pins to form a crystal oscillator, and E6 allows the output of channel A TRxC- pin, the signal known as BAUDCLK, to be fed to channel B.

For asynchronous operation, Appendix B describes the standard way of setting up jumper areas E6 and E7. Following the standard set-up, the SCC is configured as follows:

The SYNC- pins of each channel are driven by the CLKIN buffer. This should be regarded as a third status input signal.

The inputs of the CLKOUT buffers are driven from the buffered CLKIN signals. This means CLKOUT will mimic CLKIN.

Following a hardware reset the TRxC- pin on each channel will be an input. It is recommended that the user's initialisation routine programs TRxCA- as an output, allowing it to drive the BAUDCLK signal for that SCC. If TRxCB- is left disconnected, as for the default jumper settings listed in Appendix B, it should also be programmed as an output. Care should be taken, however, that only one TRxC- pin programmed as an output is connected to each BAUDCLK signal.

Both of the RTxC- pins are connected to BAUDCLK, and are thus driven by TRxCA-.

In normal asynchronous operation, the baud rate generators internal to the SCC will divide the 4MHz PCLK signal to obtain appropriate timing references. The frequencies derived in this way will not be perfect, but will be quite sufficient for most purposes. When a more exact baud rate is required, a crystal oscillator can be formed using the RTxCA- and SYNCA- pins. In this case this oscillator can be buffered and output from the TRxCA- pin and thus fed (as the BAUDCLK signal) to the other channel of the SCC. Once again, see Appendix B for details.

Note that each SCC section has provision for its own crystal oscillator, and its own BAUDCLK signal. The oscillator and BAUDCLK signals are thus local to each SCC. If one oscillator output is to be shared amongst more than one SCC, wire links can be used. Ask your distributor for details of this.

For synchronous operation, facilities exist to derive a clock from an external source, through CLKIN, and to provide a clock to the external device, through CLKOUT. Appendix B describes these options.

APPENDIX A REFERENCES

1 STEbus Draft Proposed Standard, Draft 3.2
January 1986
Pub. IEEE Computer Society

2 Z8030/Z8530 SCC Technical Manual
January 1983
Pub. Zilog Inc.

3 Z80 Family Interrupt Structure (Application Note)
January 1980
Pub. Zilog Inc.

4 Line Circuits for IEEE-488 and EIA Industry Standards
(Application Note)
Pub. Texas Instruments.

5 Transition Line Drivers and Receivers for EIA Standards
RS-422 and RS-423 (Application Note AP-214)
Pub. National Semiconductor

APPENDIX B BOARD SET UP PROCEDURE

There are 13 jumper areas which must be set up on the SL800. This appendix describes how to configure these for the chosen mode of operation.

A section at the end of this appendix lists standard jumper positions.

To help with locating jumpers and ICs a component placement diagram is given in Appendix D. When the text refers to "up", "down", "left" and "right", the board should be oriented component side up with the STEbus connector to your left and the two transistors at the top.

When oriented like this, SCC No.1 appears at the top of the SL800 card; SCC No.2 is below it, SCC No.3 below that and SCC No.4 is at the bottom of the card.

E1 PCLK FREQUENCY SELECTION

E1 controls the frequency of the PCLK signal which is fed to the SCC chips as their timing reference. The normal frequency for PCLK is 4MHz, but for higher throughput on the serial channels PCLK can be 8MHz. If a PCLK rate of 8MHz is selected, higher performance (ie 8MHz) SCC chips must also be fitted.

For a 4MHz PCLK:	place link in position A
For a 8MHz PCLK:	place link in position B

E2 DMA REQUEST SELECTION

The ATNRQ* signals on the STEbus can be used as interrupt request or DMA request pins. The SCC chips can be programmed to generate a DMA request. If this is to be used a link must be placed on E2 between rows A and B as follows:

No DMA request required:	no link required
DMA request on ATNRQ0*:	place link in position 0
DMA request on ATNRQ1*:	place link in position 1
DMA request on ATNRQ2*:	place link in position 2
DMA request on ATNRQ3*:	place link in position 3
DMA request on ATNRQ4*:	place link in position 4
DMA request on ATNRQ5*:	place link in position 5
DMA request on ATNRQ6*:	place link in position 6
DMA request on ATNRQ7*:	place link in position 7

Section 3.5 describes the way in which the SCC chips must be programmed to use the DMA facility.

E3 INTERRUPT REQUEST SELECTION

The ATNRQ* signals on the STEbus can be used as interrupt request or DMA request pins. The SCC chips can be programmed to generate interrupt requests. The ATNRQ* pin on which the interrupt request is to appear must be selected as a binary number on the three rows of E3.

The level should be converted to three bit binary number (eg ATNRQ0* corresponds to 000, ATNRQ3* to 011, etc). The three jumpers marked 0, 1 and 2 (0 is the LSB, 2 is the MSB) should be placed accordingly in the 0 or 1 position. The left-most position selects a 0, the right-most position selects a 1. For example, for ATNRQ0* all three should be to the left, and for ATNRQ3* the jumpers marked 0 and 1 should be to the right and the one marked 2 should be to the left.

E4 VECTOR INTERRUPT ENABLE

Vector fetch cycles on the STEbus allow for high speed interrupt servicing. The SL800 can be configured to respond to vector fetch cycles at jumper area E4.

Vector fetches required: place link in position A
Vector fetches not required: place link in position B

E5 I/O ADDRESS SELECTION

The SL800 occupies a 16 byte block of the STEbus I/O space. The base address of this block can be aligned on any 16-byte boundary within the 4k byte I/O space. Jumper area E5 allows this address to be set up.

To set up the address, convert the eight most significant bits of the 12 bit address to a binary number, eg 1F0H converts to 00011111 and C40H converts to 11000100. Then move the eight jumpers of E5 to the appropriate 0 or 1 position. Note that E5 is laid out in a slightly confusing manner - the pin for the least significant bit, corresponding to address bit A4, is left-most and the pin for bit A11 is right-most. For the C40H example above, the E5 jumpers are, from left to right, down, down, up, down, down, down, up, up.

The PCB is clearly marked A4 and A11, and 0 and 1 to assist with this placement.

E6-E13 CLOCK SELECTION

Each SCC has two jumper areas for clock selection. The following table summarises the functions of these jumpers:

E6	Clock Selection for SCC No.1 Channel B
E7	Clock Selection for SCC No.1 Channel A
E8	Clock Selection for SCC No.2 Channel B
E9	Clock Selection for SCC No.2 Channel A
E10	Clock Selection for SCC No.3 Channel B
E11	Clock Selection for SCC No.3 Channel A
E12	Clock Selection for SCC No.4 Channel B
E13	Clock Selection for SCC No.4 Channel A

E6/E8/E10/E12 CHANNEL B CLOCK SELECTION

These identical jumper areas select the clock options for the B channels on each of the four SCCs (see the table above). The required positions should be chosen with reference to the functions of the SCC RTxC- and TRxC- pins (see the SCC Technical Manual) and the clock signals (if any) on the serial communication channels.

The following options are possible:

Buffered signal CLKIN drives RTxCB- pin: link A1 to A2

Buffered signal CLKIN drives TRxCB- pin: link A2 to A3

Buffered signal CLKIN drives SYNCB- pin (status input): link A2 to B2

Buffered signal CLKIN drives SYNCB- pin and CLKOUT buffer: link A2 to B2, and A4 to B4

BAUDCLK signal (TRxCA- pin) drives RTxCB- pin: link A1 to B1

BAUDCLK signal (TRxCA- pin) drives TRxCB- pin: link A3 to B3

TRxCB- pin drives CLKOUT buffer: link A3 to A4

SYNCB- pin drives CLKOUT buffer: link A4 to B4. B2 must be disconnected

Whatever options are selected, it is advisable to ensure that the SCC input pins (RTxCB- and SYNCB-, normally) are driven by an active signal, rather than allowed to float. If the TRxCB- pin is left disconnected it must be programmed explicitly as an output (see section 4.3).

E7/E9/E11/E13 CHANNEL A CLOCK SELECTION

These identical jumper areas select the clock options for the A channels on each of the four SCCs (see the table above).

The required positions should be chosen with reference to the functions of the SCC RTxC- and TRxC- pins (see the SCC Technical Manual) and the clock signals (if any) on the serial communication channels.

The following options are possible:

Buffered signal CLKIN drives RTxCA- pin:
link A1 to A2

Buffered signal CLKIN drives TRxCA- pin:
link A2 to A3

Buffered signal CLKIN drives SYNCA- pin (status input):
link A2 to B2

Buffered signal CLKIN drives SYNCA- pin and CLKOUT buffer:
link A2 to B2, and A4 to B4

TRxCA- pin drives CLKOUT buffer:
link A3 to A4

SYNCA- pin drives CLKOUT buffer:
link A4 to B4. B2 must be disconnected

TRxCA- pin drives RTxCA- pin: link A1 to B1, and A3 to B3, and insert a wire link between the two holes marked "X".

RTxCA- and SYNCA- pins are used to form a crystal oscillator:
link A1 to B1, and A3 to B3, and install a crystal in the two holes marked "X".

Whatever options are selected, it is advisable to ensure that the SCC input pins (RTxCA- and SYNCA-, normally) are driven by an active signal, rather than allowed to float. The TRxCA- pin must always be programmed explicitly as an output (see section 4.3).

DEFAULT CONFIGURATION

Most jumper options will be rarely if ever used. The following jumper positions are for a "standard" SL800 - that is, a card with vectored interrupts on ATNRQ1*, no DMA requests, with 4MHz chips, eight asynchronous RS-423 ports using internal baud rate generators.

With these settings, TRxCA- on each SCC will drive both RTxCA- and RTxCB- on the same chip, buffered CLKINA will drive both SYNCA- and the CLKOUTA buffer, and buffered CLKINB will drive both SYNCB- and the CLKOUTB buffer. TRxCB- is left disconnected so should be explicitly programmed as an output.

Note that the wire link in the crystal holes has the effect of linking TRxCA- and RTxCA-, so that RTxCA- is not left floating.

E1	link in position A
E2	no link
E3	links 0, 1 and 2 in positions 1, 0 and 0 respectively
E4	link in A position
E5	must strap I/O address here (cards are usually shipped strapped to FF0H)
E6	links A1 to B1, A2 to B2, and A4 to B4
E7	links A1 to B1, A2 to B2, A3 to B3, A4 to B4 and put a wire link in the two crystal holes.
E8	as for E6
E9	as for E7
E10	as for E6
E11	as for E7
E12	as for E6
E13	as for E7

APPENDIX C CONNECTOR PIN ASSIGNMENTS

A high density 100 way socket is provided to connect the SL800 to the outside world. The usual connector is a Hirose HIF6 series connector. This mates with a female connector carrying two 50 way flat ribbon cables. The female connector together with ribbon cables is normally supplied with each SL800.

If the Hirose connector is used then pin assignments on the ribbon cable have been chosen for convenient connection to remote connectors. In particular, it is possible to connect insulation-displacement D-type connectors to the cable and end up with "more or less" correct pin assignments on the D-type connector.

DSP Design can supply the SD800 Connector Card which routes the signals from the two 50 way ribbon cables to eight 25 way D-Type connectors.

There are two cables coming from the Hirose connector - the "top" cable and the "bottom" cable, which are defined as follows. The top cable is the cable which is top-most when the cable assembly is inserted in the SL800, and the SL800 is oriented component side face up. This corresponds to the two rows of connector pins (on the PCB) closest to the ICs. Pin 1 is closest to the top of the SL800 card, when the SL800 is oriented with the STEbus connector to the left and the 100 way connector to the right.

The signals of the eight serial channels are identified by their name followed by "A1", "A2", "B1", "B2" etc, which denotes their channel number: 1, 2, 3 or 4 for SCC No.1, No.2, No.3 or No.4 and A or B for the channel within each SCC.

The pin assignments for the two cables follow.

TOP CABLE PIN ASSIGNMENTS

PIN	SIGNAL	PIN	SIGNAL	
1	+12V	2	-12V	
3	DTRA1	4	0V (GND)	
5	+5V	6	DCDA1	
7	N/C	8	CTSA1	
9	N/C	10	RTSA1	SERIAL PORT A1
11	CLKOUTA1	12	RxDA1	
13	CLKINA1	14	TxDA1	
15	DTRA2	16	0V (GND)	
17	+5V	18	DCDA2	
19	N/C	20	CTSA2	
21	N/C	22	RTSA2	SERIAL PORT A2
23	CLKOUTA2	24	RxDA2	
25	CLKINA2	26	TxDA2	
27	DTRA3	28	0V (GND)	
29	+5V	30	DCDA3	
31	N/C	32	CTSA3	
33	N/C	34	RTSA3	SERIAL PORT A3
35	CLKOUTA3	36	RxDA3	
37	CLKINA3	38	TxDA3	
39	DTRA4	40	0V (GND)	
41	+5V	42	DCDA4	
43	N/C	44	CTSA4	
45	N/C	46	RTSA4	SERIAL PORT A4
47	CLKOUTA4	48	RxDA4	
49	CLKINA4	50	TxDA4	

BOTTOM CABLE PIN ASSIGNMENTS

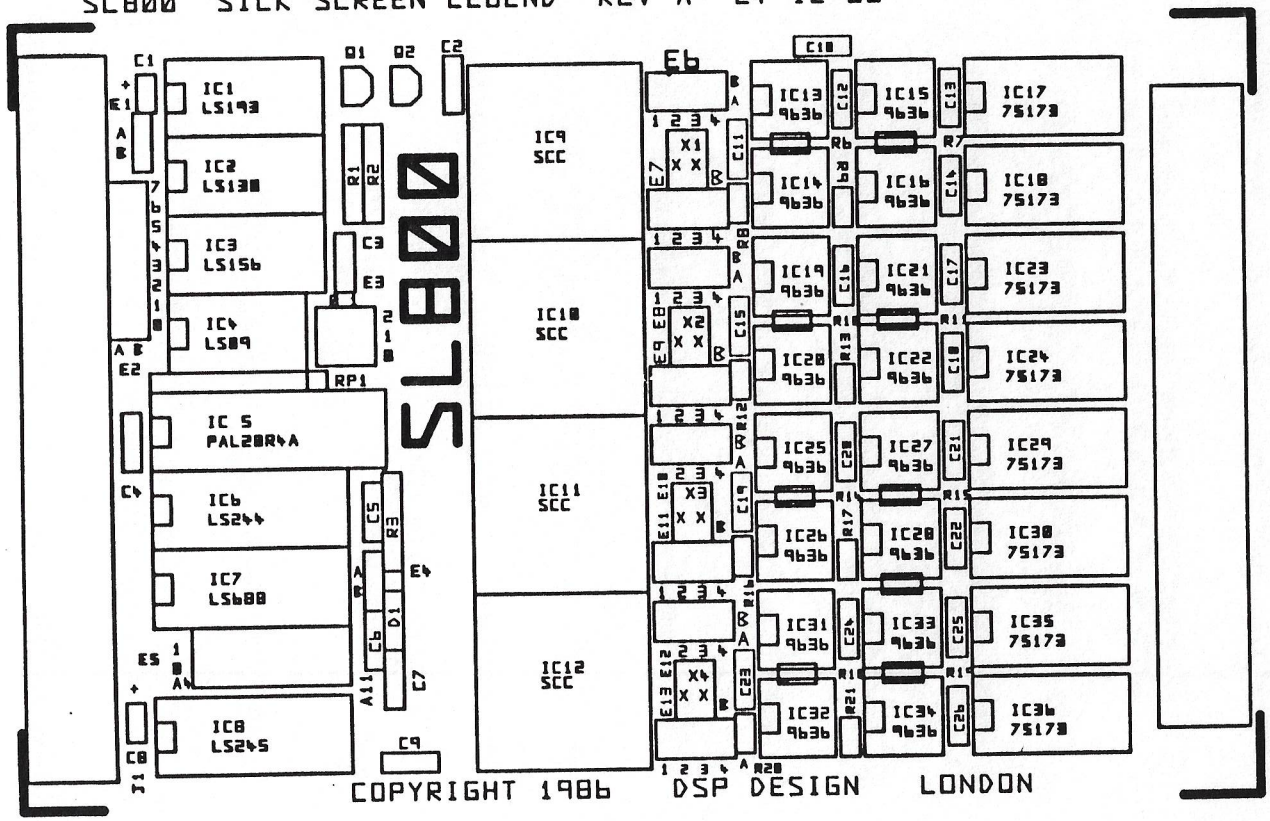
PIN	SIGNAL	PIN	SIGNAL	
1	+12V	2	-12V	
3	DTRB1	4	0V (GND)	
5	+5V	6	DCDB1	
7	N/C	8	CTSB1	
9	N/C	10	RTSB1	SERIAL PORT B1
11	CLKOUTB1	12	RxDB1	
13	CLKINB1	14	TxDB1	
15	DTRB2	16	0V (GND)	
17	+5V	18	DCDB2	
19	N/C	20	CTSB2	
21	N/C	22	RTSB2	SERIAL PORT B2
23	CLKOUTB2	24	RxDB2	
25	CLKINB2	26	TxDB2	
27	DTRB3	28	0V (GND)	
29	+5V	30	DCDB3	
31	N/C	32	CTSB3	
33	N/C	34	RTSB3	SERIAL PORT B3
35	CLKOUTB3	36	RxDB3	
37	CLKINB3	38	TxDB3	
39	DTRB4	40	0V (GND)	
41	+5V	42	DCDB4	
43	N/C	44	CTSB4	
45	N/C	46	RTSB4	SERIAL PORT B4
47	CLKOUTB4	48	RxDB4	
49	CLKINB4	50	TxDB4	

APPENDIX D COMPONENT PLACEMENT DIAGRAM

The diagram below shows the component placement on the SL800, and can be used to locate the various jumpers referred to in Appendix B and the text.

SL800.4 (7) R0 ON PHOTO.NIB T SILK SCREEN

SL800 SILK SCREEN LEGEND REV A 24-12-86



APPENDIX G ORDERING INFORMATION

The following part numbers should be used when ordering SL800 serial cards and related products:

SL200 *	Two channel version of SL800
SL400 *	Four channel version of SL800
SL600 *	Six channel version of SL800
SL800	Eight channel serial comms card
SD800	Connector card with eight female 25 pin D-type connectors. Interfaces to SL800 cable.

Related Products:

SL801	Eight channel comms card with RS-485 (RS-422 compatible) transceiver chips.
SL601 *	Six channel version of SL801.
SL401 *	Four channel version of SL801.
SL201 *	Two channel version of SL801.
SL802	Lower cost eight channel RS-232 serial card with fewer modem lines per channel.
SL802-C	All CMOS version of SL802.
SPL440	Four serial channels and forty parallel I/O lines on the one card.
SP800	Eighty line parallel I/O card.
SP600 *	Sixty line version of SP800.
SP400 *	Forty line version of SP800.
SP200 *	Twenty line version of SP800.
SP401	Lower cost CMOS forty line parallel I/O card.
SIG401	Signal conditioning card with forty opto-isolated input lines (SP800 compatible).
SIG402	Signal conditioning card with forty opto-isolated output lines (SP800 compatible).
SP488	Dual IEEE-488 controller card.

* Note that these products are available only on special order. Consult your distributor for details.

APPENDIX H FAULT REPORTING

DSP Design makes every effort to ship products and documentation which are completely free from faults, design errors and inconsistencies. Sometimes, however, problems do show up in the field. To help us put these right as quickly and efficiently as possible, we need as much information as possible from you, the user.

For this reason we have included here a "Product Fault Report" form. If you ever have cause to return a board for repair, or if you detect an error in the documentation, we would appreciate it if you could fill in the form on the next page, or a copy of it, and return the form with the goods to your dealer.

Prior to returning a faulty product, please check the following:

1. The board has been correctly configured for the intended application (see earlier appendix for board installation details).
2. The power supplies are providing correct voltage levels.
3. Cabling to the board is sound and connected correctly.
4. Other cards in the rack are known to be correctly configured and functioning.
5. **PLEASE RETURN THE BOARD TO US IN EXACTLY THE SAME CONFIGURATION AS IT FAILED IN.**

Your help with this will enable us to sort out your problem more quickly. Thank you.

PRODUCT FAULT REPORT

CUSTOMER INFORMATION

COMPANY NAME:

INDIVIDUAL CONTACT:

PHONE NO:

PRODUCT INFORMATION

PRODUCT/DOCUMENT:

SERIAL NO:

DATE OF RETURN:

SYMPTOMS OBSERVED /DOCUMENTATION ERRORS (as applicable):

IN WHAT CONFIGURATION IS THE BOARD USUALLY USED? (WHAT OTHER BOARDS, WHAT SOFTWARE ETC)?

****

FOR DSP DESIGN USE ONLY:

PRODUCT TEST REPORT:

DATE OF RECEIPT:

REPAIRED BY:

CHARGES TO BE INVOICED: £

DATE OF RETURN:

RETURNED BY:

APPENDIX J SPECIFICATION

Product: SL800

Description: Eight channel RS-232/RS-423 serial I/O card for the STEbus.

Dimensions: 100mm * 160mm (single Eurocard) PCB, overall dimensions (including connectors): 175mm * 100mm * 10mm.

Weight: 160g approx.

Operating temperature:
0 - 70 degrees C.

Humidity: 10% - 90% non-condensing.

Power Supplies:
+5V @ 1.5A max (1.25A typical)
+12V @ 275mA max (235mA typical)
-12V @ 275mA max (225mA typical)
These measurements apply to a card with no load; exact current consumption with a load connected will depend upon the nature of the load.

Connectors: DIN41612C, with rows A and C fully populated (STEbus connector), and Hirose HIF6-100P high density 100 way connector (serial interface).

STEbus interface:
I/O mapped bus slave. Fully conforms to IEEE 1000 specification.

Addressing: Occupies 16 bytes of I/O space, starting at any 16 byte boundary (jumper selectable).

Interrupts: Optional interrupt on any ATNRQn* line (jumper selectable).

DMA: Optional DMA request on any ATNRQn* line (jumper selectable).

Serial interface:
RS-232/RS-423 interface, using single ended drivers (uA9636A) and receivers (SN75173 with non-inverting inputs grounded), to two high density 50 way cables.