DSP DESIGN

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SM256

STEbus MEMORY CARD

TECHNICAL REFERENCE MANUAL

VERSION 6.0

9 AUGUST 1989

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REGISTERED OFFICE
23 BELLFIELD AVENUE
HARROW WEALD MIDDLESEX
REGISTERED IN ENGLAND
NUMBER 2121828

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APPENDICES

1.0 INTRODUCTION

This document describes the operation of the SM256 EPROM and static RAM memory card for the STEbus.

The SM256 fits any combination of static RAMs and EPROMs, in any combination of 8k, 16k and 32k byte chips, giving up to 256k of flexible memory address space. Flexible access times, robust battery backup and optional calendar clock are also featured.

The versatility of the SM256 memory card is in the tradition of powerful STEbus solutions from DSP Design. It provides the STEbus system designer with an answer for virtually all his or her memory design problems.

2.0 HARDWARE DESCRIPTION

The SM256 card has the following features:

* Eight sockets for memory chips, all of which can be individually configured to fit either an EPROM or a static RAM.

* Can fit eight 8k byte chips eg 2764 EPROM, 5565 SRAM
  or eight 16k byte chips eg 27128 EPROM
  or eight 32k byte chips eg 27256 EPROM, 55257 SRAM
  or any combination of 8k, 16k and 32k byte chips

* Flexible addressing:
  - the board address range can occupy 64k, 128k or 256k bytes of the 1M byte STEbus address map.
  - a board address range of n bytes can commence on any n byte boundary of the STEbus address map.
  - any or all chips can be individually deselected so that a gap appears in the address map.
  - all features are jumper selectable.

* Battery backup ensures data integrity during power failure or power-down by holding static RAMs in non-selectable, data retention mode.

* STEbus signal SYSRST* disables memory accesses and holds static RAMS in data retention mode.

* Flexible access times: from 50ns to 250ns in 50ns steps (jumper selectable) with the option of fitting a longer delay line for slower memory chips.

* Optional calendar clock.

* Fully conforms to IEEE 1000 (STEbus) specification.

3.0 FUNCTIONAL DESCRIPTION

The various sub-sections in this chapter describe the modes of operation of the SM256 and give instructions on how to configure the board for a particular application.

The text refers to the various strapping options - the key to the versatility of the SM256 card. A component placement diagram in Appendix C will be useful in locating these jumper areas.

3.1 ADDRESS MAPPING

The SM256 board address range can occupy 64k, 128k or 256k bytes of the 1M byte STEbus address map provided by A19-A0.

An SM256 with an n byte address range may be addressed on any n byte boundary within the STEbus address map.

The board address range is selected via jumper areas E3 and E4, while individual chip address slots may be selected, or deselected so that a gap appears in the memory map, via jumper area E1.

3.1.1 64K BYTE ADDRESS MAP: BOARD ADDRESS SELECTION

The SM256 may be configured for eight 8k byte memory areas, giving a total board address map of 64k bytes.

A19-A16 select the board addresses:

Board Addresses	*E3 Connection:	E4 Connections:
00000H-0FFFFH	A1-B1	
10000H-1FFFFH	A2-B2	
20000H-2FFFFH	A3-B3	A1-A2
30000H-3FFFFH	A4-B4	and
40000H-4FFFFH	A5-B5	B1-B2
50000H-5FFFFH	A6-B6	
60000H-6FFFFH	A7-B7	
70000H-7FFFFH	A8-B8	
80000H-8FFFFH	A1-B1	
90000H-9FFFFH	A2-B2	
A0000H-AFFFFH	A3-B3	A2-A3
B0000H-BFFFFH	A4-B4	and
C0000H-CFFFFH	A5-B5	B2-B3
D0000H-DFFFFH	A6-B6	
E0000H-EFFFFH	A7-B7	
F0000H-FFFFFH	A8-B8	

*all others disconnected

3.1.2 64K ADDRESS MAP: CHIP ADDRESS SELECTION/DESELECTION

A15-A13 select the chip addresses:

IC	*Chip Addresses	E1 Connections: to select	to deselect
12	00000H-01FFFH	A1-B1	B1-C1
13	02000H-03FFFH	A2-B2	B2-C2
14	04000H-05FFFH	A3-B3	B3-C3
15	06000H-07FFFH	A4-B4	B4-C4
16	08000H-09FFFH	A5-B5	B5-C5
17	0A000H-0BFFFH	A6-B6	B6-C6
18	0C000H-0DFFFH	A7-B7	B7-C7
19	0E000H-0FFFFH	A8-B8	B8-C8

* Example for board with starting address 00000H; for other board address ranges, offset these figures by the board starting address.

3.1.3 128K BYTE ADDRESS MAP: BOARD ADDRESS SELECTION

The SM256 may be configured for eight 16k byte memory areas, giving a total board address map of 128k bytes.

A19-A17 select the board addresses:

Board Addresses	*E3 Connection:	E4 Connections:
00000H-1FFFFH	A2-B2	A1-A2
20000H-3FFFFH	A4-B4	and
40000H-5FFFFH	A6-B6	B1-B2
60000H-7FFFFH	A8-B8	
80000H-9FFFFH	A2-B2	A2-A3
A0000H-BFFFFH	A4-B4	and
C0000H-DFFFFH	A6-B6	B2-B3
E0000H-FFFFFH	A8-B8	

*all others disconnected

3.1.4 128K ADDRESS MAP: CHIP ADDRESS SELECTION/DESELECTION

A16-A14 select the chip addresses:

IC	*Chip Addresses	E1 Connections: to select	to deselect
12	00000H-03FFFH	A1-B1	B1-C1
13	04000H-07FFFH	A2-B2	B2-C2
14	08000H-0BFFFH	A3-B3	B3-C3
15	0C000H-0FFFFH	A4-B4	B4-C4
16	10000H-13FFFH	A5-B5	B5-C5
17	14000H-17FFFH	A6-B6	B6-C6
18	18000H-1BFFFH	A7-B7	B7-C7
19	1C000H-1FFFFH	A8-B8	B8-C8

* Example for board with starting address 00000H; for other board address ranges, offset these figures by the board starting address.

3.1.5 256K BYTE ADDRESS MAP: BOARD ADDRESS SELECTION

The SM256 may be configured for eight 32k byte memory areas, giving a total board address map of 256k bytes.

A19-A18 select the board addresses:

Board Addresses	*E3 Connection:	E4 Connections:
00000H-3FFFFH	A4-B4	A1-A2
40000H-7FFFFH	A8-B8	and B1-B2
80000H-BFFFFH	A4-B4	A2-A3
C0000H-FFFFFH	A8-B8	and B2-B3

*all others disconnected

3.1.6 256K ADDRESS MAP: CHIP ADDRESS SELECTION/DESELECTION

A17-A15 select the chip addresses:

IC	*Chip Addresses	E1 Connections: to select	to deselect
12	00000H-07FFFH	A1-B1	B1-C1
13	08000H-0FFFFH	A2-B2	B2-C2
14	10000H-17FFFH	A3-B3	B3-C3
15	18000H-1FFFFH	A4-B4	B4-C4
16	20000H-27FFFH	A5-B5	B5-C5
17	28000H-2FFFFH	A6-B6	B6-C6
18	30000H-37FFFH	A7-B7	B7-C7
19	38000H-3FFFFH	A8-B8	B8-C8

* Example for board with starting address 00000H; for other board address ranges, offset these figures by the board starting address.

3.2 MEMORY SIZE

The SM256 is designed to be populated by either eight 8k byte chips or eight 32k byte chips. These choices are selected by alternative strapping options on the board and chip address decoders (jumper area E2).

However, it is also possible to populate the board with eight 16k byte chips by wire-wrapping jumper area E2.

Alternatively, the user may wish to mix large and small chips, or EPROMS and static RAMS, so individual strapping options on each memory chip socket are available.

The following table shows the eight memory chip sockets and their associated jumper areas for chip size/type selection (see sections 3.21, 3.22 and 3.23) and power supply selection (see section 3.51).

IC NO.	SELECT CHIP SIZE/TYPE	SELECT/DESELECT BATTERY BACKUP
12	E7	E6
13	E9	E8
14	E11	E10
15	E13	E12
16	E15	E14
17	E17	E16
18	E19	E18
19	E21	E20

3.2.1 MEMORY SIZE: EIGHT 8K BYTES = 64K BYTES

On 8k byte static RAMs, pin 26 functions as CS2 , so must be strapped to Vcc, via jumper E2. On 8k byte EPROMs, pin 26 is N/C so may be strapped to Vcc in the same way, or left unconnected.

A12-A0 are applied directly to the chips , so A19-A13 must be decoded by the board and chip address decoders.

To configure the board for a 64k byte address map, strap jumper E2 as shown:

E2 Connection:		A	B	C
A1-B1 A2-B2	1	*===*		*
A3-B3 A4-B4	2	*===*		*
A5-B5 A6-B6	3	*===*		*
	4	*===*		*
	5	*===*		*
	6	*===*		*

To configure a particular chip socket for an 8k byte chip, strap E7, E9, E11, E13, E15, E17, E19 and/or E21 as shown below. The reader may find it useful to refer to the component placement diagram in Appendix C, the chip address table in section 3.12 and the jumper area table in section 3.20.

Static RAM Strapping Option:		A	B	C	D
B1-C1 and	1		*===*		*
C2-D2	2	*	*	*===*	

EPROM Strapping Option:		A	B	C	D
C1-D1 and	1		*	*===*	
C2-D2	2	*	*	*===*	

3.2.2 MEMORY SIZE: EIGHT 16K BYTES = 128K BYTES

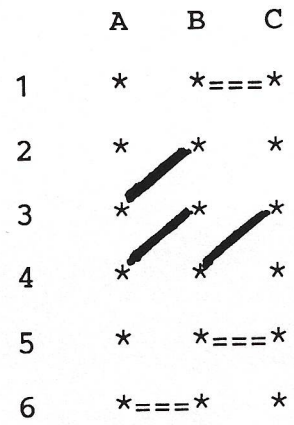
On 16k byte chips (EPROMs only), pin 26 functions as A13 so must be strapped to BA13, via jumper area E2.

A13-A0 are applied directly to the chips, so A19-A14 must be decoded by the board and chip address decoders.

To configure the board for a 128k byte address map, wire-wrap jumper area E2 as shown:

E2 Connection:

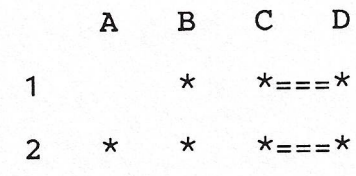
B1-C1
B2-A3
B3-A4
B4-C3
B5-C5
B6-A6



To configure a particular chip socket for a 16k byte chip, strap E7, E9, E11, E13, E15, E17, E19 and/or E21 as shown below. The reader may find it useful to refer to the component placement diagram in Appendix C, the chip address table in section 3.14 and the jumper area table in section 3.20.

EPROM Strapping Option:

C1-D1
and
C2-D2



3.2.3 MEMORY SIZE: EIGHT 32K BYTES = 256K BYTES

On 32k byte chips (EPROMs and static RAMs), pin 26 functions as A13 so must be strapped to BA13 via jumper area E2.

A14-A0 are applied to the chips directly, so A19-A14 must be decoded by the board and chip address decoders.

To configure the board for a 256k byte address map, strap jumper area E2 as shown:

E2 Connection:		A	B	C
B1-C1	1	*	*===*	
B2-C2				
B3-C3	2	*	*===*	
B4-C4				
B5-C5	3	*	*===*	
B6-C6				
	4	*	*===*	
	5	*	*===*	
	6	*	*===*	

To configure a particular chip socket for a 32k byte chip, strap E7, E9, E11, E13, E15, E17, E19 and/or E21 as shown below. The reader may find it useful to refer to the component placement diagram in Appendix C, the chip address table in section 3.16 and the jumper area table in section 3.20.

Static RAM Strapping Option:		A	B	C	D
B1-C1	1		*===*		*
and					
B2-C2	2	*	*===*		*

EPROM Strapping Option:		A	B	C	D
A2-B2	1		*	*	*
and					
C2-D2	2	*===*		*===*	

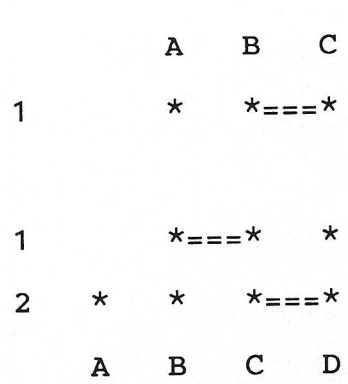
3.2.4 MEMORY SIZE: EIGHT 128K BYTES (PAGED) = 1M BYTES

Memory capacity on the SM256 can be extended up to 1M bytes using the 27011 paged mode EPROM. The 27011 128k byte EPROM is organised into eight 16k byte pages. One 27011 occupies 16k bytes. The SM256 containing eight 27011 EPROMs occupies 128k bytes of memory space and has a capacity of 1Mbyte.

To facilitate the use of the card in STEbus PC compatible systems software drivers are available. These allow the card to be used by the STEbus PC as a ROM disk with up to 1M byte capacity (see DSP Design's PC compatible range).

To accommodate 27011 EPROMS, jumper areas E1, E2, E3, E4 and E5 should be configured as though the devices were 16k byte EPROMS. E5 should be selected for the appropriate EPROM access time.

Jumper areas E6 to E21 should be configured for each 27011 EPROM as shown:-



3.3 MIXING MEMORY CHIP SIZES

It is possible to use a mixture of chip sizes on a single SM256 board; for example , six 32k byte EPROMs could be combined with two 8k byte static RAMs.

First, jumper area E2 must be configured for the largest chip size being used. Next, jumper areas E7, E9, E11, E13, E15, E17, E19 and E21 must be individually configured to make the appropriate connections to pins 1 and 27 of each memory chip (see sections 3.21, 3.22 and 3.23).

The user should read sections 3.31 and 3.32 completely before attempting to combine different chip sizes.

3.3.1 256K BYTE ADDRESS MAP: USE OF 8K OR 16K BYTE CHIPS

If the SM256 is configured for a 256k byte address map, each socket may be regarded as a 32k byte window.

A 16k byte chip may be placed in a 32k byte window, if the individual socket is strapped for a 16k byte chip. It must be noted that because the board is configured for 32k byte chips, A14 is not being decoded, so the chip may be addressed with either A14=0 or A14=1. Thus aliasing will occur, ie the 16k byte chip will appear simultaneously in two contiguous 16k address slots, so no gaps appear in the address map.

Similarly, an 8k byte chip may be placed in a 32k byte window, if the individual socket is strapped for an 8k byte chip.

An 8k byte EPROM may be addressed with A13=0 or A13=1, and A14=0 or A14=1. In this case neither A13 nor A14 are being decoded so the 8k byte chip appears simultaneously in four contiguous 8k address slots, and no gaps appear in the address map.

An 8k static RAM must always be addressed with A13=1, because CS2 will be strapped to A13 via jumper area E2. The static RAM may be addressed with either A14=0 or A14=1, so it will appear simultaneously in two non-contiguous 8k address slots, while two 8k gaps (where A13=0) appear in the address map.

For example, when using six 32k byte EPROMs at the low order chip addresses and two 8k byte static RAMs at the high order chip addresses, jumper area E2 must first be strapped as though for eight 32k byte chips. Next, jumper areas E7, E9, E11, E13, E15 and E17 must be strapped for 32k byte chips, and E19 and E21 must be strapped for 8k byte

chips.

In this example, the six 32k byte EPROMs will appear at addresses 00000H-07FFFH, 08000H-0FFFFH, 10000H-17FFFH, 18000H-1FFFFH, 20000H-27FFFH and 28000H-2FFFFH. The two 8k byte static RAMs must be addressed with A13=1, while A14 is not being decoded so becomes a 'don't care' bit, which gives rise to aliasing. Each static RAM will appear twice on the address map, ie at 32000H-33FFFH and 3A000H-3BFFFH respectively (A14=0, A13=1) and again at 36000H-37FFFH and 3E000H-3FFFFH respectively (A14=1, A13=1). Thus, gaps will appear in the address map at 30000H-31FFFH, 34000H-35FFFH, 38000H- 39FFFH, and 3C000H-3DFFFH.

3.3.2 128K BYTE ADDRESS MAP: USE OF 8K BYTE CHIPS

If the SM256 is configured for a 128k byte address map, each socket may be regarded as a 16k byte window.

An 8k byte chip may be placed in a 16k byte window, if the individual socket is strapped for an 8k byte chip. An 8k byte EPROM may be addressed with A13=0 or A13=1; in this case A13 is not being decoded so the 8k byte chip appears simultaneously in two contiguous 8k address slots, and no gaps appear in the address map.

An 8k static RAM must always be addressed with A13=1, because CS2 will be strapped to A13 via jumper area E2. In this case no aliasing will occur as the address bus will be fully decoded, but two 8k gaps (where A13=0) will appear in the address map. (See section 3.31 for an explanation of aliasing).

3.4 MEMORY TYPE: EPROM/STATIC RAM SELECTION

A single SM256 board may be populated by either static RAMs or EPROMs,or by a mixture of both.

While address and data pinouts coincide on common static RAMs and EPROMs of the same size, the positions of WE-, Vpp, and A14 (on 32k byte chips) vary on pins 1 and 27, according to chip size and type.

The pin 1 and 27 configuration for each memory chip socket can be individually selected via jumper areas E7, E9, E11, E13, E15, E17, E19 and E21. Strapping arrangements for these jumpers are shown in sections 3.21, 3.22 and 3.23.

3.5 BATTERY BACKUP/ LOW POWER MODE

3.5.1 BATTERY BACKUP

The SM256 uses an ICL7673 to provide automatic switching between the main power supply and battery backup, thus guaranteeing the integrity of data stored in the SRAMs during power failure or power-up and power-down.

Both input supplies are connected to the ICL7673; the normal +5V supply and a 3.6V NiCd secondary battery, which is trickle-charged during normal operation.

The ICL7673 compares the two and connects the higher to the board supply rail. When the battery backup is connected to the supply, a POWERFAIL signal is asserted which will disable the chip address decoder. This prevents potential random accesses to the static RAMs during power-down or power failure, and holds them in low-power, data retention mode. In this mode the static RAM supply current is reduced to a low standby current. This varies considerably between common static RAMs and will have a determining effect upon battery backup lifetime. Only low power static RAMs should be used with SM256 cards (see Appendix B).

Individual selection or deselection of battery backup to each memory chip socket is available via strapping options on jumper areas E6, E8, E10, E12, E14, E16, E18 and E20, as shown below.

The reader may also find it useful to refer to the component placement diagram in Appendix C. See section 3.20 for a reference table of memory chip sockets and their associated jumper areas.

Battery Backup Connection:	**to select**	**to deselect**
	A-B	B-C

NB: Note that battery backup selection may be required when EPROMs are installed in the SM256, to avoid unnecessary battery current drain. It is important to read Appendix B before installing any memory chips, or configuring the battery backup jumper areas.

3.5.2 SYSTEM RESET

The SM256 utilises the STEbus signal SYSRST* to assert an early POWERFAIL signal, thus holding the static RAMs in non-selectable, data retention mode.

SYSRST* is asserted by the STEbus controller card during power-on or push-button reset, and may additionally be asserted as an early indication of primary power failure. We recommend that the STEbus controller asserts SYSRST* during power-down to at least 3.5V, and during power-up from 3.5V to the minimum specified supply voltage (usually 4.6V).

The SX180, SP180, SZ801 and SV25, the STEbus CPU cards available from DSP Design, fully meet the recommended STEbus power-down protocol. That is, they assert the SYSRST* signal at any time that the power supply has fallen to a level between 4.55V (tolerance $\pm$0.05V) and 3.5V. The SM256 battery backup circuitry is guaranteed to continue to assert POWERFAIL after the primary power supply has fallen below 3.6V.

Battery backup will operate regardless of the characteristics of the SYSRST* signal; SYSRST* merely inhibits unwanted write cycles which might corrupt data during power-up and power-down.

3.6 ACCESS TIME SELECTION

The SM256 provides flexible access times: from 50ns to 250ns in 50ns steps. These are selected by strapping options on jumper E5.

The access time selected must be that of the slowest memory chip on the board.

Access Time	E5 Connection
50ns	A1-B1
100ns	A2-B2
150ns	A3-B3
200ns	A4-B4
250ns	A5-B5

An optional alternative delay line chip is available for users who wish to use EPROMs with access times longer than 250ns.

3.7 CALENDAR CLOCK OPTION

As an option, a calendar clock module can be fitted into any of the memory sockets. The "Smart Watch" module and a RAM chip ride piggy-back in the same socket, and a clever accessing algorithm ensures that the watch function is transparent to the RAM operation.

The calendar clock module may be ordered separately and fitted by the user. See Appendix D for ordering information.

APPENDIX A REFERENCES

1 STEbus Draft Proposed Standard, Draft 3.2
January 1986
Pub. IEEE Computer Society

APPENDIX B: INSTALLATION INSTRUCTIONS

1. In all cases, a memory chip must be installed in its socket before the battery backup voltage is selected for that socket. Failure to observe this could result in damage to the memory chip.

2. Only low power SRAMS (L suffix to part number) should be used in SM256 cards.

3. All memory chips other than NMOS EPROMS (ie SRAMs, CMOS EPROMs) MUST be used with battery backup selected, or unnecessary battery current drain will result.

4. If NMOS EPROM are used, then these MUST NOT have the battery backup link option selected, or unnecessary battery current drain will result.

APPENDIX C COMPONENT PLACEMENT DIAGRAM

The diagram below shows the component placement on the SM256, and can be used to locate the various jumpers referred to throughout the text.

SM-256
DSP DESIGN LONDON
IC18 MEMORY
IC19 MEMORY
IC16 MEMORY
IC17 MEMORY
IC14 MEMORY
IC15 MEMORY
IC12 MEMORY
IC13 MEMORY
IC7 HCT30
IC8 HCT138
IC9 HCT138
IC10 DELAYLI
IC11 7673
BATTERY 1
IC1 LS00
IC2 LS02
IC3 7407
IC4 LS621
IC5 LS621
IC6 LS621
RP1
RP2
RP3
RP4
T1
BACKPLANE

APPENDIX D ORDERING INFORMATION

The following part numbers should be used when ordering SM256 cards:

SM256	SM256 board with unpopulated sockets
SM256-P64	SM256 populated with eight 8k*8 RAM chips (64k bytes total)
SM256-P256	SM256 populated with eight 32k*8 RAM chips (256k bytes total)
STE-CLOCK	Plug in calendar clock module

APPENDIX E FAULT REPORTING

DSP Design makes every effort to ship products and documentation which are completely free from faults, design errors and inconsistencies. Sometimes, however, problems do show up in the field. To help us put these right as quickly and efficiently as possible, we need as much information as possible from you, the user.

For this reason we have included here a "Product Fault Report" form. If you ever have cause to return a board for repair, or if you detect an error in the documentation, we would appreciate it if you could fill in the form on the next page, or a copy of it, and return the form with the goods to your dealer.

Prior to returning a faulty product, please check the following:

1. The board has been correctly configured for the intended application (see earlier appendix for board installation details).

2. The power supplies are providing correct voltage levels.

3. Cabling to the board is sound and connected correctly.

4. Other cards in the rack are known to be correctly configured and functioning.

5. **PLEASE RETURN THE BOARD TO US IN EXACTLY THE SAME CONFIGURATION AS IT FAILED IN.**

Your help with this will enable us to sort out your problem more quickly. Thank you.

PRODUCT FAULT REPORT

CUSTOMER INFORMATION

COMPANY NAME:

INDIVIDUAL CONTACT:

PHONE NO:

PRODUCT INFORMATION

PRODUCT/DOCUMENT:

SERIAL NO:

DATE OF RETURN:

SYMPTOMS OBSERVED /DOCUMENTATION ERRORS (as applicable):

IN WHAT CONFIGURATION IS THE BOARD USUALLY USED? (WHAT OTHER BOARDS, WHAT SOFTWARE ETC)?

****

FOR DSP DESIGN USE ONLY:

PRODUCT TEST REPORT:

DATE OF RECEIPT:

REPAIRED BY:

CHARGES TO BE INVOICED: £

DATE OF RETURN:

RETURNED BY:

APPENDIX F SPECIFICATION

Product: SM256

Description: EPROM and/or static RAM card for the STEbus, taking any combination of 8k, 16k or 32k byte chips up to 256k bytes of memory.

Dimensions: 100mm * 160mm (single Eurocard) PCB, overall dimensions (including connectors): 168mm * 100mm * 15mm.

Weight: 130g approx. (unpopulated)

Operating temperature:
0 - 70 degrees C.

Humidity: 10% - 90% non-condensing.

Power Supply: +5V @ 360mA max (300mA typical)
These measurements apply to an unpopulated card; exact current consumption with memory installed will depend upon the number and type of memory chips.

Connectors: DIN41612C, with rows A and C fully populated (STEbus connector).

STEbus interface:
Memory mapped bus slave. Fully conforms to IEEE 1000 specification.

Addressing: Flexible addressing. Board address range can occupy 64k, 128k or 256k bytes of the 1M byte STEbus address map. Board address range of n bytes can commence on any n byte boundary of the STEbus address map. Any or all chips may be deselected. All these features are jumper selectable.

Access Times: Flexible, from 50ns to 250ns in 50ns steps (jumper selectable). Longer access times for slower chips are available with optional hardware modification.

Battery Backup:
Ensures data integrity during power failure or power-down by holding static RAMs in non-selectable, data retention mode. If the STEbus controller asserts SYSRST* during power-up, power-down and reset, this is additionally used to hold RAMs in data retention mode.