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SPI40

40 CHANNEL OPTO-ISOLATED

INPUT CARD FOR STEbus

TECHNICAL REFERENCE MANUAL

VERSION 1.0

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IMPORTANT NOTE

Note that the SPI40 is designed for interfacing to equipment powered by low voltage DC supplies. The opto-isolation stages are designed to isolate the STEbus logic from the effects to noise voltages which would otherwise be present. While a significant DC isolation can be expected **THE SPI40 SHOULD NOT BE USED IN SITUATIONS WHERE ISOLATION FROM HAZARDOUS VOLTAGES IS REQUIRED.**

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1 INTRODUCTION

The SPI40 is a high density opto-isolated input card for STEbus systems. It allows electrical signals from industrial plant at a variety of voltage levels to be converted to TTL level and so to be read by the STEbus processor.

The SPI40 offers the following features:

* 40 opto-isolated input lines.
* STEbus interface.
* Single Eurocard board.
* Low Power - mostly CMOS design (all CMOS and extended temperature range versions available).
* Input signals can be DC voltages of either polarity, or alternatively switch closures can be used as the input.
* A wide range of input voltages are possible.
* Input signals are connected by a 50 way ribbon cable connector.

2 INPUT SIGNAL PATH

The SPI40 is a 40-channel opto-isolated input card. The forty channels are grouped as five groups of eight channels, and each channel can be thought of as comprising an input section (connecting to the external equipment) and an output section (connecting to the STEbus logic). The input and output sections are separated by an optical-isolation barrier.

The following sections describe the input and output circuitry, and describe how the channels are divided into groups of eight.

2.1 Division of Circuitry

The SPI40 is divided into two sections, which are separated by the optical-isolation barrier. The Input Section takes the incoming signals from the 50 way connector and feeds them to the LED of the opto-isolator. The Output Section connects the photo transistor of the opto-isolator to TTL buffers with hysterisis and thence to the STEbus backplane. The two sections are discussed separately below, but both discussions will refer to the circuit of one of the 40 channels shown in Figure 1.

2.2 Input Section

The photo transistor is turned on by light emitted by the LED in the Input Section. Approximately 5mA must be passed through this LED to saturate the output photo transistor.

The SPI40 Input Section has been designed to offer as much flexibility as possible to the user. The LED can be turned on by connecting a positive or negative voltage to the INPUT pin on the 50 way connector, or a positive or negative supply voltage can be applied at the SUPPLY pin on the DIN connector which will leave the LED switched on until the INPUT pin is connected by a switch (or transistor etc) to the COMMON line. (See figure 1 for a diagram of each opto-isolator channel).

2.2.1 Positive Input Voltages.

Jumpers are used to steer current from the INPUT pins through the opto-isolator in the correct direction - ie for a positive input voltage the jumpers are placed in one position and for a negative input voltage the jumpers are placed in another position.

If the voltage at the INPUT pin, or the SUPPLY pin, is positive with respect to the COMMON pin, then the jumper links should be placed from pin A1 to A2, and from pin B1 to B2 in Figure 1.

When the SPI40 board is oriented with the STEbus DIN 41612 connector to the left and the 50 way input connector to the right, the jumper links on the board should be placed horizontally.

See Appendix B for more details on configuring the SPI40 card.

2.2.2 Negative Input Voltages

If the supply at the INPUT pin, or at the SUPPLY pin, is negative with respect to the COMMON pin, then the jumper links must be placed from pin A1 to B1, and A2 to B2 in Figure 1.

When the SPI40 board is oriented as described above, the jumper links should be placed vertically (see Appendix B for more details on configuring the SPI40 card).

2.2.3 Voltage Applied at Input Pin

If a positive voltage of sufficient amplitude is applied to the INPUT pin, the LED will turn on, causing the photo-transistor of the opto-isolator to turn on, bringing the TTL signal to a logic 0 state. If the INPUT pin is left open circuit, or connected to the COMMON pin, or if the voltage is too low, the photo-transistor will not turn on and the TTL signal will be at logic 1.

Resistor networks limit the current flowing through the LED and are chosen depending on the input voltages.

Each group of eight opto-isolators share an eight element resistor network for RN2 and an eight element resistor network for RN3 (see Figure 1). The RN3 networks are DIL packages installed in sockets so that they can be changed according to the application. Unfortunately board space did not permit the RN2 networks to be socketed, so they must be soldered in place. These networks are not normally fitted in the factory, and can be fitted if required by the user, or preferably the correct value can be ordered from DSP Design and fitted in the factory.

When a voltage is applied to the INPUT pin (for example through a switch to a +12V supply), then the resistor network RN2 (shown in Figure 1) should not be fitted. A suitable value of resistance should be chosen for resistor network RN3.

The value of RN3 should be chosen so that a current of 5mA flows through the LED. Since there is approximately 1V dropped across the LED, the value of RN3 can be chosen by the following formula:

$$RN3 = \frac{Vinput-1}{5} \quad K \text{ ohms}$$

This will give a value of RN3 in kilohms. Typical values for RN3 are given in Table 1.

RN2 should not be fitted for this mode of operation.

If the LED current exceeds 20mA the opto-isolator may be damaged. Users should take care that the nature of the incoming signal will not damage the SPI40 . In particular, care should be taken when switching off inductive loads as high energy pulses may occur.

VOLTAGE	RESISTANCE
5	750R
10	1K8
12	2K2
15	2K7
20	3K9
24	4K7
30	5K6
40	7K5
48	9K1

TABLE 1 : VALUES OF INPUT RESISTANCE
(RN2 or RN3 : see sections 2.2.3, 2.2.4)

2.2.4 Input Pin Switched to Common

When the application requires the use of switches connecting to a COMMON (0V) rail, the LED is driven from a SUPPLY rail through RN2. A very small value is chosen for RN3, so that when the external switch closes the LED is shorted to the COMMON rail and turns off.

A value of 33 ohms is suitable for RN3 in this mode of operation. Alternatively, shorting links can be placed across the RN3 socket.

The value of RN2 can be chosen from Table 1. RN2 can be fitted by the user, or DSP Design can factory fit a value of your choice. When fitting a resistor network, a 9-pin 8-resistor single in line (SIL) resistor network should be chosen. Pin 1 (the "common" pin) should be oriented towards the 50 way input connector.

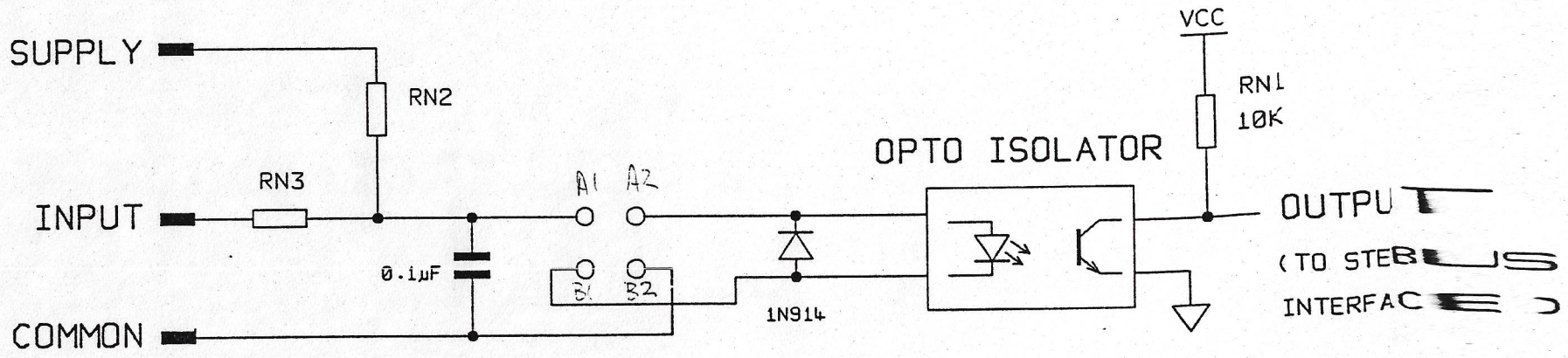


FIGURE 1: CIRCUIT OF ONE INPUT CHANNEL

2.3 Output Section

As shown in Figure 1, the Output Section consists of the photo transistor and a pull-up resistor. When no current is flowing through the LED the photo transistor is off and the pull-up resistor takes the OUTPUT pin to VCC potential (+5V, logic 1). When the LED is on the photo transistor is also on and the OUTPUT pin is pulled to GND potential (0V, logic 0).

The pin labeled OUTPUT in Figure 1 drives the input of a 74LS245 octal buffer. This TTL chip has been chosen over the CMOS version because its input features hysterisis, which can be of value reducing noise and oscillation of the data value when the input voltage is at a value where the phototransistor is neither switched hard on, nor completely off. On request DSP Design can replace the LS245 with a CMOS HC245, which lacks hysterisis but is lower power and allows extended temperature range operation.

There is no configuration required for the Output Section.

2.4 Division into Five Groups

Each of the forty channels of the SPI40 can be considered as consisting of an Input Section and an Output Section as described above. In addition, the forty channels can be considered to be divided into five groups of eight channels each. These groups are labelled A, B, C, D and E.

The five groups can be seen clearly by looking at the SPI40 itself, or at the component placement diagram in Appendix A. Each section consists of two 4-channel optical isolators, two resistor networks (RN2 and RN3), and associated components.

On the output side division into five groups of eight channels is convenient, as a group of eight signals can be conveniently bufferred by a 74LS245 octal buffer. The groups are labelled, top to bottom, A, B, C, D, and E.

On the input side, the division into five groups has two important consequences.

Firstly, each group has a single resistor network for RN2 and RN3, meaning that the value of the resistor in RN2 and RN3 is the same for each of the eight channels of that group. Each of the five groups, however, can use different values of RN2 and RN3, if the input voltages are different on different groups.

Secondly, each of the eight channels within a group share the same "COMMON" pin and the same "SUPPLY" pin on the 50

way input connector. This means that each group of eight inputs must be referenced to the same "COMMON" or return voltage, and if RN2 is used they must use the same supply voltage to turn on the opto-isolators. Each of the five groups however may use a different voltages for their COMMON and SUPPLY pins, and thus each group may be totally isolated from the other four.

2.5 Timing Considerations

As the SPI40 is normally connected to slow mechanical switches and the like, the speed of the card is unlikely to be an issue. However when the card is connected to faster signals, allowance must be made for the time it takes for the SPI40 to turn on and off.

2.5.1 Turn-On Time

When a voltage is applied to an INPUT pin the LED will turn on very quickly and the photo-transistor less quickly. The result is that the TTL signal drops to 0V (logic 0) in approximately 5uS.

2.5.2 Turn-Off Time

When the voltage is removed from the INPUT pin the LED will turn off very quickly and the photo-transistor less quickly. Once the transistor is off the pull-up resistors will charge the TTL line exponentially to +5V. The result is that the TTL signal rises to TTL logic 1 in approximately 100uS.

3 STEbus INTERFACE

The STEbus interface is extremely simple. The SPI40 occupies 8 addresses in the I/O space of the STEbus. The address can be selected by jumpers.

The SPI40 is read only, and reading five of the eight ports will return a byte representing the state of eight of the inputs. Reading from the other 3 addresses will return an indeterminate value.

The address of the SPI40 is set at the jumper area LK1. These jumpers are set to match address lines A4-A11, representing the base address of a 16 byte block. Address bit A3 must always be a 0 (this is the opposite of the SPO40 where A3 must always be a 1).

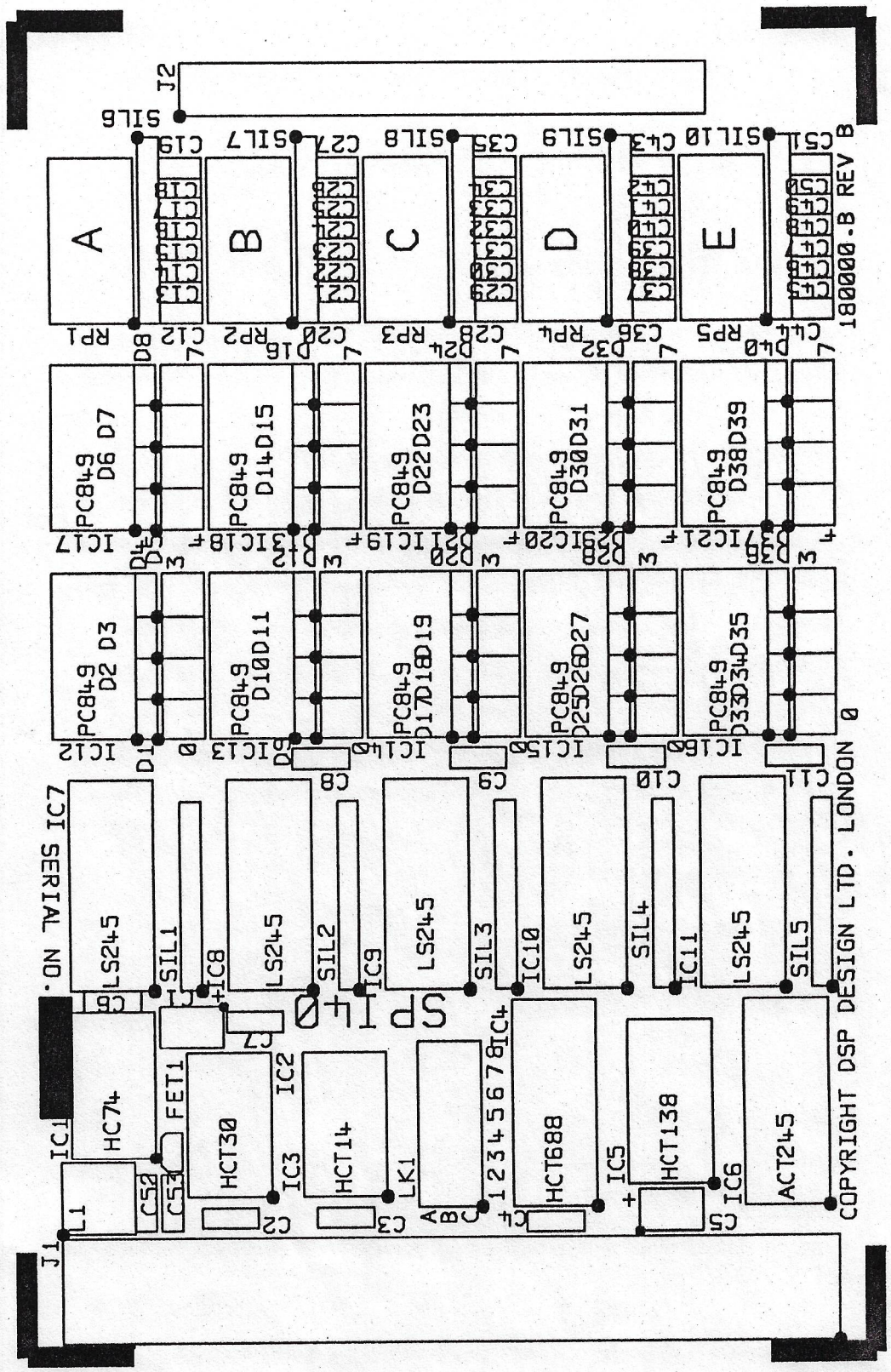
Appendix B describes how to set the jumpers at LK1 to select the I/O address of the SPI40.

Within the I/O address block allocated to the SPI40 the following address map applies. Appendix C gives a pin assignment for the input connector.

OFFSET ADDRESS	PORT ACCESSED
0	Port A - bits PA0-7
1	Port B - bits PB0-7
2	Port C - bits PC0-7
3	Port D - bits PD0-7
4	Port E - bits PE0-7
5	none - do not read
6	none - do not read
7	none - do not read
8-15	These addresses have A3=1 and so are not recognised by the SPI40.

APPENDIX A BOARD LAYOUT

This shows a SPI40 component placement. It can be used to help locate components referred to in the text.



APPENDIX B CONFIGURATION

There are 10 resistor networks and 40 pairs of jumpers which must be configured before the SPI40 can be used. In addition an STEbus address must be set up. The component placement diagram in Appendix A can be used to assist in the configuration of the card.

RN2 Resistor Network 2

Note that resistor network 2 (RN2) is the resistor which is labled as such on the circuit diagram of Figure 1. On the PCB itself there are five such single in line resistor networks (SILs), labeled SIL6 - SIL10. The term RN2 applies collectively to all of these SILs.

There are five of these 9 pin SIL networks, one for each of the five groups A-E. RN2 is used to supply current from the SUPPLY pin to the LEDs, in those cases where a switch at the INPUT pin shorts the LED to the COMMON pin. Its value should be chosen according to Table 1 (Section 2.2.3). RN2 should be omitted if an active voltage is to be applied at the INPUT pin (it is not fitted in the standard configuration).

Each of the five RN2 networks provides a resistor for eight channels.

RN2 should be a 9-pin 8-resistor SIL resistor network, oriented with pin 1 towards the 50 way input connector.

RN3 Resistor Network 3

Note that resistor network 3 (RN3) is the resistor which is labled as such on the circuit diagram of Figure 1. On the PCB itself there are five such dual in line resistors networks (DILs), labeled RP1 - RP5. The term RN3 applies collectively to all of these DILs.

There are five of these 16 pin DIL networks, one for each of the five groups A-E. RN3 is a current limiting resistor in series with the INPUT pin and the LED of the opto-isolator. Its value should be chosen according to Table 1 (Section 2.2.3). The Table 1 values for RN3 should be used if an active voltage is to be applied at the INPUT pin. If RN2 is used and the INPUT pin is connected by a switch to the COMMON pin, RN3 should be a very small value (say 33 ohms) or else replaced by shorting links.

Each of the five RN3 networks provides a resistor for eight channels.

The orientation of the resistor networks in the sockets is

unimportant as they are symmetrical.

Jumpers

There are a total of 80 jumpers associated with the input stages, one pair per channel. They are used to steer current from the INPUT pin in the correct direction through the opto-isolator LED, ie to accomodate input voltages of either potential.

The following instructions assume that the SPI40 board is oriented with the 50 way input connector to the right and the STEbus connector to the left.

If the voltage at the INPUT pin, or at the SUPPLY pin, is positive with respect of the COMMON pin, the jumper links should be placed horizontally.

If the supply at the INPUT pin, or at the SUPPLY pin, is negative with respect to the COMMON pin, then the jumper links must be placed vertically across the jumper area.

The SPI40 cards are supplied with the jumpers configured for positive INPUT voltages.

Each of the 40 channels can be configured separately, though normally all of the eight signals in each of the five groups A-E would be configured in the same way.

If the signals in each group are not all of the same polarity the following table should be used to locate the pair of jumpers relating to a particular INPUT pin. Refer to appendix A to locate the jumper areas.

Bit in TTL Port	Pair of jumpers on PCB
Bit 0	Jumpers labelled "0"
Bit 1	Jumpers labelled "1"
Bit 2	Jumpers labelled "2"
Bit 3	Jumpers labelled "3"
Bit 4	Jumpers labelled "4"
Bit 5	Jumpers labelled "5"
Bit 6	Jumpers labelled "6"
Bit 7	Jumpers labelled "7"

(Note that REV A boards are not correctly labelled in this respect).

Note that each pair of jumpers is a group of four pins.

Setting the STEbus I/O address

The address of the SPI40 is set at the jumper area LK1. These jumpers are set to match address lines A4-A11, representing the base address of a 16 byte block. Address bit A3 must always be a 0 (this is the opposite of the SPO40 where A3 must always be a 1).

To set the base address of the SPI40, first select an address which is mapped onto the STEbus by your processor. The STEbus (and the SPI40) supports a 12-bit I/O address space, but users of DSP Design's PC compatible computers should note that these processors adopt the PC convention and decode only a 10 bit I/O address (ie limit addresses to the range 100H-3F0H).

Convert the base address to a binary number, and set the links marked 1 - 8 to match bits A4 - A11 respectively of the I/O address. For a logic 1 place the link between rows A and B, and for a logic 0 between rows B and C. For example, for base address 300H (binary 0011 0000 0000) place jumpers 5 and 6 on rows A and B and the others btween rows B and C.

APPENDIX C PIN ASSIGNMENTS

The following table lists the pin assignments for the 50 way input connector (J2) and indicates the input connector pin which drives each of the bits of the five STEbus I/O ports.

The signals labelled PA0 etc are the 40 (five groups of eight) signals on the 50-way cable. The STEbus port in the table is the offset address from the base address of the SPI40.

J2 PIN NUMBER	SIGNAL NAME	STEbus PORT	J2 PIN NUMBER	SIGNAL NAME	STEbus PORT
1	PA0	0 bit 0	2	PA1	0 bit 1
3	PA2	0 bit 2	4	PA3	0 bit 3
5	PA4	0 bit 4	6	PA5	0 bit 5
7	PA6	0 bit 6	8	PA7	0 bit 7
9	SUPPLY A	-	10	COMMON A	-
11	PB0	1 bit 0	12	PB1	1 bit 1
13	PB2	1 bit 2	14	PB3	1 bit 3
15	PB4	1 bit 4	16	PB5	1 bit 5
17	PB6	1 bit 6	18	PB7	1 bit 7
19	SUPPLY B	-	20	COMMON B	-
21	PC0	2 bit 0	22	PC1	2 bit 1
23	PC2	2 bit 2	24	PC3	2 bit 3
25	PC4	2 bit 4	26	PC5	2 bit 5
27	PC6	2 bit 6	28	PC7	2 bit 7
29	SUPPLY C	-	30	COMMON C	-
31	PD0	3 bit 0	32	PD1	3 bit 1
33	PD2	3 bit 2	34	PD3	3 bit 3
35	PD4	3 bit 4	36	PD5	3 bit 5
37	PD6	3 bit 6	38	PD7	3 bit 7
39	SUPPLY D	-	40	COMMON D	-
41	PE0	4 bit 0	42	PE1	4 bit 1
43	PE2	4 bit 2	44	PE3	4 bit 3
45	PE4	4 bit 4	46	PE5	4 bit 5
47	PE6	4 bit 6	48	PE7	4 bit 7
49	SUPPLY E	-	50	COMMON E	-

PIN ASSIGNMENTS ON 50 WAY INPUT CABLE (CONNECTOR J2)

APPENDIX D ORDERING INFORMATION

The following part numbers should be used when ordering SPI40 products:

SPI40	40 channel opto-isolated input card, RN3 fitted for 24V inputs, RN2 not fitted (standard configuration).
SPI40-12V	SPI40 with RN3 optimised for 12V operation (for operation at other voltages change "-12V" as appropriate).
SPI40-1K	SPI40 with 1K ohm RN2 fitted (for other value resistors change "-1K" as appropriate)

RELATED PRODUCTS:

SPO40	40 channel opto-isolated output card with STEbus interface.
SP22	STEbus card for six Opto-22 opto-isolated input or output modules.
SIG401	40 channel digital opto-isolated input signal conditioning card with standard 50 way ribbon cable connector.
SIG402	40 channel digital opto-isolated output signal conditioning card with standard 50 way ribbon cable connector.
SP800	STEbus 80 channel digital I/O card (connects directly to SIG401 and SIG402)
SP401	STEbus 40 channel digital I/O card (connects directly to SIG401 and SIG402)
SPL440	STEbus I/O card with 4 serial ports and 40 parallel I/O lines.

APPENDIX E FAULT REPORT

DSP Design makes every effort to ship products and documentation which are completely free from faults, design errors and inconsistencies. Sometimes, however, problems do show up in the field. To help us put these right as quickly and efficiently as possible, we need as much information as possible from you, the user.

For this reason we have included here a "Product Fault Report" form. If you ever have cause to return a board for repair, or if you detect an error in the documentation, we would appreciate it if you could fill in the form on the next page, or a copy of it, and return the form with the goods to your dealer.

Prior to returning a faulty product, please check the following:

1. The board has been correctly configured for the intended application (see earlier appendix for board installation details).

2. The power supplies are providing correct voltage levels.

3. Cabling to the board is sound and connected correctly.

4. Other cards in the rack are known to be correctly configured and functioning.

5. **PLEASE RETURN THE BOARD TO US IN EXACTLY THE SAME CONFIGURATION AS IT FAILED IN.**

Your help with this will enable us to sort out your problem more quickly. Thank you.

PRODUCT FAULT REPORT

CUSTOMER INFORMATION

COMPANY NAME:

INDIVIDUAL CONTACT:

PHONE NO:

PRODUCT INFORMATION

PRODUCT/DOCUMENT:

SERIAL NO:

DATE OF RETURN:

SYMPTOMS OBSERVED /DOCUMENTATION ERRORS (as applicable):

IN WHAT CONFIGURATION IS THE BOARD USUALLY USED? (WHAT OTHER BOARDS, WHAT SOFTWARE ETC)?

****

FOR DSP DESIGN USE ONLY:

PRODUCT TEST REPORT:

DATE OF RECEIPT:

REPAIRED BY:

CHARGES TO BE INVOICED: £

DATE OF RETURN:

RETURNED BY:

APPENDIX F SPECIFICATION

Product: SPI40

Description: 40 channel opto-isolated input card.

Bus Interface: STEbus I/O slave card (occupies 8 I/O locations - jumper selectable).

Dimensions: 100mm * 160mm (single Eurocard) PCB, overall dimensions (including connectors): 188mm * 100mm * 15mm

Input stage: user selected resistor in series with an LED (approx 5-8mA current required). 100nF filter capacitor and reversed diode across LED. Max. input current is 20mA - choose resistors to ensure this is not exceeded.

Input Connector: 50 way male right angle connector with latches.

Power Requirement:
+5V @ 90mA approx, with all opto-isolators off. Add approx 20mA if all opto-isolators are on.

Channel Grouping: Five groups of eight channels, each group sharing resistor networks and a COMMON rail.

Isolation: The output sections are optically isolated from the input sections. Output sections are divided into five groups which may be isolated from each other. Isolation of 50V can be comfortably achieved - for higher isolation consult DSP Design. See important note below.

Weight: 160g approx.

Operating temperature: -0 to +70 degrees C (this spec is set by the use of LS245 chips. Extended temeperature range can be provided by using HC245 chips - ask!).

Operating Humidity: 10% - 90% non-condensing

IMPORTANT NOTE

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