System 1000 STEBus Card

1021

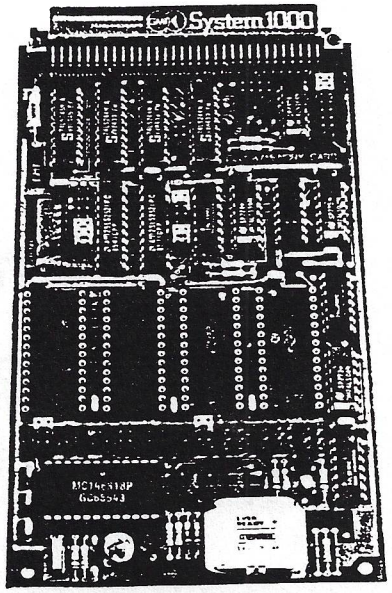
Bytewide Memory/Clock

GMT Electronic Systems Ltd
A division of GMT Group
Unit 7 Mole Business Park
Leatherhead, Surrey
KT22 7BA
England
Tel: 0372-373603
Fax: 0372-373098

STE Bytewide Memory/Clock

1021

- IEEE 1000 (STE bus) Compatible
- Four 28 Pin Memory Sockets
- Suitable for SRAM or EPROM
- Flexible Configuration
- Presettable Device Access Times
- Mapping for STE 1 Mbyte range
- Real Time Calendar/Clock
- On-card Battery Back-up



The 1021 Memory/Clock card combines the two functions of a system which may require protection during power down conditions, namely those of Random Access Memory and Real Time Clock. It can be used in systems where maintenance of real time is essential or desirable and where data retention in memory is required whether the card is retained in the system or not.

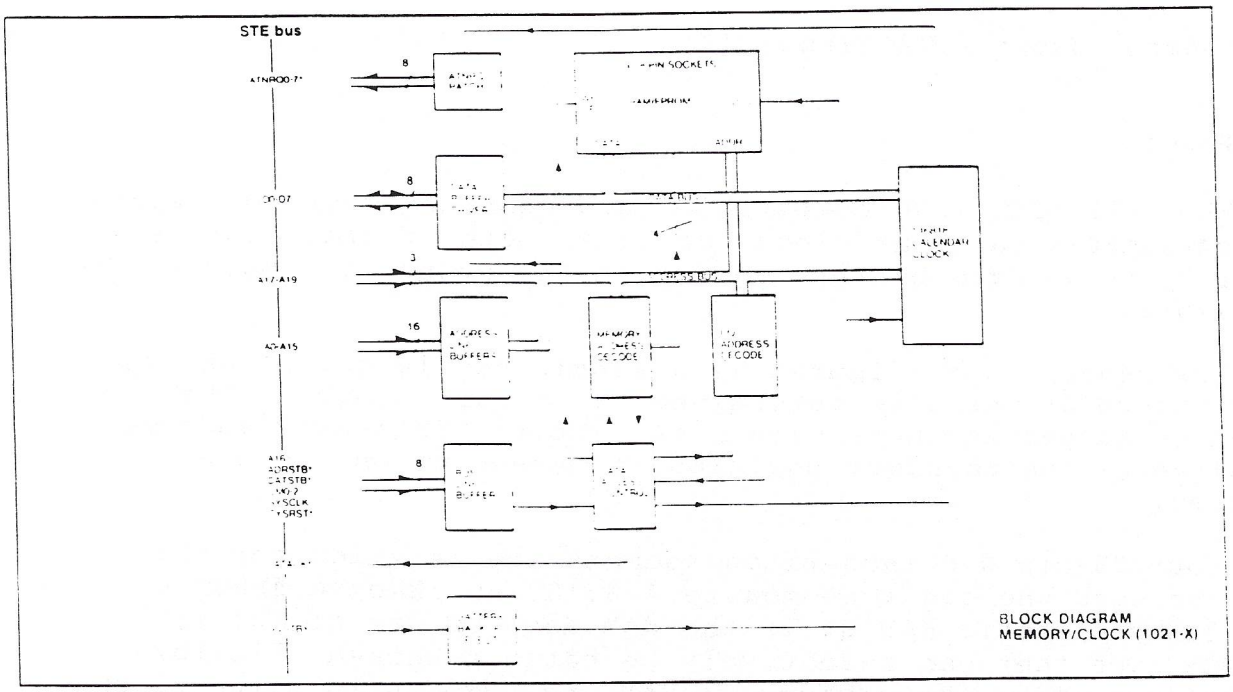
The memory section of the card comprises four 28 Pin, 0.6 inch pitch sockets which can be configured to accept either SRAM or EPROM devices. Device size selection ranges from 4 Kbyte to 32 Kbyte and is independently selectable for each socket. The memory area is designed as a contiguous block which can be positioned by on-card jumpers, on to any boundary corresponding to the block size selected within the full STE 1 Mbyte addressing range. Not only can the size of the memory in each socket be different but also the number of sockets used in the block is variable. This enables the card to be used in a wide range of sizes of system either as the sole source of memory or as an integral protected part. To further optimise the performance of the card a device speed setting is provided as a jumper selectable function. Access times between 75 and 460 nano-seconds are provided and setting is according to the slowest device fitted to the card.

An STE bus I/O interface is used on the card to communicate with the real time clock. The interface requires 16 bytes and can be mapped, by jumper selection, on to any 16 byte boundary within the STE 4 Kbyte I/O page. The Clock provides readable real-time down to seconds and a calendar which counts days of the week, date, month and year. It provides a real-time interrupt facility which is variable between 122 micro-seconds and 500 milliseconds and in addition there is a presettable alarm giving a time of day interrupt. The interrupt signals can be routed via jumpers to any of the STE bus Attention Request lines.

Facilities are provided to power the Calendar/Clock and optionally any number of the memory sockets from an on-card battery or from the STE bus Voltage Standby (+VSTBY) line, the selection between the two being by means of on-card jumpers. Use of the on-card battery, when fully charged, gives protection for a period of approximately two months for the calendar/clock alone and typically 500 hours when memory is included.

STE Bytewide Memory/Clock

1021



BLOCK DIAGRAM
MEMORY/CLOCK (1021-X)

SPECIFICATION

STE Memory Interface
Full addressing range

Memory Capacity
Up to 128 Kbyte

Memory Devices
8 or 32 Kbyte Static RAMs
4, 8, 16 or 32 Kbyte EPROMs

Block Size
4 Kbyte to 128 Kbyte
1 to 4 sockets

Block Mapping
Any boundary based on block size

Access Time Selection
75, 135, 200, 260, 335, 395, 460 nS

Real Time Clock
146818 Calendar/Clock generator
32.768 KHz on-card Time Base with trimmer
Range from 99 years to 1 second including 'day of week'
Hours/Minutes/Seconds Alarm
Programmable Interrupt range: 2Hz to 8.192 KHz

I/O Mapping
Any 16 byte block in STE 4 Kbyte I/O Page

Interrupt Routing
Any Attention Request line

Current Consumption
(Typical at 25°C)
+5 Volt: 0.2 A (without memory)

Operating Temperature
0 - 70°C

ORDERING INFORMATION

Part No.	Description
1021-1	Without Memory Devices

GMT Electronic Systems
Unit 7, Mole Business Park
Leatherhead, Surrey KT22 7BA
Phone: Leatherhead (0372) 373603
Fax: 0372 373098
Telex: 94012813 (GMTE G)
y KT18 7HN
180 Fax No. 03727 26999

MEMORY/CLOCK CARD DESCRIPTION

Use with board number -1021 issue #2.

GENERAL

This STE IEEE 1000 compatible card combines bytewide memory and a programmable calendar/clock facility, both of which can be backed up by an on-card battery source in the event of a main system power failure.

The memory is configured as a single contiguous block, the size and makeup of which is determined by on-card jumpers. The block can be mapped anywhere within the 1Mbyte STE memory address range, although the boundary position is dependent on the block size chosen.

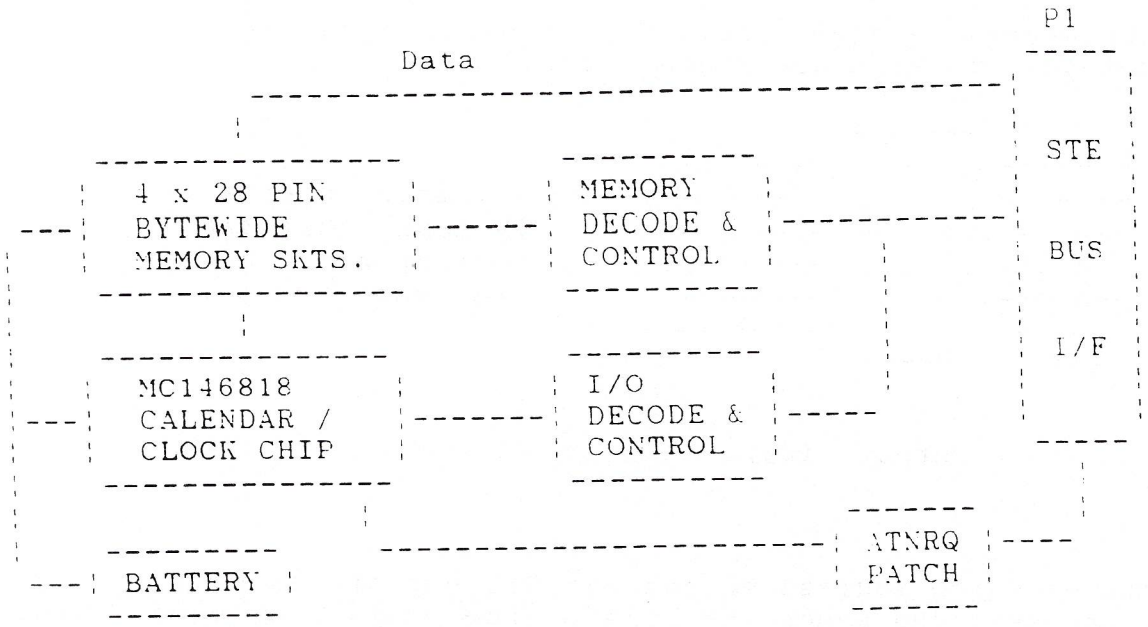
Four 28-pin 0.6 inch-pitch sockets are provided for the memory, and each one can accommodate 4,8,16, or 32Kbyte EPROM's or 8 or 32Kbyte static RAM's. If the RAM devices are of the low-power CMOS type they can selectively be battery-backed. Flexible jumper options allow the mixture of RAM and EPROM within the block, although device speed selection must be set for the slowest device used.

A separate STE I/O interface is used to communicate with the calendar/clock device which can be jumper-set onto any 16-byte boundary within the STE I/O page. It is accessed as two registers; one address and one data. The clock provides readable time down to seconds and a calendar which counts days of the week, date, month and year. A programmable real-time clock can be set to provide a periodic interrupt, and also a time-of-day alarm can be set up. The interrupt from the device can be jumper-routed to any one of the eight STE Attention Request lines.

The on-card battery is a 3.6V 100mAh NiCad type which should maintain the calendar/clock information for up to 2 months from power-down at full charge. The addition of RAM will reduce this period accordingly.

All jumper references in the following text assume that the card is orientated with P1 on the right.

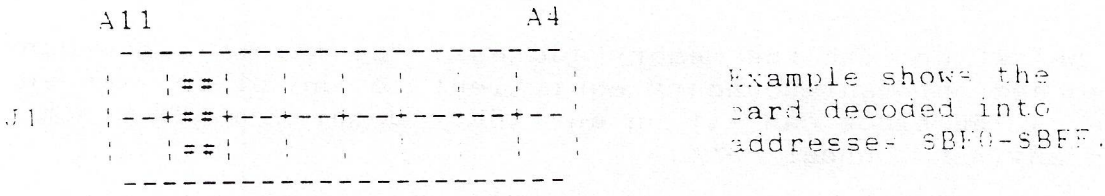
BLOCK DIAGRAM



ADDRESS DECODING

I/O (J1)

Jumper field J1 is used to decode I/O addresses A11 - A4. A jumper inserted means that the corresponding address line must be low.



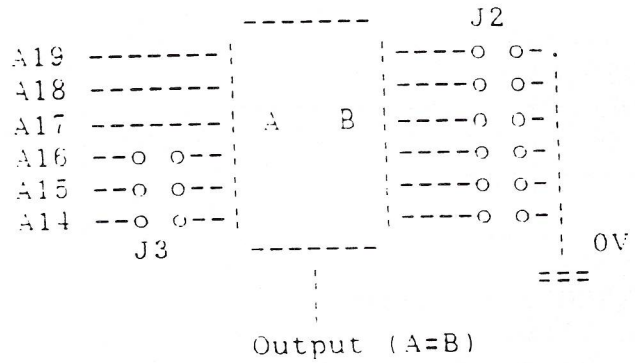
Once decoded, the logic on the card uses address A0 to determine whether the bus is accessing the address or data register within the calendar/clock device.

A0 = 0 ; Address register (write-only)
A0 = 1 ; Data register (read or write)

The address register must always be set up BEFORE reading or writing any data.

MEMORY (J2,J3)

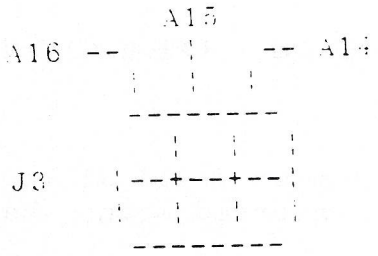
The memory decoder consists of a 6-bit comparator, the circuit details of which are shown below.



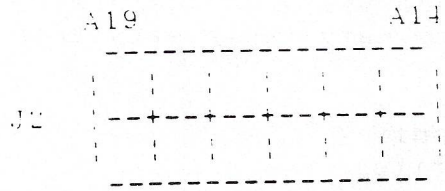
A jumper inserted in J2 means that the corresponding address line must be low.

J3 determines which addresses from the STE bus are involved in the decoding process, and hence the size of the contiguous memory block.

ADDRESSES USED	BLOCK SIZE
A16,A15,A14	16K
A16,A15	32K
A16	64K
J3 OPEN	128K



J2 should be set up with the memory address. The memory block can only be decoded onto any boundary equivalent to the block size selected. I.e. a 16K block can sit on any 16K boundary, a 32K block can sit on any 32K boundary etc.

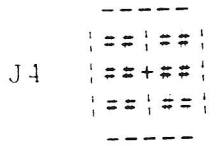


*** NOTE ***

Any jumpers removed from J3 must also be removed from J2, otherwise the decoder will not function.

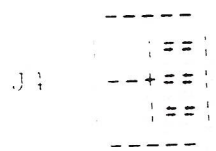
DEVICE SELECTION (J4)

The four 28-pin memory sockets are selected by decoding two address lines from the STE bus; the two lines used are dependent on the setting of J4. Note that partitioning can only be in equal parts.



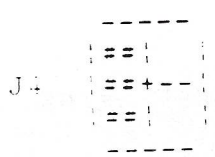
(4K)

A13	A12	DEVICE SELECTED
0	0	IC11
0	1	IC12
1	0	IC13
1	1	IC14



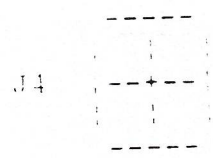
(8K)

A14	A13	DEVICE SELECTED
0	0	IC11
0	1	IC12
1	0	IC13
1	1	IC14



(16K)

A15	A14	DEVICE SELECTED
0	0	IC11
0	1	IC12
1	0	IC13
1	1	IC14

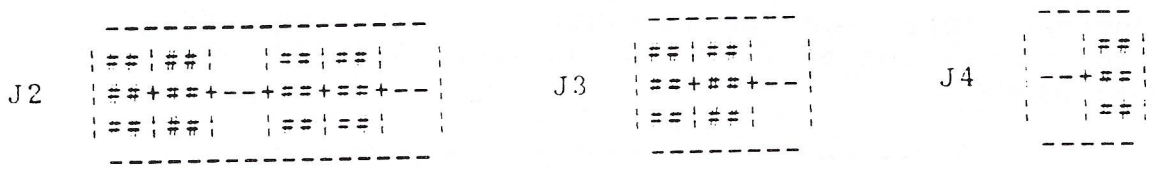


(32K)

A16	A15	DEVICE SELECTED
0	0	IC11
0	1	IC12
1	0	IC13
1	1	IC14

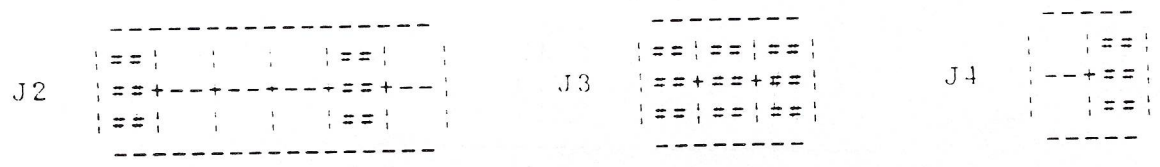
The options provided in the decoding allow the card to be fitted with 1,2 or 4 devices. The following examples should assist the system designer in making optimum use of the card.

Ex.1 - 32K of RAM located between addresses $20000 - $27FFF using 8K devices.



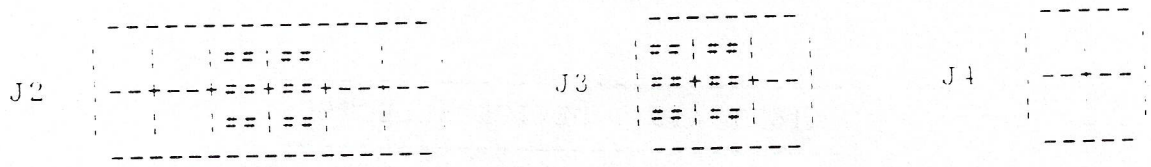
IC11 ; $20000 - $21FFF
IC12 ; $22000 - $23FFF
IC13 ; $24000 - $25FFF
IC14 ; $26000 - $27FFF

Ex.2 - 16K of RAM located between addresses $74000 - $77FFF using 8K devices.



IC13 ; $74000 - $75FFF
IC14 ; $76000 - $77FFF

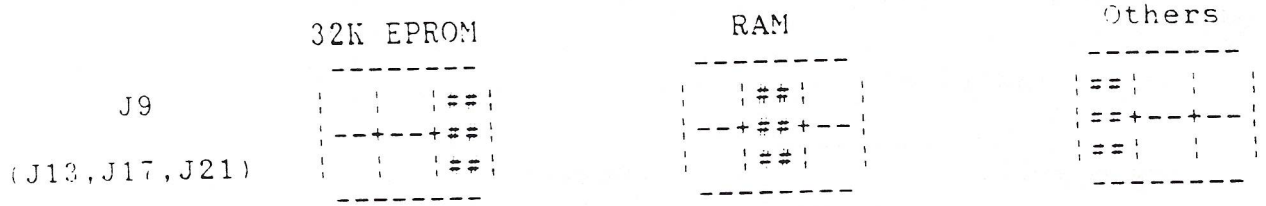
Ex.3 - 32K of EPROM located between addresses $C8000 - $CFFFF using a single 32K device.

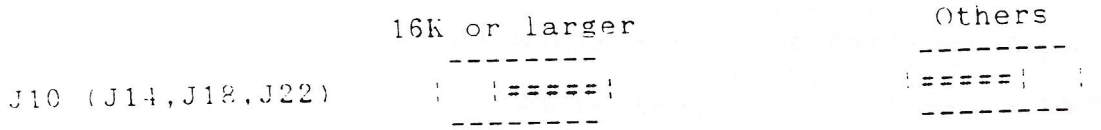


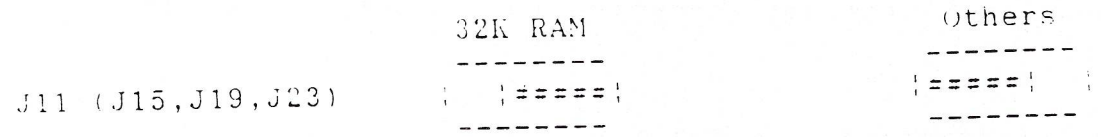
IC12 ; $C8000 - $CFFFF

DEVICE TYPE SELECTION (J8-23)

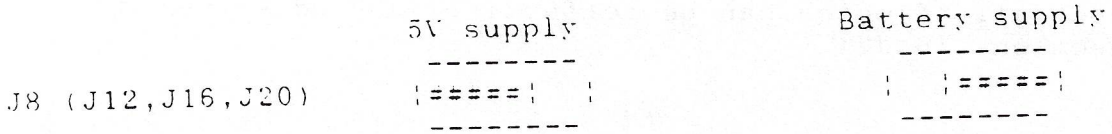
Each socket is individually configurable to take 8K or 32Kbyte RAM, or 4K, 8K, 16K or 32Kbyte EPROM devices. The following description relates to the jumpers connected to IC11 (with the equivalent jumper positions for IC12, IC13 and IC14 shown in brackets).





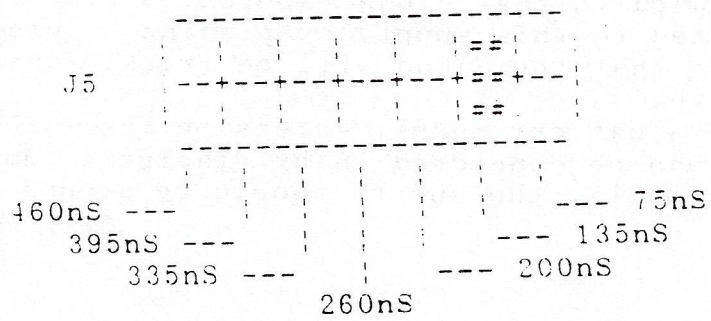


J8 is specifically concerned with connecting the battery supply to the socket, and should ONLY be used with low-power CMOS RAM.



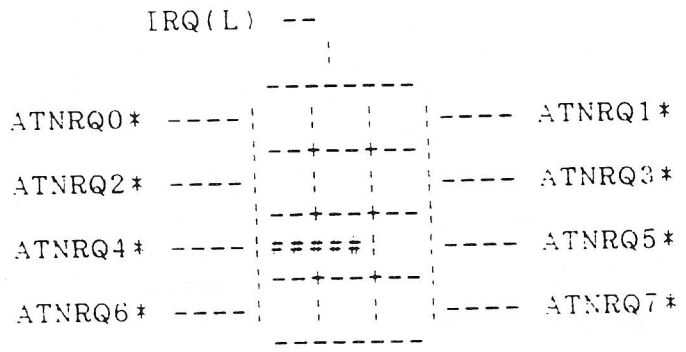
MEMORY ACCESS TIME (J5)

One jumper should be placed in J5 to correspond to the longest data access time (read or write) of the slowest memory device used on the card. The times shown are guaranteed minimum times, and they also correspond to the WRITE pulse width in the case of RAM.



ATTENTION REQUEST PATCH (J6, J7)

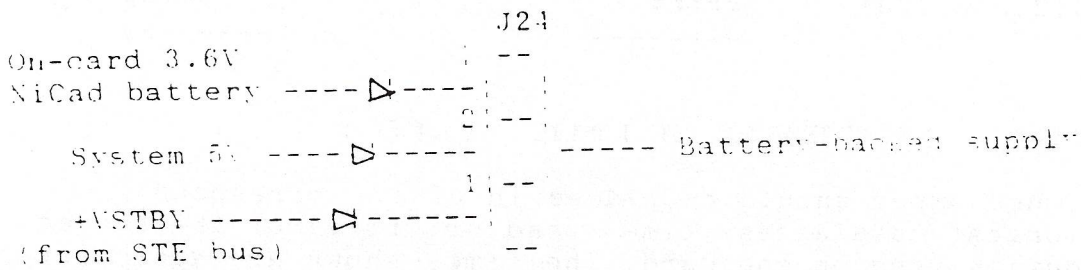
The calendar/clock device can be programmed to produce an interrupt in response to a number of internal events and conditions. This interrupt line can be routed to any one of the eight STE Attention Request line by placing a single jumper in J6 or J7, so connecting the middle row of pins to one of the outside pins.



The example shows the interrupt connected to ATNRQ4* on the bus.

BATTERY SUPPLY (J24)

The battery-backed supply which is used by the calendar/clock and any low-power RAM devices can originate from three sources, all of which can be (effectively) diode-mixed by making connections in J24.



The system 5V is permanently connected to the battery-backed supply via a low forward-voltage diode (approx. 0.2V). The battery is then be connected to this supply by placing a jumper between pins 2 and 3. Note that the NiCad will be trickle-charged when the system 5V is active.
Alternatively, if a battery supply exists on the +VSTBY line (c29) on the bus, this can be connected in by placing a jumper between pins 1 and 2. Optimally, the supply should be around 3V.

CAPACITY

The on-card battery capacity when fully charged is 100mAh. The minimum amount of time that this will keep the calendar/clock and RAM contents backed up is given by :

$$\frac{100}{I.cal(max) + I.ram(max)} \text{ hours}$$

where I.cal(max) = 0.1mA
I.ram(max) = total maximum low-power standby current taken by RAM in mA (e.g 0.1mA for Hitachi HM6264LP).

The 1021 board consumes 0.2A (typical) @ +5V, 25 C (no memory fitted).

APPENDIX
146818 PROGRAMMING REFERENCE

The internal address map of the calendar/clock chip is as follows.

Address (hex)	Function	Decimal range
0	seconds	0 - 59
1	seconds alarm	0 - 59
2	minutes	0 - 59
3	minutes alarm	0 - 59
4	hours (12-hour mode)	1 - 12 *
	hours (24-hour mode)	0 - 23
5	hours alarm (12)	1 - 12 *
	hours alarm (24)	0 - 23
6	day of week (Sunday=1)	1 - 7
7	date of month	1 - 31
8	month	1 - 12
9	year	0 - 99

* Note, in 12-hour mode the AM range is $0 - $C and the PM range is $81 - $8C.

There are a further four registers A,B,C and D used for initialisation and control of the 146818.

Register A ($0A)

MSB							LSB
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP - 1 = update in progress
0 = not in progress

This is a read only status bit to indicate to the control software when it should try to read or update calendar/clock information. When this bit is set to '0' it is an indication that an update will not occur for at least 244uS.

DV2 - DV0 The divider bits should be set to '010' since the 146818 uses the 32.768 kHz time-base. Values '110' or '111' can be used to reset the divider chain.

RS3 - RS0 These bits select the periodic interrupt rate as shown (rates assume 32.768 kHz time-base).

RS3	RS2	RS1	RS0	Interrupt rate	SQW output
0	0	0	0	None	None
0	0	0	1	3.90625 mS	256 Hz
0	0	1	0	7.8125 mS	128 Hz
0	0	1	1	122.070 uS	8.192 kHz
0	1	0	0	244.141 uS	4.096 kHz
0	1	0	1	488.281 uS	2.048 kHz
0	1	1	0	976.562 uS	1.024 kHz
0	1	1	1	1.953125 mS	512 Hz
1	0	0	0	3.90625 mS	256 Hz
1	0	0	1	7.8125 mS	128 Hz
1	0	1	0	15.625 mS	64 Hz
1	0	1	1	31.25 mS	32 Hz
1	1	0	0	62.5 mS	16 Hz
1	1	0	1	125 mS	8 Hz
1	1	1	0	250 mS	4 Hz
1	1	1	1	500 mS	2 Hz

Register B ($0B)

MSB LSB

SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

All bits in this register are software-controlled.

SET - 1 = any update cycle in progress is aborted and the program may initialise the time and calendar bytes without an update occurring.
0 = the update cycle functions normally.

PIE - 1 = periodic interrupt flag causes the IRQ line to be driven low.
0 = IRQ is not affected by the periodic interrupt.

This bit is cleared by RESET.

AIE - 1 = alarm flag causes the IRQ line to be driven low.
0 = IRQ is not affected by an alarm.

This bit is cleared by RESET

UIE - 1 = update-end flag causes the IRQ line to be driven low.
0 = IRQ is not affected by update-end.

This bit is cleared by RESET or the SET bit going high.

SQWE - 1 = SQW output (pin 23) is active.
0 = SQW output is inactive.

This bit is cleared by RESET.

DM - 1 = time and calendar values are in binary format.
0 = time and calendar values are in BCD format.

24/12 - 1 = 24-hour mode
0 = 12-hour mode

DSE - Daylight Savings Enable bit.
1 = time increment from 1:59:59 AM to 3:00:00 AM on the last Sunday in April, and a time increment from 1:59:59 AM to 1:00:00 AM on the last Sunday in October.
0 = no special updates.

Register C ($0C)

MSB							LSB
IRQF	PF	AF	UF	0	0	0	0

This is a read-only register.

IRQF = $\overline{[PF * PIE]} + \overline{[AF * AIE]} + \overline{[UF * UIE]}$
i.e. it will be high when the IRQ line is low.

PF - periodic interrupt flag.

AF - alarm interrupt flag.

UF - update-ended interrupt flag.

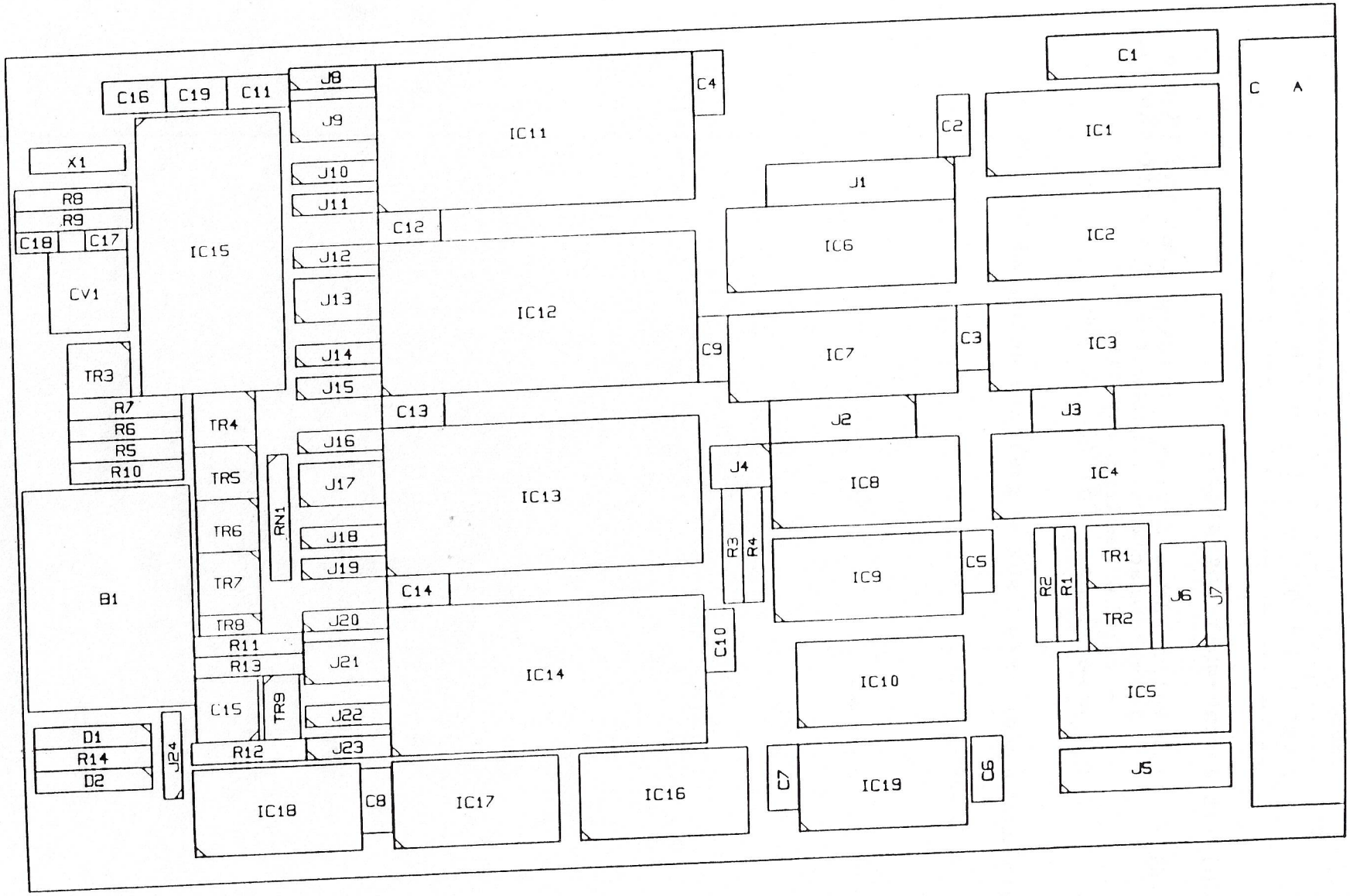
Register D ($0D)

MSB							LSB
VRT	0	0	0	0	0	0	0

This is a read-only register.

VRT - 1 = valid RAM and time providing that the PS pin is satisfactorily connected. This bit can only be set by reading register D.
0 = power-sense (PS) pin is low.

The remaining 50 addresses ($0E - $3F) are occupied by RAM.


C16
C19
C11
J8
J9
IC11
C4
C1
C A
X1
R8
R9
C18
C17
CV1
IC15
J10
J11
C12
J12
J13
IC12
C2
IC1
J1
IC6
IC2
C9
IC7
C3
IC3
TR3
R7
R6
R5
R10
TR4
TR5
TR6
TR7
TR8
J14
J15
C13
J16
J17
IC13
J18
J19
C14
J2
J3
J4
IC8
IC4
R3
R4
RN1
B1
R11
R13
C15
TR9
J20
J21
J22
J23
IC14
C10
IC9
C5
R2
R1
TR1
TR2
J6
J7
IC10
IC5
D1
R14
D2
J24
R12
IC18
C8
IC17
IC16
C7
IC19
C6
J5