


S2W SXM2

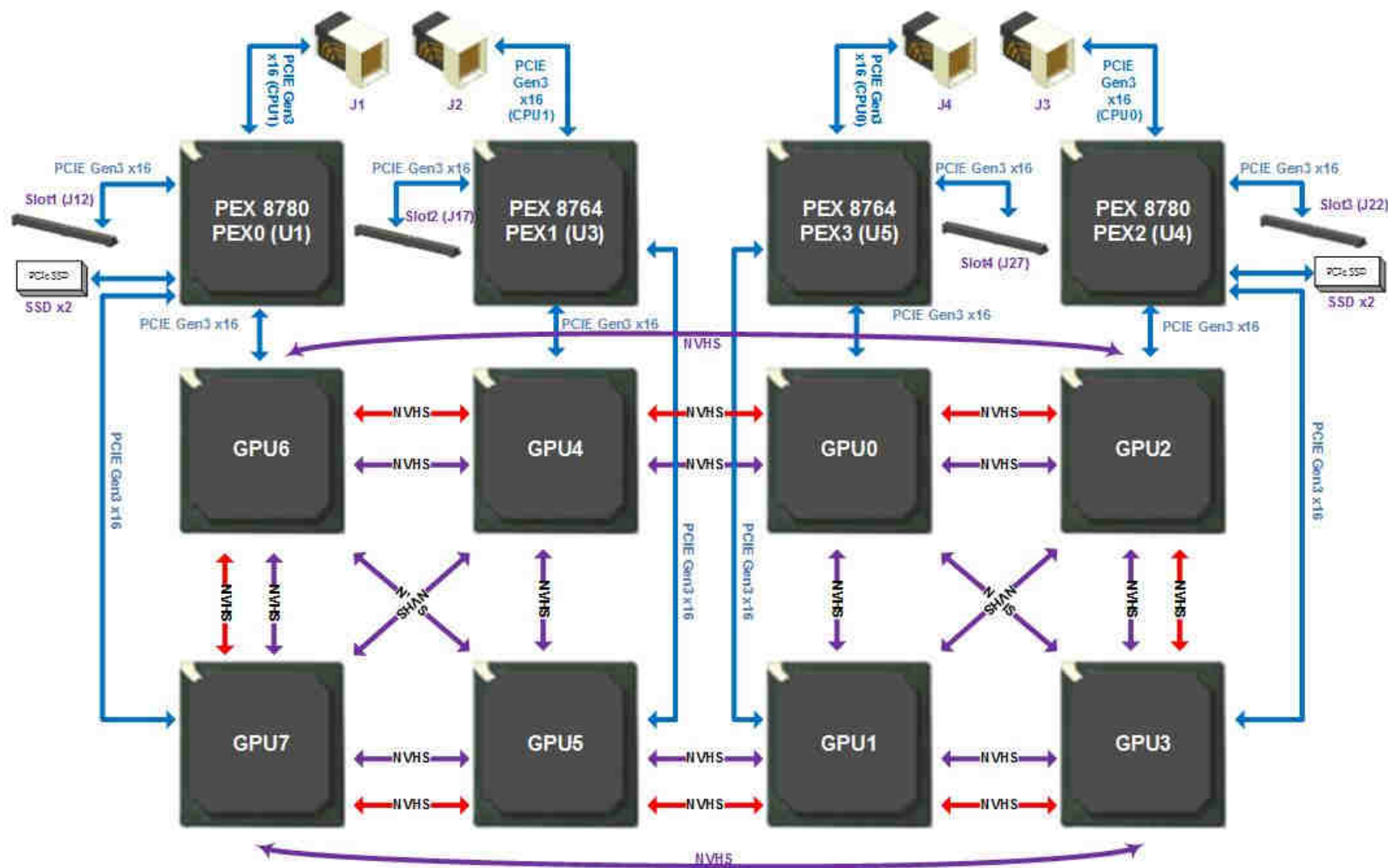
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	DEPARTMENT	DESIGNER	NAME	PROJECT	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	NAME	S2W	N/A	E
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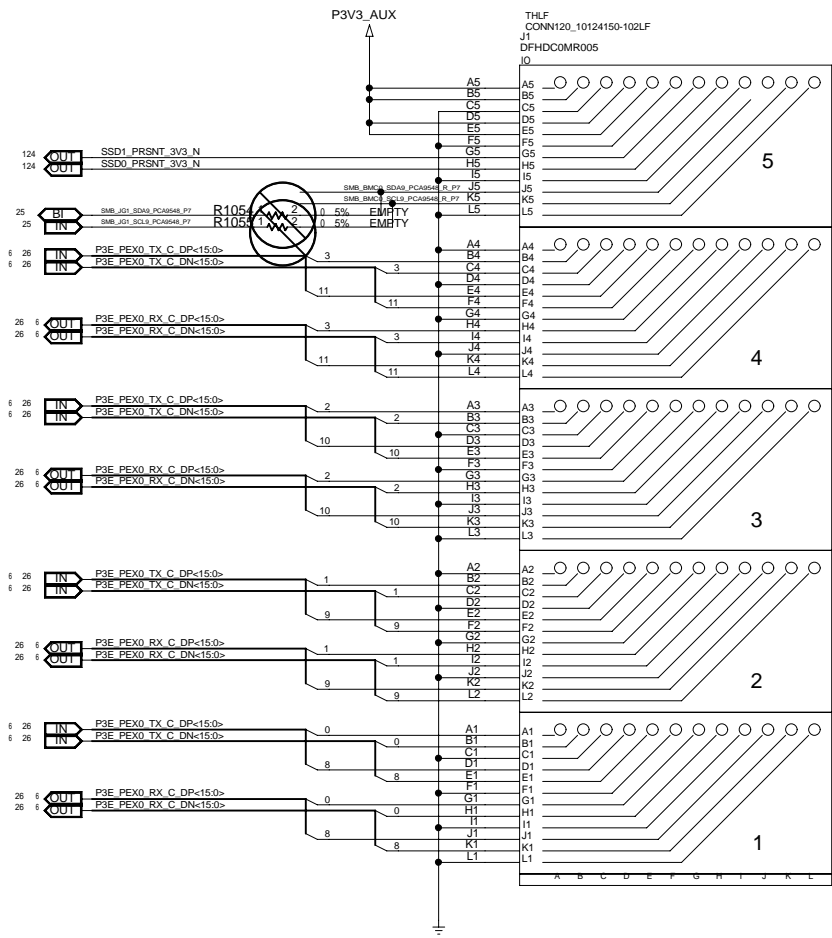
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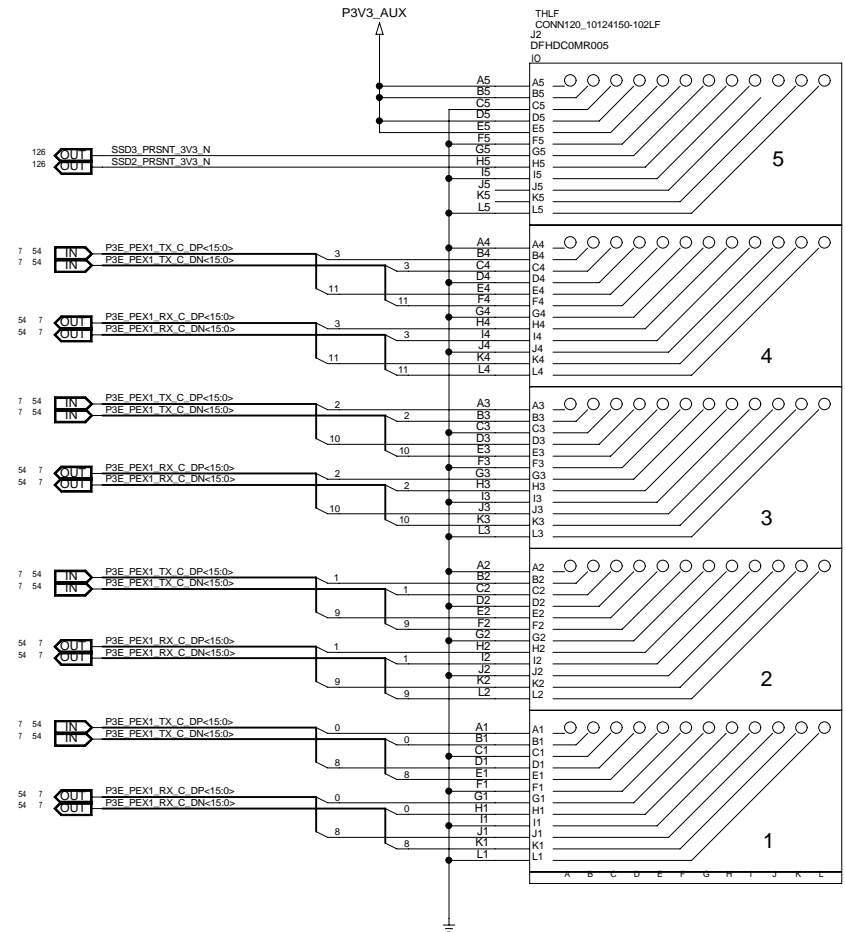
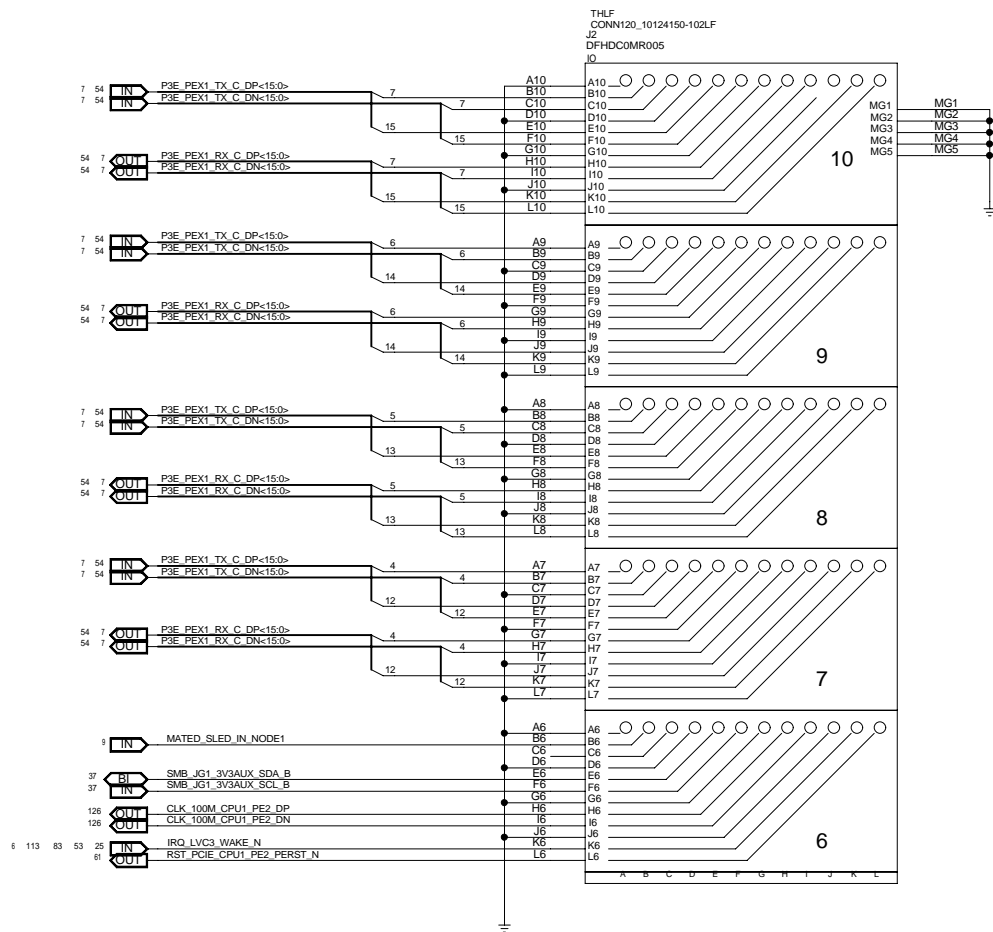
S2W SXM2 Block Diagram

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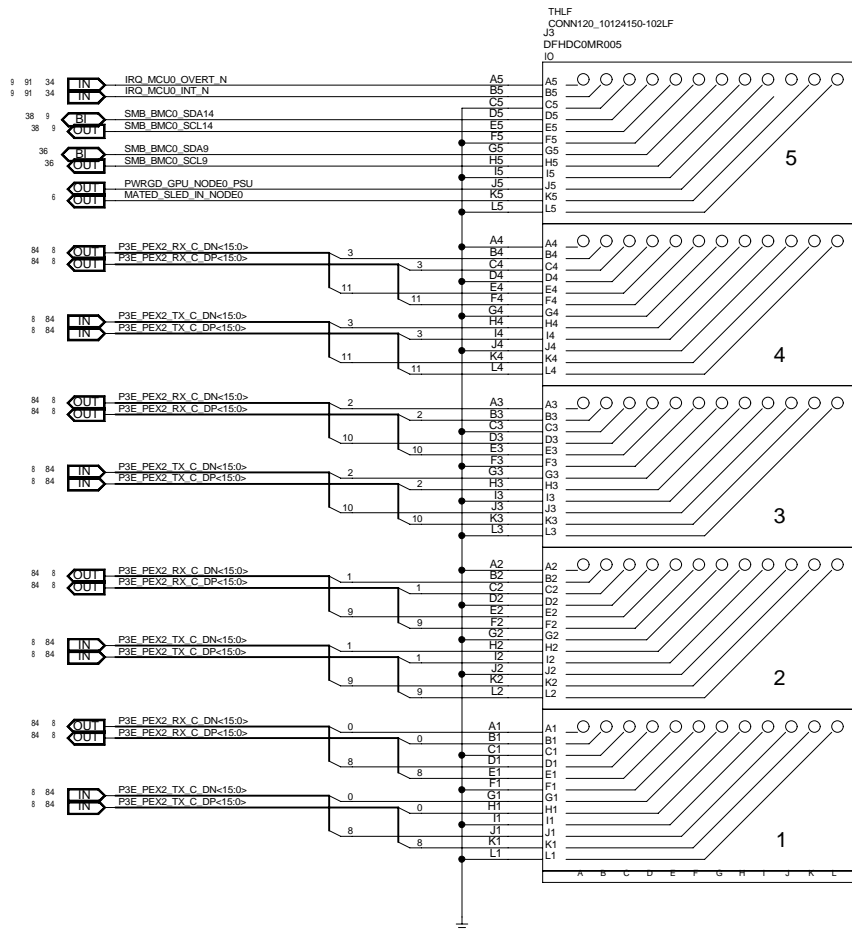
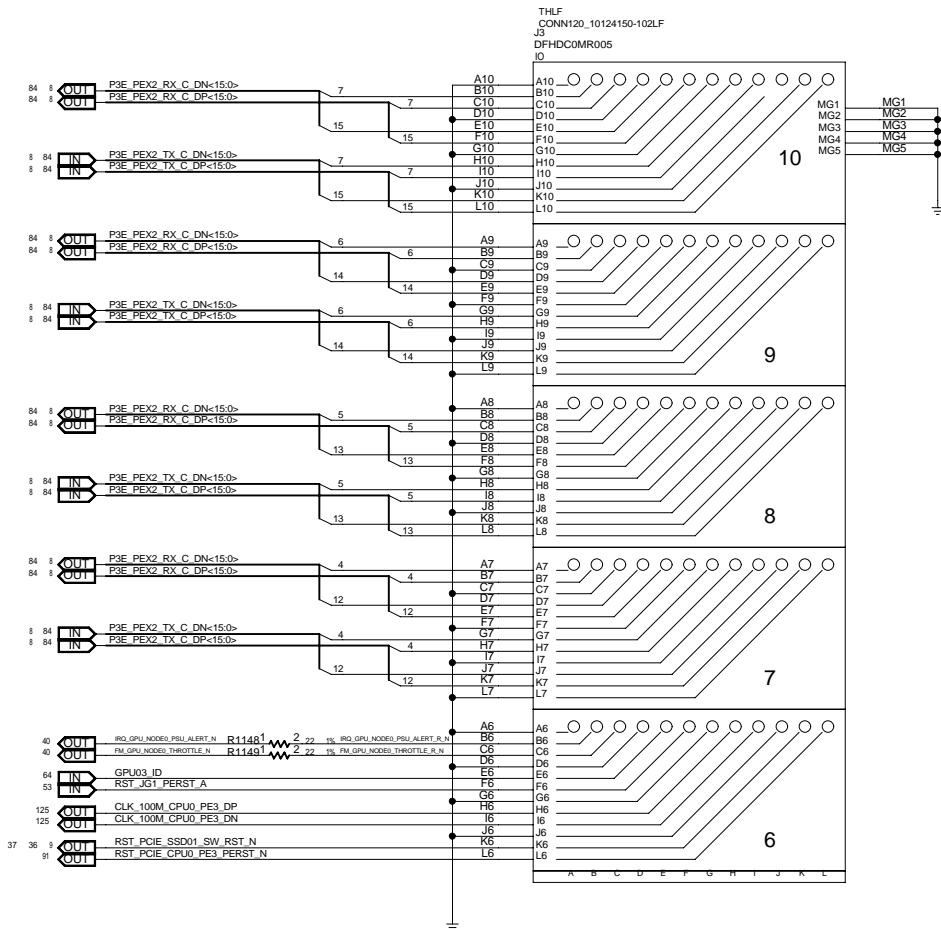
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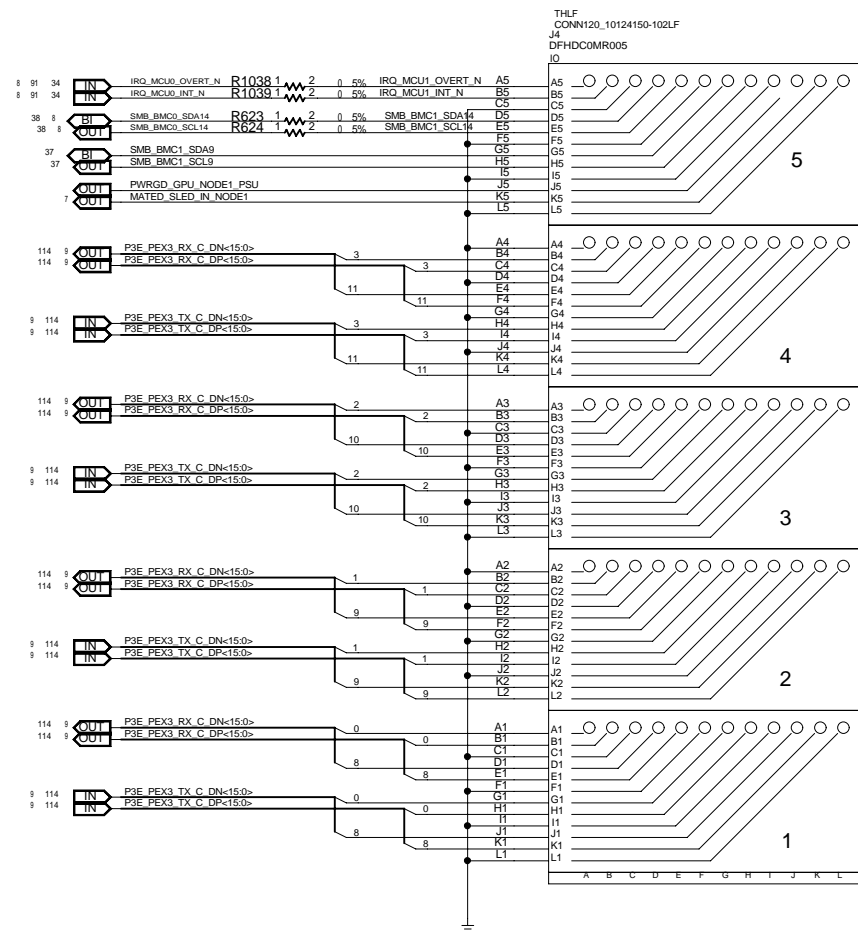
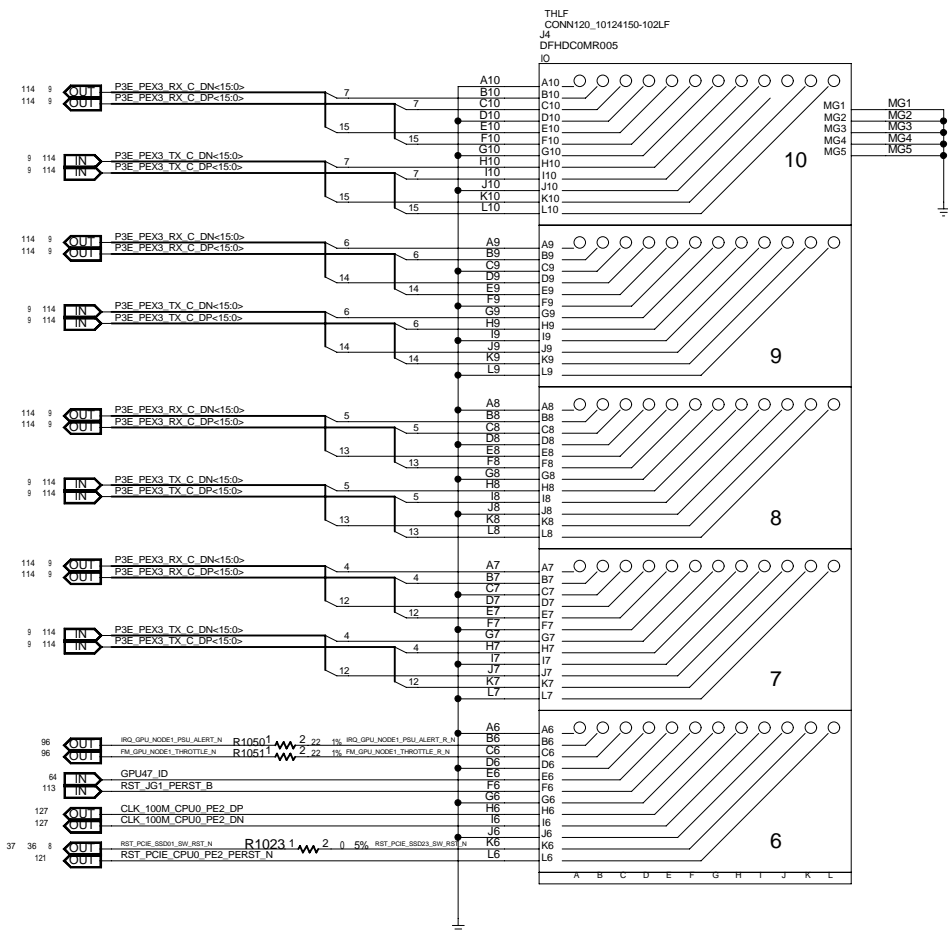
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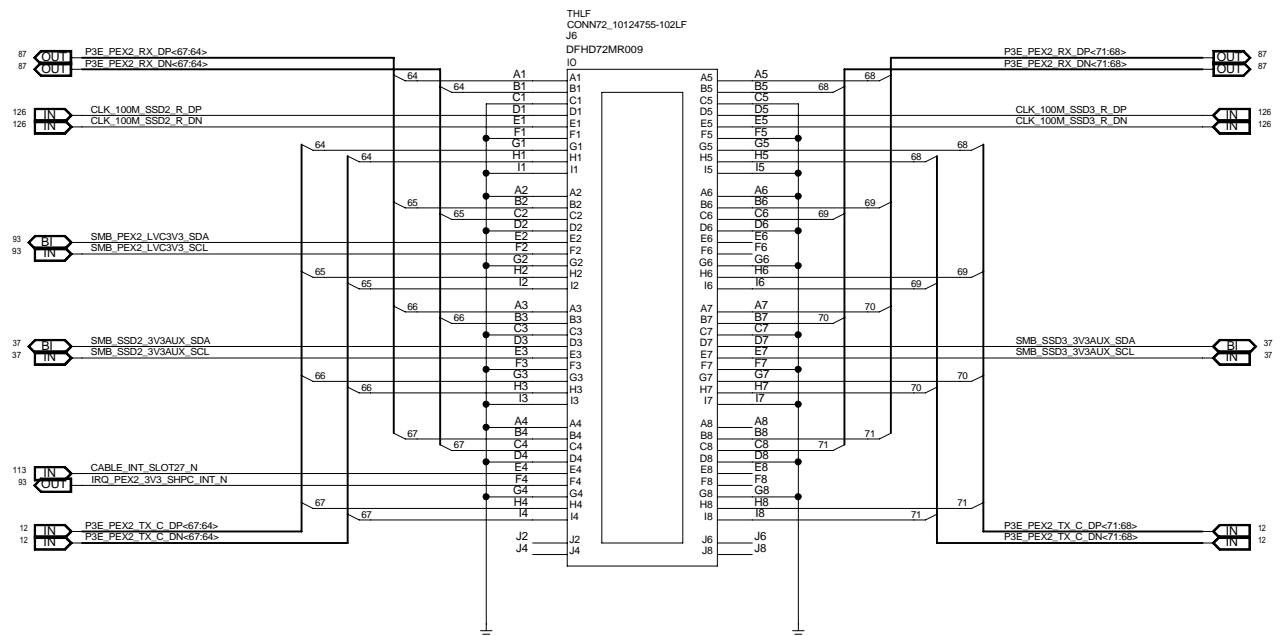
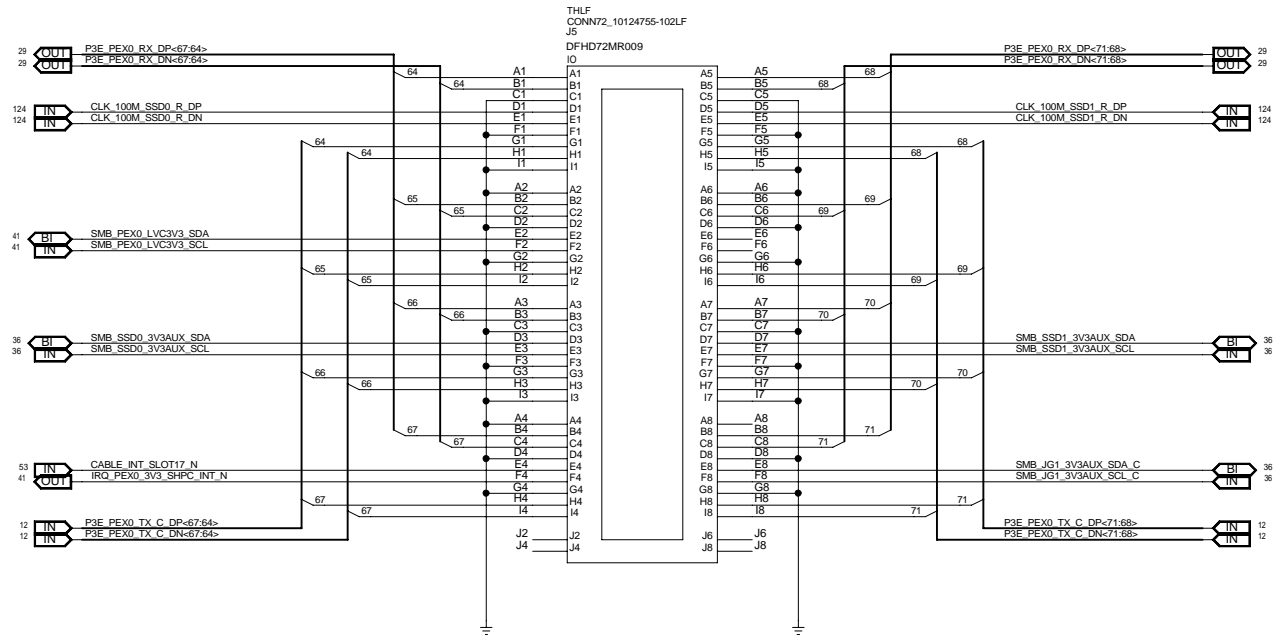


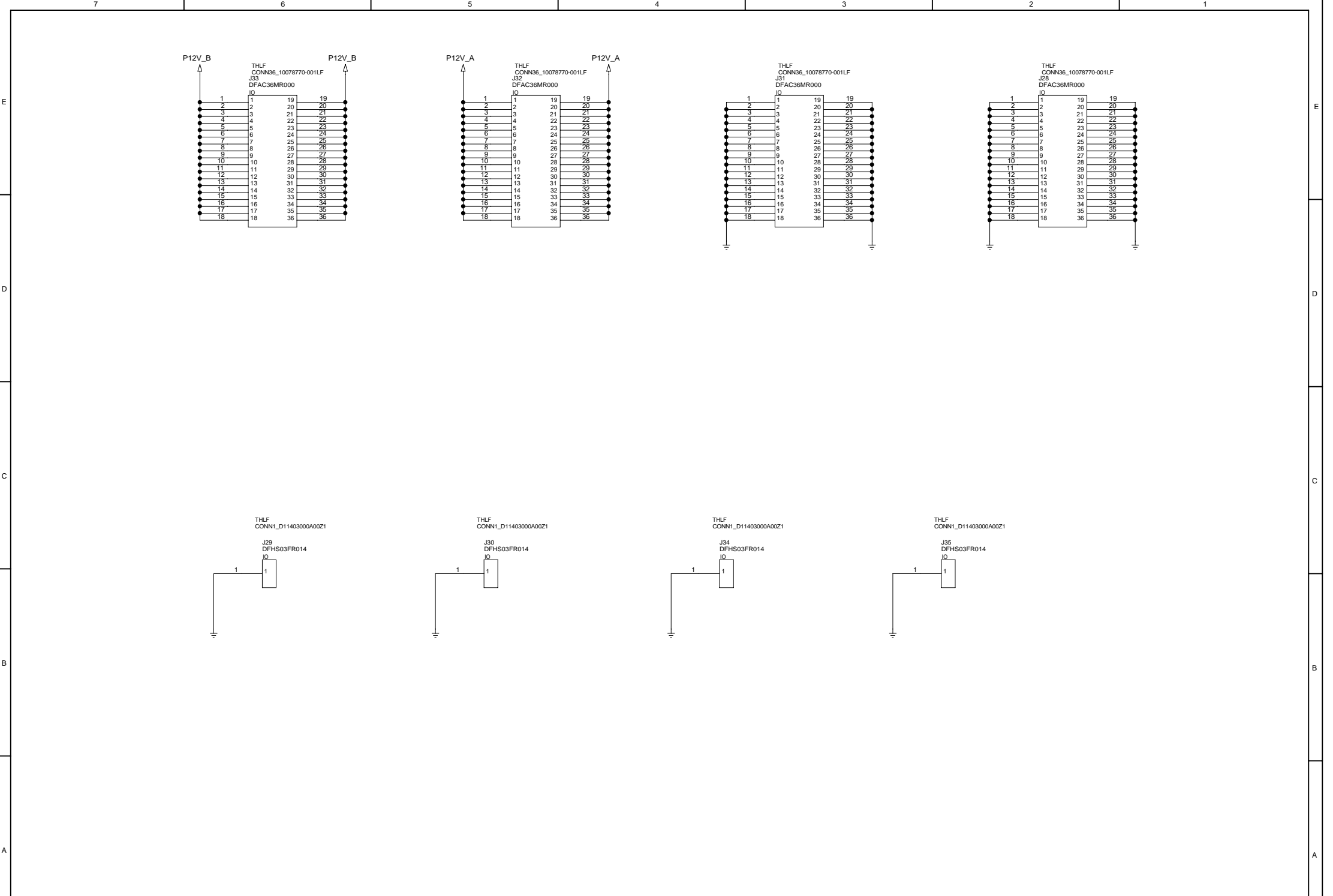
NODE0



NODE1







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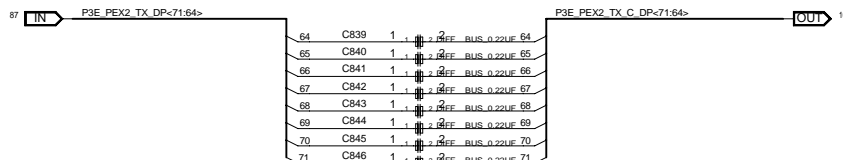
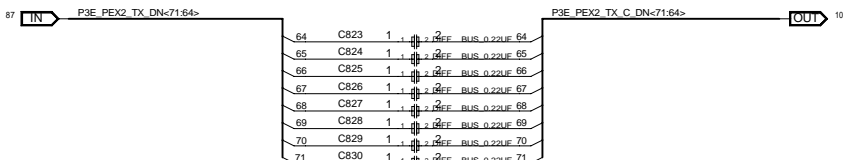
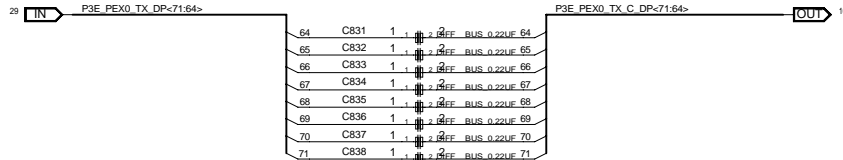
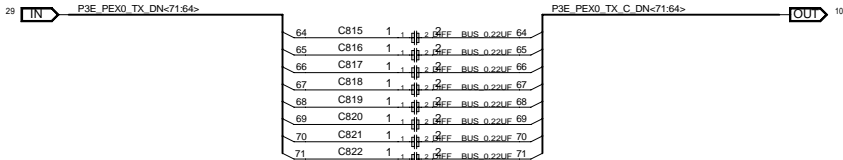
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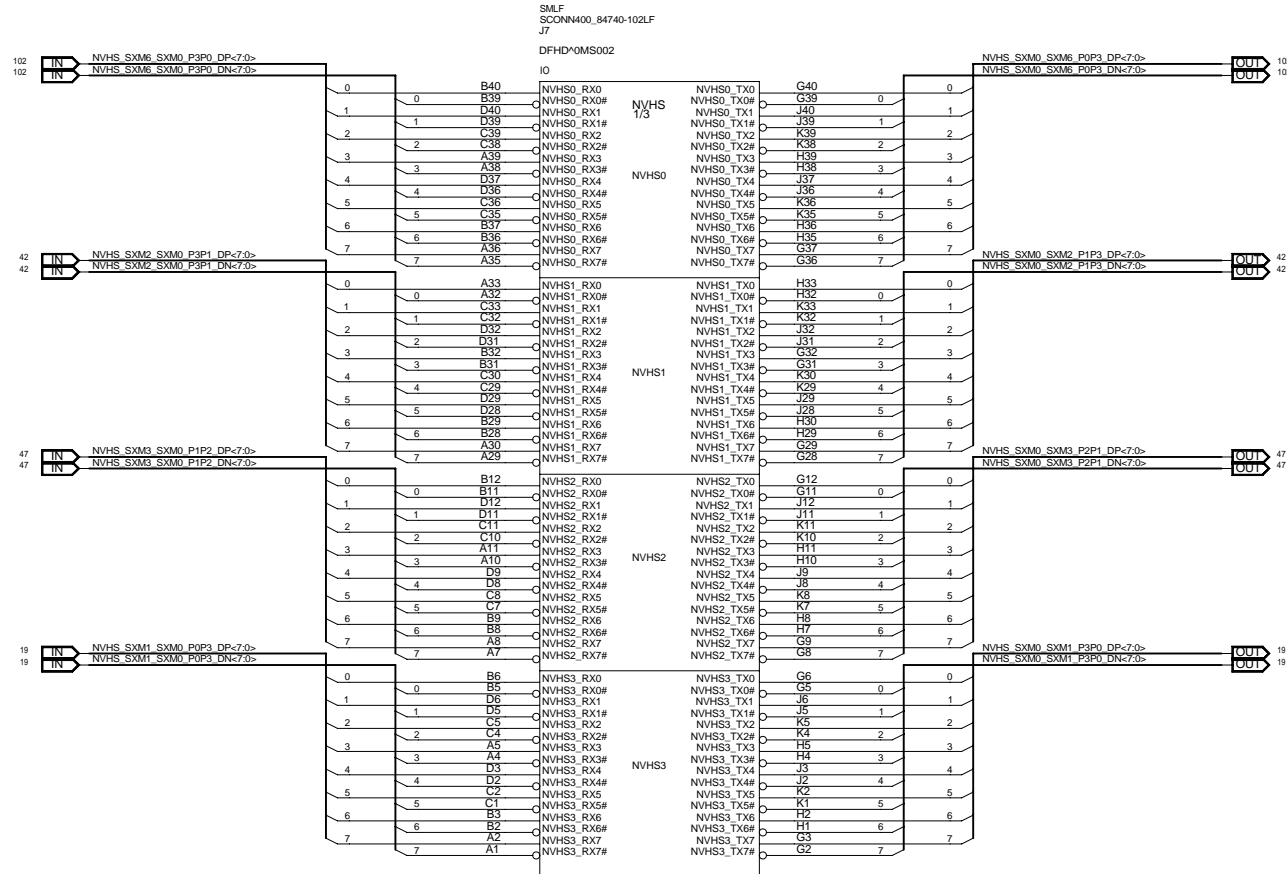
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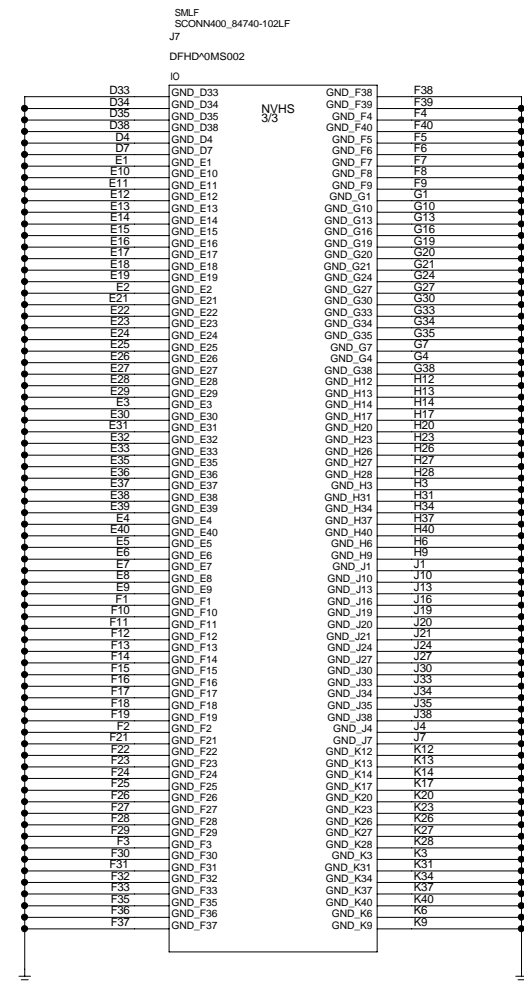
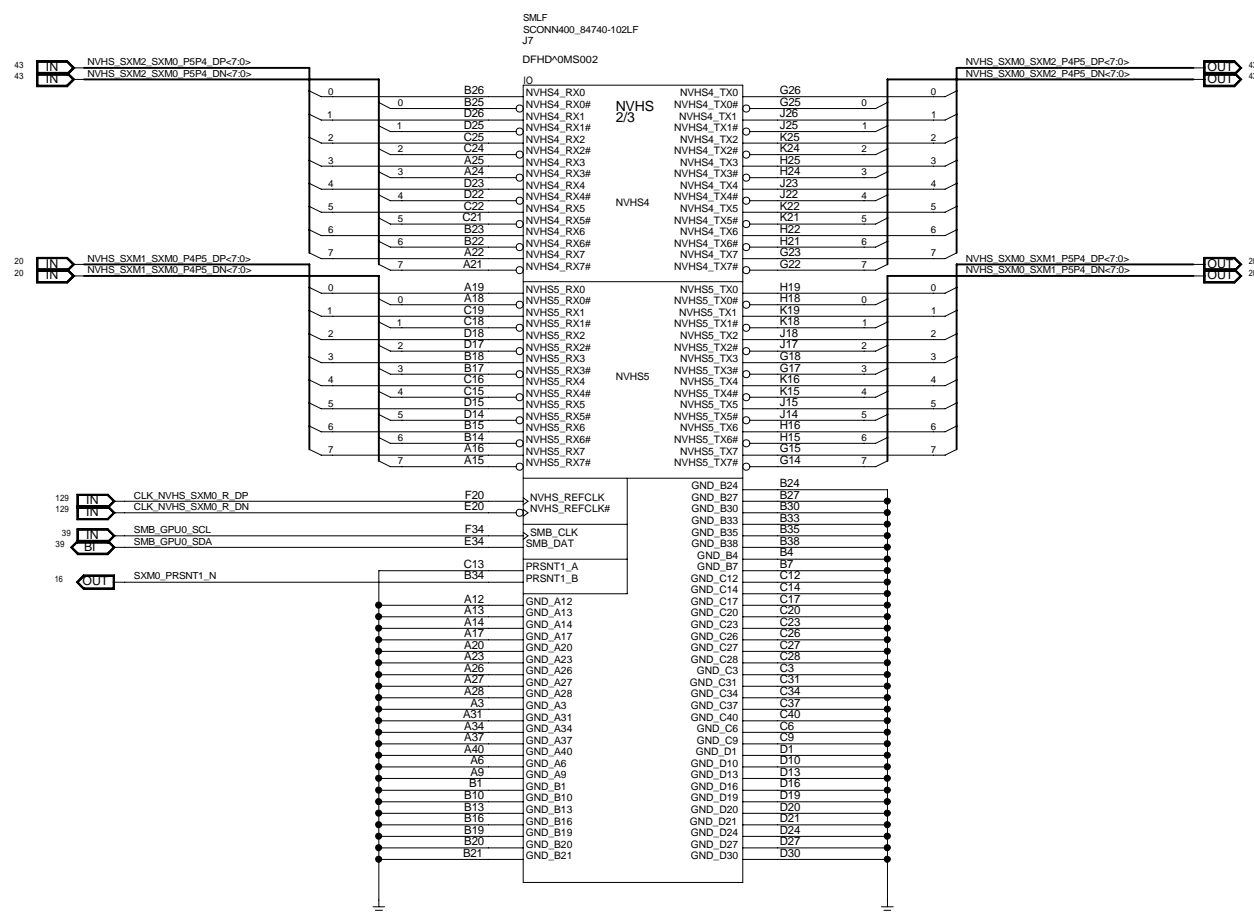
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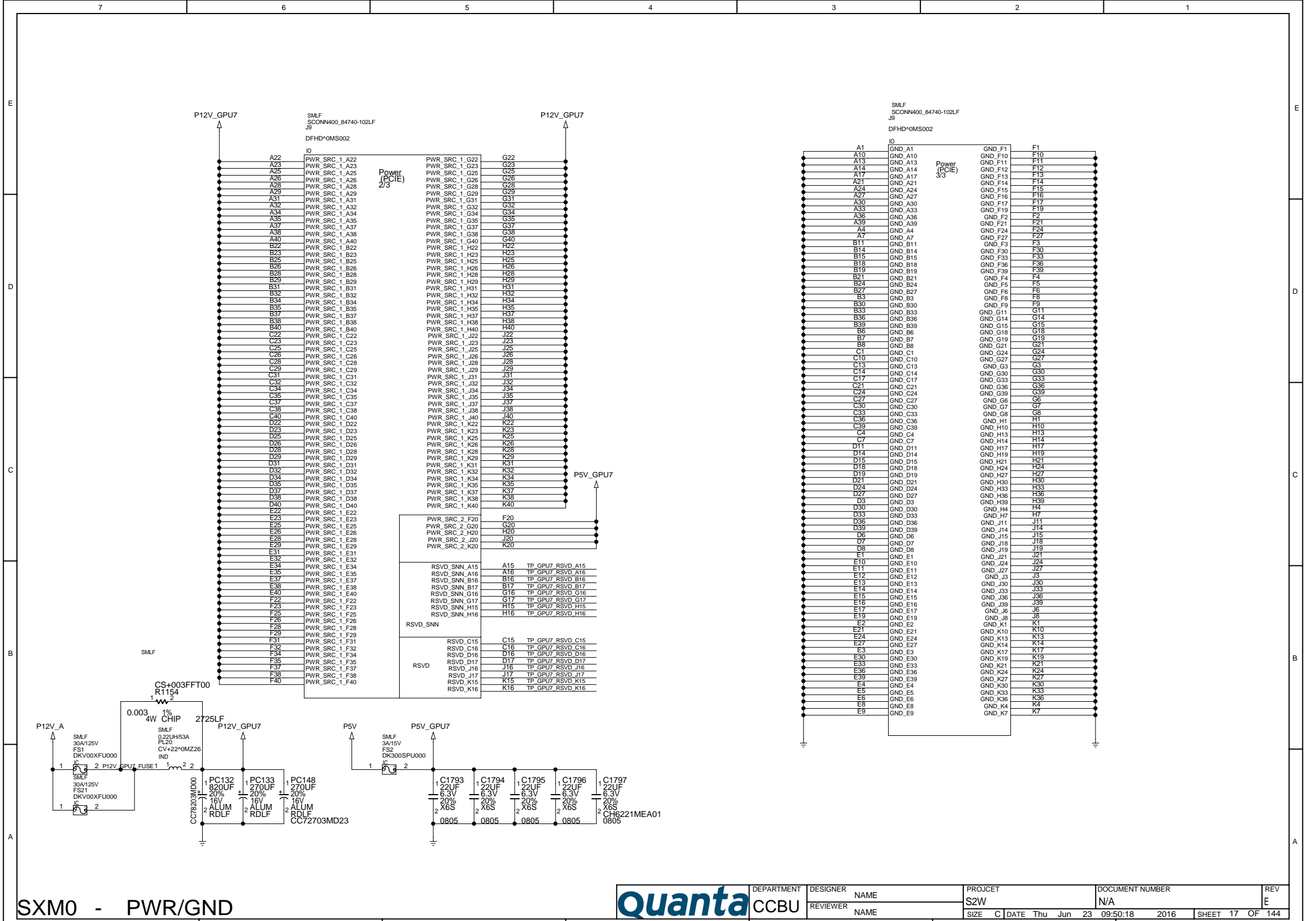
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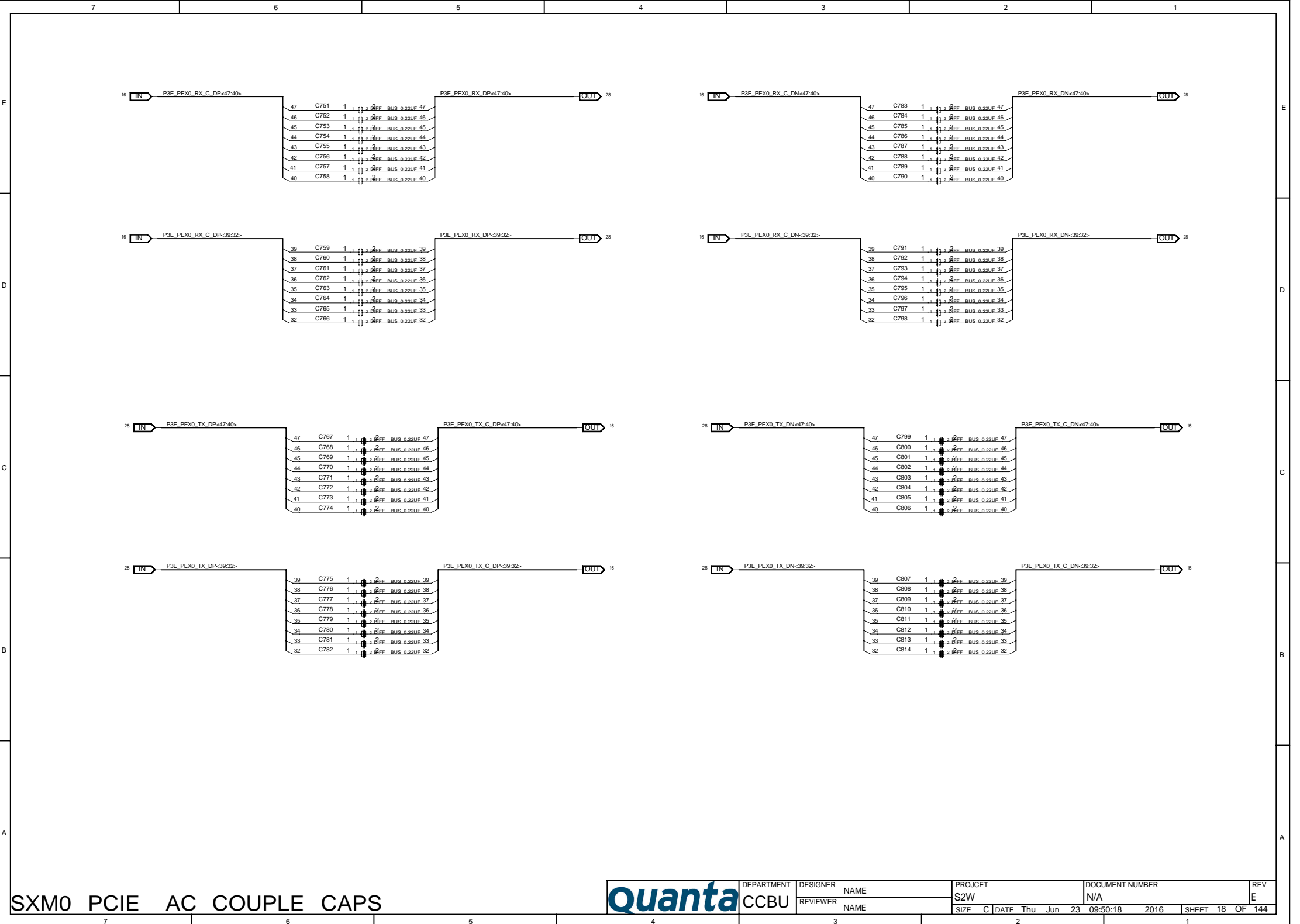
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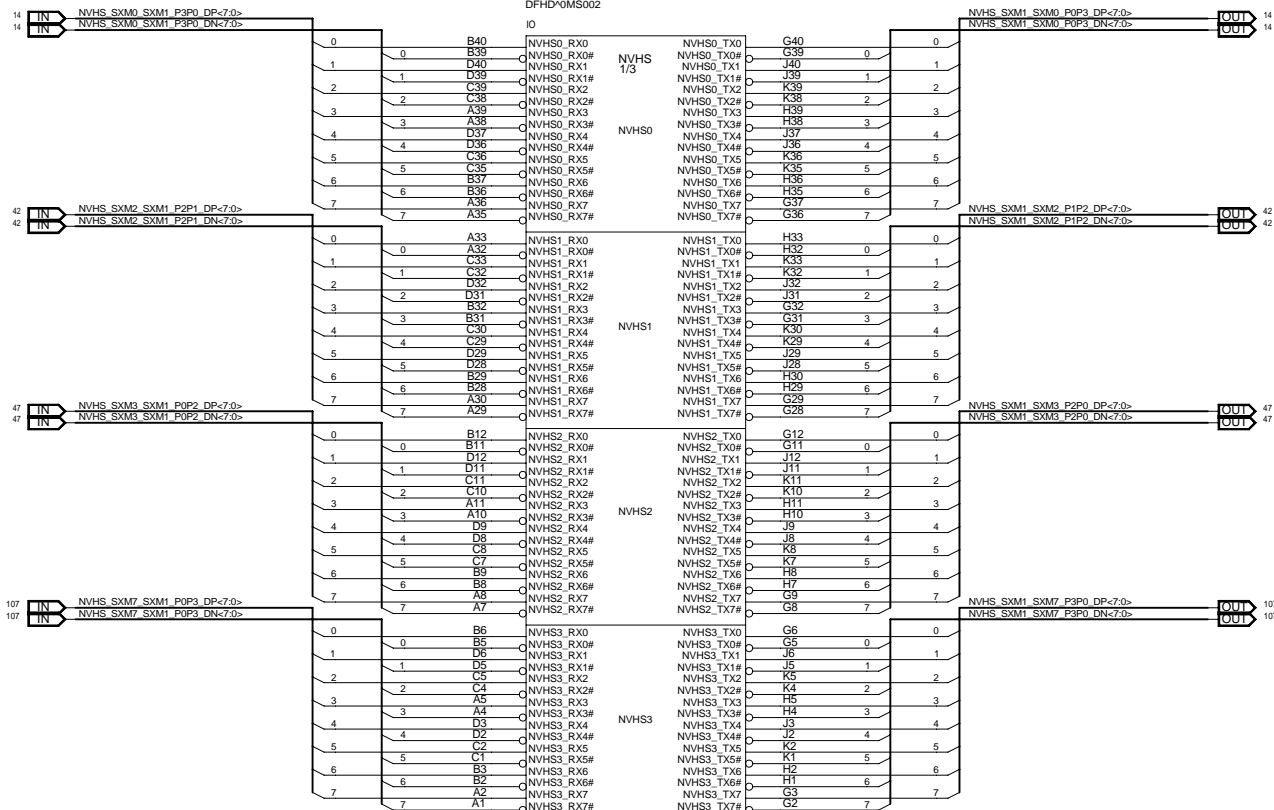
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SXM1 - NVLINK

SMLF
SCONN400_84740-102LF
J10

DFHD*OMS002

IO



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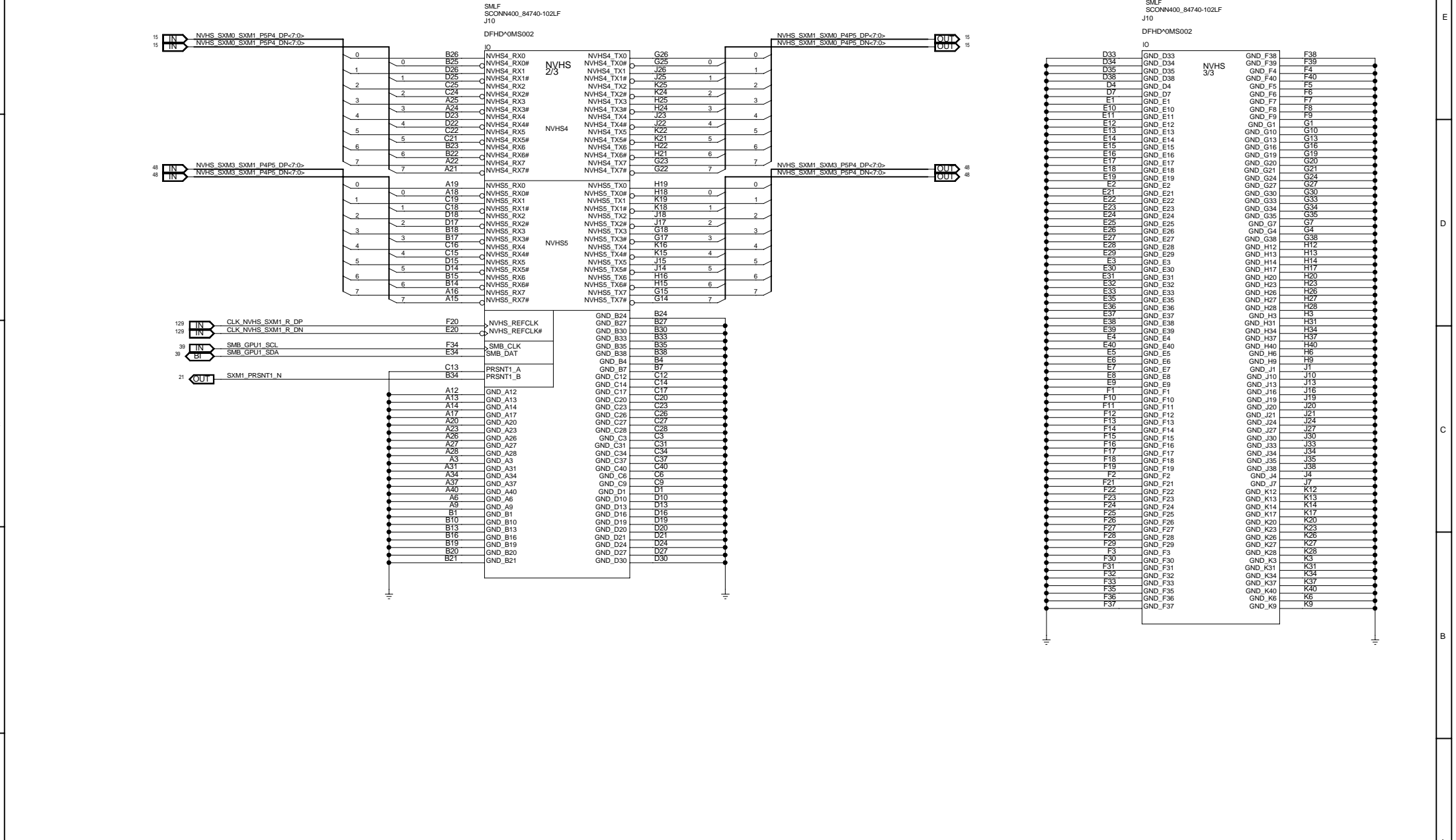
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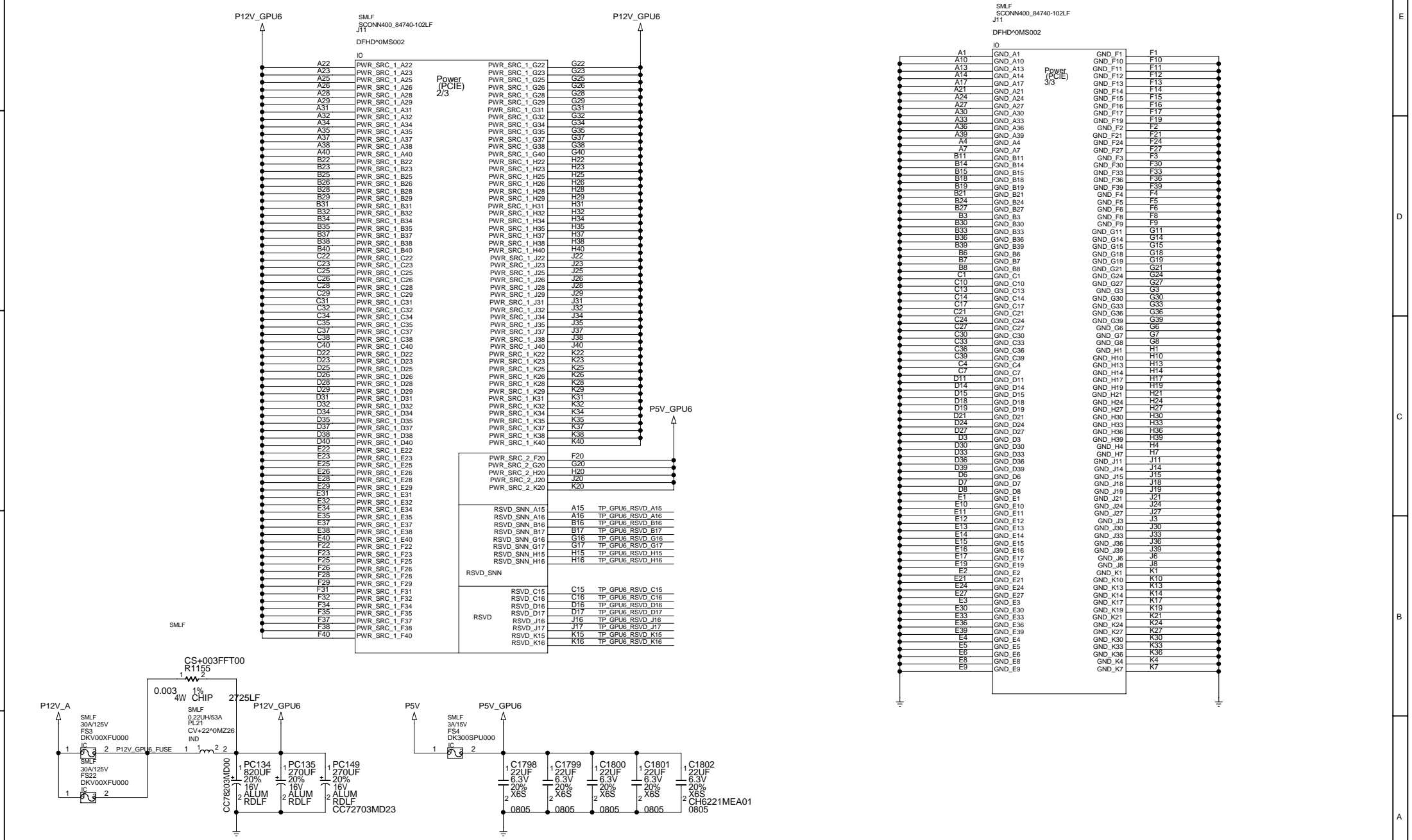
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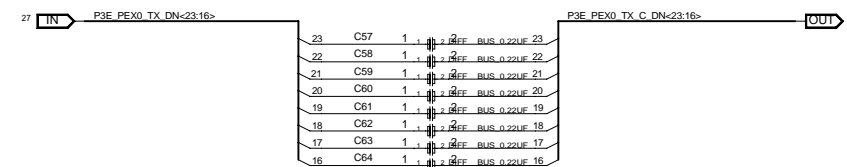
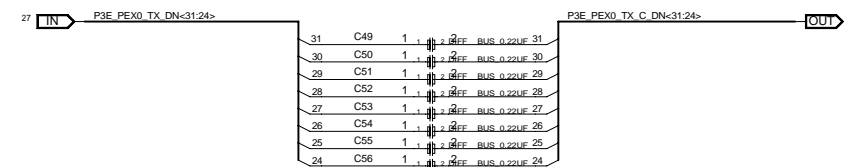
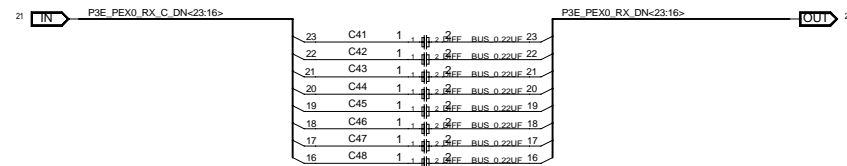
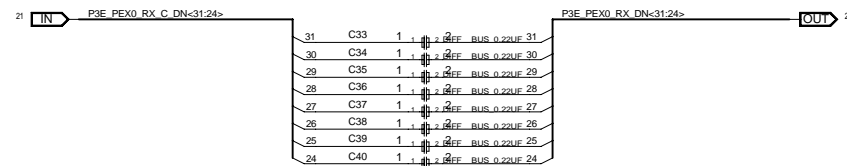
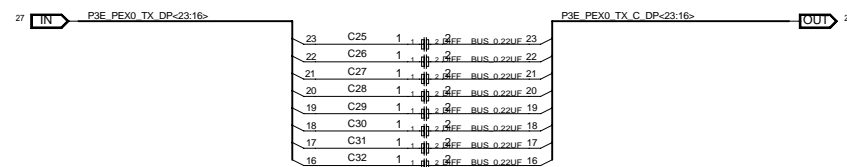
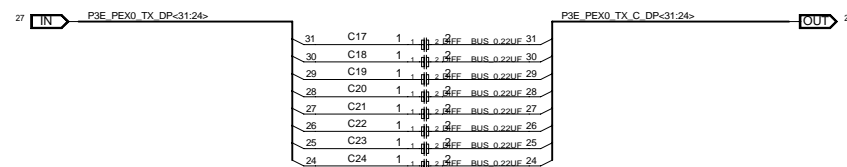
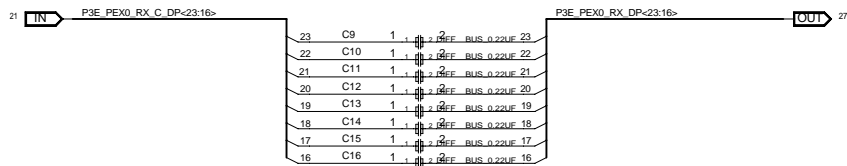
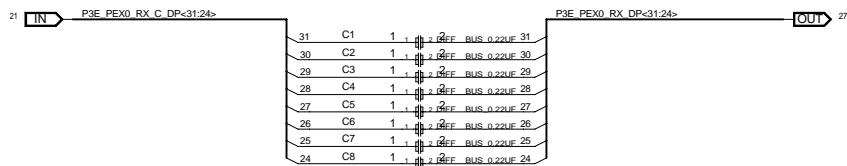
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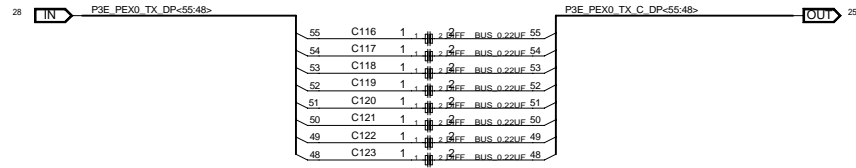
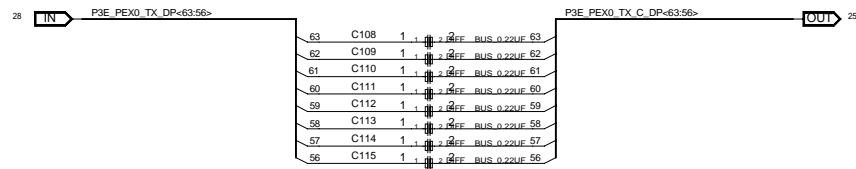
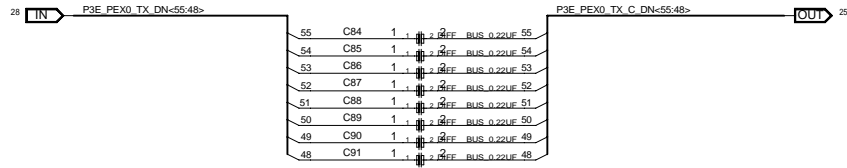
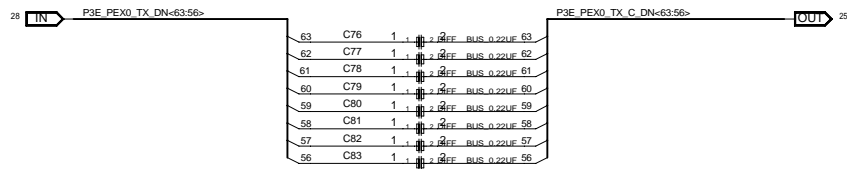
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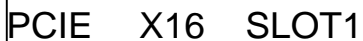
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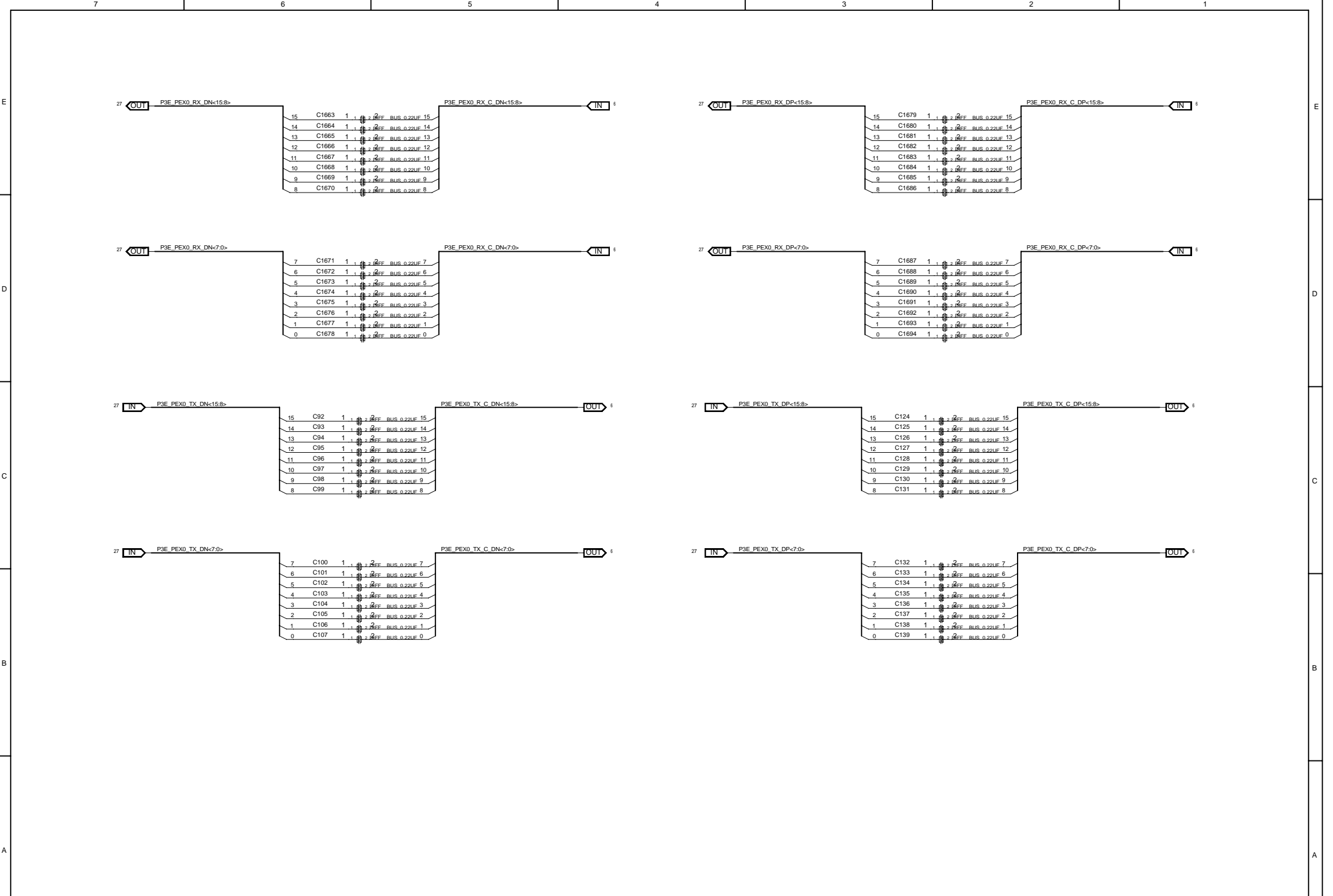
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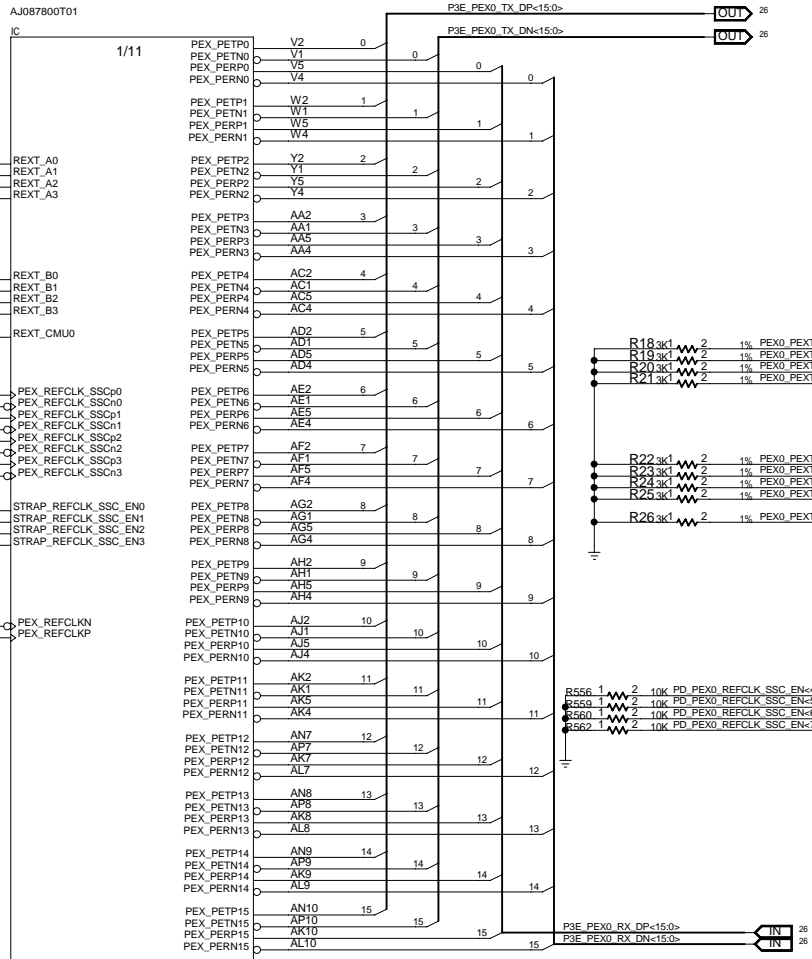
PEX0 TX/RX AC COUPLE CAPS



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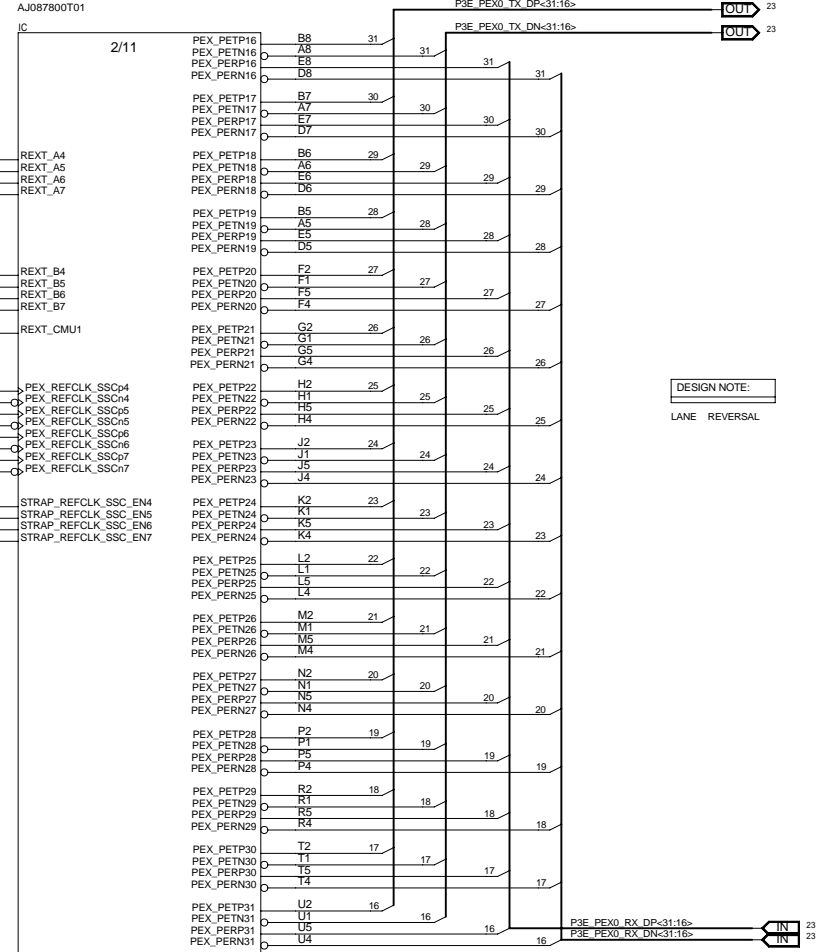
PLX TO CPU

SMLF
PEX8780-AB80BI G
U1
AJ087800T01



P3E_PEX0_TX_DP<15:0>
P3E_PEX0_TX_DN<15:0>

SMLF
PEX8780-AB80BI G
U1
AJ087800T01

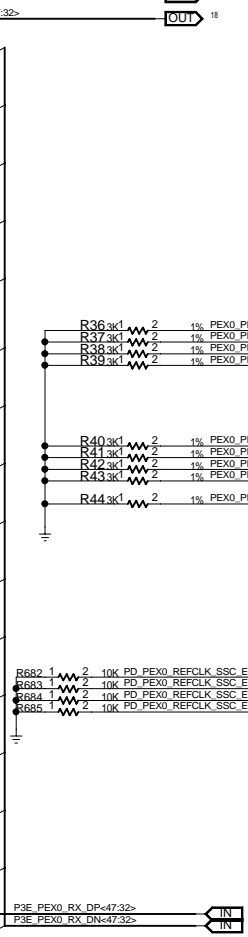
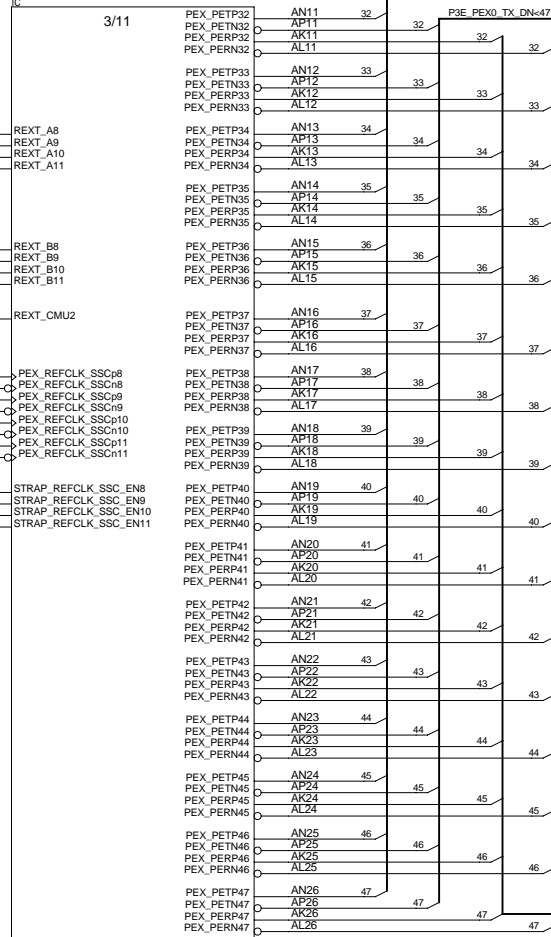


PLX TO GPU1

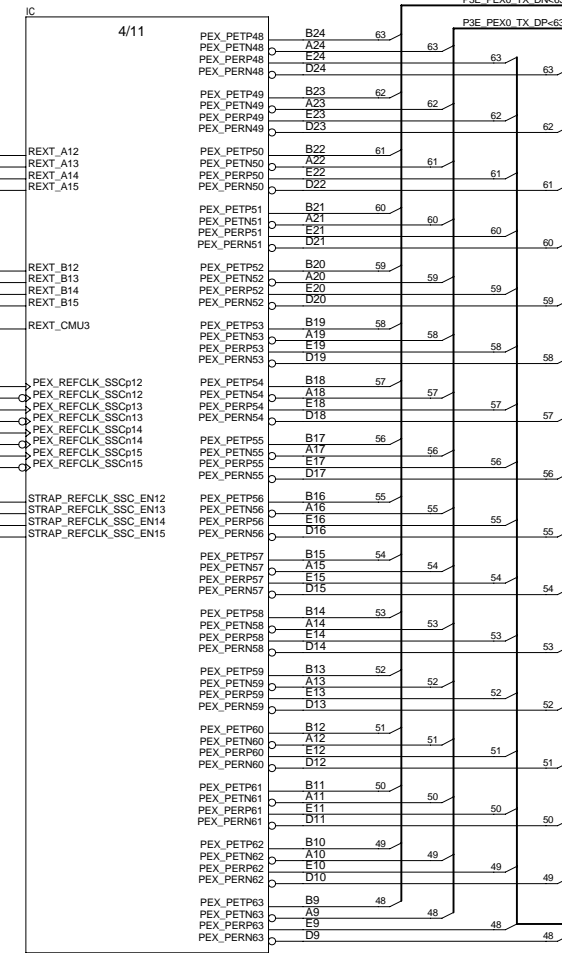
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LANE REVERSAL

PLX TO GPU0

SMLF
PEX8780-AB80BI
U1
AJ087800T01



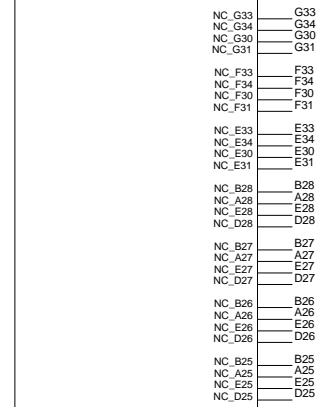
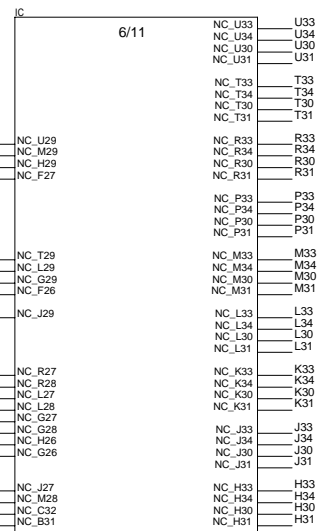
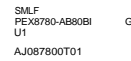
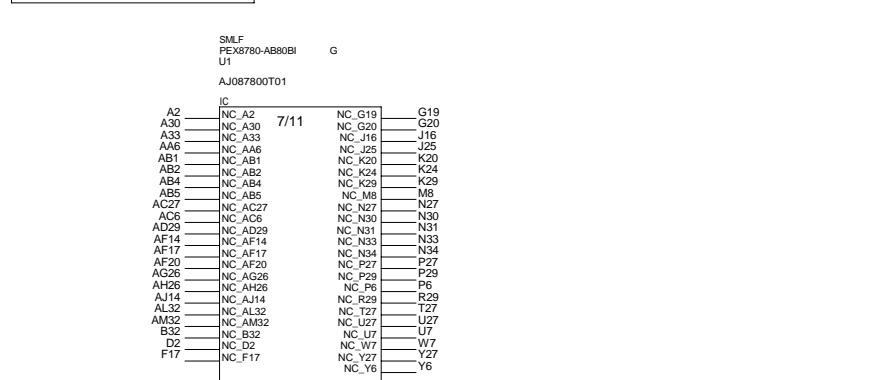
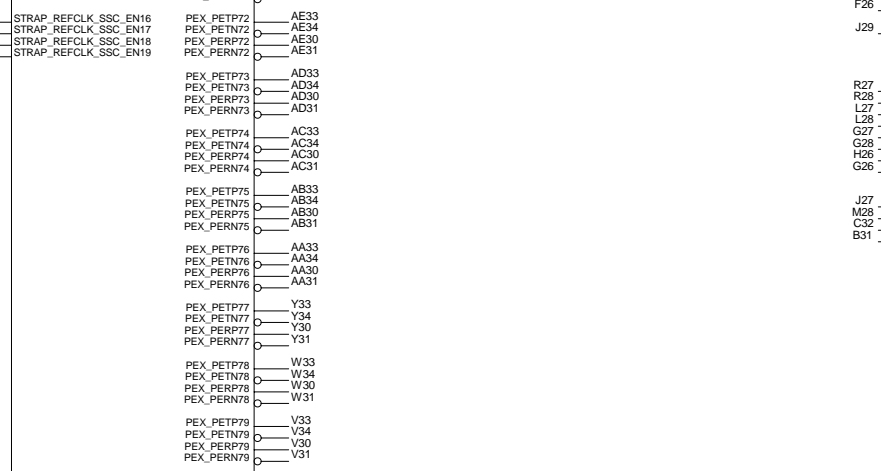
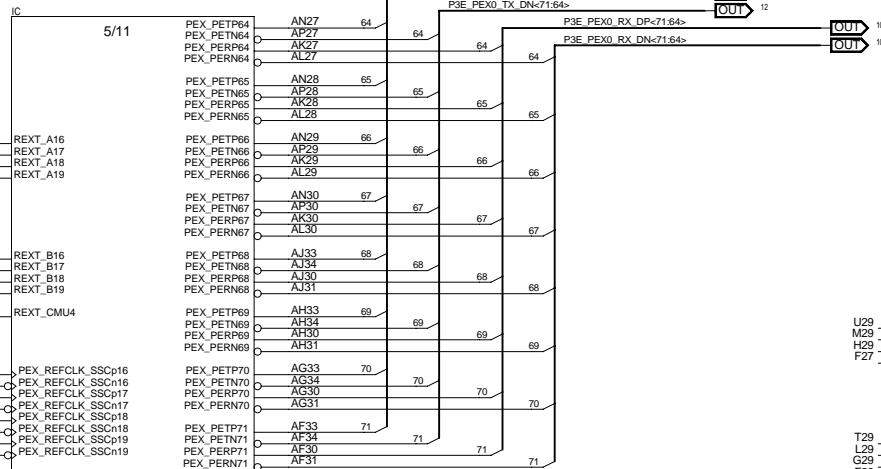
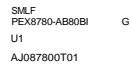
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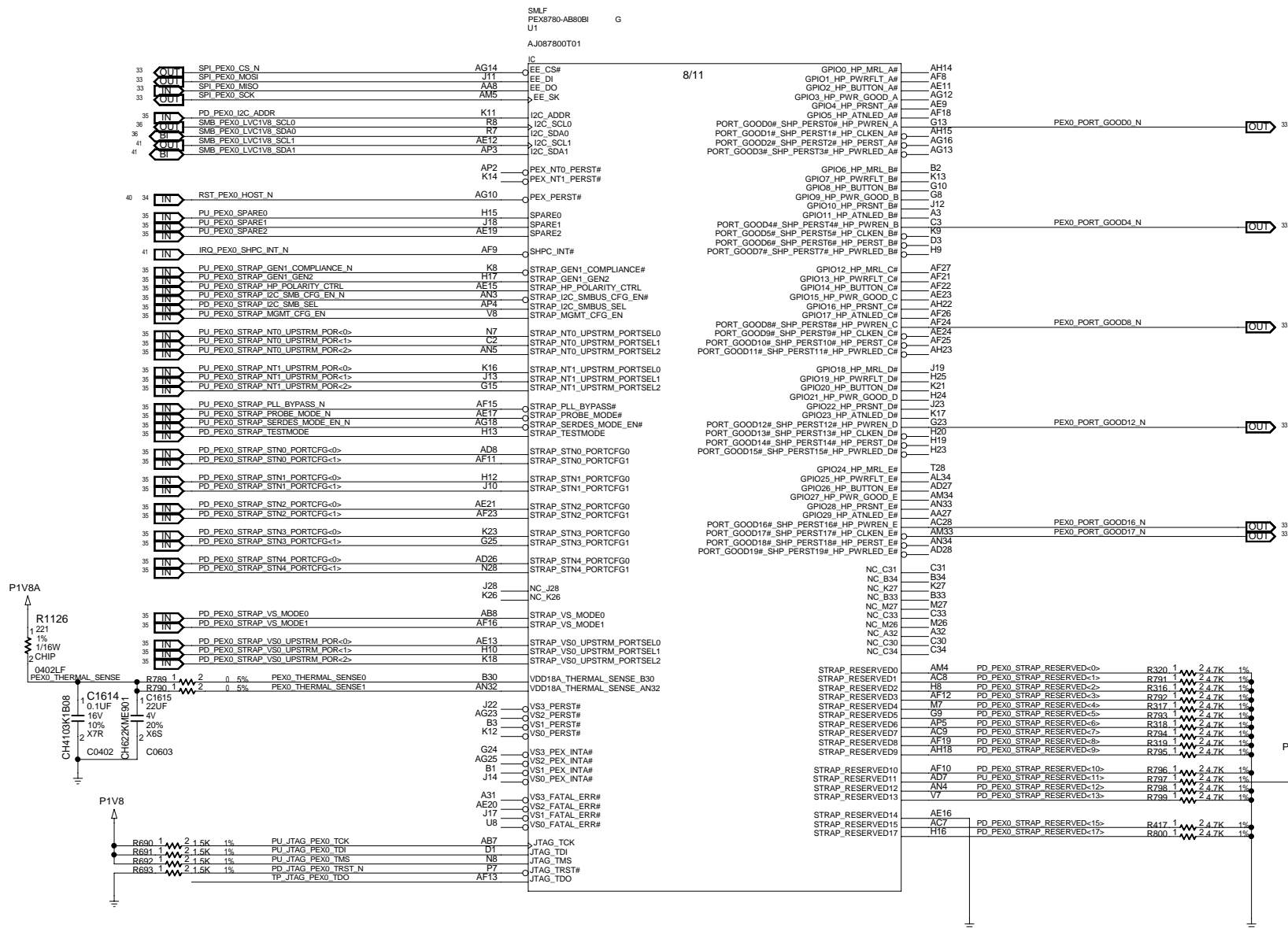


DESIGN NOTE:
POLARITY INVERSION
LANE REVERSAL

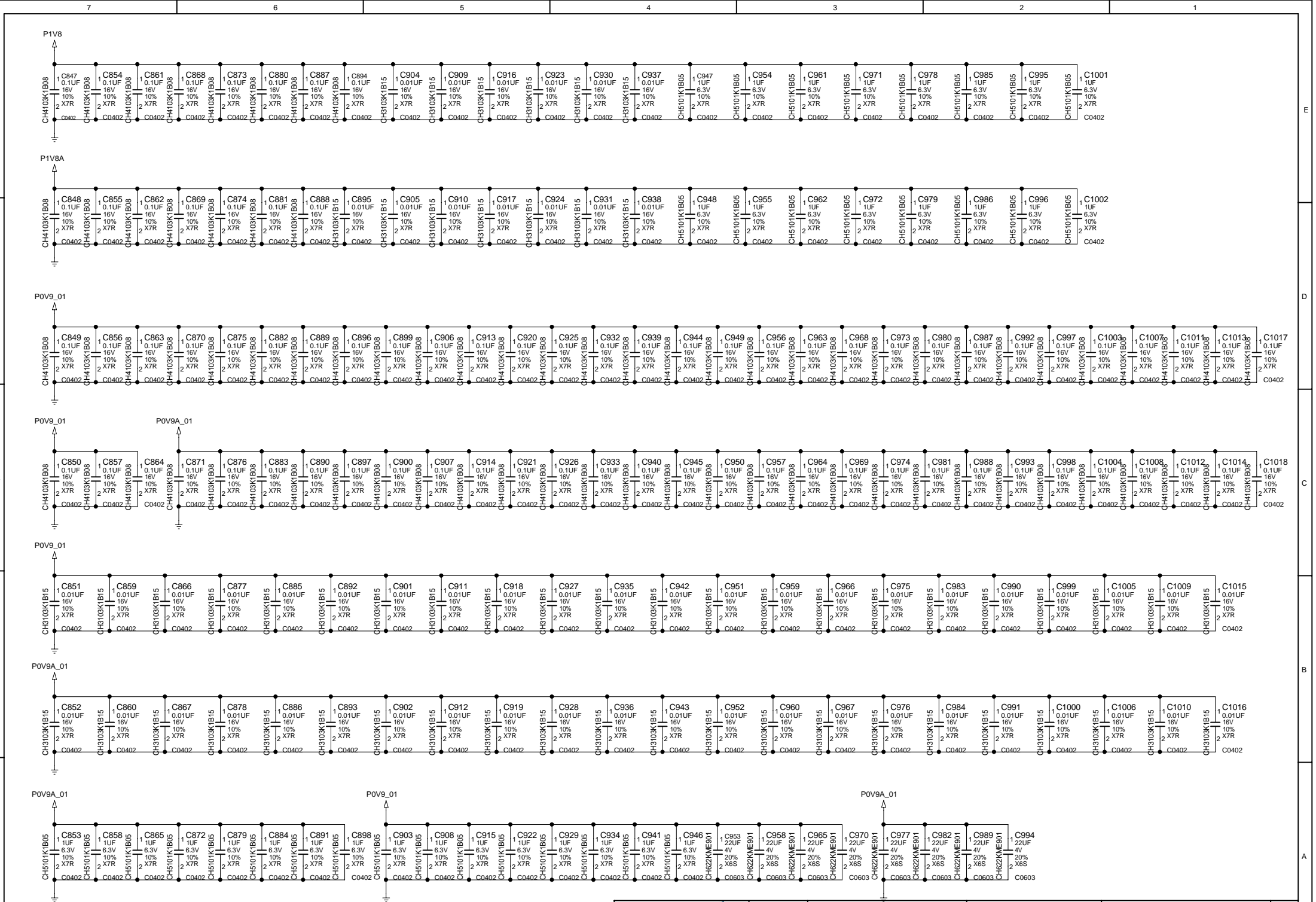
PLX TO SLOT1

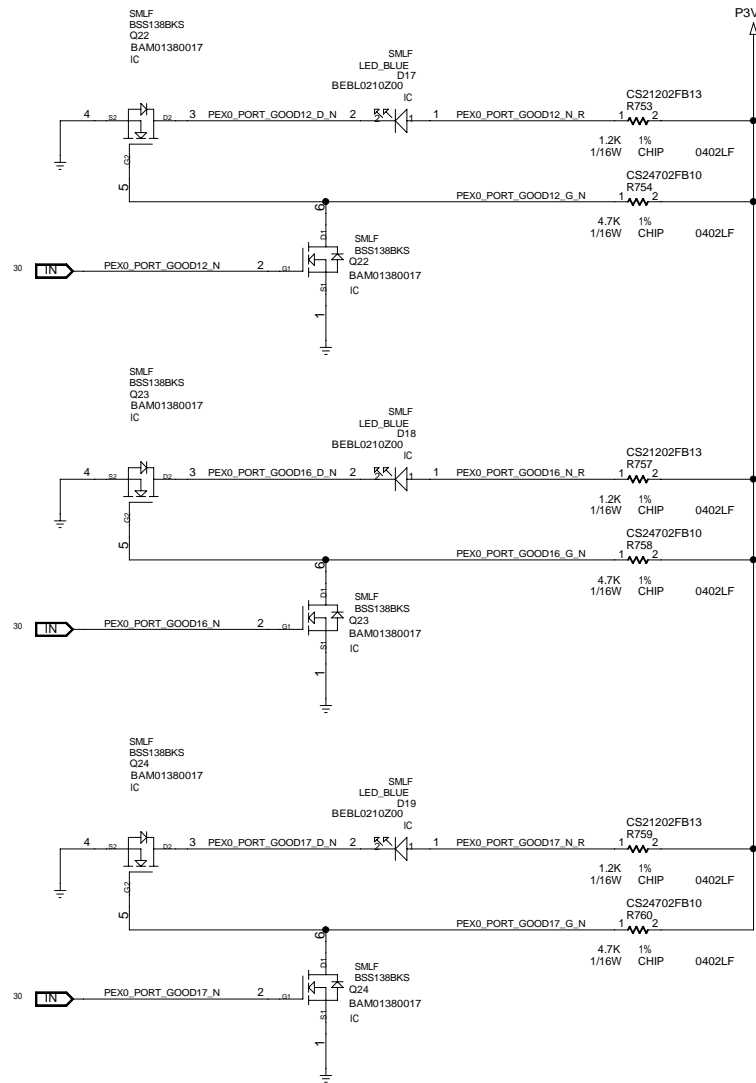
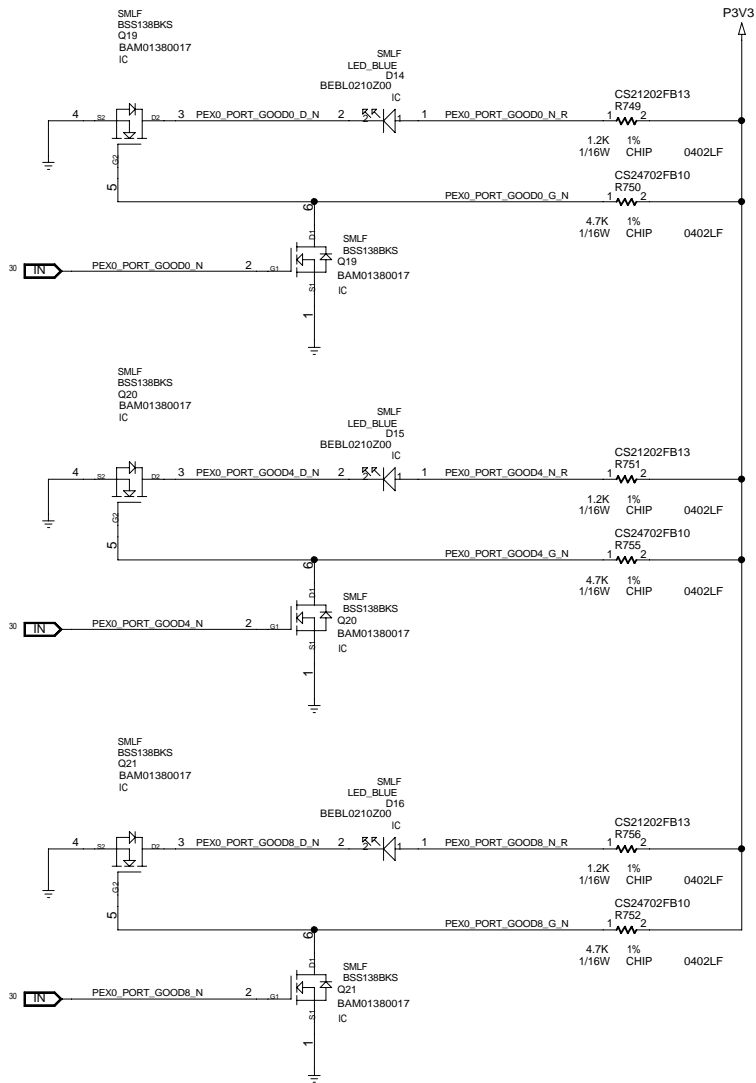
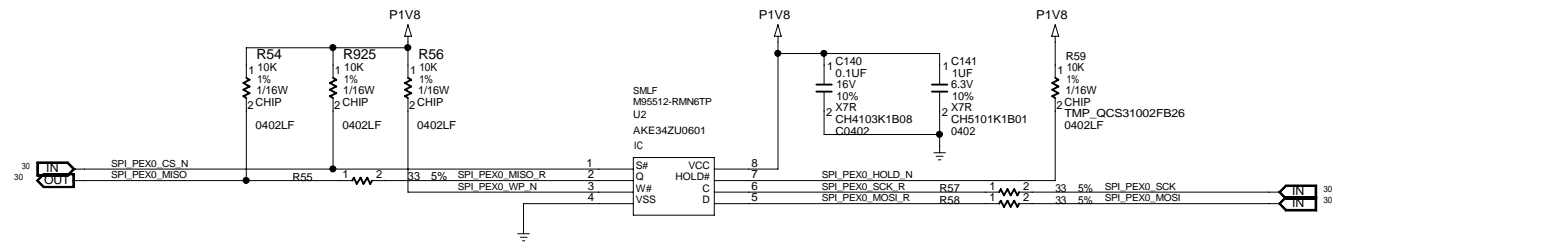
PLX TO SSD0/1











PEX0 EEPROM & PORT LED



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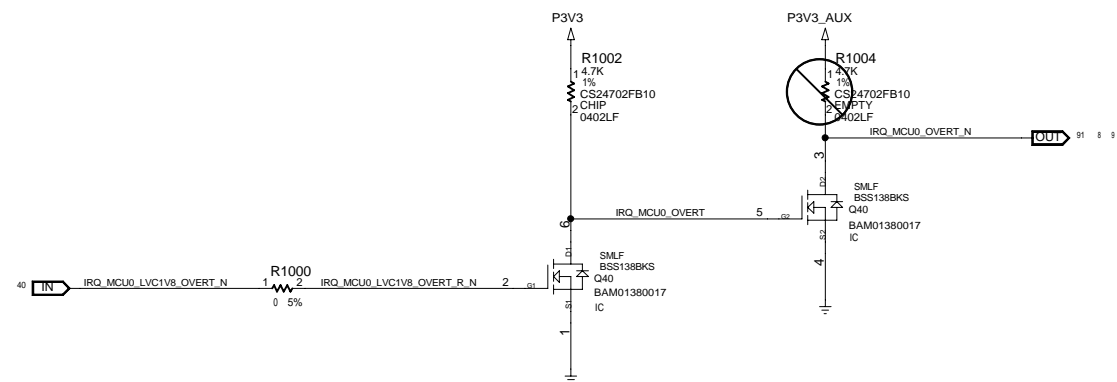
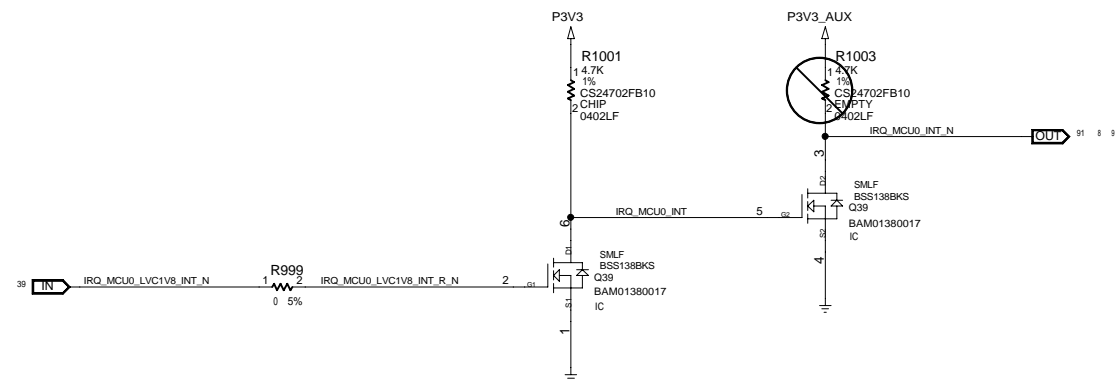
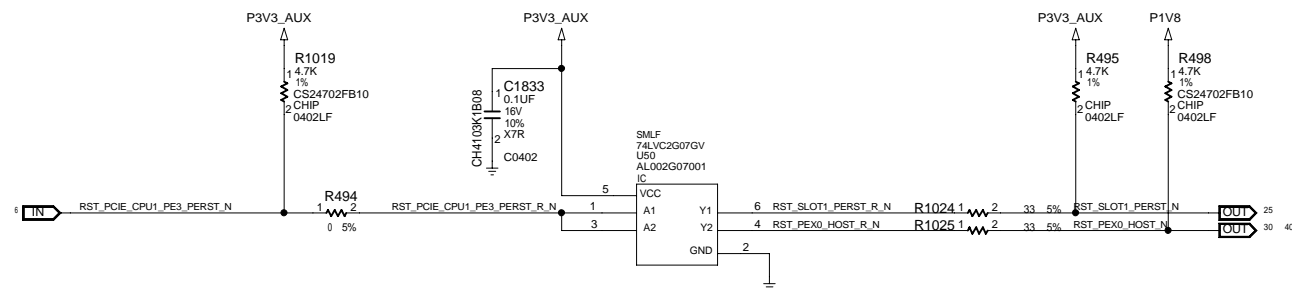
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PEX0 PERST & MCU0 INT LEVEL SHIFT



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R295 1 2 1K 1% PD_PEX0_STRAP_STN0_PORTCFG<1> OUT 3V

R296 1 2 1K 1% PD_PEX0_STRAP_STN0_PORTCFG<0> OUT 3V

EMPTY

R297 1 2 10K 1% PD_PEX0_STRAP_STN1_PORTCFG<1> OUT 30

R298 1 2 10K 1% PD_PEX0_STRAP_STN1_PORTCFG<0> OUT 30

EMPTY

The diagram shows two pins, PD_PEX0_STRAP_STN3_PORTCFG<1> and PD_PEX0_STRAP_STN3_PORTCFG<0>, both configured as outputs (OUT). They are connected to a common node through 10K resistors (R301 and R302). The node is also connected to ground. The resistors are labeled with a value of 10K and a tolerance of 1%.

R3791 2 10K 1% PD_PEX0_STRAP_VSD0 UPSTREAM_POR<0>
 R3801 2 10K 1% PD_PEX0_STRAP_VSD1 UPSTREAM_POR<1>
 R3811 2 10K 1% PD_PEX0_STRAP_VSD2 UPSTREAM_POR<2>

1=PCIE MAX DATA RATE =GEN3
1=MANAGEMENT PORT IS DISABLED

Resistor	Value	Tolerance	Signal Name	Output Pin	Pin Number
R801	10K	1%	PU_PEX0_STRAP_GEN1_COMPLIANCE_N	OUT	30
R311	10K	1%	PU_PEX0_STRAP_GEN1_GEN2	OUT	30
R382	10K	1%	PU_PEX0_STRAP_MGMT_CFG_EN	OUT	30
R802	10K	1%	PU_PEX0_STRAP_HP_POLARITY_CTRL	OUT	30

R3831 2 10K 1% PD_PEX0_STRAP_I2C_SMB_SEL OUT 30

P1V8

R305 1 2 10K 1% PU_PEX0_STRAP NT0_UPSTRM_POR<0> OUT 30

R306 1 2 10K 1% PU_PEX0_STRAP NT0_UPSTRM_POR<1> OUT 30

R307 1 2 10K 1% PU_PEX0_STRAP NT0_UPSTRM_POR<2> OUT 30

R308 1 2 10K 1% PU_PEX0_STRAP NT1_UPSTRM_POR<0> OUT 30

R309 1 2 10K 1% PU_PEX0_STRAP NT1_UPSTRM_POR<1> OUT 30

R310 1 2 10K 1% PU_PEX0_STRAP NT1_UPSTRM_POR<2> OUT 30

R3871 2 10K 1% PD_PEX0_STRAP_TESTMODE OUT 3

R418 1 2.47K 1% PD_PEX0_STRAP_VS_MODE0 OUT1 3

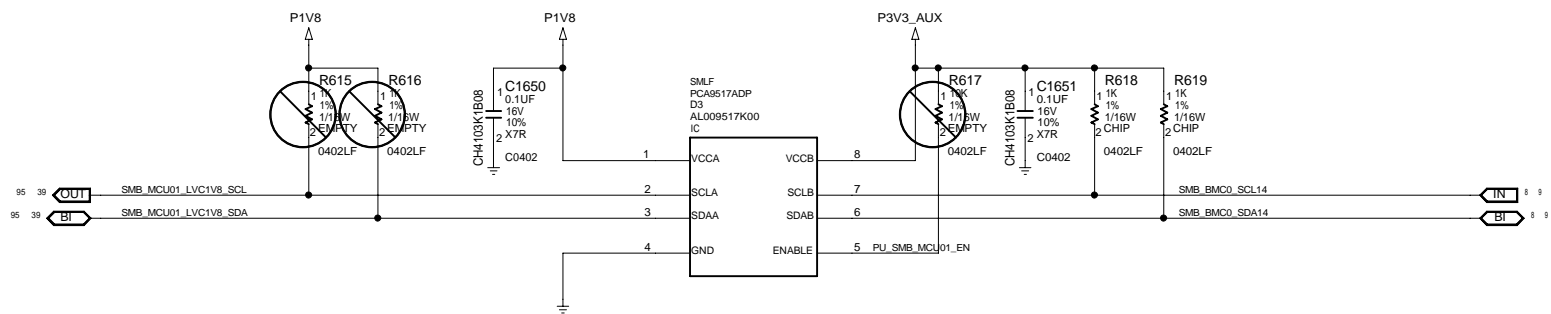
R803 1 2.47K 1% PD_PEX0_STRAP_VS_MODE1 OUT2 3

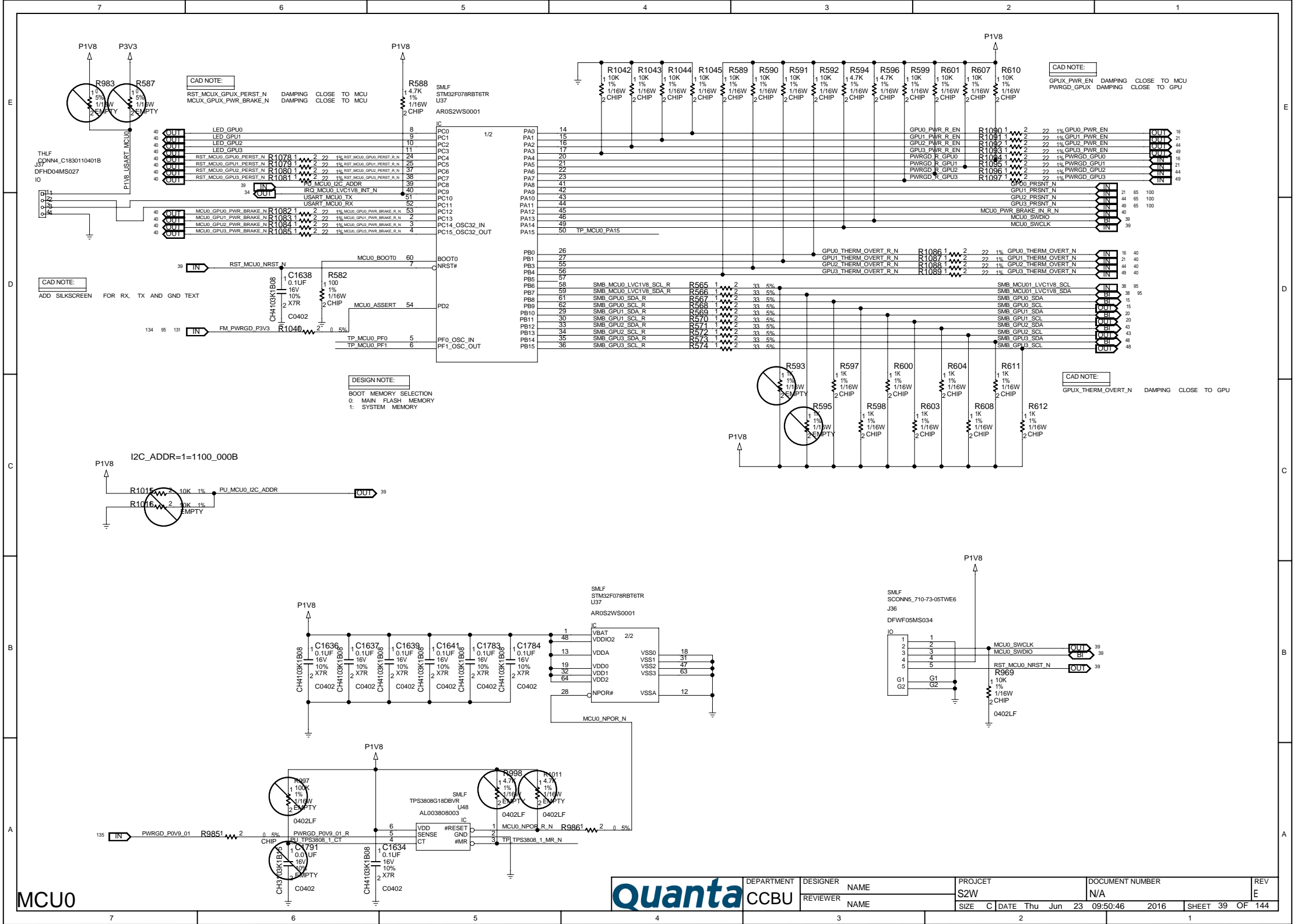
P1V8

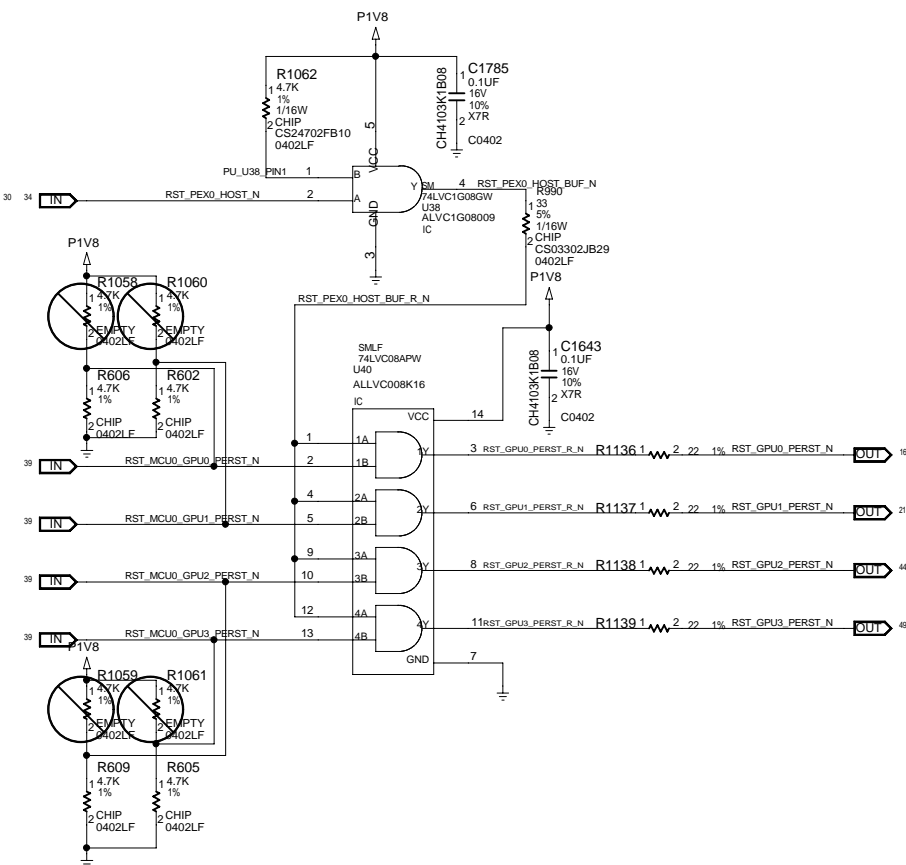
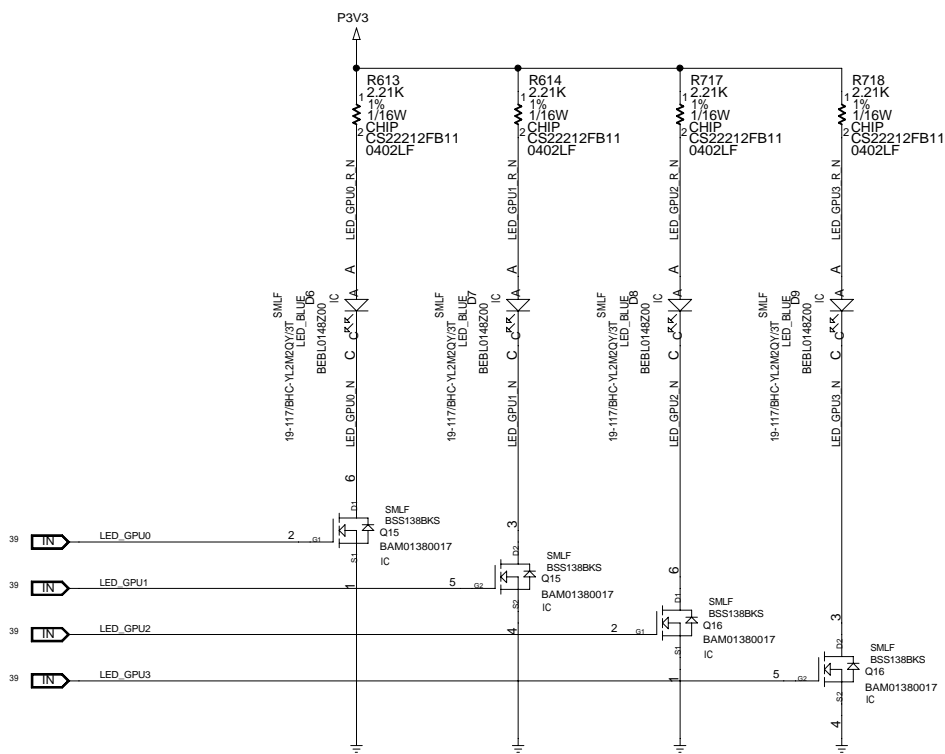
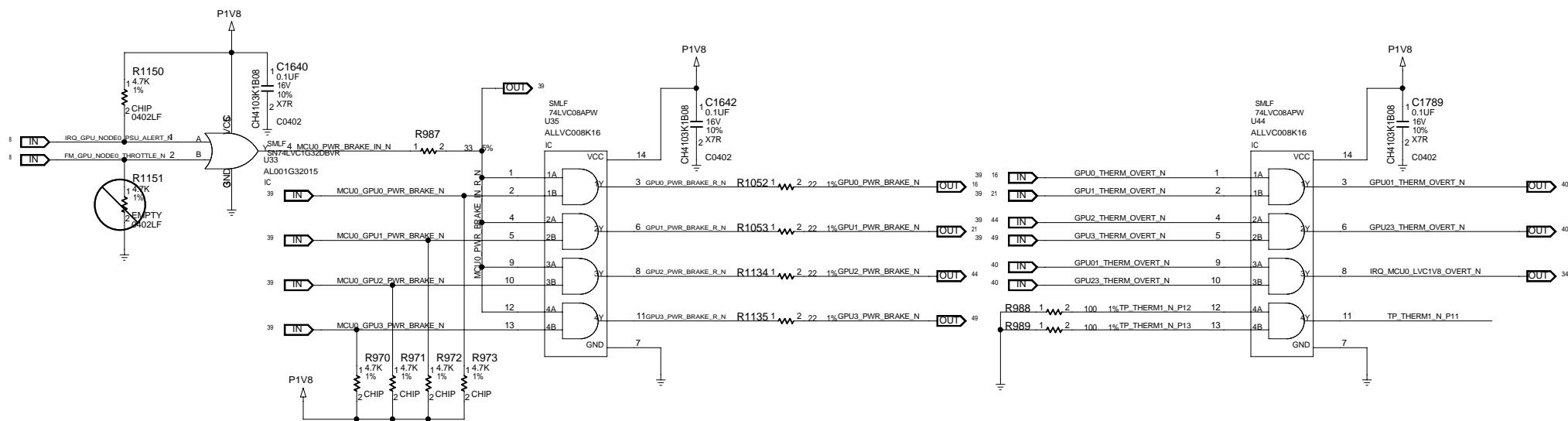
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R314 1 2 3K 1% PU_PEX0_STRAP_PROBE_MODE_N

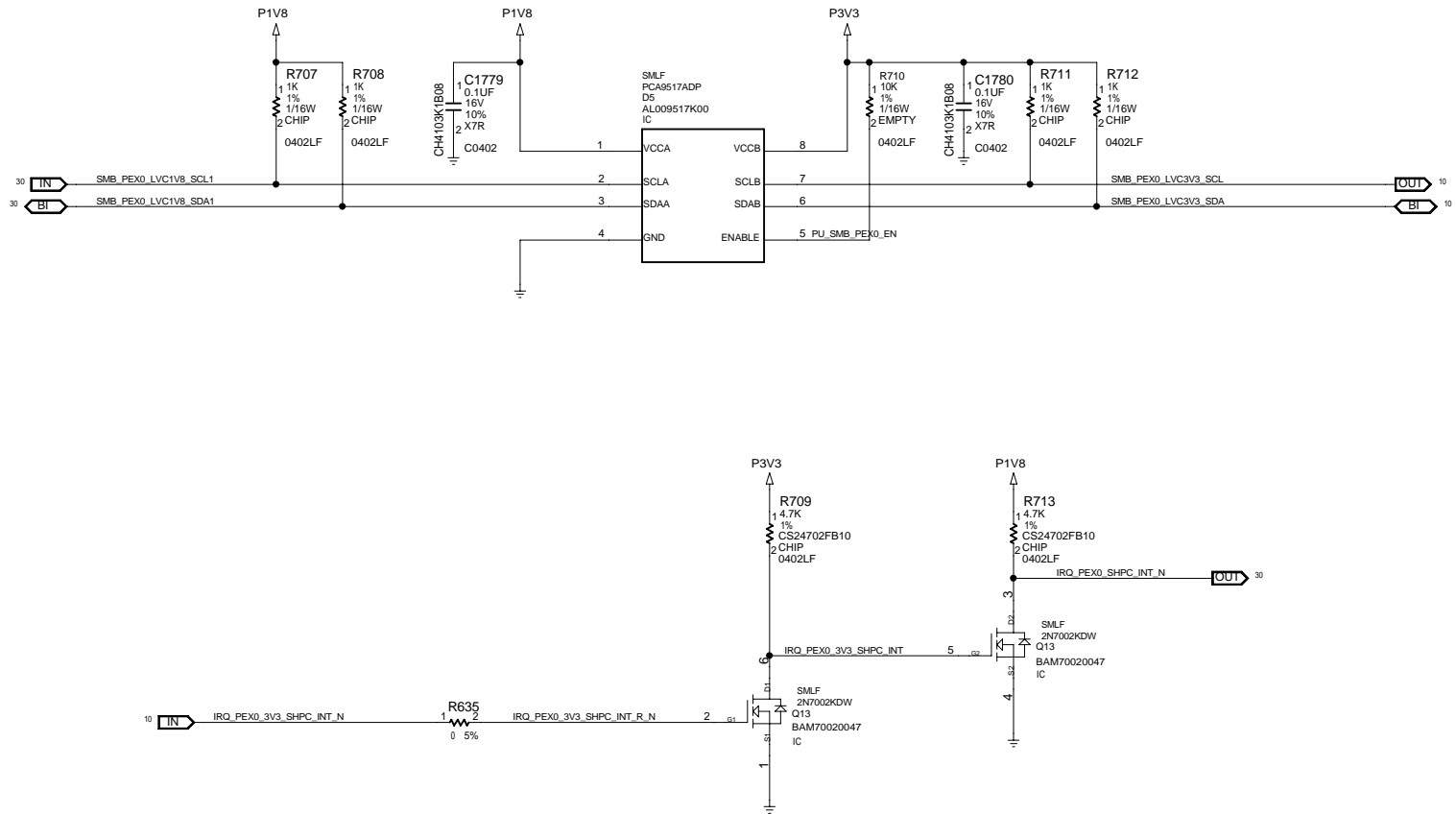
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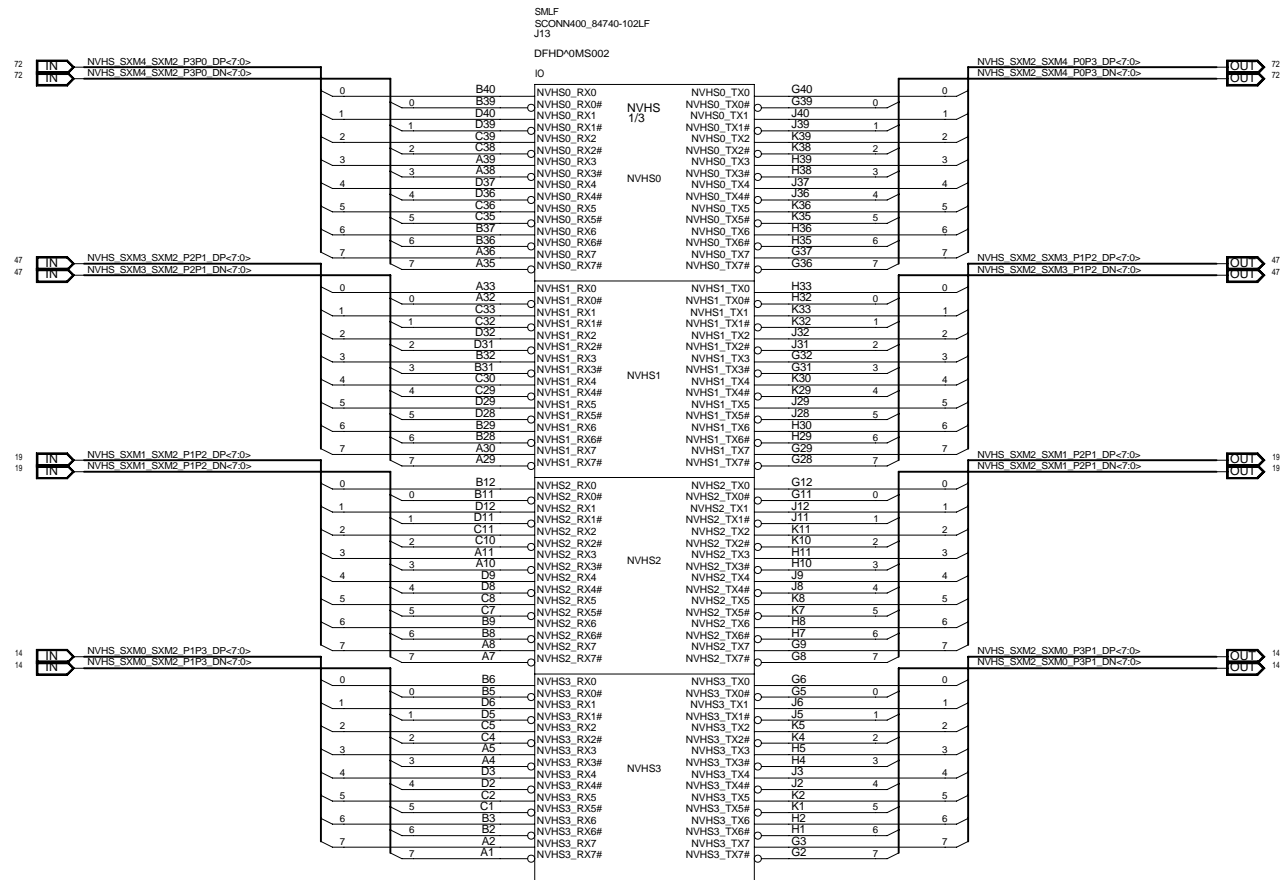


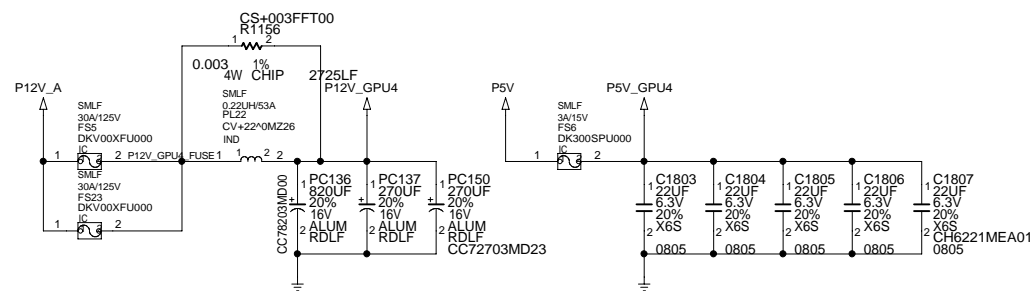
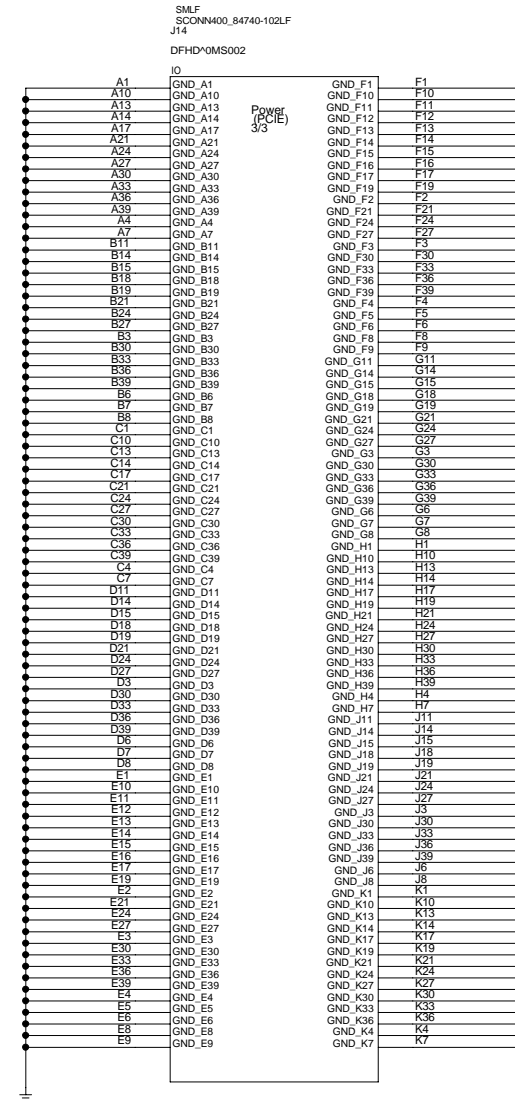
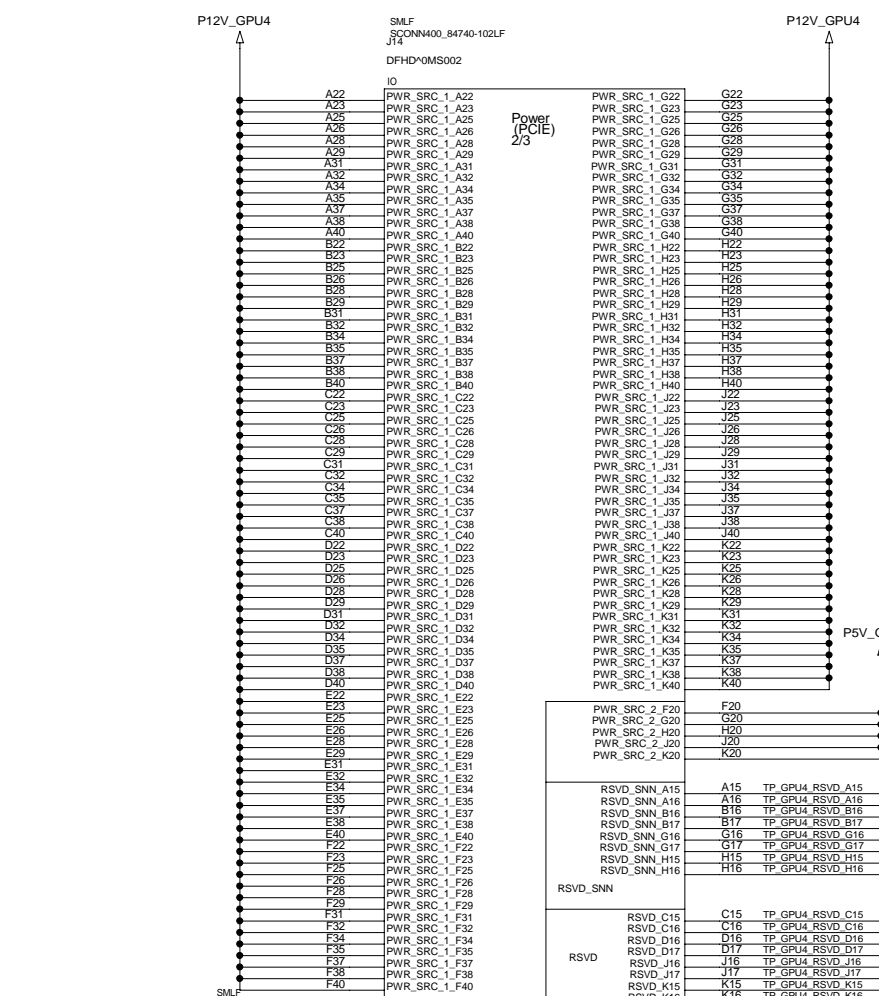


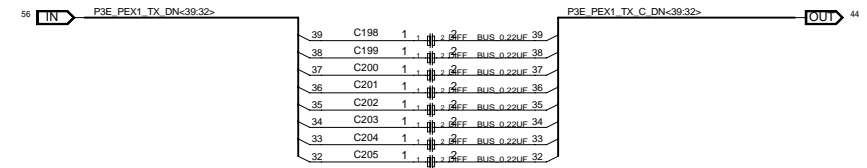
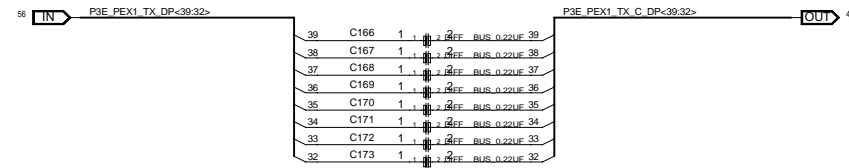
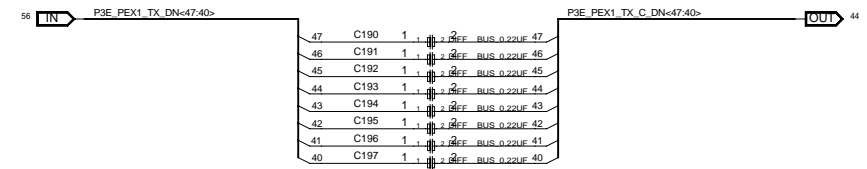
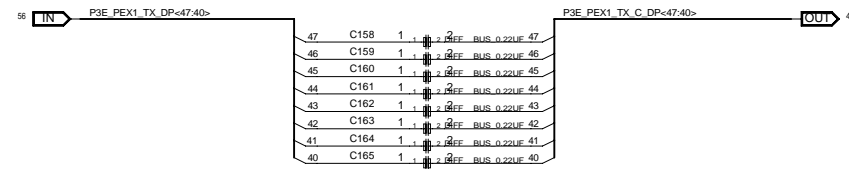
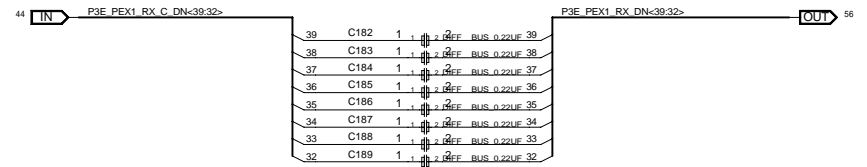
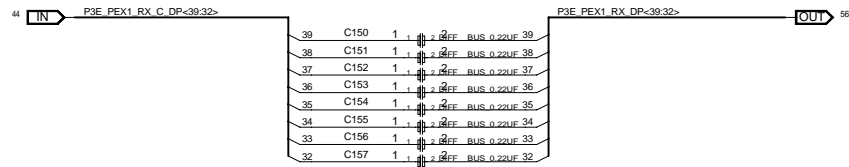
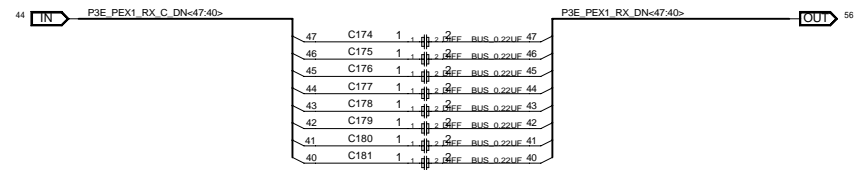
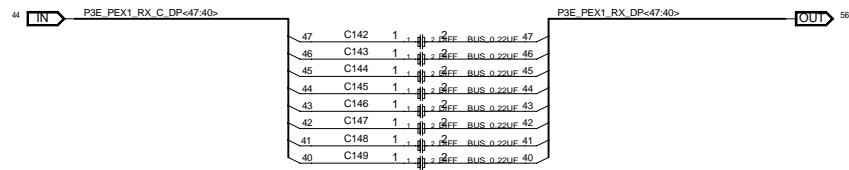


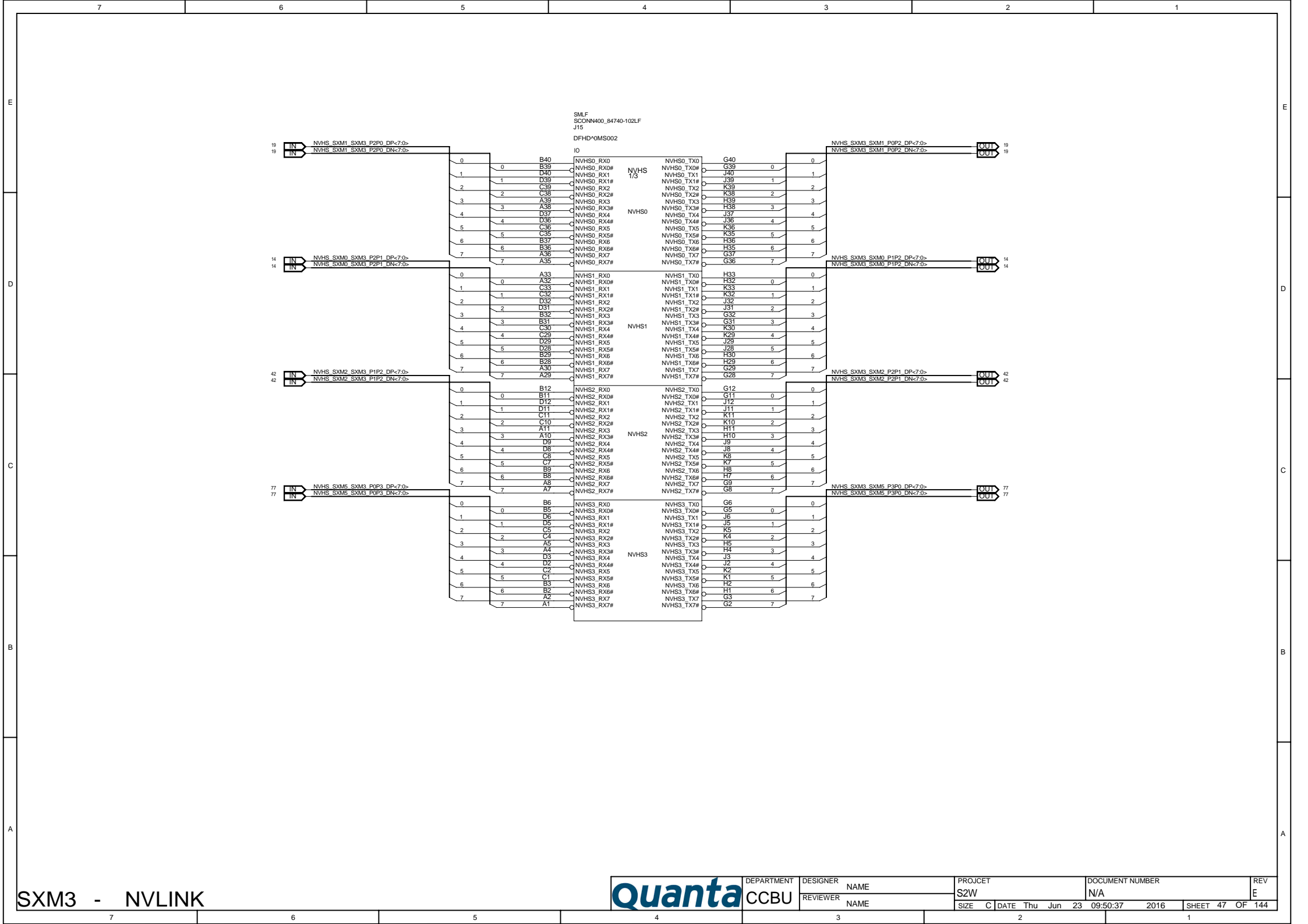
MCU0

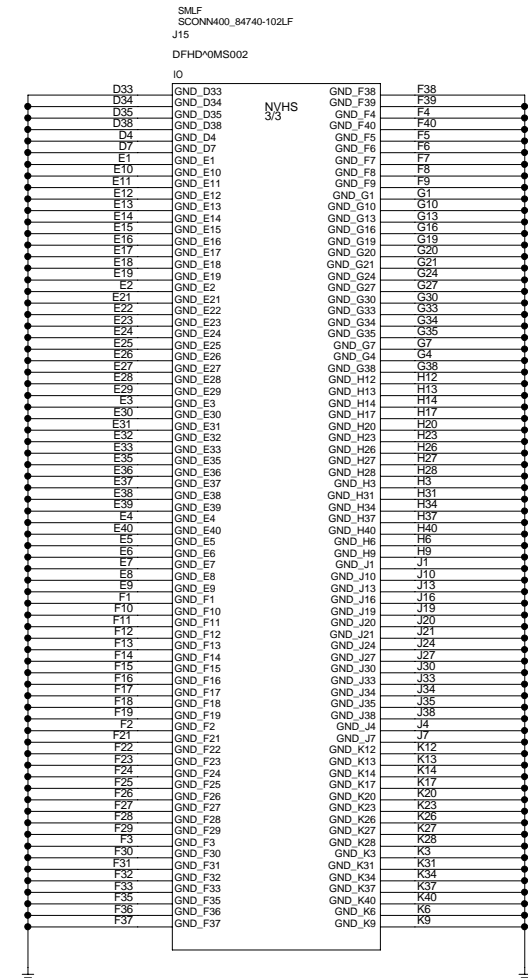
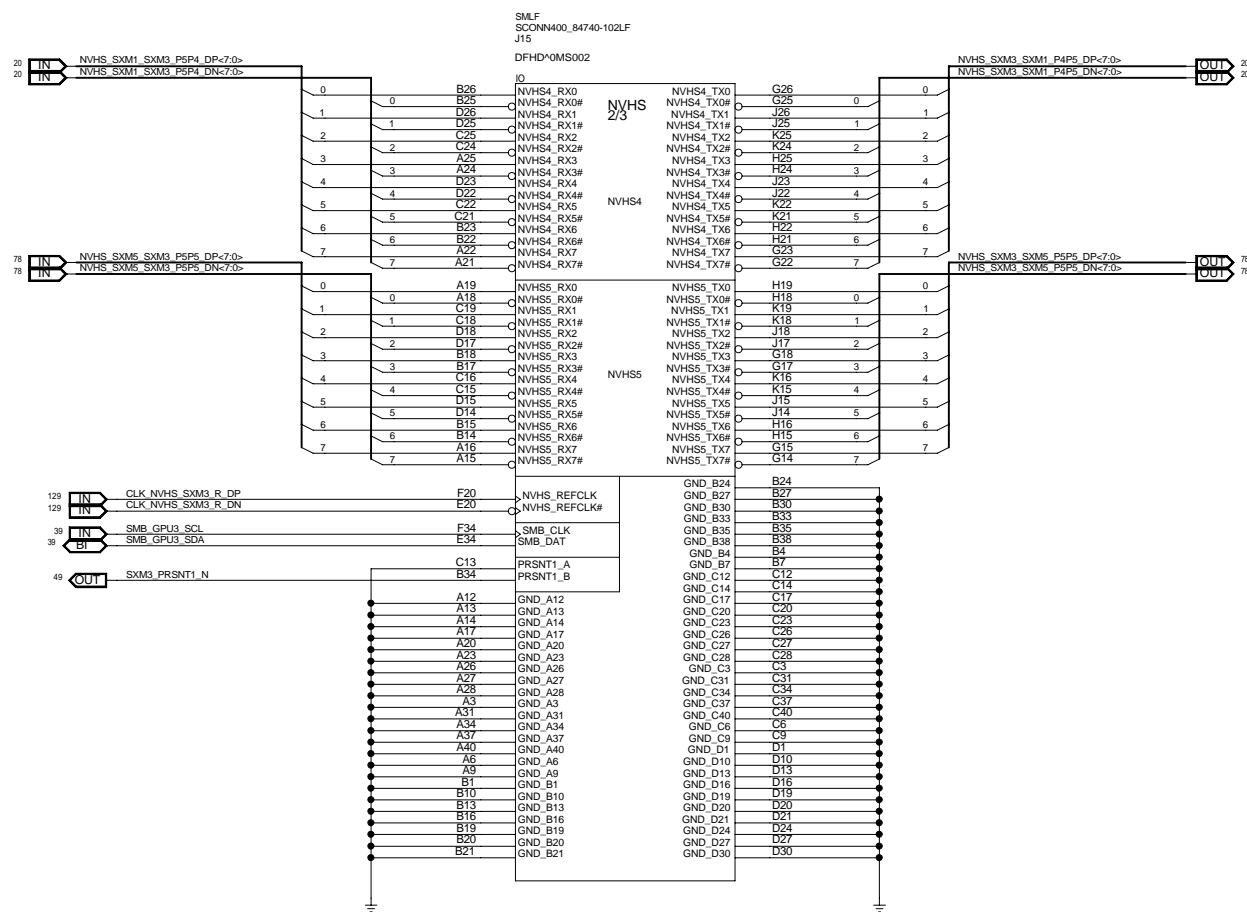


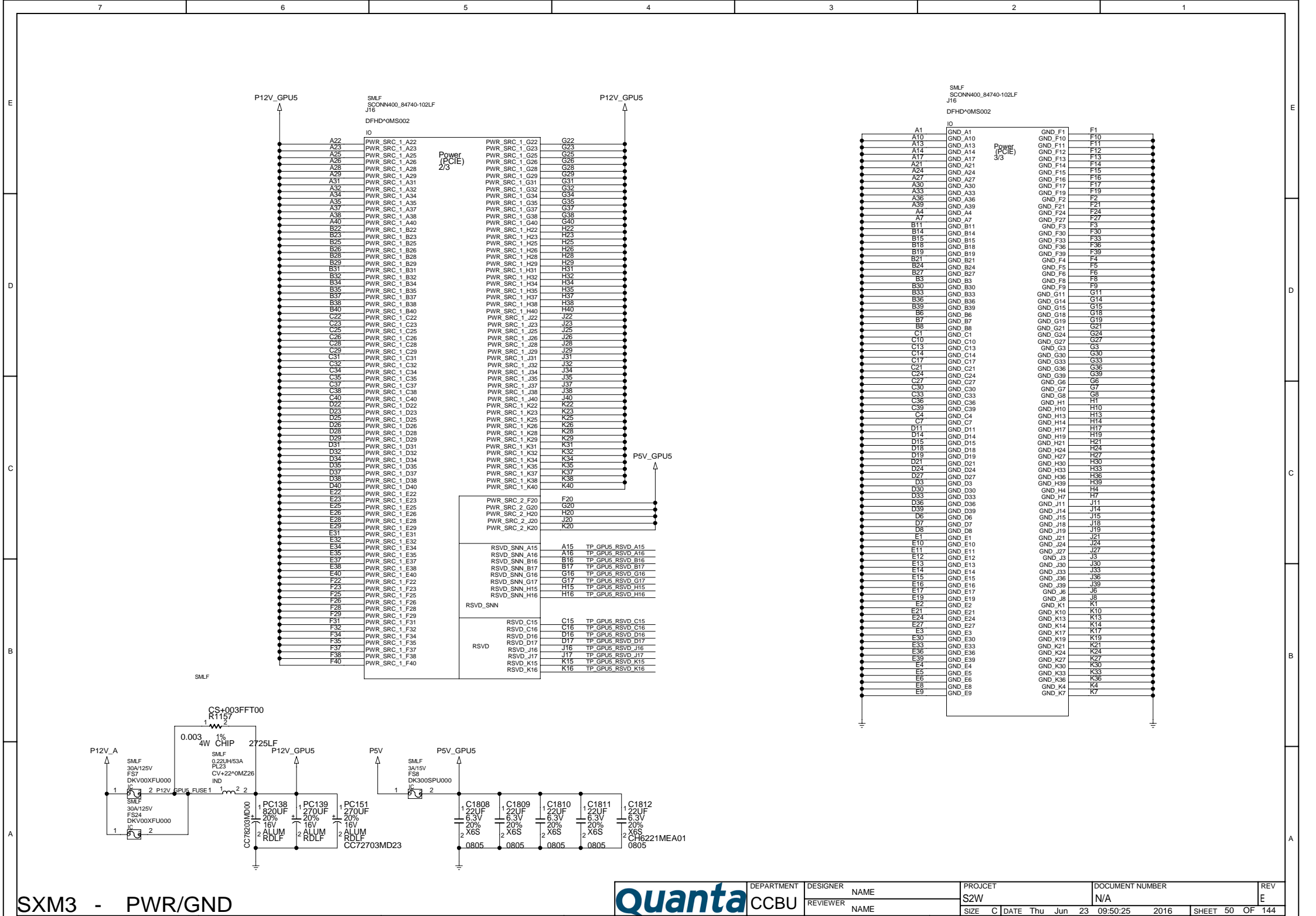












SXM3 - PWR/GND



DEPARTMENT
CCBU

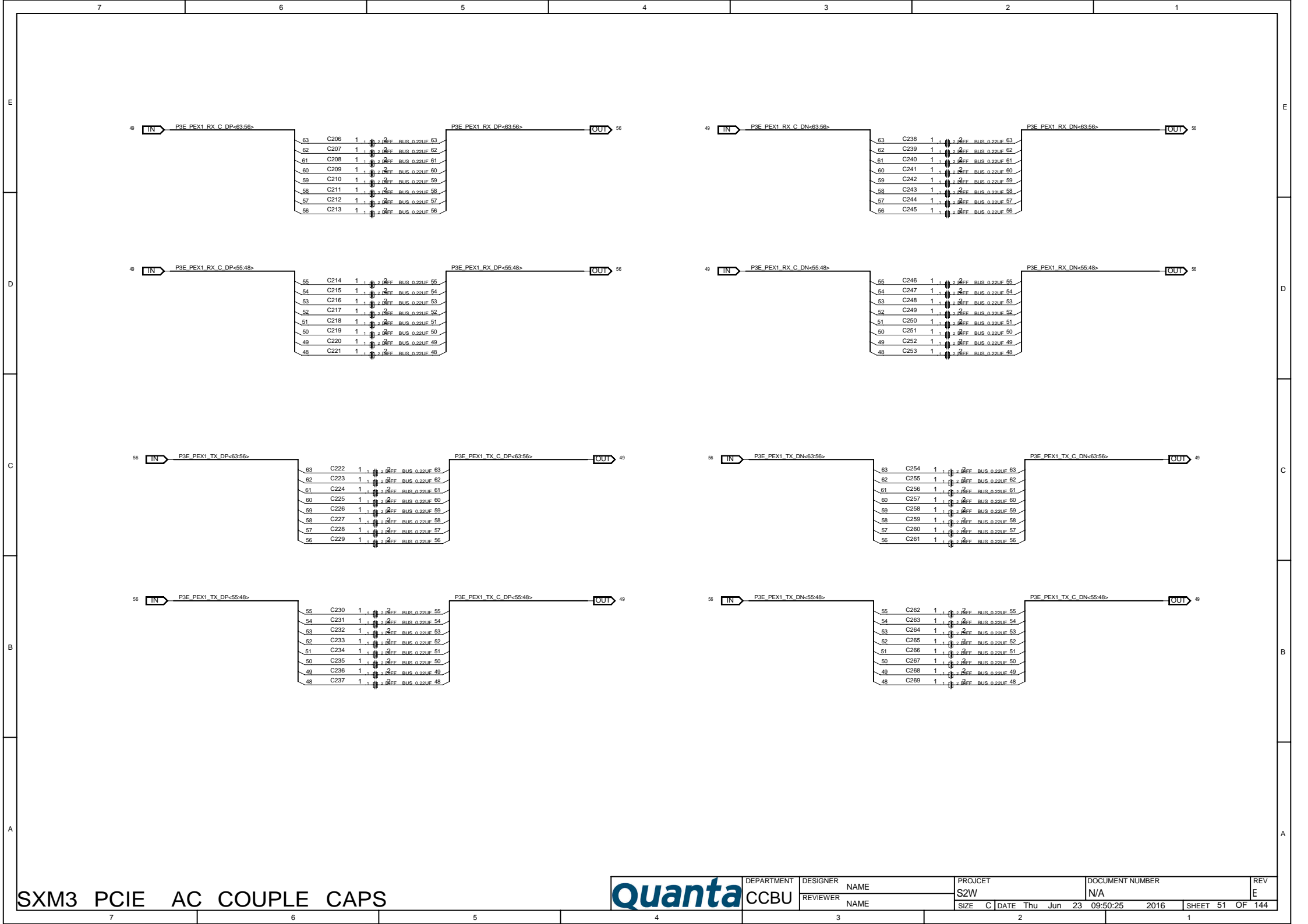
DESIGNER NAME
REVIEWER NAME

PROJCT
S2W

DOCUMENT NUMBER
N/A

REV
E

SIZE C DATE Thu Jun 23 09:50:25 2016 SHEET 50 OF 144



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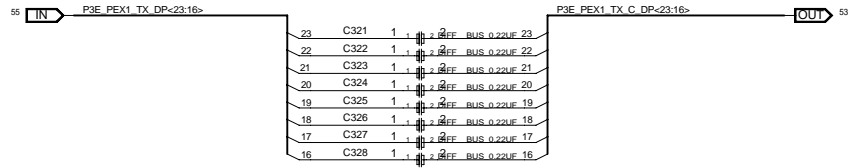
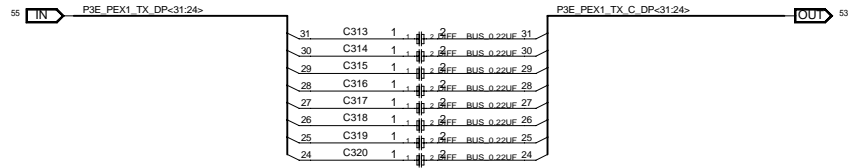
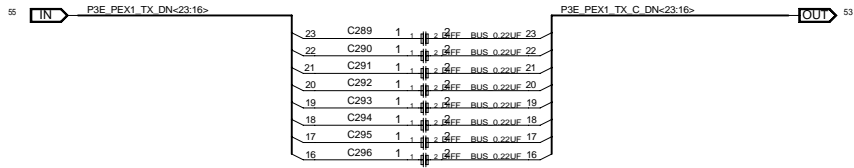
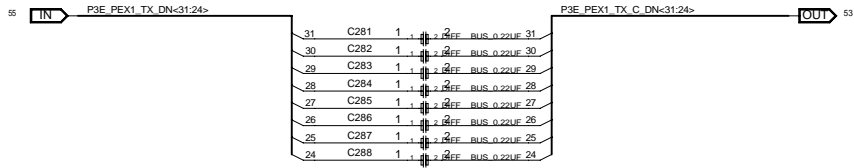
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SMLF
PEX8764-AB80BI
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IC

5/11

NC_AN27 AN27
NC_AP27 AP27
NC_AK27 AK27
NC_AL27 AL27

NC_AN28 AN28
NC_AP28 AP28
NC_AK28 AK28
NC_AL28 AL28

AJ27 NC_AJ27
AG29 NC_AG29
AB29 NC_AB29
Y29 NC_Y29

NC_AN29 AN29
NC_AP29 AP29
NC_AK29 AK29
NC_AL29 AL29

NC_AN30 AN30
NC_AP30 AP30
NC_AK30 AK30
NC_AL30 AL30

AJ26 NC_AJ26
AF29 NC_AF29
AA29 NC_AA29
W29 NC_W29

NC_AJ33 AJ33
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NC_AJ30 AJ30
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AE29 NC_AE29

NC_AH33 AH33
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AE27 NC_AE27
AE28 NC_AE28
AB27 NC_AB27
AB28 NC_AB28
W27 NC_W27
W28 NC_W28

NC_AG33 AG33
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NC_AG31 AG31

NC_AF33 AF33
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NC_AF30 AF30
NC_AF31 AF31

Y28 NC_Y28
AP33 NC_AP33
V27 NC_V27
U28 NC_U28

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NC_AD33 AD33
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SMLF
PEX8764-AB80BI
U3
AJ087640T01

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7/11

A2 NC_A2
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AB1 NC_AB1
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AB5 NC_AB5
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D2 NC_D2
F17 NC_F17

NC_G19 G19
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NC_J16 J16
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NC_R29 R29
NC_T27 T27
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SMLF
PEX8764-AB80BI
U3
AJ087640T01

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6/11

NC_U33 U33
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H29 NC_H29
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J29 NC_J29

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NC_L31 L31

R27 NC_R27
R28 NC_R28
L27 NC_L27
L28 NC_L28

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NC_K30 K30
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G27 NC_G27
G28 NC_G28
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B31 NC_B31

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NC_G31 G31

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NC_B28 B28
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NC_D27 D27

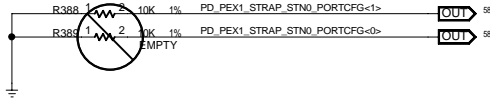
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NC_E26 E26
NC_D26 D26

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NC_D25 D25

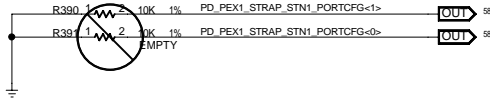




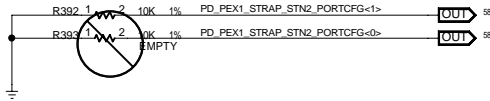
STATION0 PORT CONFIG
CONTROL THRU EEPROM
STN0: 300H[2:0]=001B=X16
STRAP_STN0_PORTCFG[1:0]=0Z=X16



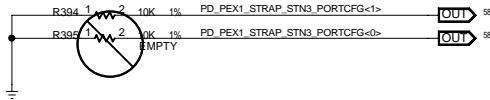
STATION1 PORT CONFIG
CONTROL THRU EEPROM
STN1: 300H[5:3]=001B=X16
STRAP_STN1_PORTCFG[1:0]=0Z=X16



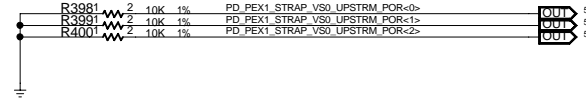
STATION2 PORT CONFIG
CONTROL THRU EEPROM
STN2: 300H[8:6]=001B=X16
STRAP_STN2_PORTCFG[1:0]=0Z=X16



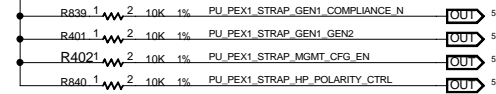
STATION3 PORT CONFIG
CONTROL THRU EEPROM
STN3: 300H[11:9]=001B=X16
STRAP_STN3_PORTCFG[1:0]=0Z=X16



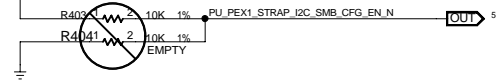
UPSTREAM PORT SELECT
CONTROL THRU EEPROM
360H[4:0]=0 0000B=PORT 0
STRAP_UPSTRM_PORTSEL[2:0]=000=PORT 0



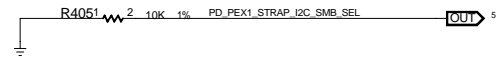
1=PCIE MAX DATA RATE =GEN3
1=MANAGEMENT PORT IS DISABLED



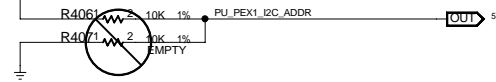
STRAP_I2C_SMBUS_CFG_EN#=1=DISABLE I2C INITIAL



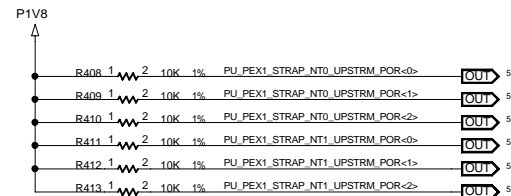
STRAP_I2C_SMBUS_SEL=0=ENABLE I2C SLAVE PROTOCOL



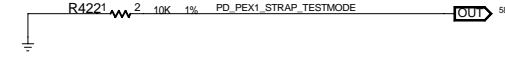
I2C_ADDR=1=1011_111B



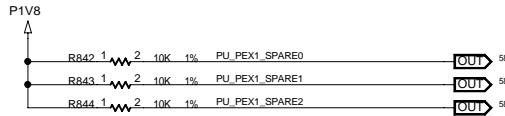
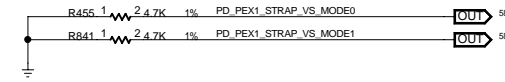
STRAP_NT_UPSTRM_POR<0:2> =111= DISABLE NT MODE



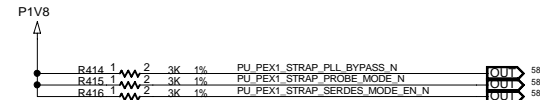
BASE MODE: TEST MODE=0
=PORT_GOODX# + GPIOX INPUT



BASE MODE: LL(00)=SINGLE SWITCH



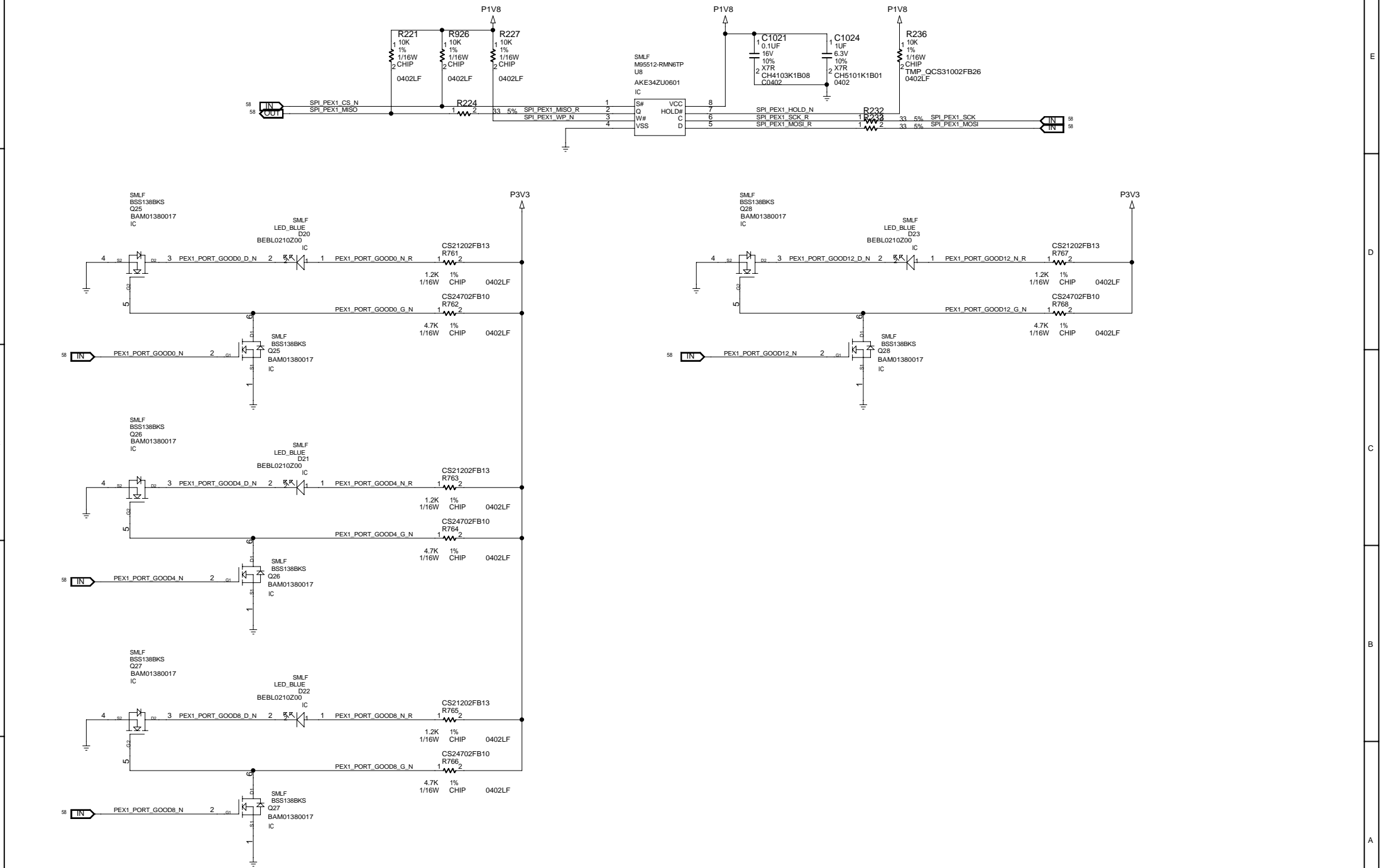
FOR FACTORY TEST ONLY



PEX1 EEPROM & PORT LED



DEPARTMENT	DESIGNER	NAME	PROJCT	DOCUMENT NUMBER	REV
CBCU	REVIEWER	NAME	S2W	N/A	E
			SIZE	C	DATE
			Thu	Jun	23
			09:50:53	2016	SHEET 63 OF 144



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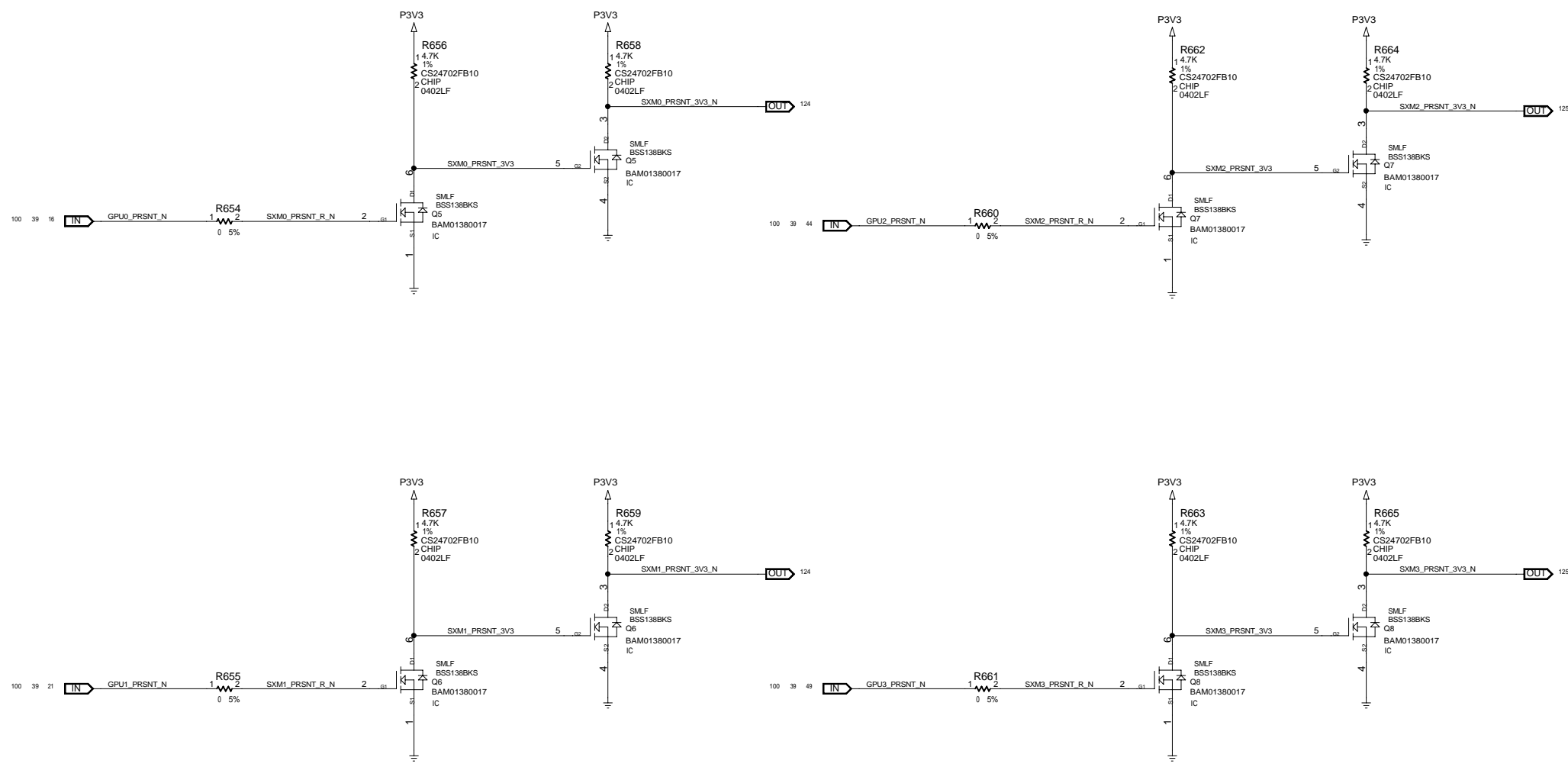
E

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SXM0/1/2/3 PRSNT# LEVEL SHIFT



DEPARTMENT	DESIGNER	NAME	PROJECT	DOCUMENT NUMBER	REV
CCBU	REVIEWER	NAME	S2W	N/A	E
SIZE	C	DATE	Thu Jun 23 09:50:47 2016	SHEET 65 OF 144	1

SXM4/5/6/7

PRSNT# LEVEL SHIFT



DEPARTMENT
CCBU

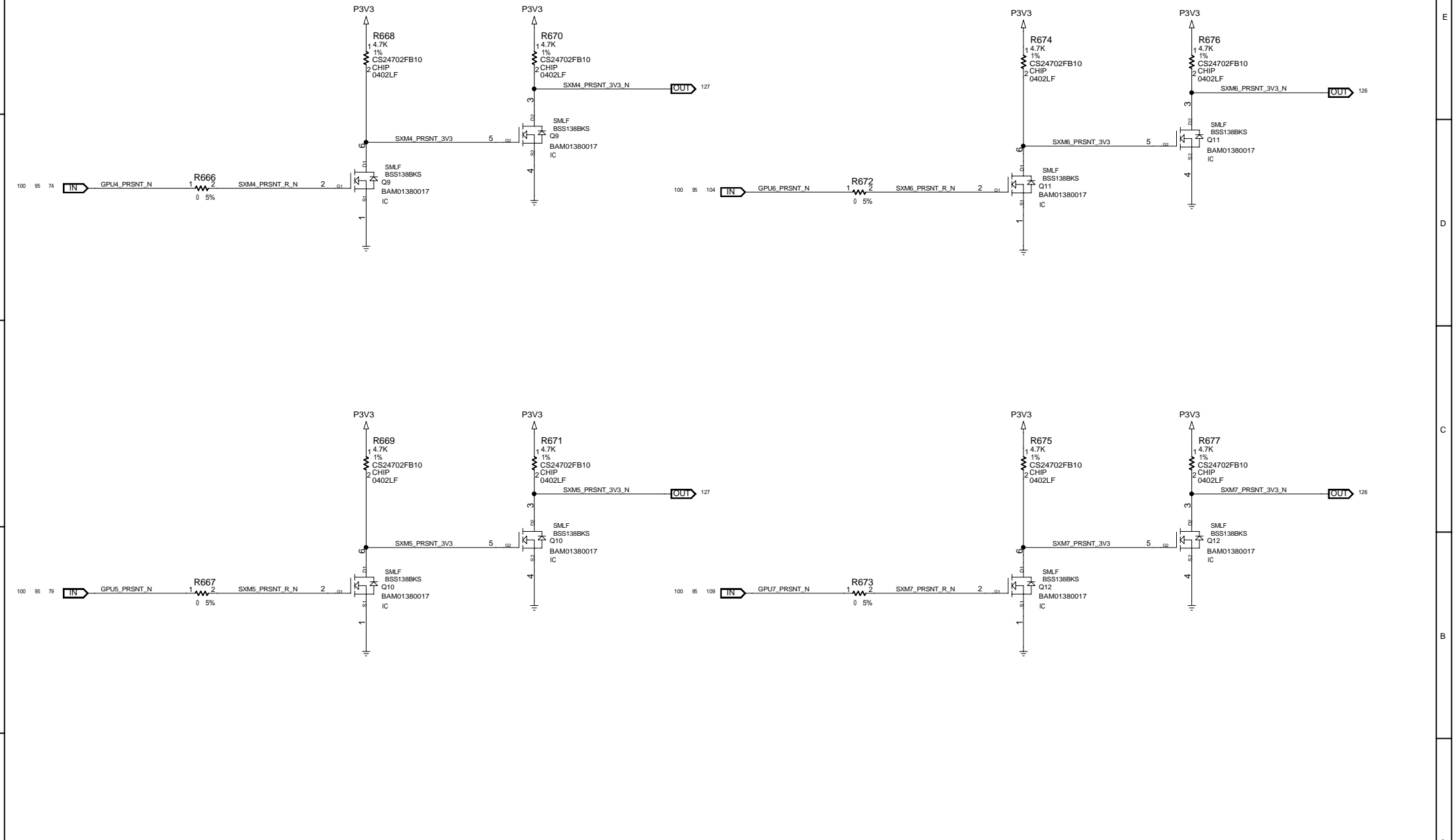
DESIGNER NAME
REVIEWER NAME

PROJCT
S2W

DOCUMENT NUMBER
N/A

REV
E

SIZE C DATE Thu Jun 23 09:50:47 2016 SHEET 66 OF 144



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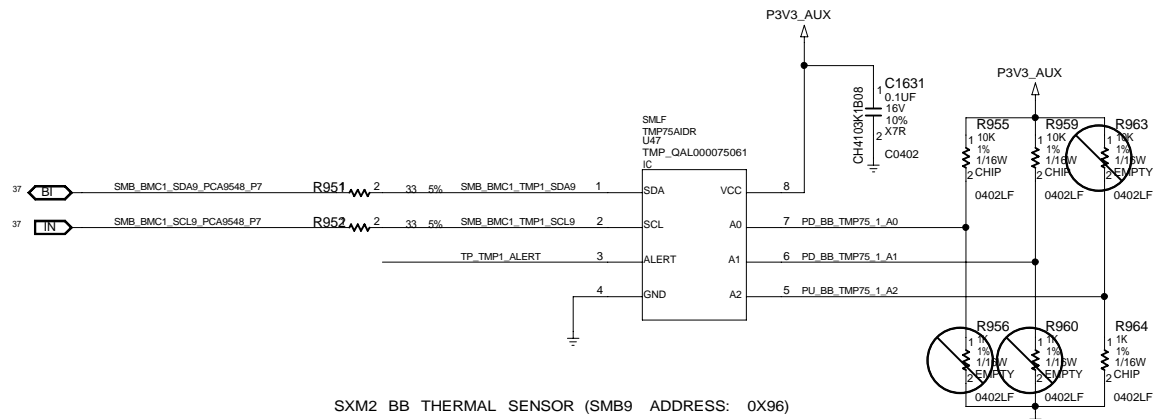
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	7	6	5	4	3	2	1
E							
D							
C							
B							
A							
UNTITLED				<div><div>Quanta</div><div>DEPARTMENT CCBU</div><div>DESIGNER NAME</div><div>REVIEWER NAME</div></div> <div><div>PROJCET S2W</div><div>DOCUMENT NUMBER N/A</div><div>SIZE C</div><div>DATE Thu Jul 23 11:27:32 2015</div><div>SHEET 69 OF 144</div></div> <div><div>REV E</div></div>			
	7	6	5	4	3	2	1

7	6	5	4	3	2	1
E						E
D						D
C						C
B						B
A						A
UNTITLED				<div><div>Quanta</div><div>DEPARTMENT CCBU</div></div>		
				DESIGNER NAME		PROJCET S2W
				REVIEWER NAME		DOCUMENT NUMBER N/A
				SIZE	C	DATE
				Thu	Jul	23
				11:27:32	2015	SHEET 70 OF 144
				2		1

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E							
D							
C							
B							
A							
UNTITLED				<div><div>Quanta</div><div>DEPARTMENT CCBU</div><div>DESIGNER NAME</div><div>REVIEWER NAME</div></div> <div><div>PROJCET S2W</div><div>DOCUMENT NUMBER N/A</div><div>SIZE C</div><div>DATE Thu Jul 23 11:27:32 2015</div><div>SHEET 71 OF 144</div></div> <div><div>REV E</div></div>			

SXM4 - NVLINK

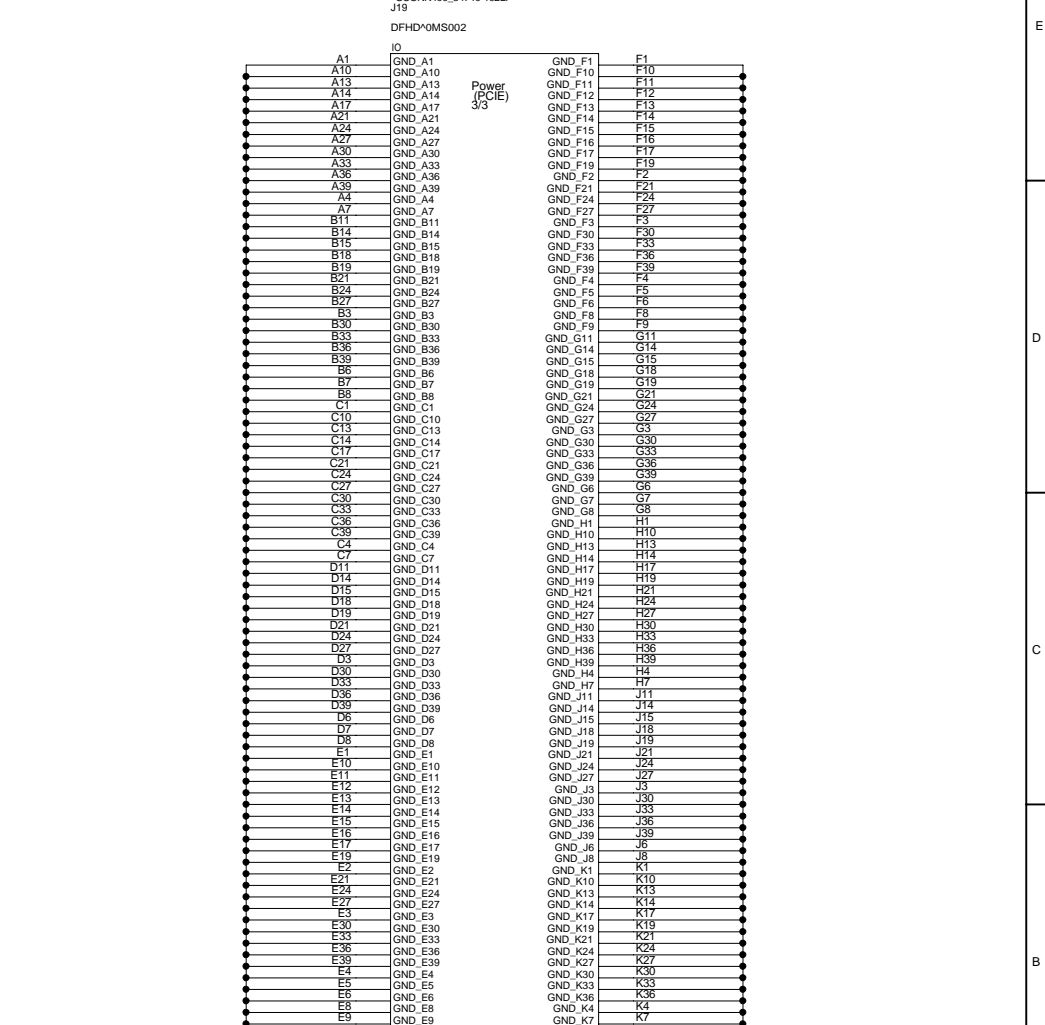
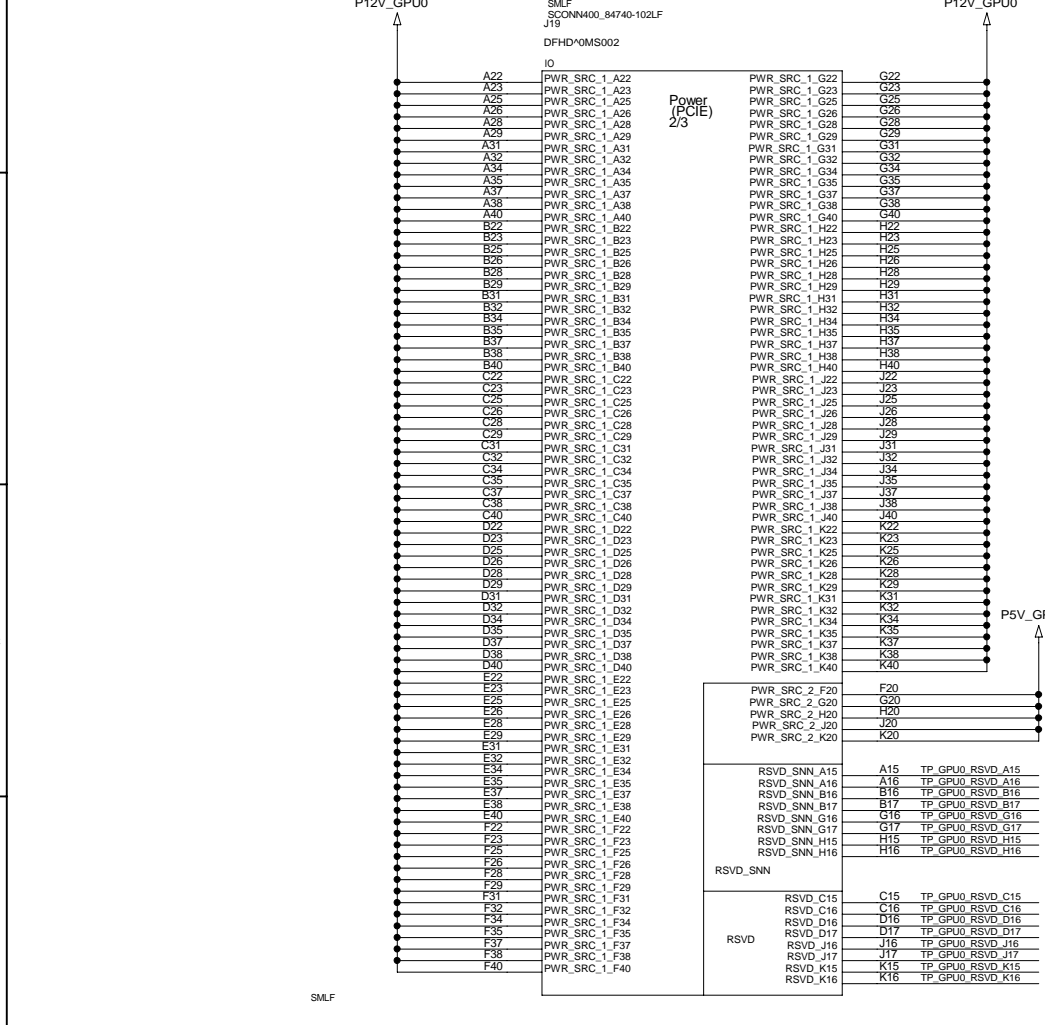
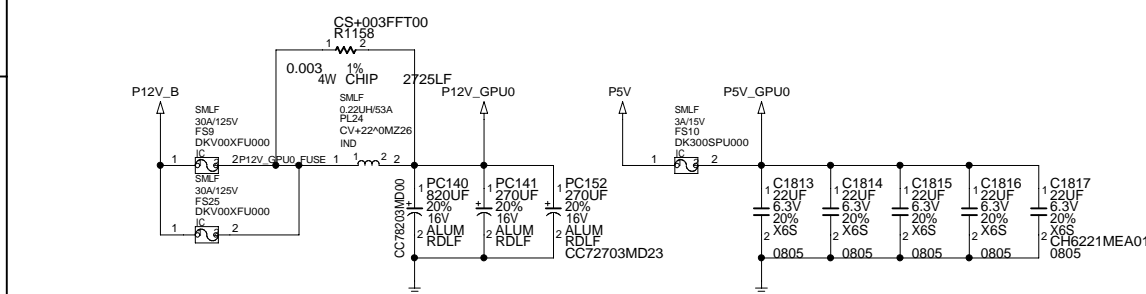


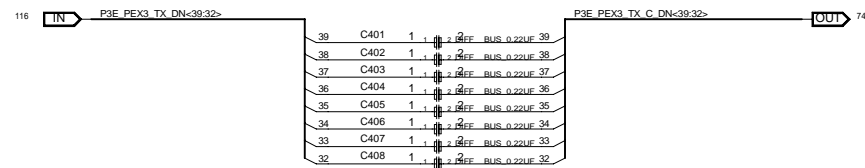
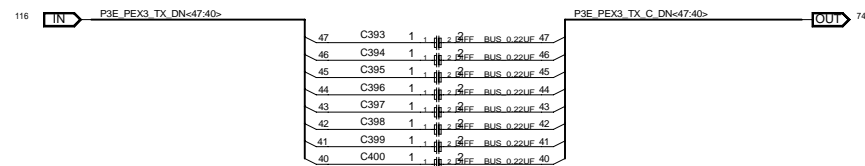
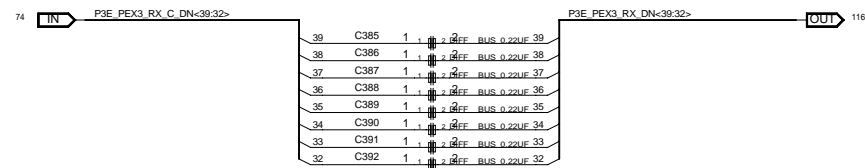
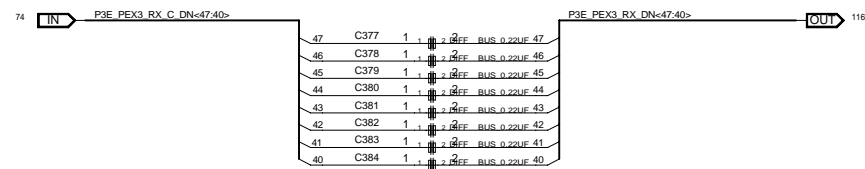
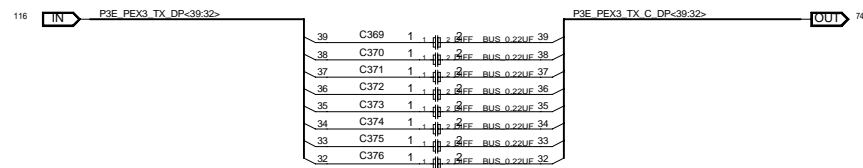
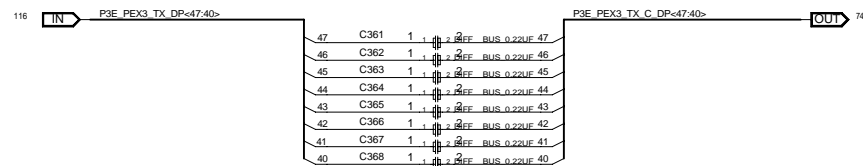
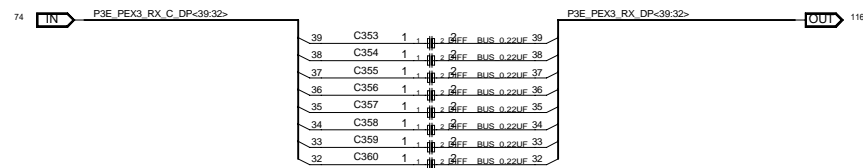
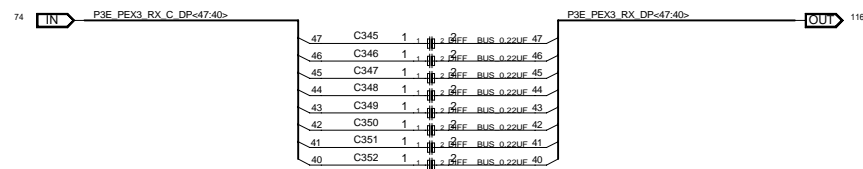
DEPARTMENT	DESIGNER	PROJECT	DOCUMENT NUMBER	REV
CCBU	NAME	S2W	N/A	E
REVIEWER	NAME	SIZE	C	DATE
		2	Thu	Jun 23
		09:50:37	2016	SHEET 72 OF 144

SXM4 - PWR/GND

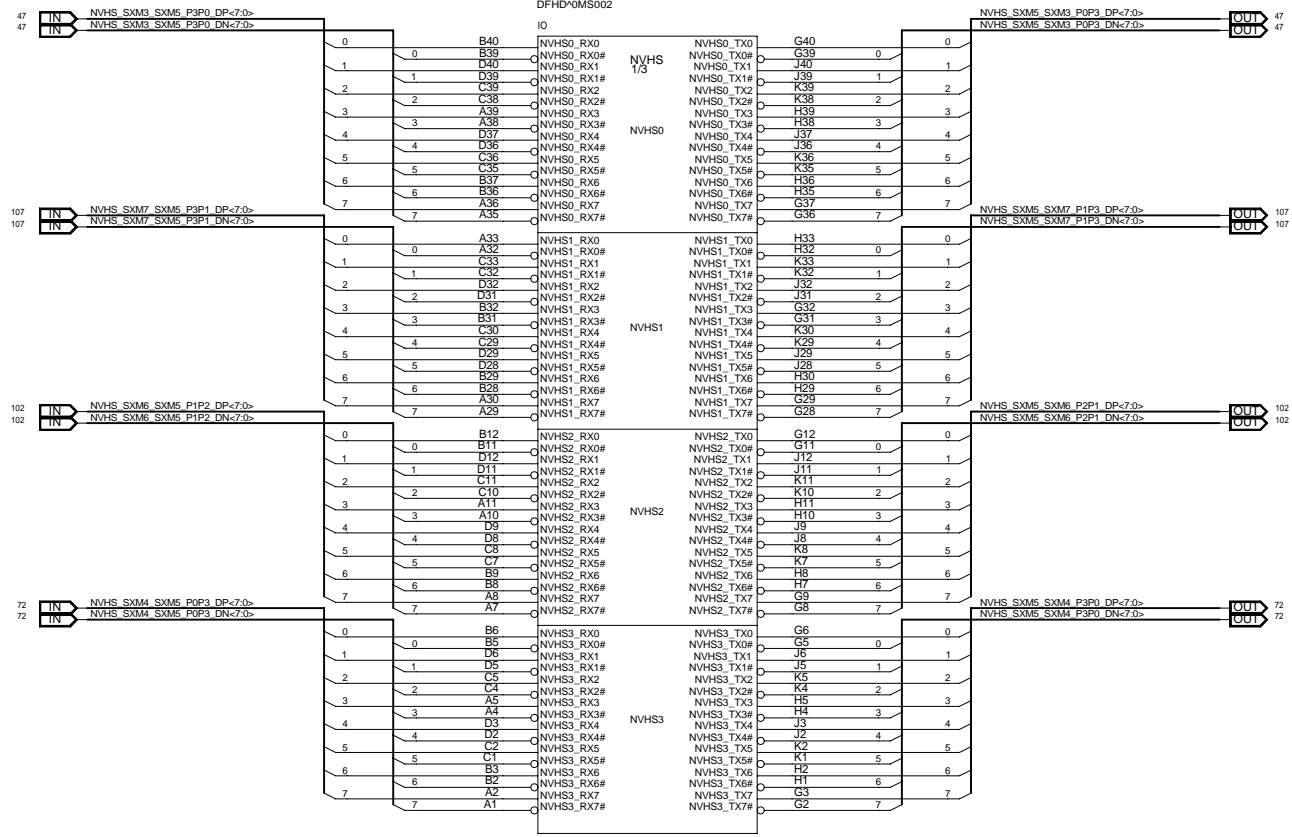


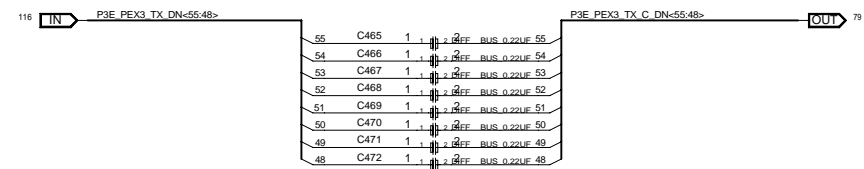
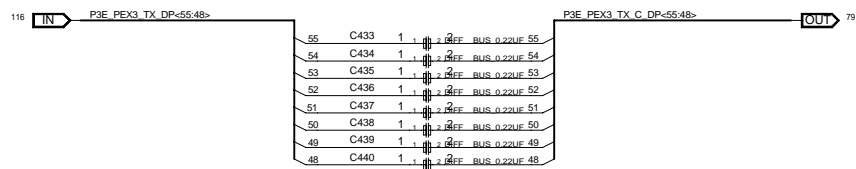
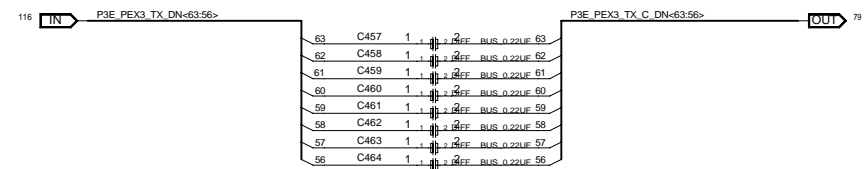
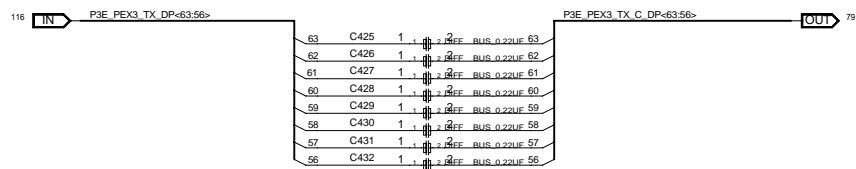
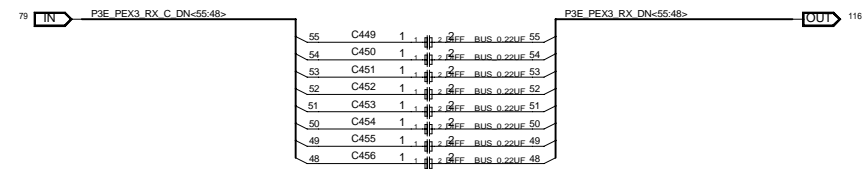
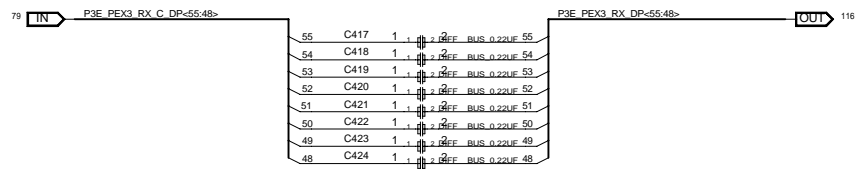
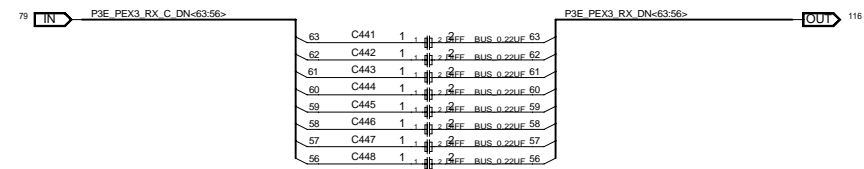
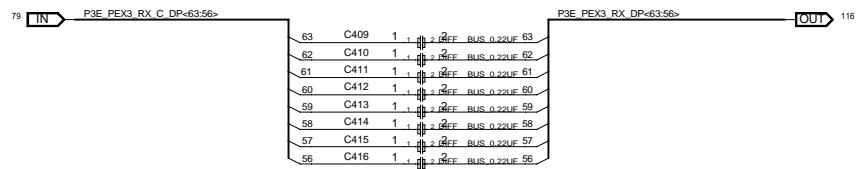
DEPARTMENT	DESIGNER	NAME	PROJECT	DOCUMENT NUMBER	REV
CBCU	REVIEWER	NAME	S2W	N/A	E
SIZE	C	DATE	Thu Jun 23 09:50:28 2016	SHEET 75 OF 144	1





SMLF
SCONN400_84740-102LF
J20
DFHD*0MS002
IO





E

D

C

B

A

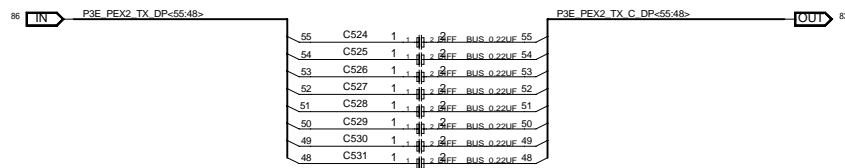
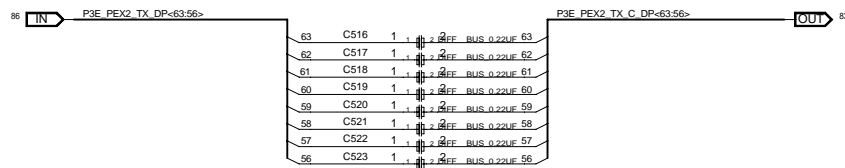
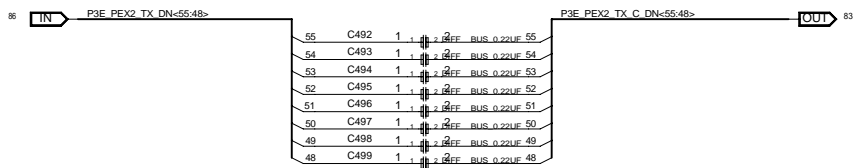
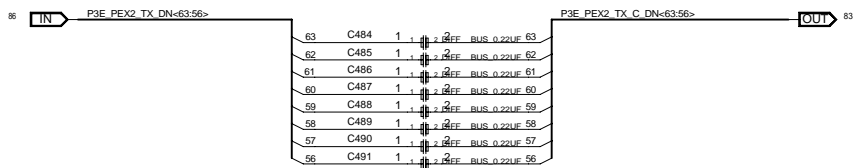
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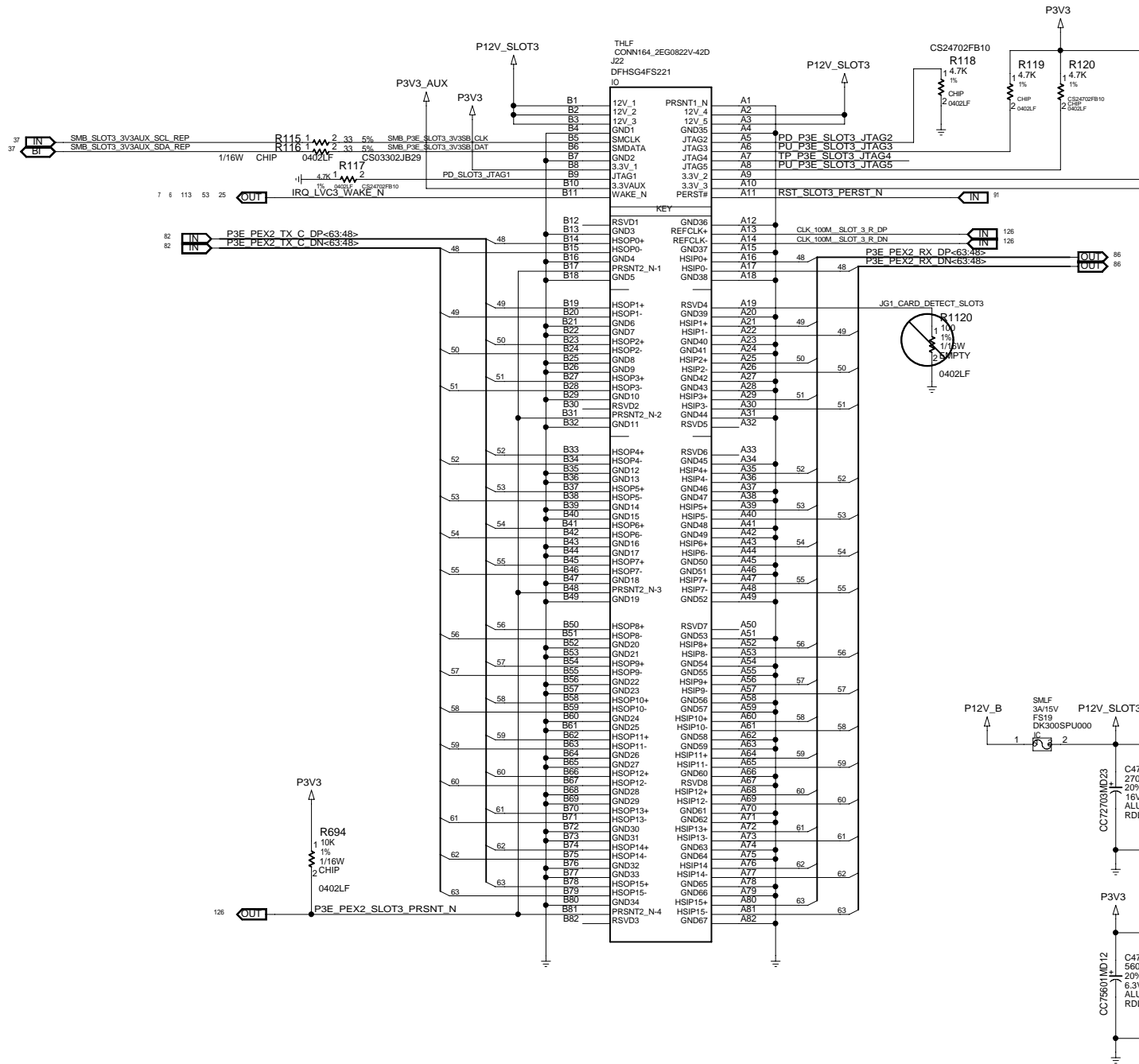
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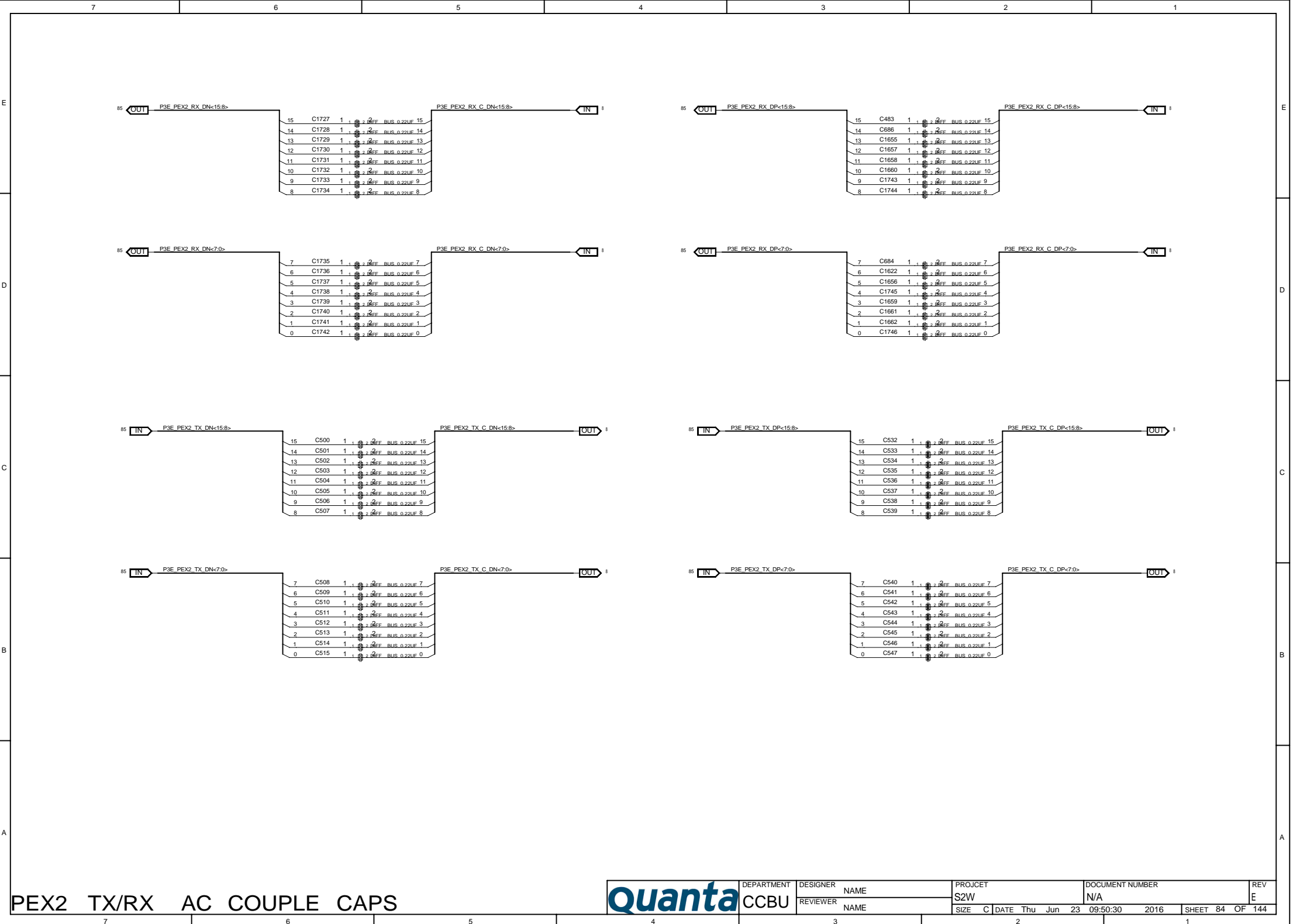
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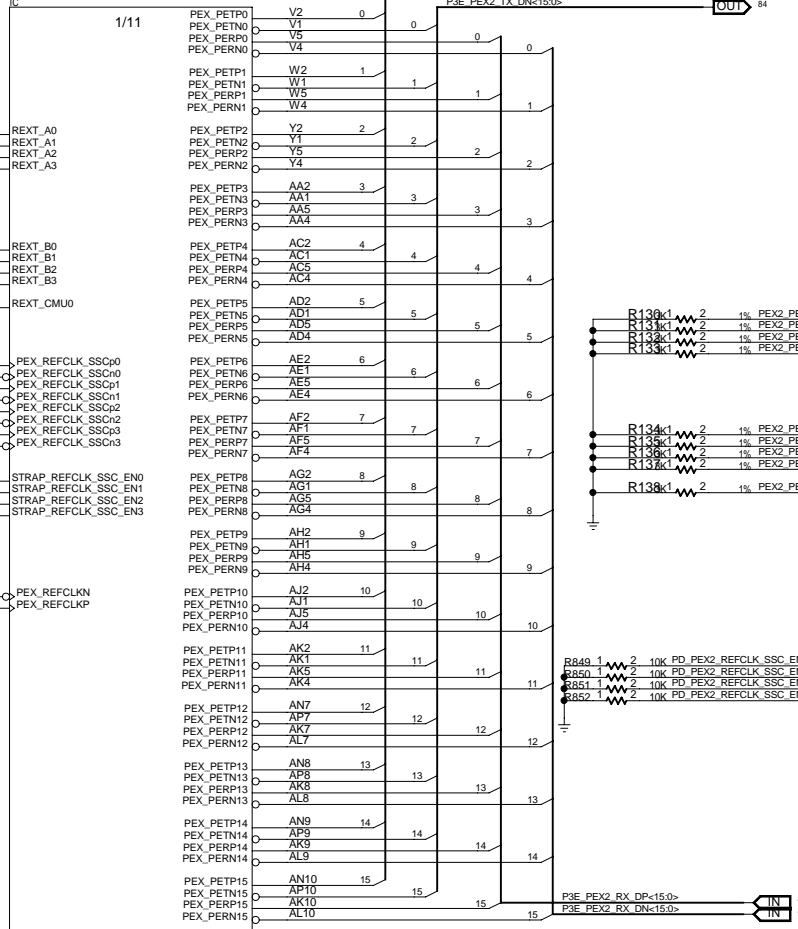
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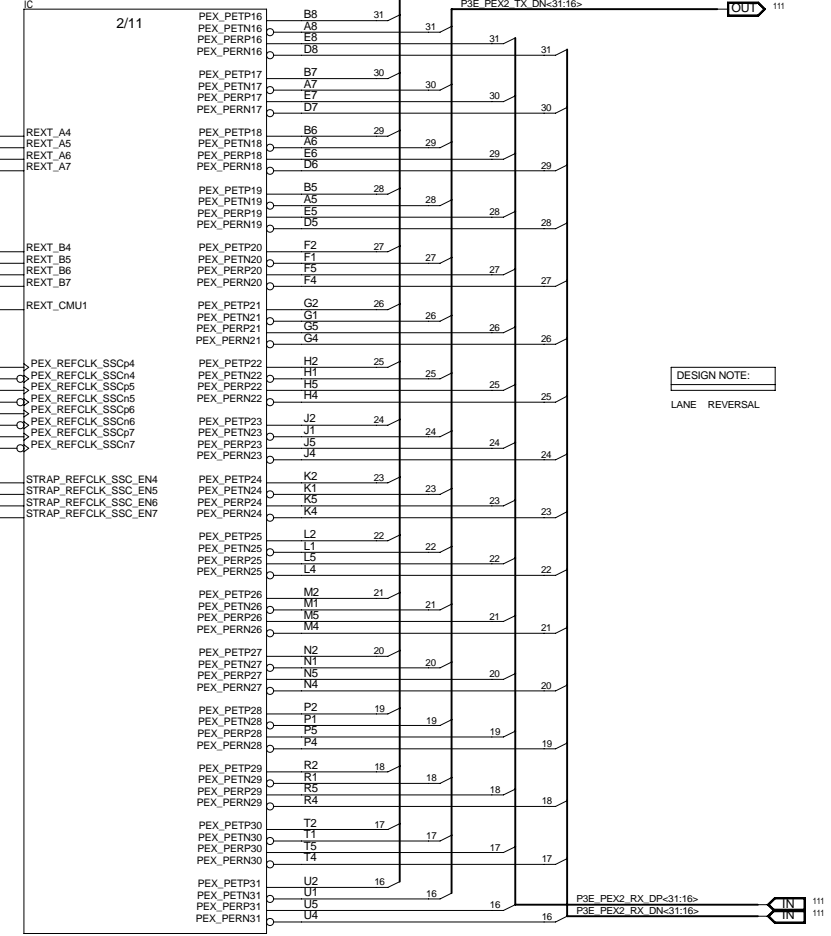


SMLF
PEX8780-AB80BI
U4
AJ087800T01



PLX TO CPU

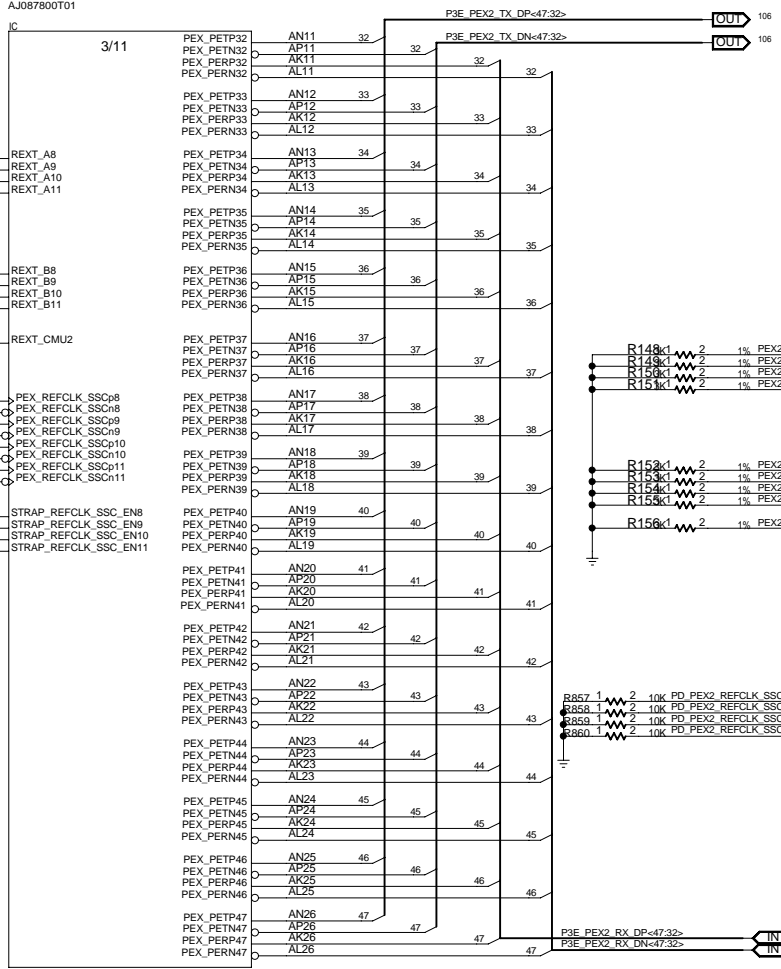
SMLF
PEX8780-AB80BI
U4
AJ087800T01



DESIGN NOTE:
LANE REVERSAL

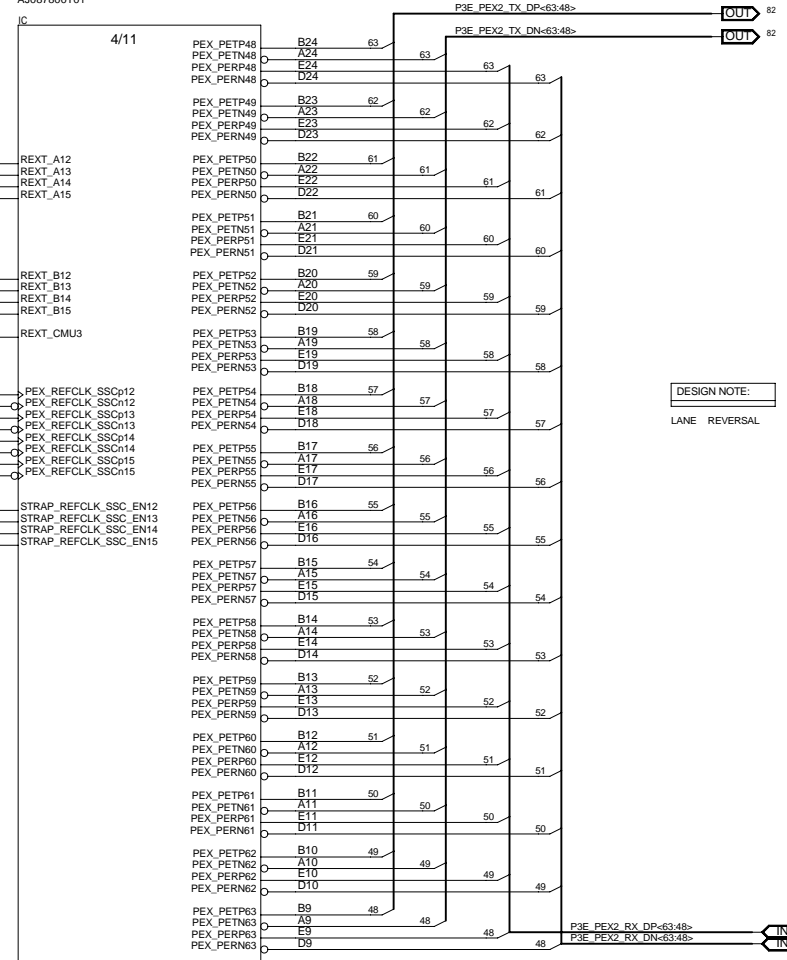
PLX TO GPU7

SMLF
PEX8780-AB80BI
U4
AJ087800T01



PLX TO GPU6

SMLF
PEX8780-AB80BI
U4
AJ087800T01



DESIGN NOTE:
LANE REVERSAL

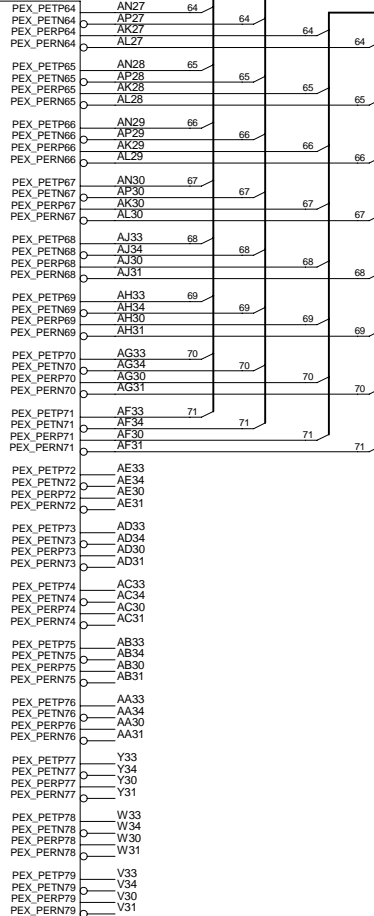
PLX TO SLOT3

PLX TO SSD2/3

SMLF
PEX8780-AB80BI
U4
AJ087800T01

IC

5/11



AG27 PEX_REFCLK_SSCp16
AH27 PEX_REFCLK_SSCn16
AE27 PEX_REFCLK_SSCp17
AE28 PEX_REFCLK_SSCn17
AB27 PEX_REFCLK_SSCp18
AB28 PEX_REFCLK_SSCn18
W27 PEX_REFCLK_SSCp19
W28 PEX_REFCLK_SSCn19

STRAP_REFCLK_SSC_EN16 Y28
STRAP_REFCLK_SSC_EN17 AP33
STRAP_REFCLK_SSC_EN18 Y27
STRAP_REFCLK_SSC_EN19 U28

R192k1 2 1% PEX2_PEXT_A16 AJ27 REXT_A16
R193k1 2 1% PEX2_PEXT_A17 AG29 REXT_A17
R194k1 2 1% PEX2_PEXT_A18 AB29 REXT_A18
R195k1 2 1% PEX2_PEXT_A19 Y29 REXT_A19

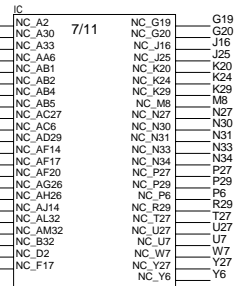
R196k1 2 1% PEX2_PEXT_B16 AJ26 REXT_B16
R197k1 2 1% PEX2_PEXT_B17 AF29 REXT_B17
R198k1 2 1% PEX2_PEXT_B18 AA29 REXT_B18
R199k1 2 1% PEX2_PEXT_B19 W29 REXT_B19

R200k1 2 1% PEX2_PEXT_CMU4AE29 REXT_CMU4

R861 1 2 10K PD PEX2_REFCLK_SSC_EN<16> Y28 STRAP_REFCLK_SSC_EN16
R862 1 2 10K PD PEX2_REFCLK_SSC_EN<17> AP33 STRAP_REFCLK_SSC_EN17
R863 1 2 10K PD PEX2_REFCLK_SSC_EN<18> Y27 STRAP_REFCLK_SSC_EN18
R864 1 2 10K PD PEX2_REFCLK_SSC_EN<19> U28 STRAP_REFCLK_SSC_EN19

SMLF
PEX8780-AB80BI
U4

AJ087800T01



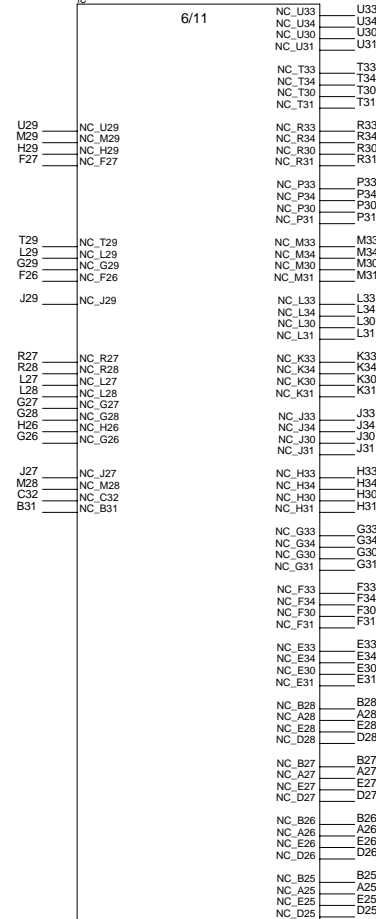
P3E_PEX2_TX_DP<71:64>
P3E_PEX2_TX_DN<71:64>
P3E_PEX2_RX_DP<71:64>
P3E_PEX2_RX_DN<71:64>

SMLF
PEX8780-AB80BI
U4

AJ087800T01

IC

6/11



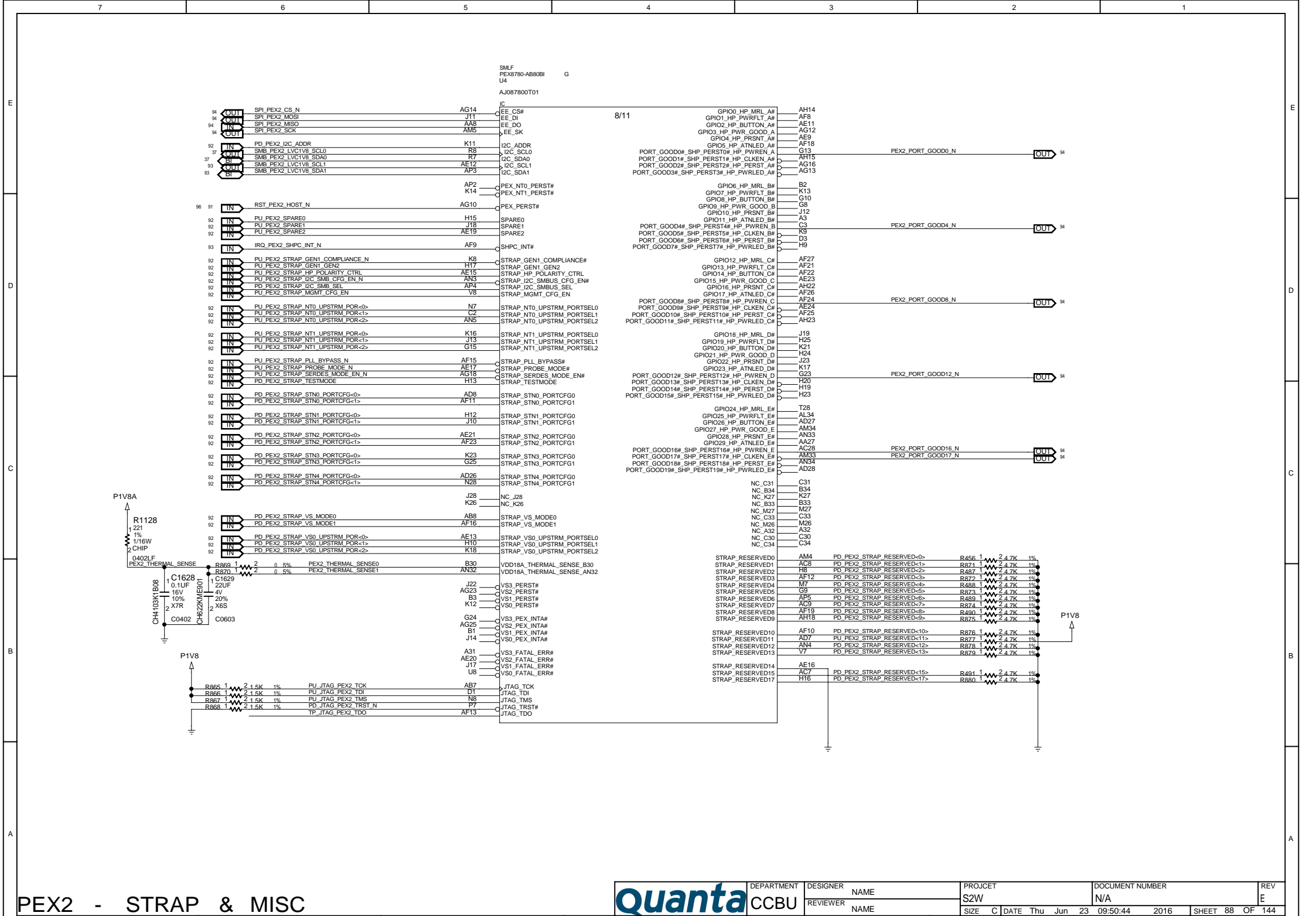
U29 NC_U29
M29 NC_M29
H29 NC_H29
F27 NC_F27

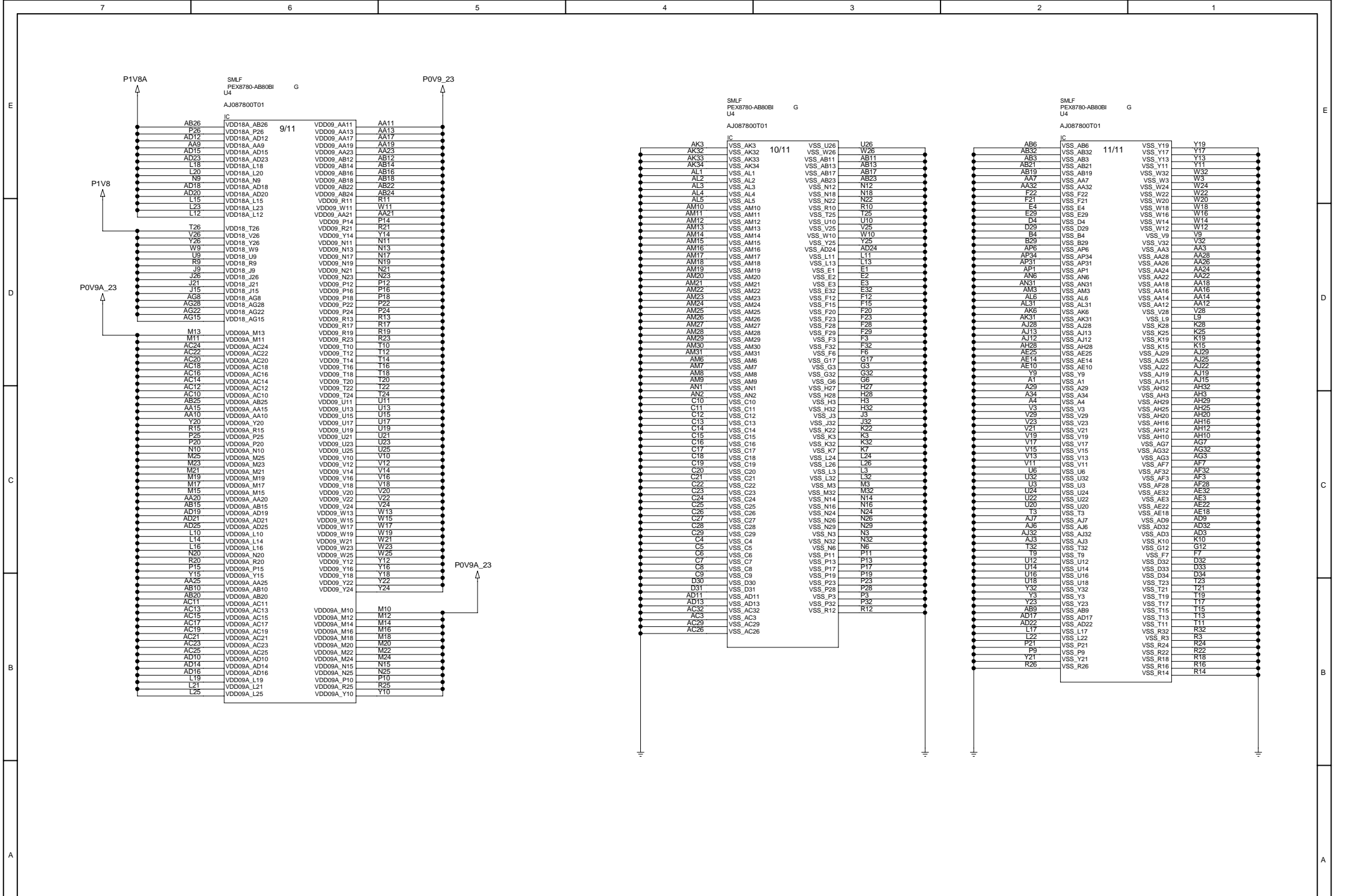
T29 NC_T29
L29 NC_L29
G29 NC_G29
F26 NC_F26

J29 NC_J29

R27 NC_R27
R28 NC_R28
L27 NC_L27
L28 NC_L28
G27 NC_G27
G28 NC_G28
H26 NC_H26
G26 NC_G26

J27 NC_J27
M28 NC_M28
C32 NC_C32
B31 NC_B31







PEX2 POWER DECOUPLING



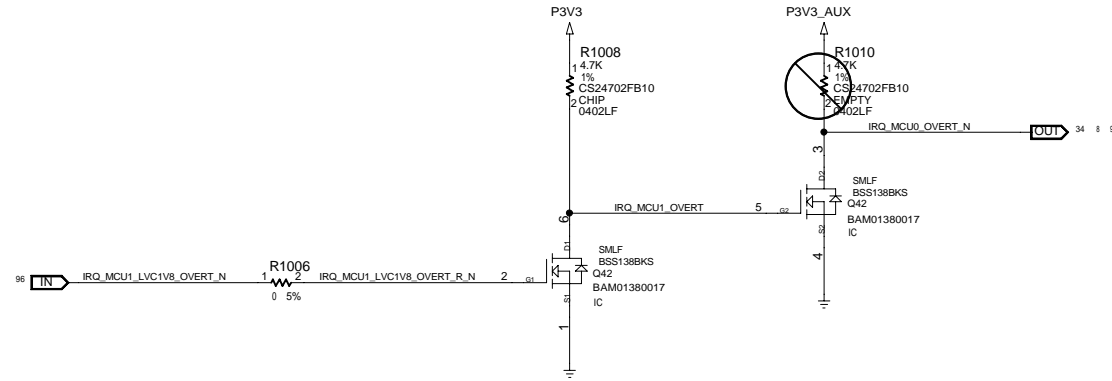
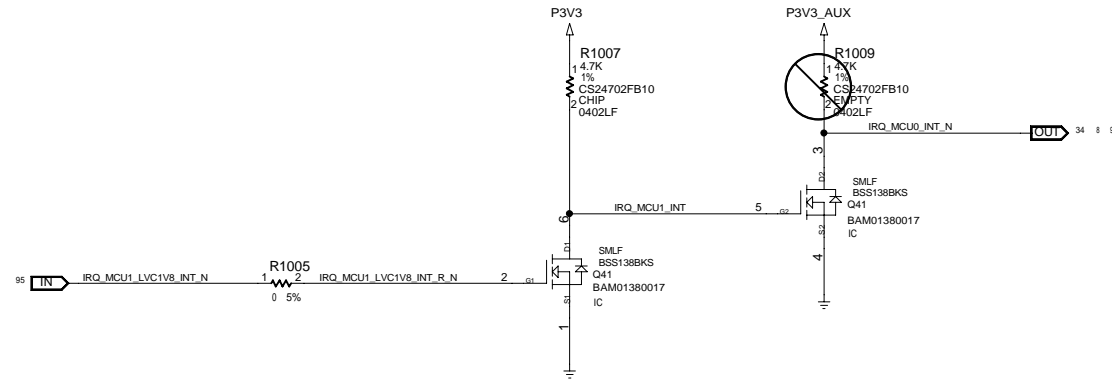
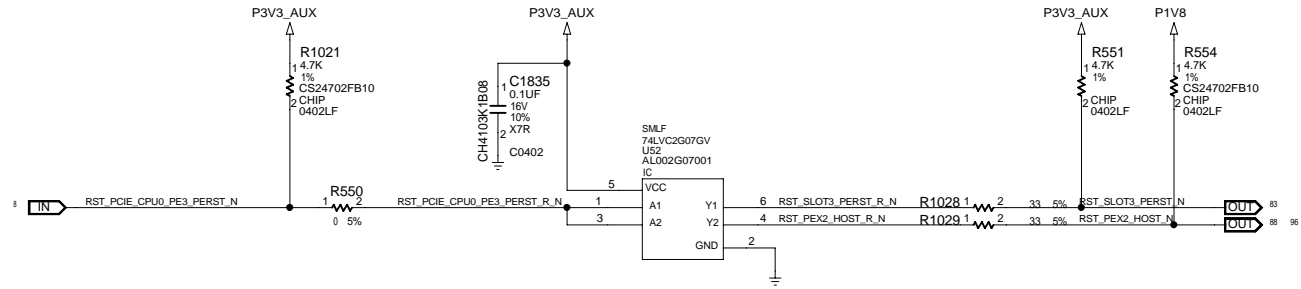
DEPARTMENT
CCBU

DESIGNER
NAME
REVIEWER
NAME

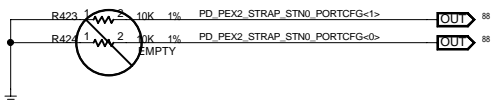
PROJCT
S2W
SIZE C DATE Thu Jun 23 09:50:39 2016

DOCUMENT NUMBER
N/A
SHEET 90 OF 144

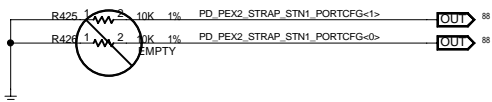
REV
E



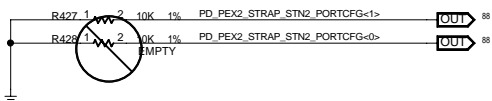
STATION0 PORT CONFIG
CONTROL THRU EEPROM
STN0: 300H[2:0]=001B=X16
STRAP_STN0_PORTCFG[1:0]=0Z=X16



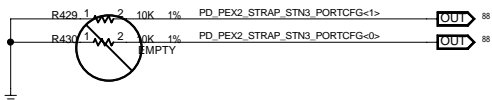
STATION1 PORT CONFIG
CONTROL THRU EEPROM
STN1: 300H[5:3]=001B=X16
STRAP_STN1_PORTCFG[1:0]=0Z=X16



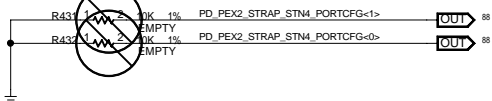
STATION2 PORT CONFIG
CONTROL THRU EEPROM
STN2: 300H[8:6]=001B=X16
STRAP_STN2_PORTCFG[1:0]=0Z=X16



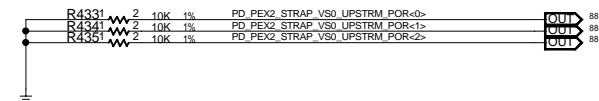
STATION3 PORT CONFIG
CONTROL THRU EEPROM
STN3: 300H[11:9]=001B=X16
STRAP_STN3_PORTCFG[1:0]=0Z=X16



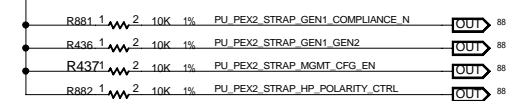
STATION4 PORT CONFIG
CONTROL THRU EEPROM
STN4: 300H[14:12]=004B=X4X4X4X4
STRAP_STN4_PORTCFG[1:0]=ZZ=X4X4X4X4



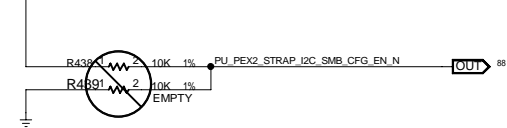
UPSTREAM PORT SELECT
CONTROL THRU EEPROM
360H[4:0]=0_0000B=PORT 0
STRAP_UPSTRM_PORTSEL[2:0]=000=PORT 0



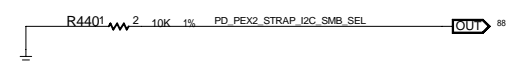
P1V8
1=PCIE MAX DATA RATE =GEN3
1=MANAGEMENT PORT IS DISABLED



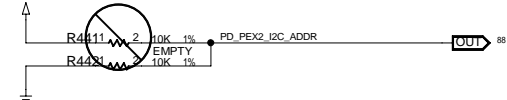
P1V8
STRAP_I2C_SMBUS_CFG_EN#1=DISABLE I2C INITIAL



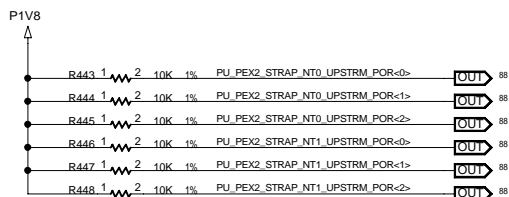
STRAP_I2C_SMBUS_SEL=0=ENABLE I2C SLAVE PROTOCOL



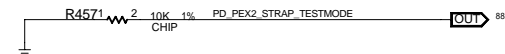
P1V8
I2C_ADDR=0=1011_101B



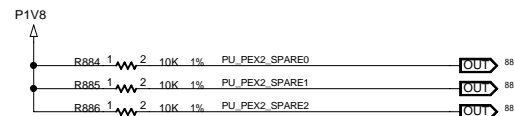
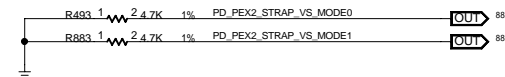
STRAP_NT_UPSTRM_POR<0:2> =111= DISABLE NT MODE



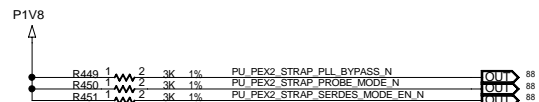
BASE MODE: TEST_MODE=0
=PORT_GOODX# + GPIOX INPUT

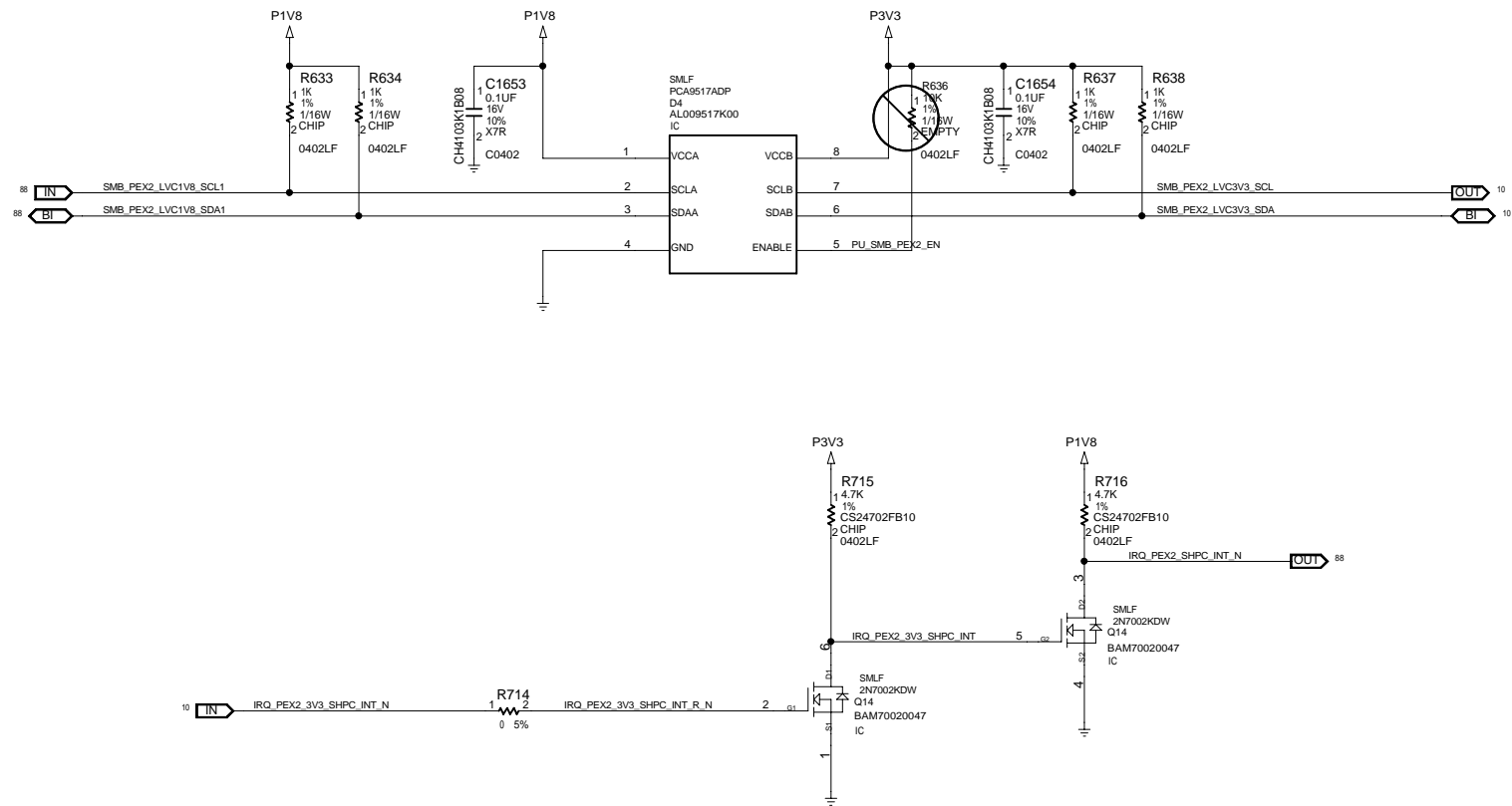


BASE MODE: LL(00)=SINGLE SWITCH



FOR FACTORY TEST ONLY





PEX2 EEPROM & PORT LED



DEPARTMENT
CCBU

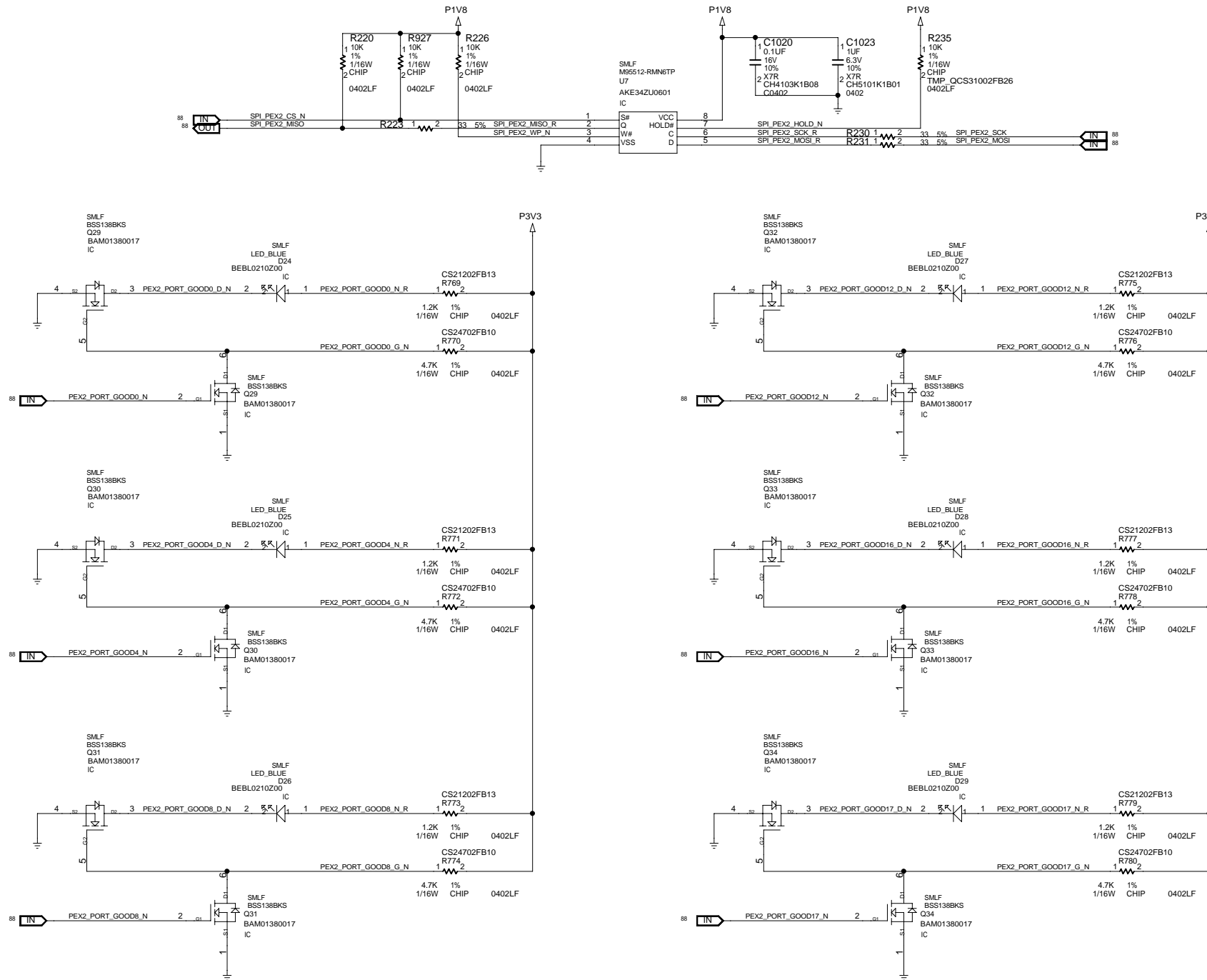
DESIGNER NAME
REVIEWER NAME

PROJCT
S2W

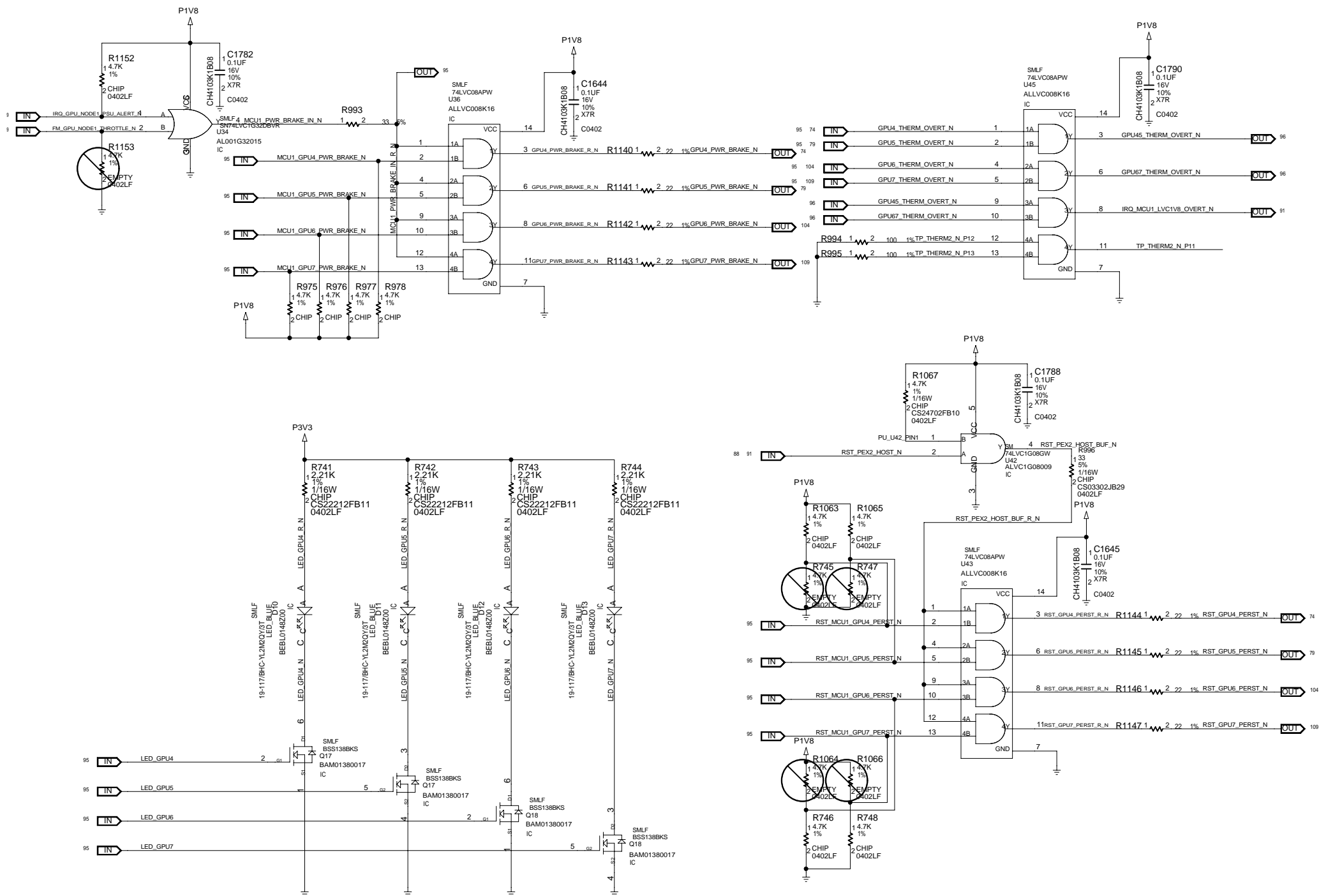
DOCUMENT NUMBER
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REV
E

SIZE C DATE Thu Jun 23 09:50:53 2016 SHEET 94 OF 144







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E							
D							
C							
B							
A							
UNTITLED				<div><div>Quanta</div><div>DEPARTMENT CCBU</div><div>DESIGNER NAME</div><div>REVIEWER NAME</div></div> <div><div>PROJCET S2W</div><div>DOCUMENT NUMBER N/A</div><div>SIZE C</div><div>DATE Thu Jul 23 11:27:26 2015</div><div>SHEET 97 OF 144</div></div> <div>REV E</div>			

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E							
D							
C							
B							
A							
UNTITLED				<div><div>Quanta</div><div>DEPARTMENT CCBU</div></div>			
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				REVIEWER NAME		SIZE C	DATE Thu Jul 23 11:27:26 2015
						SHEET 98 OF 144	

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UNTITLED



DEPARTMENT

CCBU

DESIGNER

NAME

REVIEWER

NAME

PROJCT

S2W

DOCUMENT NUMBER

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REV

E

SIZE	C	DATE	Thu	Jul	23
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2015 SHEET 99 OF 144

7

6

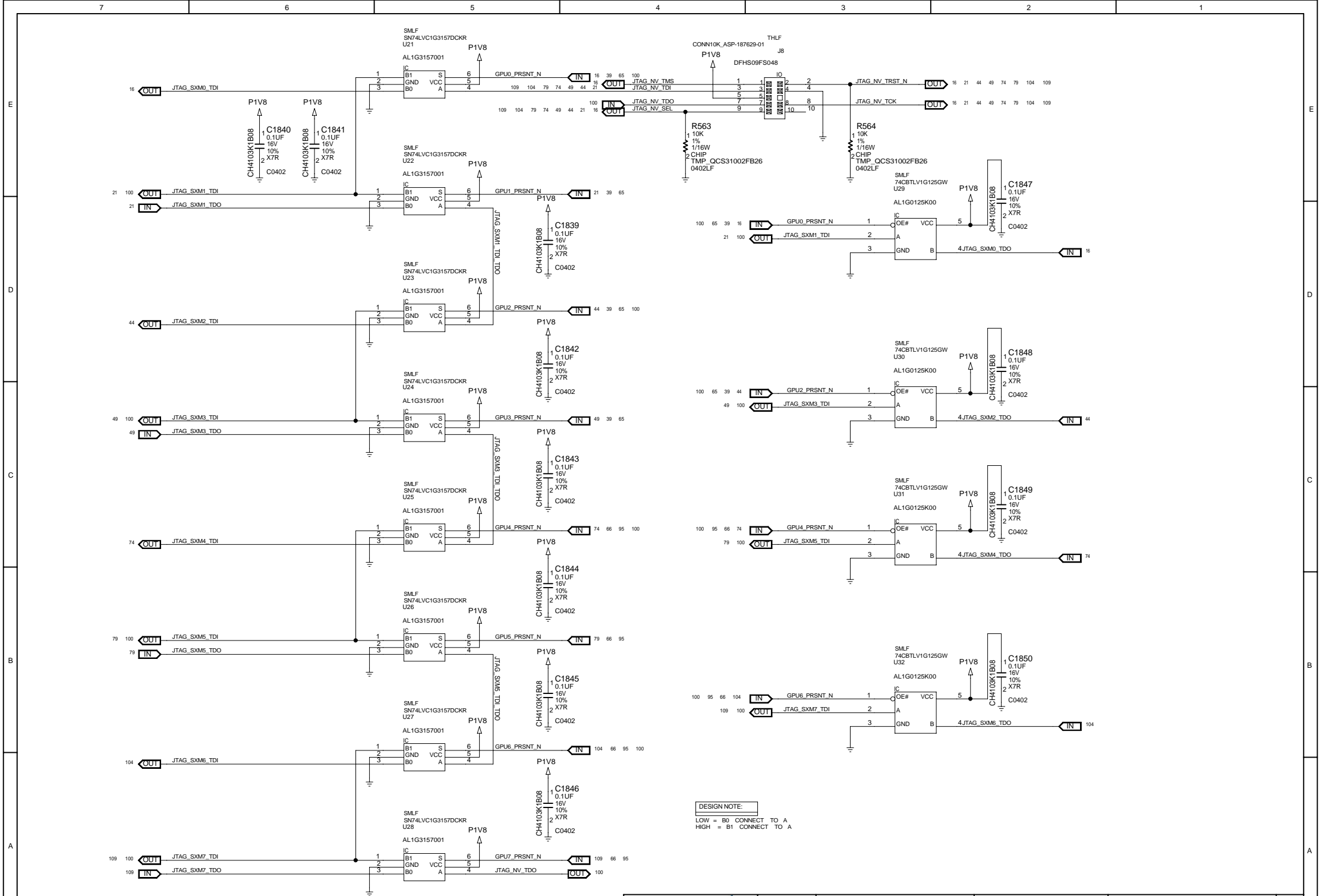
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NV SXM2 JTAG



DEPARTMENT	DESIGNER	NAME	PROJECT	DOCUMENT NUMBER	REV
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			SIZE	C	DATE
			Thu	Jun	23
			09:50:51	2016	SHEET
			100	OF	144

7

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UNTITLED



DEPARTMENT

CCBU

DESIGNER

NAME

REVIEWER

NAME

PROJECT

— S2W

DOCUMENT NUMBER

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REV

E

SIZE	C	DATE	Thu	Jul	23
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2015	SHEET 101 OF 144
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7

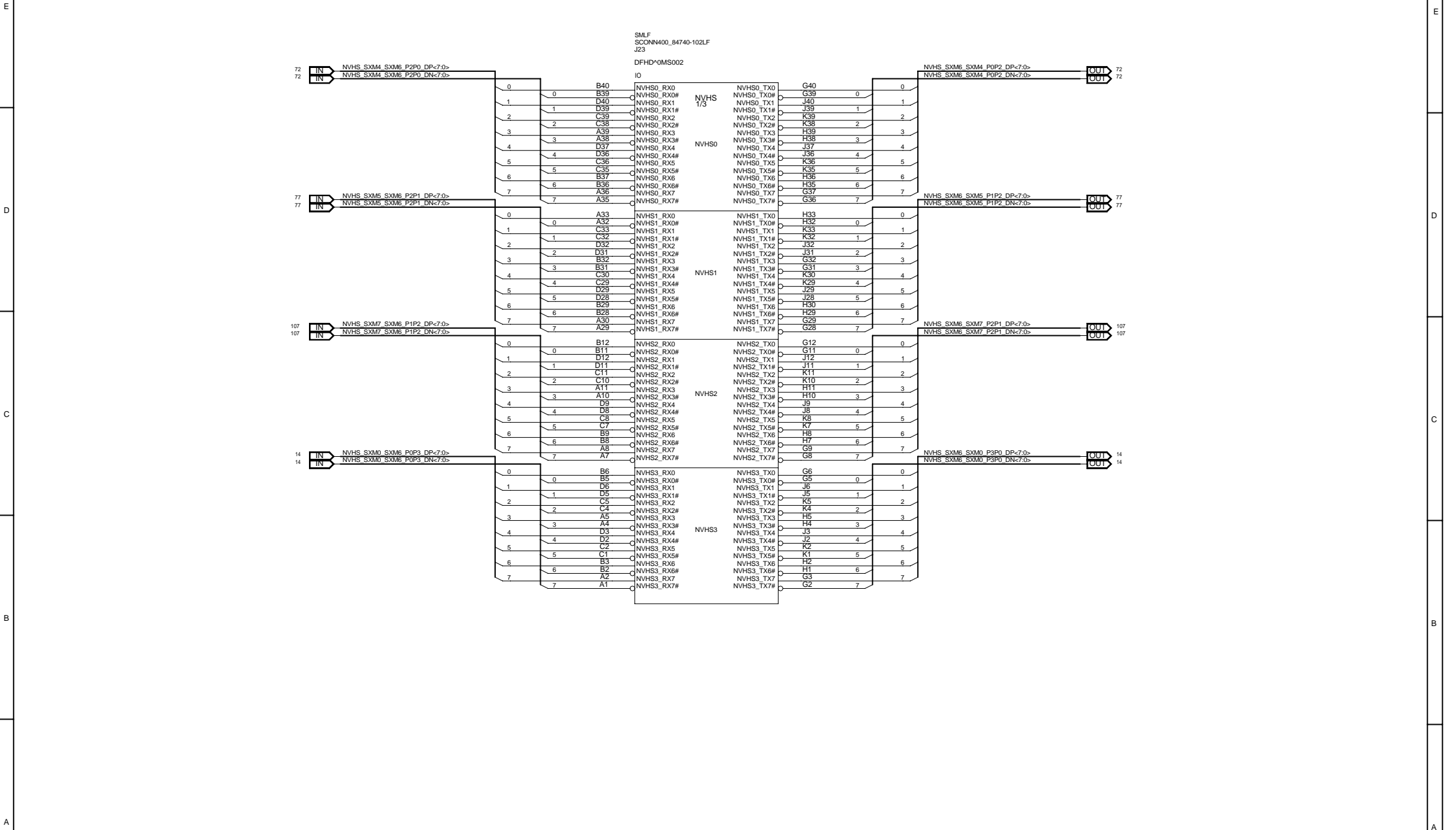
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DEPARTMENT
CCBU

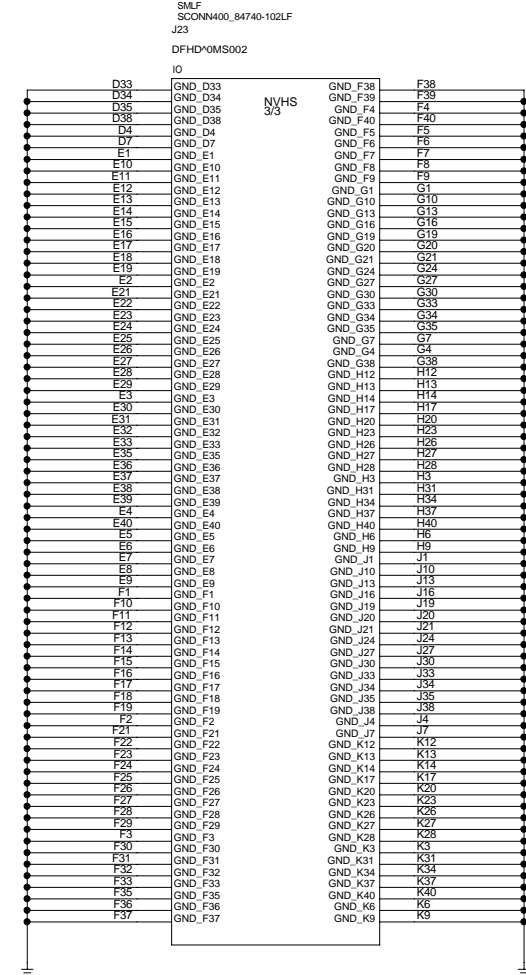
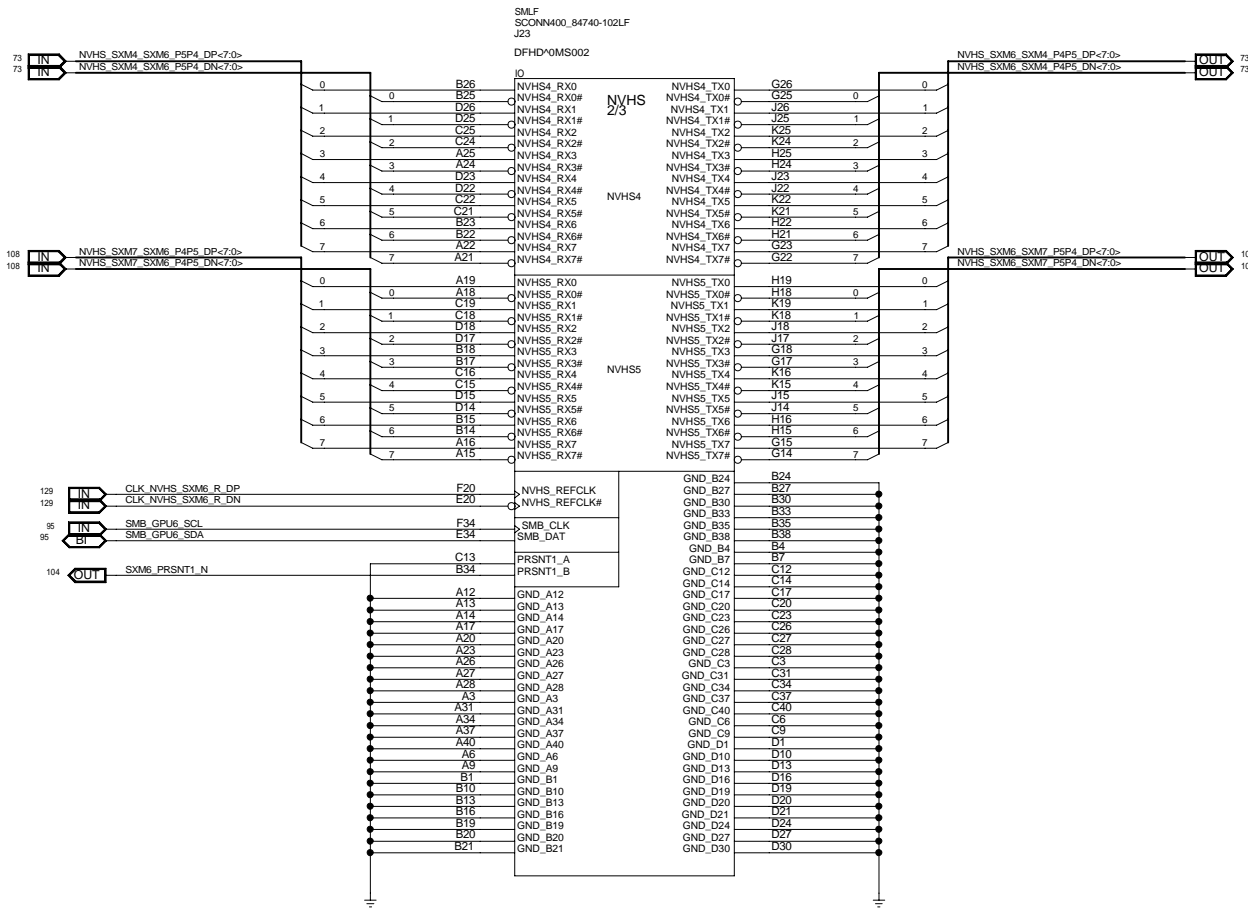
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REVIEWER NAME

PROJECT
S2W

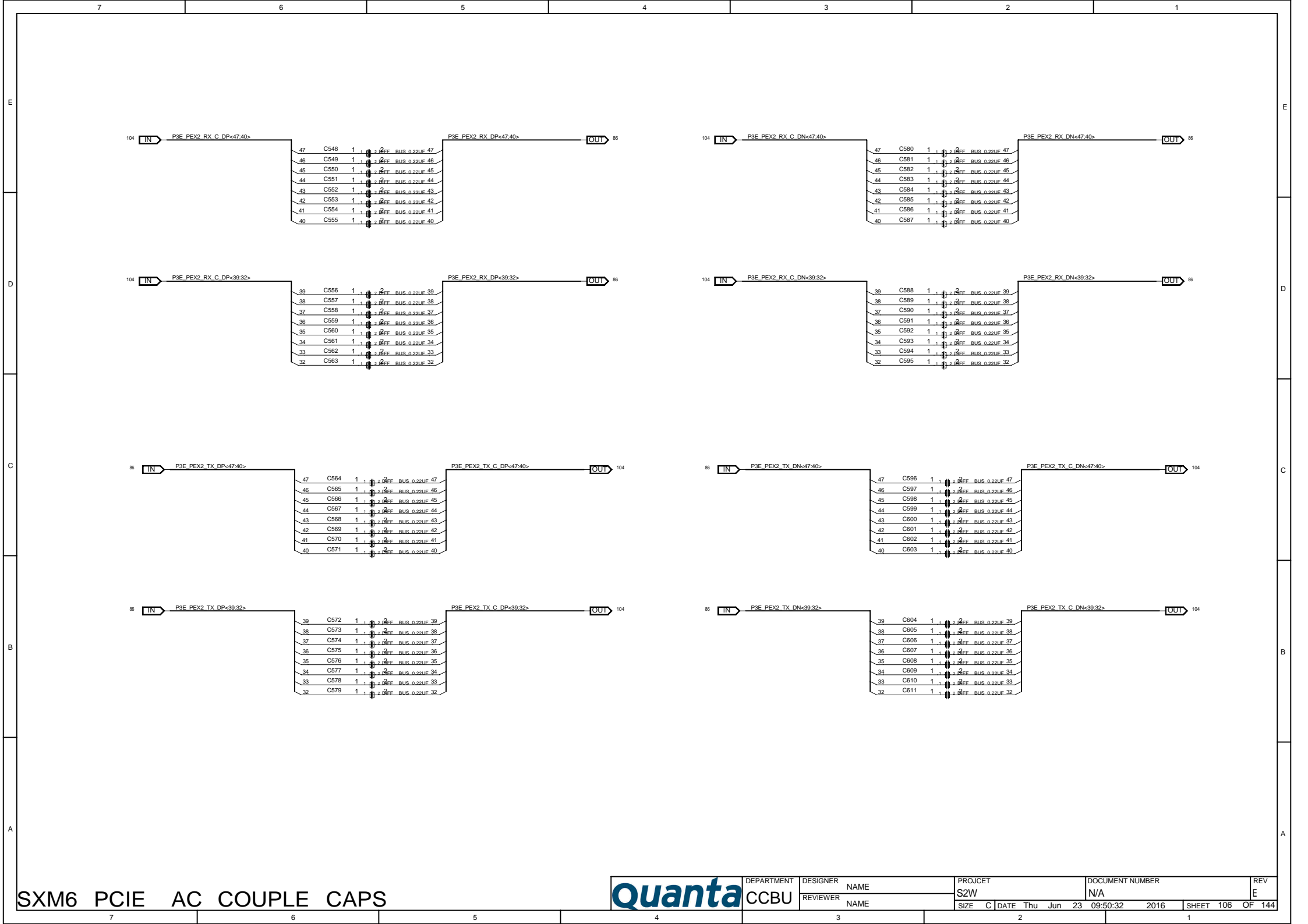
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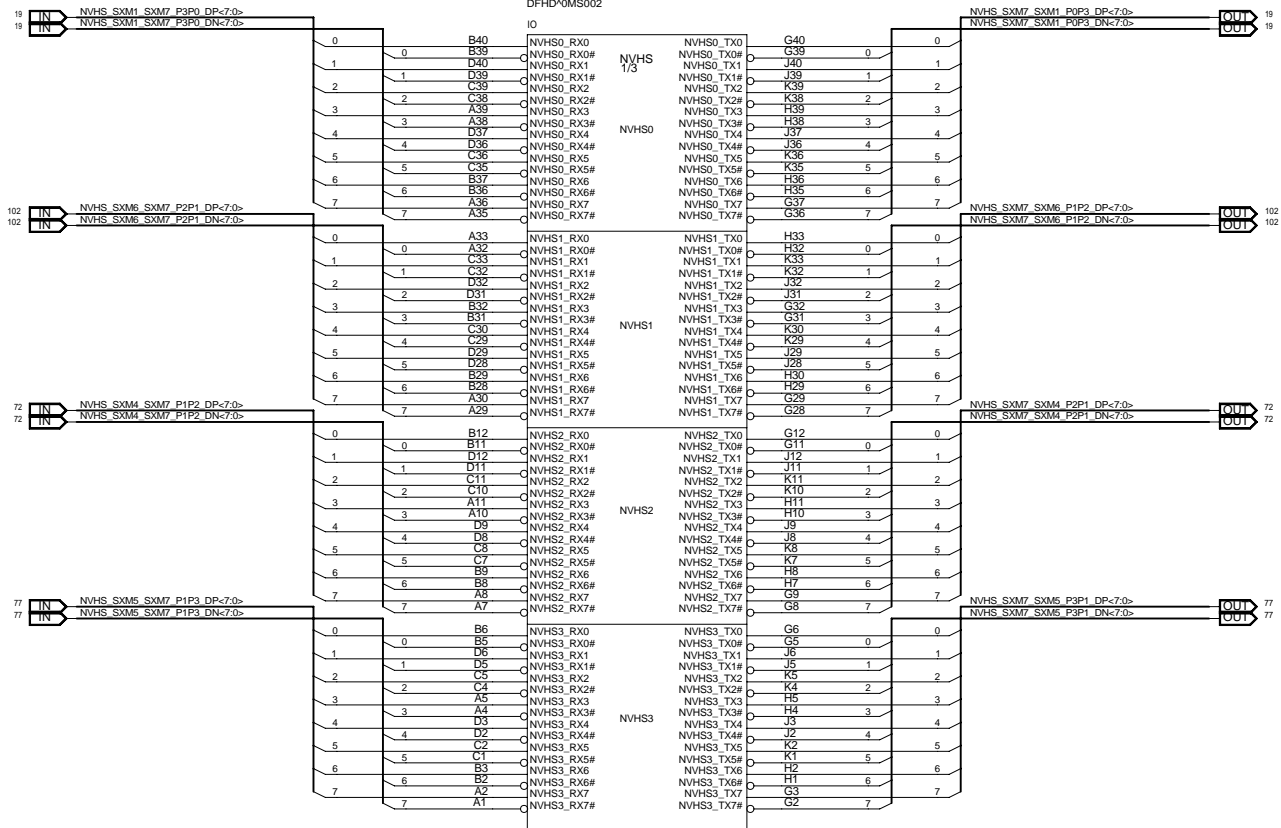
SIZE C DATE Thu Jun 23 2016 SHEET 102 OF 144







SMLF
SCONN400_84740-102LF
J25
DFHD*0MS002



DEPARTMENT
CCBU

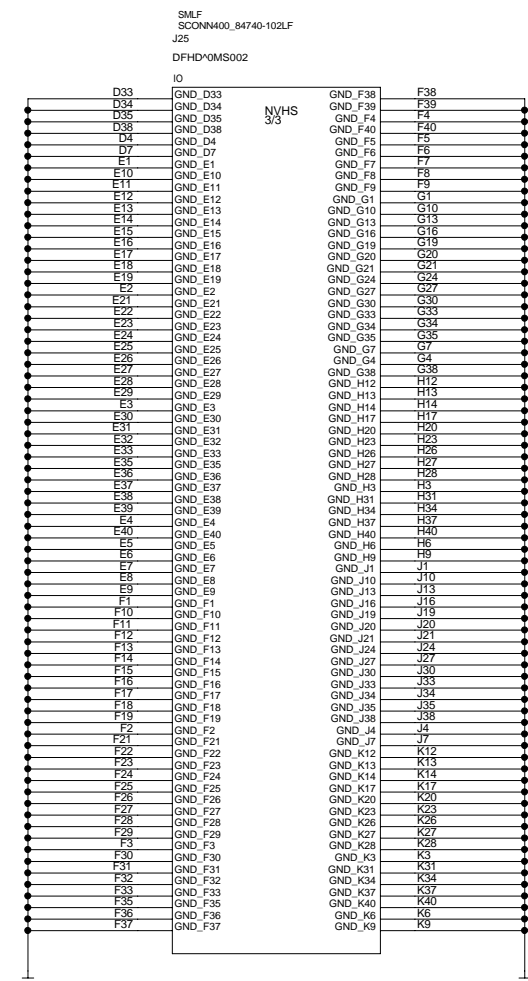
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REVIEWER NAME

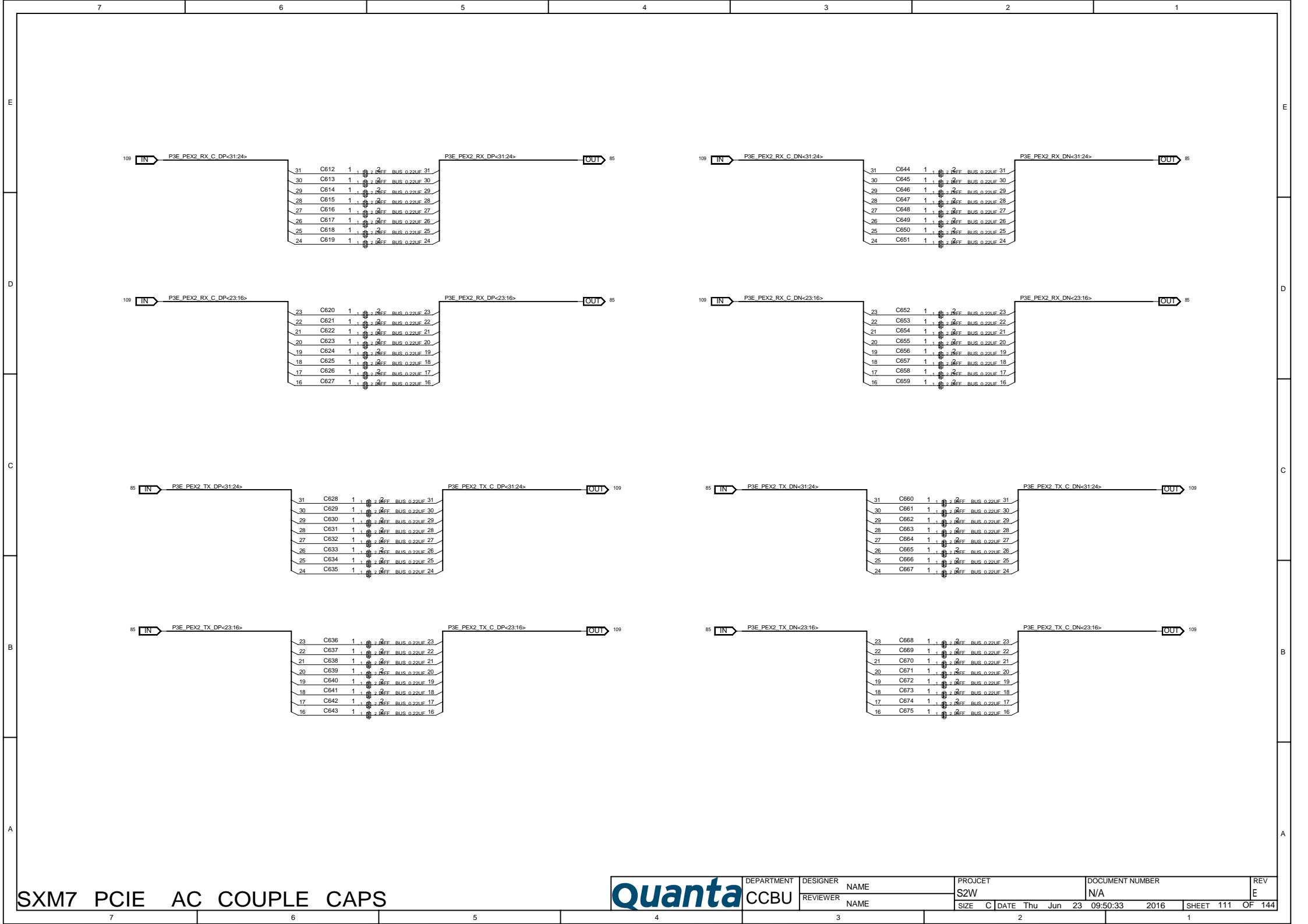
PROJECT
S2W

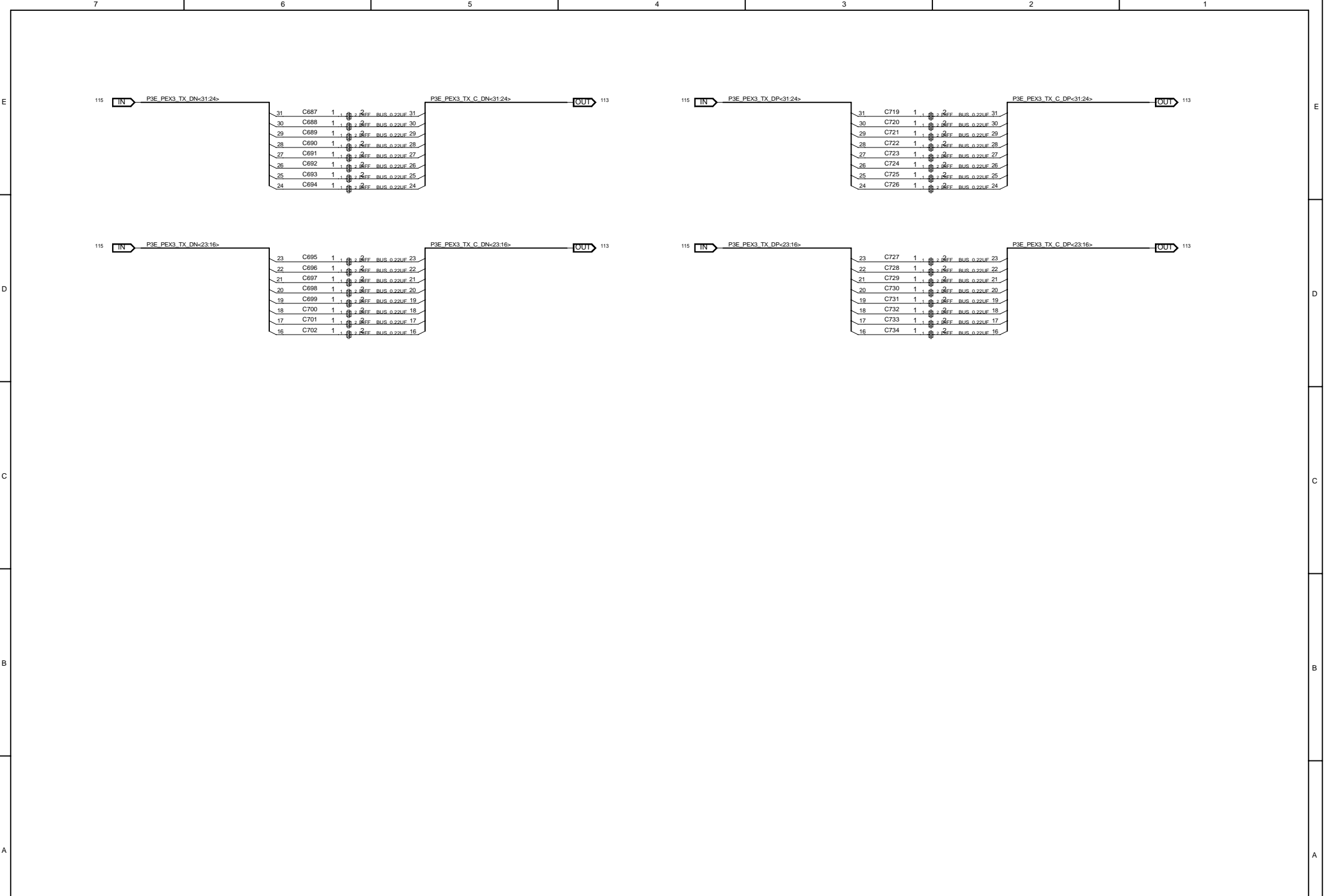
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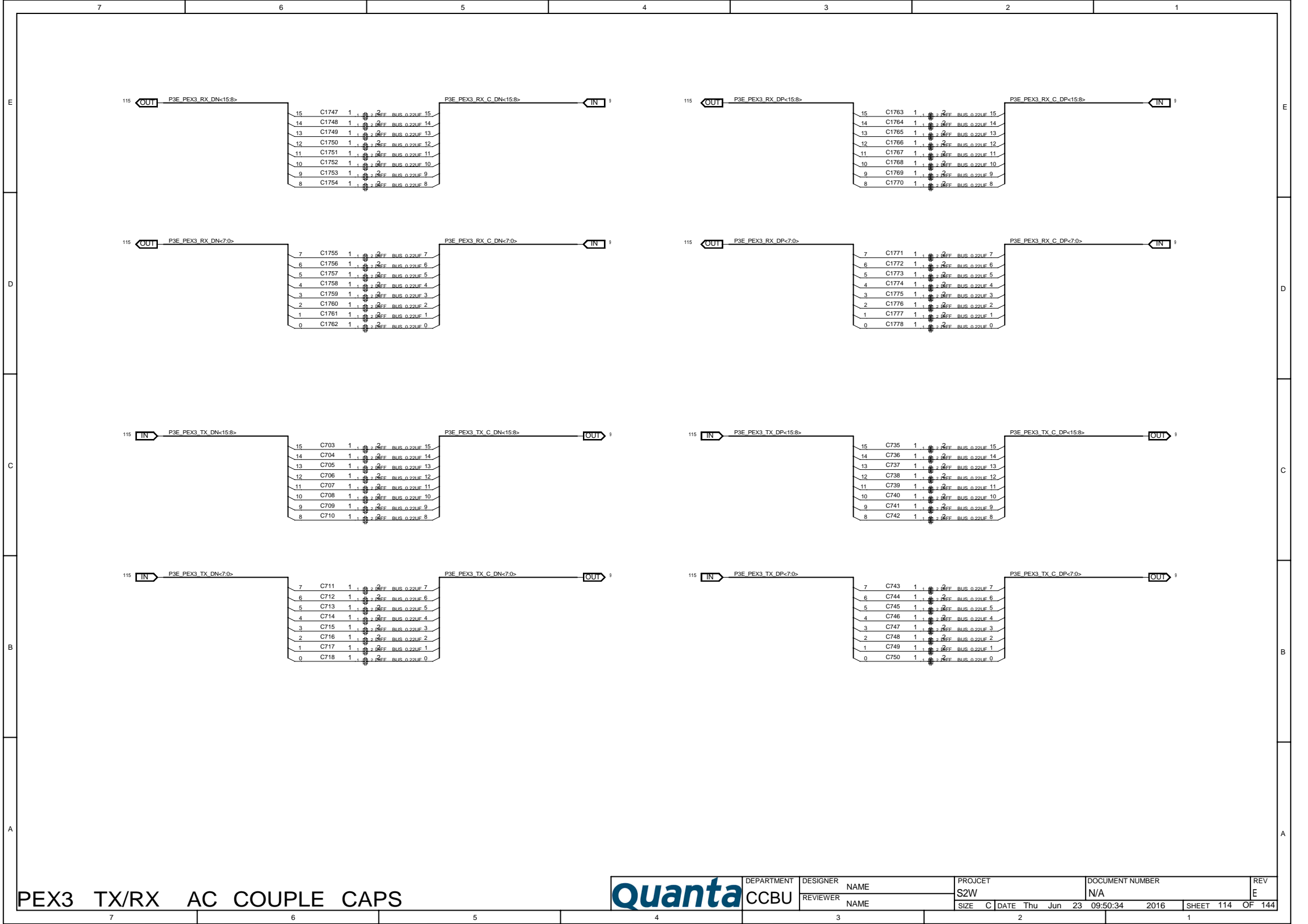
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SIZE C DATE Thu Jun 23 09:50:37 2016 SHEET 107 OF 144

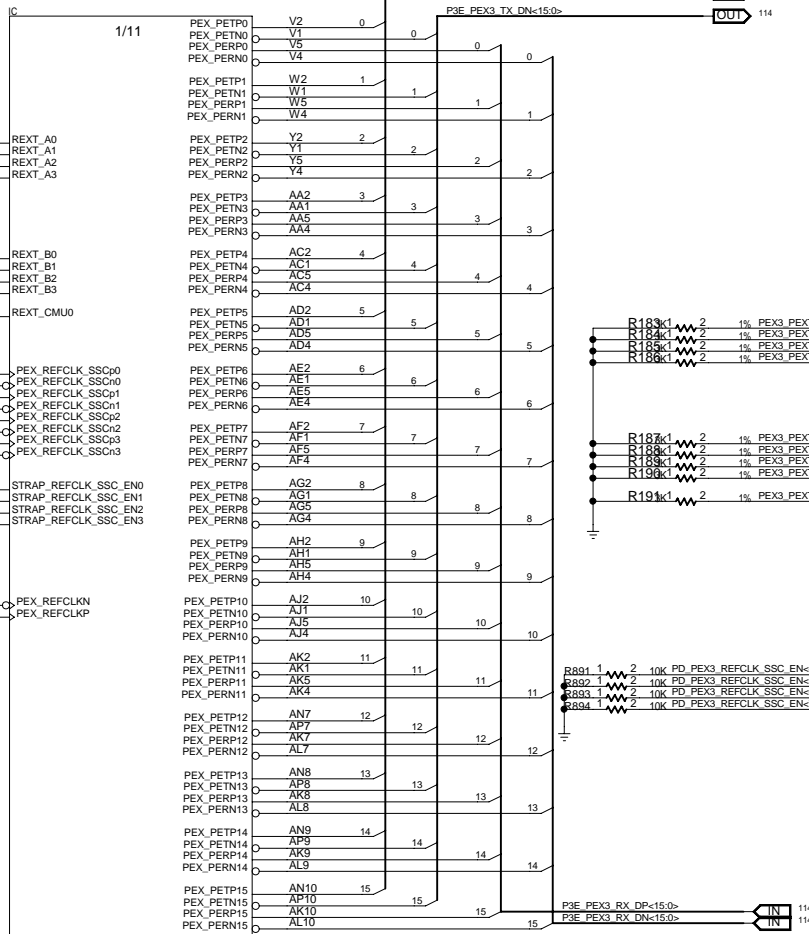




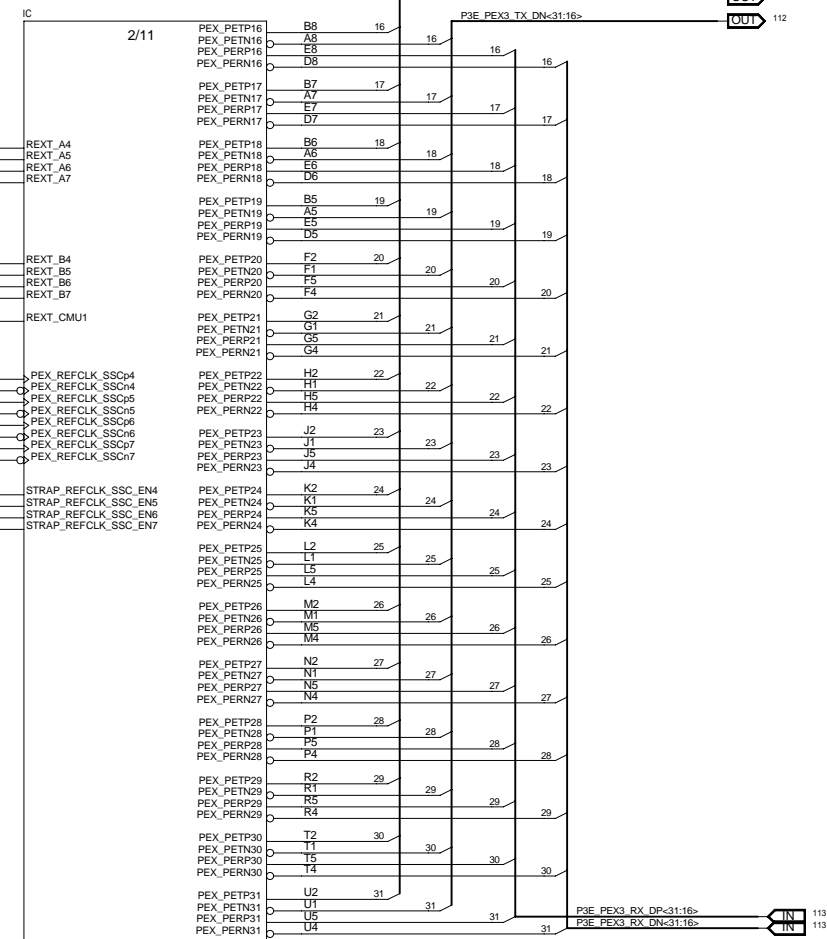




SMLF
PEX8764-AB80BI
U5
AJ087640T01



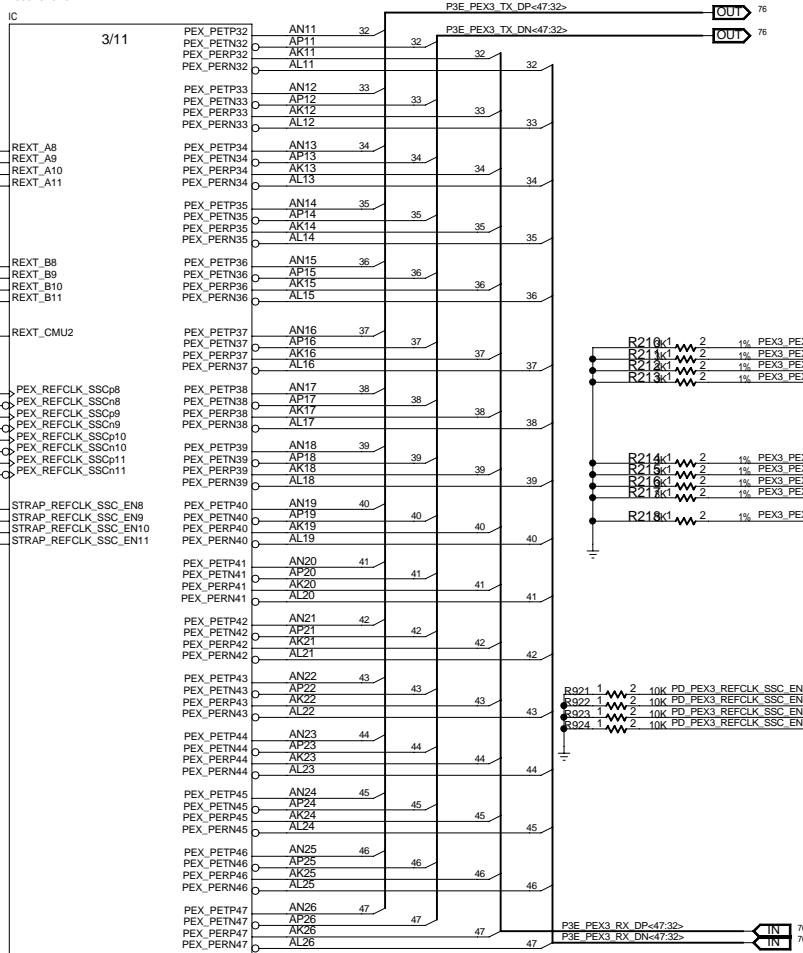
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PEX8764-AB80BI
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AJ087640T01



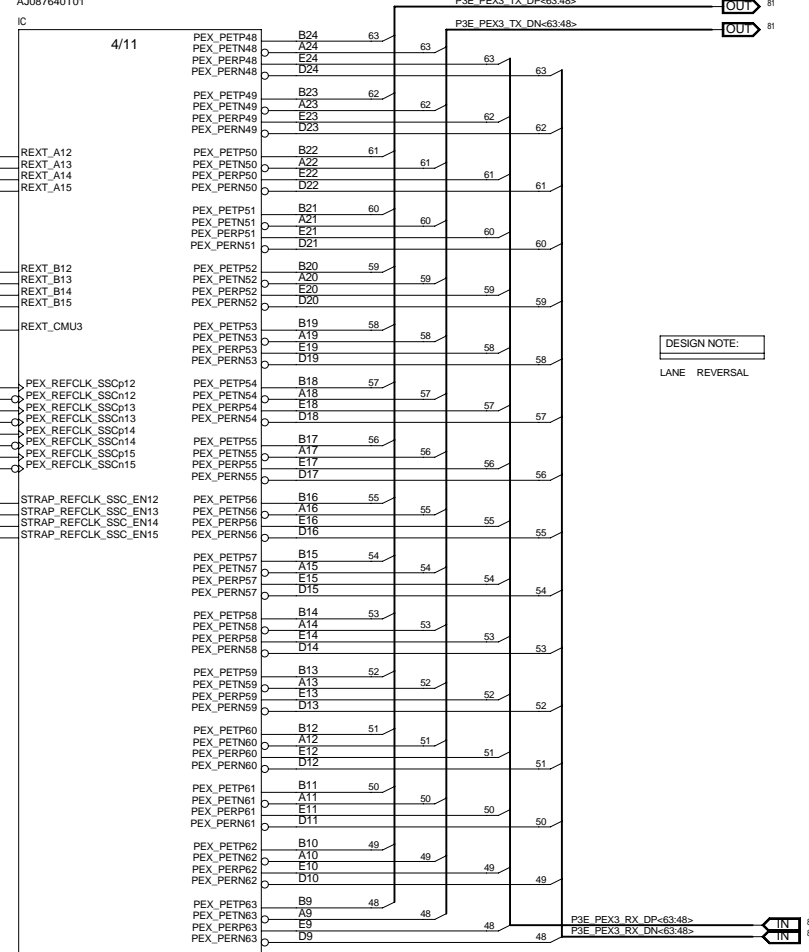
PLX TO CPU

PLX TO SLOT4

SMLF
PEX8764-AB80BI
US
AJ087640T01



SMLF
PEX8764-AB80BI
US
AJ087640T01

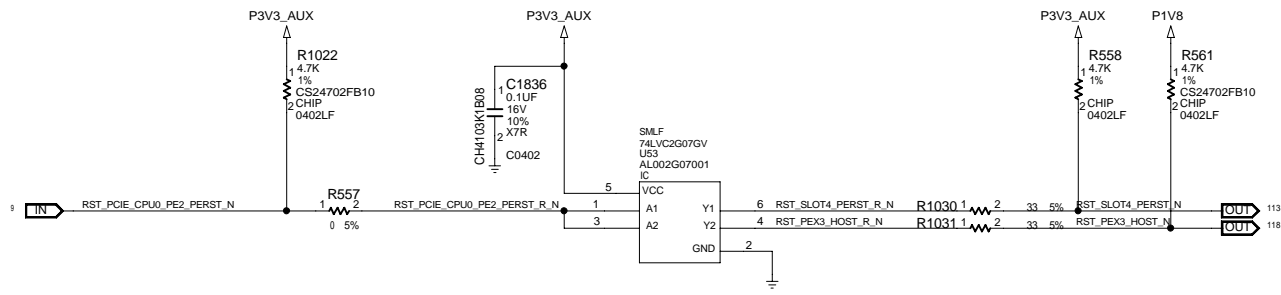


DESIGN NOTE:
LANE REVERSAL

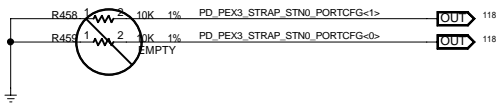
PLX TO GPU4

PLX TO GPU5

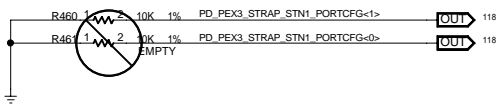




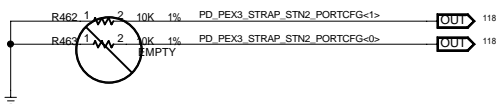
STATION0 PORT CONFIG
CONTROL THRU EEPROM
STN0: 300H[2:0]=001B=X16
STRAP_STN0_PORTCFG[1:0]=0Z=X16



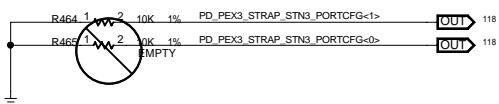
STATION1 PORT CONFIG
CONTROL THRU EEPROM
STN1: 300H[5:3]=001B=X16
STRAP_STN1_PORTCFG[1:0]=0Z=X16



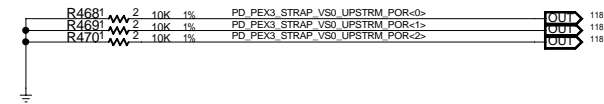
STATION2 PORT CONFIG
CONTROL THRU EEPROM
STN2: 300H[8:6]=001B=X16
STRAP_STN2_PORTCFG[1:0]=0Z=X16



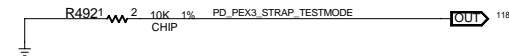
STATION3 PORT CONFIG
CONTROL THRU EEPROM
STN3: 300H[11:9]=001B=X16
STRAP_STN3_PORTCFG[1:0]=0Z=X16



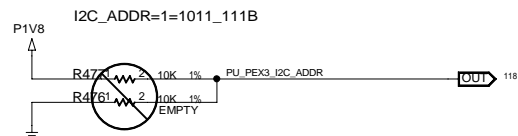
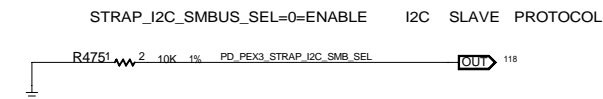
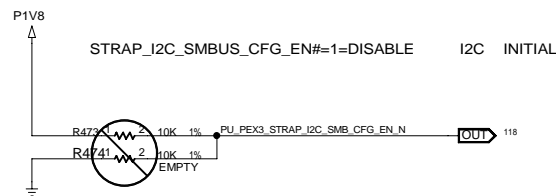
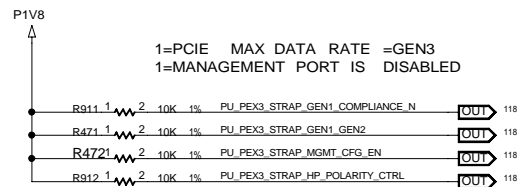
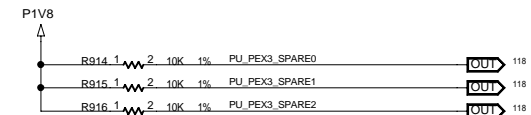
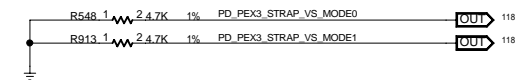
UPSTREAM PORT SELECT
CONTROL THRU EEPROM
360H[4:0]=0_0000B=PORT 0
STRAP_UPSTRM_PORTSEL[2:0]=000=PORT 0



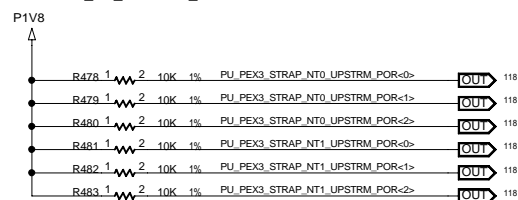
BASE MODE: TEST MODE=0
=PORT_GOODX# + GPIOX INPUT



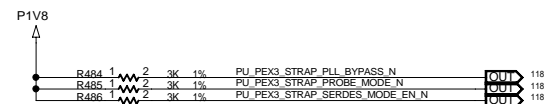
BASE MODE: LL(00)=SINGLE SWITCH



STRAP_NT_UPSTRM_POR<0:2> =111= DISABLE NT MODE



FOR FACTORY TEST ONLY



PEX3 EEPROM & PORT LED



DEPARTMENT
CCBU

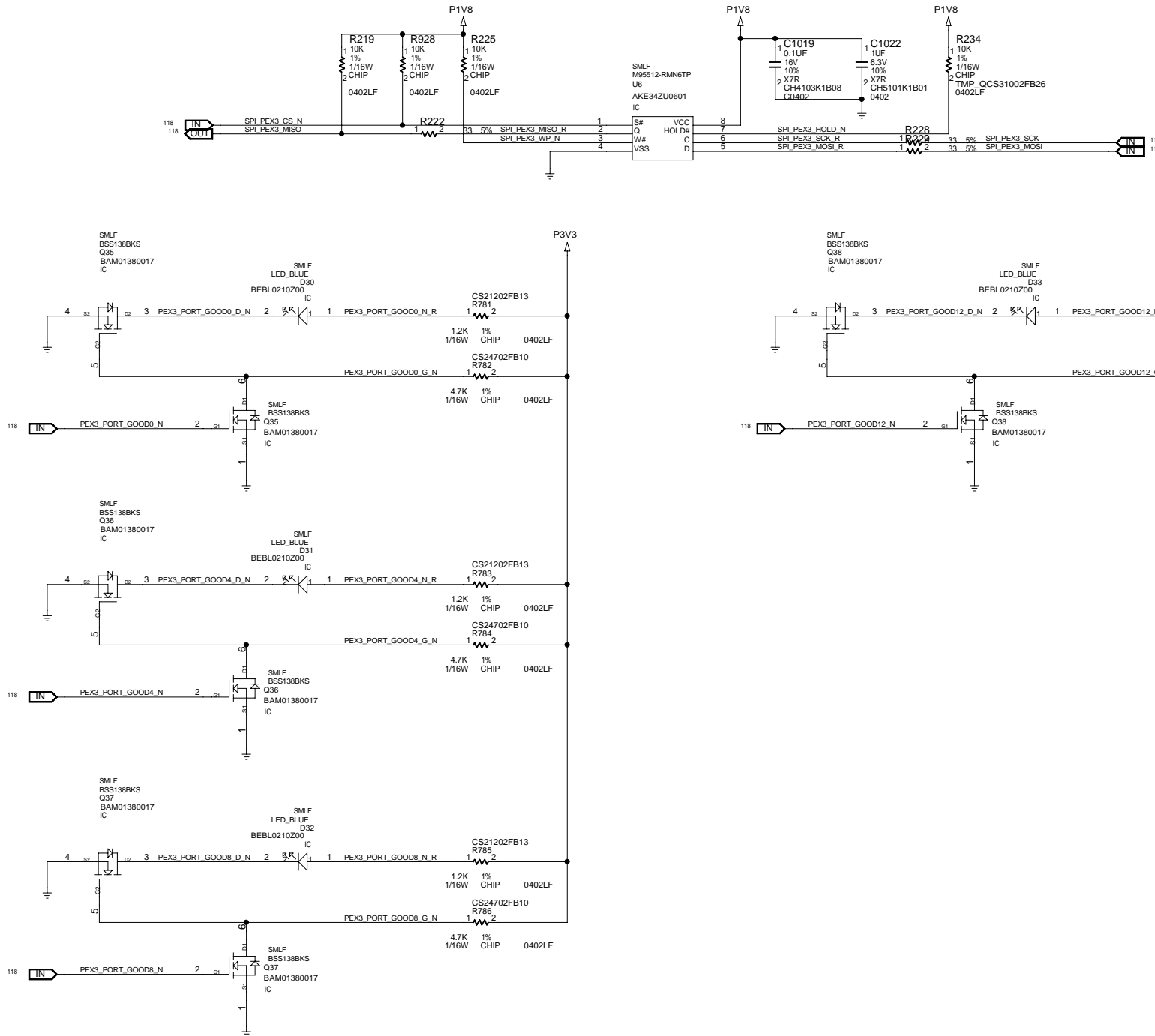
DESIGNER NAME
REVIEWER NAME

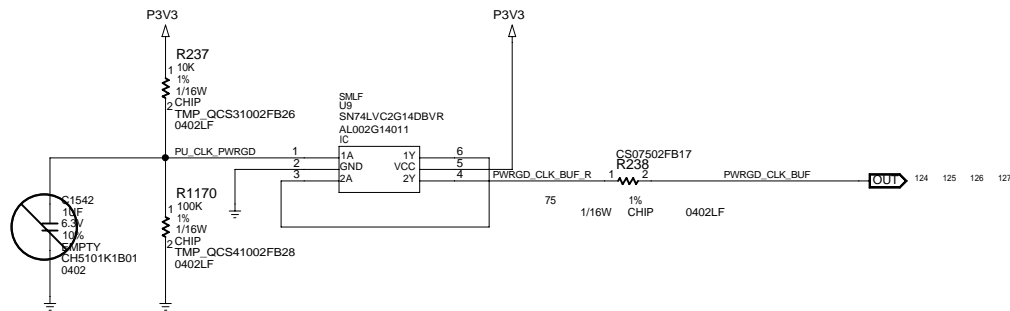
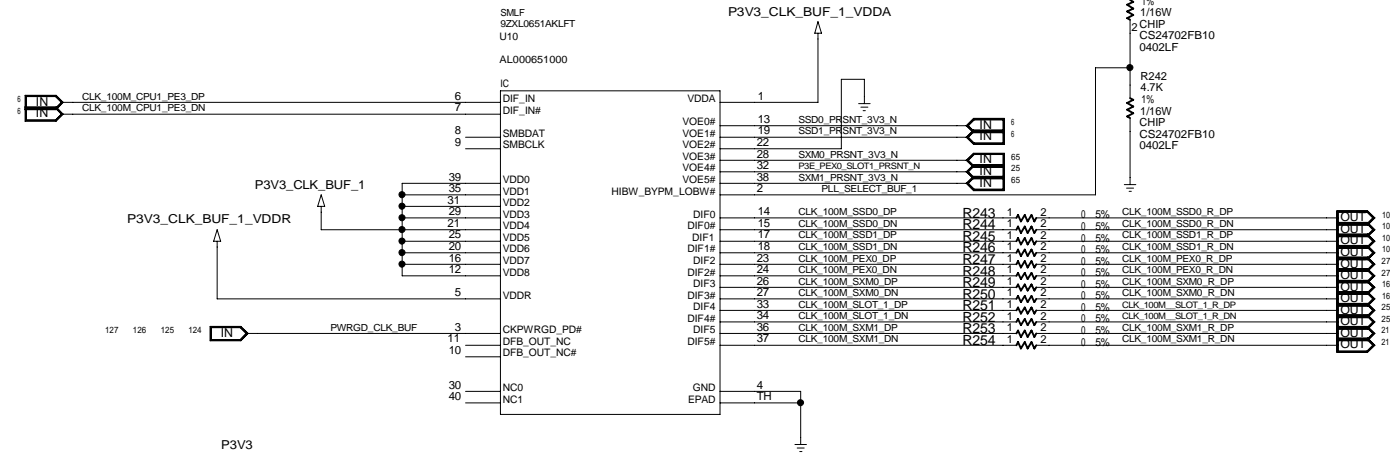
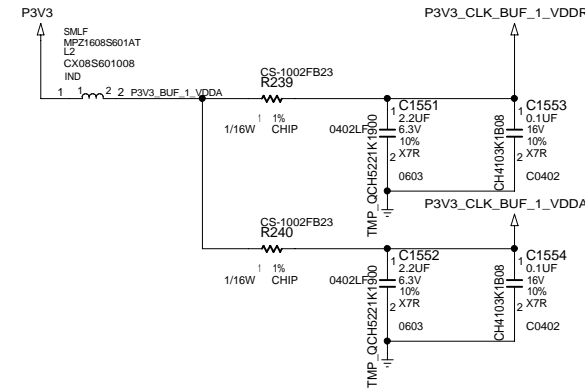
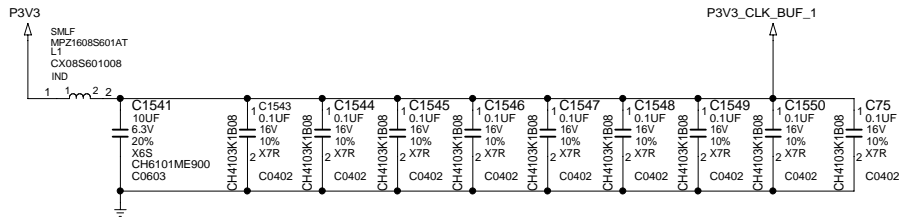
PROJCT
S2W

DOCUMENT NUMBER
N/A

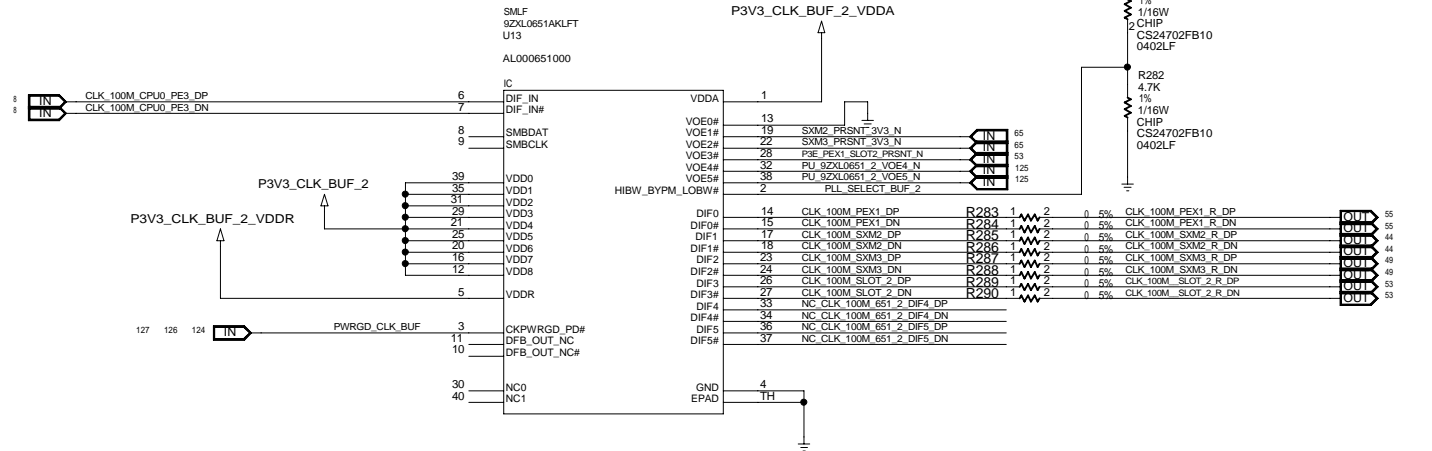
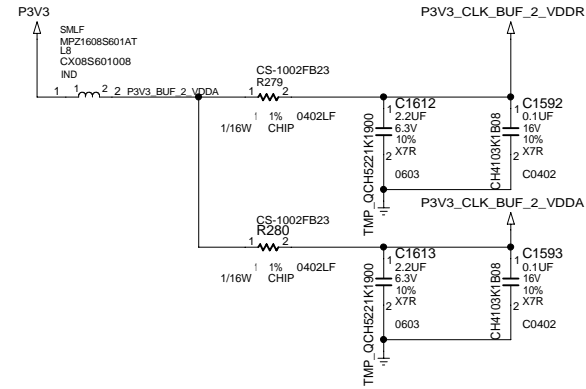
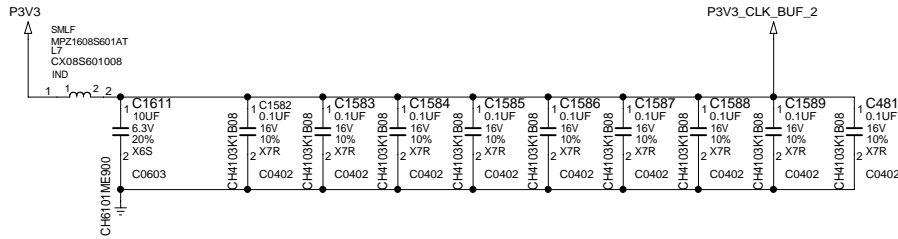
REV
E

SIZE C DATE Thu Jun 23 09:50:53 2016 SHEET 123 OF 144

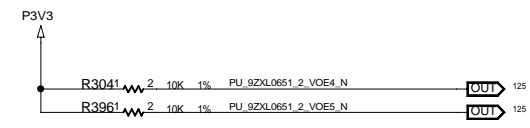




DESIGN NOTE:
BYPASS MODE



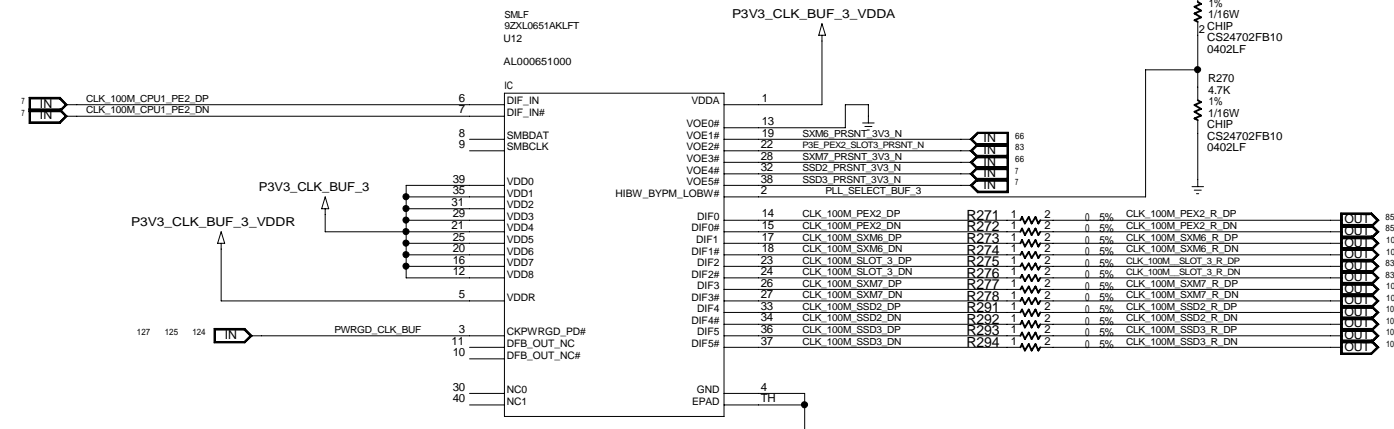
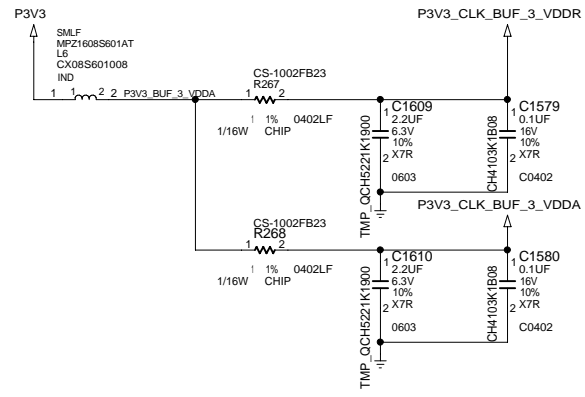
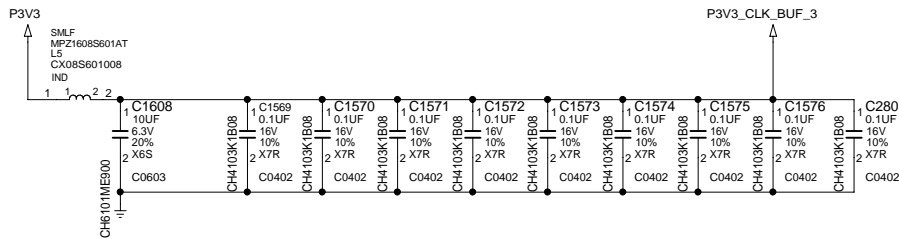
DESIGN NOTE:
BYPASS MODE



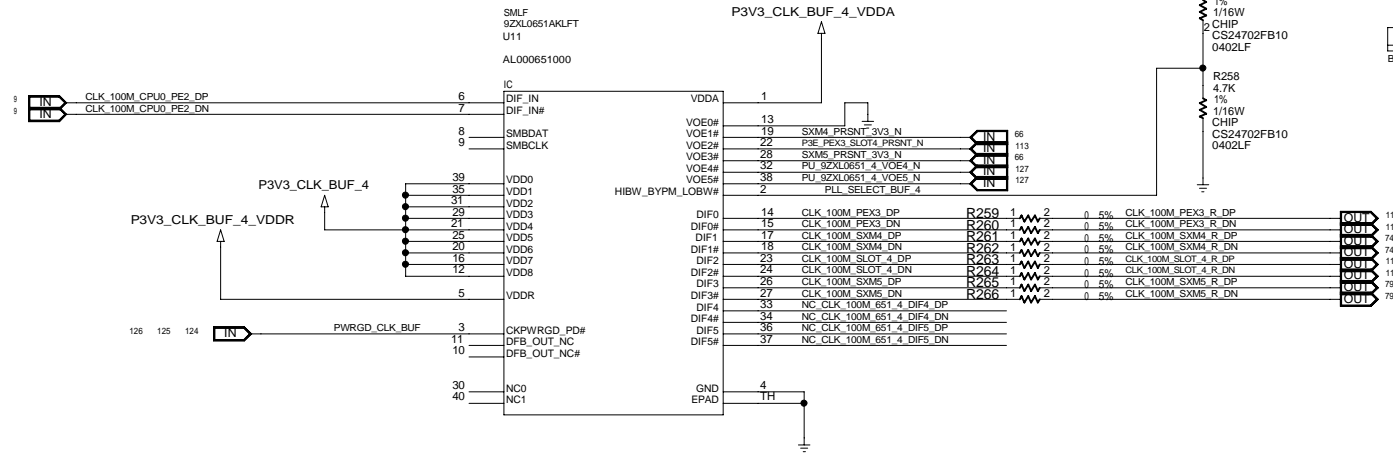
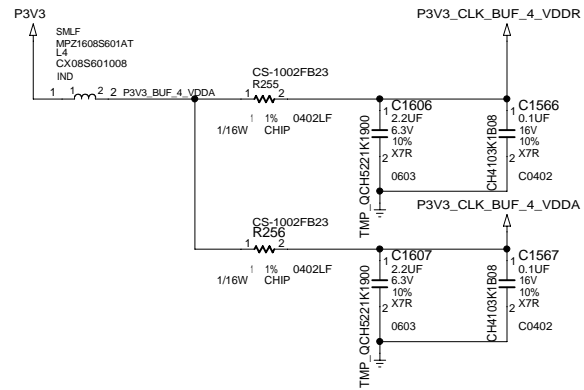
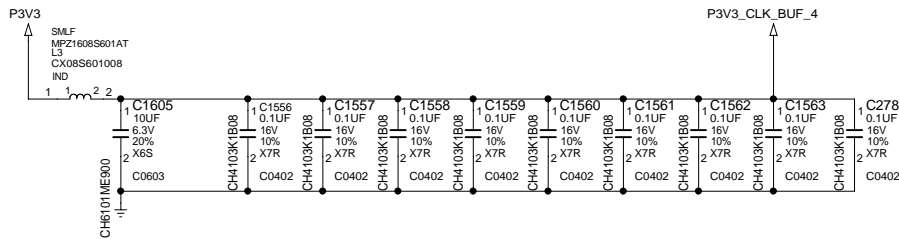
CLOCK BUFFER - PEX1



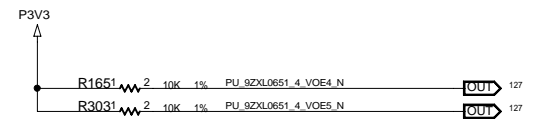
DEPARTMENT	DESIGNER	NAME	PROJECT	DOCUMENT NUMBER	REV
CCBU	REVIEWER	NAME	S2W	N/A	E
			SIZE	C	DATE
			Thu	Jun	23
			09:50:37	2016	SHEET
			125	OF	144



DESIGN NOTE:
BYPASS MODE



DESIGN NOTE:
BYPASS MODE



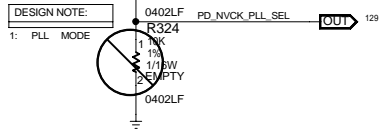
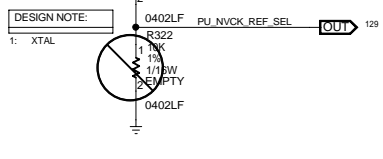
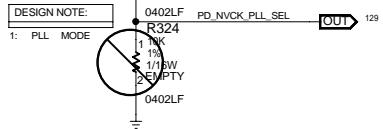
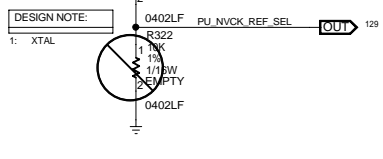
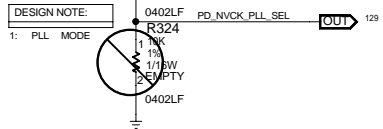
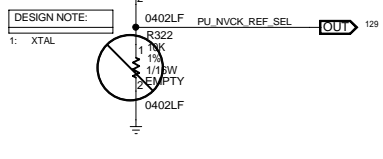
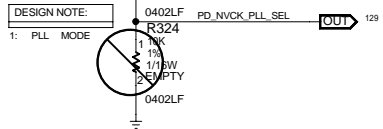
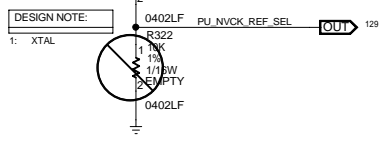
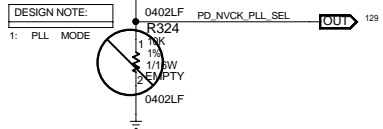
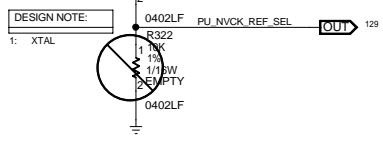
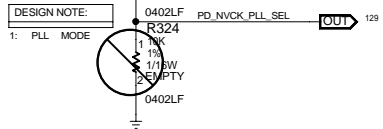
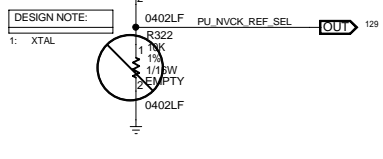
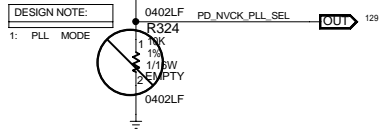
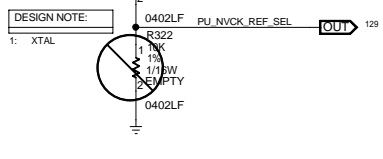
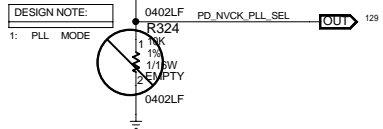
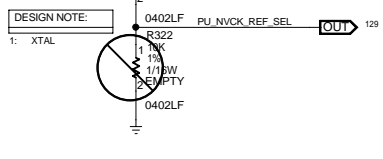
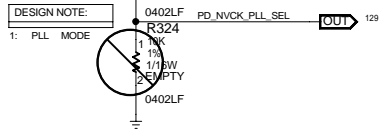
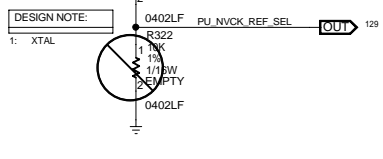
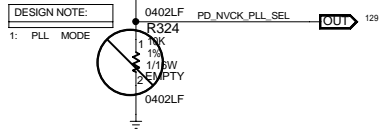
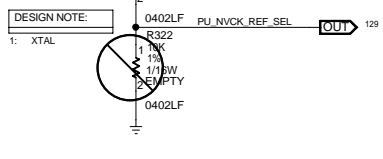
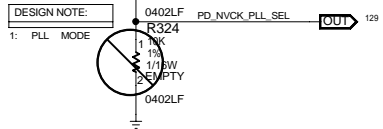
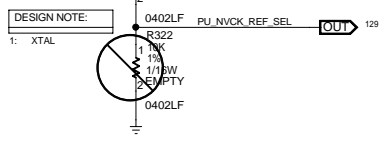
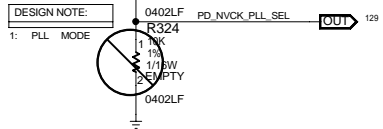
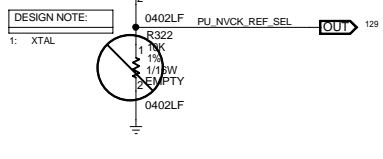
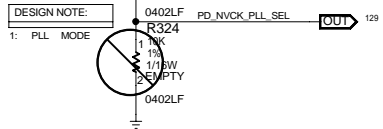
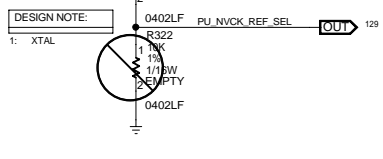
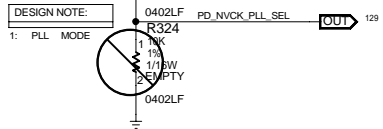
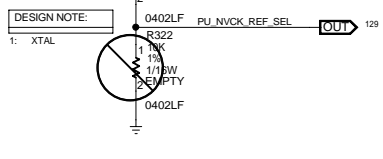
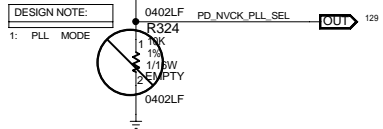
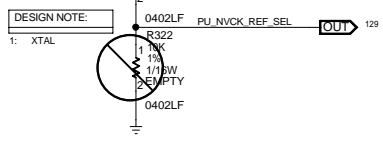
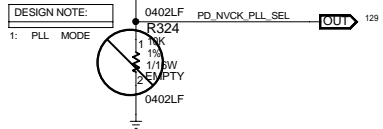
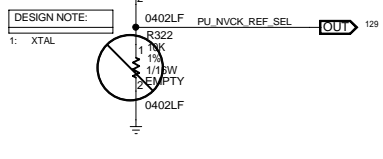
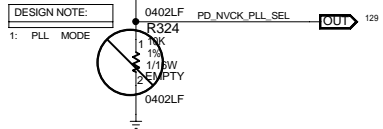
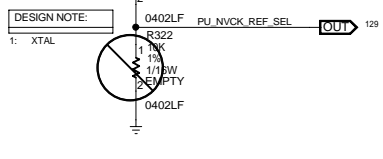
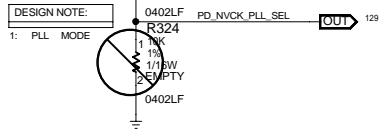
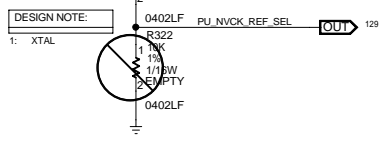
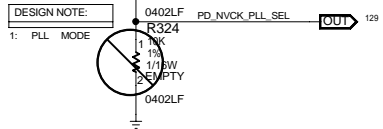
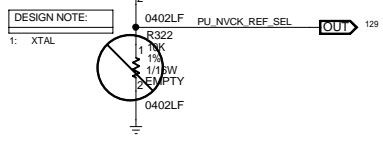
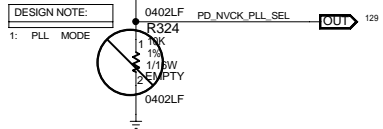
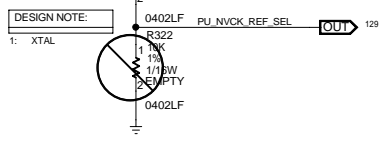
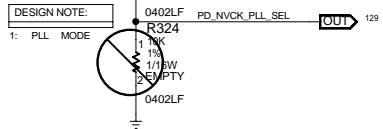
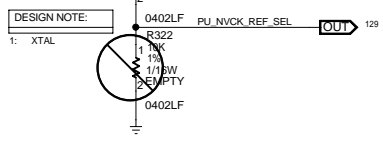
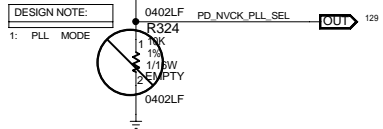
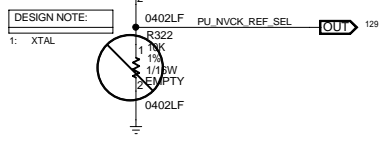
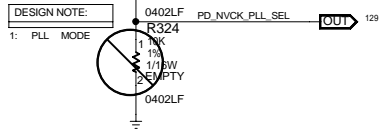
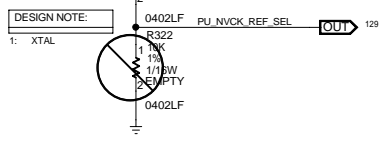
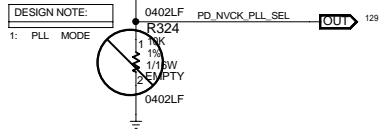
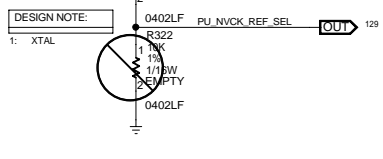
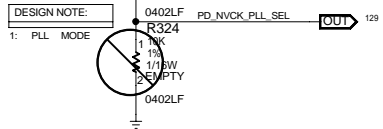
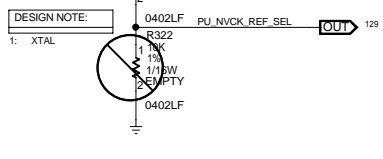
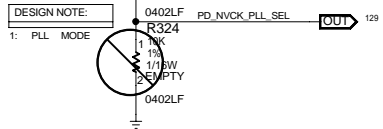
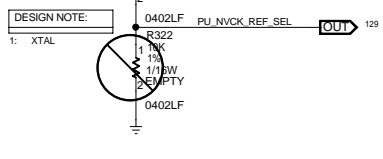
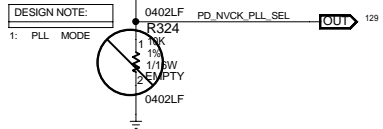
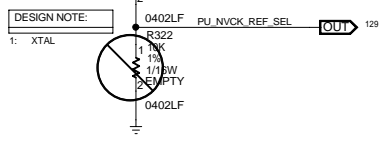
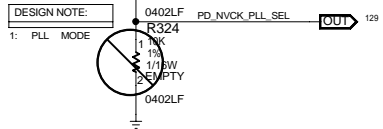
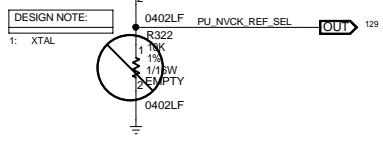
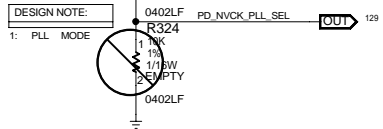
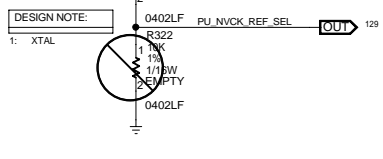
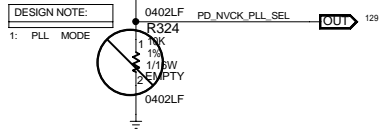
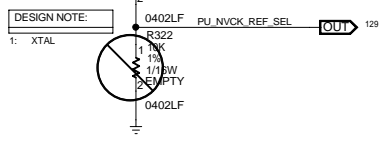
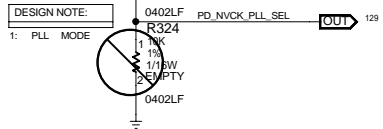
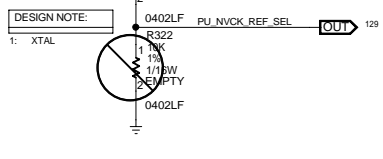
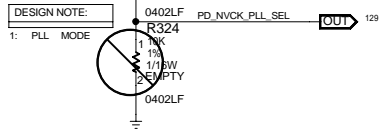
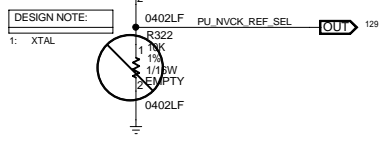
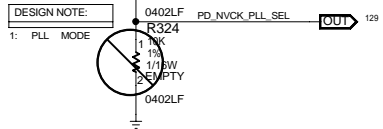
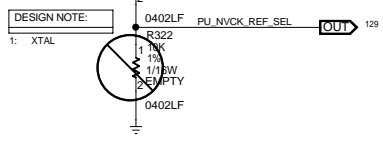
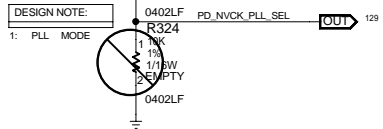
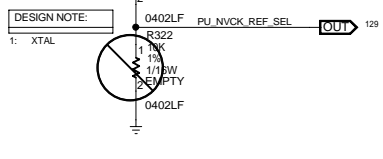
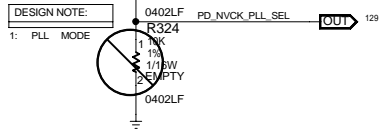
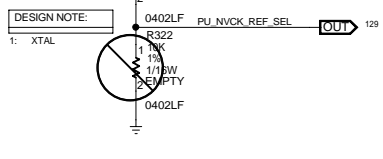
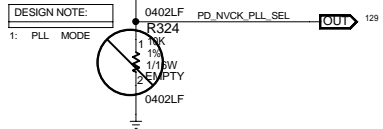
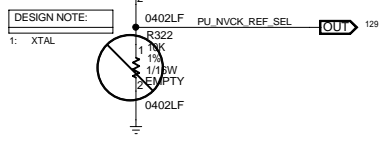
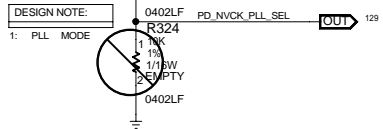
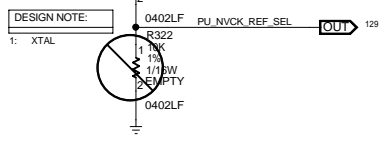
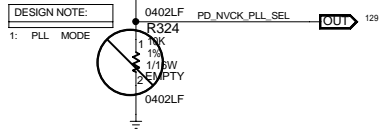
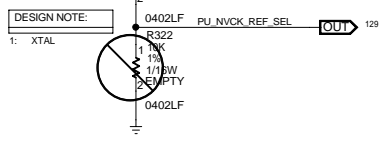
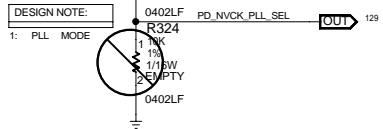
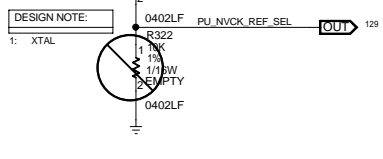
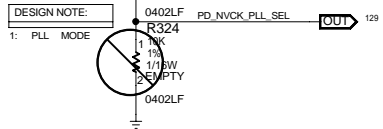
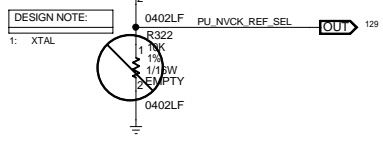
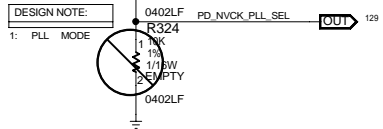
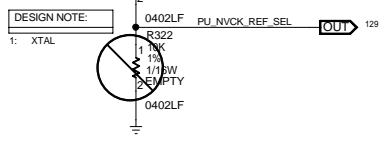
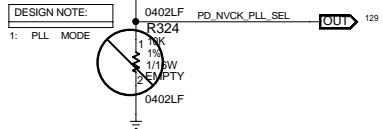
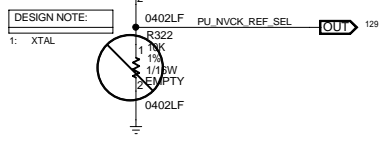
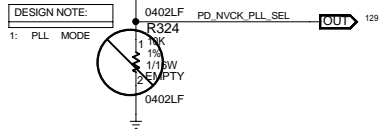
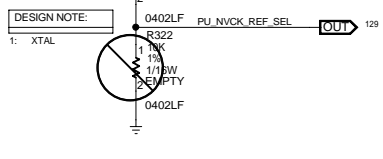
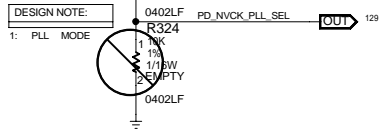
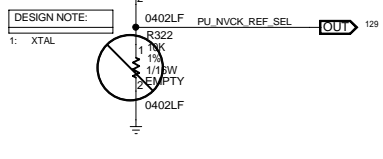
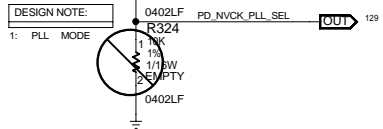
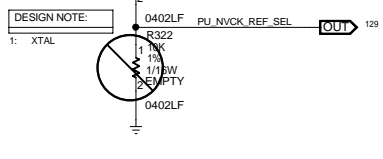
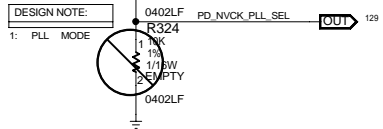
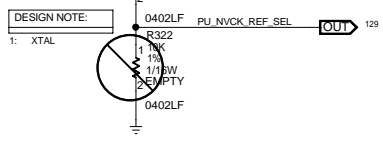
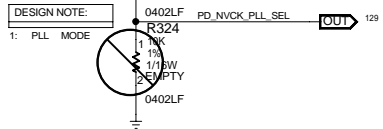
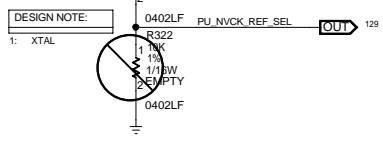
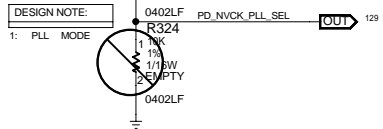
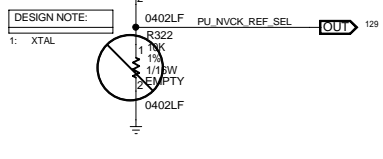
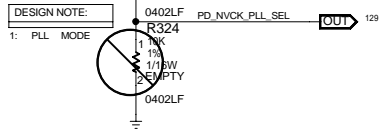
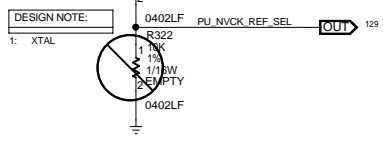
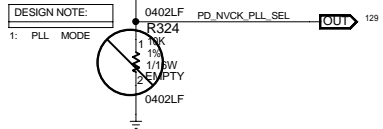
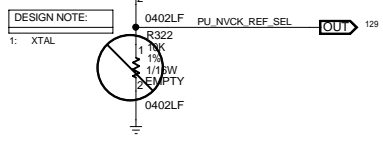
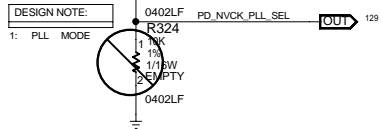
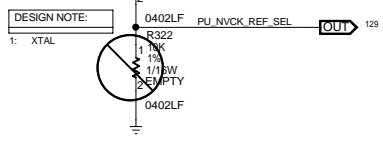
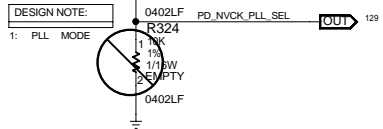
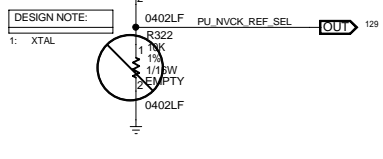
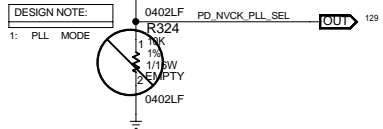
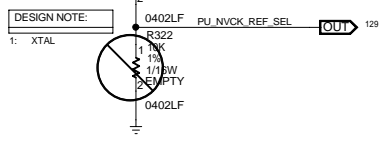
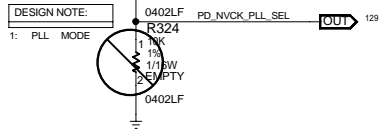
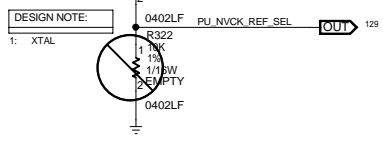
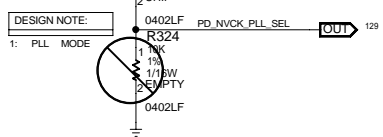
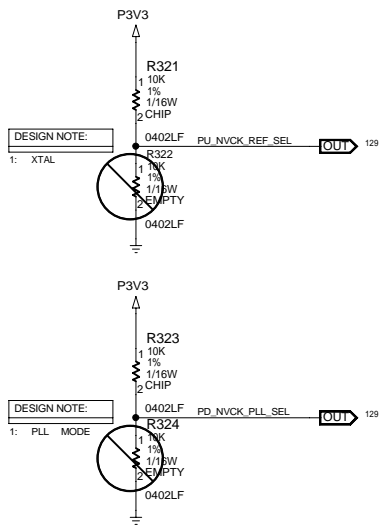
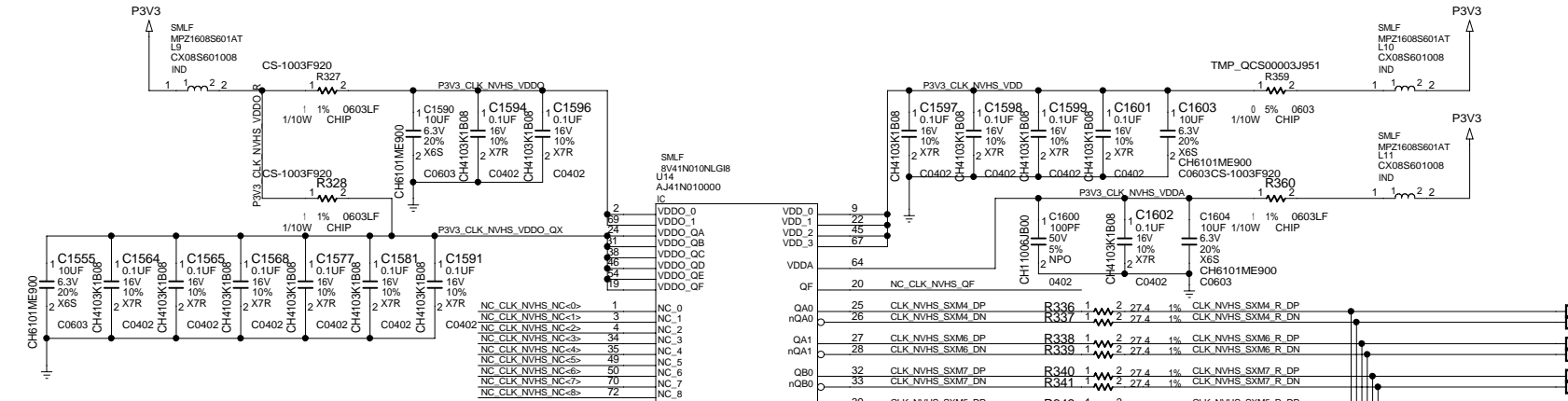
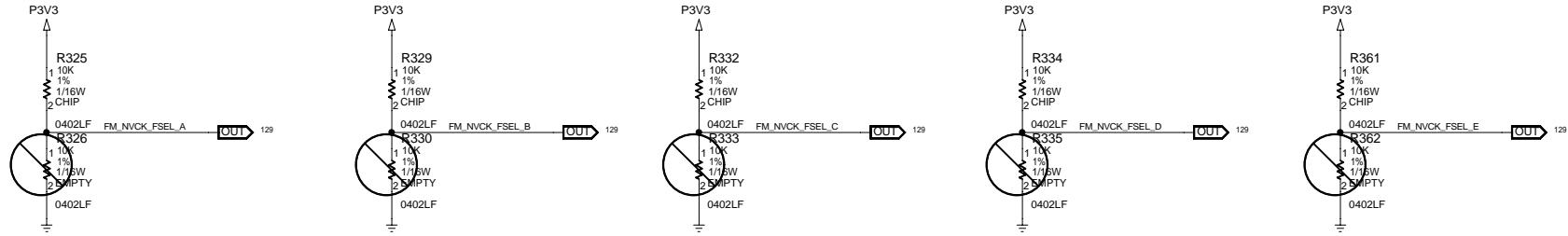
CLOCK BUFFER - PEX3



DEPARTMENT	DESIGNER	NAME	PROJECT	DOCUMENT NUMBER	REV
CCBU	REVIEWER	NAME	S2W	N/A	E
SIZE	C	DATE	Thu Jun 23 09:50:38 2016	SHEET 127 OF 144	

	7	6	5	4	3	2	1																		
E																									
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UNTITLED				<div><div><div>Quanta</div><div>CCBU</div></div><table><tr><td>DEPARTMENT</td><td>DESIGNER</td><td>NAME</td><td>PROJCET</td><td>DOCUMENT NUMBER</td><td>REV</td></tr><tr><td></td><td>REVIEWER</td><td>NAME</td><td>S2W</td><td>N/A</td><td>E</td></tr><tr><td>SIZE</td><td>C</td><td>DATE</td><td>Mon Aug 03 09:39:16 2015</td><td>SHEET 128 OF 144</td><td></td></tr></table></div>				DEPARTMENT	DESIGNER	NAME	PROJCET	DOCUMENT NUMBER	REV		REVIEWER	NAME	S2W	N/A	E	SIZE	C	DATE	Mon Aug 03 09:39:16 2015	SHEET 128 OF 144	
DEPARTMENT	DESIGNER	NAME	PROJCET	DOCUMENT NUMBER	REV																				
	REVIEWER	NAME	S2W	N/A	E																				
SIZE	C	DATE	Mon Aug 03 09:39:16 2015	SHEET 128 OF 144																					

DESIGN NOTE:
0: 100MHZ
1: 156.25MHZ (DEFAULT)



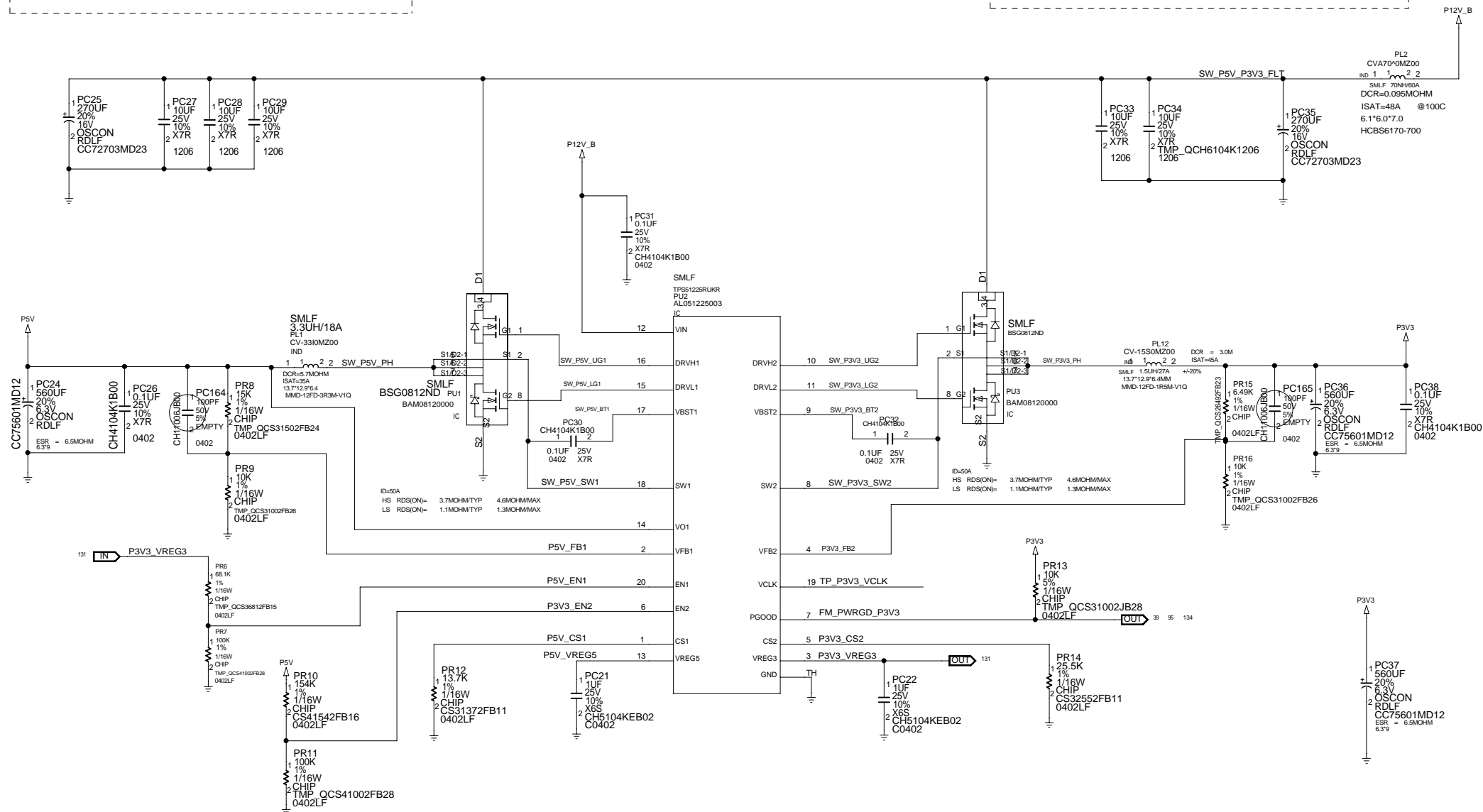
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UNTITLED				<div><div>Quanta</div><div>DEPARTMENT CCBU</div><div>DESIGNER NAME</div><div>REVIEWER NAME</div></div> <div><div>PROJCET S2W</div><div>DOCUMENT NUMBER N/A</div><div>SIZE C</div><div>DATE Mon Aug 03 09:39:14 2015</div><div>SHEET 130 OF 144</div></div> <div>REV E</div>			

DESIGN SPECIFICATION

OUTPUT VOLTAGE = 5.0V+/-5%
 OUTPUT RIPPLE & NOISE < 50MV
 TRANSIENT TOLERANCE = 500MV
 TDC = 8A
 MAX CURRENT = 14A
 OCP(IMAX*130%) = 18.2A
 CURRENT STEP = 0.5A
 SLEW RATE = 0.5A/US
 WORK FREQUENCY = 300KHZ
 EFFICIENCY > 90% @TDC

DESIGN SPECIFICATION

OUTPUT VOLTAGE = 3.3V+/-5%
 OUTPUT RIPPLE & NOISE < 50MV
 TRANSIENT TOLERANCE = 330MV
 TDC = 14.6A
 MAX CURRENT = 20A
 OCP(IMAX*130%) = 26A
 CURRENT STEP = 2.5A
 SLEW RATE = 2.5A/US
 WORK FREQUENCY = 355KHZ
 EFFICIENCY > 90% @TDC



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SIZE	C	DATE	Mon	Aug	10
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2015	SHEET 132 OF 144
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DEPARTMENT

CCBU

DESIGNER	
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NAME

REVIEWER

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PROJCT

S2W

DOCUMENT NUMBER

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SIZE	C	DATE	Mon	Aug	10
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2015 SHEET 133 OF 144

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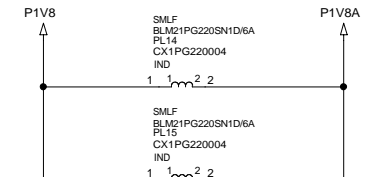
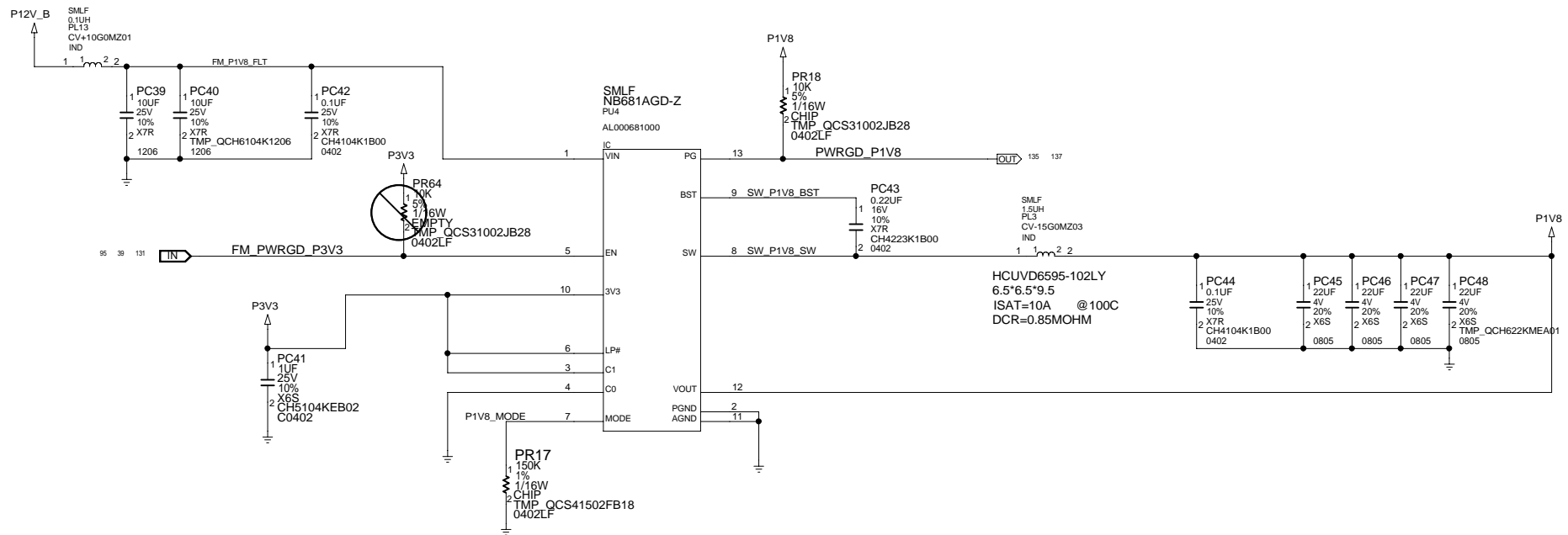
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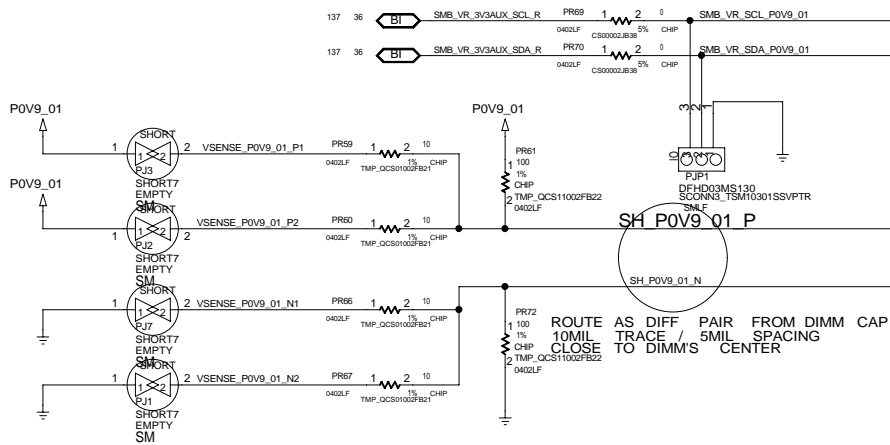
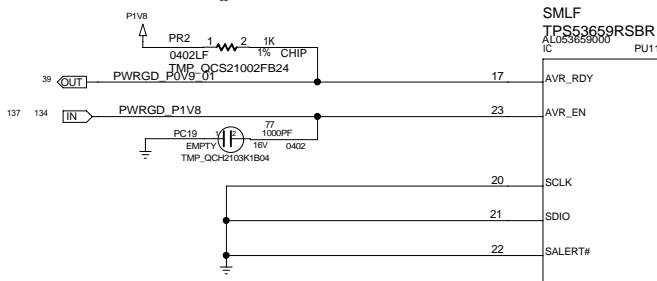
```

| OUTPUT VOLTAGE=1.8V      -5%  +8%
| OUTPUT RIPPLE<30mV
| TRANSIENT TOLERANCE=-90mV+144mV
| TDC=5.2A
| MAX CURRENT=5.73A
| OVER CURRENT PROTECTION(IC RATING)=7A
| CURRENT STEP=2A
| SLEW RATE=0.5A/US
| WORK FREQUENCY=750KHZ
| EFFICIENCY>85%@TDC

```

P1V8





SH P0V9_01 P

SH P0V9_01 N

ROUTE AS DIFF PAIR FROM DIMM CAP
10MIL TRACE / 5MIL SPACING
CLOSE TO DIMM'S CENTER

P3V3_AUX

P0V9_01 VR_FAULT#

P0V9_01 VREF

SW_P12V_P0V9_01_FLT

P0V9_01_ADDR

RAIL	SVID/ I2C	ADDRESS	UP RES	DOWM RES
P0V9_01	00	C4H	115K	49.9K
P0V9_23	02	C6H	75K	37.4K

SMLF
TPS53659RSBR
ALU53659000
PU11

P3V3_AUX

P0V9_01 V3P3

PC51

PC52

APWM1

ACSP1

APWM2

ACSP2

APWM3

ACSP3

APWM4

ACSP4

NC2

PU3

NC3

NC4

BPWM1

BCSP1

VR_HOT#

VR_HOT#

TSEN

BSKIP#

ASKIP#

ASKIP#

P0V9_01 SPECIFICATION

VBOOT=0.9V -5% +5.5%
RIPPLE=+-5MV
TRANSIENT TOLERANCE
=45MV-+50MV
TDC=59A
MAX CURRENT=72.5A
OCP(IMAX*130%)=94.25A
CURRENT STEP=41.5A
SLEW RATE=0.5A/US
WORK FREQUENCY=300KHZ

P3V3_AUX

PC53

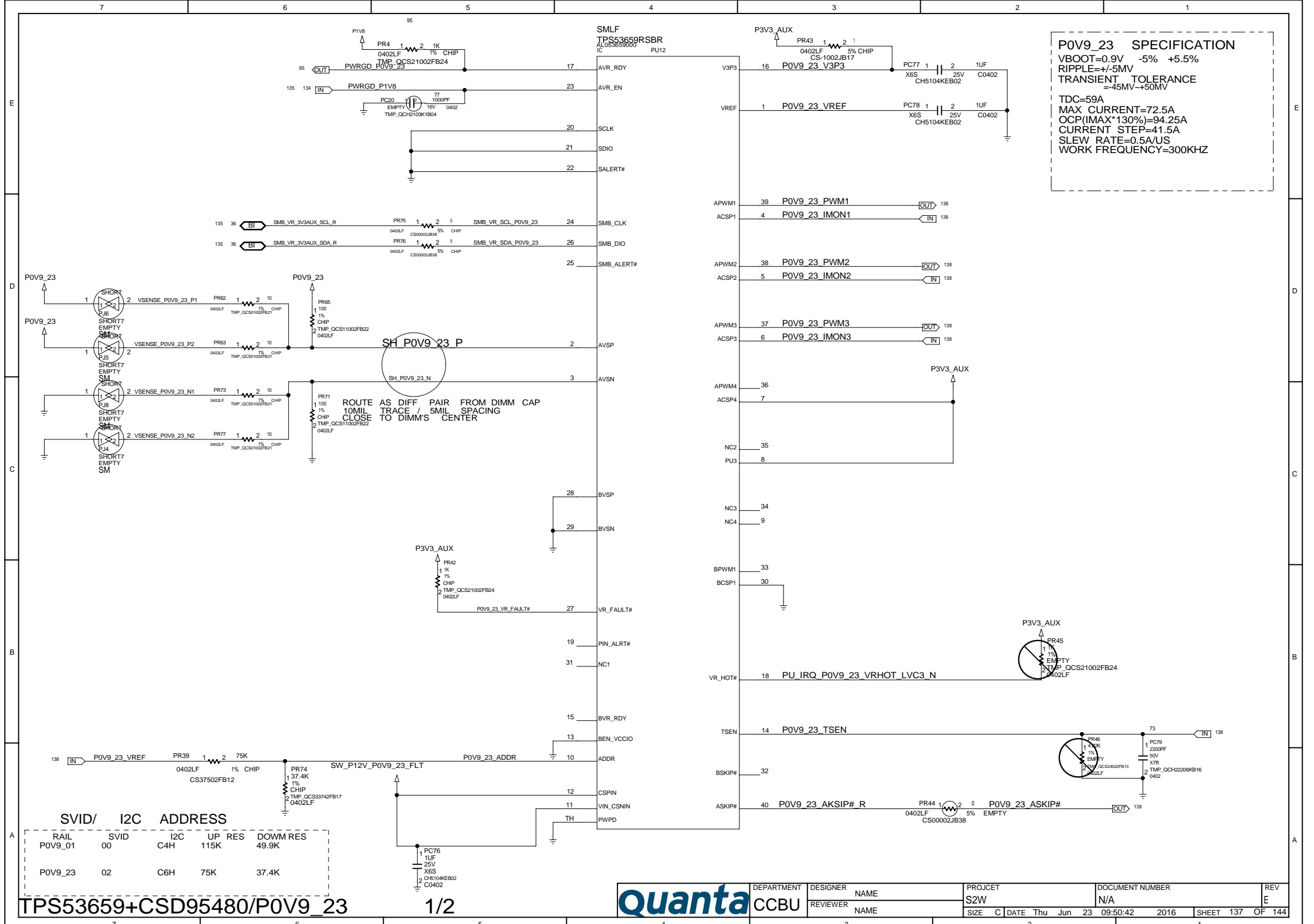
PC53


PC53

PC53

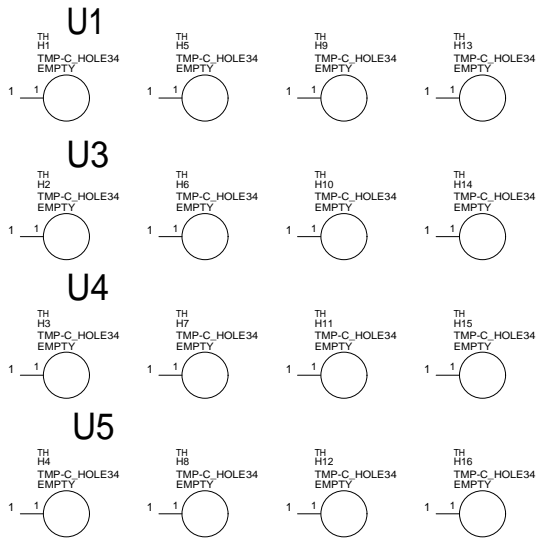


DEPARTMENT	DESIGNER	NAME	PROJECT	DOCUMENT NUMBER	REV
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SIZE	C	DATE	Thu Jun 23 09:50:41 2016	SHEET 135 OF 144	

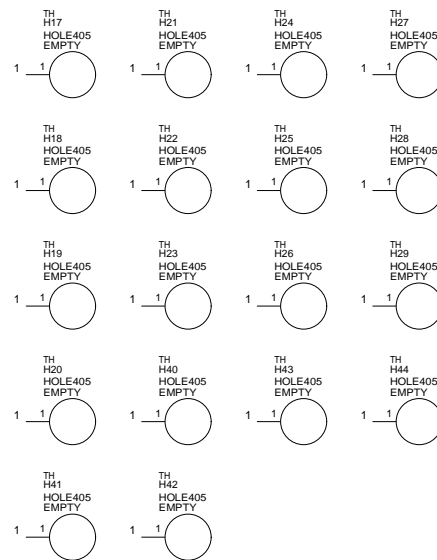


E	7	6	5	4	3	2	1	E		
	QUANTA_LOGO QCT_LOGO	WEEE	PB-E1	PCBA_LABEL	BIOS-BMCLABEL	BARCODE	PCB_VENDOR_LOGO			
	MECH QCT_LOGO_12X12 DM1 DUMMY13 EMPTY <div>DUMMY_SYMBOL</div> ¹	MECH WEEE DM2 DUMMY2 EMPTY <div>DUMMY_SYMBOL</div> ¹	MECH PB-E1_SMALL DM4 DUMMY3 EMPTY <div>DUMMY_SYMBOL</div> ¹	MECH PCBA_LABEL_15X5 DM6 DUMMY4 MECH <div>DUMMY_SYMBOL</div> ¹		MECH BARCODE_20X6 DM16 DUMMY15 MECH <div>DUMMY_SYMBOL</div> ¹ MECH BARCODE_20X6 DM17 DUMMY15 MECH <div>DUMMY_SYMBOL</div> ¹	MECH PCB_VENDOR_LOGO_15X8 DM9 DUMMY7 EMPTY <div>DUMMY_SYMBOL</div> ¹			
D	BMC_FLASH	BIOS_FLASH	MECHANIC_SYMBOL	HEATSINK	BATTERY_SYMBOL	LASER_MARK		D		
			HANDLE BAR EBS4R010010 MECH MECHANIC_SYMBOL DM3 DUMMY10 MECH <div>DUMMY_SYMBOL</div> ¹ THUMB SCREW FBS2Z042010 MECH MECHANIC_SYMBOL DM10 DUMMY10 MECH <div>DUMMY_SYMBOL</div> ¹	EBS4R010010 MECH MECHANIC_SYMBOL DM5 DUMMY10 MECH <div>DUMMY_SYMBOL</div> ¹ FBS2Z042010 MECH MECHANIC_SYMBOL DM11 DUMMY10 MECH <div>DUMMY_SYMBOL</div> ¹	PEX HS FBS2W003010 MECH THERMAL_SYMBOL DM12 DUMMY11 MECH <div>DUMMY_SYMBOL</div> ¹ FBS2W003010 MECH THERMAL_SYMBOL DM13 DUMMY11 MECH <div>DUMMY_SYMBOL</div> ¹	FBS2W003010 MECH THERMAL_SYMBOL DM14 DUMMY11 MECH <div>DUMMY_SYMBOL</div> ¹ FBS2W003010 MECH THERMAL_SYMBOL DM15 DUMMY11 MECH <div>DUMMY_SYMBOL</div> ¹	MECH LASER_MARK_LABELS_10X10B DM7 DUMMY17 EMPTY <div>DUMMY_SYMBOL</div> ¹ MECH LASER_MARK_LABELS_10X10B DM8 DUMMY17 EMPTY <div>DUMMY_SYMBOL</div> ¹			
C								C		
B								B		
A								A		
DUMMY SYMBOL						DEPARTMENT CCBUDESIGNER NAME REVIEWER NAME		PROJCT S2W SIZE C DATE Thu Jun 23 09:50:47 2016	DOCUMENT NUMBER N/A SHEET 139 OF 144	REV E
	7	6	5	4	3	2	1			

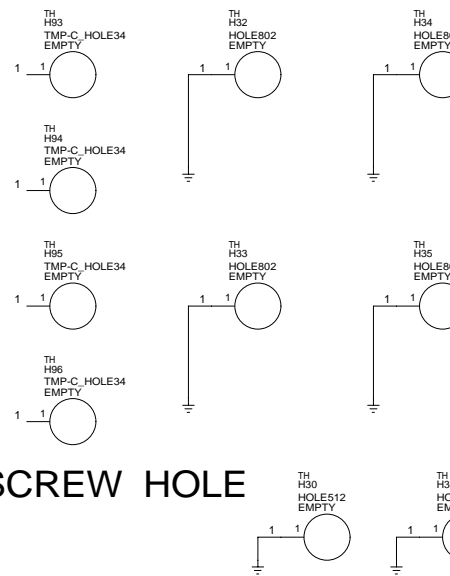
PLX HEATSINK HOLE



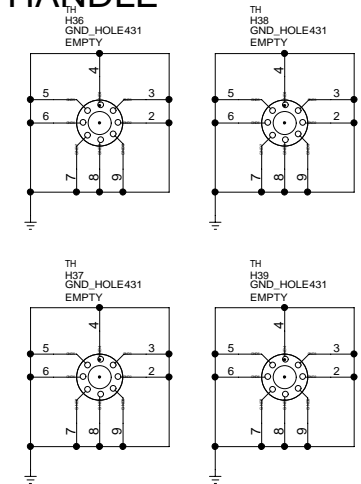
OVAL HOLE



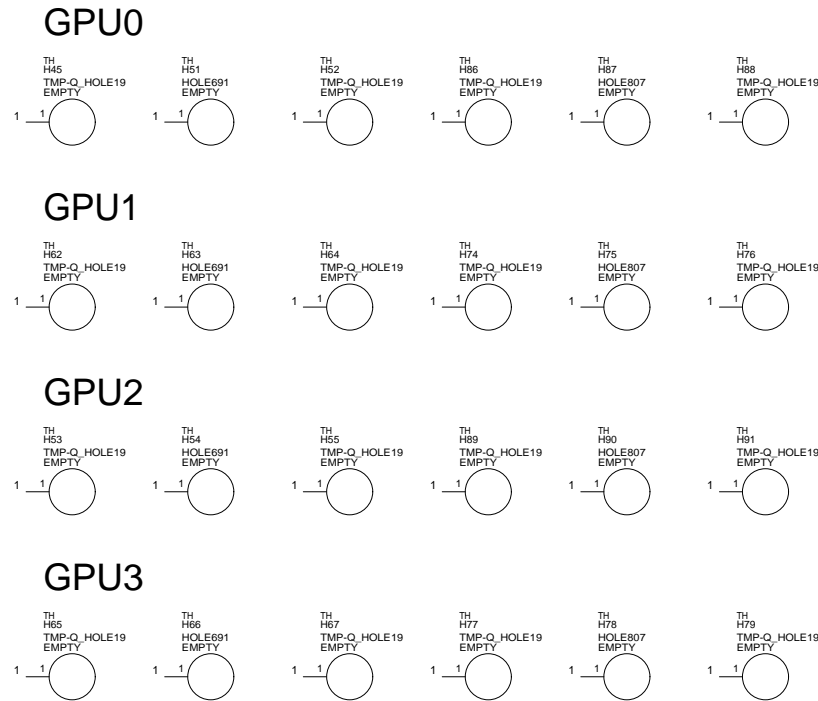
GUIDE HOLE



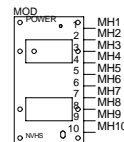
HANDLE



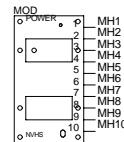
GPU SCREW HOLE



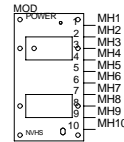
THLF
MODULE_SXM2
J52



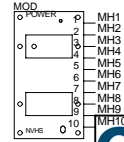
THLF
MODULE_SXM2
J48



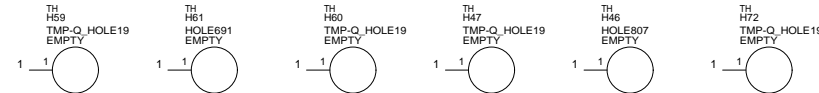
THLF
MODULE_SXM2
J53



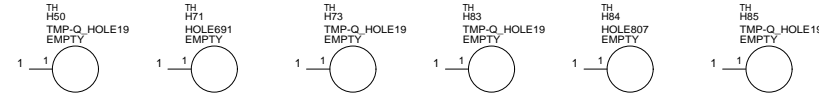
THLF
MODULE_SXM2
J49



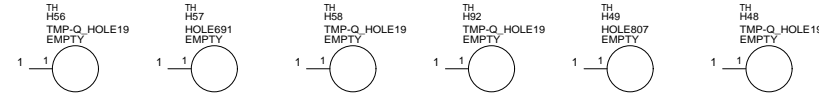
GPU4



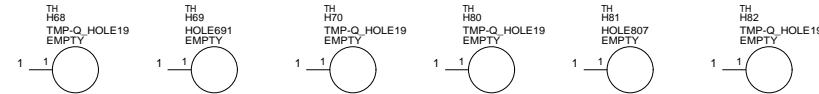
GPU5



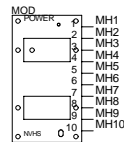
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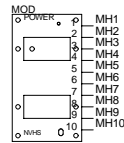
GPU7



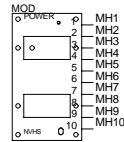
THLF
MODULE_SXM2
J55



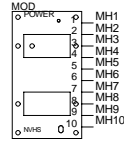
THLF
MODULE_SXM2
J51



THLF
MODULE_SXM2
J54



THLF
MODULE_SXM2
J50



Quanta

DEPARTMENT
CCBU

DESIGNER
NAME
REVIEWER
NAME

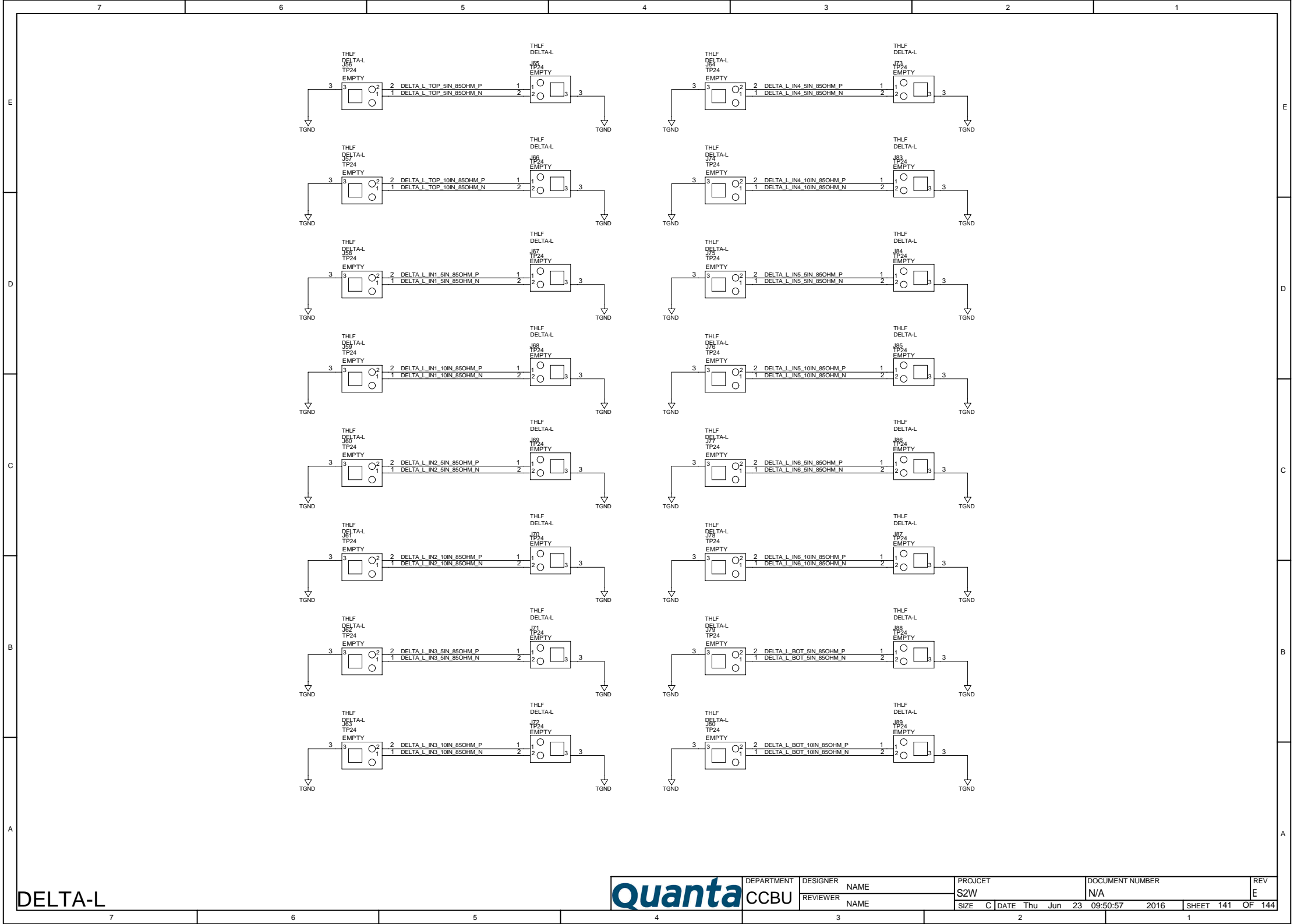
PROJECT
S2W

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N/A

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MOUNTING HOLE



DELTA-L



DEPARTMENT
CCBU

DESIGNER NAME
REVIEWER NAME

PROJCT
S2W

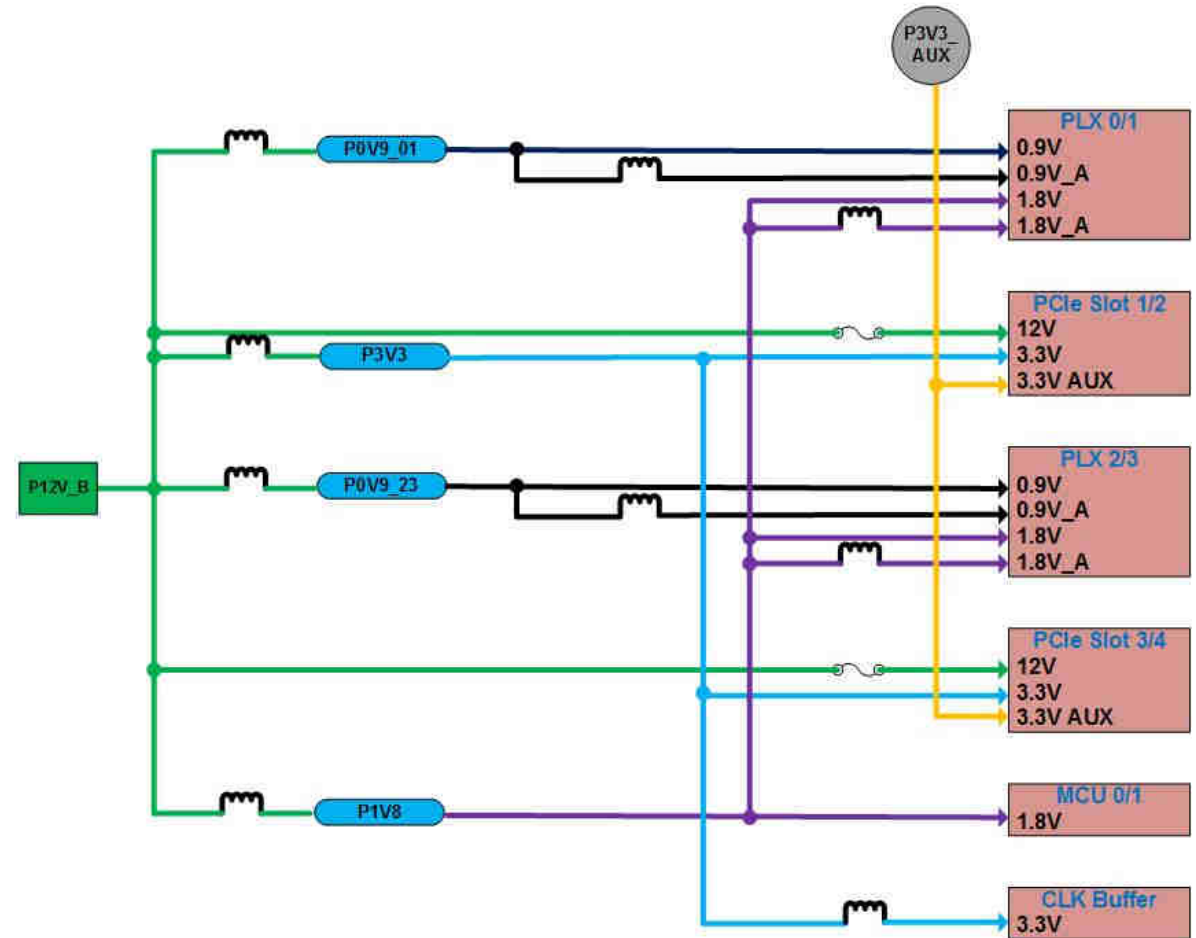
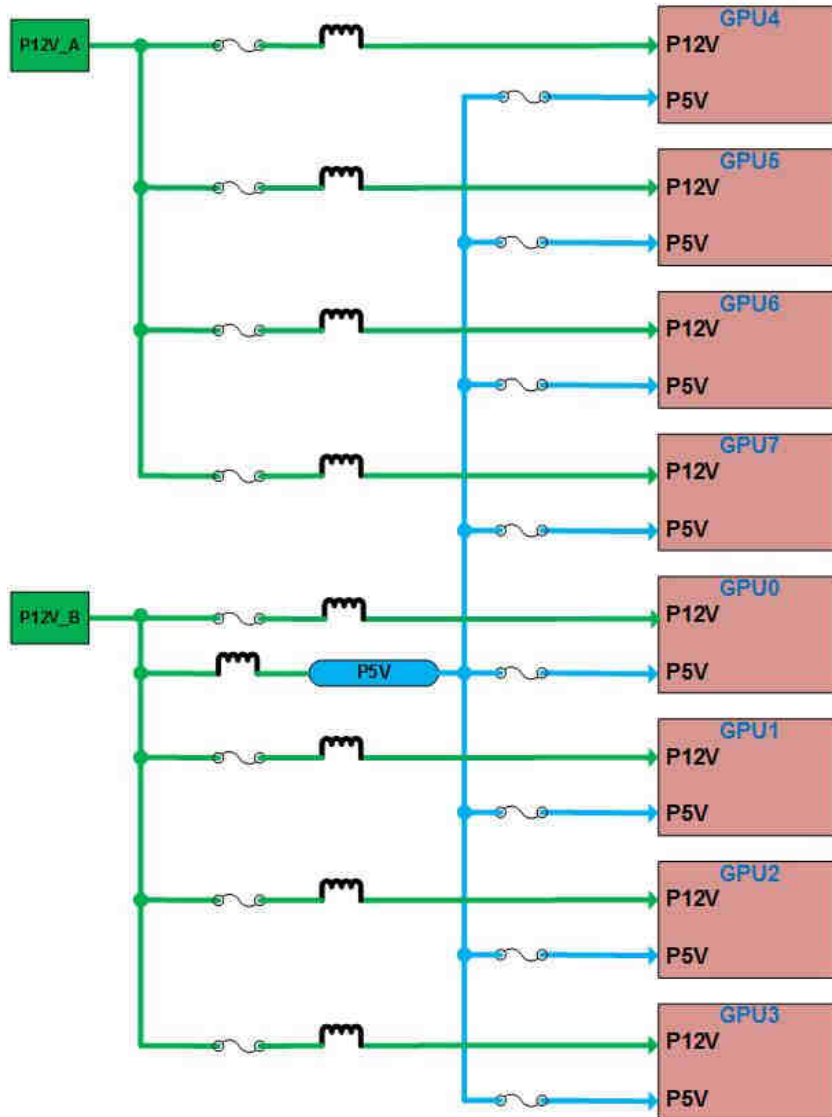
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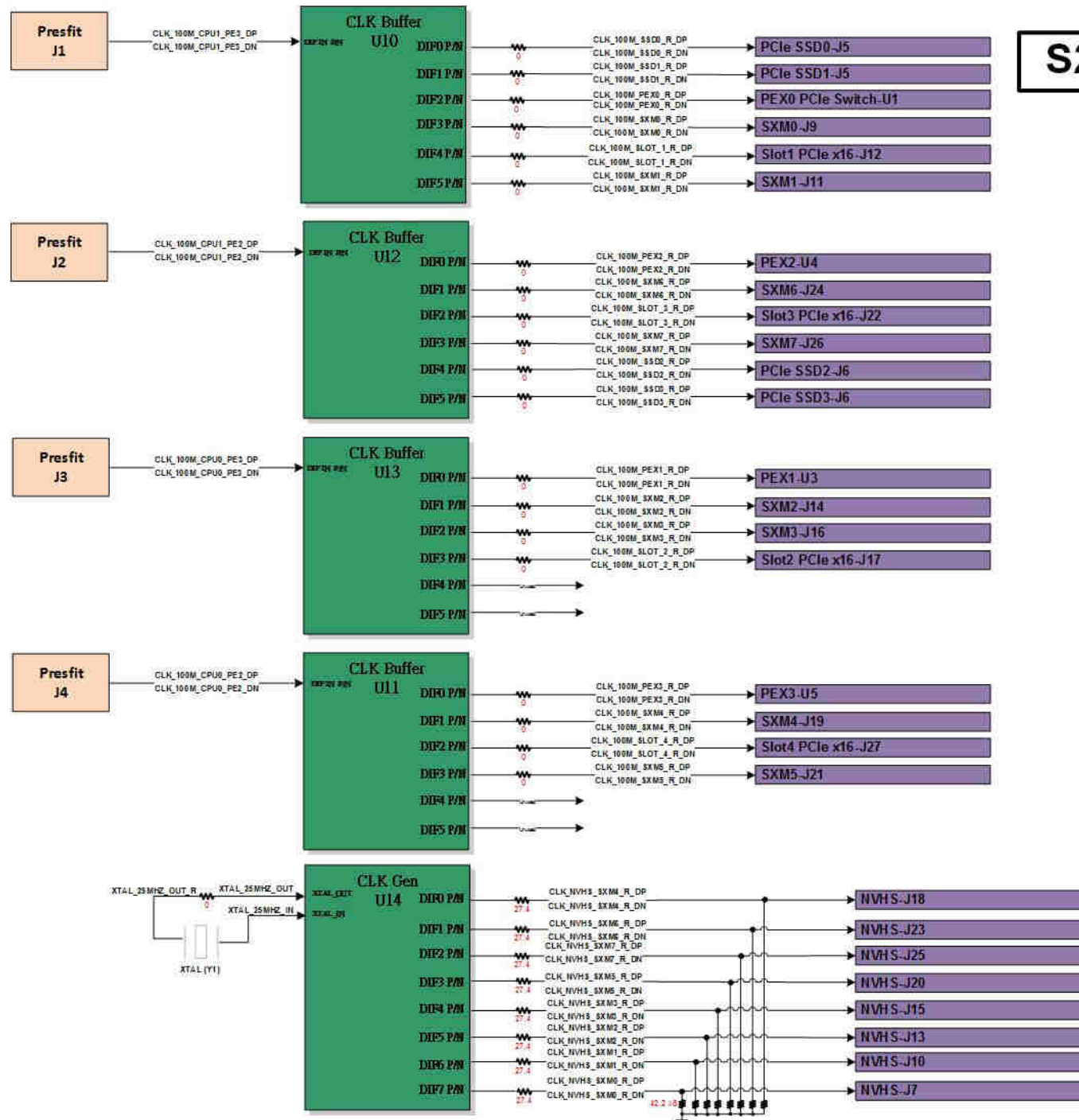
S2W BB VR Diagram

Rev. 1.3 2016/04/20



S2W BB CLK Diagram

Rev. 1.1 2016/01/28



S2W BB SMB Diagram

Rev. 1.2 2016/03/31

