"FIREFLY"

Z80 GENERAL-PURPOSE RETRO COMPUTING PLATFORM

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PREFACE

A project has to have a name and this one wound up being called "Firefly" as it's the culmination of a wirewrap board begun several years ago while binge-watching the series of the same name. That board, in turn, was a redesign of a single board computer I created in 1998, creatively named the "SBCZ1." All three of these projects were begun as a chance to tinker with a processor I first met hands-on in 1984, the ZiLOG Z-80, though it was long-established by that time and dominated the business computer market. It was the CPU of preference behind most CP/M machines and CP/M was what I wanted to tinker with again, from the ground up — not in some cozy emulator.

When I began preparing to design the board I looked around on the Internet and found many excellent Z80 projects, including kit options. The choice was made to "roll my own" for numerous reasons. In the SBCZ1 I had most of a good design and wanted to retain a lot of hard work (done before I had Internet access, mind you). There were also specific reasons for wanting "to stay within ZiLOG canon" and work with a particular hardware configuration. I saw no kits that did just what I wanted in the way that I wanted.

There was also a desire to maintain modularity and be extensible but not require a proliferation of modules for what I considered core functionality, yet great restraint was employed to keep "core functionality" spartan. Inspiration on how to extend the SBCZ1 and correct its shortcomings was drawn from a multitude of sources around the Internet. In the end the Firefly board has wound up being, in my opinion, the best combination of many ideas — some adapted and some original — and division of peripherals. The prototype boards have worked out well, though if I ever do another run there are a few mistakes to correct and improvements which can be made in hindsight.

As a last note, this project is the end-to-end product of an entirely Open Source tool chain (well, technically TASM is not FOSS but I used the purchased Linux version). The KiCAD EDA suite was used for circuit and board design, the TL866CS MiniPro programmer and FOSS command-line tools were used for the EEPROM programming, and Libre Office, Gimp, and Inkscape were used for this documentation.

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CENTRAL PROCESSOR UNIT:

A single ZiLOG Z-80, U1, provides the computational core of the unit. The board is designed to operate with either the 4 mHz Z840004 or 6 mHz Z840006 processors. The compact layout of the board will most likely support the operation of higher-speed devices but this is untested.

CPU MEMORY:

The Firefly board has a 64K address space which is accessible in two memory configurations, as follows:

Configuration 1 (Power-Up)

0000H — 7FFFH	32K Read-Only Memory (ROM)
8000H — FFFFH	32K Random-Access Memory (RAM)

Configuration 2

0000H — FFFFH	64K Random-Access Memory (RAM)

The switch from Configuration 1 to Configuration 2 is accomplished under software control by performing a write (OUT) operation to I/O Port 0 (any port 0, 1, 2, or 3). The transition is one-way. ROM can not be re-enabled under software control and will remain inaccessible until power is cycled or a Cold Reset operation is performed. The value of the data byte written is irrelevant and any value will trigger the switch.

The 628128 Static RAM (U15) chip used provides a total of 128K of memory but there is no means of using the additional memory beyond 64K at this time (bank switching is not supported).

The U16 ROM provides permanent storage for executable boot code in low memory as required by the Z80 design. The Firefly board has been tested with an Atmel 28C256 EEPROM in this role. A pin-compatible 27256 EPROM/PROM is expected work equally well.

ON-BOARD PERIPHERALS AND INPUT/OUTPUT:

Serial Communication

Two (2) synchronous/asynchronous serial ports with full handshaking capabilities are implemented by a ZiLOG Z8440 SIO/0, U18. With care given to the connection of the RI lines, a Z8470 DART may be used instead if only asynchronous communication is desired.

The data and handshaking signals are presented by a dual-row female header connector along the front edge of the board. Signals are TTL (5V) levels and will require level conversion before connection to an RS-232C modem or traditional data terminal equipment.

Signals for serial Channel A are also presented via a single-in-line (SIP) male header which is directly compatible with the pin configuration of an FTDI USB-to-Serial cable. This connection also provides current-limiting resistors on all signals for protection in case either the USB host and Firefly computers are not powered on at the same time.

Data rate is programmable independently for each serial channel. Either the system clock or an optional auxilliary clock may be used as timing reference for baud rate generation.

Parallel Interface

Two 8-bit parallel interfaces with handshaking are implemented via a ZiLOG 8420 PIO, U19. Signals are TTL (5V) and are presented by a dual-row female header connector along the front edge of the board.

Timers

Four programmable counter/timer interrupt sources are implemented via a ZiLOG Z8430 CTC, U17. If the auxillary serial clock is present all four timers are available for general use. Counter/Timer channels 2 and 3 may be configured via an on-board jumper (JP8) for cascaded operation to allow measurement or generation of longer timing intervals.

CLOCKS AND TIMING:

System Timing (OSC1)

Sytem timing governing the operational speed of the CPU is provided by oscillator unit OSC1 ("SYSCLK"). This oscillator must be selected to match the speed of the CPU, CTC, PIO, and SIO (or DART) ZiLOG family components used. The Firefly board is designed to support a 4.0 mHz system clock for the ZiLOG "A" series components, or a 6.144 mHz clock for the ZiLOG "B" series components. The "B" series components can of course run reliably at any of the lesser speeds.

The ZiLOG components require a MOS-level rail-to-rail clock signal not provided by a TTL-level oscilllator. In particular the SIO becomes problematic if clock quality deviates much from specification. To that end, the Firefly provides a ZiLOG reference-design amplifier circuit. If a high-quality MOS-level oscillator is used for OSC1 the circuit need not be populated on the board and the governing jumpers — JP1, JP2, and JP3 -- can be set to the "RAW" position. To allow greater leeway in oscillator selection, however, the amplifier/conditioner can be enabled by selecting the "AMP" jumper positions and most any TTL oscillator may be used.

Auxillary Serial Clock (OSC2)

CTC timer channels 0 and 1 are available to provide programmable reference timing for SIO Channel A and Channel B baud rate generation and use of the Auxillary Serial Clock ("AUXCLK") is not required. However, if it is desirable to separate hard-coded divisor values from dependency on the system clock rate, or if chosen baud rates are not attainable for a given system clock configuration without significant error deviation, the OSC2 AUXCLK oscillator may be used. A value should be chosen that divides cleanly by the SIO prescaler to yield the desired baud rates. A 3.6864 mHz oscillator for OSC2 is one such configuration.

ON-BOARD MASS STORAGE:

None. Mass storage will be implemented by one or more expansion bus modules.

EXPANSION BUS:

Four 50-pin female header connectors provide a means to add additional capabilities to the basic Firefly board. The connectors expose buffered copies of Address, Data, and Control signals as well as pre-decoded IOBANKn and IOSELn lines to simplify the task of interfacing new peripheral hardware and facilitate rapid prototyping. These signals are explained further in the "I/O Map" section.

The Expansion Bus connectors are labled as Slot 1, Slot 2, Slot 3, and Slot 4 and are identical in most regards. It makes no difference into which connector peripherals are plugged with one exception. Pre-decoded IOBANK4 and IOBANK5 signals appear on Slots 1 and 2. IOBANK6 and IOBANK7 signals appear on Slots 3 and 4. If a peripheral module makes use of these decode signals it must be inserted into one of the appropriate slot pairs. Detail of the signals and pin arrangements is provided in the "Connectors and Signals" section.

STATUS INDICATORS:

Three on-board LEDs are provided to indicate Power (green), CPU HALT state (red), and ROM enabled (blue).

DIRECT MEMORY ACCESS (DMA):

None on board but $\overline{\text{BUSRQ}}$ and $\overline{\text{BUSAK}}$ signals are available on the Expansion Bus if a module needs to implement for a user application.

INTERRUPT MODES:

The Firefly board is designed to chiefly support vectored ZiLOG Interrupt Mode 2 operation. Interrupt Mode 1 (single-vector RST38) is also supported. Address and Data buffer circuitry *should* support Interrupt Mode 0 operation as well but there is currently no plan to test or support this mode.

CONFIGURATION JUMPERS AND SWITCHES:

An 8-position dual-inline (DIP) switch, located at the rear corder of the board near the power connector, provides latched configuration input that may be read under software control by performing a READ operation from I/O Port 0 (any port 0, 1, 2, or 3). A CLOSED switch

will produce a logical LOW (0) value on the corresponding bit read. An OPEN switch will produce a logical HIGH (1) value on the corresponding bit read. The meaning associated with each switch and position is entirely under software control and up to the programmer. Settings meaningful to the Boot Monitor will be discussed in the "Boot Monitor" section.

Other aspects of hardware configuration that may need to vary according to usage are controlled user-configurable jumper blocks. The jumpers will be described in the "Jumper Settings" section.

OVERVIEW

The Z80 microprocessor implements an I/O space separate from main memory addresses. There are 256 seperately-addressable I/O ports addressable by the IN and OUT processor instructions. Additionally, when the C-register addressing mode is used to specify the I/O port the contents of the B register are placed on the upper 8 address lines (the port specified by the C register is placed on the lower 8 address lines). This convention allows for I/O parameter passing via the upper lines or an extended I/O address decode, providing 65536 uniquely-addressable I/O locations. The Firefly board fully supports either convention or just the simplified 256-port operation.

On-board I/O decoding is established by two 74LS138 3-to-8 decoders, U9 and U10. I/O decoding on the Firefly board employs the following terminology:

IOBANK -- an active-low decode signal representing a block of 32 I/0 ports. There are eight IOBANK signals.

IOSEL -- an active-low decode signal representing a block of 4 I/O ports

U9 provides decode for eight IOBANK signals, IOBANK0 through IOBANK7. IOBANK 0 is further decoded by U10 for on-board use. The remaining IOBANK signals are passed to the Expansion Bus to simplify hardware decode requirements for expansion modules.

U10 subdivides IOBANK0 into eight IOSEL signals. Four of these, IOSEL0 through IOSEL3, are used on-board. The other four are passed to the Expansion Bus. Of those four, two (IOSEL4 and IOSEL5) are reserved for planned IDE and RTC expansion modules.

IOBANK SIGNALS

IOBANK0	Ports 0-31	(0x00-0x1F), subdivided by U10
IOBANK1	Ports 32-63	(0x20-0x3F), available to user
IOBANK2	Ports 64-95	(0x40-0x5F), available to user
IOBANK3	Ports 96-127	(0x60-0x7F), available to user
IOBANK4	Ports 128-159	(0x80-0x9F), available to user
IOBANK5	Ports 160-191	(0xA0-0xBF), available to user
IOBANK6	Ports 192-223	(0xC0-0xDF), available to user
IOBANK7	Ports 224-255	(0xE0-0xFF), available to user

An IOSEL signal decodes a block of 4 contiguous ports, which conveniently fits the Channel A and Channel B Control and Data registers of the ZiLOG SIO and PIO and the four registers of the CTC chip. For Expansion Bus Modules, an IOSEL signal and a 74LS139 2-to-4 line decoder attached to Address Lines A0 and A1 (BA0 and BA1) will uniquely decode a set of 4 individual ports for a given user application.

IOSEL SIGNALS

IOSEL0	Ports 0-3 (0x00-0x03)	Config/Control
IOSEL1	Ports 4-7 (0x04-0x07)	CTC
IOSEL2	Ports 8-11 (0x08-0x0B)	SIO
IOSEL3	Ports 12-15 (0x08-0x0B)	PIO
IOSEL4	Ports 16-19 (0x10-0x13)	*reserved* (IDE)
IOSEL5	Ports 20-23 (0x14-0x17)	*reserved* (RTC)
IOSEL6	Ports 24-27 (0x18-0x1B)	available to user
IOSEL7	Ports 28-31 (0x1C-0x1F)	available to user

ON-BOARD PERIPHERAL ADDRESSES

Port	Assignment
00H	READ -- System configuration switch WRITE -- Enable RAM in place of ROM
01H	*reserved*
02H	*reserved*
03H	*reserved*
04H	CTC Channel 0 Control Register
05H	CTC Channel 1 Control Register
06H	CTC Channel 2 Control Register
07H	CTC Channel 3 Control Register
08H	SIO Channel A Data Register
09H	SIO CHannel B Data Register
0AH	SIO Channel A Control Register
0BH	SIO Channel B Control Register
0EH	PIO Port A Control Register
0CH	PIO Port A Data Register
0FH	PIO Port B Control Register
0DH	PIO Port B Data Register