CPU, Clock, Control, Buffers

Core

wde8016-1.sch

IO Decode & Control

IO Decode and Control

wde8016-2.sch

Memory -- RAM / ROM

Memory

wde8016-3.sch

Core Zilog Peripherals

Core Zilog Peripherals

wde8016-4.sch

Expansion Bus

Expansion Bus

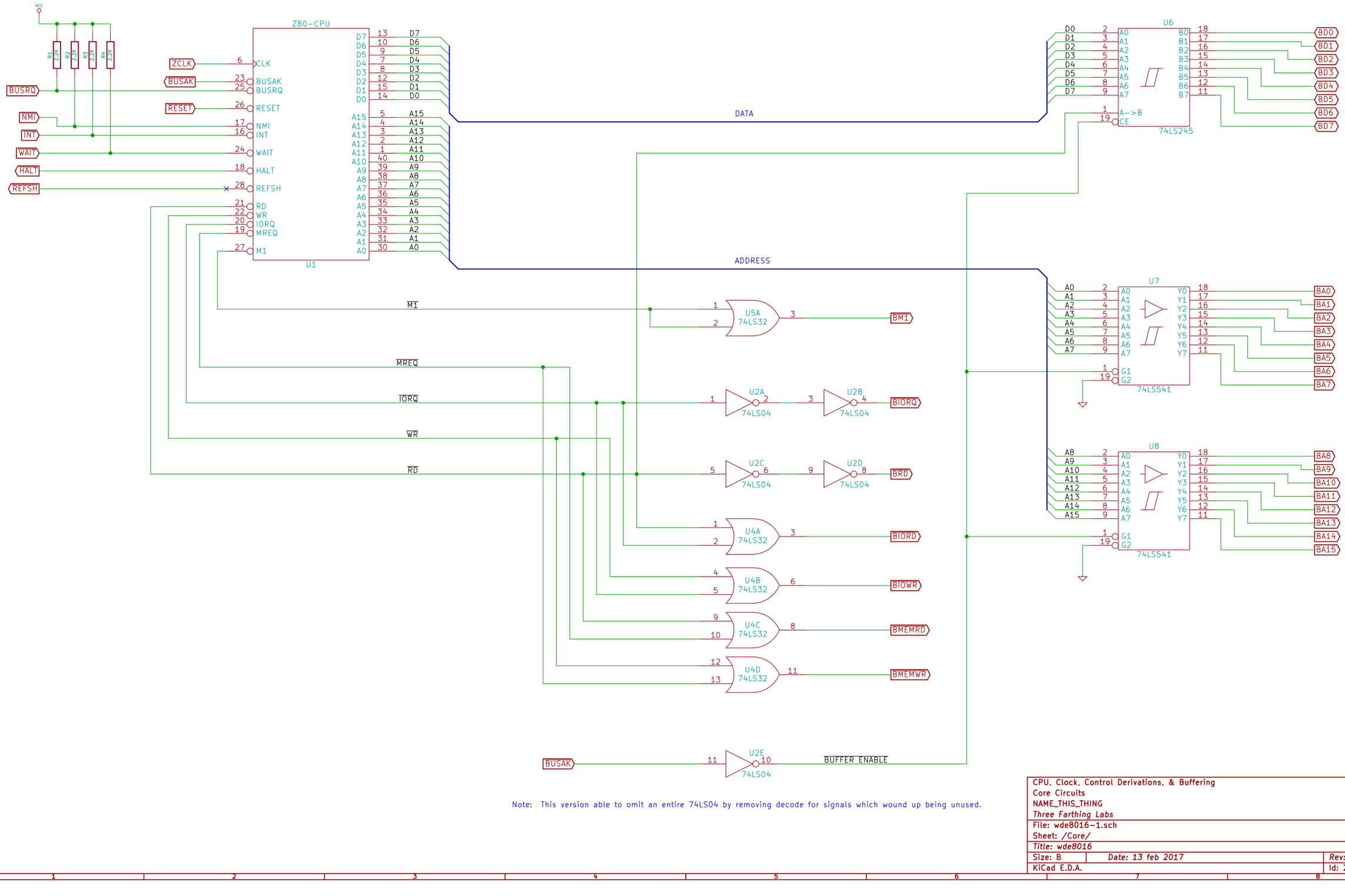
wde8016-7.sch

IPower & Misc

Power & Misc

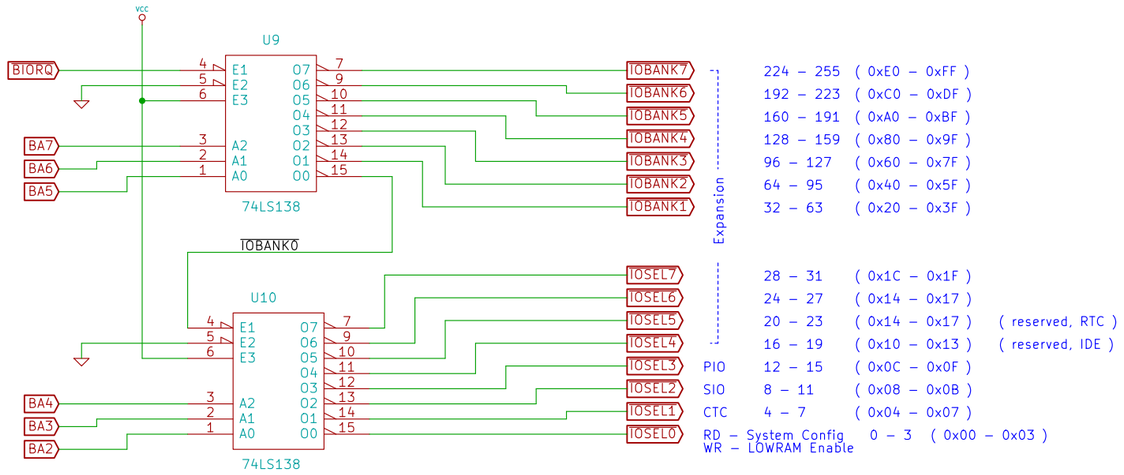
wde8016-6.sch

| | | |
|---|---|---|
| Master Sheet Index<br>NAME_THIS_THING<br>*Three Farthing Labs* | | |
| File: wde8016.sch<br>Sheet: / | | |
| *Title: wde8016* | | |
| Size: A4 | *Date: 13 feb 2017* | *Rev: 0* |
| KiCad E.D.A. | | Id: 1/7 |

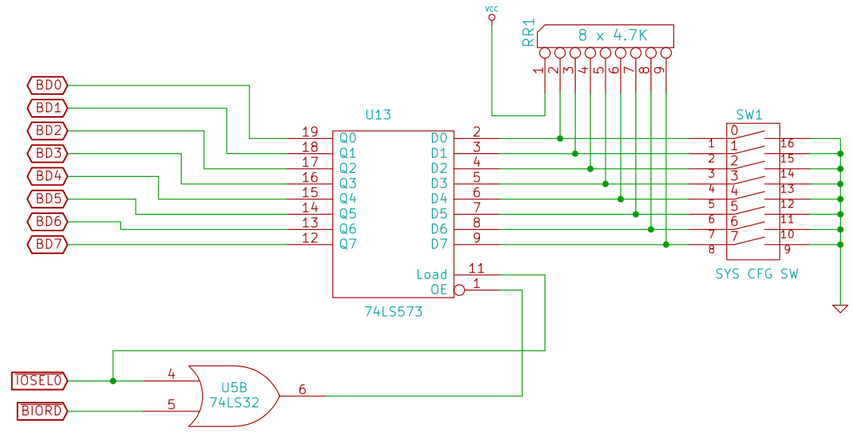



Note: This version able to omit an entire 74LS04 by removing decode for signals which wound up being unused.

| | | |
|---|---|---|
| CPU, Clock, Control Derivations, & Buffering | | |
| Core Circuits | | |
| NAME_THIS_THING | | |
| *Three Farthing Labs* | | |
| File: wde8016-1.sch | | |
| Sheet: /Core/ | | |
| *Title: wde8016* | | |
| Size: B | *Date: 13 feb 2017* | *Rev: 0* |
| KiCad E.D.A. | | Id: 2/7 |

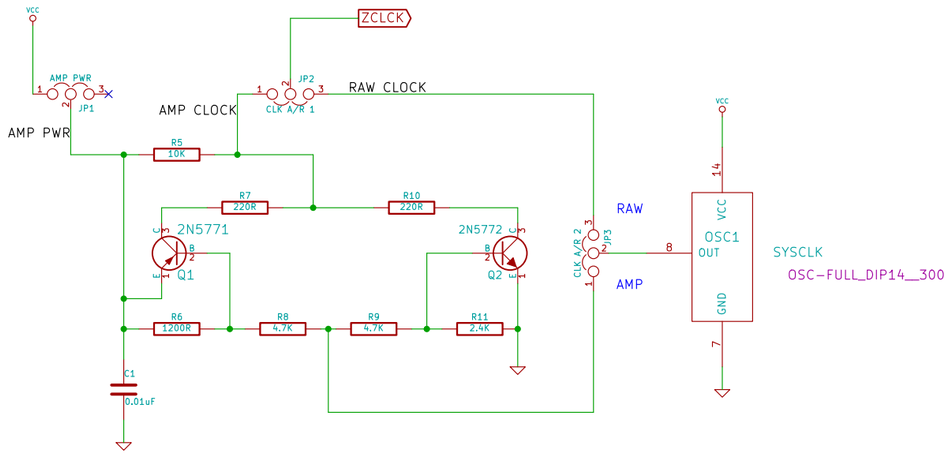



Master I/O Map Decode
IOBANKn: Selects 1 of 8 blocks of 32 I/O ports ea.
IOSELn: Selects 1 of 8 blocks of 4 I/O ports ea.

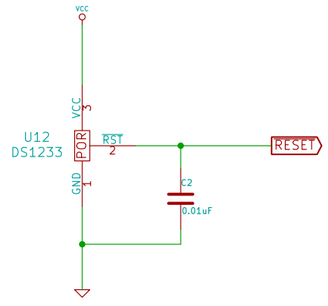



System Config Port
Value of the config switch is latched and read by any READ operation from IOSEL0 (Ports 0–3).

Open switch = bit value of 1, Closed switch = bit value of 0

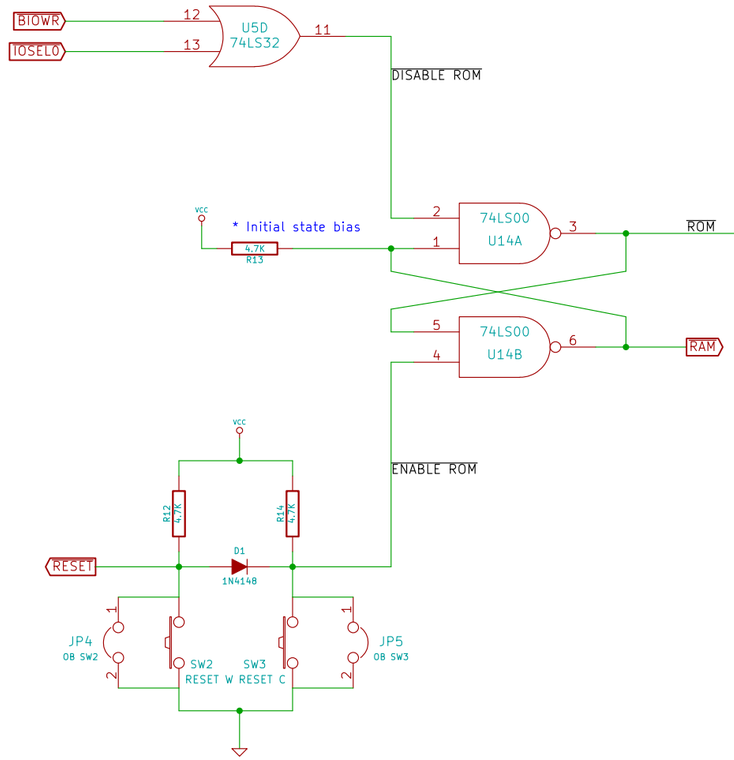



Clock Note: Zilog parts use a MOS-level clock rather than standard TTL levels. Optional amp circuit allows use of TTL oscillator devices.



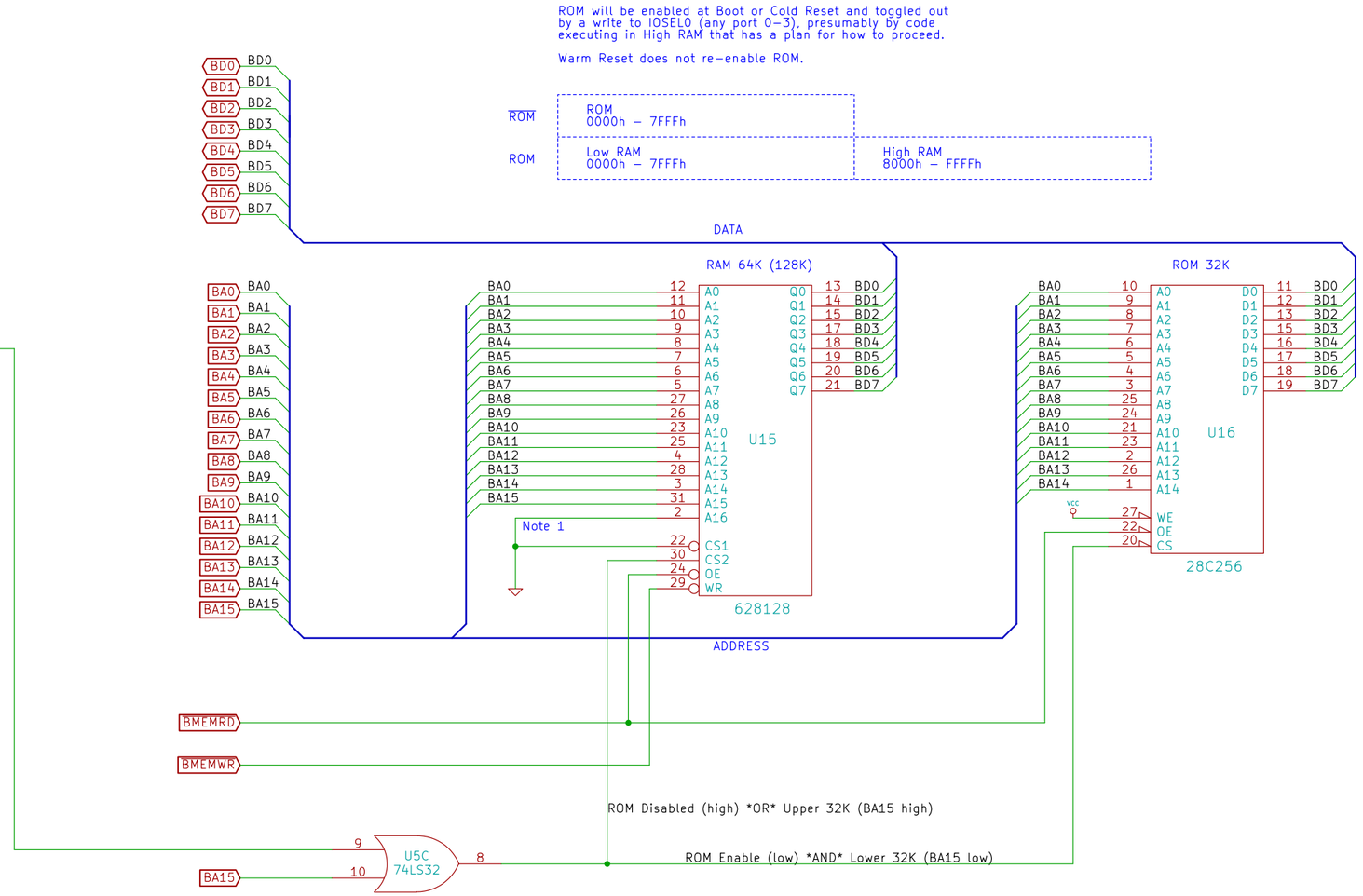

Power-On Reset Controller
RESET active for 350ms after stable Pwr or RST being brought low

| | | |
|---|---|---|
| IO Decode, Clock, POR, & System Config Port | | |
| NAME_THIS_THING | | |
| *Three Farthing Labs* | | |
| File: wde8016-2.sch | | |
| Sheet: /IO Decode and Control/ | | |
| *Title: wde8016* | | |
| Size: B | *Date: 13 feb 2017* | *Rev: 0* |
| KiCad E.D.A. | | Id: 3/7 |




RAM/ROM Toggle
THEORY OF OPERATION: At power-on ROM will be Active (low).
An I/O write to any port in IOSEL0 (port 0-3), such as OUT( 0 ),
will latch ROM to disabled (high) and swap RAM into lower 32K address space.

WARM RESET resets Z80 & peripherals w/out disrupting RAM.
COLD RESET resets everything and toggles ROM back into lower 32K.




| | | |
|---|---|---|
| Memory / Memory Control / Expansion Bus | | |
| NAME_THIS_THING | | |
| *Three Farthing Labs* | | |
| File: wde8016-3.sch | | |
| Sheet: /Memory/ | | |
| *Title: wde8016* | | |
| Size: B | *Date: 13 feb 2017* | *Rev: 0* |
| KiCad E.D.A. | | Id: 4/7 |

OPTIONAL Baud Oscillator

The Z80 CTC can internally Prescale & Divide the system clock to generate baud clocks for the SIO without the need for an external clock source. However, this both makes software timing constants bound to the system clock AND not all common boaud rates are attainable without significant error percentages at common Z80 system clock frequencies (like the Z80B's 6.144 mHz preferred clock). An external fixed oscillator can (optionally) give us a more precise clock and allow system clock variance without alternate prescaler/divisor constants.

Optional – External Baud Rate Oscillator

OSC-FULL_DIP14__300

On-Board Serial I/O & Timer Lines

SIO Ports A & B
CTC CLK/TRG for Ports 2 & 3
CTC ZC for Port 2
TTL-levels ( *not* RS-232C )
24-pin .100 center, 1"-high female header

P1 TTL SER A/B/CLK

| | | | |
|---|---|---|---|
| | 1 | 2 | |
| RTSA | 3 | 4 | RTSB |
| RXDA | 5 | 6 | RXDB |
| TXDA | 7 | 8 | TXDB |
| SYNCA | 9 | 10 | SYNCB |
| CTSA | 11 | 12 | CTSB |
| W/RDYA | 13 | 14 | W/RDYB |
| DTRA | 15 | 16 | DTRB |
| DCDA | 17 | 18 | DCDB |
| ZC/TO2 | 19 | 20 | CLK/TRG2 |
| RESET | 21 | 22 | CLK/TRG3 |
| | 23 | 24 | |

JP9 SYNCB HI
JP10 SYNCA HI
R15 10K
R16 10K

Note:
Add 2.7K current-limiting resistors in series with each TTL serial line used if connecting to a USB-to-TTL-Serial cable. This will prevent damaging current draws if either board or remote USB is not powered!

Serial Channel A TTL Serial Port
(e.g. FTDI USB-to-TTL Serial Cable)

P2 TTL SER A

| | | | |
|---|---|---|---|
| | 1 | 2 | |
| | 3 | 4 | |
| | 5 | 6 | |
| RTSA | R17 2.7K | | BLK GND |
| RXDA | R18 2.7K | | BRN CTS |
| TXDA | R19 2.7K | | RED +5V |
| CTSA | R20 2.7K | | ORNG TXD |
| | | | YEL RXD |
| | | | GRN RTS |

On-Board Parallel I/O
PIO Ports A & B,
24-pin .100-center 1"-high female header

P3 PIO A/B

| | | | |
|---|---|---|---|
| | 1 | 2 | |
| PA0 | 3 | 4 | PB0 |
| PA1 | 5 | 6 | PB1 |
| PA2 | 7 | 8 | PB2 |
| PA3 | 9 | 10 | PB3 |
| PA4 | 11 | 12 | PB4 |
| PA5 | 13 | 14 | PB5 |
| PA6 | 15 | 16 | PB6 |
| PA7 | 17 | 18 | PB7 |
| ARDY | 19 | 20 | BRDY |
| ASTB | 21 | 22 | BSTB |
| | 23 | 24 | |

OSC-FULL_DIP14__300: VCC, OSC2, OUT, AUXCLK, GND; pin 14 / 8 / 7
JP6 CLK0 EXT/INT
JP7 CLK1 EXT/INT
ZCLCK

BD0 BD1 BD2 BD3 BD4 BD5 BD6 BD7

DATA

U17 Z80-CTC

| | | | |
|---|---|---|---|
| BD0 | 25 | D0 | |
| BD1 | 26 | D1 | CLK/TRG0 23 |
| BD2 | 27 | D2 | ZC/TO0 7 |
| BD3 | 28 | D3 | |
| BD4 | 1 | D4 | CLK/TRG1 22 |
| BD5 | 2 | D5 | ZC/TO1 8 |
| BD6 | 3 | D6 | |
| BD7 | 4 | D7 | |
| IOSEL1 | 16 | CE | CLK/TRG2 21 CLK/TRG2 |
| BA0 | 18 | CS0 | ZC/TO2 9 ZC/TO2 |
| BA1 | 19 | CS1 | |
| | 14 | M1 | |
| | 10 | IORQ | CLK/TRG3 20 CLK/TRG3 |
| | 6 | RD | |
| | 12 | INT | RESET 17 |
| | 15 | CLK | |

IEI 13, IEO 11
JP8 ZC2 > TRG3 Timer Cascade
INT Priority = Highest

U18 Z80-SIO/O

| | | | |
|---|---|---|---|
| BD0 | 40 | D0 | RXDA 12 RXDA |
| BD1 | 1 | D1 | RXCA 13 |
| BD2 | 39 | D2 | TXDA 15 TXDA |
| BD3 | 2 | D3 | TXCA 14 |
| BD4 | 38 | D4 | SYNCA 11 SYNCA |
| BD5 | 3 | D5 | W/RDYA 10 W/RDYA |
| BD6 | 37 | D6 | |
| BD7 | 4 | D7 | RTSA 17 RTSA |
| | | | CTSA 18 CTSA |
| | | | DTRA 16 DTRA |
| | | | DCDA 19 DCDA |
| IOSEL2 | 35 | CE | RXDB 28 RXDB |
| RESET | 21 | RESET | TXDB 26 TXDB |
| | 8 | M1 | RXTXCB 27 RXTXCB |
| | 36 | IORQ | SYNCB 29 SYNCB |
| | 32 | RD | W/RDYB 30 W/RDYB |
| BA1 | 33 | C/D | |
| BA0 | 34 | B/A | RTSB 24 RTSB |
| | 5 | INT | CTSB 23 CTSB |
| | | | DTRB 25 DTRB |
| | 20 | CLK | DCDB 22 DCDB |

IEI 6, IEO 7

U19 Z80-PIO

| | | | |
|---|---|---|---|
| BD0 | 19 | D0 | PA0 15 PA0 |
| BD1 | 20 | D1 | PA1 14 PA1 |
| BD2 | 1 | D2 | PA2 13 PA2 |
| BD3 | 40 | D3 | PA3 12 PA3 |
| BD4 | 39 | D4 | PA4 10 PA4 |
| BD5 | 38 | D5 | PA5 9 PA5 |
| BD6 | 3 | D6 | PA6 8 PA6 |
| BD7 | 2 | D7 | PA7 7 PA7 |
| | | | ARDY 18 ARDY |
| | 23 | INT | ASTB 16 ASTB |
| IOSEL3 | 4 | CE | PB0 27 PB0 |
| | 35 | RD | PB1 28 PB1 |
| | 36 | IORQ | PB2 29 PB2 |
| | 37 | M1 | PB3 30 PB3 |
| BA1 | 5 | C/D | PB4 31 PB4 |
| BA0 | 6 | B/A | PB5 32 PB5 |
| | | | PB6 33 PB6 |
| | 25 | CLK | PB7 34 PB7 |
| | | | BRDY 21 BRDY |
| | | | BSTB 17 BSTB |

IEI 24, IEO 22
INT Priority = Lowest

JP11 w/RDYA to WAIT
JP12 w/RDYB to WAIT
WAIT

ADDRESS

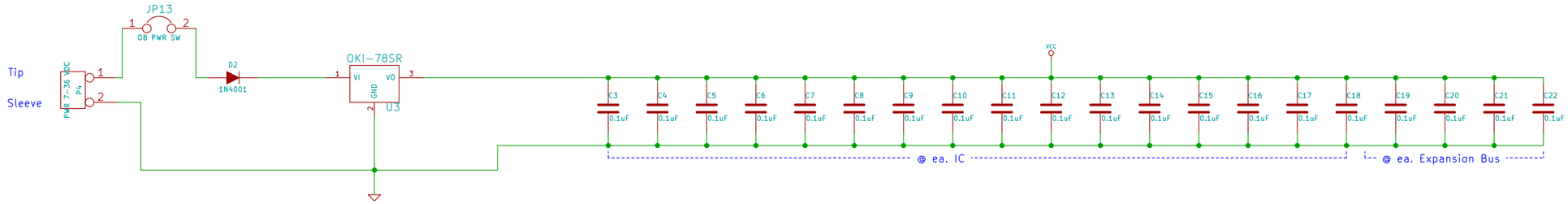
BA0 BA1

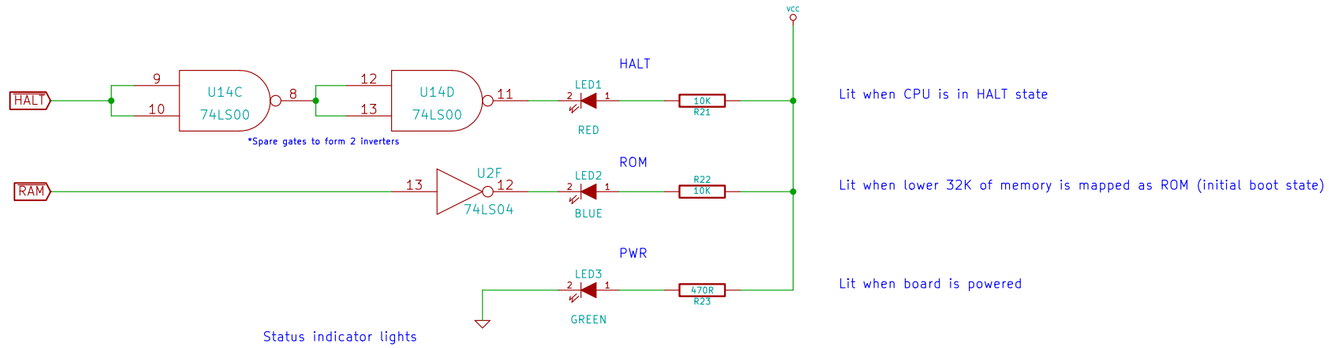
EXPIEO

BM1 BIORQ BRD INT RESET ZCLCK

ON-BOARD I/O Notes:
This will represent the compliment of on-board I/O. All signals will be presented at TTL levels in .100-center pin headers. RS-232 level conversion will be left to the domain of external interface adapter boards if ever needed. Likewise, a proper console interface (PS/2-style keyboard and terminal text output) will be left to a specialized module designed for the expansion bus.

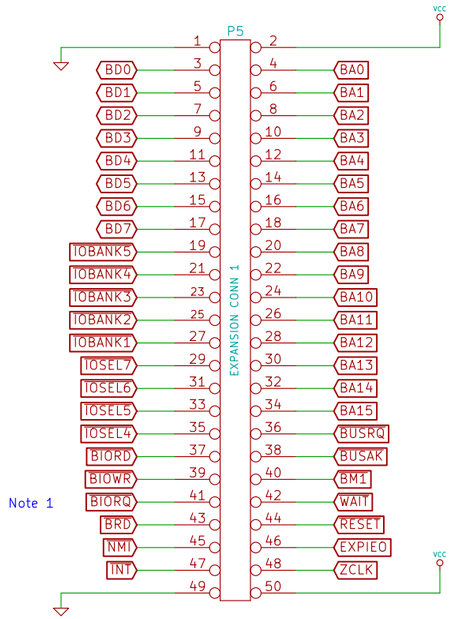
| | | |
|---|---|---|
| On-Board Zilog Serial, Parallel, & Timer I/O | | |
| NAME_THIS_THING | | |
| *Three Farthing Labs* | | |
| File: wde8016-4.sch | | |
| Sheet: /Core Zilog Peripherals/ | | |
| *Title: wde8016* | | |
| Size: B | *Date: 13 feb 2017* | *Rev: 0* |
| KiCad E.D.A. | | Id: 5/7 |



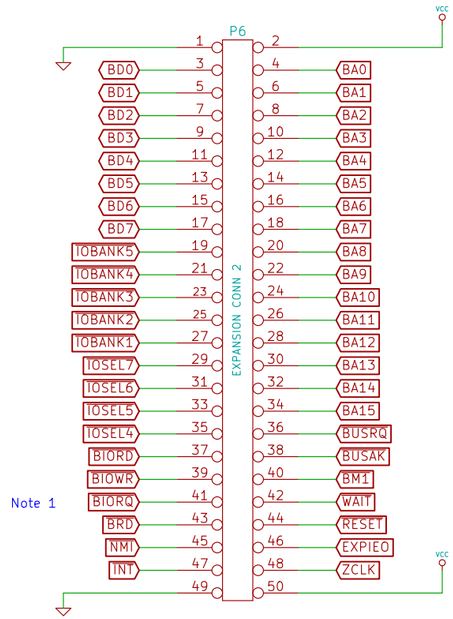




| | | |
|---|---|---|
| NAME_THIS_THING | | |
| *Three Farthing Labs* | | |
| File: wde8016-6.sch | | |
| Sheet: /Power & Misc/ | | |
| *Title: wde8016* | | |
| Size: B | *Date: 13 feb 2017* | *Rev: 0* |
| KiCad E.D.A. | | Id: 6/7 |

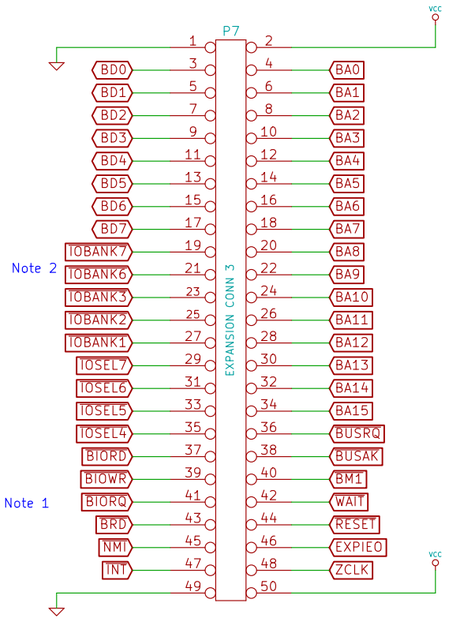
EXPANSION CONNECTOR 1



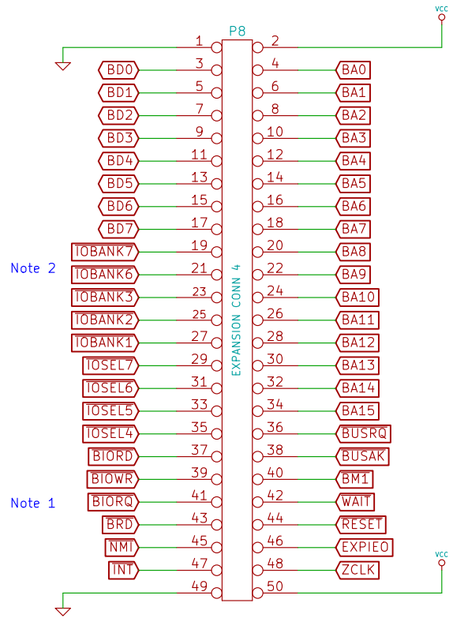

EXPANSION CONNECTOR 2




EXPANSION CONNECTOR 3




EXPANSION CONNECTOR 4




Note 1

Including the buffered IORQ and RD signals so Zilog-family devices can be used on expansion cards (these are required), even though we are already including decoded BIORD and BIOWR (for simple interfacing).

We do not include BMEMRD nor BMEMWR since architecture leaves no room for addtional memory on the expansion bus.

Note 2

On Connectors 3 & 4 pins 19 & 21 (/IOBANK5 & /IOBANK4, repectively) are replaced by /IOBANK7 & /IOBANK6 in order to make the full range of on-board decoded I/O strobes available to expansion modules.

| | |
|---|---|
| File: wde8016-7.sch | |
| Sheet: /Expansion Bus/ | |
| Title: | |
| Size: USLedger Date: 13 feb 2017 | Rev: |
| KiCad E.D.A. | Id: 7/7 |