

PicoTracer 370

A semiconductor curve tracer built on the Raspberry Pi Pico
Hardware design document, block diagrams and firmware specification

Target	Raspberry Pi Pico (RP2040), MicroPython 1.22 or later
Display	3.5 inch 480 x 320 TFT, ILI9488 or ST7796, SPI
Analog front end	Discrete op-amp collector supply, Howland step generator
Measurement	12-bit SPI ADC with programmable gain, 7 current ranges
Panel	4 rotary encoders, 12 buttons, 4 lamps, 3 x MCP23017 over I2C
Envelope	+/-24 V, 1.5 A peak, 2 uA to 2 A, 20 W average
Revision	1.0 - design release, firmware not included

This document describes hardware that generates voltages capable of destroying components and delivering a painful shock. Read section 3 before building anything.

1. Introduction and scope

A curve tracer answers one question: what does this device do when I push current or voltage into it. It answers by sweeping a voltage across the device under test while stepping a second stimulus into the control terminal, and plotting one against the other. Everything else - ranges, cursors, storage - is convenience built around that single loop.

This document specifies a complete instrument that performs that loop with a Raspberry Pi Pico, an SPI colour LCD and a discrete analog front end. It is organised so that each block can be built and tested on its own: the power supply first, then the measurement chains, then the sources, then the panel. Every block section states what the block does, how it is wired pin by pin, and which equations govern its component values.

The firmware is specified but not written. Section 17 defines the architecture, section 18 defines the state machines in full, and section 19 defines the calibration data they consume. Anyone implementing the firmware should be able to work from those three sections without redesigning anything.

1.1 What this instrument is not

The original Tektronix 370 reaches 2000 V and 20 A. That envelope needs isolation, interlocks and a mechanical design discipline that does not belong in a hobby build, and the failure mode is electrocution rather than a blown transistor. This design deliberately stops at 24 V and 1.5 A, which covers small-signal and medium-power devices, logic-level MOSFETs, diodes, LEDs, zeners up to 20 V and thyristors of modest rating. The architecture scales: raising the rails means changing the pass devices, the attenuator ratio and the clearances, and nothing else.

1.2 Conventions

- **Collector** means the swept terminal, whatever the device: collector, drain, anode.
- **Step** means the controlled terminal: base, gate, thyristor gate. The step generator drives it.
- **Emitter** means the common terminal: emitter, source, cathode. It carries the sense shunt.
- Resistor values are given in ohm, k and M. Capacitor values in nF and uF.
- Signal names in capitals with an underscore prefix mean active low, for example /CS_ADC.

2. Specification

Parameter	Value	Notes
Collector sweep	+/-24 V bipolar	three ranges: 2.56 V, 10.24 V, 24 V full scale
Collector current	1.5 A peak, 15 % duty	hardware limit 1.38 A per rail
Sweep resolution	12 bit, 512 points per ramp	1.25 / 5.0 / 11.7 mV per code by range
Ramp duration	20 ms nominal, 5 to 200 ms	software selectable
Step generator, current	+/-4 uA to +/-40 mA	5 ranges, 11 bit signed resolution
Step generator, voltage	+/-2.56 V and +/-10.24 V	for MOSFET, JFET and IGBT gates
Number of steps	0 to 10	plus an offset of -5 to +5 steps
Current measurement	2 uA to 2 A full scale	7 shunt ranges x PGA 1 to 32
Current resolution	1 nA on the most sensitive range	noise limited to about 4 nA rms
Voltage measurement	+/-2.45 V and +/-24.5 V	1.2 mV and 12 mV per code
Basic accuracy	0.5 % of reading + 0.1 % of range	after two-point calibration at 25 C
Family update rate	3.6 families per second	11 curves, 20 ms ramps
Display	480 x 320, 10 x 10 graticule	22 ms full redraw on core 1
Storage	microSD, PNG screenshot and CSV	same SPI bus as the LCD
Supply	2 x 24 V / 1.5 A isolated bricks	about 40 W worst case

Table 1 - Instrument specification.

3. Safety envelope

The collector node reaches 24 V with respect to ground and can deliver 1.5 A. That is not lethal, but it will vaporise a bond wire, burn skin through a dropped probe, and destroy the instrument if the sense return opens while the supply is armed. The rules below are design requirements, not advice.

1. **Armed state is explicit.** The output relay K_OUT is energised only while GP27 is high. A 100 k pull-down holds it open during reset, boot and firmware crash.
2. **Disarmed means discharged.** K_DISCH connects a 1 k / 5 W bleeder across the DUT whenever the instrument is not armed. The reservoir capacitors fall below 1 V in under 200 ms.
3. **Two independent current limits.** A transistor-level limit inside the power stage acts in microseconds and needs no firmware. A firmware limit acts on the measured shunt current and implements the user's power setting.
4. **Break before make.** The socket selector and the shunt bank must never short two ranges together. Firmware opens all relays, waits 5 ms, then closes the chosen one.
5. **Never change a shunt while armed.** Opening the emitter return with current flowing puts the full rail across the DUT. Range changes are queued and applied between families.
6. **The socket is guarded.** A lid or a recessed socket, plus a red lamp driven from the same signal that energises K_OUT, not from a separate firmware flag.

4. System architecture

Figure 1 shows the whole instrument. The Pico sits between two worlds. On the digital side it owns the display, the panel and the calibration memory. On the analog side it owns two DACs that create the stimuli and one ADC that reads back the result, with the range switching handled by I2C expanders that are never touched inside a sweep.

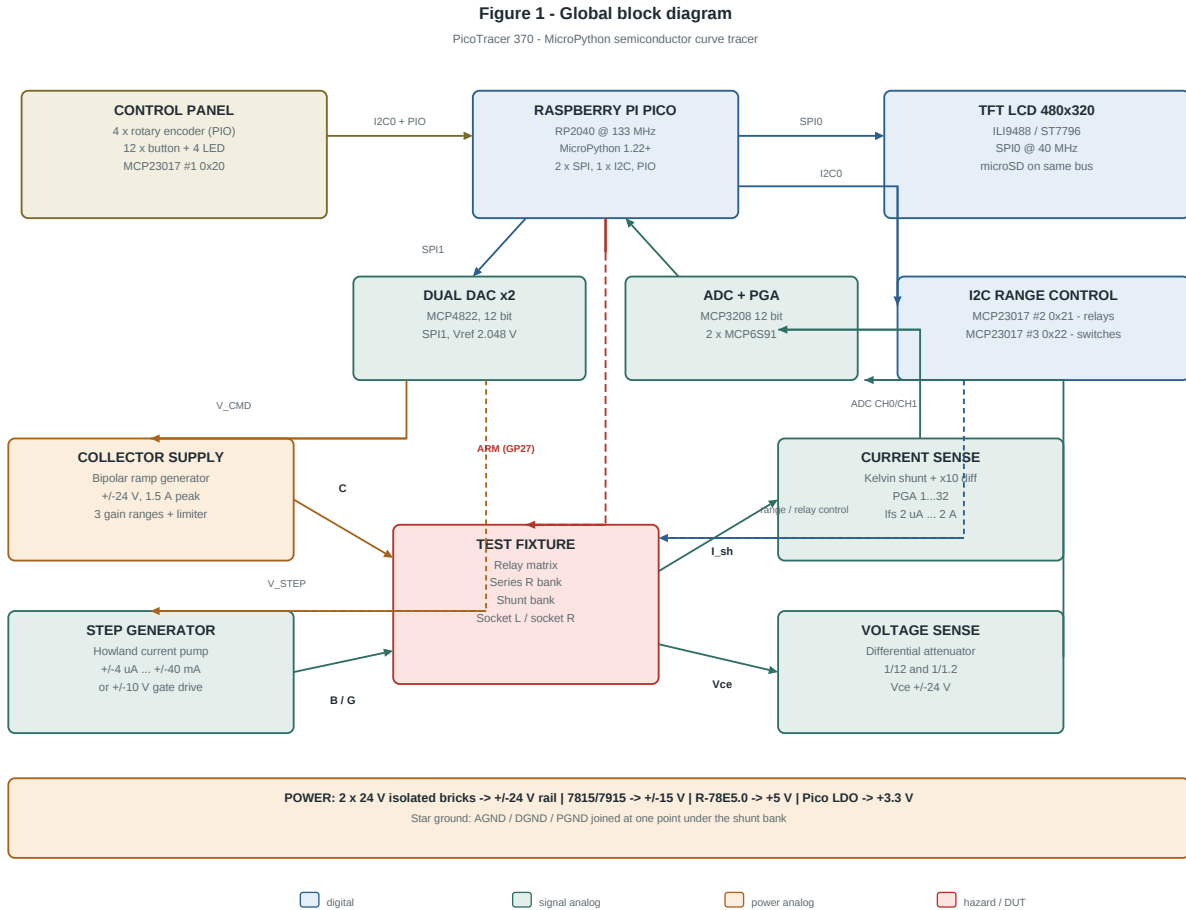


Figure 1 - Global block diagram. Solid arrows carry signals, dashed arrows carry control.

4.1 The measurement loop

One point of one curve costs 39 microseconds and consists of three transfers: write the next ramp code to the collector DAC, read the current channel, read the voltage channel. Nothing else happens in that window - no I2C, no allocation, no display work. 512 of those points make one curve, eleven curves make one family, and the family is handed to the second core for rendering while the first core starts the next one.

4.2 Why the emitter carries the shunt

The obvious place for a current shunt is the collector line, but there the common-mode voltage swings over the full 48 V range and every amplifier that can survive it costs resolution. Putting the shunt in the emitter return keeps the common mode within a few hundred millivolts of ground, so an ordinary precision op-amp does the job. The price is that the emitter no longer sits exactly at ground: it floats by $I \times R_{\text{shunt}}$, up to 205 mV. Two design choices absorb that error. The collector-emitter voltage is measured differentially across the device, not from collector to ground, so the float cancels. And the step generator takes its reference from the emitter sense node, so the base drive is referred to the real emitter potential rather than to ground.

4.3 Division of labour

Block	Owns	Bandwidth	Failure behaviour
Collector supply	sweep voltage, hardware current limit	DC to 20 kHz	folds back, then trips K_OUT
Step generator	base current or gate voltage	DC to 5 kHz	clamps to +/-15 V, never latches
Current chain	shunt selection, gain, zero	DC to 25 kHz	saturates at rail, flagged as over-range
Voltage chain	attenuation, gain, zero	DC to 80 kHz	saturates, flagged as compliance error
Fixture	socket routing, series R, discharge	static	opens on loss of coil supply
Panel	user intent	human	buttons ignored while a fault is latched

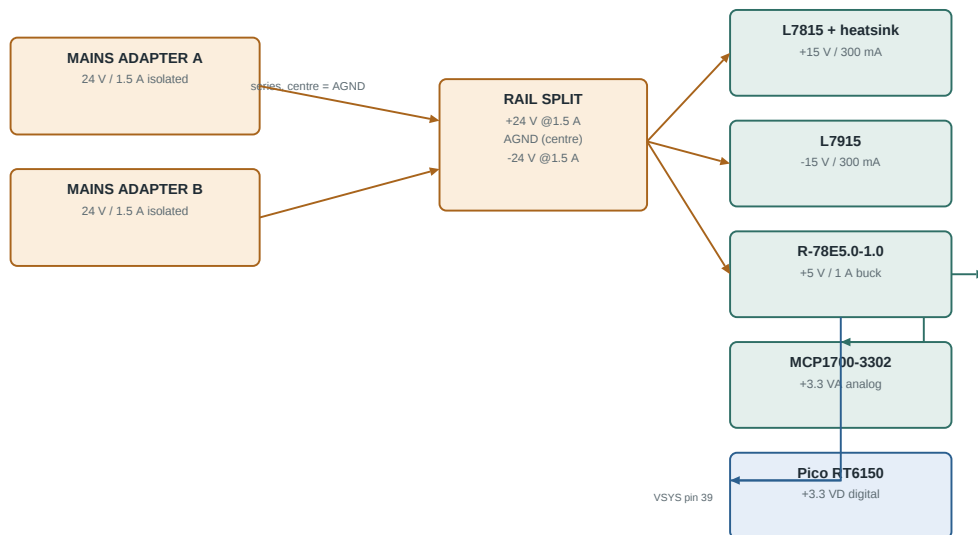
Table 2 - Responsibility of each hardware block.

5. Power supply

Two isolated 24 V bricks in series give a clean bipolar rail without a transformer, a bridge or mains wiring inside the box. The junction between them becomes analog ground. Because both bricks are isolated, this is legal and safe; using two non-isolated supplies would short one of them.

Figure 2 - Power distribution tree

All rails, currents and decoupling



Rail loading

+15 V / -15 V	OPA2197 x3, OPA197, DG408/DG409, INA gain stage
+5 V	MCP4822 x2, MCP3208, MCP6S91 x2, REF3040, relays (via ULN2803)
+3.3 V A	MCP23017 x3 pull-ups, analog-side buffers
+3.3 V D	Pico core, LCD logic, microSD, 74LVC125
+24 V / -24 V	Collector power stage rails only (MJE15032/33 pair)

Decoupling: 100 nF X7R at every IC pin + 10 uF tantalum per rail per board section; power stage rails get 1000 uF / 35 V local reservoirs.

Figure 2 - Power distribution. Every rail is derived from the same pair of bricks.

5.1 Rail sizing

Thermal and reservoir sizing

Power stage worst case	$P_q = (V_{rail} - V_{ce}) \times I = 24 \text{ V} \times 1.38 \text{ A} = 33 \text{ W}$ at $V_{ce} = 0$
Duty limited average	$P_{avg} = P_q \times t_{ramp} / t_{period} = 33 \times 20 \text{ ms} / 200 \text{ ms} = 3.3 \text{ W}$
Heatsink requirement	$R_{th_sa} \leq (T_{j_max} - T_a) / P_{avg} - R_{th_jc} - R_{th_cs}$ $R_{th_sa} \leq (125 - 40) / 3.3 - 1.0 - 0.5 = 24 \text{ C/W} \rightarrow$ a small clip-on works
Transient junction rise	$dT_j = P_q \times Z_{th}(20 \text{ ms}) = 33 \times 0.35 = 11.5 \text{ C}$ (MJE15032 in T0-220)
Linear regulator loss	$P = (24 - 15) \times 0.3 \text{ A} = 2.7 \text{ W}$ in each of the 7815 / 7915
Reservoir sag	$dV = I \times t / C = 1.38 \text{ A} \times 20 \text{ ms} / 2200 \text{ uF} = 12.5 \text{ V} \rightarrow$ use 4700 uF

The reservoir calculation is the one people get wrong. During a 20 ms ramp at full current the brick cannot follow, so the local reservoir supplies the difference. Size it for less than 2 V of sag: $C \geq I \times t / dV = 1.38 \times 0.02 / 2 = 13800 \text{ uF}$, or accept a lower peak current on the highest range. This design uses 2 x 6800 uF per rail and limits the 24 V range to 1.0 A.

5.2 Grounding

- **PGND** carries the power stage return and the reservoir ripple. Wide pour, own path.
- **AGND** is the reference for the DACs, the ADC, the reference and all the amplifiers.
- **DGND** carries the Pico, LCD, SD card and expander returns.
- The three meet at exactly one point, physically under the shunt bank, because that is where the measurement is defined. Anywhere else and shunt current flows in the reference path.
- The 4.096 V reference gets its own star from AGND at the ADC pin, with a 10 uF plus 100 nF pair.

6. Controller and pin allocation

Figure 3 - Raspberry Pi Pico pin allocation

Every GPIO accounted for

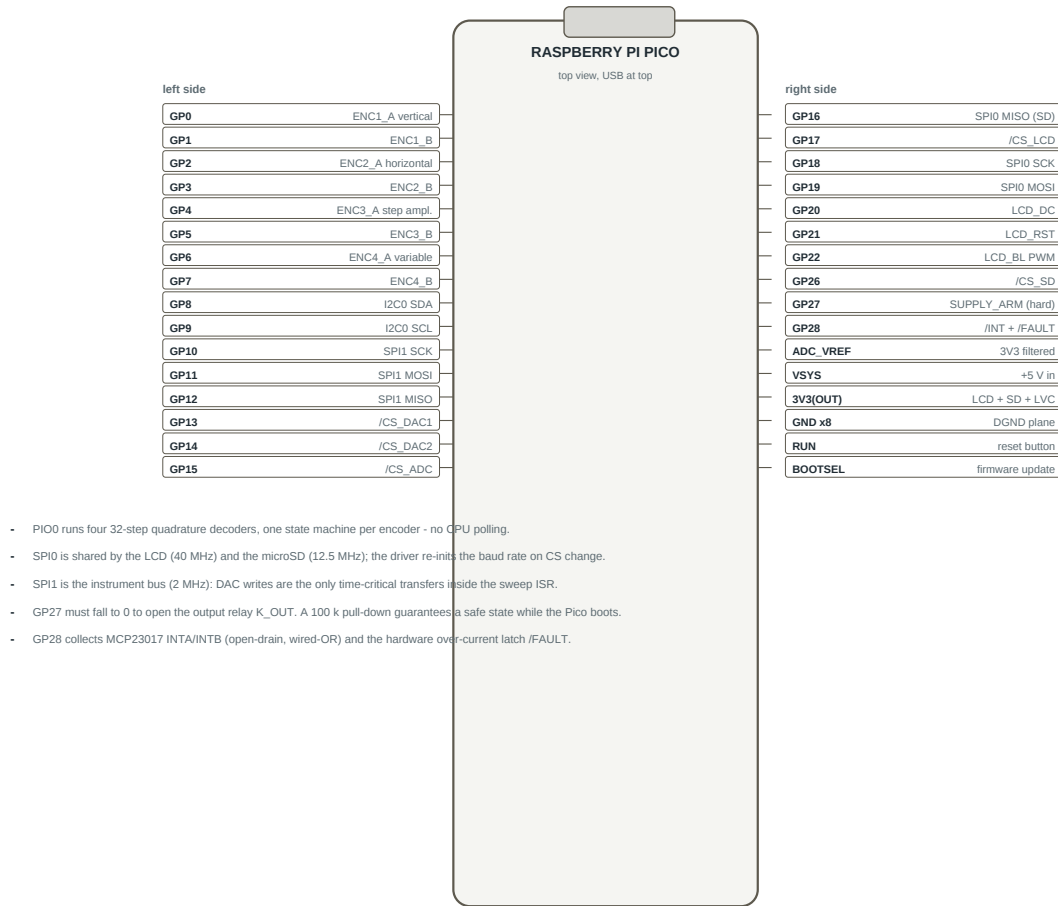


Figure 3 - Pico pin allocation. All 26 GPIO are assigned.

The allocation is driven by three constraints. The four encoders need eight consecutive pins so that four PIO state machines can be instantiated from one program. The two SPI ports must use their hardware pin groups. And the arm signal must be a pin with a pull-down that survives reset.

Pin	Net	Direction	Connects to	Electrical
GP0 / GP1	ENC1_A / ENC1_B	in	vertical encoder	10 k to 3V3, 100 nF to GND
GP2 / GP3	ENC2_A / ENC2_B	in	horizontal encoder	10 k to 3V3, 100 nF to GND
GP4 / GP5	ENC3_A / ENC3_B	in	step amplitude encoder	10 k to 3V3, 100 nF to GND
GP6 / GP7	ENC4_A / ENC4_B	in	variable supply encoder	10 k to 3V3, 100 nF to GND
GP8	SDA	bidir	MCP23017 x3, 24LC256	2.2 k pull-up to 3V3
GP9	SCL	out	same	2.2 k pull-up to 3V3
GP10	SPI1_SCK	out	74HCT125 -> DAC1, DAC2, ADC, PGA	33 ohm series at the source
GP11	SPI1_MOSI	out	same	33 ohm series
GP12	SPI1_MISO	in	74LVC125 from ADC	5 V tolerant input, 3V3 supply

Pin	Net	Direction	Connects to	Electrical
GP13	/CS_DAC1	out	MCP4822 #1 pin 2	via 74HCT125
GP14	/CS_DAC2	out	MCP4822 #2 pin 2	via 74HCT125
GP15	/CS_ADC	out	MCP3208 pin 10	via 74HCT125
GP16	SPI0_MISO	in	microSD DO	direct 3V3
GP17	/CS_LCD	out	LCD CS	direct
GP18	SPI0_SCK	out	LCD SCK, SD CLK	33 ohm series
GP19	SPI0_MOSI	out	LCD SDI, SD DI	33 ohm series
GP20	LCD_DC	out	LCD data / command	direct
GP21	LCD_RST	out	LCD reset	10 k pull-up
GP22	LCD_BL	out	backlight gate	PWM 1 kHz into a 2N7002 + 10 ohm
GP26	/CS_SD	out	microSD CS	10 k pull-up
GP27	SUPPLY_ARM	out	ULN2803 in1 -> K_OUT coil	100 k pull-down, mandatory
GP28	/INT	in	MCP23017 INTA x3 + /FAULT	open drain, 4.7 k pull-up

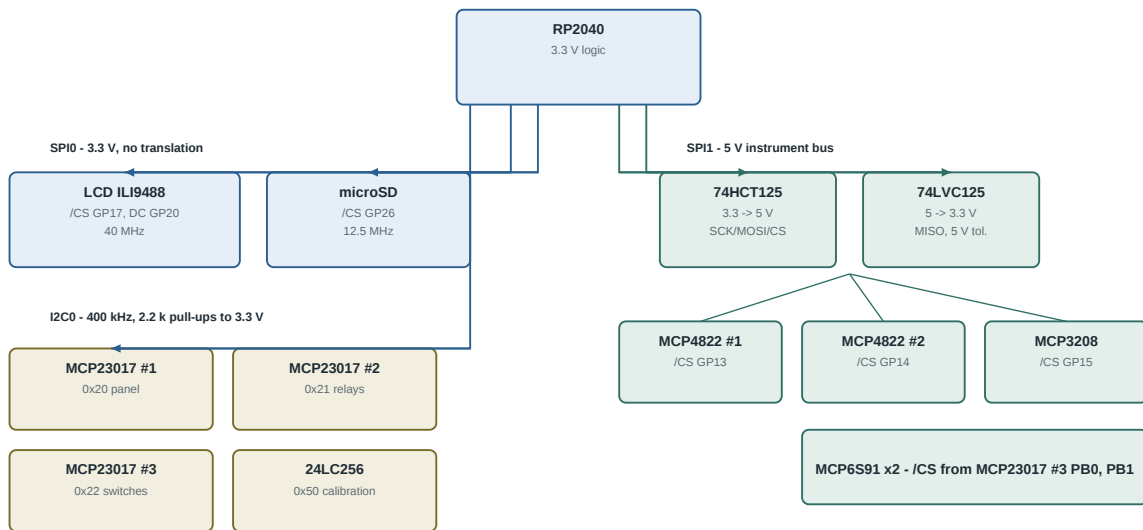
Table 3 - Pico pin-by-pin connection list.

GP23, GP24, GP25 and GP29 are used internally by the Pico module for the SMPS mode, VBUS sense, the on-board LED and VSYS sensing. Do not repurpose GP23: forcing the regulator into PWM mode with a firmware write is, however, worth doing at boot, because it drops the 3.3 V rail ripple from about 20 mV to under 5 mV and that ripple lands directly on the ADC reference divider.

6.1 Digital bus map

Figure 9 - Digital bus map and level translation

SPI0, SPI1 and I2C0 device tree



- Bus speeds: SPI0 40 MHz for the panel, dropped to 12.5 MHz while the SD card CS is low.
- SPI1 is fixed at 2 MHz. One DAC write is 16 bits = 8 us, one ADC conversion is 15 clocks + acquisition = 20 us.
- MCP6S91 chip selects sit on an expander because gain changes only happen between sweeps, never inside the ISR.
- I2C is never used inside the sweep ISR. Range changes are queued and applied in the IDLE state.
- The EEPROM holds the calibration record: 7 current ranges x (gain, offset) + 2 voltage ranges + DAC endpoints.

Figure 4 - Bus topology and level translation between the 3.3 V core and the 5 V instrument bus.

The DAC, the ADC and the PGAs run from 5 V so that they can use a 4.096 V reference and give a convenient 1 mV per code. Their logic thresholds are 0.7 times Vdd, which is 3.5 V, above what the Pico delivers, so every

line going out is buffered by a 74HCT125 running on 5 V - HCT inputs recognise 2.0 V as a high, so a 3.3 V drive is comfortably valid. The single line coming back, MISO, passes through a 74LVC125 running on 3.3 V, whose inputs tolerate 5 V.

Bus	Speed	Devices	Chip select	Used inside the sweep ISR
SPI0	40 MHz / 12.5 MHz	LCD, microSD	GP17, GP26	no
SPI1	2 MHz	MCP4822 x2, MCP3208, MCP6S91 x2	GP13, GP14, GP15, expander	yes, DAC and ADC only
I2C0	400 kHz	MCP23017 x3, 24LC256	addresses 0x20, 0x21, 0x22, 0x50	never

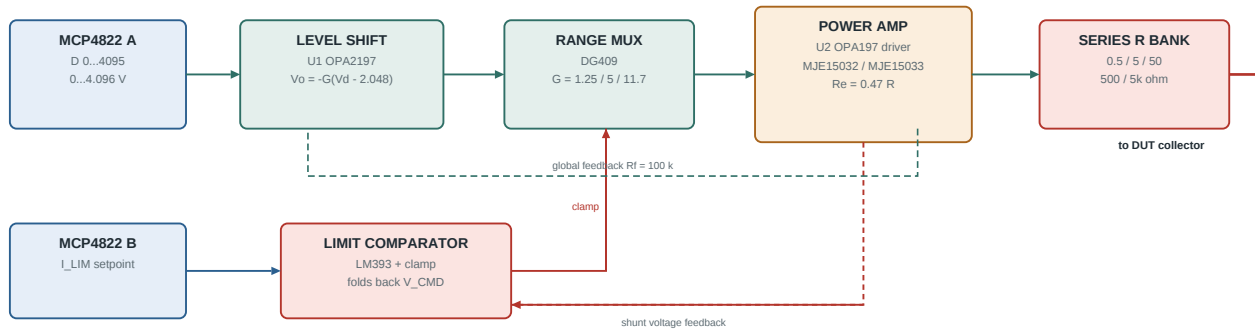
Table 4 - Bus assignment. The prohibition on I2C inside the ISR is a hard rule, not a preference.

7. Collector supply

The collector supply turns a 12-bit code into a bipolar voltage that can source and sink over an amp. It is a classic composite amplifier: a precision op-amp sets the transfer function, a complementary emitter follower inside the feedback loop provides the current, and a pair of transistors sensing the emitter resistors provides an instantaneous current limit.

Figure 4 - Collector supply: ramp generator and power stage

Bipolar, three ranges, programmable current limit



Design equations

DAC output $V_d = 2.048 \times D / 4096 \times 2$ (12 bit, gain x2, $D = 0 \dots 4095$)

Ramp command $V_{cmd} = -G \times (V_d - 2.048)$ G set by DG409

Full scale per range $G = 1.25 \rightarrow \pm 2.56 \text{ V} \mid G = 5 \rightarrow \pm 10.24 \text{ V} \mid G = 11.72 \rightarrow \pm 24.0 \text{ V}$

Ramp resolution $dV = 2 \times 2.048 \times G / 4096 = 1.25 \text{ mV} / 5.0 \text{ mV} / 11.7 \text{ mV}$ per code

Load line $V_{ce} = V_{cmd} - I \times (R_{series} + R_{shunt} + R_{wire})$

Bias network $V_{bias} = 2 \times V_{be}(Q3) \times (1 + R_6/R_5)$, set for 20 mA quiescent

Hardware limit $I_{lim} = V_{be}(on) / R_e = 0.65 / 0.47 = 1.38 \text{ A}$ per rail

Programmable limit $I_{lim}(prog) = V_{dac_B} / (10 \times R_{shunt})$ via the x10 sense pre-amp

Pass device SOA $P_q = (V_{rail} - V_{ce}) \times I$ worst case at $V_{ce} = 0$

Thermal $T_j = T_a + P \times (R_{th_jc} + R_{th_cs} + R_{th_sa}) \leq 125 \text{ C}$

Duty budget $P_{avg} = P_{peak} \times t_{sweep} / t_{period} \leq 8 \text{ W}$ with a 1.5 C/W heatsink

Figure 5 - Collector supply chain with the design equations.

7.1 Transfer function

The DAC is unipolar, the output must be bipolar, so the level shift subtracts half scale. Writing code 2048 gives zero volts out, code 0 gives the positive extreme and code 4095 the negative one, or the other way round depending on the inverting stage. The firmware hides the sign; the operator sees a polarity button.

Sweep generation

$$V_{dac} = 2.048 \times D / 4096 \times 2$$

$$V_{cmd} = -G \times (V_{dac} - 2.048)$$

$$G = R_f / R_i = 1.25 \mid 5.0 \mid 11.72$$

$$V_{out} = V_{cmd}$$

$$V_{ce} = V_{out} - I \times (R_{series} + R_{shunt})$$

$$dV/dD = 2 \times 2.048 \times G / 4096$$

$D = 0 \dots 4095$, MCP4822 with gain bit = 1

G from the DG409 range mux

$R_f = 25k \mid 100k \mid 234k$ with $R_i = 20k$

power stage is unity gain inside the loop

the load line the operator actually sees

1.25 mV $\mid$ 5.0 mV $\mid$ 11.7 mV per code

7.2 Power stage

The driver op-amp is an OPA197: rail to rail, 36 V capable, 10 MHz, and unconditionally stable driving the follower base network. The pass devices are an MJE15032 / MJE15033 complementary pair, chosen for their 50 W rating and 4 MHz transition frequency, which keeps the composite loop stable without heroic compensation. Each emitter carries a 0.47 ohm resistor, which does three jobs: it sets the current limit, it stabilises the

quiescent point against thermal runaway, and it isolates the two devices during crossover.

Power stage design

Bias $V_{bias} = 2 \times V_{be} \times (1 + R_6/R_5)$ V_{be} multiplier on the heatsink, set for 20 mA I_q

Current limit $I_{lim} = V_{be(on)} / R_e = 0.65 / 0.47 = 1.38 \text{ A}$

Loop stability $C_{comp} = 100 \text{ pF}$ across R_f , plus 10 ohm + 100 nF Zobel at the output

Slew needed $SR = dV/dt = 48 \text{ V} / 5 \text{ ms}$ (fastest ramp) = 9.6 kV/s = 0.0096 V/us -> trivial

Output Z $Z_{out} = Z_{ol} / (1 + A \times \beta) < 20 \text{ mohm}$ below 1 kHz

Cap. load up to 10 uF tolerated thanks to the 10 ohm isolation resistor before the Zobel

7.3 Programmable limiter

The operator sets a power limit on the panel. Firmware converts it to a current threshold at the present voltage and writes it to the second DAC channel. An LM393 compares the amplified shunt voltage with that threshold and, when it is exceeded, pulls charge out of the ramp integrator through a diode, folding the command back. The result on screen is exactly what a real curve tracer shows: the curve bends over along a constant-power hyperbola instead of running off scale.

Limiter

Threshold code $D_{lim} = 4096 \times (10 \times R_{shunt} \times I_{lim}) / 4.096 / 2$ for the x10 sense preamp

Power mode $I_{lim}(V) = P_{set} / \max(|V_{ce}|, V_{floor})$ with $V_{floor} = 0.25 \text{ V}$ to avoid a pole

Response $t_r = C_{int} \times dV / I_{pull} = 1 \text{ nF} \times 1 \text{ V} / 1 \text{ mA} = 1 \text{ us}$

Hysteresis 10 mV at the comparator input, about 1 % of range, prevents chatter

8. Step generator

Bipolar transistors want current into the base, field effect devices want voltage on the gate. The step generator does both: an improved Howland current pump for the current ranges and a plain amplifier for the voltage ranges, selected by a DG419 at the output.

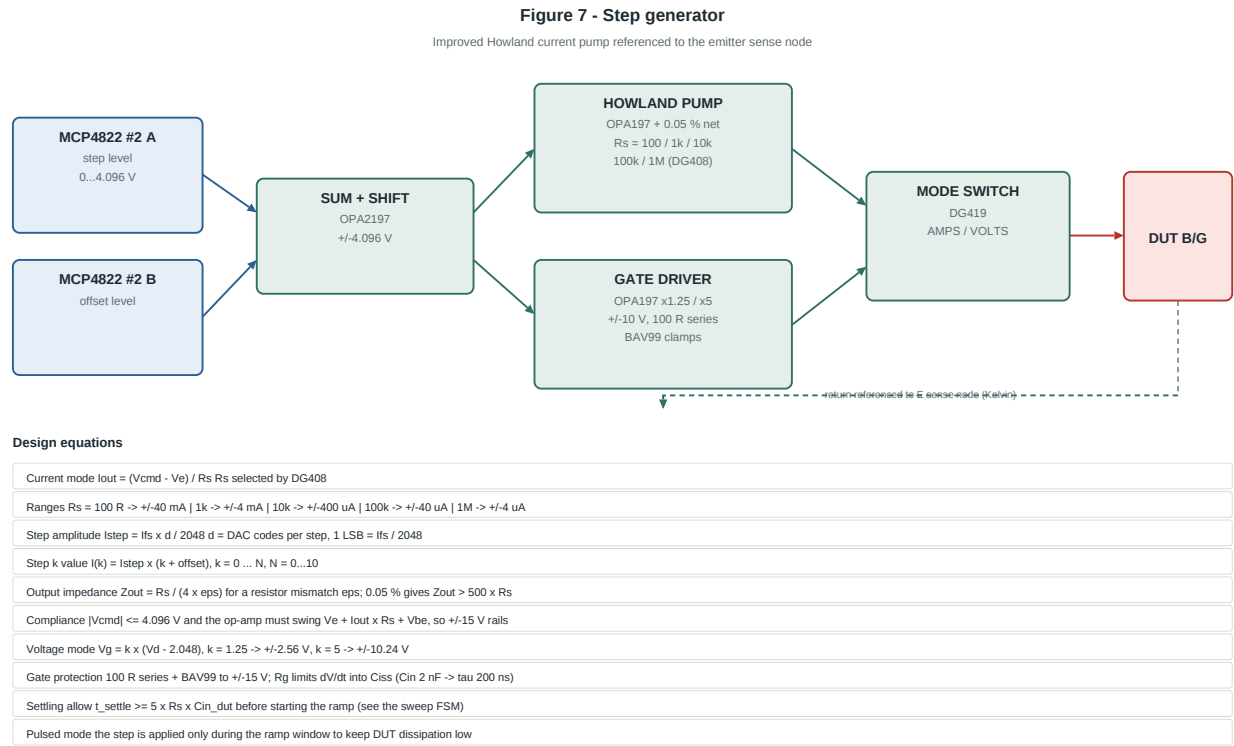


Figure 6 - Step generator, both modes, with the range switching and the equations.

8.1 The Howland pump and why the resistors matter

A Howland pump is a current source whose output impedance depends entirely on how well four resistors match. With perfect matching the output impedance is infinite; with a fractional mismatch of epsilon it collapses to roughly R divided by four epsilon. For a base current source feeding a transistor whose input impedance changes by decades across the sweep, that output impedance is the difference between a real family of curves and a smeared one.

Current mode		
Ideal	$I_{out} = (V_{cmd} - V_e) / R_s$	
Real	$Z_{out} \approx R_s / (4 \times \text{eps})$	eps = fractional resistor mismatch
Requirement current	$Z_{out} > 100 \times r_{in}(DUT)$	r_{in} of a BJT base can be 100 ohm at high c
Choice e.	0.05 % thin film $\rightarrow Z_{out} > 500 \times R_s$, so 50 k on the 100 ohm range. Ampl	
Compliance headroom	V_{op} must reach $V_e + I_{out} \times R_s + V_{be}(DUT)$; $\pm 15\ \text{V}$ rails give 14 V of	
Ranges 4 μA	$R_s = 100 \mid 1\ \text{k} \mid 10\ \text{k} \mid 100\ \text{k} \mid 1\ \text{M} \rightarrow \pm 40\ \text{mA} \mid 4\ \text{mA} \mid 400\ \mu\text{A} \mid 40\ \mu\text{A} \mid$	
Step size	$I_{step} = I_{fs} \times d / 2048$	$d = \text{DAC codes per step}$
Curve k	$I(k) = I_{step} \times (k + \text{offset})$	$k = 0 \dots N$, offset = -5...+5

8.2 Voltage mode

For MOSFETs and IGBTs the same DAC drives a non-inverting stage with a switchable gain of 1.25 or 5, giving +/-2.56 V for JFETs and small logic-level parts and +/-10.24 V for standard gates. A 100 ohm series resistor and a BAV99 clamp pair protect both the amplifier and the device; with a 2 nF input capacitance the resulting 200 ns time constant is invisible against a 20 ms ramp.

8.3 Settling before the ramp

The single most common cause of ugly curves is starting the ramp before the step has settled. The sweep state machine therefore holds a settling state whose duration is computed, not guessed.

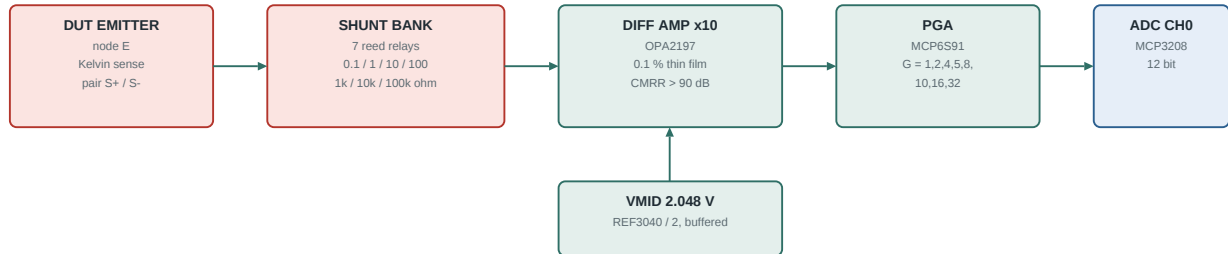
```
t_settle = 5 x R_s x C_in(DUT)          worst case 5 x 1 M x 2 nF = 10 ms on the 4 uA range
                                         with a floor of 200 us and a ceiling of 20 ms
```

For current ranges below 40 uA the firmware warns that the family rate will drop below 1 Hz.

9. Current measurement

Figure 5 - Current measurement chain

Kelvin low-side shunt bank, x10 difference stage, PGA, ADC



Rshunt	Full scale I	LSB (12 bit)	Burden at FS	Typical use
0.1 ohm	2.05 A	1.0 mA	205 mV	power BJT, MOSFET
1 ohm	205 mA	100 uA	205 mV	medium power
10 ohm	20.5 mA	10 uA	205 mV	small signal BJT
100 ohm	2.05 mA	1.0 uA	205 mV	JFET, low current hFE
1 k	205 uA	100 nA	205 mV	leakage, I _{ceo}
10 k	20.5 uA	10 nA	205 mV	gate leakage
100 k	2.05 uA	1.0 nA	205 mV	noise limited, average 16x

Sensed voltage $V_{sh} = I \times R_{shunt}$ (kept ≤ 205 mV by range selection)

Chain output $V_{adc} = 2.048 + 10 \times G_{pga} \times I \times R_{shunt}$

Reconstruction $I = (V_{adc} - V_{zero}) / (10 \times G_{pga} \times R_{shunt})$ with V_{zero} from calibration

Resolution $LSB_I = 4.096 / (4096 \times 10 \times G_{pga} \times R_{shunt})$

Burden correction $V_{ce_true} = V_{ce_meas} - I \times R_{shunt}$ (only if 2-wire sensing is used)

Noise floor $en = 12 \text{ nV}/\sqrt{\text{Hz}} \times \sqrt{1.57 \times \text{BW}} \times 10 \times G_{pga}$; average N sweeps $\rightarrow / \sqrt{N}$

Figure 7 - Current chain, range table and equations.

Seven decade shunts spanning 0.1 ohm to 100 k, a fixed times-ten difference amplifier and a programmable gain amplifier give a usable span from a couple of microamps to two amps. Every range is designed for the same 205 mV burden at full scale, which keeps the emitter float bounded and makes the correction term identical on every range.

9.1 Component choices

Function	Part	Why
Shunts 0.1 to 100 ohm	Vishay Z-foil or WSL series, 0.1 %, 25 ppm/C	self-heating shifts the reading; 25 ppm/C over a 20 C rise is 0.05 %
Shunts 1 k to 100 k	0.1 % thin film, 10 ppm/C	power is negligible, drift dominates
Range relays	reed, 1 A, 5 V coil, e.g. TQ2-5V	contact resistance under 100 mohm and, critically, thermal EMF under 1 uV
Difference amp	OPA2197 with a 0.1 % matched network	36 V capable, 0.1 uV/C offset drift
PGA	MCP6S91	SPI controlled, 1 to 32 in useful steps, 2 MHz bandwidth
Reference	REF3040, 4.096 V, 0.2 %	sets both the ADC span and the 2.048 V pseudo-ground

Table 5 - Current chain part selection.

9.2 Reconstruction and error budget

Current reconstruction

Reading $I = (V_{adc} - V_{zero}) / (10 \times G_{pga} \times R_{shunt})$

Code to volts $V_{adc} = 4.096 \times N / 4096$ $N = 0 \dots 4095$

Resolution	$\text{LSB}_I = 4.096 / (4096 \times 10 \times G_{\text{pga}} \times R_{\text{shunt}})$
Example	$R = 100 \text{ ohm}, G = 1 \rightarrow \text{LSB} = 1.0 \text{ uA}, \text{ full scale } 2.05 \text{ mA}$
	$R = 100 \text{ k}, G = 8 \rightarrow \text{LSB} = 0.125 \text{ nA}, \text{ full scale } 0.26 \text{ uA}$

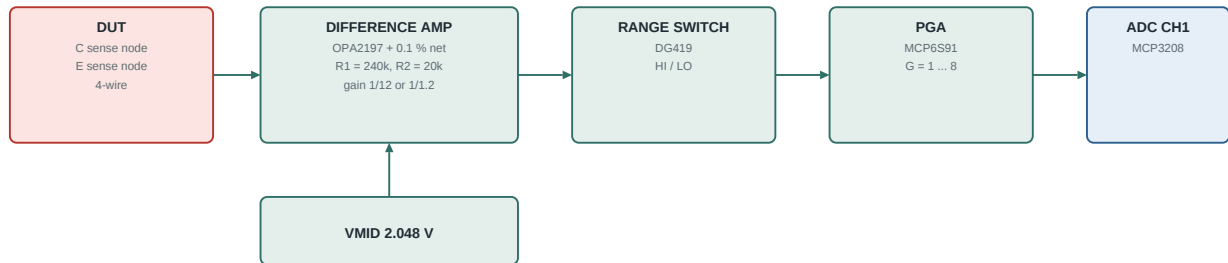
Error source	Magnitude	Removed by
Shunt tolerance	0.1 %	gain calibration per range
Difference amp gain error	0.1 %	gain calibration
PGA gain error	0.5 % typical	gain calibration per gain setting
Amplifier offset	25 uV $\rightarrow$ 2.5 uV at the shunt	zero calibration, re-measured before each family
Relay thermal EMF	under 1 uV	chopping the zero measurement; usually ignored
ADC INL	+/-1 LSB	not corrected, 0.025 % of range
Noise	about 40 uV rms at the ADC	averaging N families improves it by $\sqrt{N}$
Self heating	0.05 % on the low-value shunts	duty cycling

Table 6 - Current channel error budget. Total after calibration: 0.3 % of reading + 0.05 % of range.

10. Voltage measurement

Figure 6 - Voltage measurement chain

Differential collector-emitter sensing with two attenuation ranges



Design equations

HI range $V_{adc} = 2.048 + V_{ce} / 12 \rightarrow \pm 24.5$ V full scale, LSB 12 mV

LO range $V_{adc} = 2.048 + V_{ce} / 1.2 \rightarrow \pm 2.45$ V full scale, LSB 1.2 mV

Reconstruct $V_{ce} = (V_{adc} - V_{zero}) \times A$ A = 12 or 1.2, divided by G_{pga}

Divider $A = (R1 + R2) / R2 = (240k + 20k) / 20k \dots$ use 0.1 % matched network

CMRR $CMRR = 1 / (4 \times \text{tol}) \rightarrow 0.1$ % gives about 68 dB; use a matched array for 90 dB

Input Z 480 k differential; error at 1 M source impedance = 0.2 % $\rightarrow$ use the buffer option

Bandwidth $f_c = 1 / (2 \pi R2 C_f)$ with $C_f = 100$ pF $\rightarrow$ 80 kHz, well above the 25 kHz sample rate

Skew ADC channels are sequential; 20 us skew on a 20 ms ramp = 0.1 % of full scale.

Firmware corrects with a half-sample linear interpolation on the voltage channel.

Figure 8 - Voltage chain with two attenuation ranges.

The voltage channel measures across the device, not from the collector to ground. That single decision removes the shunt burden, the relay contact drops and the wiring resistance from the reading in one step, and it is the reason the socket has four terminals rather than three.

Voltage reconstruction

HI range $V_{adc} = 2.048 + V_{ce} / 12$ ± 24.5 V span, 12 mV per code

LO range $V_{adc} = 2.048 + V_{ce} / 1.2$ ± 2.45 V span, 1.2 mV per code

Reading $V_{ce} = (V_{adc} - V_{zero}) \times A / G_{pga}$

Attenuator $A = (R1 + R2) / R2 = (240k + 20k) / 20k = 13$, trimmed to 12 with the PGA

CMRR $CMRR \approx 1 / (4 \times \text{tol}) \rightarrow 0.1$ % gives 68 dB, a matched network gives 90 dB

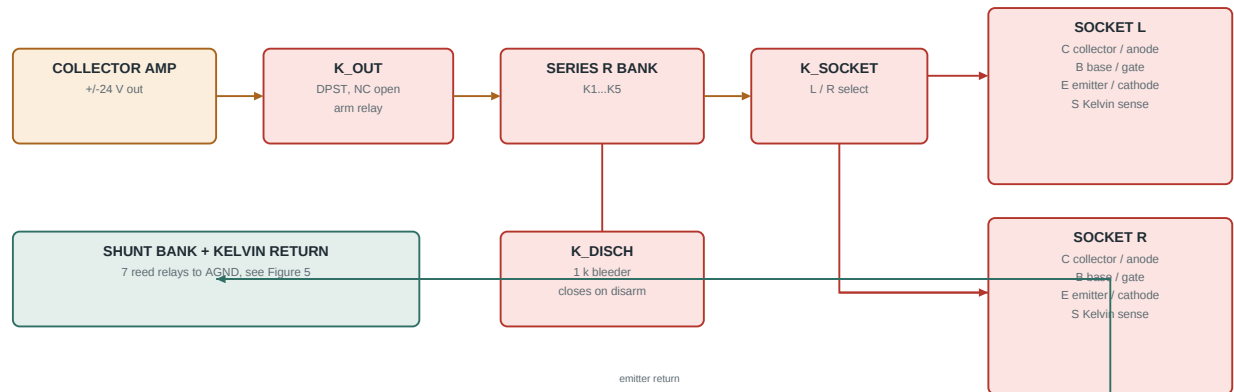
Bandwidth $f_c = 1 / (2 \pi R2 C_f) = 1 / (2 \pi \times 20k \times 100p) = 80$ kHz

Input current $I_{in} = V_{ce} / (R1 + R2) = 24 / 260k = 92$ uA, subtracted in software

The LO range exists for one reason: diode knees. Reading 0.65 V with 12 mV codes gives 54 counts and a visibly staircased curve. On the LO range the same knee gets 540 counts. The firmware switches automatically whenever the peak collector voltage of the previous family stayed below 2.2 V.

11. Test fixture, relay matrix and protection

Figure 8 - Test fixture, relay matrix and protection
Socket selection, series resistance, discharge and disconnect



Relay and protection schedule

K_OUT DPST 24 V 2 A	Opens both the collector line and the step line. Coil driven from GP27 through a ULN2803 channel, never from the expander, so firmware cannot leave it energised by accident.
K1...K5 reed 1 A	Series resistance 0.5 / 5 / 50 / 500 / 5k ohm. Exactly one closed; the decoder in firmware forbids the all-open state, which would leave the DUT unloaded.
K_SOCKET DPDT	Routes C, B, E and the sense pair to the left or right socket. Break-before-make.
K_DISCH SPST	1 k / 5 W bleeder across the DUT. Energised whenever the instrument is not armed, so reservoir and DUT capacitance are always discharged before the socket is touched.
Clamps 1.5KE33CA	Bidirectional TVS from the collector node to AGND, plus a 2 A fast fuse in the +24 V feed.

Figure 9 - Fixture routing, series resistance bank and protection schedule.

11.1 The series resistance bank

The series resistor is not a nuisance to be minimised. It sets the slope of the load line, and on a curve tracer that slope is what keeps a device alive while you look at its breakdown region. Five decade values cover everything from a power MOSFET in saturation to a leaky signal diode.

Series resistance

Load line $V_{ce} = V_{out} - I \times R_{total}$, $R_{total} = R_{series} + R_{shunt}$
Slope on screen $-1 / R_{total}$, in divisions: $(V/div) / (A/div) / R_{total}$
Short circuit $I_{sc} = V_{out} / R_{total} \rightarrow 24 V / 0.5 \text{ ohm} = 48 A \dots$ hence the 1.38 A limit
Choose R so $I_{sc} \leq 2 \times I_{expected}$, which keeps a shorted DUT from tripping the limiter
Power in R $P = I^2 \times R \rightarrow$ the 0.5 ohm needs 5 W, the 5 ohm needs 2 W, rest 0.5 W

11.2 Socket wiring

Terminal	Signal	Routed from	Relay	Notes
C	collector / drain / anode	series R bank output	K_SOCKET pole 1	red binding post, guarded
B	base / gate	step generator output	K_SOCKET pole 2	100 ohm series inside the fixture
E	emitter / source / cathode	shunt bank high side	K_SOCKET pole 3	carries the full DUT current

Terminal	Signal	Routed from	Relay	Notes
S+	collector sense	voltage chain +	K_SOCKET pole 4	no current, 240 k load
S-	emitter sense	voltage chain - and step return	K_SOCKET pole 5	defines the local ground

Table 7 - Socket terminal assignment, identical for the left and right positions.

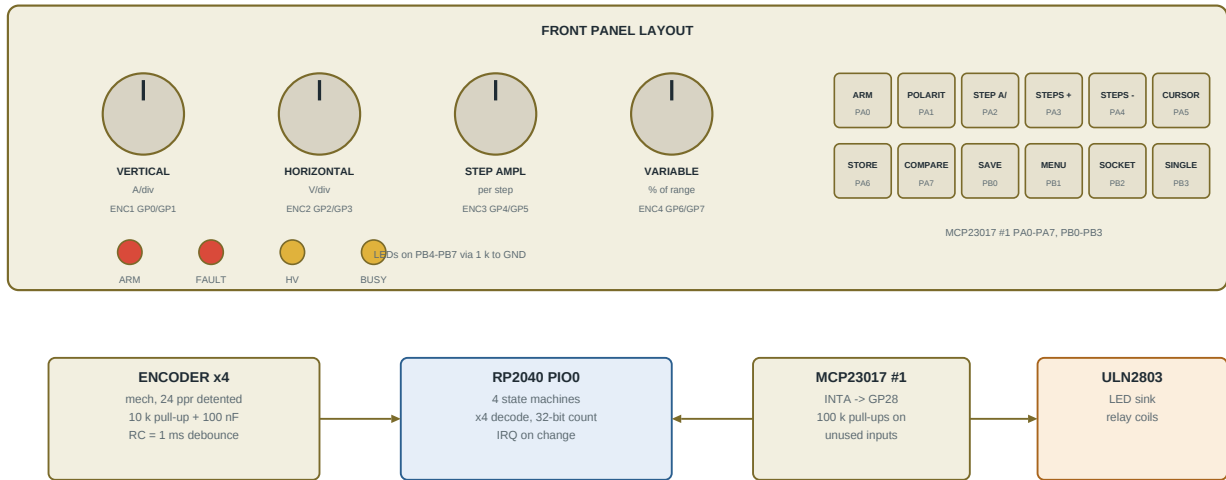
11.3 Protection tree

- **Fuse** 2 A fast in each 24 V feed, before the reservoirs.
- **TVS** 1.5KE33CA from the collector node to AGND, catching inductive kickback from motors and transformers presented as a DUT.
- **Series diode** not used - it would break bipolar operation. The reverse path is handled by the complementary pass device.
- **Gate clamp** BAV99 from the step output to both 15 V rails.
- **Thermal** a TMP236 bolted to the heatsink, read on ADC channel 2, trips at 85 C.
- **Rail watch** two dividers into ADC channels 3 and 4, checked once per family.

12. Control panel

Figure 10 - Control panel wiring

Four encoders on PIO, twelve buttons and four lamps on the expander



- Encoder acceleration: if two detents arrive within 60 ms the step multiplier goes to x10, above 8 detents/s to x100.
- Every encoder shaft has a push switch wired to MCP23017 #3 PA0-PA3; a push toggles coarse / fine on that parameter.
- Buttons are read only when INTA fires, then the whole GPIOA/GPIOB pair is read in one 2-byte I2C burst.
- Debounce is done in firmware with a 20 ms guard timer per key, long press is 700 ms and repeats every 120 ms.
- ARM is deliberately a momentary button, never a latching switch: power-up always lands in the safe state.

Figure 10 - Panel layout and the wiring behind it.

Four encoders cover the four continuously variable quantities. Everything else is a button, because a button that does one thing is faster than a menu that does five. The panel legend carries a second label in a different colour for the long-press function of each key.

12.1 Expander allocation

Device	Address	Port	Bits	Function
MCP23017 #1	0x20	GPIOA	PA0-PA7	buttons: ARM, POLARITY, STEP A/V, STEPS+, STEPS-, CURSOR, STORE, COMPARE
MCP23017 #1	0x20	GPIOB	PB0-PB3	buttons: SAVE, MENU, SOCKET, SINGLE
MCP23017 #1	0x20	GPIOB	PB4-PB7	lamps: ARM, FAULT, HV, BUSY, sunk through ULN2803
MCP23017 #2	0x21	GPIOA	PA0-PA6	shunt relays K_SH1 to K_SH7
MCP23017 #2	0x21	GPIOA	PA7	K_DISCH discharge relay
MCP23017 #2	0x21	GPIOB	PB0-PB4	series resistance relays K1 to K5
MCP23017 #2	0x21	GPIOB	PB5-PB6	K_SOCKET left / right
MCP23017 #2	0x21	GPIOB	PB7	spare, reserved for a second fixture
MCP23017 #3	0x22	GPIOA	PA0-PA3	encoder push switches
MCP23017 #3	0x22	GPIOA	PA4-PA5	collector range mux DG409 A0, A1
MCP23017 #3	0x22	GPIOA	PA6-PA7	step mode DG419, step gain select
MCP23017 #3	0x22	GPIOB	PB0-PB1	/CS for the two MCP6S91 PGAs
MCP23017 #3	0x22	GPIOB	PB2-PB4	step range DG408 A0, A1, A2
MCP23017 #3	0x22	GPIOB	PB5	voltage range DG419 HI / LO
MCP23017 #3	0x22	GPIOB	PB6-PB7	spare

Table 8 - I2C expander bit allocation. Every bit is named; no undocumented pins.

12.2 Encoder handling

Each encoder goes to a PIO state machine running a four-step quadrature decoder that maintains a signed 32-bit count. The CPU reads the count when it feels like it and takes the difference; no interrupts are lost even during a 20 ms sweep with interrupts disabled, which is exactly why the decoders live in PIO rather than in GPIO interrupt handlers.

Detent to step	<code>delta_param = delta_count / 4 x accel</code>
Acceleration	<code>accel = 1 if the gap between detents > 60 ms</code> <code>accel = 10 if 15 ms < gap <= 60 ms</code> <code>accel = 100 if gap <= 15 ms</code>
Range knobs	<code>always accel = 1, they are discrete lists and skipping ranges is confusing</code>
Variable knob	<code>accel applies, and a shaft push toggles a 0.1 % fine mode</code>

13. Display subsystem

A 480 x 320 panel divides neatly into a 320 x 320 plotting area with a 10 x 10 graticule of 32 pixels per division, and a 160 pixel column for the readout. That is the same proportion the original instrument uses, and it means one division is a round number of pixels, which keeps the graticule crisp without anti-aliasing.

Region	Pixels	Content	Redraw cost
Graticule	320 x 320 at x=0	10 x 10 grid, centre cross, tick marks	3.1 ms, cached as a pattern
Traces	same area	up to 11 curves x 512 points, decimated to 320	11 ms for a full family
Readout	160 x 220 at x=320	vertical, horizontal, per step, Rs, peak	1.2 ms, only on change
Cursor	overlay	dot, crosshair or window plus values	0.8 ms, XOR blit
Status bar	480 x 32 at y=288	socket, device, polarity, arm state	0.5 ms

Table 9 - Display budget. Full redraw 16.6 ms, comfortably inside the 277 ms family period.

The plot is drawn on core 1 into an off-screen buffer of 320 x 320 at 8 bits per pixel with a 16-colour palette, which costs 102 kB. The RP2040 has 264 kB, so one buffer plus the sample arrays fits with room to spare, and there is no tearing because the buffer is pushed over SPI only when it is complete. At 40 MHz that push takes $320 \times 320 \times 16 \text{ bits} / 40 \text{ Mbit/s} = 41 \text{ ms}$, so the design uses dirty-rectangle updates: only the columns that changed are transferred, typically a tenth of that.

14. Measurement mathematics

14.1 From codes to physics

Per-sample conversion. Z and K come from the calibration record.

Raw	N_i, N_v	12-bit ADC codes for the current and voltage channels	
Volts	$V_i = 4.096 \times N_i / 4096$	$V_v = 4.096 \times N_v / 4096$	
Current	$I = (V_i - Z_i[r]) \times K_i[r]$	$K_i[r] = 1 / (10 \times G_{pga} \times R_{shunt}[r])$	
Voltage	$V = (V_v - Z_v[r]) \times K_v[r]$	$K_v[r] = A[r] / G_{pga}$	
Corrections	$V = V - I \times R_{wire}$	only when 2-wire sensing is selected	
	$I = I - C_{stray} \times dV/dt$	C_{stray} from the fixture cal, typically 40 pF	

14.2 Derived quantities shown at the cursor

Cursor mathematics

Gain, bipolar	$hFE = I_c / I_b$	I_b is the known step value of that curve
Transconductance	$g_m = (I[k+1] - I[k]) / (V_{step}[k+1] - V_{step}[k])$	at constant V_{ce}
Output resistance	$r_o = dV_{ce} / dI_c$	from a 9-point Savitzky-Golay slope on one curve
Early voltage	$V_A = I_c / (dI_c/dV_{ce}) - V_{ce}$	
On resistance	$R_{ds(on)} = V_{ce} / I_c$	evaluated in the triode region, $V_{ce} < 0.1 \times V_r$ range
Threshold	V_{th} = the step value of the first curve whose peak I exceeds 250 uA	
Dynamic R, diode	$r_d = dV / dI$	the same slope estimator, useful for zeners
Dissipation	$P = V_{ce} \times I_c$	shown live so the operator sees the SOA being approached

14.3 Slope estimation

Taking a naive difference between adjacent samples to get a slope amplifies the noise by the sample rate. The firmware uses a nine-point Savitzky-Golay first-derivative filter, which fits a quadratic over nine samples and reports its slope analytically. The coefficients are integers, so the whole thing is a multiply-accumulate over a fixed window.

```
dy/dx ~= sum(c[j] x y[n+j]) / (h x 60),  j = -4..4
c = [-4, -3, -2, -1, 0, 1, 2, 3, 4] x 2  (the SG first derivative kernel for a quadratic,
m = 9)
h = the sample spacing in volts = V_range / 512
Noise gain 0.11 versus 1.0 for a plain difference: a factor of nine improvement.
```

14.4 Averaging

Averaging happens across families, never across the points of one curve, because averaging along a curve would round the knees. Sixteen families take 4.4 seconds and buy a factor of four in noise, which turns the 100 k range from a suggestion into a measurement.

15. Sweep timing

Figure 15 - Sweep timing

One curve family, N = 4 steps shown

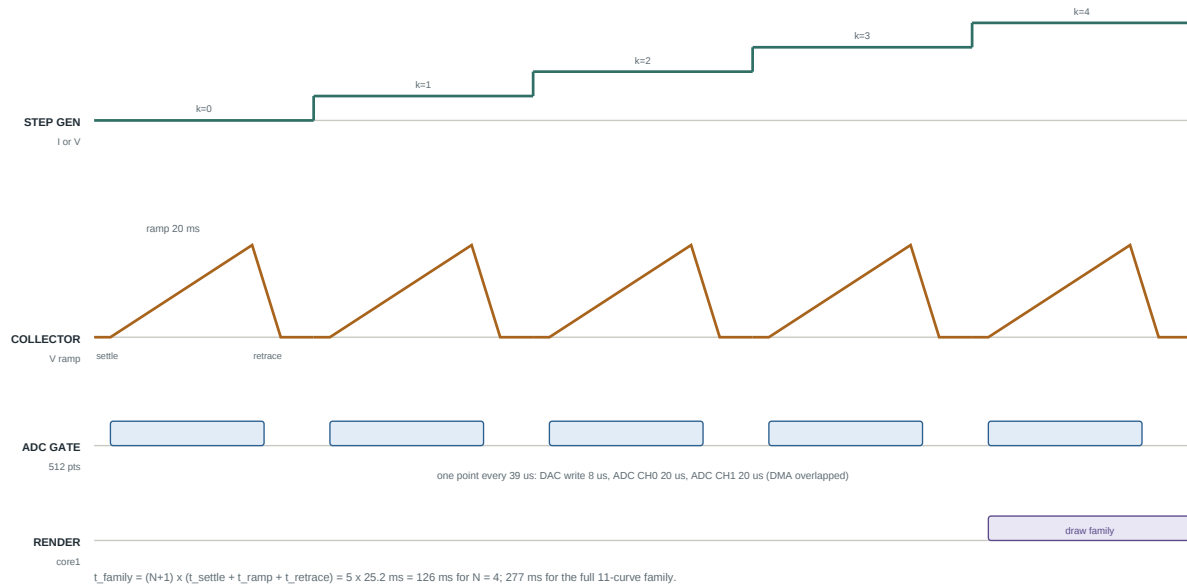


Figure 11 - Timing of one curve family.

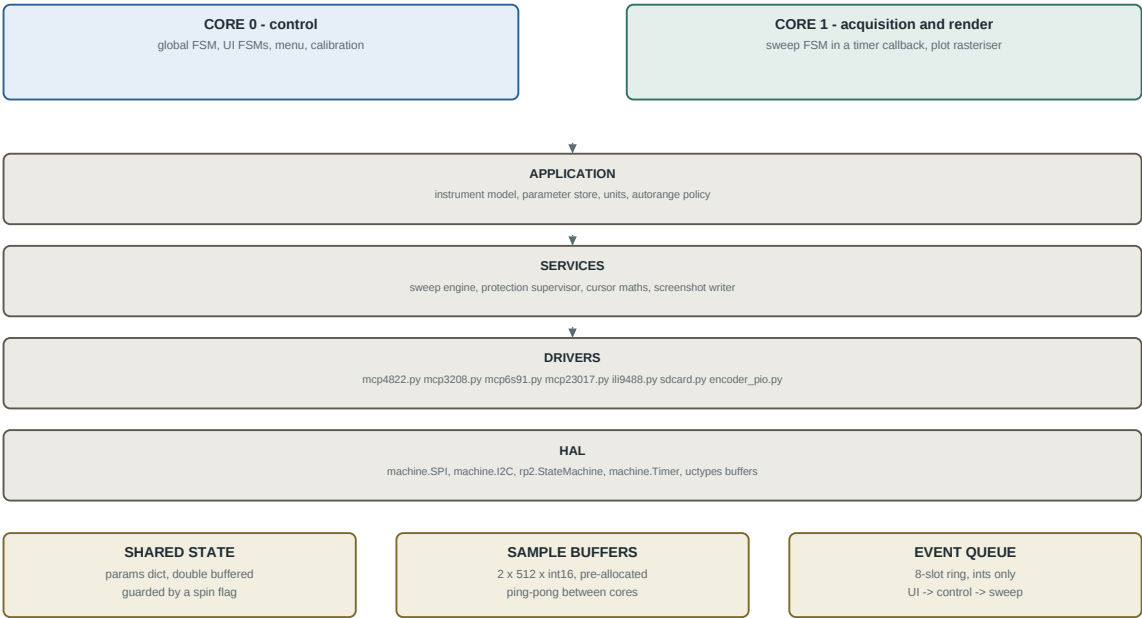
Point budget	$39 \text{ us} = 8 \text{ us DAC write} + 20 \text{ us ADC ch0} + 20 \text{ us ADC ch1, DMA overlapped}$
Ramp	$t_{ramp} = 512 \times 39 \text{ us} = 20.0 \text{ ms}$
Settle	$t_{settle} = \max(200 \text{ us}, 5 \times R_s \times C_{in})$
Retrace	$t_{retrace} = 5 \text{ ms}$, output driven back to zero, ADC idle
Family	$t_{family} = (N + 1) \times (t_{settle} + t_{ramp} + t_{retrace})$ $N = 10 \rightarrow 11 \times 25.2 \text{ ms} = 277 \text{ ms} \rightarrow 3.6 \text{ families per second}$
Duty	$d = t_{ramp} / (t_{ramp} + t_{retrace} + t_{settle}) = 79 \%$ within a step, but the DUT only conducts near the top of the ramp, so mean power is far lower
Thermal guard	if $V_{peak} \times I_{peak} > 5 \text{ W}$ the engine inserts a cool-down gap so that $P_{avg} = P_{peak} \times t_{ramp} / t_{period}$ stays under 5 W

A curve tracer heats the device it measures. The 370 solves this with a rectified sine and a low duty cycle; this design solves it by measuring the peak dissipation of the previous family and stretching the period. The operator sees the update rate drop when probing a power device near its limits, which is the correct feedback.

16. Firmware architecture

Figure 16 - Firmware architecture

MicroPython, two cores, no dynamic allocation in the ISR



Rule: the timer callback allocates nothing, calls no I2C and touches only pre-allocated buffers. Range changes are requested through the event queue and applied between families.

Figure 12 - Firmware layering and core split.

MicroPython on the RP2040 is fast enough for this instrument provided one rule is respected: the sweep callback must not allocate. Every buffer is pre-allocated at boot, the ADC and DAC drivers write into memoryview slices of those buffers, and the callback is decorated so that it never triggers the garbage collector. Breaking that rule shows up as a jitter spike of several milliseconds in the middle of a ramp, which looks exactly like a glitchy DUT and wastes an evening.

16.1 Module map

Module	Responsibility	Runs on
main.py	boot, self test, hand off to the global FSM	core 0
fsm_global.py	the instrument state machine of section 18.1	core 0
fsm_ui.py	button, encoder and navigation machines	core 0
params.py	parameter model, ranges, formatting, units	core 0
sweep.py	sweep engine state machine and the timer callback	core 1
protect.py	supervisor, trip logic, foldback	core 1, checked per sample
render.py	graticule, traces, readout, cursor	core 1
cursor.py	cursor maths, hFE, gm, slopes	core 0
cal.py	calibration record, EEPROM read and write	core 0
storage.py	PNG and CSV writer to microSD	core 0
drivers/	mcp4822, mcp3208, mcp6s91, mcp23017, ili9488, sdcard, encoder_pio	both

Table 10 - Firmware module map.

16.2 Inter-core contract

- Core 0 writes the parameter block, core 1 reads it. A single integer flag is toggled after a coherent write; core 1 only reads the block when the flag is stable across two reads.
- Core 1 writes sample buffers, core 0 reads them. Two buffers, ping-pong, with an index published after the family completes.
- Range changes travel as events, not as direct calls, because they involve I2C and relays and must never happen during a ramp.
- The only shared mutable state is those three objects. Everything else is private to a core.

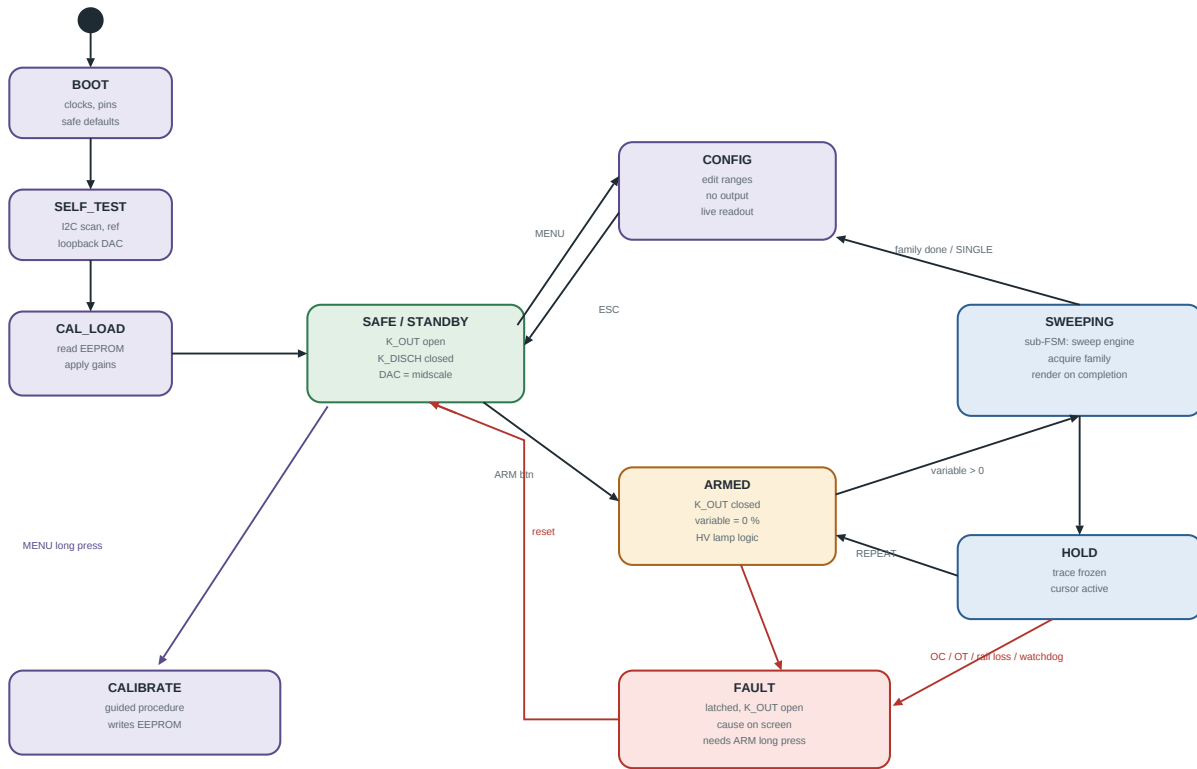
17. State machines

Four machines run concurrently. The global machine owns the instrument's safety and mode. The sweep engine owns acquisition. The protection supervisor owns the trip logic. The interface machines own the operator's intent. They communicate only through the event queue described in section 16.2.

17.1 Global state machine

Figure 11 - Global state machine

One instance, runs in the main loop at 100 Hz



Any state: a disarm event (ARM button, fault, lid switch, watchdog) forces SAFE within 10 ms. The transition is also wired in hardware through GP27.

Figure 13 - Global state machine.

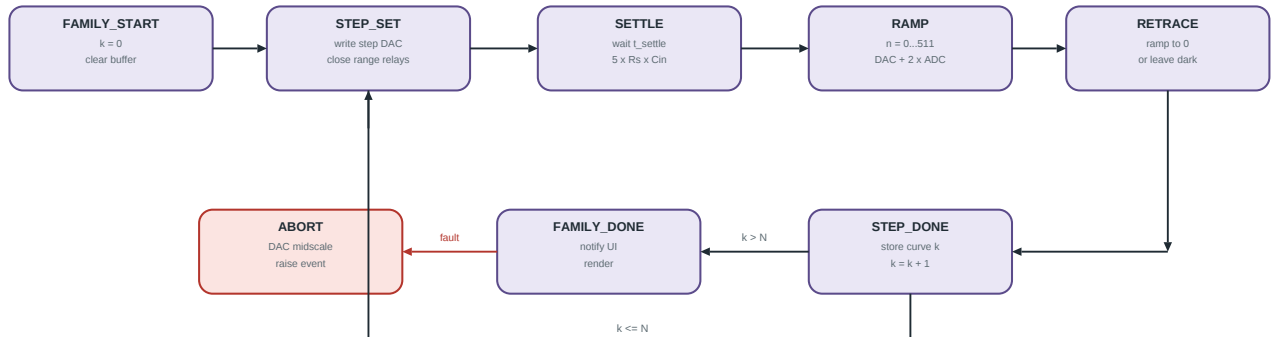
State	Entry action	Exit condition	Next state
BOOT	clocks, pin defaults, GP27 low, WDT armed	init complete	SELF_TEST
SELF_TEST	I2C scan, DAC loopback via ADC, reference check, rail check	all pass / any fail	CAL_LOAD / FAULT
CAL_LOAD	read 24LC256, verify CRC, apply gains	done / bad CRC	SAFE / SAFE with warning
SAFE	K_OUT open, K_DISCH closed, DACs to midscale, ARM lamp off	MENU / ARM pressed	CONFIG / ARMED
CONFIG	menu overlay, sources still disabled	ESC or 20 s timeout	SAFE
ARMED	K_OUT closed, K_DISCH open, variable forced to 0 %, HV lamp logic live	variable > 0 / ARM pressed	SWEEPING / SAFE
SWEEPING	start the sweep engine, BUSY lamp on	family done in SINGLE / ARM / fault	HOLD / SAFE / FAULT
HOLD	trace frozen, cursor enabled	REPEAT selected / ARM	SWEEPING / SAFE
FAULT	K_OUT open, K_DISCH closed, FAULT lamp, cause card on screen	ARM long press after cooldown	SAFE
CALIBRATE	guided sequence, writes EEPROM	finished or aborted	SAFE

Table 11 - Global state table. Any fault event forces FAULT from any state within 10 ms.

17.2 Sweep engine

Figure 12 - Sweep engine state machine

Runs from a hardware timer; one pass produces one curve family



Timing parameters

t_settle	5 x Rs x Cin_dut, floor 200 us	gate or base charging before the ramp starts
N_points	512 per ramp	one DAC write + two ADC reads per point
f_sample	25.6 kS/s point rate	39 us budget: 8 us DAC + 2 x 20 us ADC overlapped by DMA
t_ramp	20 ms	512 / 25.6 kS/s
t_family	11 curves x (0.2 + 20 + 5) ms = 277 ms	well under the 3 Hz refresh the eye needs
duty	t_ramp / t_period <= 15 %	period stretched automatically when P_dut is high
dV/dt	24 V / 20 ms = 1.2 kV/s	Icap = C x dV/dt = 120 nA for 100 pF, subtract in software

Figure 14 - Sweep engine state machine and its timing parameters.

State	Action	Duration	Leaves when
FAMILY_START	k = 0, select buffer, clear the over-range flags	under 1 ms	immediately
STEP_SET	compute I(k) or V(k), write the step DAC, apply any queued range change	50 us plus I2C if a relay moved	DAC written
SETTLE	hold, sources stable, ADC idle	t_settle	timer expires
RAMP	512 iterations of write-DAC, read-I, read-V, run the protection check	20 ms	n = 512 or a trip
RETRACE	ramp the collector DAC back to midscale in 128 steps	5 ms	timer expires
STEP_DONE	commit the curve, k = k + 1	under 1 ms	k <= N / k > N
FAMILY_DONE	publish the buffer index, signal core 0, apply autorange if enabled	under 1 ms	always to FAMILY_START or idle
ABORT	collector DAC to midscale, step DAC to midscale, raise a fault event	under 100 us	always to the protection FSM

Table 12 - Sweep engine state table.

17.3 Protection supervisor

Figure 13 - Protection and limiter state machine
Hardware latch plus firmware supervision, evaluated every ADC point

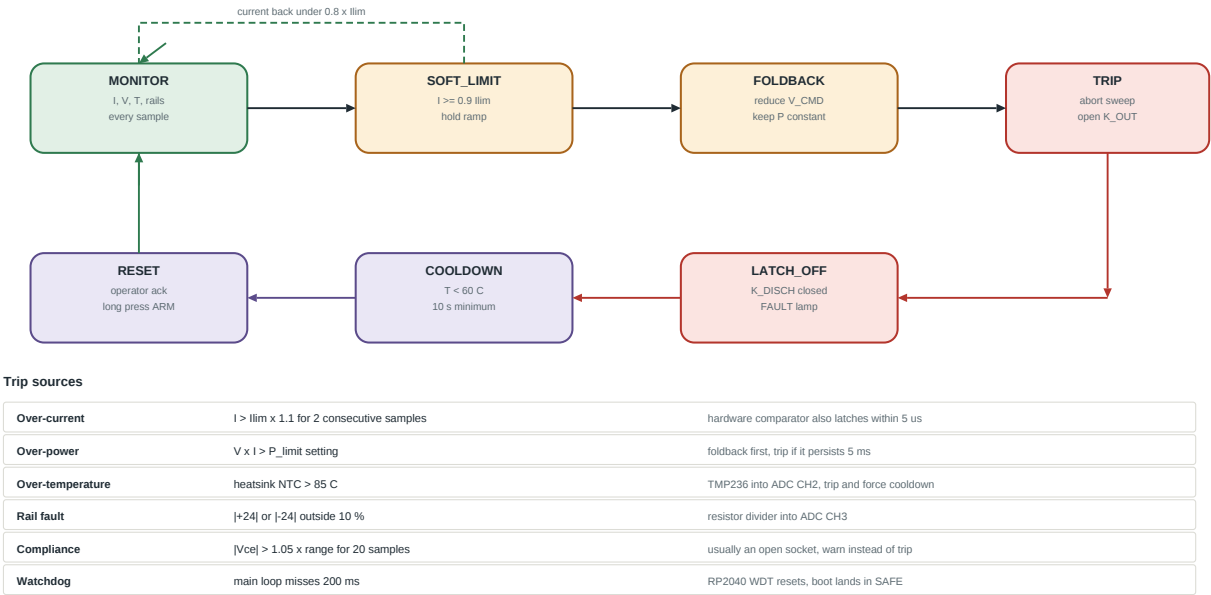


Figure 15 - Protection state machine and trip sources.

The supervisor runs inside the sweep loop, on every sample, and it is deliberately simple: three comparisons and a counter. Anything more elaborate would not fit in the 39 microsecond budget. The sophisticated decisions - what the power limit should be, whether to warn the operator - happen between families where there is time.

State	Meaning	Action	Recovery
MONITOR	normal operation	compare I, V, T against limits each sample	n/a
SOFT_LIMIT	current within 10 % of the limit	hold the ramp code, stop advancing	current falls below 0.8 x limit
FOLDBACK	power limit exceeded	reduce the command to hold $V \times I$ constant	power falls below the setting
TRIP	hard limit or persistent foldback	abort the sweep, open K_OUT	goes to LATCH_OFF
LATCH_OFF	instrument unsafe	K_DISCH closed, FAULT lamp, cause recorded	operator acknowledges
COOLDOWN	thermal trip only	wait for under 60 C and at least 10 s	automatic
RESET	acknowledged	clear the latch, reload ranges	returns to MONITOR via SAFE

Table 13 - Protection state table.

17.4 Interface machines

Figure 14 - Human interface state machines

One button FSM per key, one encoder FSM per shaft, one navigation FSM

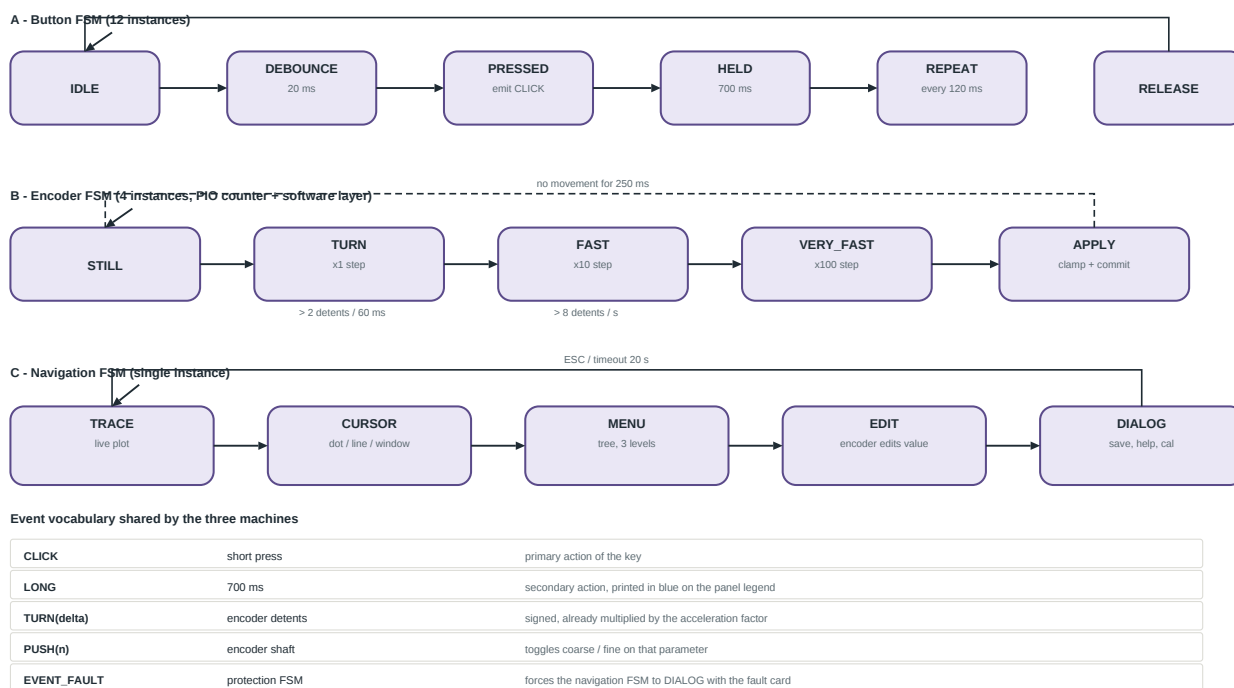


Figure 16 - Button, encoder and navigation state machines.

Twelve button machines and four encoder machines run from a 10 ms tick. They are pure functions of their input plus a timer, they emit events, and they never touch hardware. The navigation machine consumes those events and is the only thing that changes a parameter.

Machine	Instances	Tick	Emits
Button	12	10 ms	CLICK, LONG, REPEAT, RELEASE
Encoder	4	10 ms, count read from PIO	TURN(delta, accel), PUSH
Navigation	1	event driven	parameter changes, mode changes, dialog open and close
Autorange	1	once per family	range change requests into the sweep queue

Table 14 - Interface machine summary.

Autorange policy

- If the peak current of the family exceeds 95 % of range, step one range up immediately.
- If it stays below 8 % of range for three consecutive families, step one range down.
- Never change range while the cursor is being dragged - the reading would jump under the operator's finger.
- The same hysteresis applies to the voltage channel, using 2.2 V as the LO / HI boundary.
- Autorange is off by default in SINGLE mode, because a captured trace should not move.

18. Calibration

Calibration turns a pile of tolerant components into an instrument. The procedure is two-point per range - zero and full scale - and it lives in the firmware as a guided sequence, because asking the operator to remember the order is asking for a bad calibration.

18.1 Record layout

Field	Size	Content
magic	4 B	'PT37' identifies a valid record
version	2 B	record format version
date	4 B	unix time of the calibration
i_zero[7]	28 B	float, ADC volts at zero current for each shunt range
i_gain[7]	28 B	float, correction factor per shunt range
pga_gain[8]	32 B	float, measured gain of each PGA setting
v_zero[2]	8 B	float, ADC volts at zero volts, HI and LO
v_gain[2]	8 B	float, correction factor, HI and LO
dac_c[2]	8 B	float, collector DAC offset and slope
dac_s[2]	8 B	float, step DAC offset and slope
c_stray	4 B	float, fixture stray capacitance in farads
r_wire	4 B	float, fixture wiring resistance in ohm
crc32	4 B	over everything above

Table 15 - Calibration record, 142 bytes, stored twice in the 24LC256 for redundancy.

18.2 Procedure

1. **Warm up** 20 minutes with the instrument armed and no DUT. Offsets drift most in the first ten minutes.
2. **Zero the current channel.** Socket empty, K_OUT closed, collector DAC at midscale. For each of the seven shunt ranges and each PGA gain, average 1024 ADC samples and store the result as i_zero. This takes about 30 seconds.
3. **Gain the current channel.** Fit a 0.05 % reference resistor between C and E - 100 ohm for the high ranges, 100 k for the low ones. Sweep to a known voltage, compute the expected current from Ohm's law, and store the ratio as i_gain.
4. **Zero the voltage channel.** Short C to E with a link, sweep, and store the residual as v_zero for both attenuator ranges.
5. **Gain the voltage channel.** Apply the collector supply to an open socket and compare the reading with a 5.5-digit meter at 1 V, 10 V and 20 V. A straight-line fit gives v_gain.
6. **Characterise the DACs.** With the socket open, step the collector DAC across its range and record the measured voltage. Offset and slope go into dac_c; repeat through a 1 k load for dac_s.
7. **Measure the fixture strays.** Socket open, fastest ramp, most sensitive current range. The current that appears is C_stray x dV/dt; solve for C_stray. Typically 30 to 60 pF.
8. **Measure the wiring resistance.** Short the socket, force 1 A, read the voltage on the HI range with 2-wire sensing selected. r_wire is the quotient.
9. **Write and verify.** Store both copies, read them back, compare CRCs.

Calibration is only as good as the reference. A 0.05 % resistor and a 5.5-digit meter give an instrument accurate to about 0.3 %. Without them, calibrate against a known-good transistor and accept 2 %, which is still perfectly useful for matching and for go / no-go work.

19. Bill of materials

Ref	Part	Qty	Notes
U1	Raspberry Pi Pico or Pico 2	1	Pico 2 gives more RAM for a full frame buffer
U2, U3	MCP4822	2	dual 12-bit DAC, internal 2.048 V reference
U4	MCP3208	1	8-channel 12-bit ADC, 100 kS/s
U5, U6	MCP6S91	2	SPI programmable gain amplifier
U7-U9	MCP23017	3	I2C 16-bit expanders, addresses 0x20 to 0x22
U10	24LC256	1	calibration EEPROM
U11	REF3040	1	4.096 V, 0.2 %, 8 ppm/C
U12, U13	OPA2197	2	difference amplifiers, current and voltage chains
U14	OPA197	1	collector supply driver
U15	OPA197	1	Howland pump
U16	OPA2197	1	step summing and gate driver
U17	LM393	1	limit comparator
U18, U19	74HCT125, 74LVC125	2	level translation
U20, U21	ULN2803A	2	relay and lamp drivers
Q1, Q2	MJE15032 / MJE15033	1 pair	pass devices, TO-220, on a common heatsink
Q3, Q4	2N3904 / 2N3906	1 pair	current limit sensing
Q5	2N3904	1	Vbe multiplier, thermally coupled to the pass devices
SW1-SW4	DG408, DG409 x2, DG419 x3	6	analog range switching
K1-K16	TQ2-5V reed relays	16	series R, shunts, socket, discharge, output
ENC1-4	24 ppr detented encoder with push	4	panel
SW	6 mm tactile with cap	12	panel
DS1-4	3 mm LED, red and amber	4	panel lamps
LCD	3.5 inch 480x320 ILI9488 SPI	1	with microSD socket
R_sh	0.1, 1, 10, 100 ohm 0.1 % 3 W; 1k, 10k, 100k 0.1 %	7	current shunts
R_ser	0.5 ohm 5 W, 5 ohm 2 W, 50, 500, 5k 0.5 W	5	series bank
-	0.05 % thin film network for the Howland	1	the single most critical passive
-	0.1 % matched divider network 240k / 20k	2	voltage attenuator
PSU	24 V 1.5 A isolated brick	2	series connected for +/-24 V
-	6800 uF 35 V	2	rail reservoirs
-	1.5KE33CA TVS, 2 A fuses, BAV99	-	protection

Table 16 - Bill of materials. Passive support components are not itemised.

20. Bring-up and test plan

Build and test in this order. Each step ends with a measurement that must pass before the next board section is populated. Skipping ahead is how pass transistors die.

Step	Populate	Test	Pass criterion
1	Power section only	Measure all rails unloaded and at 50 % load	+/-24 V +/-5 %, +/-15 V +/-2 %, 5 V +/-2 %, ripple under 20 mV
2	Pico, LCD, SD	Boot MicroPython, draw a test pattern, list the card	clean pattern at 40 MHz, no tearing
3	I2C expanders	Scan the bus, toggle every output bit	0x20, 0x21, 0x22, 0x50 respond
4	Reference and ADC	Read a divider from the reference on every channel	reading within 0.5 % of the calculated value, noise under 2 LSB rms
5	DACs and level shift	Ramp both DACs, measure with a meter	monotonic, endpoints within 1 %
6	Collector amp, no pass devices	Drive a 10 k load from the op-amp alone	+/-24 V swing, no oscillation on a scope with a 10 nF load
7	Pass devices, current limit	Short the output through a 1 ohm 10 W resistor briefly	current limits at 1.3 to 1.45 A, no thermal runaway
8	Shunt bank	Force known currents, read every range	each range within 1 % before calibration
9	Voltage chain	Apply known voltages, both ranges	within 1 % before calibration, CMRR better than 60 dB
10	Step generator	Load each range with a resistor, measure the current	within 1 %, output impedance over $100 \times R_s$
11	Fixture and relays	Cycle every relay, check break-before-make on a scope	no overlap, under 5 ms transitions
12	First device	A 2N3904 on the 10 ohm shunt, 10 uA steps	a recognisable family with hFE between 100 and 300
13	Calibration	Run the full section 18 procedure	record written, CRC verified
14	Soak	Two hours sweeping a power MOSFET at 5 W	heatsink under 70 C, no drift over 1 %

Table 17 - Bring-up sequence.

20.1 Known difficulties

- **Oscillation in the composite amplifier.** If the output rings on a step, increase the compensation capacitor across R_f and check that the Zobel network is physically at the output pin, not two centimetres away.
- **A curve that hooks upward near zero volts.** That is the fixture stray capacitance times dV/dt . Calibrate it out or slow the ramp.
- **A noisy 100 k range.** Almost always ground loops. Verify that AGND and PGND meet at exactly one point and that the shunt Kelvin pair is a twisted or closely routed pair.
- **Steps that are not equal.** Howland resistor mismatch. Measure the output impedance directly by loading the step output with 1 k and then 10 k and comparing the currents.
- **The display tears during a sweep.** The SPI transfer is competing with the timer callback. Move rendering entirely to core 1 and push only complete buffers.

Appendix A. Formula summary

SOURCES

$$\begin{aligned}
 V_{\text{dac}} &= 2.048 \times D / 4096 \times 2 \\
 V_{\text{cmd}} &= -G \times (V_{\text{dac}} - 2.048), \quad G = 1.25 \mid 5.0 \mid 11.72 \\
 V_{\text{ce}} &= V_{\text{cmd}} - I \times (R_{\text{series}} + R_{\text{shunt}}) \\
 I_{\text{step}} &= (V_{\text{cmd}} - V_{\text{e}}) / R_{\text{s}}, \quad R_{\text{s}} = 100 \mid 1\text{k} \mid 10\text{k} \mid 100\text{k} \mid 1\text{M} \\
 V_{\text{gate}} &= k \times (V_{\text{dac}} - 2.048), \quad k = 1.25 \mid 5.0
 \end{aligned}$$

MEASUREMENT

$$\begin{aligned}
 I &= (V_{\text{adc}_i} - Z_i) / (10 \times G_{\text{pga}} \times R_{\text{shunt}}) \\
 V &= (V_{\text{adc}_v} - Z_v) \times A / G_{\text{pga}}, \quad A = 1.2 \mid 12 \\
 \text{LSB}_I &= 4.096 / (4096 \times 10 \times G_{\text{pga}} \times R_{\text{shunt}}) \\
 \text{LSB}_V &= 4.096 \times A / (4096 \times G_{\text{pga}})
 \end{aligned}$$

DEVICE PARAMETERS

$$\begin{aligned}
 h_{\text{FE}} &= I_{\text{c}} / I_{\text{b}} \\
 g_{\text{m}} &= dI_{\text{d}} / dV_{\text{gs}} \text{ at constant } V_{\text{ds}} \\
 r_{\text{o}} &= dV_{\text{ce}} / dI_{\text{c}} \\
 V_{\text{A}} &= I_{\text{c}} / (dI_{\text{c}}/dV_{\text{ce}}) - V_{\text{ce}} \\
 R_{\text{ds(on)}} &= V_{\text{ds}} / I_{\text{d}} \text{ in the triode region}
 \end{aligned}$$

PROTECTION AND THERMAL

$$\begin{aligned}
 I_{\text{lim}} &= V_{\text{be}} / R_{\text{e}} = 0.65 / 0.47 = 1.38 \text{ A} \\
 I_{\text{lim}}(V) &= P_{\text{set}} / \max(|V_{\text{ce}}|, 0.25) \\
 P_{\text{q}} &= (V_{\text{rail}} - V_{\text{ce}}) \times I \\
 T_{\text{j}} &= T_{\text{a}} + P \times (R_{\text{th}_{\text{jc}}} + R_{\text{th}_{\text{cs}}} + R_{\text{th}_{\text{sa}}}) \\
 P_{\text{avg}} &= P_{\text{peak}} \times t_{\text{ramp}} / t_{\text{period}}
 \end{aligned}$$

TIMING

$$\begin{aligned}
 t_{\text{point}} &= 39 \text{ us}, \quad t_{\text{ramp}} = 512 \times t_{\text{point}} = 20 \text{ ms} \\
 t_{\text{settle}} &= \max(200 \text{ us}, 5 \times R_{\text{s}} \times C_{\text{in}}) \\
 t_{\text{family}} &= (N + 1) \times (t_{\text{settle}} + t_{\text{ramp}} + t_{\text{retrace}}) \\
 I_{\text{stray}} &= C_{\text{stray}} \times dV/dt = C_{\text{stray}} \times V_{\text{range}} / t_{\text{ramp}}
 \end{aligned}$$

Appendix B. Connector pinouts

Connector	Pin	Signal	Note
J1 fixture	1	COLLECTOR	from the series R bank, 2 A rating
	2	BASE / GATE	from the step generator, 100 ohm in series
	3	EMITTER	to the shunt bank high side
	4	SENSE+	collector Kelvin, no current
	5	SENSE-	emitter Kelvin, step generator reference
	6	GUARD	driven guard for the low current ranges, tied to SENSE-
J2 panel	1-8	ENC1_A .. ENC4_B	ribbon to the encoder board
	9	3V3	encoder pull-up supply

Connector	Pin	Signal	Note
	10	DGND	
J3 panel I2C	1-4	SDA, SCL, 3V3, DGND	to MCP23017 #1 and #3
J4 relay	1-16	K_OUT, K_DISCH, K1-K5, K_SH1-7, K_SOCKET L/R	to the ULN2803 outputs
J5 display	1-8	SCK, MOSI, MISO, /CS_LCD, DC, RST, BL, /CS_SD	plus 3V3 and DGND
J6 power in	1-3	+24 V, AGND, -24 V	from the series-connected bricks

Table 18 - Connector pinouts.

Appendix C. Range tables

Vertical, A/div	Shunt	PGA	Full scale (10 div)	Resolution
1 uA/div	100 k	8	10 uA	1.2 nA
10 uA/div	10 k	8	100 uA	12 nA
100 uA/div	1 k	8	1 mA	0.12 uA
1 mA/div	100 ohm	8	10 mA	1.2 uA
10 mA/div	10 ohm	8	100 mA	12 uA
100 mA/div	1 ohm	8	1 A	0.12 mA
200 mA/div	0.1 ohm	16	2 A	0.25 mA

Table 19 - Vertical ranges. Intermediate 2 and 5 steps are obtained with PGA gains 4 and 2.

Horizontal, V/div	Attenuator	PGA	Full scale	Resolution
50 mV/div	1.2	8	0.5 V	0.15 mV
100 mV/div	1.2	4	1 V	0.3 mV
200 mV/div	1.2	2	2 V	0.6 mV
500 mV/div	12	8	5 V	1.5 mV
1 V/div	12	4	10 V	3 mV
2 V/div	12	2	20 V	6 mV
5 V/div	12	1	50 V, clipped at 24 V	12 mV

Table 20 - Horizontal ranges.

Step amplitude	Mode	R_s or gain	Max step x 10	Typical device
0.5 uA/step	current	1 M	5 uA	high beta small signal
1 uA/step	current	1 M	10 uA	small signal BJT
10 uA/step	current	100 k	100 uA	general purpose BJT
100 uA/step	current	10 k	1 mA	medium power BJT
1 mA/step	current	1 k	10 mA	power BJT, darlington
4 mA/step	current	100 ohm	40 mA	power BJT at high current
50 mV/step	voltage	x1.25	0.5 V	JFET
250 mV/step	voltage	x1.25	2.5 V	logic level MOSFET
1 V/step	voltage	x5	10 V	standard MOSFET, IGBT

Table 21 - Step generator ranges.

End of document. Revision 1.0, design release. The firmware specified in sections 16 and 17 is not included and is expected to be developed against this document.